EPSON

S1C63256

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Low Current Consumption
- Wide-range Operating Voltage (2.7V to 5.5V)
- High Speed Operation in Low Voltage

■ DESCRIPTION

The S1C63256 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (6,144 words × 13 bits), RAM (256 words × 4 bits), clock timer, watchdog timer, programmable timer, an LCD driver that can drive a maximum 20 segments × 4 commons and A/D converter built-in. It features a wide operating voltage (2.7 to 5.5 V) and operating frequency (0.5 to 4.5 MHz), and is most suitable for applications such as control units for the household electric appliances which need A/D conversion and liquid crystal display.

■ FEATURES

- Oscillation circuit ..... 0.5 to 4.5 MHz
  Crystal, ceramic, CR oscillation circuit or external clock input (∗1)
- Instruction set ..... Basic instruction: 47 types (411 instructions with all)
  Addressing mode: 8 types
- Instruction execution time ..... During operation at 2 MHz: 1 µsec 2 µsec 3 µsec
  During operation at 4.194304 MHz: 0.48 µsec 0.95 µsec 1.43 µsec
- ROM capacity ..... Code ROM: 6,144 words × 13 bits
- RAM capacity ..... Data memory: 256 words × 4 bits
  Display memory: 20 words × 4 bits
- Input port ..... 4 bits (Pull-up resistors may be supplemented ∗1)
- Output port ..... 4 bits (It is possible to switch the 2 bits to clock output ∗2)
- I/O port ..... 8 bits (It is possible to switch the 4 bits to A/D converter input ∗2)
- LCD driver ..... 20 segments × 4, 3 or 2 commons (∗2) 1/3 or 1/2 bias drive (∗1)
- Time base counter ..... Clock timer (when 4.194304 MHz oscillation clock is used)
- Programmable timer ..... Built-in 8 bits × 4 ch, with event counter and clock output function
  Usable for 8 bits × 4 ch, 8 bits × 2 ch & 16 bits × 1 ch or 16 bits × 2 ch
- Watchdog timer ..... Built-in
- Buzzer output ..... Buzzer frequency: 2 kHz or 4 kHz (∗2)
- A/D converter ..... Resolution: 8 bits, analog input: 4 ch
- External interrupt ..... Input port interrupt: 1 system
- Internal interrupt ..... Clock timer interrupt: 1 system
  Programmable timer interrupt: 4 systems
  A/D converter interrupt: 1 system
- Power supply voltage ..... 2.7 V to 5.5 V
- Operating temperature range ..... -20°C to 85°C
- Current consumption (Typ.) ..... During SLEEP 0.3 µA
  During HALT (∗3)

4.194304 MHz:	3.0 V	620 µA
(Crystal oscillation)	5.0 V	660 µA
4 MHz:	3.0 V	670 µA
(Ceramic oscillation)	5.0 V	710 µA
2 MHz:	3.0 V	740 µA
(CR oscillation)	5.0 V	780 µA

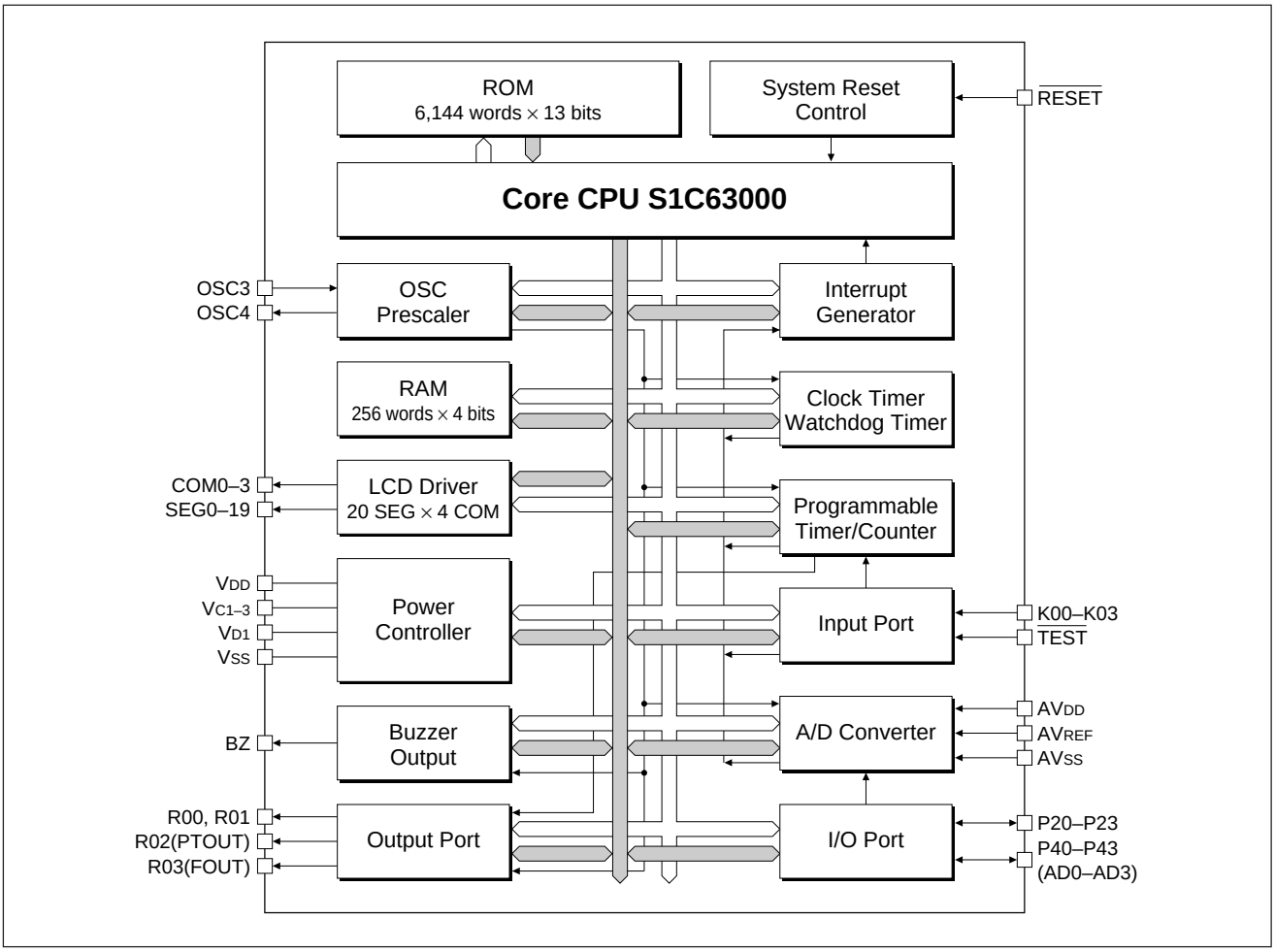
During operation (∗3)

4.194304 MHz:	3.0 V	1.5 mA
(Crystal oscillation)	5.0 V	1.5 mA
4 MHz:	3.0 V	1.5 mA
(Ceramic oscillation)	5.0 V	1.5 mA
2 MHz:	3.0 V	1.2 mA
(CR oscillation)	5.0 V	1.2 mA

● Package ..... QFP13-64pin (plastic) or chip

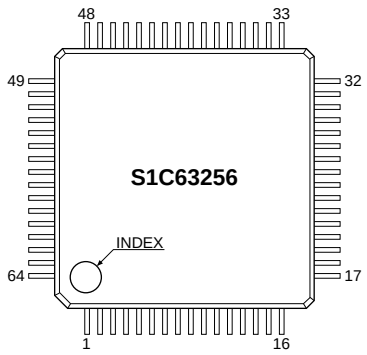
∗1: Can be selected with mask option. ∗2: Can be selected with software.
∗3: A/D converter operating current is not included.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP13-64pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG13	17	$\overline{\text{RESET}}$	33	N.C.	49	COM2
2	SEG14	18	$\overline{\text{TEST}}$	34	BZ	50	COM3
3	SEG15	19	V_{SS}	35	R00	51	SEG0
4	SEG16	20	OSC3	36	R01	52	SEG1
5	SEG17	21	OSC4	37	R02	53	SEG2
6	SEG18	22	V_{D1}	38	R03	54	SEG3
7	SEG19	23	V_{DD}	39	P20	55	SEG4
8	N.C.	24	AV_{DD}	40	P21	56	SEG5
9	N.C.	25	AV_{REF}	41	P22	57	SEG6
10	N.C.	26	AV_{SS}	42	P23	58	SEG7
11	N.C.	27	N.C.	43	K00	59	SEG8
12	N.C.	28	N.C.	44	K01	60	SEG9
13	N.C.	29	P40	45	K02	61	SEG10
14	V_{C1}	30	P41	46	K03	62	SEG11
15	V_{C2}	31	P42	47	COM0	63	SEG12
16	V_{C3}	32	P43	48	COM1	64	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	23	–	Power (+) supply pin
V_{SS}	19	–	Power (–) supply pin
AV_{DD}	24	–	Power (+) supply pin for analog circuit system
AV_{SS}	26	–	Power (–) supply pin for analog circuit system
AV_{REF}	25	I	Reference voltage input pin for analog circuit system
V_{D1}	22	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}, V_{C2}, V_{C3}	14, 15, 16	–	LCD system power supply pin 1/3 or 1/2 bias (selected by mask option)
OSC3	20	I	Crystal/ceramic/CR oscillation/external clock input pin (selected by mask option)
OSC4	21	O	Crystal/ceramic/CR oscillation output pin (selected by mask option)
K00–K03	43–46	I	Input port
P20–P23	39–42	I/O	I/O port
P40–P43	29–32	I/O	I/O port (switching to A/D converter input is possible by software)
R00	35	O	Output port
R01	36	O	Output port
R02	37	O	Output port (switching to PTOUT signal output is possible by software)
R03	38	O	Output port (switching to FOUT signal output is possible by software)
COM0–COM3	47–50	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG19	51–63, 1–7	O	LCD segment output pin
BZ	34	O	Buzzer output pin
$\overline{\text{RESET}}$	17	I	Initial reset input pin
$\overline{\text{TEST}}$	18	I	Testing input pin

■ OPTION LIST

1 OSC SYSTEM CLOCK

☐ 1. X'tal
☐ 2. Ceramic
☐ 3. CR
☐ 4. External Clock

2 MULTIPLE KEY ENTRY RESET COMBINATION

☐ 1. Not Use
☐ 2. Use <K00, K01, K02, K03>
☐ 3. Use <K00, K01, K02>
☐ 4. Use <K00, K01>

3 MULTIPLE KEY ENTRY RESET TIME AUTHORIZE

☐ 1. Not Use
☐ 2. Use

4 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct

5 OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R01	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R02	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R03	☐ 1. Complementary	☐ 2. Nch-OpenDrain

6 I/O PORT OUTPUT SPECIFICATION

• P20	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P21	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P22	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P23	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P40	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P41	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P42	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P43	☐ 1. Complementary	☐ 2. Nch-OpenDrain

7 I/O PORT PULL UP RESISTOR

• P20	☐ 1. With Resistor	☐ 2. Gate Direct
• P21	☐ 1. With Resistor	☐ 2. Gate Direct
• P22	☐ 1. With Resistor	☐ 2. Gate Direct
• P23	☐ 1. With Resistor	☐ 2. Gate Direct
• P40	☐ 1. With Resistor	☐ 2. Gate Direct
• P41	☐ 1. With Resistor	☐ 2. Gate Direct
• P42	☐ 1. With Resistor	☐ 2. Gate Direct
• P43	☐ 1. With Resistor	☐ 2. Gate Direct

8 LCD DRIVING POWER

☐ 1. Internal Power Voltage (VC3=External Power Voltage)
☐ 2. Internal Power Voltage (VC3=VDD)
☐ 3. External Power Voltage
☐ 4. Not Use

9 LCD DRIVING BIAS

☐ 1. Internal Power Voltage 1/3 Bias
☐ 2. Internal Power Voltage 1/2 Bias
☐ 3. External Power Voltage 1/3 Bias
☐ 4. External Power Voltage 1/2 Bias
☐ 5. Not Use

10 BUZZER POLARITY FOR OUTPUT

☐ 1. Positive
☐ 2. Negative

11 /RESET PULL UP RESISTOR

☐ 1. With Resistor
☐ 2. Gate Direct

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Condition	Value	Unit	Note
Supply voltage	V_{DD}		-0.3 to +7.0	V	
LCD supply voltage	V_C		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD}+0.3	V	
Output voltage	V_O		-0.3 to V_{DD}+0.3	V	1
High-level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low-level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Operating temperature	Topr		-20 to +85	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	
Permissible disspation	P_D		250	mW	2

Note) 1. It is applied to the output voltage when Nch open drain is selected by mask option.
2. In case of plastic package.

● Recommended Operating Conditions

(V_{SS}=AV_{SS}=0V, Ta=-20 to 85°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{DD}		V_{DD}	2.7	3.0/5.0	5.5	V	
LCD supply voltage	V_{C3I}		V_{C3}	2.7		5.5	V	1
	V_{C3E}		V_{C3}	2.7		5.5	V	2
	V_{C2E}	1/3 bias	V_{C2}	Typ. - 0.2	V_{C3}·2/3	Typ. + 0.2	V	2
		1/2 bias	V_{C2}	Typ. - 0.2	V_{C3}·1/2	Typ. + 0.2	V	2
	V_{C1E}	1/3 bias	V_{C1}	Typ. - 0.2	V_{C3}·1/3	Typ. + 0.2	V	2
		1/2 bias	V_{C1}	Typ. - 0.2	V_{C3}·1/2	Typ. + 0.2	V	2
Analog supply voltage	V_{AVDD}		AV_{DD}	2.7		V_{DD}	V	
Analog reference voltage range	V_{REF}		AV_{REF}	2.7		AV_{DD}	V	
Analog input voltage range	V_{IN}		AD0 to AD3 (P40 to P43)	AV_{SS}		AV_{REF}	V	
Operating frequency	f_{OSC}	V_{DD}=2.7 to 5.5V	Crystal oscillation circuit	0.5	4.194	4.5	MHz	3,4
			Ceramic oscillation circuit	0.5	4.0	4.5	MHz	3
			CR oscillation circuit	0.5	2.0	2.5	MHz	3
			External clock input	0.5	4.0	4.5	MHz	3,5

Note) 1. When "Internal power (external V_{C3} is used)" is selected by mask option.
2. When "External power" is selected by mask option.
3. The CPU uses the clock output from the oscillation circuit as the operating clock.
4. Crystal oscillator = 4.194304 MHz
5. When an external clock is input from the OSC3 terminal by setting the mask option, do not connect anything to the OSC4 terminal.

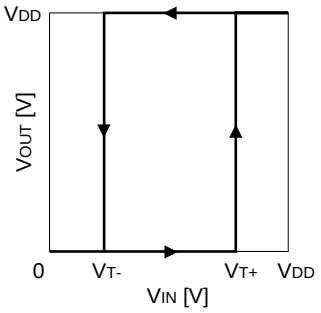
● DC Characteristics

Input Characteristics

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
High-level input voltage	V_{IH1}		Kxx, Pxx	0.7·V_{DD}		V_{DD}	V	
	V_{IH2}		OSC3	1.7		V_{DD}	V	1
Low-level input voltage	V_{IL1}		Kxx, Pxx	0		0.3·V_{DD}	V	
	V_{IL2}		OSC3	0		0.7	V	1
High-level schmitt input voltage	V_{T+}		$\overline{RESET}$	0.5·V_{DD}		0.9·V_{DD}	V	
Low-level schmitt input voltage	V_{T-}			0.1·V_{DD}		0.5·V_{DD}	V	
Input leak current	I_{LIH}	V_{LIH}=V_{DD}	Kxx, Pxx, $\overline{RESET}$	0		1.0	µA	
	I_{LIL}	V_{LIL}=V_{SS}		-1.0		0	µA	
Input pull-up resistance	R_{IN}		Kxx, Pxx	100	250	400	kΩ	2
			$\overline{RESET}$	250	450	650	kΩ	2
Input terminal capacitance	C_{IN}	V_{IN}=0V, f=1MHz	Kxx, Pxx		10	15	pF	

Note) 1. When "External clock" is selected by mask option.
2. When "with pull-up resistor" is selected by mask option.



Output Characteristics

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, V_{C3}=2.7 to 5.5V, V_{C2}/V_{C1} are internal voltage, Ta=-20 to 85°C, C_2=C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
High-level output voltage	I_{OH1}	V_{OH1}=0.9·V_{DD}, V_{DD}=5.0V	Pxx, Rxx		5.3		mA	3
		V_{OH1}=0.9·V_{DD}, V_{DD}=3.0V			2.5		mA	3
	I_{OH2}	V_{OH2}=0.9·V_{DD}, V_{DD}=5.0V	BZ		5.3		mA	3
		V_{OH2}=0.9·V_{DD}, V_{DD}=3.0V			2.5		mA	3
	I_{OH3}	V_{OH3}=0.9·V_{DD}, V_{DD}=5.0V	SEGxx		1.2		mA	1,3
		V_{OH3}=0.9·V_{DD}, V_{DD}=3.0V	(during DC output)		0.6		mA	1,3
Low-level output voltage	I_{OL1}	V_{OL1}=0.1·V_{DD}, V_{DD}=5.0V	Pxx, Rxx		8.5		mA	4
		V_{OL1}=0.1·V_{DD}, V_{DD}=3.0V			4.1		mA	4
	I_{OL2}	V_{OL2}=0.1·V_{DD}, V_{DD}=5.0V	BZ		8.5		mA	4
		V_{OL2}=0.1·V_{DD}, V_{DD}=3.0V			4.1		mA	4
	I_{OL3}	V_{OL3}=0.1·V_{DD}, V_{DD}=5.0V	SEGxx		1.4		mA	1,4
		V_{OL3}=0.1·V_{DD}, V_{DD}=3.0V	(during DC output)		0.7		mA	1,4
Output leak current	I_{LOH}	V_{LOH}=V_{DD}	Pxx, Rxx	0		1.0	µA	
	I_{LOL}	V_{LOL}=V_{SS}		-1.0		0	µA	
Common output current	I_{COMH}	V_{COMH}=V_{C3}-0.05V	COMx			-5	µA	
	I_{COML}	V_{COML}=V_{SS}+0.05V		5			µA	
Segment output current	I_{SEGH}	V_{SEGH}=V_{C3}-0.05V	SEGxx			-5	µA	2
	I_{SEGL}	V_{SEGL}=V_{SS}+0.05V	(during LCD output)	5			µA	2

Note) 1. When "DC output" is selected by mask option.
2. When "LCD output" is selected by mask option.
3. See "Characteristic Curves", for the maximum values.
4. See "Characteristic Curves", for the minimum values.

● Analog Circuit Characteristics

LCD Drive Voltage Characteristics

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, V_{C2}/V_{C1} are internal voltage, Ta=-20 to 85°C, C_2=C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD supply voltage	V_{C3I}		V_{C3}	2.7		5.5	V	1
LCD drive voltage (when 1/3 bias is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} or V_{DD} and V_{C1} (without panel load)		Typ. - 0.2	V_{C3}·1/3	Typ. + 0.2	V	2
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} or V_{DD} and V_{C2} (=V_{C2}) (without panel load)		Typ. - 0.2	V_{C3}·2/3	Typ. + 0.2	V	2
LCD drive voltage (when 1/2 bias is selected)	$V_{C1\&2}$	Connect 1 MΩ load resistor between V_{SS} or V_{DD} and V_{C1}(=V_{C2})(without panel load), V_{C1} and V_{C2} are shorted		Typ. - 0.2	V_{C3}·1/2	Typ. + 0.2	V	2
Built-in resistance	R_{LCD}	Resistance between V_{C3} and V_{SS}		30	50	100	kΩ	2

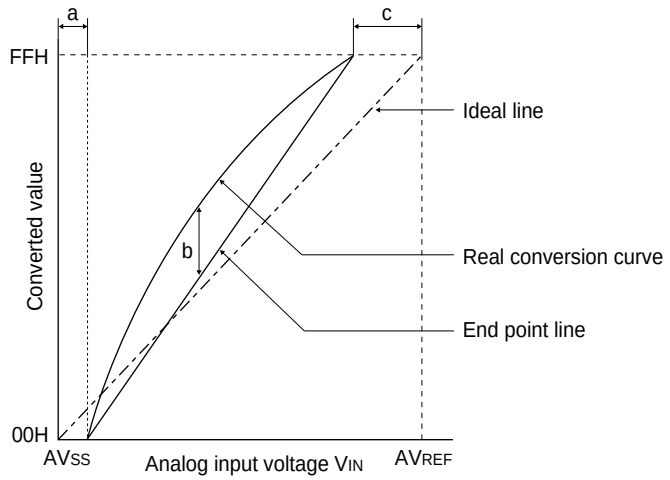
Note) 1. When "Internal power (external V_{C3} is used)" is selected by mask option.
2. V_{C3} = V_{DD} when "Internal power (external V_{C3} is not used)" is selected by mask option.

A/D Conversion Characteristics

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=-20 to 85°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
Analog supply voltage	V_{AVDD}		AV_{DD}	2.7		V_{DD}	V	
Analog reference voltage range	V_{REF}		AV_{REF}	2.7		AV_{DD}	V	
Analog input voltage range	V_{IN}		AD0 to AD3 (P40 to P43)	AV_{SS}		AV_{REF}	V	
Analog input capacitance	C_{AIN}	During sampling	AD0 to AD3 (P40 to P43)		35	60	pF	
Analog reference resistance	R_{REF}	Resistance for AV_{REF}–AV_{SS}		10	20	30	kΩ	
Resolution	–					8	bit	
Offset error	E_{OFF}	AV_{DD}=2.7V to V_{DD}		-1		1	LSB	1
Full scale error	E_{FS}	AV_{REF}=2.7V to AV_{DD}		-1		1	LSB	1
Non-linearity error	E_{LI}	f_{AD}=240kHz to 2.5MHz		-2		4	LSB	1,2
Overall error	E_T			-2		4	LSB	1,2
A/D conversion time	t_{ADC}	f_{AD}=240kHz to 2.5MHz		20		21	clock	1
Sampling time	t_{SMP}	f_{AD}=240kHz to 2.5MHz			8		clock	1

Note) 1. f_{AD}=f_{PRS}=f_{OSC}/2n or f_{AD}=f_{OSC}/2 (f_{AD}: A/D conversion clock frequency, f_{OSC}: oscillation clock frequency, n=1–16: PRSM setting value + 1)
2. The best straight line within a ±3LSB of error can be obtained by correcting the conversion result with -1LSB by software.



Offset error : E_{OFF} = a (the deviation from the ideal value at zero point)
Non-linearity error : E_{LI} = b (the deviation of the real conversion curve from the end point line)
Full scale error : E_{FS} = c (the deviation from the ideal value at the full scale point)

Total error : E_T = max (E_{OFF}, E_{LI}, E_{ABS})
E_{ABS} = the deviation from the ideal line (including quantizing error)

● Current Consumption

(Unless otherwise specified: V_{DD}=AV_{DD}=AV_{REF}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=25°C, C_1=0.1µF, C_2=C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
Power current during SLEEP	I_{SLP}				0.3	1.0	µA	
Power current during HALT	I_{HALT}	LCD system circuit and A/D convertor are not used	Crystal oscillation (4.194304MHz)		560	1200	µA	1,4,7
			Ceramic oscillation (4.0MHz)		610	1400	µA	2,4,7
			CR oscillation (2MHz)		680	1400	µA	3,4,7
			External clock input (4.0MHz)		220	420	µA	4,7
Power current during execution	I_{EXE}	LCD system circuit and A/D convertor are not used Software duty = 100%	Crystal oscillation (4.194304MHz)		1400	2600	µA	1,5,7
			Ceramic oscillation (4.0MHz)		1400	2600	µA	2,5,7
			CR oscillation (2MHz)		1100	2100	µA	3,5,7
			External clock input (4.0MHz)		1000	1700	µA	5,7
LCD system operating current	I_{LCD}	V_{DD}=V_{C3}=3.0V, no panel load			60	100	µA	8
		V_{DD}=V_{C3}=5.0V, no panel load			100	170	µA	8
A/D conversion operating current	I_{ADC}	V_{DD}=AV_{DD}=AV_{DD}=3.0V, f_{AD}=262kHz			600	1000	µA	6
		V_{DD}=AV_{DD}=AV_{DD}=5.0V, f_{AD}=262kHz			1800	3000	µA	6

Note) 1. R_f=1MΩ, C_G=C_D=15pF
2. R_f=1MΩ, C_G=C_D=30pF
3. R_{CR}=20kΩ
4. OSC: oscillated (except for external clock input) CPU, ROM, RAM: HALT status Others: stopped
5. OSC: oscillated (except for external clock input) CPU, ROM, RAM: operating Others: stopped
6. f_{AD}=f_{PRS}=f_{OSC}/2n (f_{AD}: A/D conversion clock frequency, f_{OSC}: oscillation clock frequency, n=1–16: PRSM setting value + 1)
f_{OSC}=4.194304MHz, PRSM=7
7. Current consumption when the LCD system circuit or A/D converter is used is found by adding the LCD system operating current or the A/D conversion current.
8. When "Internal power" is selected by mask option.

● AC Characteristics

Operating Range

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating clock frequency	f_{OSC}	Crystal oscillation circuit	0.5		4.5	MHz	1
		Ceramic oscillation circuit	0.5		4.5	MHz	1
		CR oscillation circuit	0.5		2.5	MHz	1
		External clock input	0.5		4.5	MHz	1,2
Instruction execution time	tcy	1-cycle instruction	0.44 (0.8)		4.0	µS	3
		2-cycle instruction	0.89 (1.6)		8.0	µS	3
		3-cycle instruction	1.33 (2.4)		12.0	µS	3

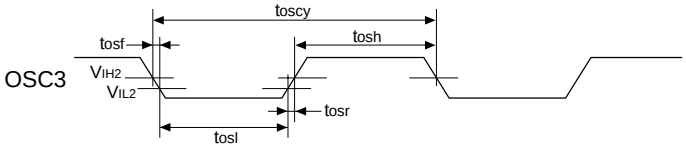
Note) 1. The CPU uses the clock output from the oscillation circuit as the operating clock.
2. When an external clock is input from the OSC3 terminal by setting the mask option, do not connect anything to the OSC4 terminal.
3. The values enclosed with ( ) indicate the execution time when the CR oscillation circuit is used.

Input Clock

• OSC3 external clock

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C, V_{IH2}=1.7V, V_{IL2}=0.7V)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input clock cycle time	toscy		230		2,000	nS	
Input clock "H" pulse width	tosh		115		1,000	nS	
Input clock "L" pulse width	tosl		115		1,000	nS	
Input clock rising time	tosr				25	nS	
Input clock falling time	tosf				25	nS	

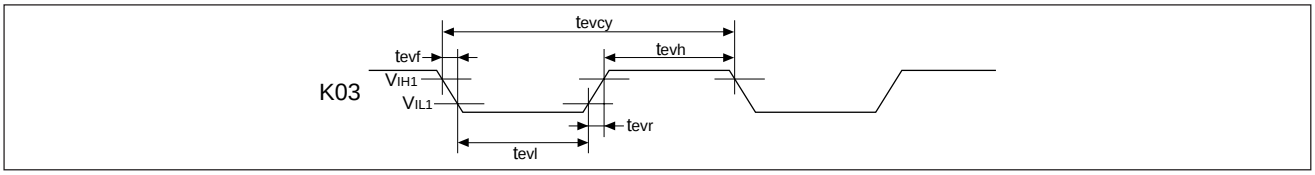


• K03 external clock (event counter external clock)

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C, V_{IH1}=0.8·V_{DD}, V_{IL1}=0.2·V_{DD})

Characteristic	Symbol	Condition	Min.	Max.	Unit	Note
Input clock cycle time	tevcy	With noise rejecter	512·n/fosc		S	1
Input clock "H" pulse width	tevh		256·n/fosc		S	1
Input clock "L" pulse width	tevl		256·n/fosc		S	1
Input clock cycle time	tevcy	Without noise rejecter	4		µS	
Input clock "H" pulse width	tevh		2		µS	
Input clock "L" pulse width	tevl		2		µS	
Input clock rising time	tosr			25	nS	
Input clock falling time	tosf			25	nS	

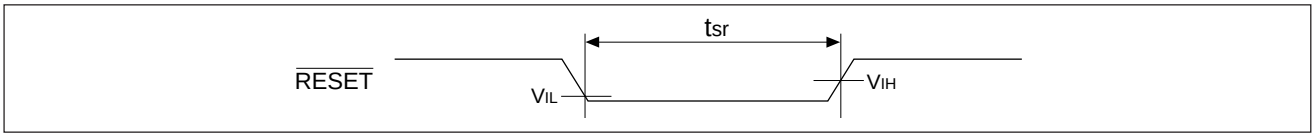
Note) 1. fosc: oscillation clock frequency, n=1–16: PRSM setting value + 1



• $\overline{\text{RESET}}$ input clock

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C, V_{IH}=0.5·V_{DD}, V_{IL}=0.1·V_{DD})

Characteristic	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr		100		µS	

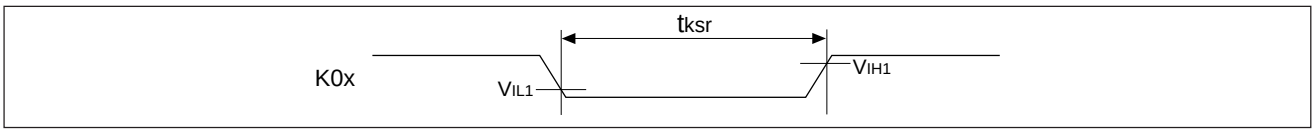


• K00–K03 simultaneous low input clock

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C, V_{IH1}=0.8·V_{DD}, V_{IL1}=0.2·V_{DD})

Characteristic	Symbol	Condition	Min.	Max.	Unit	Note
Simultaneous low input time	tksr	Time authorize circuit is used	524288·n/fosc		S	1
		Time authorize circuit is not used	768·n/fosc		S	1

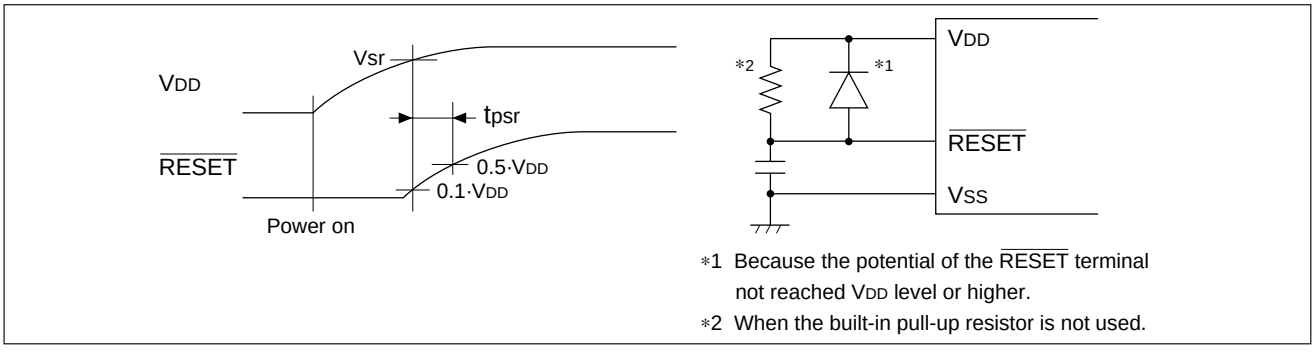
Note) 1. fosc: oscillation clock frequency, n=1–16: PRSM setting value + 1
When the simultaneous low input reset function is selected by mask option.



Power-on Reset

(Unless otherwise specified: V_{SS}=0V, Ta=-20 to 85°C, V_{IH}=0.5·V_{DD}, V_{IL}=0.1·V_{DD})

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	$\overline{\text{RESET}}$=0.1·V_{DD}	2.7			V	
$\overline{\text{RESET}}$ input time	tpsr		100			µS	



∗1 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

∗2 When the built-in pull-up resistor is not used.

A/D Conversion Characteristics

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=AV$_{SS}$=0V, Ta=-20 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
A/D conversion time	tADC	fAD=240kHz to 2.5MHz	20		21	clock	1
Sampling time	tSMP	fAD=240kHz to 2.5MHz		8		clock	1

Note) 1. fAD=fPRS=fOSC/2n or fAD=fOSC/2 (fAD: A/D conversion clock frequency, fOSC: oscillation clock frequency, n=1–16: PRSM setting value + 1)

● Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C, Crystal oscillator: Q21CA301xxx*, R_f=1MΩ, C_G=C_D=15pF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start voltage	Vsta		2.7			V	
Oscillation start time	tsta				20	mS	1
Oscillation stop voltage	Vstp		2.7			V	
Built-in gate capacitance	C_G			16		pF	
Built-in drain capacitance	C_D			13		pF	
Frequency/IC deviation	∂f/∂IC		-10		10	ppm	
Frequency/supply voltage deviation	∂f/∂V				1	ppm /V	
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ	

* Q21CA301xxx: made by Seiko Epson

Note) 1. The crystal oscillation start time varies according to the crystal oscillator, C_G and C_D to be used.

Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C, Ceramic oscillator: CSA 4.00MG*, R_f=1MΩ, C_G=C_D=30pF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start voltage	Vsta		2.7			V	
Oscillation start time	tsta				5	mS	
Oscillation stop voltage	Vstp		2.7			V	

* CSA 4.00MG: made by Murata Mfg. Co.

CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=-20 to 85°C)

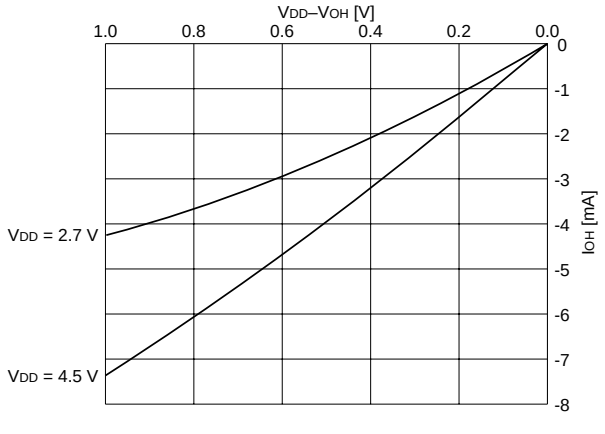
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start voltage	Vsta		2.7			V	
Oscillation start time	tsta				1	mS	
Oscillation stop voltage	Vstp		2.7			V	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

● Characteristic Curves (reference value)

Output Current Characteristics

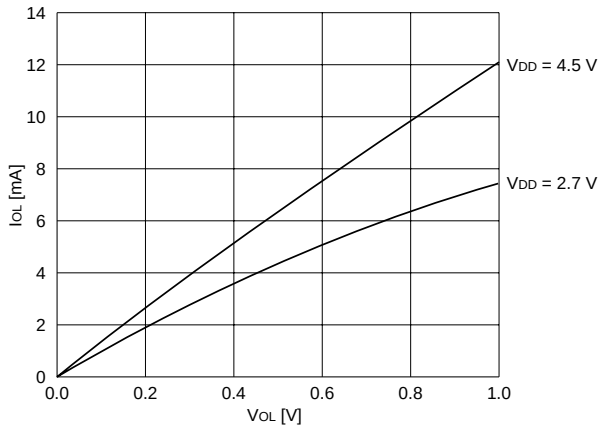
• High level output current (Pxx, Rxx, BZ)

Ta = 85˚C, Max. value



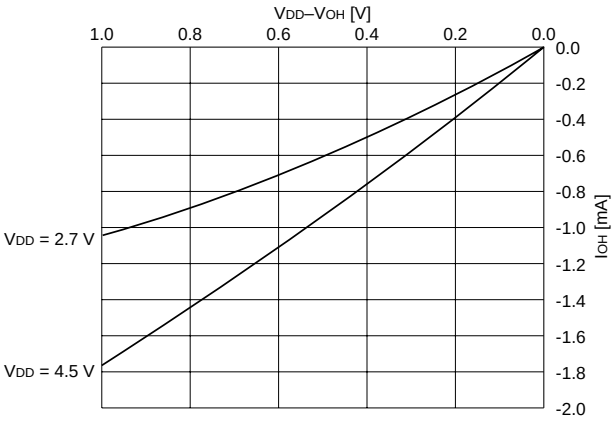
• Low level output current (Pxx, Rxx, BZ)

Ta = 85˚C, Min. value



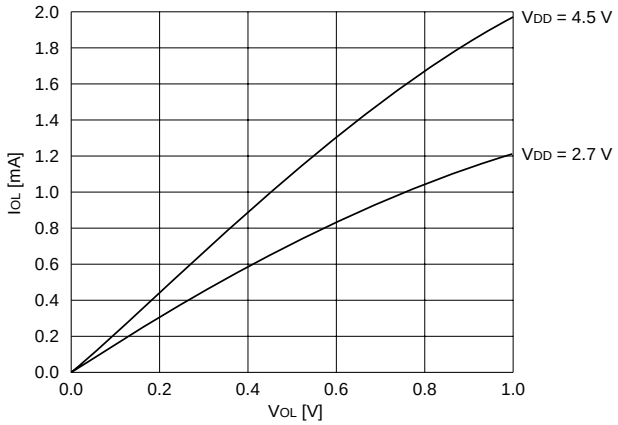
• High level output current (SEGxx)

Ta = 85˚C, Max. value



• Low level output current (SEGxx)

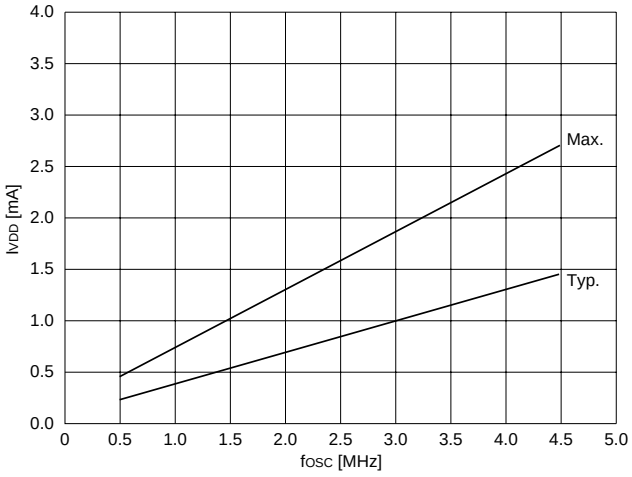
Ta = 85˚C, Min. value



Power Current - Frequency Characteristics

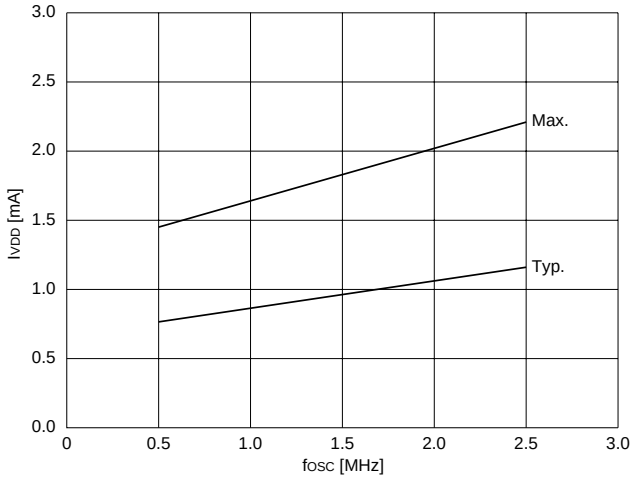
• Crystal oscillation/ceramic oscillation (during operation)

Ta = 25˚C



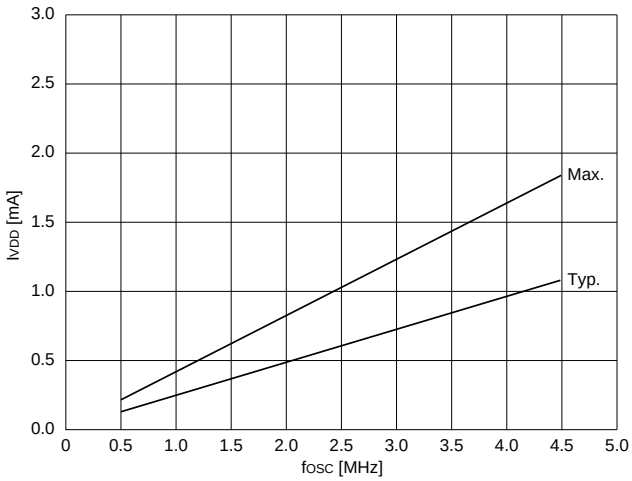
• CR oscillation (during operation)

Ta = 25˚C



• External clock (during operation)

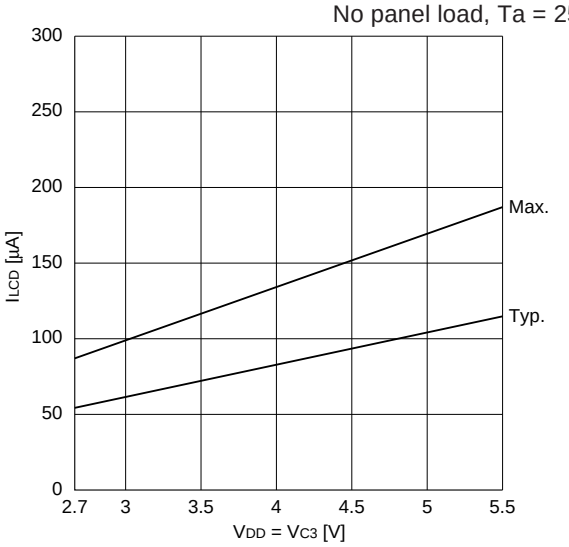
Ta = 25˚C



Analog System Operating Current - Voltage Characteristic

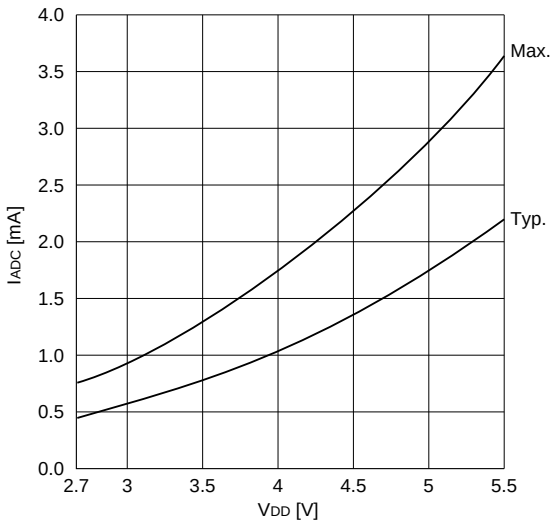
• LCD system operating current

No panel load, Ta = 25˚C



• A/D converter operating current

Ta = 25˚C



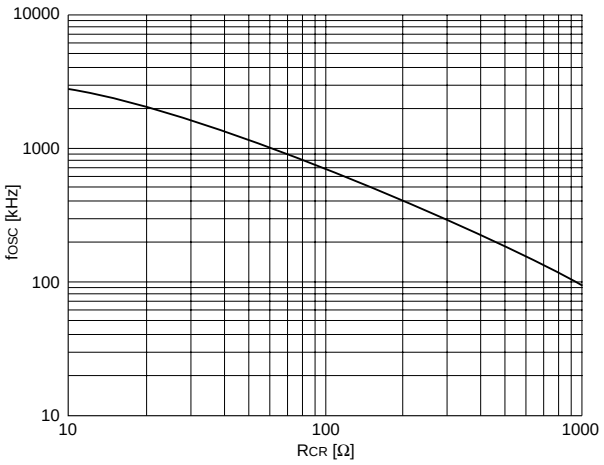
Note: Since the A/D converter operating current varies according to the A/D conversion clock frequency (f_{AD}) and analog input voltage, use the following voltage characteristics only for reference.

CR Oscillation Frequency Characteristics

Oscillation frequency changes depending on the conditions (components used, board pattern, etc.). In particular, extensively depending on the product from (chip, plastic package or ceramic package) and board capacitance. Therefore, use the following chart for reference only and select the resistance value after evaluating the actual product.

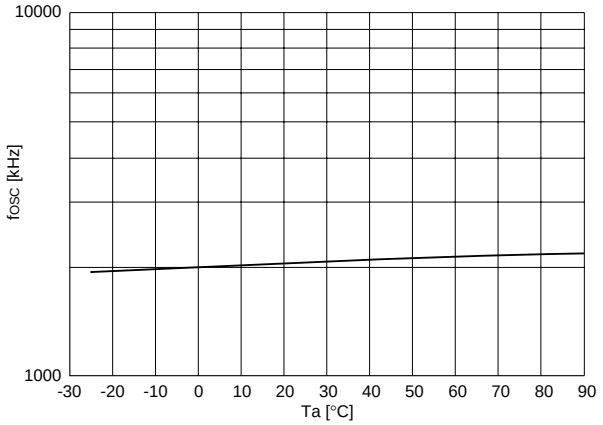
• Oscillation frequency - resistance characteristic

Ta = 25˚C, Typ. value

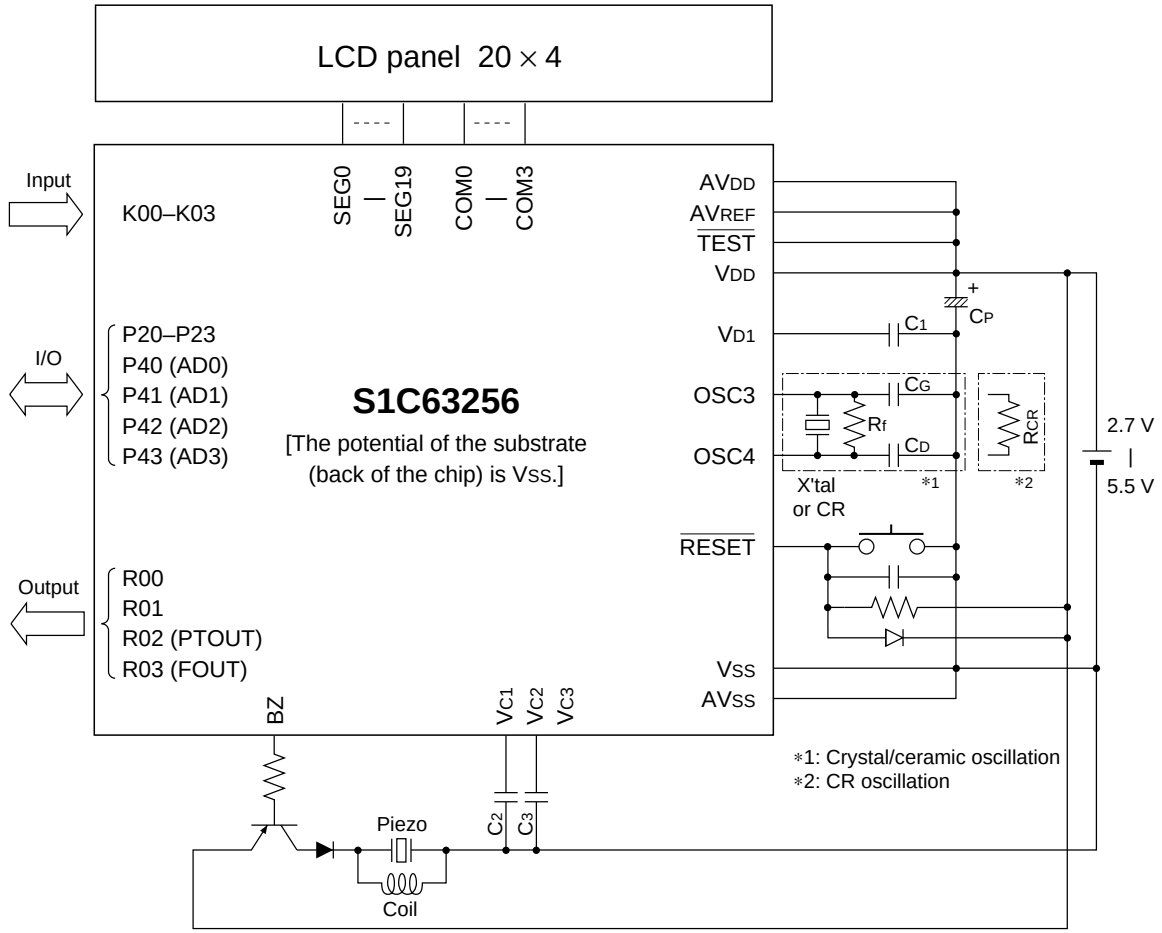


• Oscillation frequency - temperature characteristic

R_{CR} = 20 kΩ



■ BASIC EXTERNAL CONNECTION DIAGRAM



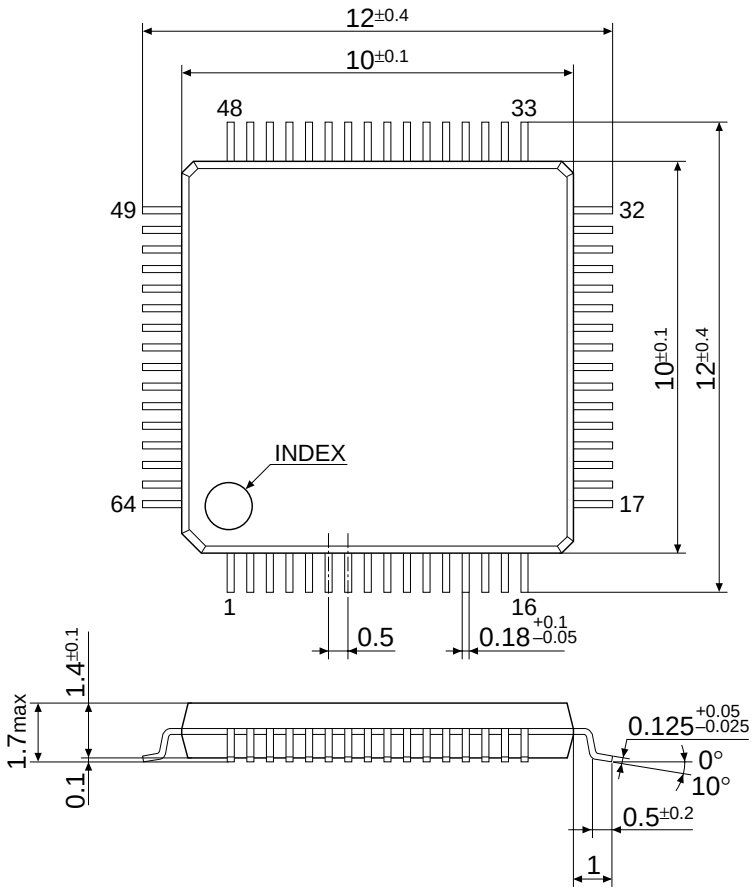
X'tal	Crystal oscillator	4.194304 MHz
CR	Ceramic oscillator	4.0 MHz
C_G	Gate capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
C_D	Drain capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
Rf	Feedback resistor	1 MΩ
R_{CR}	Resistor for CR oscillation	20 kΩ (2 MHz)
C_1	Capacitor	0.1 µF
C_2, C_3	Capacitor	0.1 µF
C_P		3.3 µF

* The connection diagram shown above is an example of when mask option settings are as follows:
  Buzzer signal: Negative polarity
  LCD power source: Internal LCD power supply (external V_{C3} not used)

Note:
- The above table is simply an example.
- Capacitors should be connected to the V_{C1}, V_{C2} and V_{C3} terminals for noise measure and to prevent reduction in LCD display quality. (These terminals do not necessarily have to be connected to a capacitor.)
- To interrupt current that flows in the resistor (analog reference resistor) connected between the AV_{REF} and AV_{SS} terminals, use a switching transistor from outside the IC.

■ PACKAGE DIMENSIONS

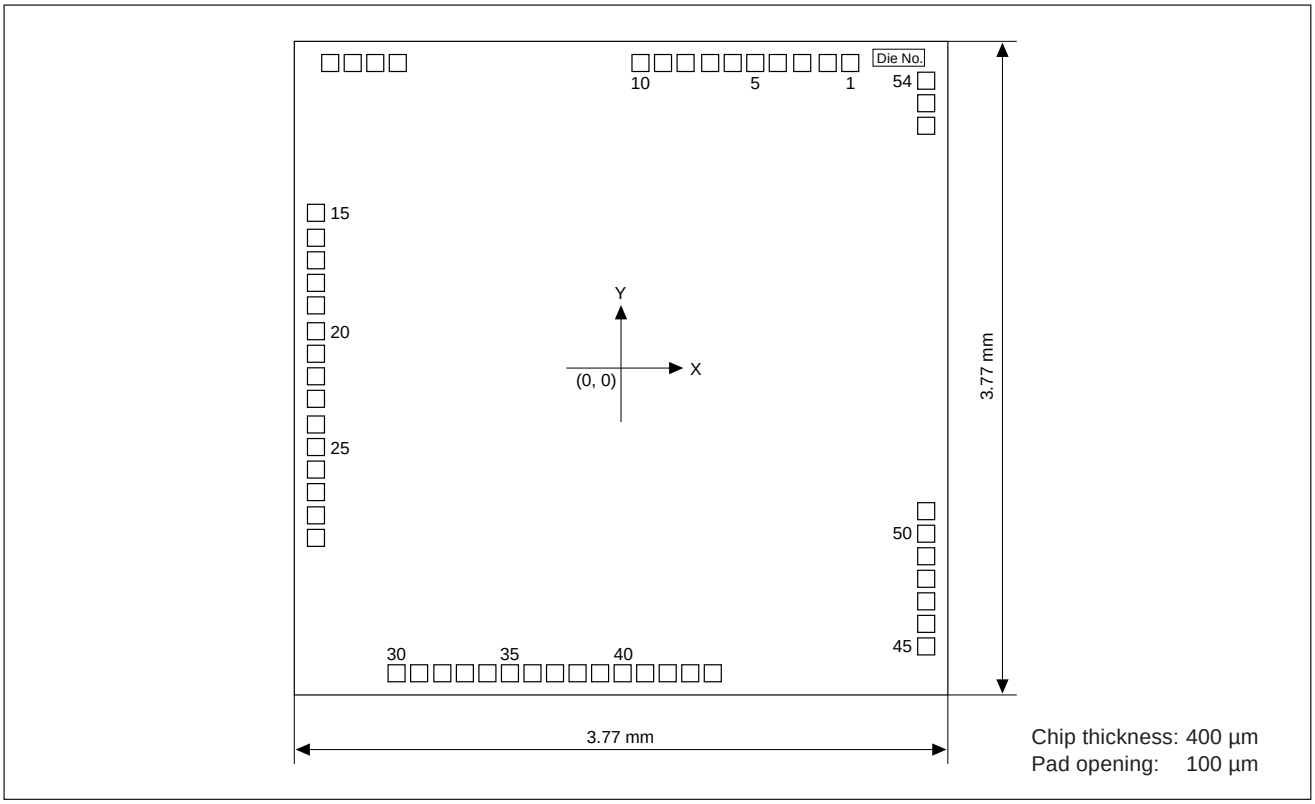
Plastic QFP13-64pin



Unit: mm

■ PAD LAYOUT

● Diagram of Pad Layout



● Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	$\overline{\text{RESET}}$	1322	1760	19	R03	-1760	362	37	SEG5	-381	-1760
2	$\overline{\text{TEST}}$	1192	1760	20	P20	-1760	213	38	SEG6	-251	-1760
3	V_{SS}	1045	1760	21	P21	-1760	83	39	SEG7	-121	-1760
4	OSC3	904	1760	22	P22	-1760	-47	40	SEG8	9	-1760
5	OSC4	774	1760	23	P23	-1760	-177	41	SEG9	139	-1760
6	V_{D1}	644	1760	24	K00	-1760	-325	42	SEG10	269	-1760
7	V_{DD}	514	1760	25	K01	-1760	-455	43	SEG11	399	-1760
8	AV_{DD}	372	1760	26	K02	-1760	-585	44	SEG12	529	-1760
9	AV_{REF}	242	1760	27	K03	-1760	-715	45	SEG13	1760	-1605
10	AV_{SS}	112	1760	28	COM0	-1760	-849	46	SEG14	1760	-1475
11	P40	-1288	1760	29	COM1	-1760	-979	47	SEG15	1760	-1345
12	P41	-1418	1760	30	COM2	-1295	-1760	48	SEG16	1760	-1215
13	P42	-1548	1760	31	COM3	-1165	-1760	49	SEG17	1760	-1085
14	P43	-1678	1760	32	SEG0	-1031	-1760	50	SEG18	1760	-955
15	BZ	-1760	896	33	SEG1	-901	-1760	51	SEG19	1760	-825
16	R00	-1760	752	34	SEG2	-771	-1760	52	V_{C1}	1760	1398
17	R01	-1760	622	35	SEG3	-641	-1760	53	V_{C2}	1760	1528
18	R02	-1760	492	36	SEG4	-511	-1760	54	V_{C3}	1760	1658

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