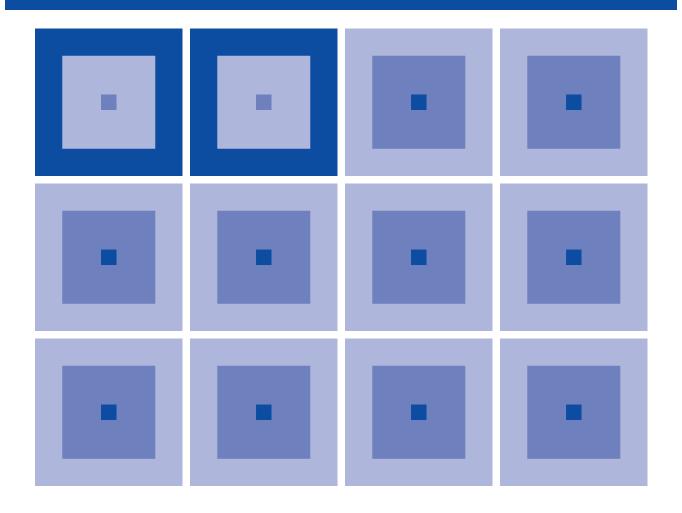


# CMOS 4-BIT SINGLE CHIP MICROCOMPUTER **S5U1C6S3N7D** Manual

(Development Software Tool for S1C6S3N7)



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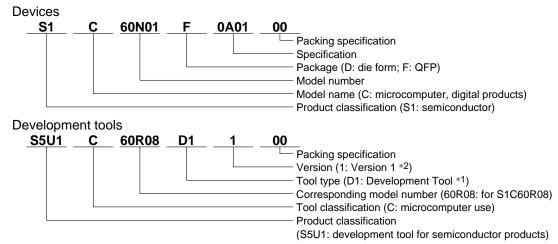
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## The information of the product number change

Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

# Configuration of product number



<sup>\*1:</sup> For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)

# Comparison table between new and previous number

S1C60 Family processors

<u> </u>	·
Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

#### S1C62 Family processors

Previous No.	New No.	Previous No.	New No.
E0C621A	S1C621A0	E0C6247	S1C62470
E0C6215	S1C62150	E0C6248	S1C62480
E0C621C	S1C621C0	E0C6S48	S1C6S480
E0C6S27	S1C6S2N7	E0C624C	S1C624C0
E0C6S37	S1C6S3N7	E0C6251	S1C62N51
E0C623A	S1C6N3A0	E0C6256	S1C62560
E0C623E	S1C6N3E0	E0C6292	S1C62920
E0C6S32	S1C6S3N2	E0C6262	S1C62N62
E0C6233	S1C62N33	E0C6266	S1C62660
E0C6235	S1C62N35	E0C6274	S1C62740
E0C623B	S1C6N3B0	E0C6281	S1C62N81
E0C6244	S1C62440	E0C6282	S1C62N82
E0C624A	S1C624A0	E0C62M2	S1C62M20
E0C6S46	S1C6S460	E0C62T3	S1C62T30

# Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.	Previous No.	New No.	
ASM62	S5U1C62000A	DEV6262	S5U1C62620D	
DEV6001	S5U1C60N01D	DEV6266	S5U1C62660D	
DEV6002	S5U1C60N02D	DEV6274	S5U1C62740D	
DEV6003	S5U1C60N03D	DEV6292	S5U1C62920D	
DEV6004	S5U1C60N04D	DEV62M2	S5U1C62M20D	
DEV6005	S5U1C60N05D	DEV6233	S5U1C62N33D	
DEV6006	S5U1C60N06D	DEV6235	S5U1C62N35D	
DEV6007	S5U1C60N07D	DEV6251	S5U1C62N51D	
DEV6008	S5U1C60N08D	DEV6256	S5U1C62560D	
DEV6009	S5U1C60N09D	DEV6281	S5U1C62N81D	
DEV6011	S5U1C60N11D	DEV6282	S5U1C62N82D	
DEV60R08	S5U1C60R08D	DEV6S27	S5U1C6S2N7D	
DEV621A	S5U1C621A0D	DEV6S32	S5U1C6S3N2D	
DEV621C	S5U1C621C0D	DEV6S37	S5U1C6S3N7D	
DEV623B	S5U1C623B0D	EVA6008	S5U1C60N08E	
DEV6244	S5U1C62440D	EVA6011	S5U1C60N11E	
DEV624A	S5U1C624A0D	EVA621AR	S5U1C621A0E2	
DEV624C	S5U1C624C0D	EVA621C	S5U1C621C0E	
DEV6248	S5U1C62480D	EVA6237	S5U1C62N37E	
DEV6247	S5U1C62470D	EVA623A	S5U1C623A0E	

Previous No.         New No.           EVA623B         S5U1C623B0E           EVA623F         S5U1C623B0E           EVA6247         S5U1C62470E           EVA6248         S5U1C62480E           EVA6256R         S5U1C62N51E1           EVA6256S         S5U1C62N56E           EVA6262S         S5U1C6260E           EVA6274S         S5U1C62740E           EVA6281S         S5U1C62N81E           EVA6282S         S5U1C62N82E           EVA6281S         S5U1C62N82E           EVA6281S         S5U1C62N82E           EVA6281S         S5U1C62N82E           EVA627S         S5U1C62N30E           EVA6S27S         S5U1C63N2E2           EVA6S32RS         S5U1C63N2E2           ICE62RS         S5U1C62000H           KIT6003S         S5U1C60N03K           KIT6004S         S5U1C60N07K		
EVA623E S5U1C623E0E EVA6247 S5U1C62470E EVA6248 S5U1C62480E EVA6251R S5U1C62N51E1 EVA6256 S5U1C62050E EVA6262 S5U1C62600E EVA6274 S5U1C62740E EVA6281 S5U1C62740E EVA6282 S5U1C62N81E EVA6281 S5U1C62N81E EVA6281 S5U1C62N82E EVA62M1 S5U1C62N10E EVA6273 S5U1C62N30E EVA6273 S5U1C63N7E EVA6827 S5U1C6S3N7E EVA6832R S5U1C6S3N2E2 ICE62R S5U1C60N03K KIT6004 S5U1C60N04K	Previous No.	New No.
EVA6247 S5U1C62470E EVA6248 S5U1C62480E EVA6251R S5U1C62N51E1 EVA6256 S5U1C62N56E EVA6262 S5U1C62600E EVA6264 S5U1C62600E EVA6264 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N81E EVA6281 S5U1C62N81E EVA6281 S5U1C62N81E EVA6282 S5U1C62N81E EVA6283 S5U1C62N81E EVA62T3 S5U1C62N10E EVA62T3 S5U1C6SN7E EVA6S32R S5U1C6SN2E2 ICE62R S5U1C60N03K KIT6004 S5U1C60N04K	EVA623B	S5U1C623B0E
EVA6248 S5U1C62480E EVA6251R S5U1C62N51E1 EVA6256 S5U1C62N56E EVA6262 S5U1C62600E EVA6266 S5U1C62600E EVA6274 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N81E EVA6281 S5U1C62N81E EVA6287 S5U1C62N80E EVA6273 S5U1C62N10E EVA6273 S5U1C6SN7E EVA6S32R S5U1C6SN7E EVA6S32R S5U1C6SN0E2 KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA623E	S5U1C623E0E
EVA6251R S5U1C62N51E1 EVA6256 S5U1C62N56E EVA6262 S5U1C62620E EVA6266 S5U1C6260E EVA6274 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N81E EVA6281 S5U1C62N81E EVA6287 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C6S2N72 EVA6S32R S5U1C6SN2E2 ICE62R S5U1C60N03K KIT6004 S5U1C60N04K	EVA6247	S5U1C62470E
EVA6256 S5U1C62N56E EVA6262 S5U1C62620E EVA6266 S5U1C62660E EVA6274 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6248	S5U1C62480E
EVA6262 S5U1C62620E EVA6266 S5U1C62660E EVA6274 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6251R	S5U1C62N51E1
EVA6266 S5U1C62660E EVA6274 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6256	S5U1C62N56E
EVA6274 S5U1C62740E EVA6281 S5U1C62N81E EVA6282 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C6C900H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6262	S5U1C62620E
EVA6281 S5U1C62N81E EVA6282 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S227 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C6C000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6266	S5U1C62660E
EVA6282 S5U1C62N82E EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S227 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C6C2000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6274	S5U1C62740E
EVA62M1 S5U1C62M10E EVA62T3 S5U1C62T30E EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6281	S5U1C62N81E
EVA62T3 S5U1C62T30E EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6282	S5U1C62N82E
EVA6S27 S5U1C6S2N7E EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA62M1	S5U1C62M10E
EVA6S32R S5U1C6S3N2E2 ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA62T3	S5U1C62T30E
ICE62R S5U1C62000H KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6S27	S5U1C6S2N7E
KIT6003 S5U1C60N03K KIT6004 S5U1C60N04K	EVA6S32R	S5U1C6S3N2E2
KIT6004 S5U1C60N04K	ICE62R	S5U1C62000H
	KIT6003	S5U1C60N03K
KIT6007 S5U1C60N07K	KIT6004	S5U1C60N04K
	KIT6007	S5U1C60N07K

<sup>\*2:</sup> Actual versions are not written in the manuals.

### **PREFACE**

This manual mainly explains the outline of the development support tool for the 4-bit Single Chip Microcomputer S1C6S3N7.

Refer to the "S1C62 Family Development Tool Reference Manual" for the details (common to all models) of each development support tool. Manuals for hardware development tools are separate, so you should also refer to the below manuals.

Development tools S1C62 Family Development Tool Reference Manual S5U1C62N51E1 Manual (Evaluation Board for S1C60N01/60N02/60N05/62N51/6S3N7) S5U1C62000H Manual (S1C60/62 Family In-Circuit Emulator)

Device (S1C6S3N7) S1C6S3N7 Technical Manual

Instructions S1C6200/6200A Core CPU Manual

\* In this manual, "ICE" and "evaluation board" indicate S5U1C62000H and S5U1C62N51E1, respectively.

#### **CONTENTS**

1	COMI	POSITION OF DEVELOPMENT SUPPORT TOOL	1
	1.1	Configuration of S5U1C6S3N7D1	
	1.2	Developmental Environment	
	1.3	Development Flow	
	1.4	Installation	
2	DEVE	CLOPMENT TOOL MANAGEMENT SYSTEM DMS6200	4
	2.1	DMS6200 Outline	
	2.2	DMS6200 Quick Reference	
3	CROS	S ASSEMBLER ASM6S37	5
	3.1	ASM6S37 Outline	
	3.2	S1C6S3N7 Restrictions	
	3.3	ASM6S37 Quick Reference	
4	FUNC	CTION OPTION GENERATOR FOG6S37	8
	4.1	FOG6S37 Outline 8	
	4.2	S1C6S3N7 Option List	
	4.3	Option Specifications and Selection Message	)
	4.4	FOG6S37 Quick Reference	
	4.5	Sample File	
5	SEGN	MENT OPTION GENERATOR SOG6S37	20
	5.1	SOG6S37 Outline	1
	5.2	<i>Option List</i>	1
	5.3	Segment Ports Output Specifications	
	5.4	SOG6S37 Quick Reference	
	5.5	Sample Files	
6	ICE C	CONTROL SOFTWARE ICS6S37	25
	6.1	ICS6S37 Outline	
	6.2	ICS6S37 Restrictions	
	6.3	ICS6S37 Quick Reference	,

#### **CONTENTS**

7 MASK DA	ATA CHECKER MDC6S37	29
7.1 M	DC6S37 Outline	29
7.2 M	DC6S37 Quick Reference	29
APPENDIX	A. S1C6S3N7 INSTRUCTION SET	32
	B. S1C6S3N7 RAM MAP	36
	C. S1C6S3N7 I/O MEMORY MAP	37
	D. TROUBLESHOOTING	39
	E. DEBUGGING FOR 1/2 DUTY DRIVE	
	ON EVALUATION BOARD	41

# 1 COMPOSITION OF DEVELOPMENT SUPPORT TOOL

Here we will explain the composition of the software for the development support tools, developmental envilonment and how to generate the execution disk.

# 1.1 Configuration of S5U1C6S3N7D

The below software are included in the product of the S1C6S3N7 development support tool S5U1C6S3N7D.

- 1. Development Tool Management System DMS6200 ..... Menu selection for each software / start-up software
- 2. Cross Assembler ASM6S37 ...... Cross assembler for program preparation
- 3. Function Option Generator FOG6S37..... Function option data preparation program
- 4. Segment Option Generator SOG6S37 ...... Segment option data preparation program
- 5. ICE Control Software ICS6S37 ...... ICE control program
- 6. Mask Data Checker MDC6S37 ...... Mask data preparation program

# 1.2 Developmental Environment

The software product of the development support tool S5U1C6S3N7D operates on the following host systems:

• IBM PC/AT (at least PC-DOS Ver. 2.0)

When developing the S1C6S3N7, the above-mentioned host computer, editor, P-ROM writer, printer, etc. must be prepared by the user in addition to the development tool which is normally supported by Seiko Epson.

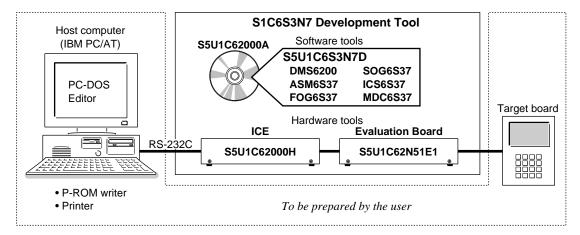
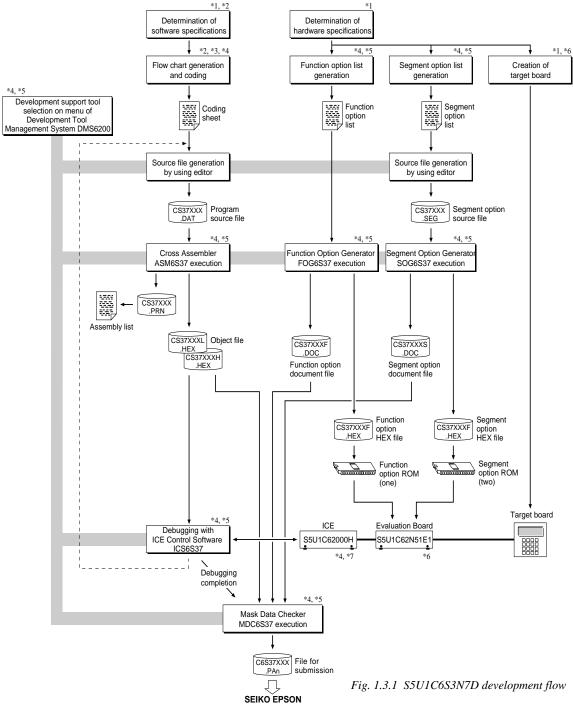


Fig. 1.2.1 System configuration

Note The S5U1C6S3N7D system requires a host computer with a RAM capacity of about 140K bytes. Since the ICE (S5U1C62000H) is connected to the host computer with a RS-232C serial interface, adapter board for asynchronous communication will be required depending on the host computer used.

# 1.3 Development Flow

Figure 1.3.1 shows the development flow through the S5U1C6S3N7D.



#### Concerning file names

All the input-output file name for the each development support tool commonly use "CS37XXX". In principle each file should be produced in this manner. Seiko Epson will designate the "XXX" for each customer.

#### Reference Manual

- \*1 S1C6S3N7 Technical Manual (Hardware)
- \*2 S1C6S3N7 Technical Manual (Software)
- \*3 S1C6200/6200A Core CPU Manual
- \*4 S1C62 Family Development Tool Reference Manual
- \*5 S5U1C6S3N7D Manual (this manual)
- \*6 S5U1C62N51E1 Manual
- \*7 S5U1C62000H Manual

# 1.4 Installation

The S5U1C6S3N7D tools are included on the CD-ROM of the S5U1C62000A (S1C60/62 Family Assembler Package), and they can be installed in your hard disk using the installer (Setup.exe) on the CD-ROM. Refer to the "S5U1C62000A Manual" for how to install the S5U1C6S3N7D tools.

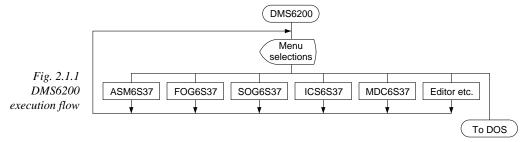
Note The DMS6200 configures a menu from files that are located in the current directory. Therefore, do not move the development tools from the directory in which the DMS6200 exists.

To invoke an editor (DOS version) or other programs from the DMS6200, copy those executable files to the directory in which the DMS6200 exists.

# 2 DEVELOPMENT TOOL MANAGEMENT SYSTEM DMS6200

#### 2.1 DMS6200 Outline

The DMS6200 (<u>D</u>evelopment Tool <u>M</u>anagement <u>S</u>ystem) is a software which selects the S5U1C6S3N7D software development support tool and the program such as an editor in menu form and starts it. In this way the various software frequently executed during debugging can be effectively activated.



Refer to the "S1C62 Family Development Tool Reference Manual" for detailes of the operation.

# 2.2 DMS6200 Quick Reference

#### ■ Starting command

Execution file: DMS6200.EXE

*Starting command:* DMS6200 □

☐ indicates the Return key.

# ■ Display examples

*** E0C62	00 Development	tool	Manageme	ent Syst	em	Ver 1.	) ***
EEEEEEEEE	PPPPPPPP	SSS	SSSS	0000	0000	NNN	NNN
EEEEEEEEE	PPPPPPPPPP	SSS	SSSS	000	000	NNNN	NNN
EEE	PPP PPP	SSS	SSS	000	000	NNNNN	NNN
EEE	PPP PPP	SSS		000	000	NNNNN	NNN V
EEEEEEEEE	PPPPPPPPPP	SSS	SSS	000	000	NNN N	NNN NNN
EEEEEEEEE	PPPPPPPP		SSSS	000	000	NNN I	NNNNN
EEE	PPP		SSS	000	000	NNN	NNNNN
EEE	PPP	SSS	SSS	000	000	NNN	NNNN
EEEEEEEEE	PPP	SSSS	SSS	000	000	NNN	NNN
EEEEEEEEE	PPP	SSS	SSSS	0000	0000	NNN	NN
	(C) Copyright 1990 SEIKO EPSON CORP.						
		STRIK	E ANY KI	ΞY.			

#### Start message

When DMS6200 is started, the following message is displayed. For "STRIKE ANY KEY.", press any key to advance the program execution.

To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

DMS6200 Version 1.0	Copyright(C)	SEIKO	EPSON	CORP.	1990.	
1) ASM6S37 .EXE 2) FOG6S37 .EXE 3) ICS6S37B.BAT 4) ICS6S37W.EXE 5) MDC6S37 .EXE 6) SOG6S37 .EXE						
Input Number ? [1 ]						

#### Menu screen

A list of all executable files will appear on this menu screen.

Input the number of the development support tool you wish to start and then press the "RETURN" key. To return to DOS at this point, press the "ESC" key.

# DMS6200 Version 1.0 Copyright(C) SEIKO EPSON CORP. 1990. 1) CS37XXX .DAT 2) CS37XXX .PRN 3) CS37XXX .SEG: : : 10) C6S37XXX.PAO Input Number ? [1 ] Edit > [ASM6S37 CS37XXX ]

#### Source file selection screen

To starting ASM6S37, select the source file on this screen. When the source file is selected by number, the edit line enclosed in [] will appear; enter the option parameter if necessary. Press the "RETURN" key when input is completed. When starting, press the "RETURN" key twice particularly for the support tools which do not require source files. To return to DOS at this point, press the "ESC" key.

# 3 CROSS ASSEMBLER ASM6S37

#### 3.1 ASM6S37 Outline

The ASM6S37 cross assembler is an assembler program for generating the machine code used by the S1C6S3N7 4-bit, single-chip microcomputers. The Cross Assembler ASM6S37 will assemble the program source files which have been input by the user's editor and will generate an object file in Intel-Hex format and assembly list file.

In this assembler, program modularization has been made possible through macro definition functions and programming independent of the ROM page structure has been made possible through the auto page set function. In addition, consideration has also been given to precise error checks for program capacity (ROM capacity) overflows, undefined codes and the like, and for debugging of such things as label tables for assembly list files and cross reference table supplements.

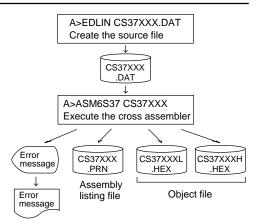


Fig. 3.1.1 ASM6S37 execution flow

The format of the source file and its operating method are same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

#### 3.2 S1C6S3N7 Restrictions

Note the following when generating a program by the S1C6S3N7:

#### ■ ROM area

The capacity of the S1C6S3N7 ROM is 1K steps (0000H to 03FFH).

Therefore, the specification range of the memory setting pseudo-instructions and PSET instruction is restricted.

#### ■ RAM area

The capacity of the S1C6S3N7 RAM is 144 words (000H to 04FH, 090H to 0AFH, and 0E0H to 0FFH, 4 bits/word). Memory access is invalid when the unused area of the index register is specified.

#### **■** Undefined codes

The following instructions have not been defined in the S1C6S3N7 instruction sets.

#### Memory configuration:

Bank: Only bank 0, Page: 4 pages (0 to 3H), each 256 steps

## Significant specification range:

ORG pseudo-instruction: 0000H to 03FFH
PAGE pseudo-instruction: 00H to 03H
BANK pseudo-instruction: Only 0H
PSET instruction: 00H to 03H

Example: LD X,050H 50H is loaded into the IX register, but an

unused area has been specified so that the memory accessible with the IX register

(MX) is invalid.

LD Y, 0C7H C7H is loaded into the IY register, but an

unused area has been specified so that the memory accessible with the IY register

(MY) is invalid.

SLP			
PUSH	XP	PUSH	ΥP
POP	XP	POP	ΥP
LD	XP,r	LD	YP,r
LD	r.XP	LD	r.YP

# 3.3 ASM6S37 Quick Reference

#### ■ Starting command and input/output files

\_ indicates a blank.

Execution file: ASM6S37.EXE

☐ indicates the Return key.
A parameter enclosed by [] can be omitted.

Starting command: ASM6S37\_ [drive-name:] source-file-name [.shp]\_ [-N] -

*Option:* .shp Specifies the file I/O drives.

S pecifies the drive from which the source file is to be input. (A-P, @)
 h Specifies the drive to which the object file is to be output. (A-P, @, Z)

p Specifies the drive to which the assembly listing file is to be output. (A–P, @, Z)

@: Current drive, Z: File is not generated

-N The code (FFH) in the undefined area of program memory is not created.

Input file: CS37XXX.DAT (Source file)

Output file: CS37XXXL.HEX (Object file, low-order)

CS37XXXH.HEX (Object file, high-order) CS37XXX.PRN (Assembly listing file)

#### ■ Display example

*	** E0C6S37 CROS	S ASSEN	MBLER.	Ver	2.00 ***		
EEEEEEEEE EEE EEE EEE	PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	SSSS SSS SSS	SSSS SSSS SSS	0000 000 000	00000	NNN NNNN NNNNN	NNN NNN NNN
EEEEEEEEE EEE	PPPPPPPPPP PPPPPPPP PPP	SSSS	SSSS	000 000 000	000 000 000	NNN N NNN NNN	NN NNN NNNNNN NNNNN
EEE EEEEEEEEE EEEEEEEEE	PPP PPP PPP	SSS SSSS SSSS	SSS SSSS	000 000	000	NNN NNN NNN	NNNN NNN NN
S	(C) COPYRIGHT 1989 SEIKO EPSON CORP. SOURCE FILE NAME IS " CS37XXX.DAT "						
T	HIS SOFTWARE MA	KES NEX	T FILE	s.			
CS37XXXH.HEX HIGH BYTE OBJECT FILE. CS37XXXL.HEX LOW BYTE OBJECT FILE. CS37XXX .PRN ASSEMBLY LIST FILE.							
DO YOU NEED	AUTO PAGE SET?	(Y/N)	Y				(1)
DO YOU NEED	CROSS REFERENC	E TABLE	E? (Y/N	) Y			(2)

When ASM6S37 is started, the start-up message is displayed.

At (1), select whether or not the auto-pageset function will be used.

Use ...... Y 
Not use ...... N

If the assembly listing file output is specified, message (2) is displayed. At this stage, cross-reference table generation may be selected.

Generating ...... Y 
Not generating ...... N

When the above operation is completed, ASM6S37 assembles the source file. To suspend execution, press the "CTRL" and "C" keys together at stage (1) or (2).

#### Operators

Arithmetic	operators	Logical operators		
+a	Monadic positive	a_AND_b	Logical product	
-a	Monadic negative	a_OR_b	Logical sum	
a+b	Addition	a_XOR_b	Exclusive logical sum	
a-b	Subtraction	NOT_a	Logical negation	
a*b	Multiplication	Relational operators		
a/b	Division	a_EQ_b	True when a is equal to b	
a_MOD_b	Remainder of a/b	a_NE_b	True when a is not equal to b	
a_SHL_b	Shifts a b bits to the left	a_LT_b	True when a is less than b	
a_SHR_b	Shifts a b bits to the right	a_LE_b	True when a is less than or equal to b	
HIGH_a	Separates the high-order eight bits from a	a_GT_b	True when a is greater than b	
LOW_a	Separates the low-order eight bits from a	a_GE_b	True when a is greater than or equal to b	

#### **■** Pseudo-instructions

Pseudo-instruction		Meaning		fuse	
EQU	(Equation)	To allocate data to label	ABC	EQU	9
			BCD	EQU	ABC+1
SET	(Set)	To allocate data to label	ABC	SET	0001н
		(data can be changed)	ABC	SET	0002H
DW	(Define Word)	To define ROM data	ABC	DW	'AB'
			BCD	DW	0FFBH
ORG	(Origin)	To define location counter		ORG	100H
				ORG	256
PAGE	(Page)	To define boundary of page		PAGE	1H
				PAGE	3
SECTION	(Section)	To define boundary of section		SECTION	1
END	(End)	To terminate assembly		END	
MACRO	(Macro)	To define macro	CHECK LOCAL	MACRO LOOP	DATA
LOCAL	(Local)	To make local specification of label during macro definition	LOOP	CP JP ENDM	MX,DATA NZ,LOOP
ENDM	(End Macro)	To end macro definition		CHECK	1

# **■** Error messages

Error message	Explanation
S (Syntax Error)	An unrecoverable syntax error was encountered.
U (Undefined Error)	The label or symbol of the operand has not been defined.
M (Missing Label)	The label field has been omitted.
O (Operand Error)	A syntax error was encountered in the operand, or the operand could
	not be evaluated.
P (Phase Error)	The same label or symbol was defined more than once.
R (Range Error)	The location counter value exceeded the upper limit of the program
	memory, or a location exceeding the upper limit was specified.
	• A value greater than that which the number of significant digits of the
	operand will accommodate was specified.
! (Warning)	Memory areas overlapped because of a "PAGE" or "ORG" pseudo-
	instruction or both.
FILE NAME ERROR	The source file name was longer than 8 characters.
FILE NOT PRESENT	The specified source file was not found.
DIRECTORY FULL	No space was left in the directory of the specified disk.
FATAL DISK WRITE ERROR	The file could not be written to the disk.
LABEL TABLE OVERFLOW	The number of defined labels and symbols exceeded the label table
	capacity (4000).
CROSS REFERENCE TABLE OVERFLOW	The label/symbol reference count exceeded the cross-reference table
	capacity (only when the cross-reference table is generated).

# 4 FUNCTION OPTION GENERATOR FOG6S37

#### 4.1 FOG6S37 Outline

With the 4-bit single-chip S1C6S3N7 microcomputers, the customer may select 10 hardware options. By modifying the mask patterns of the S1C6S3N7 according to the selected options, the system can be customized to meet the specifications of the target system.

The Function Option Generator FOG6S37 is a software tool for generating data files used to generate mask patterns. It enables the customer to interactively select and specify pertinent items for each hardware option. From the data file created with FOG6S37, the S1C6S3N7 mask pattern is automatically generated by a general purpose computer.

The HEX file for the evaluation board (S5U1C62N51E1) hardware option ROM is simultaneously generated with the data file.

The operating method is same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

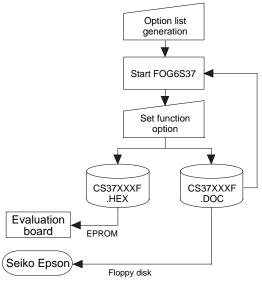


Fig. 4.1.1 FOG6S37 execution flow

# 4.2 S1C6S3N7 Option List

Multiple specifications are available in each option item as indicated in the Option List. Using "4.3 Option Specifications and Selection Message" as reference, select the specifications that meet the target system. Be sure to record the specifications for unused ports too, according to the instructions provided.

# 1. DEVICE TYPE, LCD VOLTAGE REGULATOR AND LCD VOLTAGE 1. F0C6S37 (Normal Type < S1C6S3N7>) LCD Voltage Regulator Use

☐ 1. E0C0337	(Normai Type < 51C055N7>)	LCD voltage Regurator	Use	LCD 3 V
☐ 2. E0C6S37	(Normal Type <s1c6s3n7>)</s1c6s3n7>	LCD Voltage Regurator	Not Use	LCD 3 V
☐ 3. E0C6S37	(Normal Type <s1c6s3n7>)</s1c6s3n7>	LCD Voltage Regurator	Not Use	LCD 4.5 V
☐ 4. E0C6SL37	(Low Power Type <s1c6s3l7>)</s1c6s3l7>	LCD Voltage Regurator	Use	LCD 3 V
☐ 5. E0C6SL37	(Low Power Type <s1c6s3l7>)</s1c6s3l7>	LCD Voltage Regurator	Not Use	LCD 3 V
☐ 6. E0C6SL37	(Low Power Type <s1c6s3l7>)</s1c6s3l7>	LCD Voltage Regurator	Not Use	LCD 4.5 V
☐ 7. E0C6SB37	(Wide Range Type <s1c6s3b7>)</s1c6s3b7>	LCD Voltage Regurator	Use	LCD 3 V

#### 2. MULTIPLE KEY ENTRY RESET

COMBINATION	□ 1	. Not	Use			
	$\square$ 2	. Use	K00,	K01		
	$\square$ 3	. Use	K00,	K01,	K02	
	$\Box$ 1	Πse	K00	K01	KN2	KOS

#### 3. INTERRUPT NOISE REJECTOR

• K00-K03	☐ 1. Use	□ 2. Not Use

#### 4. INPUT PORT PULL DOWN RESISTOR

• K00	🗆 1. With Resistor	☐ 2. Gate Direct
• K01	🗆 1. With Resistor	☐ 2. Gate Direct
• K02	🗆 1. With Resistor	☐ 2. Gate Direct
• K03	□ 1 With Resistor	☐ 2 Gate Direct

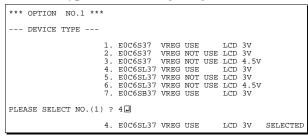
ICD 9 V

5.	<b>R00 SPECIFICATION</b>				
	OUTPUT TYPE	□ 2. Buzzer	Inverted Ou Inverted Ou	tput (R00 Control) tput (R01 Control)	
	• FOUT OUTPUT SPACIFICATION	F1	256[Hz] 512[Hz] 1,024[Hz] 2,048[Hz] 4,096[Hz] 512[Hz] 1,024[Hz] 2,048[Hz] 4,096[Hz] 8,192[Hz]	F3	1,024[Hz] 2,048[Hz] 4,096[Hz] 8,192[Hz] 16,384[Hz] 2,048[Hz] 4,096[Hz] 8,192[Hz] 16,384[Hz] 32,768[Hz]
	• OUTPUT SPECIFICATION	🗆 1. Complei	,	□ 2. Pch-Open □	
6.	R01 SPECIFICATION  • OUTPUT TYPE  • OUTPUT SPECIFICATION			☐ 2. Buzzer Out	
7.	OUTPUT SPECIFICATION (R02, • R02	🗆 1. Complei		☐ 2. Pch-Open ☐ ☐ 2. Pch-Open ☐	
8.	<ul> <li>I/O PORT SPECIFICATION</li> <li>P00</li> <li>P01</li> <li>P02</li> <li>P03</li> </ul>	□ 1. Complei □ 1. Complei	mentary mentary	<ul> <li>□ 2. Pch-Open E</li> <li>□ 2. Pch-Open E</li> <li>□ 2. Pch-Open E</li> <li>□ 2. Pch-Open E</li> </ul>	Orain Orain
9.	LCD COMMON DUTY AND BIAS	☐ 1. 1/4 Duty ☐ 2. 1/3 Duty ☐ 3. 1/2 Duty ☐ 4. 1/4 Duty ☐ 5. 1/3 Duty ☐ 6. 1/2 Duty	y 1/3 Bias y 1/3 Bias y 1/2 Bias y 1/2 Bias		
10.	OSC1 SYSTEM CLOCK	□ 1. Crystal □ 2. CR			

# 4.3 Option Specifications and Selection Message

Screen that can be selected as function options set on the S1C6S3N7 are shown below, and their specifications are also described.

## 1 Device type, LCD voltage regulator and LCD voltage



S1C6S3N7, S1C6S3L7, S1C6S3B7

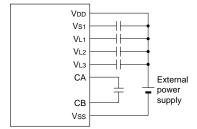


Fig. 4.3.1 External elements when LCD system voltage regulator is used

Note: VL1 is shorted to Vss inside the IC.

Select the chip specification.

There are three models: "E0C6S37" (S1C6S3N7) (3 V supply voltage), "E0C6SL37" (S1C6S3L7) (1.5 V supply voltage, low-power specification) and "E0C6SB37" (S1C6S3B7) (0.9 to 3.6 V supply voltage, wide range specification).

The other specifications of the "E0C6SB37" are same as the "E0C6S37".

In the "E0C6S37" and the "E0C6SL37", select either "Use" or "Not use" for the LCD system voltage regulator. The "E0C6SB37" always uses the LCD system voltage regulator.

When the LCD system voltage regulator is not used in the "E0C6S37" or the "E0C6SL37", the external capacitors can be minimized. However, the display quality of the LCD panel when the supply voltage drops is inferior to when the LCD system voltage regulator is used.

Moreover, when the LCD system voltage regulator is not used in the "E0C6S37" or the "E0C6SL37" select the LCD drive voltage (3 V or 4.5 V) according to the LCD panel to be used. When the LCD system voltage regulator is used, the LCD drive voltage is fixed at 3 V. Figure 4.3.1 shows the external elements when the LCD system voltage regulator is used.

Figure 4.3.2 shows the external elements when the LCD system voltage regulator is not used.

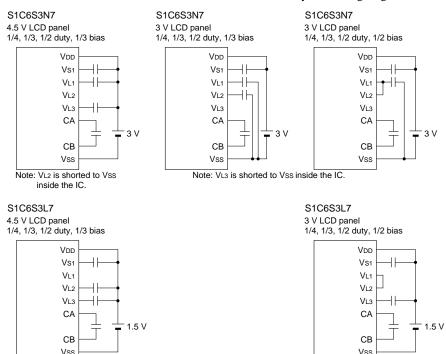
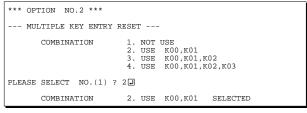
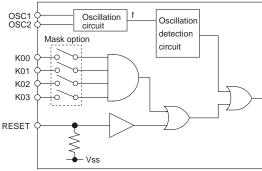


Fig. 4.3.2 External elements when LCD system voltage regulator is not used

Note: VL1 is shorted to Vss inside the IC.

## 2 Multiple key entry reset





The reset function is set when K00 through K03 are entered.

When "NOT USE" is selected, the reset function is not activated even if K00 through K03 are entered. When "USE K00, K01" is selected, the system is reset immediately the K00 and K01 inputs go high at the same time. Similarly, the system is reset as soon as the K00 through K02 inputs or the K00 through K03 inputs go high.

However, the system is reset when a high signal is input for more than a rule time (1-3 sec).

The system reset circuit is shown in Figure 4.3.3.

Fig. 4.3.3 System reset circuit

# 3 Interrupt noise rejector

```
*** OPTION NO.3 ***
--- INTERRUPT NOISE REJECTOR ---

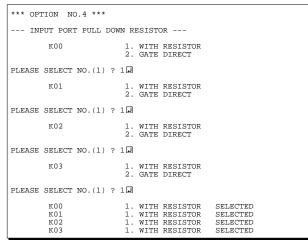
K00-K03 1. USE
2. NOT USE

PLEASE SELECT NO.(1) ? 1 2

K00-K03 1. USE SELECTED
```

Select whether noise rejector will be supplemented to the input interrupter of K00–K03. When "USE" is selected, the entry signal will pass the noise rejector, and occurrence of interrupt errors due to noise or chattering can be avoided. Note, however, that because the noise rejector performs entry signal sampling at 4 kHz, "NOT USE" should be selected when high speed response is required.

# 4 Input ports pull down resistor



Select whether input ports (K00–K03) will each be supplemented with pull down resistors or not. When "GATE DIRECT" is selected, see to it that entry floating state does not occur. Select "WITH RESISTOR" pull down resistor for unused ports. Moreover, the input port status is changed from "H" level (VDD) to "L" level (VSS) with pull down resistors, a delay of approximately 1 msec in waveform fall time will occur depending on the pull down resistor and entry load time constant. Because of this, when input reading is to be conducted, ensure the appropriate wait time with the program. The configuration of the pull down resistor circuit is shown in Figure 4.3.4.

VDD

VDD

Data bus

Read signal

Vss

Fig. 4.3.4 Configuration of pull down resistor

J 1

**EPSON** 

## 5 R00 specification

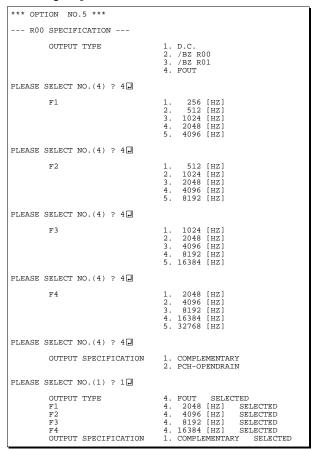




Fig. 4.3.5 Output waveform at DC output selection



Fig. 4.3.6 Output waveform at buzzer inverted output selection

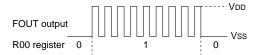
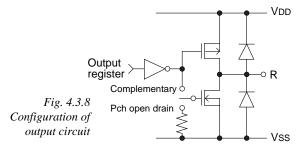


Fig. 4.3.7 Output waveform at FOUT output selection



Select the output specification for the R00 terminal. Either complementary output or Pch open drain output may be selected.

When "D.C." (DC output) is selected, R00 becomes a regular output port.

When "/BZ R00" (buzzer inverted output, R00 control) is selected, by writing "1" to the R00 register, clock with frequency specified through the software is generated from the R00 terminal. When "/BZ R01" (buzzer inverted output, R01 control) is selected, by writing "1" to the R01 register, clock with frequency specified through the software is generated from the R00 terminal.

When FOUT is selected, clock with frequency selected from the R00 terminal is generated by writing "1" to the R00 register.

When the DC output or buzzer inverted output is selected as the output type, the FOUT frequencies cannot be selected.

- When DC output is selected When the R00 register is set to "1", the R00 terminal output goes high (VDD), and goes low (Vss) when set to "0". Output waveform is shown in Figure 4.3.5.
- When buzzer inverted output (R00 control) is selected

When the R00 register is set to "1", 50% duty and VDD-Vss amplitude square wave is generated at the specified frequency by the software. When set to "0", the R00 terminal goes low (Vss). The clock phase when buzzer drive signal is output from R00 terminal is antiphase to that of the R01 terminal. Output waveform is shown in Figure 4.3.6.

When buzzer inverted output (R01 control) is selected

When the R01 register is set to "1", 50% duty and VDD-Vss amplitude square wave is generated at the specified frequency by the software. When set to "0", the R00 terminal goes low (Vss). The clock phase when buzzer drive signal is output from the R00 terminal is antiphase to that of the R01 terminal. Output waveform is shown in Figure 4.3.6.

When FOUT output is selected

When the R00 register is set to "1", 50% duty and VDD-Vss amplitude square wave is generated at the specified frequency. When set to "0", the FOUT terminal goes low (Vss).

The F1 to F4 FOUT frequencies are set by mask option. One of them is used by the software. FOUT output is normally utilized to provide clock to other devices but since hazard occurs at the square wave breaks, great caution must be observed when using it.

Output waveform is shown in Figure 4.3.7.

The output circuit configuration is shown in Figure 4.3.8.

# 6 R01 specification

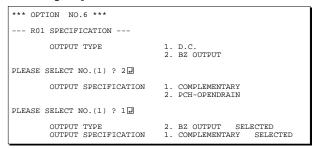




Fig. 4.3.9 Output waveform at DC output selection

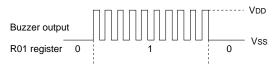


Fig. 4.3.10 Output waveform at buzzer output selection

Select the output specification for the R01 terminal. Either complementary output or Pch open drain output may be selected.

When "D.C." (DC output) is selected, R01 becomes a regular output port.

When "BZ OUTPUT" (buzzer output) is selected, by writing "1" to the R01 register, clock with frequency specified through the software is generated from the R01 terminal.

# • When DC output is selected When the R01 register is set to "1", the R01 terminal output goes high (VDD), and goes low (VSS) when set to "0". Output waveform is shown in Figure 4.3.9.

#### When buzzer output is selected

When the R01 register is set to "1", 50% duty and VDD-VSS amplitude square wave is generated at the specified frequency by the software. When set to "0", the R01 terminal goes low (VSS). The clock phase when buzzer drive signal is output from the R01 terminal is antiphase to that of the R00 terminal.

Output waveform is shown in Figure 4.3.10.

# 7 Output port output specification (R02, R03)

*** OPTION NO.7 ***		
OUTPUT PORT SPECIFICATION		
R02	1. COMPLEMENTARY 2. PCH-OPENDRAIN	
PLEASE SELECT NO.(1) ? 24		
R03	1. COMPLEMENTARY 2. PCH-OPENDRAIN	
PLEASE SELECT NO.(1) ? 2		
R02 R03	2. PCH-OPENDRAIN SELECTED 2. PCH-OPENDRAIN SELECTED	

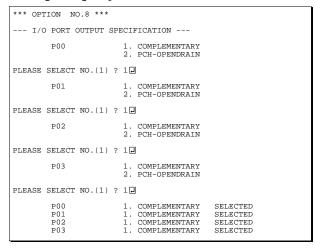
Select the output specification for the R02 and R03 output ports.

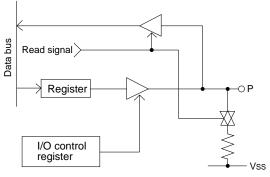
Either complementary output or Pch open drain output may be selected.

When output port is to be used on key matrix configuration, select Pch open drain output. For unused output ports, select complementary output

The circuit configuration is the same as that of output ports (R00 shown in Figure 4.3.8).

## 8 I/O port specification





Select the output specification to be used during I/O ports (P00–P03) output mode selection.

Either complementary output or Pch open drain output may be selected.

The circuit configuration of the output driver is the same as that of output ports (R00 shown in Figure 4.3.8).

Select complementary output for unused ports. The I/O ports can control the input/output direction according to the IOC bit (FC address, D0 bit); at "1" and "0" settings, it is set to output port and input

The pull down resistor of this port is turned on by the read signal and is normally turned off to minimize leak current. Because of this, when the port is set for input, take care that a floating state does not occur in the terminal.

The circuit configuration of the I/O port is shown in Figure 4.3.11.

Fig. 4.3.11
Configuration of I/O port

port, respectively.

## 9 LCD common duty and bias

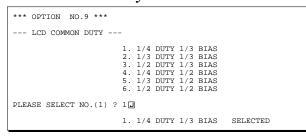


Table 4.3.1 Common duty selection standard

	·
Number of segments	Common duty
1–52	1/2
53–78	1/3
79–104	1/4

Select the common (drive) duty and bias.

When 1/2 duty is selected, up to 52 segments of LCD panel can be driven with 2 COM terminals and 26 SEG terminals. When 1/3 duty is selected, up to 78 segments can be driven with 3 COM terminals, and when 1/4 duty is selected, up to 104 segments with 4 COM terminals.

When 1/2 duty is selected, the COM0 and COM1 terminals are effective for COM output and the COM2 and COM3 terminals always output an off signal. When 1/3 duty is selected, the COM0 to COM2 terminals are effective and the COM3 terminal always outputs an off signal. Refer to Table 4.3.1 for common duty selection.

For the LCD drive bias, either 1/3 bias (drives LCD with 4 levels, VDD, VL1, VL2 and VL3) or 1/2 bias (drives LCD with 3 levels, VDD, VL1=VL2 and VL3) can be selected.

By selecting 1/2 bias, external elements can be minimized (see Figure 4.3.2). However, it is limited when the LCD system voltage regulator is not used. Furthermore, when 1/2 bias is selected, be sure to short between the VL1 terminal and the VL2 terminal outside the IC.

Figures 4.3.12 and 4.3.13 show the drive waveforms of 1/3 bias driving and 1/2 bias driving, respectively.

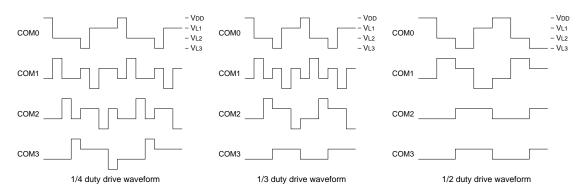


Fig. 4.3.12 Drive waveform from COM terminals (1/3 bias)

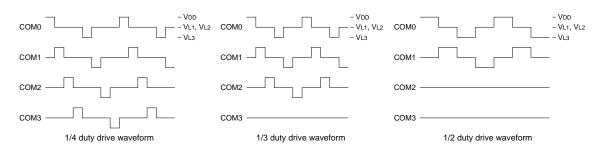


Fig. 4.3.13 Drive waveform from COM terminals (1/2 bias)

## 10 OSC1 system clock

```
*** OPTION NO.10 ***
--- OSC1 SYSTEM CLOCK ---

1. CRYSTAL
2. CR

PLEASE SELECT NO.(1) ? 1

1. CRYSTAL SELECTED
```

Select oscillation circuit that uses OSC1 and OSC2. To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, crystal oscillation circuit would be suitable.

When CR oscillation circuit is selected, only resistors are needed as external components since capacities are built-in.

On the other hand, when crystal oscillation circuit is selected, crystal oscillator and trimmer capacitor are needed as external components. Although when crystal oscillation circuit is selected, it is fixed at 32.768 kHz, when CR oscillation circuit is selected, frequency may be modified to a certain extent depending on the resistance of external components.

# 4.4 FOG6S37 Quick Reference

#### Starting command and input/output files

Execution file: FOG6S37.EXE

Starting command: FOG6S37 I indicates the Return key.

*Input file:* CS37XXXF.DOC (Function option document file, when modifying)

Output file: CS37XXXF.DOC (Function option document file)
CS37XXXF.HEX (Function option HEX file)

#### ■ Display example

ſ	***	E0C6S37 FUNC	TION OPT	ION GENER	ATOR	Ver 3.	15 ***	
	EEEEEEEE	PPPPPPPP	S	SSSSSS	0000	00000	NNN	NNN
	EEEEEEEEE	PPPPPPPPP	ss s	S SSSS	000	000	NNNN	NNN
	EEE	PPP PI	PP SSS	SSS	000	000	NNNNN	NNN
	EEE	PPP PI	PP SS	S	000	000	NNNNNN	NNN
	EEEEEEEEE	PPPPPPPPP	e s	SSSSS	000	000	NNN NN	N NNN
	EEEEEEEEE	PPPPPPPP		SSSS	000	000	NNN N	NNNNN
	EEE	PPP		SSS	000	000	NNN	NNNNN
	EEE	PPP	SSS	SSS	000	000	NNN	NNNN
	EEEEEEEEE	PPP	SSS	S SSS	000	000	NNN	NNN
	EEEEEEEEE	PPP	S	SSSSSS	0000	00000	NNN	NN
		(C) COPYI	RIGHT 19	94 SEIKO	EPSON (	CORP.		
	Т	HIS SOFTWARE	MAKES N	EXT FILES				
		CS37XXXF.HI		FUNCTION FUNCTION	OPTION OPTION			

```
*** EOC6S37 USER'S OPTION SETTING. --- Ver 3.15 ***

CURRENT DATE IS 94/12/26

PLEASE INPUT NEW DATE : 94/12/28
```

STRIKE ANY KEY.

```
*** OPERATION SELECT MENU ***

1. INPUT NEW FILE
2. EDIT FILE
3. RETURN TO DOS

PLEASE SELECT NO.?
```

```
*** OPERATION SELECT MENU ***

1. INPUT NEW FILE
2. EDIT FILE
3. RETURN TO DOS

PLEASE SELECT NO.? 1 PLEASE INPUT FILE NAME? CS370A0 PLEASE INPUT FILE NAME? CS370A0 CORP. C.(1)
PLEASE INPUT LIVER'S NAME? SEIKO EPSON CORP. C.(2)
PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)? FUJIMI PLANT COMENT
? 281 FUJIMI SUWA-GUN NAGANO-KEN 399-0200 JAPAN PROBLEM PROBLEM
```

```
PLEASE INPUT FILE NAME? CS370A0 
EXISTS OVERNITE(Y/N)? NU
PLEASE INPUT FILE NAME? CS370B0 
PLEASE INPUT USER'S NAME?
```

#### Start-up message

When FOG6S37 is started, the start-up message is displayed.

For "STRIKE ANY KEY.", press any key to advance the program execution.

To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

#### Date input

Enter the 2-digit year, month, and day of the month by delimiting them with a slash ("/"). When not modifying the date, press the RETURN key " []" to continue.

#### Operation selection menu

Enter a number from 1 to 3 to select a subsequent operation.

- 1. To set new function options.
- 2. To modify the document file.
- To terminate FOG6S37.

#### Setting new function options

Select "1" on the operation selection menu.

- (1) Enter the file name.
- (2) Enter the customer's company name.
- (3) Enter any comment.

(Within 50 characters x 10 lines) Next, start function option setting from option No. 1.

In case a function option document file with the same name as the file name specified in the current drive exists, the user is asked whether overwrition is desired. Enter "Y" or "N" accordingly.

```
*** OPERATION SELECT MENU ***
           1. INPUT NEW FILE
          2. EDIT FILE
3. RETURN TO DOS
PLEASE SELECT NO.? 2
*** SOURCE FILE(S) ***
CS370A0
                     CS370B0
                                            CS370C0
                                                                          ..(1)
PLEASE INPUT FILE NAME? CS370A0
                                                                          ..(2)
PLEASE INPUT USER'S NAME? PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)? PLEASE INPUT EDIT NO.? 4
                                                                          . . (3)
                                                                          ..(4)
(Modifying function option settings)
PLEASE INPUT EDIT NO.? E
```

In step (1), if no modifiable source exists, the following message is displayed and the sequence returns to the operation selection menu.

```
*** SOURCE FILE(S) ***
FUNCTION OPTION DOCUMENT FILE IS NOT FOUND.
```

In step (2), if the function option document file is not in the current drive, the following message is displayed, prompting entry of other file name.

```
PLEASE INPUT FILE NAME? CS370NO PUNCTION OPTION DOCUMENT FILE IS NOT FOUND.
PLEASE INPUT FILE NAME?
```

```
*** OPTION NO.2 ***

--- MULTIPLE KEY ENTRY RESET ---

COMBINATION 1. Not Use
2. Use K00,K01
3. Use K00,K01,K02
4. Use K00,K01,K02,K03

PLEASE SELECT NO.(1) ? 2  

COMBINATION 2. Use K00,K01 SELECTED
```

```
END OF OPTION SETTING
DO YOU MAKE HEX FILE (Y/N) ? Y
                                                         ..(1)
*** OPTION EPROM SELECT MENU ***
        1. 27C64
2. 27C128
           27C256
        4. 27C512
PLEASE SELECT NO.? 24
                                                         ..(2)
        2. 27C128 SELECTED
MAKING FILE(S) IS COMPLETED.
*** OPERATION SELECT MENU ***
        1. INPUT NEW FILE
        2. EDIT FILE
        3. RETURN TO DOS
PLEASE SELECT NO.?
```

#### Modifying function option settings

Select "2" on the operation selection menu.

- (1) Will display the files on the current drive.
- (2) Enter the file name.
- (3) Enter the customer's company name.
- (4) Enter any comment. Previously entered data can be used by pressing the RETURN key "☐" at (3) and (4).
- (5) Enter the number of the function option to be modified. When selection of one option is complete, the system prompts entry of another function option number. Repeat selection until all options to be modified are selected. Enter "E⊒" to end option setting. Then, move to the confirmation procedure for HEX file generation.

#### **Option** selection

The selections for each option correspond one to one to the option list. Enter the selection number. The value in parentheses ( ) indicates the default value, and is set when only the RETURN key "" is pressed.

In return, the confirmation is displayed. When you wish to modify previously set function options in the new setting process, enter "B 🖃" to return 1 step back to the previous function option setting operation.

#### EPROM selection

When setting function options setting is completed, the following message is output to ask the operator whether to generate the HEX file.

- (2) For the option ROM selection menu displayed when "Y☐" is entered in Step (1), select the EPROM to be used for setting evaluation board options.

When a series of operations are complete, the sequence returns to the operation selection menu.

# 4.5 Sample File

#### ■ Example of function option document file

```
* E0C6S37 FUNCTION OPTION DOCUMENT V 3.15
* FILE NAME
            CS370A0F.DOC
* USER'S NAME SEIKO EPSON CORP.
* INPUT DATE 1994/12/26
* COMMENT
            FUJIMI PLANT
            281 FUJIMI SUWA-GUN NAGANO-KEN 399-0200 JAPAN
            TEL 0266-61-1211
            FAX 0266-61-1273
* OPTION NO.1
* < DEVICE TYPE & LCD POWER VREG >
                       E0C6SL37 VREG USE LCD 3V -- SELECTED
OPT0101 02
OPT0103 01
* OPTION NO.2
* < MULTIPLE KEY ENTRY RESET >
    COMBINATION USE K00,K01, K02, K03 ----- SELECTED
OPT0201 04
* OPTION NO.3
 < INTERRUPT NOISE REJECTOR >
                           ----- SELECTED
                     USE
   K00-K03
OPT0301 01
* OPTION NO.4
 < INPUT PORT PULL DOWN RESISTOR >
                        WITH RESISTOR
                                    ----- SELECTED
                        WITH RESISTOR ----- SELECTED
    K01
    K02
                        WITH RESISTOR ----- SELECTED
                        WITH RESISTOR ----- SELECTED
    K03
OPT0401 01
OPT0402 01
OPT0403 01
OPT0404 01
* OPTION NO.5
* < R00 SPECIFICATION >
    OUTPUT TYPE
                        FOUT ----- SELECTED
                        512 (HZ) ----- SELECTED
    F1
                                ----- SELECTED
    F2
                        1024 (HZ)
    F3
                        2048 (HZ)
                                ----- SELECTED
                        4096 (HZ)
    OUTPUT SPECIFICATION COMPLEMENTARY ----- SELECTED
OPT0501 04
OPT0502 02
OPT0503 02
OPT0504 02
OPT0505 02
OPT0506 01
* OPTION NO.6
* < R01 PORT OUTPUT SPECIFICATION >
    OUTPUT TYPE
                    DC ----- SELECTED
    OUTPUT SPECIFICATION COMPLEMENTARY ----- SELECTED
OPT0601 01
OPT0602 01
* OPTION NO.7
* < OUTPUT PORT SPECIFICATION >
                     COMPLEMENTARY ----- SELECTED
    R03
                        COMPLEMENTARY ----- SELECTED
OPT0701 01
OPT0702 01
```

```
* OPTION NO.8
 < I/O PORT OUTPUT SPECIFICATION >
                          COMPLEMENTARY ----- SELECTED
                          COMPLEMENTARY ----- SELECTED
     P01
                          COMPLEMENTARY ----- SELECTED
     P02
     P03
                          COMPLEMENTARY ----- SELECTED
OPT0801 01
OPT0802 01
OPT0803 01
OPT0804 01
* OPTION NO.9
* < LCD COMMON DUTY AND BIAS >
                         1/4 DUTY 1/3 BIAS ----- SELECTED
OPT0901 01
* OPTION NO.10
* < OSC 1 SYSTEM CLOCK >
                          CRYSTAL ----- SELECTED
OPT1001 01
* SEIKO EPSON'S AREA
* OPTION NO.11
OPT1101 01
OPT1102 01
OPT1103 01
OPT1104 01
* OPTION NO.12
OPT1201 01
OPT1202 01
OPT1203 01
OPT1204 01
* OPTION NO.13
OPT1301 01
OPT1302 01
* OPTION NO.14
OPT1401 01
OPT1402 01
* OPTION NO.15
OPT1501 01
* OPTION NO.16
OPT1601 01
* OPTION NO.17
OPT1701 01
\\END
```

Note End mark "\\\ END" may be used instead of "\\\ END" depending on the PC used. (The code of \\ and \\ \cdot is 5CH.)

# 5 SEGMENT OPTION GENERATOR SOG6S37

## 5.1 SOG6S37 Outline

With the 4-bit single-chip S1C6S3N7 microcomputers, the customer may select the LCD segment options. By modifying the mask patterns of the S1C6S3N7 according to the selected options, the system can be customized to meet the specifications of the target system.

The Segment Option Generator SOG6S37 is a software tool for generating data file used to generate mask patterns. From the data file created with SOG6S37, the S1C6S3N7 mask pattern is automatically generated by a general purpose computer. The HEX file for the evaluation board (S5U1C62N51E1) segment option ROM is simultaneously generated with the data file.

The operating method is same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

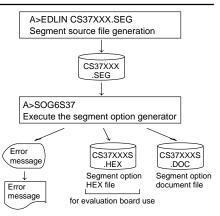


Fig. 5.1.1 SOG6S37 execution flow

# 5.2 Option List

TEDMINIAL	ADDRESS						S						
TERMINAL		ОМ	0		СОМ	1	COM2 COM3		3	OUTPUT SPECIFICATION			
NAME	Н	┙	D	Н	L	D	Н	┙	D	Н	┙	D	
SEG0													SEG output
SEG1													DC output ☐ C ☐ P
SEG2													SEG output
SEG3													DC output ☐ C ☐ P
SEG4													SEG output
SEG5													DC output ☐ C ☐ P
SEG6													SEG output
SEG7													DC output ☐ C ☐ P
SEG8													SEG output
SEG9													DC output ☐ C ☐ P
SEG10													SEG output
SEG11													DC output ☐ C ☐ P
SEG12													SEG output
SEG13													DC output ☐ C ☐ P
SEG14													SEG output
SEG15													DC output □ C □ P
SEG16													SEG output
SEG17													DC output ☐ C ☐ P
SEG18													SEG output
SEG19													DC output ☐ C ☐ P
SEG20													SEG output
SEG21													DC output ☐ C ☐ P
SEG22													SEG output
SEG23													DC output ☐ C ☐ P
SEG24													SEG output
SEG25													DC output ☐ C ☐ P
Legend:	< <i>F</i>	ADD:	RES	S>			•			•			<output specification=""></output>
	H: High order address, L: Low order address								ess		C: Complementary output		
		D: Data bit											P: Pch open drain output

#### Note:

20

- 1. Even if there are unused areas, set "---" (hyphens) such that there are no blank columns.
- 2. When DC output is selected, the display memory of the COM0 column becomes effective.

# 5.3 Segment Ports Output Specifications

For the output specification of the segment output ports SEG0–SEG25, segment output and DC output can be selected in units of two terminals. When used for liquid crystal panel drives, select segment output; when used as regular output port, select DC output. When DC output is selected, either complementary output or Pch open drain output may further be selected.

However, for segment output ports that will not be used, select segment output.

Refer to the "S1C62 Family Development Tool Reference Manual" for the segment option source file creation.

#### ■ When segment output is selected

The segment output port has a segment decoder built-in, and the data bit of the optional address in the segment memory area (090H–0AFH) can be allocated to the optional segment. With this, up to 104 segments (78 segments when 1/3 duty is selected or 52 segments when 1/2 duty is selected) of liquid crystal panel could be driven.

The segment memory may be allocated only one segment and multiple setting is not possible. The allocated segment displays when the bit for this segment memory is set to "1", and goes out when bit is set to "0".

Segment allocation is set to H for high address (9–A), to L for low address (0–F), and to D for data bit (0–3) and are recorded in their respective column in the option list. For segment ports that will not be used, write "---" (hyphen) in the H, L, and D columns of COM0–COM3.

#### Examples

```
• When 1/4 duty is selected
 0 900
                      903
         901
               902
    910
          911
                912
                      913
                           S
• When 1/3 duty is selected
   900 901 902
                            S
    910
          911
                912
• When 1/2 duty is selected
 0 900 901
                            S
               ___
    910
          911
                ---
```

#### When DC output is selected

The DC output can be selected in units of two terminals and up to 26 terminals may be allocated for DC output. Also, either complementary output or Pch open drain output is likewise selected in units of two terminals. When the bit for the selected segment memory is set to "1", the segment output port goes high (VDD), and goes low (Vss) when set to "0". Segment allocation is the same as when segment output is selected but for the while the segment memory allocated to COM1–COM3 becomes ineffective. Write three hyphens ("---") in the COM1–COM3 columns in the option list.

#### Example

• When complementary output is set to SEG22 and SEG23, and Pch open drain output is set to SEG24 and SEG25.

```
22 A00 --- --- C
23 A10 --- --- C
24 A21 --- P
25 A31 --- P
```

Note Only complementary output is enabled as the DC output of the SEG ports of the evaluation board. Therefore, complementary output is enabled even if Pch open drain output is selected. Respond to it by adding external circuits as required.

# 5.4 SOG6S37 Quick Reference

#### Starting command and input/output files

Execution file: SOG6S37.EXE

\_ indicates a blank.

indicates the Return key.

Starting command: SOG6S37\_ [-H] A parameter enclosed by [ ] can be omitted.

Input file: CS37XXX.SEG (Segment option source file)

CS37XXXS.DOC (Segment option document file, when -H option use)

-H: Specifies the segment option document file for input file of SOG6S37.

Output file: CS37XXXS.DOC (Segment option document file)

CS37XXXS.HEX (Segment option HEX file)

#### Display example

Option:

*** E	OC6S37 SEGMENT	OPTION GENE	RATOR	- Ver 3.0	00 ***						
EEEEEEEEE	PPPPPPPP	SSSSSSS	000	00000	NNN	NNN					
EEEEEEEEE	PPPPPPPPPP	SSS SSS	SS 000	000	NNNN	NNN					
EEE	PPP PPP	SSS SS	SS 000	000	NNNNN	NNN					
EEE	PPP PPP	SSS	000	000	NNNNNN	NNN					
EEEEEEEEE	PPPPPPPPPP	SSSSSS	000	000	NNN NNN	I NNN					
EEEEEEEEE	PPPPPPPP	SSSS	000	000	NNN NN	INNNN					
EEE	PPP	SSS	000	000	NNN N	INNNN					
EEE	PPP	SSS SS	SS 000	000	NNN	NNNN					
EEEEEEEEE	PPP	SSSS SS	SS 000	000	NNN	NNN					
EEEEEEEEE	PPP	SSSSSSS	000	00000	NNN	NN					
		STRIKE ANY F	EY.								

\*\*\* E0C6S37 USER'S OPTION SETTING. --- Ver 3.00 \*\*\*

CURRENT DATE IS 94/12/26

PLEASE INPUT NEW DATE : 94/12/28

```
*** SOURCE FILE(S) ***

SEGMENT OPTION SOURCE FILE IS NOT FOUND. ...(5) -H option not use

*** SOURCE FILE(S) ***

SEGMENT OPTION DOCUMENT FILE IS NOT FOUND. ...(6) -H option use
```

```
PLEASE INPUT SEGMENT OPTION SOURCE FILE NAME? CS370NO SEGMENT OPTION SOURCE FILE IS NOT FOUND. ...(7) -H option not use

PLEASE INPUT SEGMENT OPTION DOCUMENT FILE NAME? CS370NO SEGMENT OPTION DOCUMENT FILE IS NOT FOUND. ...(8) -H option use
```

#### Start-up message

When SOG6S37 is started, the start-up message is displayed.

For "STRIKE ANY KEY.", press any key to advance the program execution.

To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

#### Date input

Enter the 2-digit year, month, and day of the month by delimiting them with a slash ("/"). When not modifying the date, press the RETURN key " [ ]" to continue.

#### Input file selection

- (1) Will display the files on the current drive.
- (2) Enter the file name.
- (3) Enter the customer's company name.
- (4) Enter any comment.

(Within 50 characters x 10 lines)

Then, move to the confirmation procedure for HEX file generation.

In step (1), if no modifiable source exists, an error message (5) or (6) will be displayed and the program will be terminated. In step (2), if the specified file name is not found in the current drive, an error message (7) or (8) is displayed, prompting entry of other file name.

```
END OF OPTION SETTING.

DO YOU MAKE HEX FILE (Y/N) ? Y ...(1)

*** OPTION EPROM SELECT MENU ***

1. 27C64
2. 27C128
3. 27C256
4. 27C512

PLEASE SELECT NO.? 2 ...(2)
2. 27C128 SELECTED

MAKING FILE IS COMPLETED.
```

#### EPROM selection

When selecting file is completed, the following message is output to ask the operator whether to generate the HEX file.

- (1) When debugging the program with the evaluation board, HEX file is needed, so enter "Y ]. If "N ]" is entered, no HEX file is generated and only document file is generated.
- (2) For the option ROM selection menu displayed when "Y !=" is entered in Step (1), select the EPROM to be used for setting evaluation board options.

When a series of operations are complete, the SOG6S37 generates files. If no error is committed while setting segment options, "MAKING FILE IS COMPLETED" will be displayed and the SOG6S37 program will be terminated.

#### ■ Error messages

	Error message	Explanation
S	(Syntax Error)	The data was written in an invalid format.
N	(Segment No. Select Error)	The segment number outside the specificable range was specified.
R	(RAM Address Select Error)	The segment memory address or data bit outside the specificable range was specified.
D	(Duprication Error)	The same data (SEG port No., segment memory address, or data bit) was specified
		more then once.
Out Port Set Error		The output specifications were not set in units of two ports.

# 5.5 Sample Files

#### Example of segment option source file

```
; CS370A0.SEG, VER.3.00
 LCD SEGMENT DECODE TABLE
 0
      901
            900
                 932
                                     ;1st DIGIT
                       AEO S
      912
            911
                  910
                       923 S
      913
            920
                  921
                       922 S
 3
      AC0
            902
                  930
                       931 S
      941
            940
                  972
                       AE1 S
                                     ;2nd DIGIT
 5
      952
            951
                  950
                       963 S
 6
      953
            960
                  961
                       962 S
      AC1
            942
                  970
                       971 S
8
      981
            980
                  9B2
                       AE2 S
                                     ;3rd DIGIT
 9
      992
            991
                  990
                       9A3 S
10
      993
            9A0
                  9A1
                       9A2 S
11
      AC2
            982
                  9B0
                       9B1 S
12
      9C1
            9C0
                  9F2
                       AE3 S
                                     ;4th DIGIT
13
      9D2
            9D1
                  9D0
                       9E3 S
            9E0
                       9E2 S
14
      9D3
                  9E1
15
      AC3
            9C2
                  9F0
                       9F1 S
16
      A01
            A00
                 A32
                       AF0 S
                                     ;5th DIGIT
17
      A12
                       A23 S
            A11
                 A10
18
      A13
            A20
                  A21
                       A22
      AD0
                 A30
19
            A02
                       A31 S
20
      A41
            A40
                 A72
                       AF1 S
                                     ;6th DIGIT
21
      A52
            A51
                  A50
                       A63 S
22
      A53
            A60
                 A61
                       A62 S
23
      AD1
                 A70
                       A71 S
            A42
24
      AD3
            ___
                  ___
                       --- C
                                     ; DC OUTPUT
25
      AF3
            ___
                  ___
```

#### Example of segment option document file

```
* E0C6S37 SEGMENT OPTION DOCUMENT V 3.00
                CS370A0S.DOC
 FILE NAME
 USER'S NAME
                SEIKO EPSON CORP.
  INPUT DATE
                 94/12/26
  COMMENT
                FUJIMI PLANT
                 281 FUJIMI SUWA-GUN NAGANO-KEN 399-0200 JAPAN
                TEL 0266-61-1211
                FAX 0266-61-1273
  OPTION NO.11
  < LCD SEGMENT DECODE TABLE >
  SEG COM0 COM1 COM2 COM3 SPEC
      901
   0
            900
                 932
                       AE0
      912
                       923
   1
            911
                  910
                             S
   2
      913
            920
                  921
                       922
                             S
   3
      AC0
            902
                  930
                       931
                             S
   4
      941
            940
                  972
                       AE1
      952
                  950
   5
            951
                       963
                             S
   б
      953
            960
                  961
                       962
                             S
      AC1
            942
                  970
                       971
   8
      981
            980
                  9B2
                       AE2
                             S
   9
      992
            991
                  990
                       9 A 3
  10
      993
            9A0
                  9A1
                       9A2
                             S
  11
      AC2
            982
                  9B0
                       9B1
                             S
  12
      9C1
            900
                  9F2
                             S
                       AE3
  13
      9D2
            9D1
                  9D0
                       9E3
                             S
  14
      9D3
            9E0
                  9E1
                       9E2
  15
      AC3
            9C2
                  9F0
                       9F1
  16
      A01
            A00
                  A32
                       AF0
                             S
  17
      A12
            A11
                  A10
                       A23
  18
      A13
            A20
                  A21
                       A22
                             S
  19
      AD0
            A02
                  A30
                       A31
                             S
  20
      A41
            A40
                  A72
                       AF1
                             S
  21
      A52
            A51
                  A50
                       A63
  22
                             S
      A53
            A60
                       A62
                  A61
  23
      AD1
            A42
                  A70
                       A71
                             S
                                                Note End mark "¥¥END" may be used instead
  24
      AD3
            A80
                  AB2
                       AF2
                             C
                                                       of "\END" depending on the PC used.
  25
            A91
                 A90
                       AA3
                             C
      AF3
\\END
                                                       (The code of \ and \ is 5CH.)
```

# 6 ICE CONTROL SOFTWARE ICS6S37

#### 6.1 ICS6S37 Outline

The In-Circuit Emulator (S5U1C62000H) connects the target board produced by the user via the evaluation board (S5U1C62N51E1) and performs real time target system evaluation and debugging by passing through the RS-232C from the host computer and controlling it. The operation on the host computer side and ICE (S5U1C62000H) control is done through the ICE Control Software ICS6S37.

The ICS6S37 has a set of numerous and highly functional emulation commands which provide sophisticated break function, on-the-fly data display, history display, etc., and so perform a higher level of debugging.

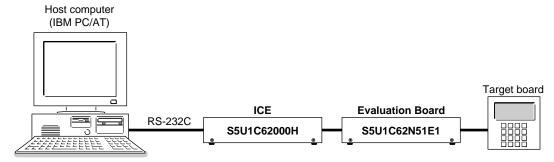


Fig. 6.1.1 Debugging system using ICE

The functions of the ICE and commands are same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

# 6.2 ICS6S37 Restrictions

Take the following precautions when using the ICS6S37.

#### ■ ROM Area

The ROM area is limited to a maximum address of 3FFH. Assigning data above the 3FFH address causes an error.

#### ■ RAM Area

The RAM area is limited to a maximum address of 0FFH. However, as the following addresses are in the unused area, designation of this area with the ICE commands produces an error.

Unused area: 050H to 08FH, 0B0H to 0DFH

Memory 090H to 0AFH is display memory; 0E0H to 0FFH is I/O memory. (Refer to the "S1C6S3N7 Technical Manual" for details.)

#### ■ Undefined Code

The instructions below are not specified for the S1C6S3N7 and so cannot be used.

SLP							
PUSH	XP	POP	ΧP	LD	XP,r	LD	r,XP
PUSH	ΥP	POP	ΥP	ΙΓ	) YPr	ΙD	r YP

#### **■** OPTLD Command

In the ICS6S37, OPTLD command cannot be used.

# 6.3 ICS6S37 Quick Reference

#### ■ Starting command and input/output files

Execution file: ICS6S37B.BAT (ICS6S37W.EXE)

Starting command: ICS6S37B (ICS6S37W)

Input file: CS37XXXL.HEX (Object file, low-order)

CS37XXXH.HEX (Object file, high-order)

CS37XXXD.HEX (Data RAM file) CS37XXXC.HEX (Control file)

Output file: CS37XXXL.HEX (Object file, low-order)

CS37XXXH.HEX (Object file, high-order) CS37XXXD.HEX (Data RAM file)

CS37XXXC.HEX (Control file)

#### **■** Display example

**	** E0C6S37 ICE	CONTRO	L SOFTW.	ARE	Ver 3.0	01 ***	
EEEEEEEEE	PPPPPPPP	SSS	SSSS	0000	0000	NNN	NNN
EEEEEEEEE	PPPPPPPPPP	SSS	SSSS	000	000	NNNN	NNN
EEE	PPP PPP	SSS	SSS	000	000	NNNNN	NNN
EEE	PPP PPP	SSS		000	000	NNNNN	NNN I
EEEEEEEEE	PPPPPPPPPP	SSS	SSS	000	000	NNN NN	IN NNN
EEEEEEEEE	PPPPPPPP	:	SSSS	000	000	NNN 1	NNNNN
EEE	PPP		SSS	000	000	NNN	NNNNN
EEE	PPP	SSS	SSS	000	000	NNN	NNNN
EEEEEEEEE	PPP	SSSS	SSS	000	000	NNN	NNN
EEEEEEEEE	PPP	SSS	SSSS	0000	0000	NNN	NN
	(C) COPYRIGH	HT 1991	SEIKO :	EPSON CO	RP.		
* ICE POWER * DIAGNOSTIC #							

#### Start-up message

When ICS6S37 is started, the start-up message is displayed, and a self-test is automatically performed. ICS6S37 commands are awaited when the program is properly loaded and the # mark is displayed.

Debugging can be done by entering command after the # mark.

☐ indicates the Return key.

The ICS6S37 program is terminated by entering the Q (Quit) command.

Note Confirm that the cables connected properly, then operate the ICS6S37.

#### ■ Error messages

Error message	Meaning	Recover procedure			
* COMMUNICATION ERROR	ICE is disconnected or power	Switch OFF the host power supply, connect cable, and			
OR ICE NOT READY *	is OFF.	reapply power. Or switch ON power to ICE.			
* TARGET DOWN (1) *	Evaluation board is disconnected.	Switch OFF power to ICE, and connect the evaluation			
	(Check at power ON)	board. Then, apply power to ICE.			
* TARGET DOWN (2) *	Evaluation board is disconnected.	Switch OFF power to ICE, and connect the evaluation			
	(Check at command execution)	board. Then, apply power to ICE.			
* UNDEFINED PROGRAM	Undefined code is detected in the	Convert ROM and FD data with the cross assembler,			
CODE EXIST *	program loaded from ROM or FD.	then restart the ICE.			
* COMMAND ERROR *	A miss occurs by command input.	Reenter the proper command.			
(No response after power on)	The ICE-to-HOST cable is	Switch OFF the host power supply, connect cable,			
	disconnected on the host side.	and reapply power.			

# **■ ICE commands**

Item No.	Function	Command Format	Outline of Operation			
1	Assemble	#A,a <b>↓</b>	Assemble command mnemonic code and store at address "a"			
2	Disassemble	#L,a1,a2 ₽	Contents of addresses a1 to a2 are disassembled and displayed			
3	Dump	#DP,a1,a2 🎝	Contents of program area a1 to a2 are displayed			
		#DD,a1,a2 🔟	Content of data area a1 to a2 are displayed			
4	Fill	#FP,a1,a2,d 🗐	Data d is set in addresses a1 to a2 (program area)			
		#FD,a1,a2,d <b>→</b>	Data d is set in addresses a1 to a2 (data area)			
5	Set	#G,a↓	Program is executed from the "a" address			
	Run Mode	#TIM 🎝	Execution time and step counter selection			
		#OTF.J	On-the-fly display selection			
6	Trace	#T,a,n ↓	Executes program while displaying results of step instruction			
			from "a" address			
		#U,a,n ┛	Displays only the final step of #T,a,n			
7	Break	#BA,a ┛	Sets Break at program address "a"			
		#BAR,a ⋥	Breakpoint is canceled			
		#BD↓	Break condition is set for data RAM			
		#BDR ┛	Breakpoint is canceled			
		#BR ↓	Break condition is set for evaluation board CPU internal registers			
		#BRR ↓	Breakpoint is canceled			
		#BM 🎝	Combined break conditions set for program data RAM address			
			and registers			
		#BMR ↓	Cancel combined break conditions for program data ROM			
			address and registers			
		#BRES ↓	All break conditions canceled			
		#BC ┛	Break condition displayed			
		#BE 🎝	Enter break enable mode			
		#BSYN ┛	Enter break disable mode			
		#BT ┛	Set break stop/trace modes			
		#BRKSEL,REM ┛	Set BA condition clear/remain modes			
8	Move	#MP,a1,a2,a3 Д	Contents of program area addresses a1 to a2 are moved to			
			addresses a3 and after			
		#MD,a1,a2,a3 <b>⅃</b>	Contents of data area addresses a1 to a2 are moved to addresses			
			a3 and after			
9	Data Set	#SP,a ┛	Data from program area address "a" are written to memory			
		#SD,a↓	Data from data area address "a" are written to memory			
10	10 Change CPU #DR ☐ Display evaluation		Display evaluation board CPU internal registers			
	Internal	#SR ┛	Set evaluation board CPU internal registers			
	Registers	#I 🎝	Reset evaluation board CPU			
		#DXY 🗓	Display X, Y, MX and MY			
		#SXY↓	Set data for X and Y display and MX, MY			

#### 6 ICE CONTROL SOFTWARE ICS6S37

Item No.	Function	Command Format	Outline of Operation				
11	History	#H,p1,p2 ↓	Display history data for pointer 1 and pointer 2				
#HB <b>→</b>		#HB ↓	Display upstream history data				
		#HG ₽	Display 21 line history data				
		#HP↓	Display history pointer				
		#HPS,a ┛	Set history pointer				
		#HC,S/C/E	Sets up the history information acquisition before (S),				
			before/after (C) and after (E)				
		#HA,a1,a2 →	Sets up the history information acquisition from program area				
			a1 to a2				
		#HAR,a1,a2 <b>⅃</b>	Sets up the prohibition of the history information acquisition				
			from program area a1 to a2				
		#HAD 🎝	Indicates history acquisition program area				
		#HS,a ┛	Retrieves and indicates the history information which executed				
			a program address "a"				
		#HSW,a ⋥	Retrieves and indicates the history information which wrote or				
		#HSR,a ┛	read the data area address "a"				
12	File	#RF,file ┛	Move program file to memory				
		#RFD,file ₽	Move data file to memory				
		#VF,file 🎜	Compare program file and contents of memory				
		#VFD,file ₽	Compare data file and contents of memory				
		#WF,file ┛	Save contents of memory to program file				
		#WFD,file ┛	Save contents of memory to data file				
		#CL,file ┛	Load ICE set condition from file				
		#CS,file ┛	Save ICE set condition to file				
13	Coverage	#CVD-	Indicates coverage information				
		#CVR ┛	Clears coverage information				
14	ROM Access	#RP ┛	Move contents of ROM to program memory				
		#VP↓	Compare contents of ROM with contents of program memory				
		#ROM ₽	Set ROM type				
15	Terminate ICE	#Q 🗗	Terminate ICE and return to operating system control				
16	Command	#HELP •	Display ICE instruction				
	Display						
17	Self	#CHK ┛	Report results of ICE self diagnostic test				
	Diagnosis						

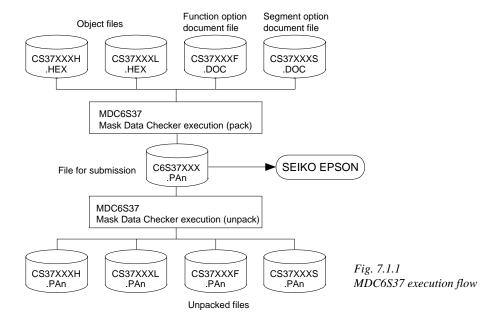
□ means press the RETURN key.

# 7 MASK DATA CHECKER MDC6S37

#### 7.1 MDC6S37 Outline

The Mask Data Checker MDC6S37 is a software tool which checks the program data (CS37XXXH.HEX and CS37XXXL.HEX) and option data (CS37XXXF.DOC and CS37XXXS.DOC) created by the user and creates the data file (C6S37XXX.PAn) for generating mask patterns. The user must send the file generated through this software tool to Seiko Epson.

Moreover, MDC6S37 has the capability to restore the generated data file (C6S37XXX.PA0) to the original file format.



The operating method is same as for the S1C62 Family. Refer to the "S1C62 Family Development Tool Reference Manual" for details.

# 7.2 MDC6S37 Quick Reference

#### Starting command and input/output files

Execution file:	MDC6S37.EXE	
Starting command:	MDC6S37 ⊒	indicates the Return key.
Input file:	CS37XXXL.HEX (Object file, low-order) CS37XXXH.HEX (Object file, high-order) CS37XXXF.DOC (Function option document file CS37XXXS.DOC (Segment option document file C6S37XXX.PAn (Packed file)	
Output file:	C6S37XXX.PAn (Packed file) CS37XXXL.PAn (Object file, low-order) CS37XXXH.PAn (Object file, high-order) CS37XXXF.PAn (Function option document file CS37XXXS.PAn (Segment option document file	′

#### ■ Display examples

	*** E0C6S37 PA	CK / UNI	PACK PR	OGRAM Ve	r 1.00	***	
EEEEEEEEE EEE EEE EEE EEE EEE EEE EEEEEE	PPPPPPPP PPP	SSS SSS SSS SSS SSS SSS SSS SSS SSS SS	SSSS SSSS SSS SSS SSS SSS SSS SSS SSS	0000 000 000 000 000 000 000 000	00000 000 000 000 000 000 000 000	NNN NNNN NNNNN NNNNN	MINI NINI NINI NINI NINI NINI NINI NINI
PLEASE SELECT NO.?							

#### 

#### Start-up message

When MDC6S37 is started, the start-up message and operation menu are displayed. Here, the user is prompted to select operation options.

#### Packing of data

- Select "1. PACK" in the operation menu.
- (2) Enter the file name.

  After submitting the data to Seiko
  Epson and there is a need to re-submit
  the data, increase the numeric value of
  "n" by one when the input is made.
  (Example: When re-submitting data
  after "C6S37XXX.PA0" has been
  submitted, the pack file name should be
  entered as "C6S37XXX.PA1".)

With this, the mask file (C6S37XXX.PAn) is generated, and the MDC6S37 program will be terminated.

Submit this file to Seiko Epson.

Note Don't use the data generated with the -N option of the Cross Assembler (ASM6S37) as program data. If the program data generated with the -N option of the Cross Assembler is packed, undefined program area is filled with FFH code. In this case, following message is displayed.

```
WARNING: FILLED <file_name> FILE WITH FFH.
```

#### Unpacking of data

- (1) Select "2. UNPACK" in the operation menu.
- (2) Enter the packed file name.

With this, the mask data file (C6S37XXX.PAn) is restored to the original file format, and the MDC6S37 program will be terminated.

Since the extension of the file name remains as "PAn", it must be renamed back to its original form ("HEX" and "DOC") in order to re-debug or modify the restored file.

### **■** Error messages

### Program data error

			Er	ror Message	Explanation
1.	HEX DA	TA ERROF	:	NOT COLON.	There is no colon.
2.	HEX DA	TA ERROF	:	DATA LENGTH. (NOT 00-20h)	The data length of 1 line is not in the 00–20H range.
3.	HEX DA	TA ERROF	:	ADDRESS.	The address is beyond the valid range of the program ROM.
4.	HEX DA	TA ERROF	:	RECORD TYPE. (NOT 00)	The record type of 1 line is not 00.
5.	HEX DA	TA ERROF	:	DATA. (NOT 00-FFh)	The data is not in the range between 00H and 0FFH.
6.	HEX DA	TA ERROF	:	TOO MANY DATA IN ONE LINE.	There are too many data in 1 line.
7.	HEX DA	TA ERROF	:	CHECK SUM.	The checksum is not correct.
8.	HEX DA	TA ERROF	:	END MARK.	The end mark is not: 00000001FF.
9.	HEX DA	TA ERROF	:	DUPLICATE.	There is duplicate definition of data in the same address.

### Function option data error

	Error Message	Explanation
1.	OPTION DATA ERROR : START MARK.	The start mark is not "\OPTION". (during unpacking) *
2.	OPTION DATA ERROR : OPTION NUMBER.	The option number is not correct.
3.	OPTION DATA ERROR : SELECT NUMBER.	The option selection number is not correct.
4.	OPTION DATA ERROR : END MARK.	The end mark is not "\END" (packing) or "\END" (unpacking).*

## Segment option data error

		Error M	1essage	Explanation				
1.	SEGMENT DATA	ERROR	: START MARK.	The start mark is not "\SEGMENT". (during unpacking) *				
2.	SEGMENT DATA	ERROR	: DATA.	The segment data is not correct.				
3.	SEGMENT DATA	ERROR	: SEGMENT NUMBER.	The SEG No. is not correct.				
4.	SEGMENT DATA	ERROR	: SPEC.	The output specification of the SEG terminal is not correct.				
5.	SEGMENT DATA	ERROR	: END MARK.	The end mark is not "\END" (packing) or "\END" (unpacking).*				

#### File error

	Error Message	Explanation				
1.	<pre><file_name> FILE IS NOT FOUND.</file_name></pre>	The file is not found or the file number set in CONFIG.SYS				
		is less than 10.				
2.	PACK FILE NAME (File_name) ERROR.	The packed input format for the file name is wrong.				
3.	PACKED FILE NAME (File_name) ERROR.	The unpacked input format for the file name is wrong.				

## System error

Error Mess	age	Explanation					
1. DIRECTORY FULL.		The directory is full.					
2. DISK WRITE ERROR.		Writing on the disk is failed.					

<sup>\*\</sup>sometimes appears as \(\forall \), depending on the personal computer being used.

## APPENDIX A. S1C6S3N7 INSTRUCTION SET

0	Mne-						Оре	eratio	on C	ode					Flag		• •
Classification	monic	Operand	В	Α	9	8	7	6	5	4	3	2	1	0	IDZC	Cloc	C Operation
Branch	PSET	p	1	1	1	0	0	1	0	p4	р3	p2 :	p1 j	р0		5	NBP ←p4, NPP ←p3~p0
instructions	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0		5	PCB←NBP, PCP←NPP, PCS←s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0		5	PCB←NBP, PCP←NPP, PCS←s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0		5	PCB←NBP, PCP←NPP, PCS←s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0		5	PCB $\leftarrow$ NBP, PCP $\leftarrow$ NPP, PCS $\leftarrow$ s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0		5	PCB $\leftarrow$ NBP, PCP $\leftarrow$ NPP, PCS $\leftarrow$ s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0		5	$PCB \leftarrow NBP, PCP \leftarrow NPP, PCSH \leftarrow B, PCSL \leftarrow A$
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0		7	$M(SP-1) \leftarrow PCP, M(SP-2) \leftarrow PCSH, M(SP-3) \leftarrow PCSL+1$
																	$SP \leftarrow SP-3$ , $PCP \leftarrow NPP$ , $PCS \leftarrow s7 \sim s0$
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0		7	$M(SP-1) \leftarrow PCP, M(SP-2) \leftarrow PCSH, M(SP-3) \leftarrow PCSL+1$
																	$SP \leftarrow SP-3, PCP \leftarrow 0, PCS \leftarrow s7 \sim s0$
	RET		1	1	1	1	1	1	0	1	1	1	1	1		7	$PCSL \leftarrow M(SP), PCSH \leftarrow M(SP+1), PCP \leftarrow M(SP+2)$
																	$SP \leftarrow SP+3$
	RETS		1	1	1	1	1	1	0	1	1	1	1	0		12	$PCSL \leftarrow M(SP), PCSH \leftarrow M(SP+1), PCP \leftarrow M(SP+2)$
																	$SP \leftarrow SP+3, PC \leftarrow PC+1$
	RETD	l	0	0	0	1	<i>l</i> 7	<i>l</i> 6	<i>l</i> 5	l 4	<i>l</i> 3	<i>l</i> 2	<i>l</i> 1	l 0		12	$PCSL \leftarrow M(SP), PCSH \leftarrow M(SP+1), PCP \leftarrow M(SP+2)$
																	$SP \leftarrow SP+3$ , $M(X) \leftarrow l3\sim l0$ , $M(X+1) \leftarrow l7\sim l4$ , $X \leftarrow X+2$
System	NOP5		1	1	1	1	1	1	1	1	1	0	1	1		5	No operation (5 clock cycles)
control	NOP7		1	1	1	1	1	1	1	1	1	1	1	1		7	No operation (7 clock cycles)
instructions	HALT		1	1	1	1	1	1	1	1	1	0	0	0		5	Halt (stop clock)
Index	INC	X	1	1	1	0	1	1	1	0	0	0	0	0		5	X←X+1
operation		Y	1	1	1	0	1	1	1	1	0	0	0	0		5	Y ← Y+1
instructions	LD	X, x	1	0	1	1	x7	х6	x5	х4	х3	x2	x1 :	x0		5	$XH \leftarrow x7 \sim x4, XL \leftarrow x3 \sim x0$
		Y, y	1	0	0	0	у7	у6	у5	y4	у3	y2 :	y1 :	y0		5	YH←y7~y4, YL←y3~y0
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0		5	XH←r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0		5	XL←r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0		5	YH←r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0		5	YL←r
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0		5	r←XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0		5	r←XL
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0		5	r←YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0		5	r←YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0	11	7	XH←XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0	11	7	XL←XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	il	i0	11	7	YH←YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0	11	7	YL←YL+i3~i0+C

	Mne-			Operation Code					Flag								
Classification	monic	Operand	В	Α	9	8	7	6	5	4	3	2	1	0	IDZC	Clock	: Operation
Index	СР	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0	11	7	XH-i3~i0
operation		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0	11	7	XL-i3~i0
instructions		YH, i	1	0	1	0	0	1	1	0	i3	i2	il	i0	11	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0	11	7	YL-i3~i0
Data	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	il	i0		5	r ←i3~i0
transfer		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0		5	$r \leftarrow q$
instructions		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0		5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0		5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0		5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0		5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0		5	$M(X) \leftarrow i3 \sim i0, X \leftarrow X+1$
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0		5	$r \leftarrow q, X \leftarrow X+1$
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0		5	$M(Y) \leftarrow i3 \sim i0, Y \leftarrow Y+1$
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0		5	$r \leftarrow q, Y \leftarrow Y+1$
	LBPX	MX, l	1	0	0	1	<i>l</i> 7	<i>l</i> 6	<i>l</i> 5	<i>l</i> 4	13	12	<i>l</i> 1	<i>l</i> 0		5	$M(X) \leftarrow l3 \sim l0, M(X+1) \leftarrow l7 \sim l4, X \leftarrow X+2$
Flag	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	$\uparrow\uparrow\uparrow\uparrow$	7	F←F∀i3~i0
operation	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	$\downarrow\downarrow\downarrow\downarrow\downarrow$	7	F←F^i3~i0
instructions	SCF		1	1	1	1	0	1	0	0	0	0	0	1	1	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0	<b>1</b>	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0	1	7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1	<b>\</b>	7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0	1	7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1	<b>\</b>	7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	1	7	$I \leftarrow 1$ (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	$\downarrow$	7	$I \leftarrow 0$ (Disables Interrupt)
Stack	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1		5	SP←SP+1
operation	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1		5	SP←SP-1
instructions	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0		5	$SP \leftarrow SP-1, M(SP) \leftarrow r$
		XH	1	1	1	1	1	1	0	0	0	1	0	1		5	$SP \leftarrow SP-1, M(SP) \leftarrow XH$
		XL	1	1	1	1	1	1	0	0	0	1	1	0		5	$SP \leftarrow SP-1, M(SP) \leftarrow XL$
		YH	1	1	1	1	1	1	0	0	1	0	0	0		5	$SP \leftarrow SP-1, M(SP) \leftarrow YH$
		YL	1	1	1	1	1	1	0	0	1	0	0	1		5	$SP \leftarrow SP-1, M(SP) \leftarrow YL$
		F	1	1	1	1	1	1	0	0	1	0	1	0		5	$SP \leftarrow SP-1, M(SP) \leftarrow F$
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0		5	$r \leftarrow M(SP), SP \leftarrow SP+1$
		XH	1	1	1	1	1	1	0	1	0	1	0	1		5	$XH \leftarrow M(SP), SP \leftarrow SP+1$
		XL	1	1	1	1	1	1	0	1	0	1	1	0		5	$XL \leftarrow M(SP), SP \leftarrow SP+1$

Mne-							Оре	ratio	n C	ode					Flag		
Classification	sification monic Operand B A 9		8	7	6	5	4	3	2	1	0	IDZC	Clock	Operation			
Stack	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0		5	$YH \leftarrow M(SP), SP \leftarrow SP+1$
operation		YL	1	1	1	1	1	1	0	1	1	0	0	1		5	$YL \leftarrow M(SP), SP \leftarrow SP+1$
instructions		F	1	1	1	1	1	1	0	1	1	0	1	0	$\uparrow\uparrow\uparrow\uparrow$	5	$F \leftarrow M(SP), SP \leftarrow SP+1$
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0		5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0		5	SPL ← r
ı		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0		5	r←SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0		5	r←SPL
Arithmetic	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	<b>*</b> \$ \$	7	r←r+i3~i0
instructions		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	<b>*</b> 1 1	7	r←r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	<b>*</b> \$ \$	7	r←r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	<b>*</b> \$ \$	7	r←r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	<b>*</b> 1 1	7	r←r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	<b>*</b> \$ \$	7	r←r-i3~i0-C
.		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	<b>*</b> \$ \$	7	r←r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0	<b>1</b>	7	r←r\i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0	<b>\$</b>	7	$r \leftarrow r \land q$
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0	<b>\$</b>	7	r←r√i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0	<b>\$</b>	7	$r \leftarrow r \lor q$
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0	<b>\$</b>	7	r←r∀i3~i0
ı		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0	<b>1</b>	7	$r \leftarrow r \forall q$
ı	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0	11	7	r-i3~i0
.		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0	11	7	r-q
ı	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0	<b>1</b>	7	r∧i3~i0
ı		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0	<b>1</b>	7	r∧q
.	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		7	$d3 \leftarrow d2, d2 \leftarrow d1, d1 \leftarrow d0, d0 \leftarrow C, C \leftarrow d3$
ı	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0	<b>1</b> 1	5	$d3 \leftarrow C$ , $d2 \leftarrow d3$ , $d1 \leftarrow d2$ , $d0 \leftarrow d1$ , $C \leftarrow d0$
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		7	$M(n3\sim n0) \leftarrow M(n3\sim n0)+1$
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0	11	7	$M(n3\sim n0) \leftarrow M(n3\sim n0)-1$
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	rl	r0	<b>*</b> \$ \$	7	$M(X) \leftarrow M(X) + r + C, X \leftarrow X + 1$
. [	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	rl	r0	<b>*</b> \$ \$	7	$M(Y) \leftarrow M(Y) + r + C, Y \leftarrow Y + 1$
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	rl	r0	<b>*</b> \$ \$	7	$M(X) \leftarrow M(X)$ -r-C, $X \leftarrow X+1$
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	<b>*</b> \$ \$	7	$M(Y) \leftarrow M(Y)$ -r-C, $Y \leftarrow Y+1$
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1	1	7	r←r

Abbreviations used in the explanations have the following meanings.

Symbols a	ssociated with registers and memory
A	A register
В	B register
X	XHL register
	(low order eight bits of index register IX)
Y	YHL register
	(low order eight bits of index register IY)
XH	XH register
	(high order four bits of XHL register)
XL	XL register
	(low order four bits of XHL register)
YH	YH register
	(high order four bits of YHL register)
YL	YL register
	(low order four bits of YHL register)
SP	Stack pointer SP
SPH	High-order four bits of stack pointer SP
SPL	Low-order four bits of stack pointer SP
MX, M(X)	Data memory whose address is specified
	with index register IX
MY, M(Y)	Data memory whose address is specified
	with index register IY
Mn, M(n)	Data memory address 000H-00FH
	(address specified with immediate data n of
	00H_0FH)

M(SP) Data memory whose address is specified with stack pointer SP

Two-bit register code r, q

r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

mach ic	gisters i	zi una i	1)	
ı	ſ	C	1	Register
r1	r0	q1	q0	specified
0	0	0	0	A
0	1	0	1	В
1	0	1	0	MX
1	1	1	1	MY

#### Symbols associated with program counter

NBP	New bank pointer
NPP	New page pointer
PCB	Program counter bank
PCP	Program counter page
PCS	Program counter step
PCSH	Four high order bits of PCS
<b>PCSL</b>	Four low order bits of PCS

#### Symbols associated with flags

F	Flag register (I, D, Z, C)
C	Carry flag
$\mathbf{Z}$	Zero flag
D	Decimal flag
I	Interrupt flag
$\downarrow$	Flag reset
$\uparrow$	Flag set
<b>‡</b>	Flag set or reset

#### Associated with immediate data

p	Five-bit immediate data or label 00H-1FH
S	Eight-bit immediate data or label 00H-0FFH
l	Eight-bit immediate data 00H–0FFH
i	Four-bit immediate data 00H-0FH

#### Associated with arithmetic and other operations

+	Add
-	Subtract
٨	Logical AND
V	Logical OR
$\forall$	Exclusive-OR

Add-subtract instruction for decimal operation when the D flag is set

## APPENDIX B. S1C6S3N7 RAM MAP

P.R.	305	3RAM	PROGRAM NAME:															
۵	/ <sub>=</sub>	]	0	_	2	3	4	5	9	7	8	6	∢	В	ပ	۵	ш	ш
0	0	NAME MSB																
		<del>-  </del>	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1	1 1 1 1 1 1 1	1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
		LSB		1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1		1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1
	~	NAME	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1		1 1 1		1	1		1 1 1 1	1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			1
						. ! ! ! ! ! ! ! ! !							1 I I I I I I I I I I I I I I I I I I I	1 I I I I I I I I I I I I I I I I I I I				
		LSB	1					1	1		1 1 1 1 1 1 1 1	1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1				1
	2	NAME																
		MSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	 		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1	 	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	 	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1 1 1 1
			1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	1 1		1 1 1 1 1 1 1 1 1			1 1	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1		1 1	
	- 1	LSB																
	က	NAME MSB		1									1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				1 1 1
		a.	1	1 1 1 1 1 1 1 1	-					-	1	1	1	1	1 1 1 1 1 1 1 1 1			1
_	- 1	7 7 7																
	4	MSB					1 1											
			1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1	1	1	1 1 1 1 1 1 1 1 1	1	1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1	1
		LSB	1 1 1 1 1 1	1 1 1 1 1 1 1 1				1 1 1 1 1 1 1	1 1 1 1 1 1		1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1			
	<u>გ</u>	NAME	1 1 1	 	1			1	 	1	1 1 1		1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
		200	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1	1 1 1 1 1 1 1 1	1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
		5			1 1						1 I I I I I I I I I I I I I I I I I I I							
		LSB																
	∠	NAME MSB					1 1											
					-	-		-			1 1 1 1 1 1		1	1				
		LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
	Ш	NAME																
		MSB	. K03		- SWL3	SWH3	TM3				_ Е Е Е	1 1		FIT2	1 1			T2
			¥04		SWL1	1	TM1			1 .	EIK01		EISW1	ELT8	1		SW1	E
!		LSB	K00		SWLO	SWHO	TM0				EIK00		EISW0	EIT32		<u>K</u> 0	ISW0	IT32
	L L	NAME		1		_		-		-	1				1		-	1
		MSB			1	R03	1		- P03		1		HLMOD	CSDC		XBZR	1	
						-			202		-	I MRS	T-170	1		1 - L	1	
_		LSB			1 1	R00			5 8 8	1 1		SWRST	SVDON		00	XFOUTO	1 1	

# APPENDIX C. S1C6S3N7 I/O MEMORY MAP

		Rea	ister						
Address	D3	D2	D1	D0	Name	Init	1	0	Comment
					K03	-	High	Low	Input port data K03
05011	K03	K02	K01	K00	K02	_	High	Low	Input port data K02
0E0H					K01	_	High	Low	Input port data K01
			R		K00	_	High	Low	Input port data K00
	SWL3	SWL2	SWL1	SWL0	SWL3	0			Stopwatch timer data 3 (1/100 sec) MSB
٥٣٥١١	SWLS	SVVLZ	SWLI	SWLU	SWL2	0			Stopwatch timer data 2 (1/100 sec)
0E2H			R		SWL1	0			Stopwatch timer data 1 (1/100 sec)
			N.		SWL0	0			Stopwatch timer data 0 (1/100 sec) LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			Stopwatch timer data 3 (1/10 sec) MSB
	SWIIS	SWIIZ	SWIII	SWIII	SWH2	0			Stopwatch timer data 2 (1/10 sec)
UESH			R		SWH1	0			Stopwatch timer data 1 (1/10 sec)
					SWH0	0			Stopwatch timer data 0 (1/10 sec) LSB
	TM3	TM2	TM1	TM0	TM3	_	High	Low	Clock timer data 2 Hz
0E4H	TIVIO	TIVIZ	11011	TIVIO	TM2	_	High	Low	Clock timer data 4 Hz
			R		TM1	_	High	Low	Clock timer data 8 Hz
					TM0	-	High	Low	Clock timer data 16 Hz
	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
0E8H	211100	Liitoz	Liitoi	Liitoo	EIK02	0	Enable	Mask	Interrupt mask register (K02)
OLOIT		R	/W		EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
	0	0	EISW1	EISW0	0				
0EAH					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch timer 1 Hz)
		₹	R.	W	EISW0	0	Enable	Mask	Interrupt mask register (stopwatch timer 10 Hz)
	_				0				
	0	EIT2	EIT8	EIT32	EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
0EBH			DAV		EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R		R/W		EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
	0	0	0	IK0	0				
0EDH				1110	0				
	R				0				
	κ				IK0	0	Yes	No	Interrupt factor flag (K00–K03)
	0	0	ISW1	ISW0	0				
0EEH	0   0   13441   13440				0				
			R		ISW1	0	Yes	No	Interrupt factor flag (stopwatch timer 1 Hz)
		1	1		ISW0	0	Yes	No	Interrupt factor flag (stopwatch timer 10 Hz)
	0	IT2	IT8	IT32	0		,,	l	
0EFH					IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
			R		IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

Address		Reg	ister						Comment
Address	D3	D2	D1	D0	Name	Init *1	1	0	Comment
			R01	R00	R03	0	High	Low	Output port data R03
0F3H	R03	R02			R02	0	High	Low	Output port data R02
			BUZZER	FOUT	R01	0	High	Low	Output port data R01
UF3H					BUZZER	0	On	Off	Buzzer On/Off control register
		R	/W		R00	0	High	Low	Output port data R00
					FOUT	0	On	Off	Frequency output control register
	P03	P02	P01	P00	P03	-	High	Low	I/O port data P03
OFCLI	P03	P02	PUI	P00	P02	_	High	Low	I/O port data P02
0F6H		В	/W		P01	-	High	Low	I/O port data P01
		K	/VV		P00	-	High	Low	I/O port data P00
	0	TMRST	SWRUN	SWRST	0				
0F9H	U	TIVINGT	SWKUN	SWKST	TMRST	Reset	Reset	-	Clock timer reset
UF9H	R	w	R/W	l w	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	, r	VV	IN/VV	VV	SWRST	Reset	Reset	-	Stopwatch timer reset
	HLMOD	0	SVDDT	SVDON	HLMOD 0	0	Heavy	Normal	Heavy load protection mode register
0FAH			1		SVDDT	0	Low	Normal	Supply voltage detection data
	R/W		R	R/W	SVDON	0	On	Off	Supply voltage detection data Supply voltage detection circuit On/Off
					CSDC	0	Static	Dynamic	LCD drive switch
	CSDC	0	0	0	0	U	Static	Dynamic	LCD drive switch
0FBH					0				
	R/W		R		0				
0FCH	0	0	0	IOC	0				
					0				
	R R/W			0					
		Г			IOC	0	Out	In	I/O port I/O control register
	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
0FDH					0				
	R/W	R	R	W	XFOUT1	0			FOUT frequency control
					XFOUT0	0			FOUT frequency control

## APPENDIX D. TROUBLESHOOTING

Tool	Problem	Remedy measures
ICE	Nothing appears on the screen, or	Check the following and remedy if necessary:
S5U1C62000H	nothing works, after activation.	• Is the RS-232C cable connected correctly?
		• Is the RS-232C driver installed?
		• Is MODE.COM on the disk?
		• Is the execution file correct?
		PC-DOS ICS6S37W.EXE
		• Is the DOS version correct?
		PC-DOS Ver. 2.1 or later
		• Is the DIP switches that set the baud rate of the main ICE
		unit set correctly?
		• Is the fuse of the ICE cut off?
	The ICE fuse cut immediately after	Check the following and remedy if necessary:
	activation.	Are connectors F1 and F5 connected to the evaluation
		board correctly?
		Is the target board power short-circuiting?
	<illegal ice6200="" version=""></illegal>	The wrong version of ICE is being used. Use the latest
	appears on the screen immediately after	version.
	activation.	
	<illegal p="" parameter<="" version=""></illegal>	The wrong version of ICS6S37P.PAR is being used. Use the
	FILE> appears on the screen immedi-	latest version.
	ately after activation.	
	Immediate values A (10) and B (11)	The A and B registers are reserved for the entry of A and B.
	cannot be entered correctly with the A	Write 0A and 0B when entering A (10) and B (11).
	command.	Example: LD A, B Data in the B register is
		loaded into the A register.
		LD B, 0A Immediate value A is loaded
		into the B register.
	<unused area=""> is displayed by the</unused>	This message is output when the address following one in
	SD command.	which data is written is unused. It does not indicates
		problem. Data is correctly set in areas other than the read-
		only area.
	You can not do a real-time run in	Since the CPU stops temporarily when breaking conditions
	break-trace mode.	are met, executing in a real-time is not performed.
	Output from the evaluation board is	Output is possible only in the real-time run mode.
	impossible when data is written to the	
	I/O memory for Buzzer and Fout	
	output with the ICE command.	
SOG6S37	An R error occurs although the address	Check the following and remedy if necessary:
	is correctly set in the segment source	• Does the address symbol use capital letters?
	file.	• Are the output ports set for every two terminals?
		-

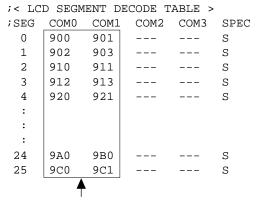
#### **APPENDIX D. TROUBLESHOOTING**

Tool	Problem	Remedy measures
ASM6S37	An R error occurs although the final	The cross assembler is designed to output "R error" every
	page is passed.	time the page is changed. Use a pseudo-instruction to set
		the memory, such as ORG or PAGE, to change the page.
		See "Memory setting pseudo-instructions" in the cross
		assembler manual.
MDC6S37	Activation is impossible.	Check the following and remedy if necessary:
		Is the number of files set at ten or more in OS environ-
		ment file CONFIG.SYS?
Evaluation	The evaluation board does not work	Check the following and remedy if necessary:
board	when it is used independently.	Has the EPROM for F.HEX and S.HEX been replaced
S5U1C62N51E1		by the EPROM for the target?
		• Is the EPROM for F.HEX and S.HEX installed correctly?
		• Is the appropriate voltage being supplied? (5V DC, 3A,
		or more)
		Are the program ROMs (H and L) installed correctly?
		• Is data written from address 4000H? (When the 27C256
		is used as the program ROM)
		• Is the EN/DIS switch on the evaluation board set to EN?
	Target segment does not light.	Check the following and remedy if necessary:
		• Is an EPROM with an access time of 250 ns or less being
		used for S.HEX.
		Has the VADJ VR inside the evaluation board top cover
		been turned to a lower setting?

# APPENDIX E. DEBUGGING FOR 1/2 DUTY DRIVE ON EVALUATION BOARD

The evaluation board (S5U1C62N51E1) is used to debug S1C6S3N7 systems. However, the evaluation board cannot output 1/2 duty signal to drive LCD. When debugging a S1C6S3N7 system that uses a 1/2 duty drive, it should be done with the following procedure.

- 1. Set 1/3 duty function option using the FOG6S37.
- Assign the segments using the SOG6S37.
   Since only the COM0 and COM1 signals are used for 1/2 duty drive, assign the RAM addresses to be used to COM0 and COM1.



RAM addresses that are used for 1/2 duty drive

3. Debug with the evaluation board and check whether the segment assignment is correct or not. Be aware that the LCD drive waveform is different and the LCD corresponding to COM2 goes on.

#### **Creating Mask Data**

- 1. Edit the function option data (option No. 9) using the FOG6S37 to change the 1/3 duty setting to the 1/2 duty setting.
- 2. It is unnecessary to change the segment assignment by the SOG6S37.

Note: The evaluation board does not support the 1/2 bias LCD drive method. The LCD drive waveform is a 1/3 bias waveform.

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**S5U1C6S3N7D** Manual (Development Software Tool for S1C6S3N7)

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■ EPSON Electronic Devices Website

http://www.epson.co.jp/device/