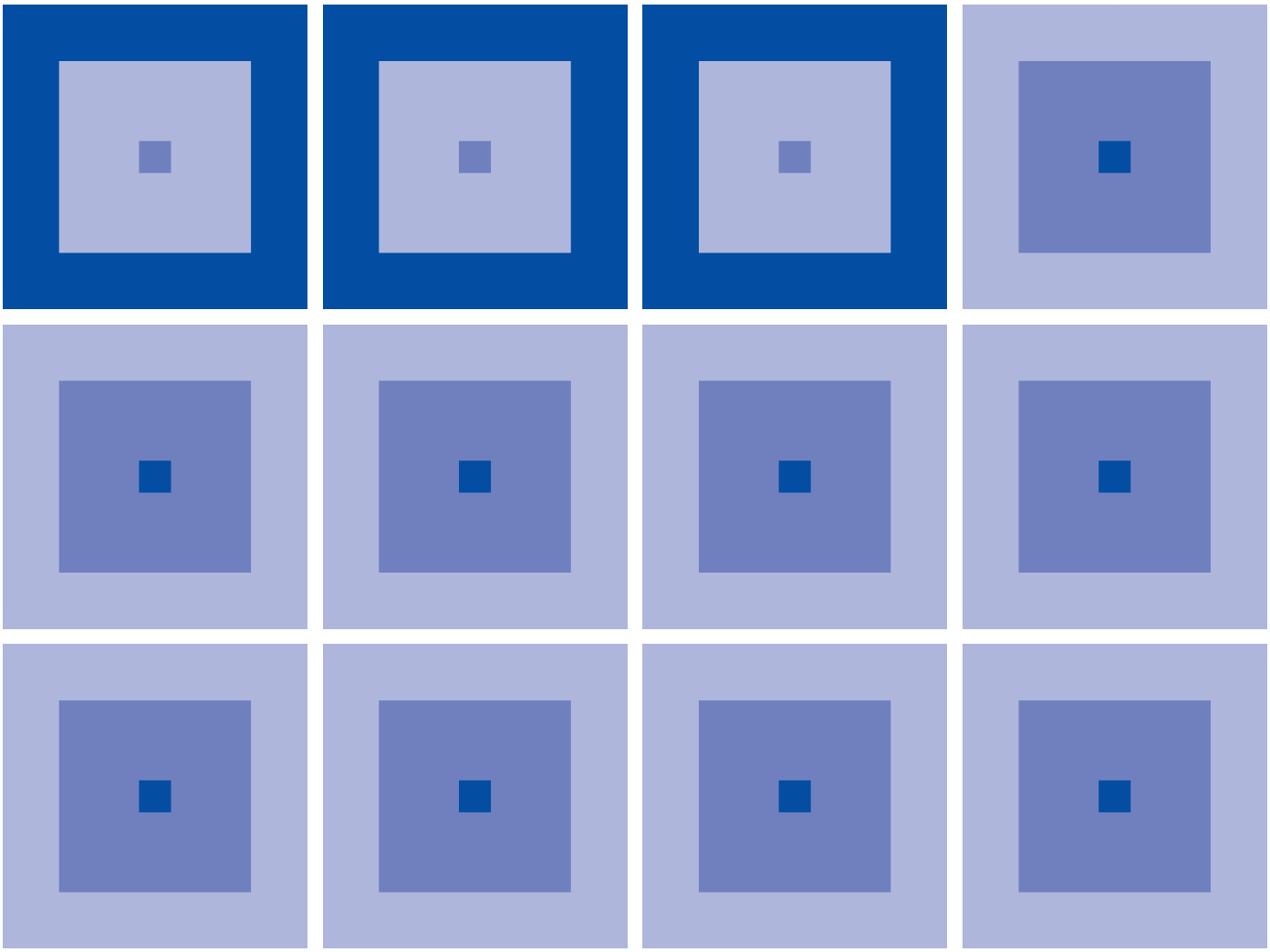
MF1559-02

EPSON

On-The-Go Device Controller LSI

S1R72005

Evaluation Board Manual



SEIKO EPSON CORPORATION

NOTICE

Configuration of product number

●DEVICES

S1 R 72005 F 00A1 00

CONTENTS

1. DESCRIPTION

The EPSON On-The-Go Development Kit is a system that allows you to efficiently develop the On-The-Go hardware and software which use EPSON's On-The-Go device controller LSI S1R72005.

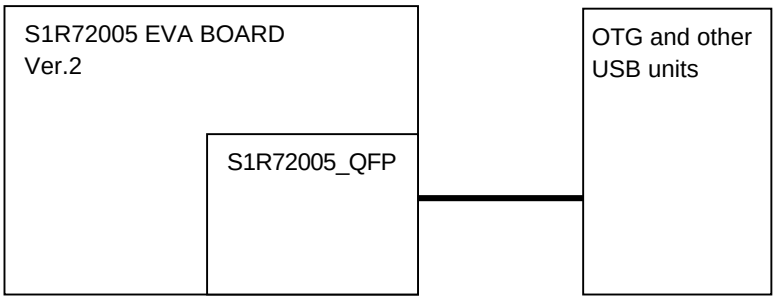
2. FEATURES

The features of the EPSON On-The-Go Development Kit are as follows:

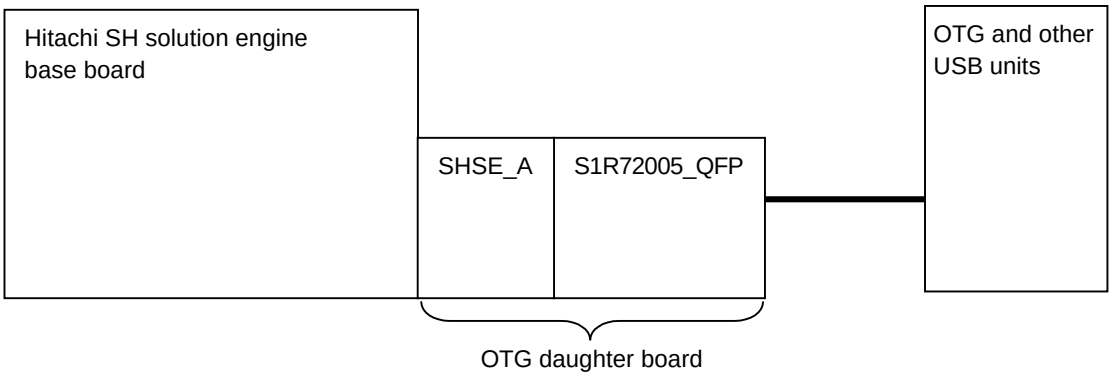
- Operates as an OTG unit through configuration of the S1R72005 EVA BOARD Ver.2 (CPU board) and the S1R72005_QFP (OTG board).
- By combining the SHSE_A or the SHSE_B (SH solution engine connection board) and the S1R72005_QFP (OTG board), it becomes a OTG daughter board supporting Hitachi SH solution engine that enables connection with the SH solution engine.

3. SYSTEM CONFIGURATION

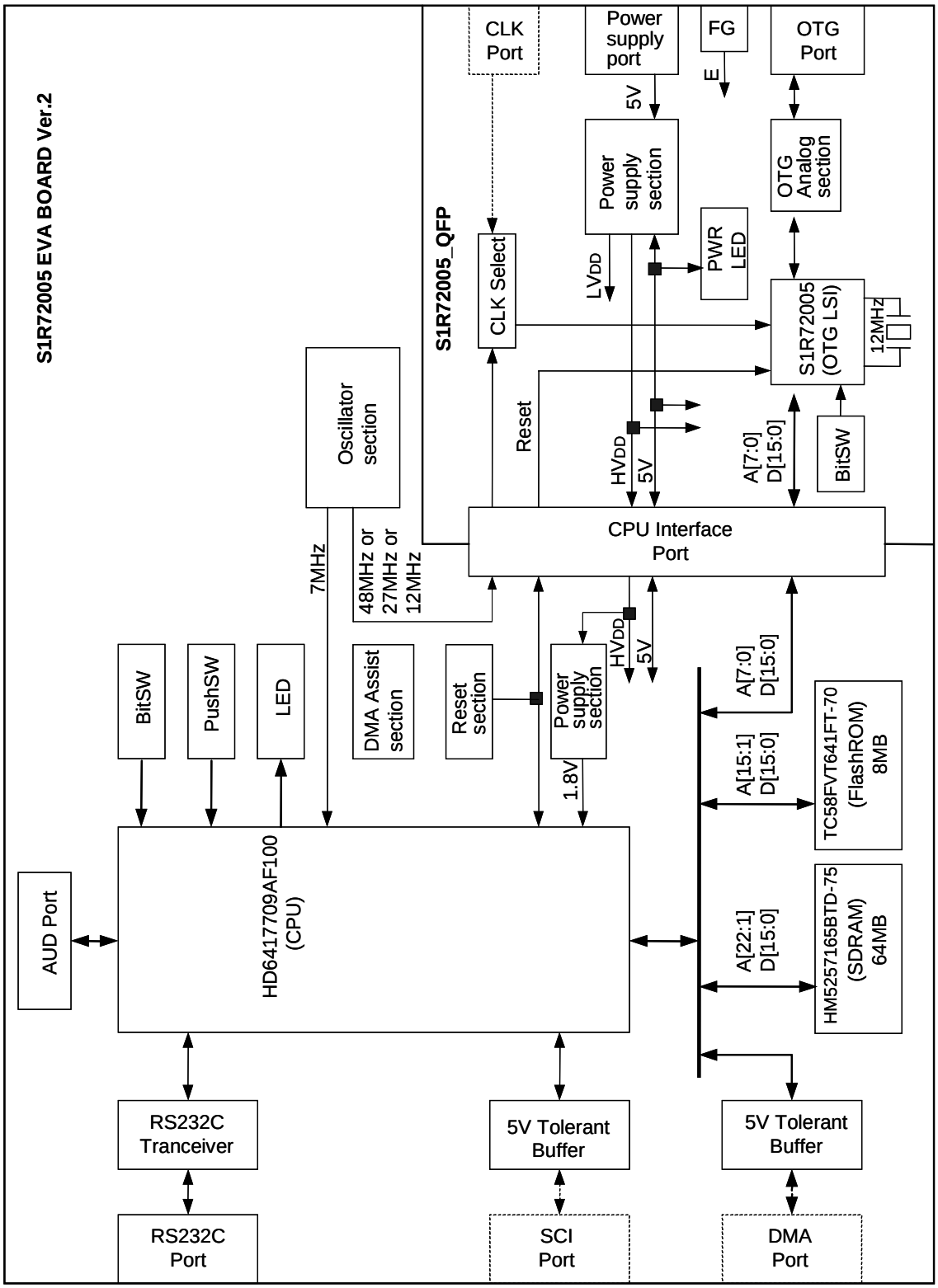
3.1 Configuration 1



3.2 Configuration 2

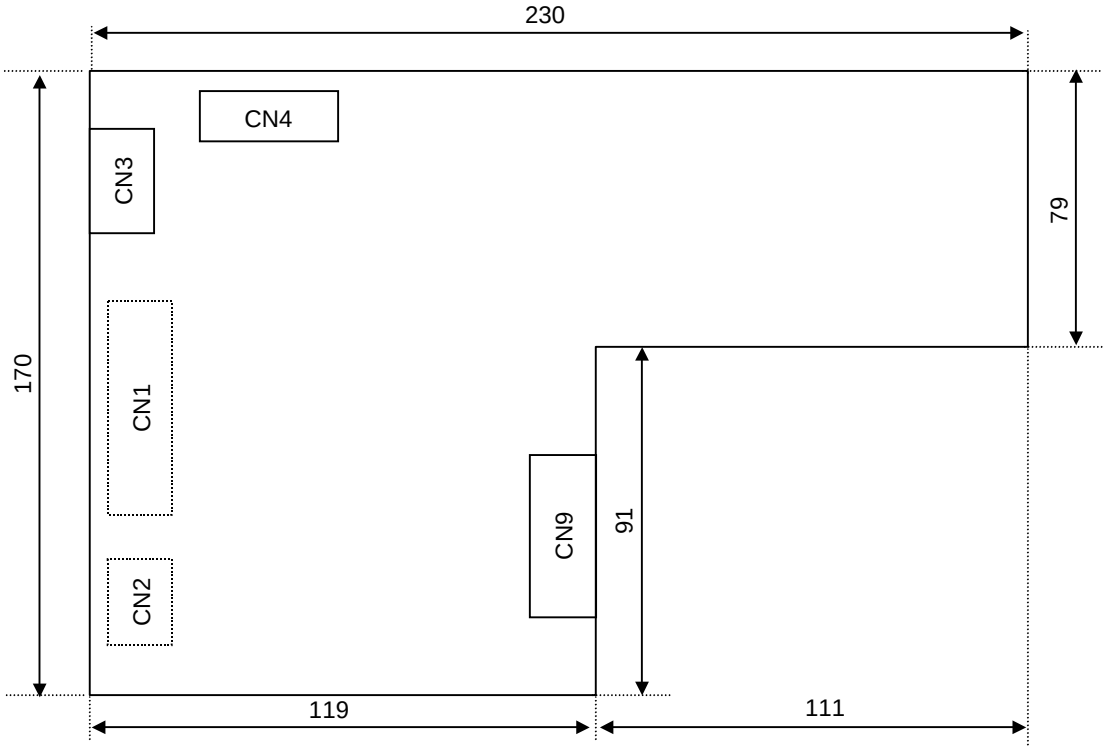


4. BLOCK DIAGRAM

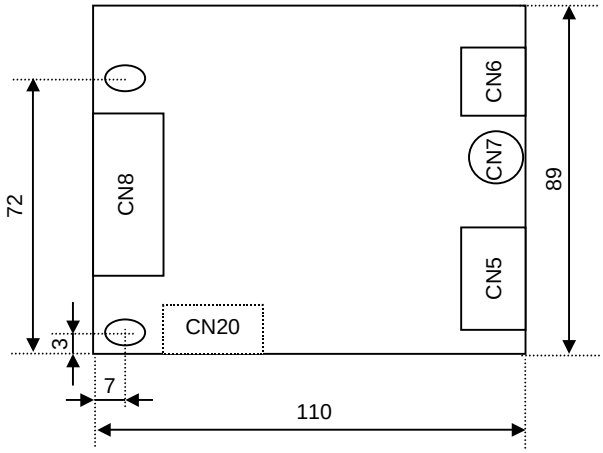


5. APPEARANCE

5.1 S1R72005 EVA BOARD Ver.2



5.2 S1R72005_QFP



6. CONNECTION METHOD

Connect CN9 of the S1R72005 EVA BOARD Ver.2 and CN8 of the S1R72005_QFP.

7. BOARD SPECIFICATION

7.1 Power supply

Power supply voltage : +5.0±0.25V
Consumption current : 360mA (Typ.) for configuration 1
50mA (Typ.) for S1R72005_QFP

7.2 Mode Setting, Switch and Display Description

In the remarks column, ① represents implementation to the S1R72005 EVA BOARD Ver.2 (CPU board) and ② represents implementation to the S1R72005_QFP (OTG board).

●Jumper pins

Pin	Setting	Description	Remarks
J1	Unoperated	LV_{DD}: 2.5V (J1's 1 and 2 are connected with pattern by default)	② Unused by default (not implemented)
	1-2 connection	LV_{DD}: 2.5V (pattern cut is necessary between J1's 3 and 4)	
	3-4 connection	HV_{DD}: 2.8V (pattern cut is necessary between J1's 1 and 2)	
J2	Unoperated	HV_{DD}: 3.3V (J2's 1 and 2 are connected with pattern by default) LV_{DD}: J1's preset value (3 and 4 are connected with pattern by default)	② Unused by default (not implemented)
	1-2 connection 3-4 connection	HV_{DD}: 3.3V (pattern cut is necessary between J2's 1 and 2) HV_{DD}: J1's preset value (pattern cut is necessary between J2's 3 and 4)	
	2-3 connection	HV_{DD}, LV_{DD}: J1's preset value (pattern cut is necessary between J2's 1 and 2)	
J3	Unoperated	CPU clock: 7.000MHz (J3's 1 and 2 are connected with pattern by default) OTG clock: J5's preset value (J3's 3 and 4 are connected with pattern by default)	① Unused by default (not implemented)
	1-2 connection 3-4 connection	CPU clock: 7.000MHz (pattern cut is necessary between J3's 1 and 2) OTG clock: J5's preset value (pattern cut is necessary between J3's 3 and 4)	
	2-3 connection	CPU clock, OTG clock: J5's preset value (pattern cut is necessary between J5's 1 and 2)	
J4	OPEN	Normal	① OPEN by default (not implemented)
	SHORT	Release bus	
J5	Unoperated	CLKIN: 48MHz (J5's 1 and 2 are connected with pattern by default)	① Unused by default (not implemented)
	1-2 connection	CLKIN: 48MHz (pattern cut is necessary between J5's 1 and 2)	
	3-4 connection	CLKIN: 27MHz (pattern cut is necessary between J5's 1 and 2)	
	5-6 connection	CLKIN: 12MHz (pattern cut is necessary between J5's 1 and 2)	
J6	OPEN	Normal	② OPEN by default (not implemented)
	SHORT	Connects to UV_{DD}3.3V Cannot be used with J7.	
J7	OPEN	Normal	② OPEN by default (not implemented)
	SHORT	Connects to DGND Cannot be used with J6.	
J8	Unoperated	Connects to V_{BUS}5V	① OPEN by default (not implemented)
	1-2 connection 3-4 connection	Connects to V_{BUS}5V (pattern cut is necessary between J3's 1 and 2, and 3 and 4), used when measures against static electricity is performed	

Pin	Setting	Description	Remarks
J9	OPEN	Normal	② OPEN by default (not implemented)
	SHORT	Connects to UV_{DD}3.3V	
J10	OPEN	Normal	② OPEN by default (not implemented)
	SHORT	Connects to V_{BUS} (pattern cut is necessary between J10's 1 and 2)	
J11	OPEN	Normal	② OPEN by default (not implemented)
	SHORT	Connects to DGND	

●Switch

Pin	Setting	Description			Remarks
S1	Push button	Hard reset			① Reset when pressed
S2, S3	DipSW ON = "1", OFF = "0"	Switch no.	CPU port	Setting	① OFF by default
		S2-1	PTC[7]	Set the applicable bit for register address H'04000124. Input mode For general use ※1	
		S2-2	PTC[6]		
		S2-3	PTC[5]		
		S2-4	PTC[4]		
		S2-5	PTC[3]		
		S2-6	PTC[2]		
		S2-7	PTC[1]		
		S2-8	PTC[0]		
		S3-1	PTD[3]	Set the applicable bit for register address H'04000126. Input mode For general use ※1	
		S3-2	PTD[2]		
		S3-3	PTD[1]		
		S3-4	PTD[0]		
		S3-5	PTF[3]	Set the applicable bit for register address H'0400012A. Input mode For general use ※1	
		S3-6	PTF[2]		
		S3-7	PTF[1]		
		S3-8	PTF[0]		
S4 to S11	Push button "1" Normal "0" When pressed	Switch no.	CPU port	Setting	①
		S4	PTL[7]	Set the applicable bit for register address H'04000134. Input mode For general use ※1	
		S5	PTL[6]		
		S6	PTL[5]		
		S7	PTL[4]		
		S8	PTL[3]		
		S9	PTL[2]		
		S10	PTL[1]		
		S11	PTL[0]		

Pin	Setting	Description		Remarks
S20	DipSW ON = “1”, OFF = “0”	S20-1	TSTEN: Test pin	② OFF by default S20-1 to 4: OFF unless testing S20-5, 6: Set according to CLK you are using S20-7,8:OFF S21-1:OFF S21-2:ON S21-3:OFF
		S20-2	TIN2: Test pin	
		S20-3	TIN1: Test pin	
		S20-4	TIN0: Test pin	
		S20-5 S20-6	S20-5 = CLKSEL1, S20-6 = CLKSEL0	
			CLKSEL[1:0]: “00” Uses crystal oscillator 12MHz	
			CLKSEL[1:0]: “01” Uses external input 27MHz	
			CLKSEL[1:0]: “10” Uses external input 48MHz	
			CLKSEL[1:0]: “11” Uses external input 12MHz	
		S20-7, 8	Reserved	
S21	DipSW ON = “1”, OFF = “0”	S21-1	MD[5]: “1” Little endian setting	
			MD[5]: “0” Big endian setting	
		S21-2 S21-3	S21-2 = MD[4], S21-3 = MD[3]	
			MD[4:3]: “00” CPU’s reserved bit. Not set for this board.	
			MD[4:3]: “01” Set the CPU’s bus width to 8bit.	
			MD[4:3]: “10” Set the CPU’s bus width to 16bit.	① Default S21-4:OFF S21-5:OFF S21-6:ON S21-7:OFF S21-8:ON
			MD[4:3]: “11” Set the CPU’s bus width to 32bit.	
		S21-4 S21-5 S21-6	S21-4 = MD[2], S21-5 = MD[1], S21-6 = MD[0] MD[2:0]: CPU’s clock operation mode setting. See the “SH7709A Hardware Manual”, page 9-8 for details.	
		S21-7	Reserved	
		S21-8	ASEMD[0]: “1” Normal	
			ASEMD[0]: “0” ASE mode (user debug mode)	
S22 ※2	Toggle	1-2	Connect the mother board’s CLKIN pin to OTG’s CLKIN pin.	② Default 1-2
		2-3	Connect the daughter board’s CLKIN pin to OTG’s CLKGEN pin.	
S23 ※2	DipSW ON = “1”, OFF = “0”	S23-1 S23-2 S23-3 S23-4	Set the clock frequency output to J5’s 5-6. S23-1 = “0” normal, “1” 24MHz output (Note: fixed to “0”) S23-2 = “0” normal, “1” 12MHz output S23-3 = “0” normal, “1” 6MHz output (Note: fixed to “0”) S23-4 = “0” normal, “1” 3MHz output (Note: fixed to “0”) *Do not set more than one “1” at the same time for S23-1 to 4.	① OFF by default S23-1,3,4, 6 to 8: Fixed to OFF S23-2,5: ON when 12MHz is used
		S23-5	Count setting for IC21 (HC163).“0” stop, “1” operate	
		S23-6 to 8	Reserved	

※1: Do not access the applicable area before configuring the CPU’s initial setting.
※2: Not implemented

●Display (LED)

Pin	Setting	Description			Remarks
LED17	Goes off during power OFF Comes on during power ON	+5V power supply monitor.			②
LED1 to LED16	ON="0", OFF="1"	LED no.	CPU port	Setting	①
		LED16	PTL[7]	Set the applicable bit for register address H'04000120. Input mode For general use ※1	
		LED15	PTA [6]		
		LED14	PTA [5]		
		LED13	PTA [4]		
		LED12	PTA [3]		
		LED11	PTA [2]		
		LED10	PTA [1]		
		LED9	PTA [0]		
		LED8	PTB[7]	Set the applicable bit for register address H'04000122. Input mode For general use ※1	
		LED7	PTB [6]		
		LED6	PTB [5]		
		LED5	PTB [4]		
		LED4	PTB [3]		
		LED3	PTB [2]		
		LED2	PTB [1]		
		LED1	PTB [0]		

※1: Do not access the applicable area before configuring the CPU's initial setting.

●Setting

Device	Description	Remarks
Flash ROM	Allocated to area 0 (the address: H'00000000 to H'007FFFFF). Set wait control register WCR2[2:0] to "001". ※1	①
SDRAM	Allocated to area 3 (addresses: H'0C000000 to H'0FFFFFFF). Does not support EDO. Set the bus control register BCR1[4:2] to "010". Set the individual memory control register MCR[5:3] to "100". Set the wait control register WCR2[6:5] to "00". ※1	①
OTG LSI	Allocated to area 5. Addresses H'14000000 to H'17FFFFFF ※1	②
DMA port (Reserved)	DMA transfer interface Allocated to area 6. Addresses H'18000000 to H'1BFFFFFF	① (Not used)
RS232C port	Serial interface. 9-pin. Clock is not connected, so use the start-stop synchronization mode. TxD2, RxD2, RTS2, CTS2 ※1	①
SCI port (Reserved)	Serial interface. Connect the SCK0 pin to the serial clock output pin. TxD0, RxD0, SCK0	① (Not used)
AUD port	User debug interface.	①

※1: Do not access the applicable area before configuring the CPU's initial setting.

8. LIST OF CONNECTORS

In the remarks column, ① represents implementation to the S1R72005 EVA BOARD Ver.2 (CPU board) and ② represents implementation to the S1R72005_QFP (OTG board).

Symbol	Function	Type	Manufacturer	Remarks
CN1	DMA Port (Reserved)	HIF3FC-40PA-2.54DSA	Hirose Electric	① (not implemented)
CN2	SCI Port (Reserved)	HIF3FC-10PA-2.54DSA	Hirose Electric	① (not implemented)
CN3	RS232C Port	17LE-23090-27(D3BB)	DDK	① Pin
CN4	AUD Port	DX20M-36S	Hirose Electric	① Socket
CN5	Power supply port	53109-0410	Molex	②
CN6	OTG Port	MNE20	ACON	②
CN7	FG	—	—	②
CN8	CPU Interface Port (S1R72005_QFP Side)	DHB-PA60-R131N	DDK	② Pin
CN9	CPU Interface Port (S1R72005 EVA BOARD Ver.2 Side)	DHB-RA60-R131N	DDK	① Socket
CN20	CLK Port (Reserved)	SMA-300-126S	Japan Aviation Electronics Industry	② (not implemented)

8.1 CN1 DMA Port

No use

8.2 CN2 SCI Port

No use

8.3 CN3 RS232C Port

This is used for connecting to the PC's RS232C port.
Use the Dsub9-pin socket-socket cross cable to connect to the PC.

Pin no.	I/O	Signal name	Pin no.	I/O	Signal name
1	I	DCD	6	I	DSR
2	I	RxD	7	O	RTS
3	O	TxD	8	I	CTS
4	O	DTR	9	I	RI
5	Power supply	GND	—	—	—

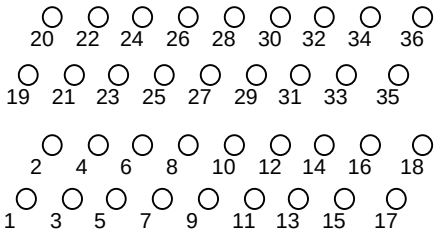
8.4 CN4 AUD Port

This is a port for user debugging.
Use an AUD cable specified by the debugger manufacturer for connecting to the debugger.
The performance of Computex's H020-SH7709 has been tested for our product, but as for connection with other debuggers, check the following pin layout and the respective debugger's instruction manual carefully before using it.
Please note that following pin layout uses the pin array (Note 3) specified by the connector manufacturer as the reference and may differ from the pin layout in the instruction manual provided by the debugger manufacturer.

Pin no.	I/O	Signal name	Pin no.	I/O	Signal name
1	—	NC	19	Power supply	GND
2	I/O	AUDATA0	20	Power supply	GND
3	I/O	AUDATA1	21	Power supply	GND
4	O	AUDATA2	22	Power supply	GND
5	O	AUDATA3	23	Power supply	GND
6	O	xAUDSYNC	24	Power supply	GND
7	—	NC	25	Power supply	GND
8	—	NC	26	Power supply	GND
9	I	TCK	27	Power supply	GND
10	I	TMS	28	Power supply	GND
11	I	xTRST	29	Power supply	GND
12	I	TDO (Note 1)	30	Power supply	GND
13	O	TDI (Note 2)	31	Power supply	GND
14	O	XASEBRK/BRKACK	32	Power supply	GND
15	—	NC	33	Power supply	GND
16	O	xRESET	34	Power supply	GND
17	Power supply	GND	35	Power supply	GND
18	I	AUDCK	36	Power supply	GND

(Note 1) It is connected to the CPU's TDI pin.
(Note 2) It is connected to the CPU's TDO pin.

(Note 3) The pin array provided by the connector manufacturer.



8.5 CN5 Power Supply Port

This is used for the connection with the external power supply.

Pin no.	I/O	Signal name	Pin no.	I/O	Signal name
1	Power supply	+12V (Reserved) (Note)	—	—	—
2	Power supply	Vss	—	—	—
3	Power supply	Vss	—	—	—
4	Power supply	+5V	—	—	—

(Note) The board has been processed with "None Connect" process since +12V is not used, so you may supply or not supply +12V.

8.6 CN6 OTG Port

This is used to connect to the OTG unit or the USB unit.

Pin no.	I/O	Signal name	Pin no.	I/O	Signal name
1	Power supply	V_{BUS}	—	—	—
2	I/O	DM	—	—	—
3	I/O	DP	—	—	—
4	I	ID	—	—	—
5	Power supply	GND	—	—	—

8.7 CN7 FG

This is used to connect to the FG. Use a cable with a crimping terminal and screw on to the board.

8.8 CN8 CPU Interface Port (S1R72005_QFP board side)

Pin no.	I/O	Signal name	Pin no.	I/O	Signal name
1	Power supply	DGND	31	Power supply	HV_{DD}
2	I	CKIO	32	Power supply	DGND
3	Power supply	DGND	33	Power supply	HV_{DD}
4	Power supply	HV_{DD}	34	I	CLKIN
5	O	xDREQ	35	Power supply	DGND
6	I	xDACK	36	I	xRESET
7	Power supply	DGND	37	I	xRD
8	I	xCS	38	Power supply	HV_{DD}
9	O	xINT	39	I	xWR
10	Power supply	HV_{DD}	40	O	xWAIT
11	I/O	D15	41	I/O	D14
12	I/O	D13	42	Power supply	DGND
13	I/O	D12	43	I/O	D11
14	I/O	D10	44	I/O	D9
15	Power supply	HV_{DD}	45	I/O	D8
16	I/O	D7	46	I/O	D6
17	I/O	D5	47	Power supply	DGND
18	I/O	D4	48	I/O	D3
19	Power supply	HV_{DD}	49	I/O	D2
20	I/O	D1	50	I/O	D0
21	I	A7	51	Power supply	DGND
22	I	A6	52	I	A5
23	Power supply	HV_{DD}	53	I	A4
24	I	A3	54	I	A2
25	I	A1	55	Power supply	DGND
26	Power supply	HV_{DD}	56	I	A0
27	Power supply	HV_{DD}	57	Power supply	DGND
28	Power supply	5V	58	Power supply	5V
29	Power supply	5V	59	Power supply	5V
30	Power supply	5V	60	Power supply	5V

8.9 CN9 CPU Interface Port (S1R72005 EVA BOARD Ver.2 side)

Pin no.	I/O	Signal name	Pin no.	I/O	Signal name
1	Power supply	DGND	31	Power supply	HV_{DD}
2	O	CKIO	32	Power supply	DGND
3	Power supply	DGND	33	Power supply	HV_{DD}
4	Power supply	HV_{DD}	34	O	CLKIN
5	I	xDREQ	35	Power supply	DGND
6	O	xDACK	36	O	xRESET
7	Power supply	DGND	37	O	xRD
8	O	xCS	38	Power supply	HV_{DD}
9	I	xINT	39	O	xWR
10	Power supply	HV_{DD}	40	I	xWAIT
11	I/O	D15	41	I/O	D14
12	I/O	D13	42	Power supply	DGND
13	I/O	D12	43	I/O	D11
14	I/O	D10	44	I/O	D9
15	Power supply	HV_{DD}	45	I/O	D8
16	I/O	D7	46	I/O	D6
17	I/O	D5	47	Power supply	DGND
18	I/O	D4	48	I/O	D3
19	Power supply	HV_{DD}	49	I/O	D2
20	I/O	D1	50	I/O	D0
21	O	A7	51	Power supply	DGND
22	O	A6	52	O	A5
23	Power supply	HV_{DD}	53	O	A4
24	O	A3	54	O	A2
25	O	A1	55	Power supply	DGND
26	Power supply	HV_{DD}	56	O	A0
27	Power supply	HV_{DD}	57	Power supply	DGND
28	Power supply	5V	58	Power supply	5V
29	Power supply	5V	59	Power supply	5V
30	Power supply	5V	60	Power supply	5V

8.10 CN20 CLK Port

No use

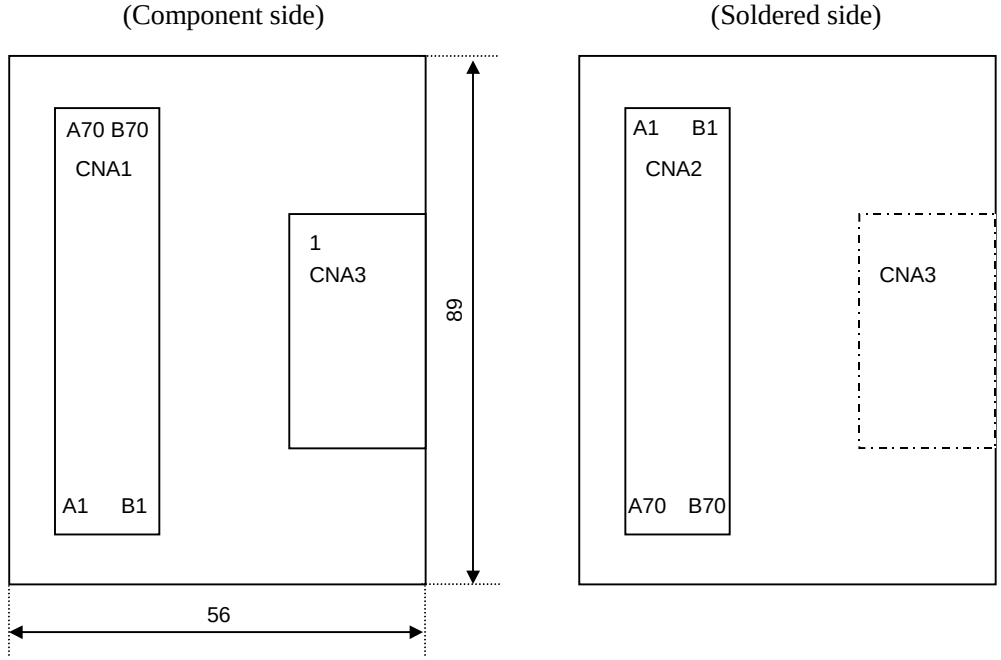
9. OPTIONAL BOARDS

By combining the optional board and the S1R72005_QFP (OTG board), it becomes a OTG daughter board supporting Hitachi SH solution engine that enables connection with the SH solution engine. This connection allows OTG application development on the Hitachi SH solution engine.

- SHSE_A: solution engine connection board for the SH76XX and the SH77XX.

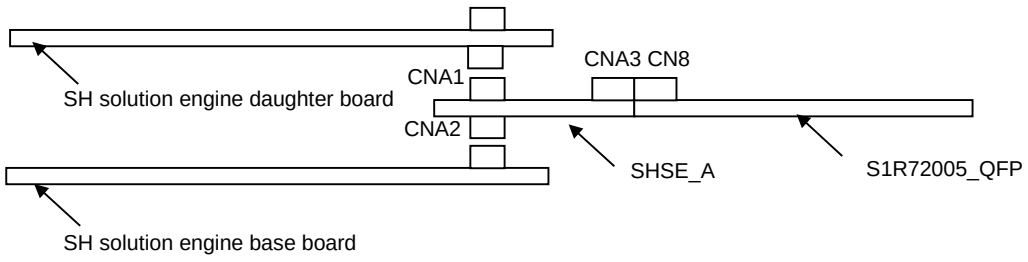
9.1 SHSE_A

9.1.1 Appearance



9.1.2 Connection Method

Connect to the SH solution engine as follows.



9.1.3 List of Connectors

Symbol	Function	Type	Manufacturer	Remarks
CNA1	For connecting the daughter board side (component side)	KX14-140K5D1	Japan Aviation Electronics Industry	—
CNA2	For connecting the base board side (soldered side)	KX15-140K4D1	Japan Aviation Electronics Industry	—
CNA3	For connecting the S1R72005_QFP	DHB-RA60-R131N	DDK	—

9.1.4 Connector Pin Layout and Connector Connections

CNA1, CNA2			CNA3		CNA1, CNA2			CNA3	
No.	Pin name	Connection	No.	Pin name	No.	Pin name	Connection	No.	Pin name
A1	GND	———		DGND	B1	GND	———		DGND
A2	CKIO	———	2	CKIO	B2	GND	———		DGND
A3	GND	———		DGND	B3	GND	———		DGND
A4	D0	———	50	D0	B4	D1	———	20	D1
A5	D2	———	49	D2	B5	D3	———	48	D3
A6	D4	———	18	D4	B6	D5	———	17	D5
A7	D6	———	46	D6	B7	D7	———	16	D7
A8	GND	———		DGND	B8	GND	———		DGND
A9	D8	———	45	D8	B9	D9	———	44	D9
A10	D10	———	14	D10	B10	D11	———	43	D11
A11	D12	———	13	D12	B11	D13	———	12	D13
A12	D14	———	41	D14	B12	D15	———	11	D15
A13	GND	———		DGND	B13	GND	———		DGND
A14	D16		—		B14	D17		—	
A15	D18		—		B15	D19		—	
A16	D20		—		B16	D21		—	
A17	D22		—		B17	D23		—	
A18	GND	———		DGND	B18	GND	———		DGND
A19	D24		—		B19	D25		—	
A20	D26		—		B20	D27		—	
A21	D28		—		B21	D29		—	
A22	D30		—		B22	D31		—	
A23	3.3V		—		B23	3.3V		—	
A24	3.3V		—		B24	3.3V		—	
A25	NC0				B25	3.3V		—	
A26	A0	———	56	A0	B26	A1	———	25	A1
A27	A2	———	54	A2	B27	A3	———	24	A3
A28	A4	———	53	A4	B28	A5	———	52	A5
A29	A6	———	22	A6	B29	A7	———	21	A7
A30	GND	———		DGND	B30	GND	———		DGND
A31	A8		—		B31	A9		—	
A32	A10		—		B32	A11		—	
A33	A12		—		B33	A13		—	
A34	A14		—		B34	A15		—	
A35	GND	———		DGND	B35	GND	———		DGND
A36	A16		—		B36	A17		—	
A37	A18		—		B37	A19		—	
A38	A20		—		B38	A21		—	
A39	A22		—		B39	A23		—	
A40	A24		—		B40	A25		—	
A41	GND	———		DGND	B41	GND	———		DGND
A42	/DACK0	———	6	xDACK	B42	/DACK1		—	
A43	/DREQ0	———	5	xDREQ	B43	/DREQ1		—	
A44	GND	———		DGND	B44	GND	———		DGND
A45	/CS0		—		B45	/CS1		—	
A46	/CS2		—		B46	/CS3		—	
A47	/CS4		—		B47	/CS5	———	8	xCS
A48	/CS6		—		B48	R/W		—	
A49	GND	———		DGND	B49	GND	———		DGND
A50	/RD	———	37	xRD	B50	/BS		—	
A51	GND	———		DGND	B51	GND	———		DGND
A52	/WE0		—		B52	/WE1	———	39	xWR
A53	/WE2		—		B53	/WE3		—	
A54	GND	———		DGND	B54	GND	———		DGND
A55	/WAIT0	———	40	xWAIT	B55	/WAIT1		—	
A56	/WAIT2		—		B56	/WAIT3		—	
A57	GND	———		DGND	B57	GND	———		DGND
A58	/IRQ1		—		B58	/IRQ2	———	9	xINT
A59	/IRQ3		—		B59	/IRQ4		—	
A60	/IRQ5		—		B60	/IRQ6		—	
A61	/IRQ7		—		B61	/IRQ8		—	
A62	+5V	———		5V	B62	+5V	———		5V
A63	+5V	———		5V	B63	+5V	———		5V
A64	NC1		—		B64	+5V	———		5V
A65	/RES	———	36	xRESET	B65	+5V	———		5V
A66	A+5V		—		B66	+5V	———		5V
A67	A+5V		—		B67	NC2		—	
A68	NC3		—		B68	NC4		—	
A69	NC5		—		B69	NC6		—	
A70	NC7		—		B70	NC8		—	
					—			34	CLKIN

10. PRECAUTIONS FOR USE

EPSON On-The-Go Development Kit is a kit developed for performing various evaluations before product development. Note the following upon use.

(1) Install and use the kit indoors at a room temperature.
(2) Avoid installation and use of the kit in a dusty environment.
(3) Make sure that no foreign matter, such as solder dust or bits of wire, adheres to the top or the bottom of the board.
(4) If necessary, mount a spacer (use M3 screw 6mm) to the board so that the board and the lower part of the board do not contact.
(5) When connecting and using the kit with the SH solution engine board, adjust the height of the SH solution engine board and this board, and mount a spacer (use M3 screw 6mm) of an appropriate length to fix the board and the SH solution engine board located on the lower part of this board.
(6) Always connect or disconnect CN5 (power supply connector) with the power supply OFF.
(7) Always turn the power supply OFF when connecting the S1R72005_QFP board and the S1R72005 EVA BOARD Ver.2 board or the optional board, and the optional board and the SH solution engine board.
(8) Always reset after changing switch settings for S20, S21, S22 and S23 (press S1).
(9) For the connection and use of the debugger, see the instruction manual provided by the debugger manufacturer and the CPU's instruction manual.
(10) Do not mount circuits or components as they are into a product. Redesign them before incorporating them into a product, taking timing and operating margin into account.

11. REFERENCE

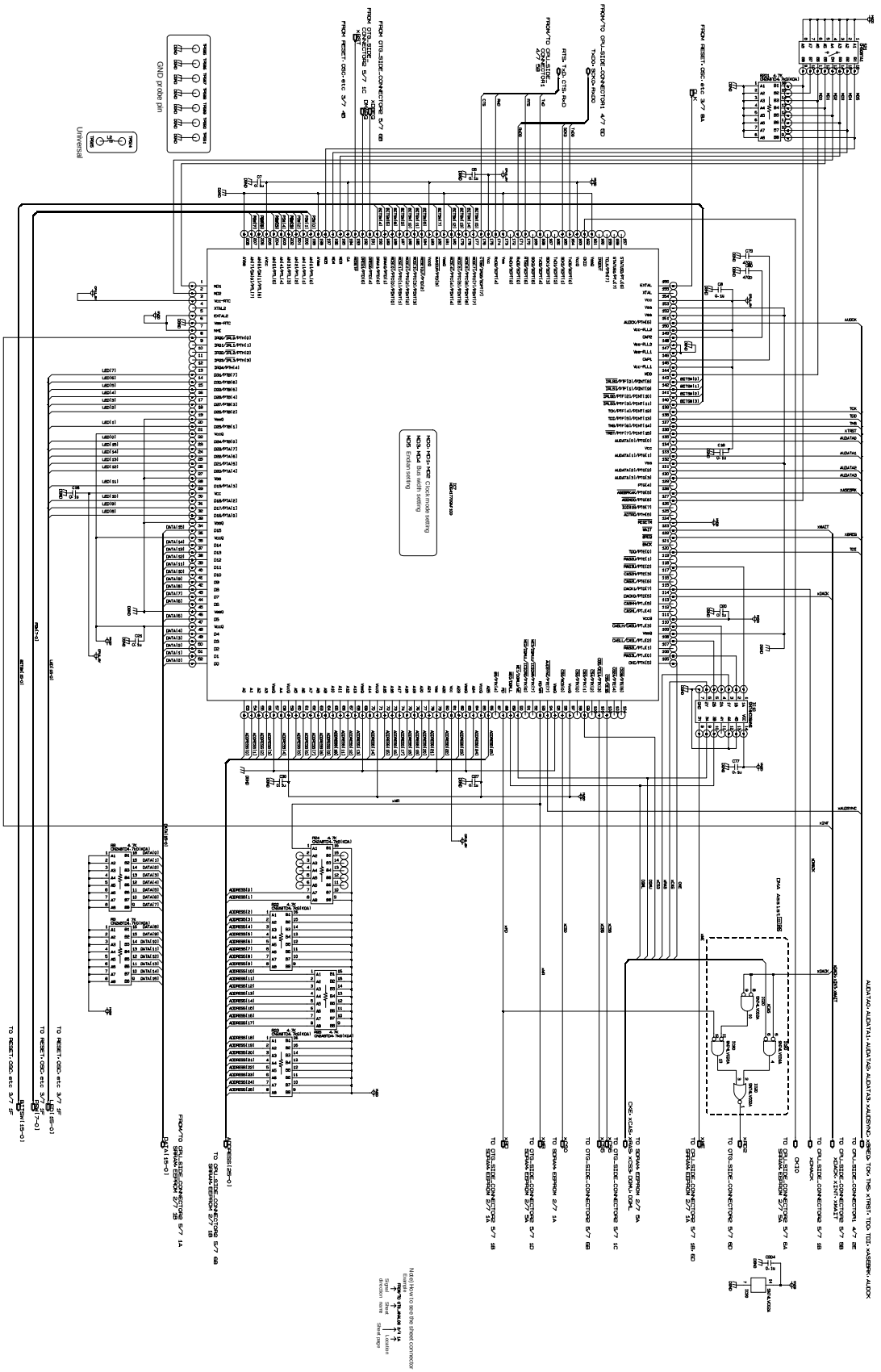
The reference for the S1R72005 EVA BOARD Ver.2 (CPU board), the S1R72005_QFP (OTG board) and the optional board is as follows:

- Circuit diagram (Note 1)
- Table of parts
- Pattern diagram (Note 2)

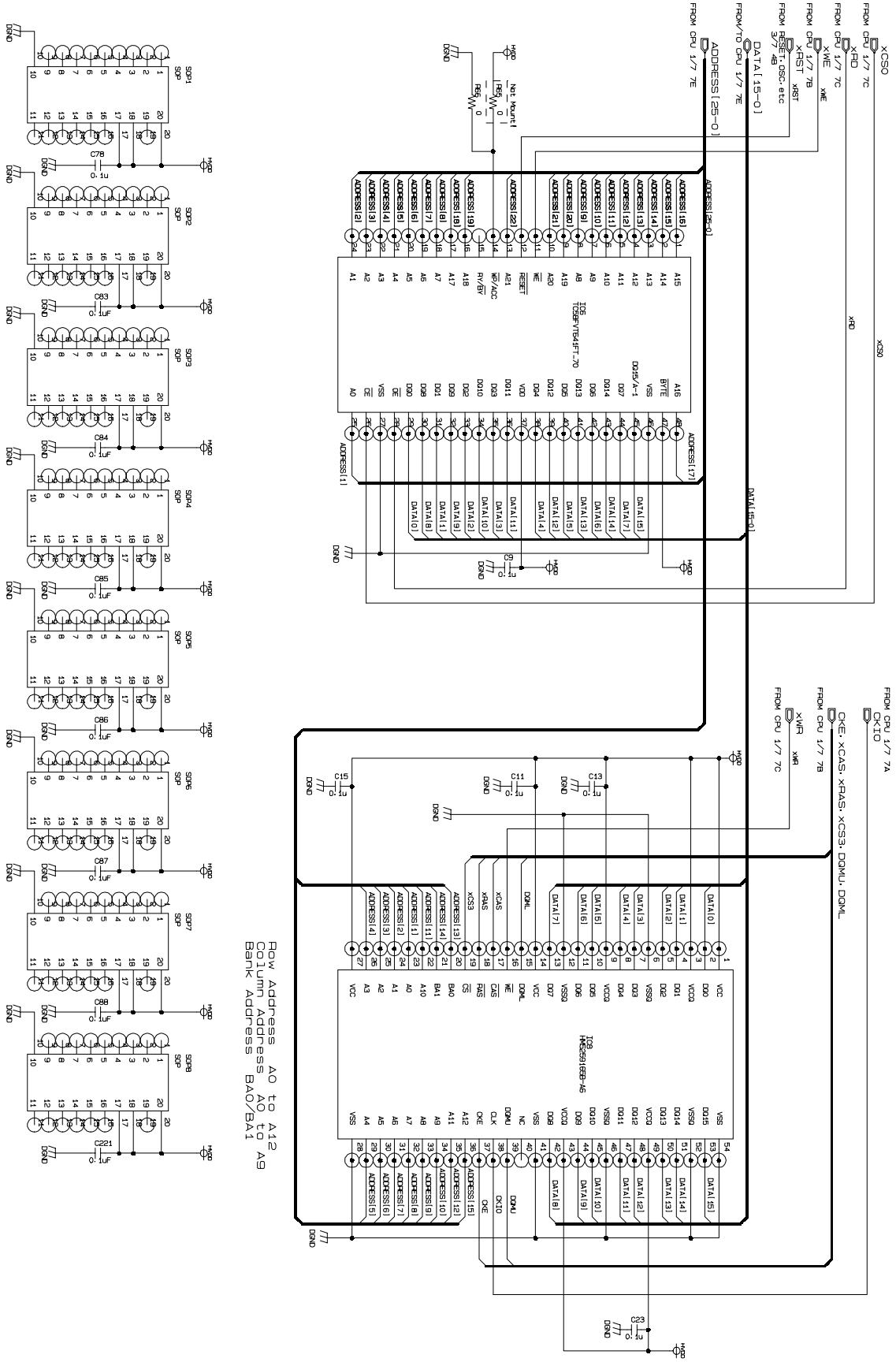
(Note 1) Some of the circuits of this board are redundant for evaluating the LSI function.
See the connection example in the S1R72005 Specifications for information on minimum circuits.
(Note 2) The pattern diagram is sent upon request by our Sales contact.

Circuit Diagram

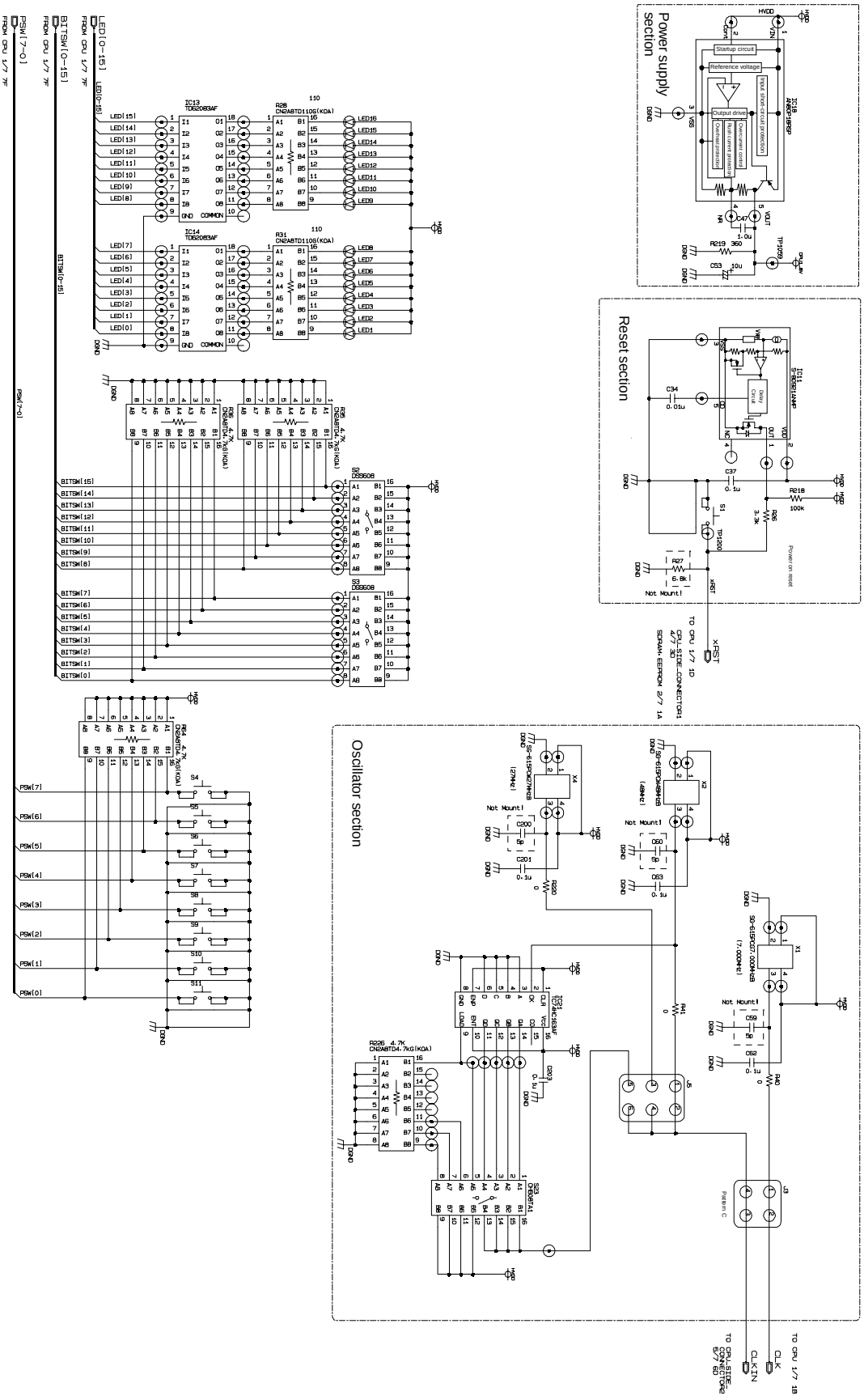
S1R72005 EVA Mother Board Ver.2 (CPU)



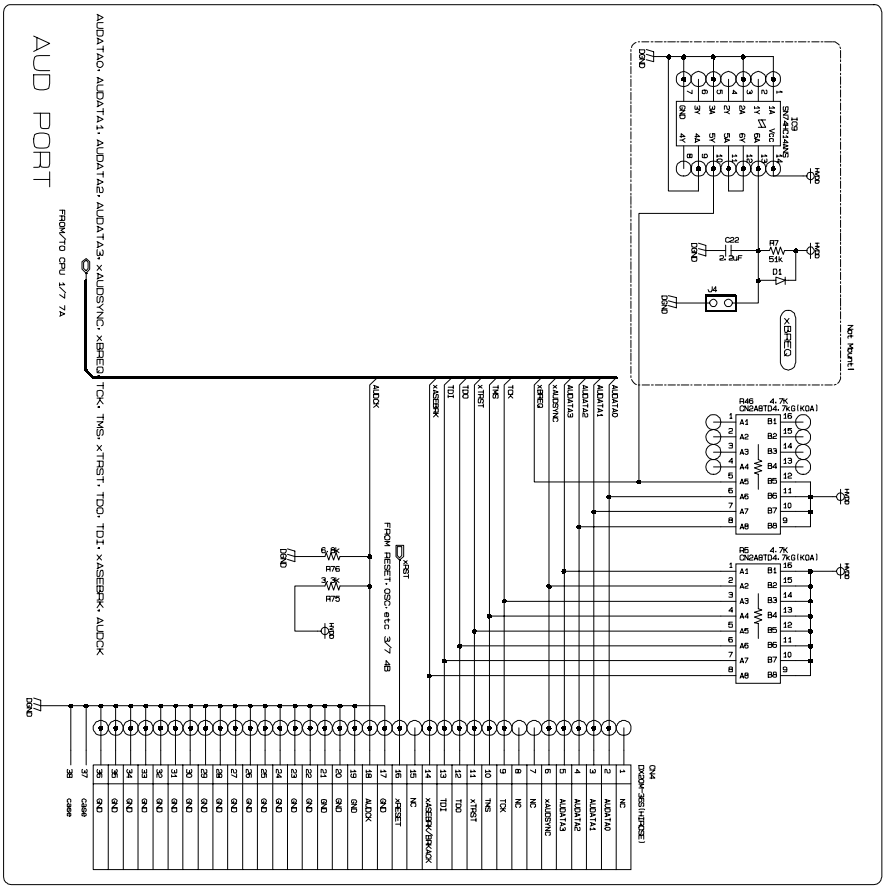
S1R72005 EVA Mother Board Ver.2 (SDRAM, EEPROM)



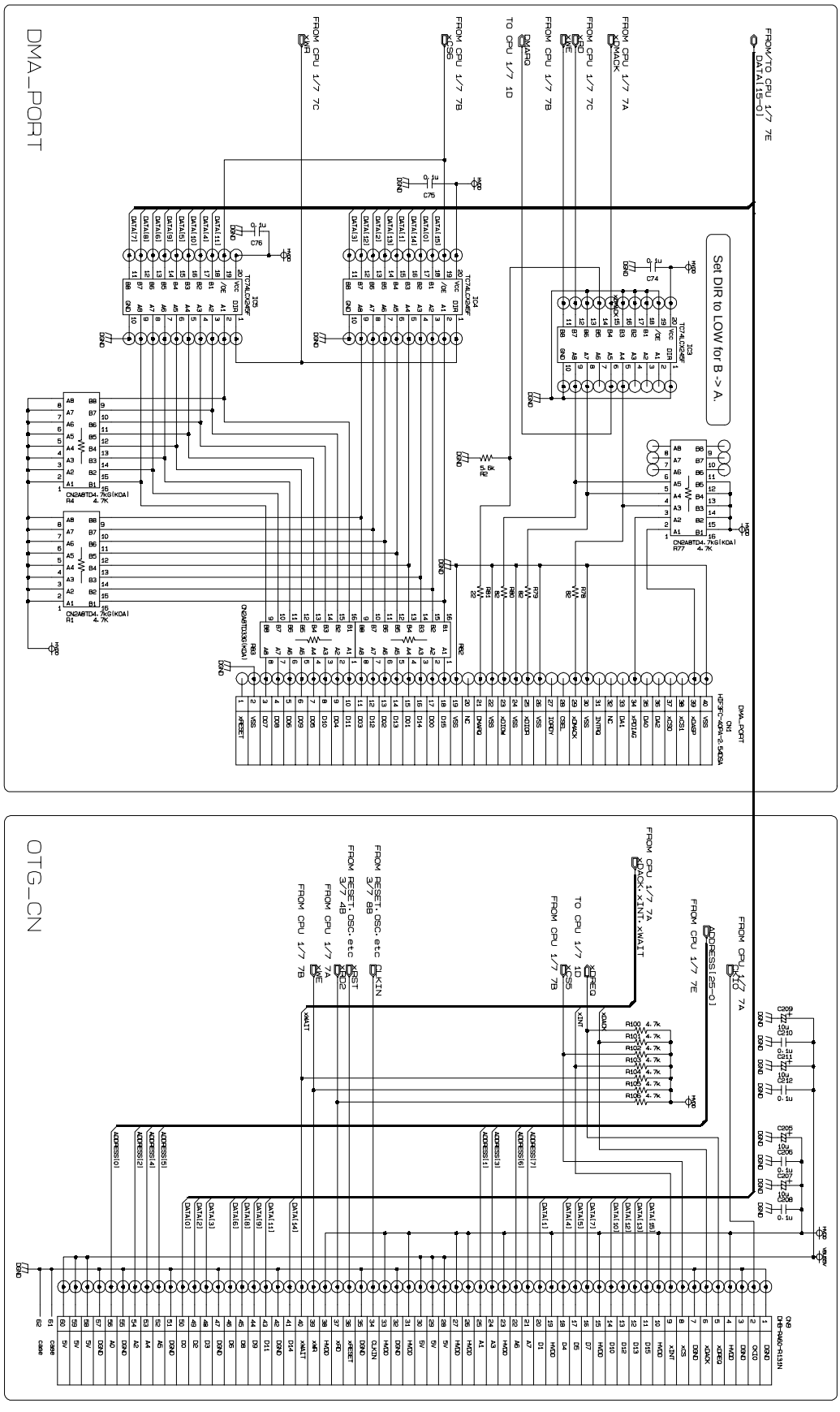
S1R72005 EVA Mother Board Ver.2 (RESET, OSC, ETC)



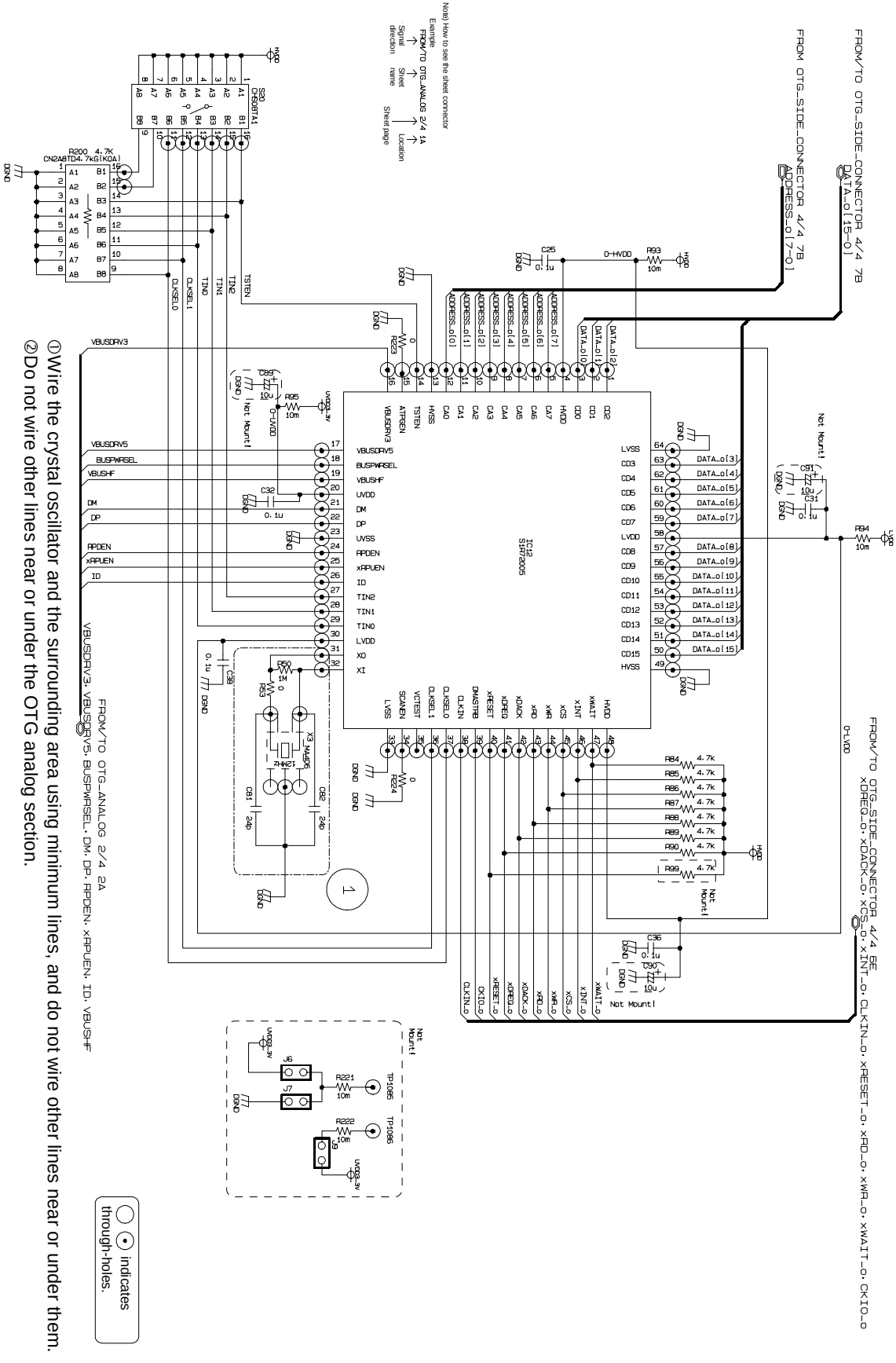
S1R72005 EVA Mother Board Ver.2 (CPU_SIDE_CONNECTOR1)



S1R72005 EVA Mother Board Ver.2 (CPU_SIDE_CONNECTOR2)



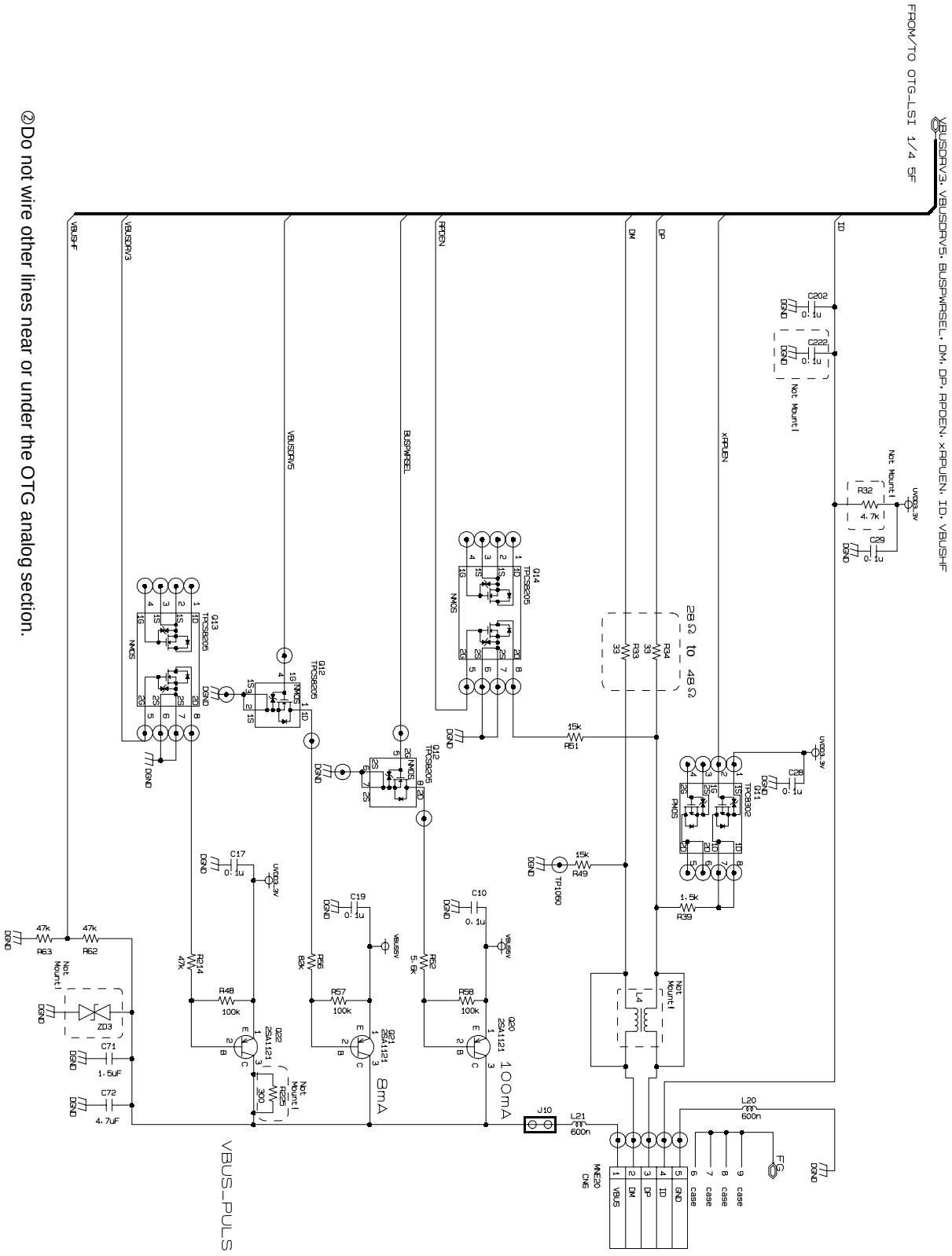
S1R72005_QFP (OTG_LSI)



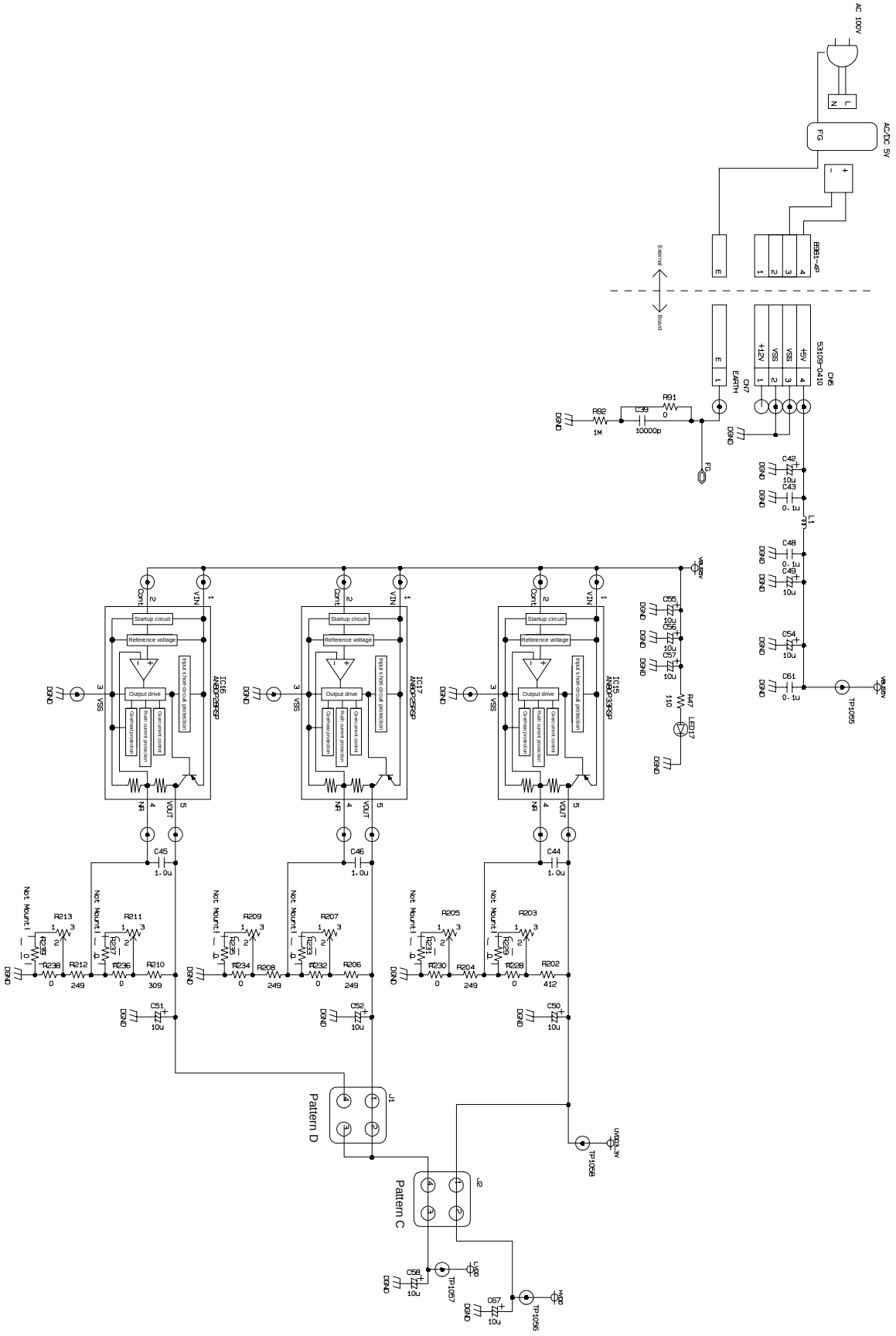
①Wire the crystal oscillator and the surrounding area using minimum lines, and do not wire other lines near or under them.
②Do not wire other lines near or under the OTG analog section.

◯ ⊙ indicates through-holes.

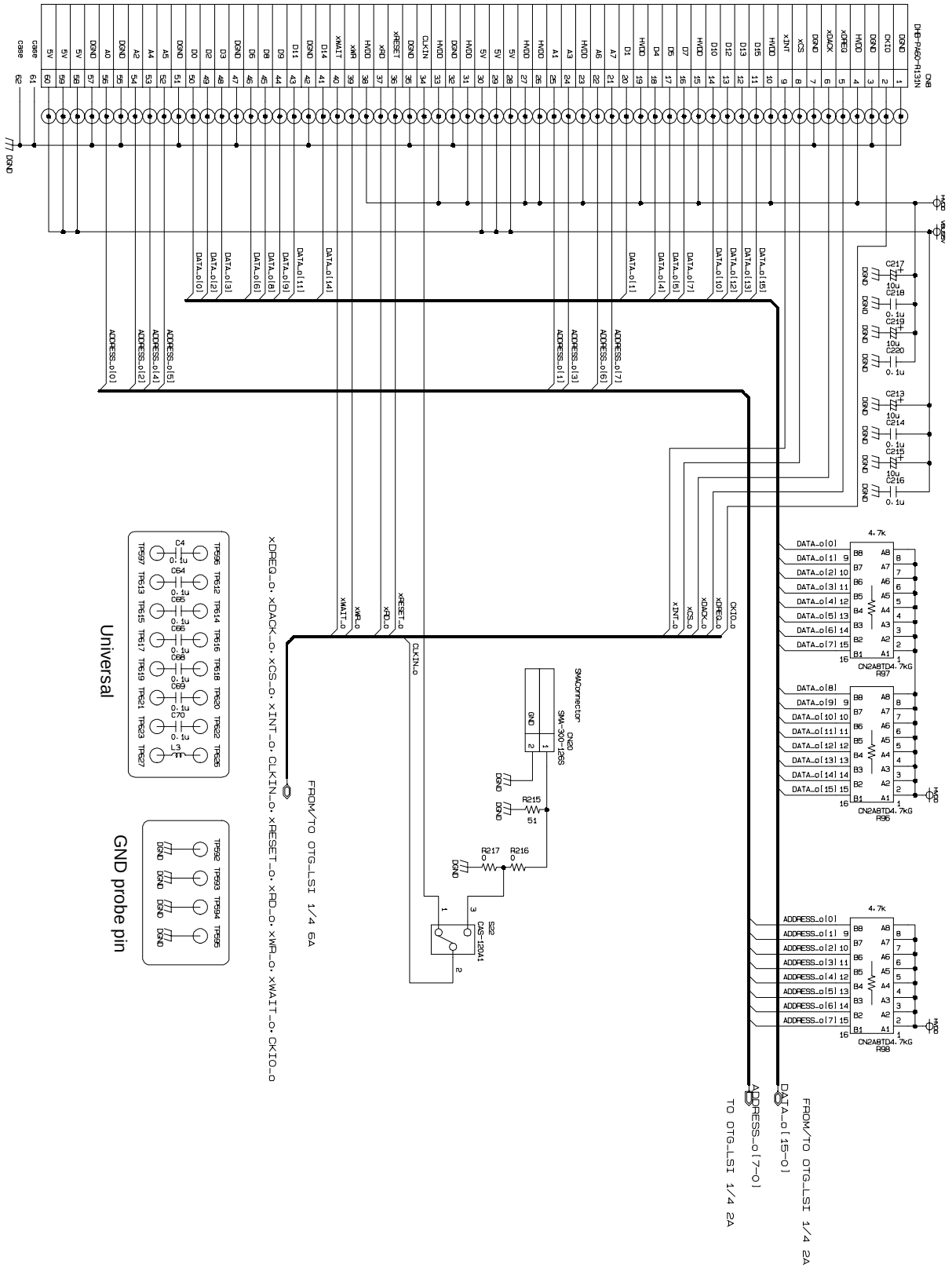
S1R72005_QFP (OTG_ANALOG)



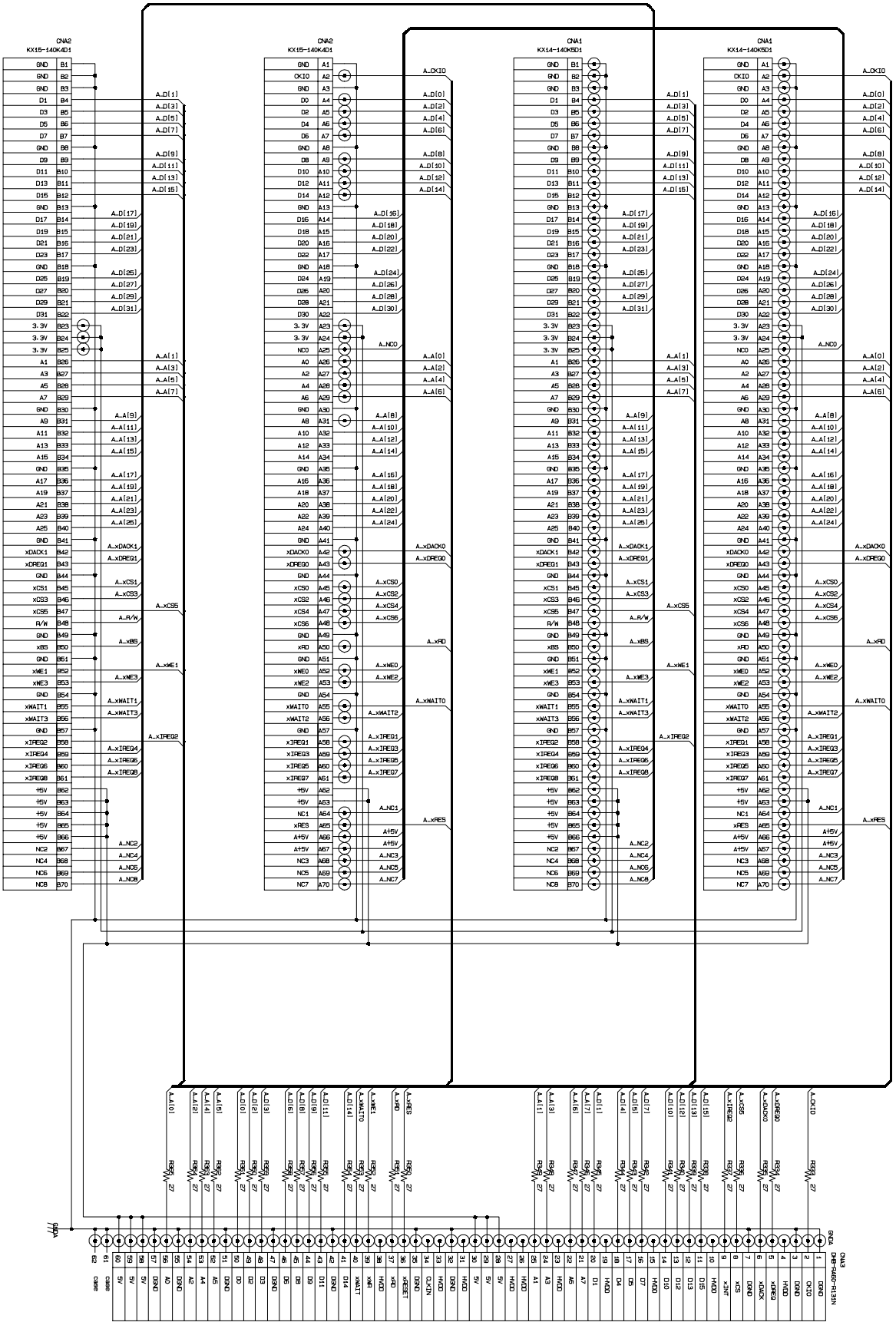
S1R72005_QFP (POWER SUPPLY)



S1R72005_QFP (OTG_SIDE_CONNECTOR)



SHSE_A



S1R72005 EVA BOARD Ver.2 Table of Parts

Section	Symbol	Component	Model number	Specification (constant)	Operating temperature (°C)	Manufacturer	No. of units	Remarks
1	CN3	Connector (RS-232C)	17LE-23090-27 (D3BB)	DSUB9pin (male)	-5 to 105	DDK	1	—
2	D1	Diode	1SS352		-55 to 125	Toshiba	1	Not implemented
3	X2	Crystal oscillator	230HFU-48.00000	DC3.0V±10% 48MHz±50ppm	-20 to 70	Seiko Precision	1	Not implemented
4	IC18	Regulator (1.8V)	AN80P18RSP	1.8V1A	-30 to 85	Matsushita Electric Industrial	1	—
5	S21	Dip switch	CHS08TA	8bit dip switch	-40 to 85	Copal Electronics	1	—
6	S23	Dip switch	CHS08TA	8bit dip switch	-40 to 85	Copal Electronics	1	Not implemented
7	R28,R31	Network resistor (8 components)	CN2A8TD110ΩG or J	110Ω	-55 to 125	KOA	2	—
8	R82,R83	Network resistor (8 components)	CN2A8TD33ΩG or J	33Ω	-55 to 125	KOA	2	—
9	R1, R3, R4, R5, R8, R9, R22, R23, R24, R25, R35, R36, R46, R64, R77, R201	Network resistor (8 components)	CN2A8TD4.7kΩG or J	4.7kΩ	-55 to 125	KOA	16	—
10	R226	Network resistor (8 components)	CN2A8TD4.7kΩG or J	4.7kΩ	-55 to 125	KOA	1	Not implemented
11	CN9	Connector (split board) mother side	DHB-RA60-R131N	60pin	—	DDK	1	—
12	S2, S3	Dip switch	DSS608 DSS808	—	-25 to 85	Fujisoku	2	—
13	CN4	Connector (AUD)	DX20M-36S	AUD36pin straight	—	Hirose Electric	1	Screws necessary (note)
14	C53	Tantalum capacitor	ECSH1CC106R 16MC106MC-TER	16V10μF	-55 to 125	Matsushita Electric Industrial Nippon Chemi-Con	1	—
15	C205, C207, C209, C211	Tantalum capacitor	ECSH1CC106R 16MC106MC-TER	16V10μF	-55 to 125	Matsushita Electric Industrial Nippon Chemi-Con	4	Not implemented
16	L2	Choke coil	ELC0607SKI-5R6K1R9 ELC0607SKI-5R6J1R9	5.6μH1.9A	-20 to 80	Matsushita Electric Industrial	1	Not implemented
17	C1, C2, C3, C5, C7, C8, C9, C11, C12, C13, C15, C16, C18, C20, C21, C23, C27, C30, C37, C62, C63, C73, C74, C75, C76, C77, C92, C93, C201, C203, C204, C206, C208, C210, C212	Ceramic capacitor	GRM21BB11H104KA11B GRM40F104Z50PT	50V0.1μF	-25 to 85	Murata Manufacturing Co.	35	—
18	C78, C83, C84, C85, C86, C87, C88, C221	Ceramic capacitor	GRM21BB11H104KA11B GRM40F104Z50PT	50V0.1μF	-25 to 85	Murata Manufacturing Co.	8	Not implemented
19	C34	Ceramic capacitor	GRM3192C1E103JA01B	25V0.01μF	-55 to 125	Murata Manufacturing Co.	1	—
20	C79, C80	Ceramic capacitor	GRM31M2C2D471JY21B	200V470pF	-55 to 125	Murata Manufacturing Co.	2	—
21	C59, C60, C200	Ceramic capacitor	GRM31M2C2H5R0CY21B	500V5pF	-55 to 125	Murata Manufacturing Co.	3	Not implemented
22	C22	Ceramic capacitor	GRM31MB11C225KC11B	16V2.2μF	-25 to 85	Murata Manufacturing Co.	1	Not implemented
23	C47	Ceramic capacitor	GRM31MB11E105KC01B	25V1.0μF	-25 to 85	Murata Manufacturing Co.	1	—

Section	Symbol	Component	Model number	Specification (constant)	Operating temperature (°C)	Manufacturer	No. of units	Remarks
24	IC7	CPU	HD6417709AF100	QFP	-20 to 75	Hitachi	1	—
25	CN2	Connector (SCI)	HIF3FC-10PA-2.54DSA	10pin	-55 to 85	Hirose Electric	1	Not implemented
26	CN1	Connector (DMA)	HIF3FC-40PA-2.54DSA	40pin	-55 to 85	Hirose Electric	1	Not implemented
27	IC8	SDRAM (64MByte SDRAM)	HM5257165BTD-A6 HM5257165BTD-75	SOP	0 to 60	ELPIDA	1	—
28	R218	Resistor	RK73H2BTD100kF	100kΩ	-55 to 125	KOA	1	—
29	R81	Resistor	RK73H2BTD22F	22Ω	-55 to 125	KOA	1	—
30	R26,R75	Resistor	RK73H2BTD3.3kF	3.3kΩ	-55 to 125	KOA	2	—
31	R219	Resistor	RK73H2BTD360F	360Ω	-55 to 125	KOA	1	—
32	R100, R101, R102, R103, R104, R105, R106	Resistor	RK73H2BTD4.7kF	4.7kΩ	-55 to 125	KOA	7	—
33	R2	Resistor	RK73H2BTD5.6kF	5.6kΩ	-55 to 125	KOA	1	—
34	R7	Resistor	RK73H2BTD51kF	51kΩ	-55 to 125	KOA	1	Not implemented
35	R27	Resistor	RK73H2BTD6.8kF	6.8kΩ	-55 to 125	KOA	1	Not implemented
36	R76	Resistor	RK73H2BTD6.8kF	6.8kΩ	-55 to 125	KOA	1	—
37	R78, R79, R80	Resistor	RK73H2BTD82F	82Ω	-55 to 125	KOA	3	—
38	R40, R41, R66, R220	Jumper Resistor	RK73Z2A	0Ω	-55 to 125	KOA	4	—
39	R65	Jumper Resistor	RK73Z2A	0Ω	-55 to 125	KOA	1	Not implemented
40	IC11	Reset IC	S-80921CNMC-G8R	Detected voltage 2.1V	-40 to 85	SII	1	—
41	X1	Crystal oscillator (7.000MHz)	SG-615PCG 7.000MHzB	SG-615PCG 7.000MHz50ppm※1	-40 to 85	EPSON	1	—
42	X4	Crystal oscillator (27MHz)	SG-615PCW 27MHzB	SG-615PCW 27MHz50ppm※2	-20 to 70	EPSON	1	Not implemented
43	X2	Crystal oscillator (48MHz)	SG-615PCW 48MHzB	SG-615PCW 48MHz50ppm※2	-20 to 70	EPSON	1	Not implemented
44	LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16	LED(Green)	SML-310MTT86	—	-30 to 85	ROHM	16	—
45	IC10	AND gate	SN74HC08ANS	SOP	-40 to 85	TI	1	
46	IC9	Inverter	SN74HC14ANS	SOP	-40 to 85	TI	1	Not implemented
47	IC20	NOR	SN74LVC02A	2 input NOR	-40 to 85	TI	1	—
48	IC2	RS232 transceiver	SN75LV4737ADB	SSOP	0 to 70	TI	1	—
49	IC6	FlashROM (4MByte)	TC58FVT641FT-70	SOP	-40 to 85	Toshiba	1	—
50	IC21	Synchronous counter	TC74HC163AF	SOP	-40 to 85	Toshiba	1	—
51	IC1, IC3, IC4, IC5	Buffer	TC74LCX245F	SOP	-40 to 85	Toshiba	4	—
52	IC13, IC14	Driver IC	TD62083AF	SOP	-40 to 85	Toshiba	2	—
53	S1, S4, S5, S6, S7, S8, S9, S10, S11	Push button SW	TMEG1-01	—	-25 to 70	Fujisoku	9	—
54	Test pin (for signals)	Test pin	LC-4-S (Yellow)	S: copper base solder plating	—	Mac-Eight	24	—
55	Test pin (for GND)	Test pin	LC-3-S-Black	S: copper base solder plating	—	Mac-Eight	7	—
56	Test pin (for CPU1_8V)	Test pin	LC-3-S-Red	S: copper base solder plating	—	Mac-Eight	1	—
57	J3, J4, J5, J8	Jumper	WL-1	Pin section height 4.3mm	-40 to 125	Mac-Eight	4	Not implemented

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indicates components not implemented

S1R72005_QFP Table of Parts

Section	Symbol	Component	Model number	Specification (constant)	Operating temperature (°C)	Manufacturer	No. of units	Remarks
1	CN5	Power supply connector	53109-0410	5.08mm Pitch	-40 to 80	MOLEX	1	—
2	Q20, Q21, Q22	Transistor	2SA1121	PNP	-55 to 125	Toshiba	3	—
3	CN20	Connector	SMA-300-126S	SMA Connector	—	JAE	1	Not implemented
4	IC17	Regulator (2.5V)	AN80P25RSP	2.5V1A	-30 to 85	Matsushita Electric Industrial	1	—
5	IC16	Regulator (2.8V)	AN80P28RSP	2.8V1A	-30 to 85	Matsushita Electric Industrial	1	Not implemented
6	IC15	Regulator (3.3V)	AN80P33RSP	3.3V1A	-30 to 85	Matsushita Electric Industrial	1	—
7	L20,L21	EMI Firter	BLM21PG600SN1	600nH	-55 to 125	Murata Manufacturing Co.	2	—
8	S22	Jumper switch	CAS-120A1	Jumper switch	-40 to 85	Copal Electronics	1	Not implemented
9	S20	Dip switch	CHS08TA	8bit dip switch	-40 to 85	Copal Electronics	1	—
10	R96, R97, R98, R200	Network resistor (8 components)	CN2A8TD4.7kΩG or J	4.7kΩ	-55 to 125	KOA	4	—
11	X3	CERALOCK (12MHz)	CSTCE12M0G15		0 to 70	Murata Manufacturing Co.	1	Not implemented
12	C39	Ceramic capacitor	DEBE33D103ZB3B	2000V10000pF	-25 to 85	Murata Manufacturing Co.	1	—
13	CN8	Connector (split board) OTG side	DHB-PA60-R131N	60pin	—	DDK	1	—
14	L4	EMI Firter	DLP31SN121SL2		-40 to 85	Murata Manufacturing Co.	1	Not implemented
15	C51, C89, C90, C91, C213, C215, C217, C219	Tantalum capacitor	ECSH1CC106R 16MC106MC-TER	16V10μF	-55 to 125	Matsushita Electric Industrial Nippon Chemi-Con	8	Not implemented
16	C42, C49, C50, C52, C54, C55, C56, C57, C58, C67	Tantalum capacitor	ECSH1CC106R 16MC106MC-TER	16V10μF	-55 to 125	Matsushita Electric Industrial Nippon Chemi-Con	10	—
17	L3	Choke coil	ELC0607SKI-5R6K1R9 ELC0607SKI-5R6J1R9	5.6μH1.9A	-20 to 80	Matsushita Electric Industrial	1	Not implemented
18	L1	Choke coil	ELC0607SKI-5R6K1R9 ELC0607SKI-5R6J1R9	5.6μH1.9A	-20 to 80	Matsushita Electric Industrial	1	—
19	C81, C82	Ceramic capacitor	GQM2192C1H240GB01B GQM2192C1H240JB01	50V24pF	-55 to 125	Murata Manufacturing Co.	2	—
20	C4, C64, C65, C66, C68, C69, C70, C214, C216, C218, C220, C222	Ceramic capacitor	GRM21BB11H104KA11B GRM40F104Z50PT	50V0.1μF	-25 to 85	Murata Manufacturing Co.	12	Not implemented
21	C10, C17, C19, C25, C28, C29, C31, C32, C36, C38, C43, C48, C61, C202	Ceramic capacitor	GRM21BB11H104KA11B GRM40F104Z50PT	50V0.1μF	-25 to 85	Murata Manufacturing Co.	14	—
22	C44,C45,C46	Ceramic capacitor	GRM31MB11E105KC01B	25V1.0μF	-25 to 85	Murata Manufacturing Co.	3	—
23	C72	Ceramic capacitor	GRM31MF11C475ZA12B	16V4.7μF	-25 to 85	Murata Manufacturing Co.	1	—
24	C71	Ceramic capacitor	GRM31MR11C155KC11B GRM31MF11C155ZC01	16V1.5μF	-55 to 125	Murata Manufacturing Co.	1	—
25	X3	Crystal oscillator (12MHz)	MA-406 12MHz50*10-6 MA-406 12MHz30*10-6	MA-406 12MHz10pF50ppm※3 MA-406 12MHz10pF30ppm※3	-20 to 70	EPSON	1	—
26	CN6	USB Receptacle	MNE20	USB miniAB	—	ACON	1	—

Section	Symbol	Component	Model number	Specification (constant)	Operating temperature (°C)	Manufacturer	No. of units	Remarks
27	R39	Resistor	RK73H1JTD1.5kF	1.5kΩ	-55 to 125	KOA	1	Not implemented
28	R48, R57, R58	Resistor	RK73H1JTD100kD	100kΩ	-55 to 125	KOA	3	—
29	R49, R51	Resistor	RK73H1JTD15kF	15kΩ	-55 to 125	KOA	2	Not implemented
30	R225	Resistor	RK73H1JTD300D	300Ω	-55 to 125	KOA	1	Not implemented
31	R33, R34	Resistor	RK73H1JTD33F	33Ω	-55 to 125	KOA	2	—
32	R214	Resistor	RK73H1JTD24kD	24kΩ	-55 to 125	KOA	1	—
33	R52	Resistor	RK73H1JTD2.2kD	2.2kΩ	-55 to 125	KOA	1	—
34	R56	Resistor	RK73H1JTD43kD	43kΩ	-55 to 125	KOA	1	—
35	R47	Resistor	RK73H2BTD110F	110Ω	-55 to 125	KOA	1	—
36	R50	Resistor	RK73H2BTD1MF	1MΩ	-55 to 125	KOA	1	—
37	R212	Resistor	RK73H2BTD249D	249Ω	-55 to 125	KOA	1	Not implemented
38	R204, R206, R208	Resistor	RK73H2BTD249D	249Ω	-55 to 125	KOA	3	—
39	R210	Resistor	RK73H2BTD309D	309Ω	-55 to 125	KOA	1	Not implemented
40	R32, R99	Resistor	RK73H2BTD4.7kF	4.7kΩ	-55 to 125	KOA	2	Not implemented
41	R84, R85, R86, R87, R88, R89, R90	Resistor	RK73H2BTD4.7kF	4.7kΩ	-55 to 125	KOA	7	—
42	R202	Resistor	RK73H2BTD412D	412Ω	-55 to 125	KOA	1	—
43	R62, R63	Resistor	RK73H2BTD47kF	47kΩ	-55 to 125	KOA	2	—
44	R215	Resistor	RK73H2BTD51D	51Ω	-55 to 125	KOA	1	Not implemented
45	R92	Resistor	RK73H3ATD1MF	1MΩ	-55 to 125	KOA	1	—
46	R216, R217, R229, R231, R233, R235, R236, R237, R238, R239	Jumper resistor	RK73Z2A	0Ω	-55 to 125	KOA	10	Not implemented
47	R53, R223, R224, R228, R230, R232, R234,	Jumper resistor	RK73Z2A	0Ω	-55 to 125	KOA	7	—
48	R91	Jumper resistor	RK73Z3A	0Ω	-55 to 125	KOA	1	—
49	IC12	OTG LSI	S1R72005F0A0	QFP13-64	-40 to 85	EPSON	1	—
50	R93, R94, R95, R221, R222	Resistor	SL1TE10mF	10mΩ	-55 to 180	KOA	5	—
51	LED17	LED (Green)	SML-310MTT86	—	-30 to 85	ROHM	1	—
52	R211, R213	Variable resistor	ST-3A200 (22)	200Ω	-55 to 125	Copal Electronics	2	Not implemented
53	R203, R205, R207, R209	Variable resistor	ST-3A200 (22)	200Ω	-55 to 125	Copal Electronics	4	—
54	Q11	FET	TPC8302	—	-55 to 150	Toshiba	1	Not implemented
55	Q14	FET	TPCS8205	—	-55 to 150	Toshiba	1	Not implemented
56	Q12,Q13	FET	TPCS8205		-55 to 150	Toshiba	2	—
57	Test pin (for signals)	Test pin	LC-4-S (yellow)	S: copper base solder plating	—	Mac-Eight	40	—
58	Test pin (for DGND)	Test pin	LC-3-S-black	S: copper base solder plating	—	Mac-Eight	4	—
59	Test pin (for V_{BUS}5V, UV_{DD3}_3V, HV_{DD}, LV_{DD})	Test pin	LC-3-S-red	S: copper base solder plating	—	Mac-Eight	4	—
60	J1, J2, J6, J7, J9, J10	Jumper	WL-1	Pin section height 4.3mm	-40 to 125	Mac-Eight	8	Not implemented
61	ZD3	Surge killer	VRD-Z2008		-40 to 125	Ishizuka Electronics	1	Not implemented
62	Jumper line (note)	—	—	0.32mmϕ or 0.26mmϕ	—	—	1	For S22-2pin to DGND connection

200

indicates components not implemented

SHSE_A Table of Parts

Section	Symbol	Component	Model number	Specification (constant)	Operating temperature (°C)	Manufacturer	No. of units	Remarks
1	CNA3	Connector	DHB-RA60-R131N	pin:60	—	DDK	1	
2	CNA1	Connector	KX14-140K5D1	pin:140	-40 to 85	JAE	1	
3	CNA2	Connector	KX14-140K4D1	pin:140	-40 to 85	JAE	1	
4	R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365	Resistor	RK73H1JTD27F MCR03EZHF27R0	27Ω	-55 to 125	KOA ROHM	13	

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