CMOS 4-BIT SINGLE CHIP MICROCOMPUTER
S5U1C63000H2 Manual
(S1C63 Family In-Circuit Emulator)
New configuration of product number

Starting April 1, 2001, the product number has been changed as listed below. Please use the new product number when you place an order. For further information, please contact Epson sales representative.

Devices

<table>
<thead>
<tr>
<th>S1</th>
<th>C</th>
<th>63158</th>
<th>F</th>
<th>0A01</th>
<th>00</th>
</tr>
</thead>
</table>

- Packing specification
- Specification
- Package (D: die form; F: QFP)
- Model number
- Model name (C: microcomputer, digital products)
- Product classification (S1: semiconductor)

Development tools

<table>
<thead>
<tr>
<th>S5U1</th>
<th>C</th>
<th>63000</th>
<th>A1</th>
<th>1</th>
<th>00</th>
</tr>
</thead>
</table>

- Packing specification
- Version (1: Version 1)
- Tool type (A1: Assembler Package)
- Corresponding model number
  (63000: common to S1C63 Family)
- Tool classification (C: microcomputer use)
- Product classification
  (S5U1: development tool for semiconductor products)
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CHAPTER 1 INTRODUCTION

S5U1C63000H2 (In-Circuit Emulator for S1C63 Family) is a hardware tool to effectively develop software for the S1C63 Family, 4-bit single chip microcomputers. In combination with a peripheral circuit board (S5U1C63xxxP), it provides the development environment of the software using a personal computer as a host computer, which requires Windows.

This manual describes the operation of the S5U1C63000H2 hardware and connections of the S5U1C63000H2 system. Refer to "S5U1C63000A Manual" for use of the debugging commands. Figure 1.1 shows the external view of the S5U1C63000H2.

Fig. 1.1 External view of S5U1C63000H2
CHAPTER 2 S5U1C63000H2 PACKAGE

2.1 Components

This package is common with all models of the S1C63 Family. After unpacking the S5U1C63000H2 package, check to see that all of the following components are included.

Figure 2.1.1 shows the packing structure.

1. S5U1C63000H2 (main unit with LCD board) ...................................................... 1 unit
2. RS232C cable (for IBM PC/AT) ........................................................................ 1 cable
3. AC adapter ........................................................................................................ 1 pcs.
4. AC cable .......................................................................................................... 1 cable
5. Jig for installing/dismounting board ......................................................... 2 pcs.
6. S5U1C63000H2 Manual (S1C63 Family In-Circuit Emulator) ........ 1 copy (this manual)
7. Flat cable with 50-pin × 2 connectors ............................................................. 1 pair
8. Flat cable with 34-pin connector .................................................................... 1 cable
9. 50-pin connector for target system ................................................................. 2 pcs.
10. 34-pin connector for target system ............................................................... 1 pcs.
11. User registration card .................................................................................... 1 card
12. Warranty card .................................................................................................. 1 card
13. Precautions on using the S5U1C63000H2 ..................................................... 1 sheet

Note: Following items need to be provided separately, not included in this package.

14. S5U1C63xxxP board (included in the S5U1C63xxxP package)
15. S5U1C63xxxP Manual (included in the S5U1C63xxxP package)
16. S1C63 Family Debugger (included in the S1C63 Family Assembler package)
17. S5U1C63000A Manual (included in the S1C63 Family Assembler package)

Fig. 2.1.1 Packing structure
### 2.2 Component Specifications

Table 2.2.1 shows the specifications of the component in the S5U1C63000H2 package.

<table>
<thead>
<tr>
<th>No.</th>
<th>Components</th>
<th>Items</th>
<th>Specifications</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>S5U1C63000H2</td>
<td>Dimensions</td>
<td>282 (W) × 177 (L) × 90 (H)</td>
<td>Rubber feet included</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Weight</td>
<td>Approx. 3.5 kg (main body)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>External color</td>
<td>Cygnus white</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input voltage</td>
<td>DC 5 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power consumption</td>
<td>2 A, max.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Board mounted</td>
<td>ICE board and LCD board</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RS232C cable (for IBM PC/AT)</td>
<td>Length</td>
<td>3 m</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interface level</td>
<td>EIA-RS232C level</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cable</td>
<td>12-pair shielded cab tyre cable</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cable-ended connector</td>
<td>DEU 9S-F0</td>
<td>or equivalent</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Connector on host</td>
<td>DE-9P</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>AC adapter</td>
<td>Dimensions</td>
<td>160 × 80 × 60</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input voltage</td>
<td>AC 90 V to 264 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input frequency</td>
<td>47 Hz to 63 Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power consumption</td>
<td>25 W, max. (in ICE system load)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output voltage+current</td>
<td>DC 5 V/5 A, with over current protection</td>
<td>Outside: 5 V, Inside: 0 V</td>
</tr>
<tr>
<td>4</td>
<td>AC cable</td>
<td>Length</td>
<td>1.8 m</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Plug type</td>
<td>Bipolar with ground</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Accessories</td>
<td>Jig</td>
<td>for installing/dismounting option boards</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Package</td>
<td>Dimensions</td>
<td>380 (W) × 260 (L) × 225 (H)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Materials</td>
<td>W carton, cardboard</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total weight of package</td>
<td>Approx. 5 kg</td>
<td></td>
</tr>
</tbody>
</table>

* Peripheral circuit board is sold separately

### 2.3 Environmental Conditions for Operation

Table 2.3.1 shows the environmental conditions to operate S5U1C63000H2 that has to be used.

<table>
<thead>
<tr>
<th>No.</th>
<th>Items</th>
<th>Specifications</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Operating temperature</td>
<td>5 to 40 °C</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Storage temperature</td>
<td>-10 to 60 °C</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Operating humidity</td>
<td>35 to 80%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Storage humidity</td>
<td>20 to 90%</td>
<td>No condensation</td>
</tr>
<tr>
<td>5</td>
<td>Resistance to vibration</td>
<td>Operating: 0.25 m/S²</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transportation: 1 m/S²</td>
<td></td>
</tr>
</tbody>
</table>
2.4 Specifications of Operation Panels

This section explains the operation of each switch. Figure 2.4.1 shows the external view of the panels.

*Fig. 2.4.1 External view of S5U1C63000H2 panels*
Table 2.4.1 shows the function of each component on the panels.

<table>
<thead>
<tr>
<th>No.</th>
<th>Position</th>
<th>Indicated symbol</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Side panel</td>
<td>CB</td>
<td>Circuit breaker</td>
<td>The breaker cuts off the power of the ICE system (ICE board, LCD board, peripheral circuit board and target board) at consumption current of 3 A or more. A small staff of the breaker comes up at the shut-off. The staff should be at the recessed position for normal operating status. The breaker does not work at the normal operation.</td>
</tr>
<tr>
<td>2</td>
<td>Front panel</td>
<td>ICE/RUN</td>
<td>ICE mode/Free run mode switch</td>
<td>Shifting the switch to &quot;RUN&quot; (slant to right) loads a target program from the flash memory in the S5U1C63000H2 without connection to a host computer and gets the system into free run status of the target program. In this mode, however, debugging function such as break and trace does not work. Shifting the switch to &quot;ICE&quot; (slant to left) enables the S5U1C63000H2 to be connected with a host computer and debugging function is operative through the debugger on the host computer.</td>
</tr>
<tr>
<td>3</td>
<td>Front panel</td>
<td>TRGOUT</td>
<td>Tracing trigger output terminal</td>
<td>Upon coincidence of trigger conditions with a tracing trigger point, a pulse is output from this terminal.</td>
</tr>
<tr>
<td>4</td>
<td>Front panel</td>
<td>STOPOUT</td>
<td>HALT/SLEEP status output terminal</td>
<td>When the S1C63000 CPU is in HALT or SLEEP status, low level signal is output from this terminal. This is used to measure execution rate of the CPU. At the break mode, low level signal is also output.</td>
</tr>
<tr>
<td>5</td>
<td>Front panel</td>
<td>TRCIN</td>
<td>Trace input terminal</td>
<td>Information is stored in the trace memory by connection with a signal of the target system.</td>
</tr>
<tr>
<td>6</td>
<td>Front panel</td>
<td>BRKIN</td>
<td>Break input terminal</td>
<td>A running program enters in break status by input a low level signal from the target system.</td>
</tr>
<tr>
<td>7</td>
<td>Front panel</td>
<td>GND</td>
<td>Ground terminal for above</td>
<td>In case the above terminal is monitored with such an oscilloscope, the GND line of the oscilloscope is connected to this terminal. This is also used as a GND in case the signals are input to the above terminals.</td>
</tr>
<tr>
<td>8</td>
<td>Front panel</td>
<td>DSW1–8</td>
<td>DIP switch</td>
<td>This is a switch to set a baud rate of communication with a host computer. 9600 bps has been set at ex-factory. Refer to Section 2.5 for details.</td>
</tr>
<tr>
<td>9</td>
<td>Front panel</td>
<td>POWER</td>
<td>Power-on LED</td>
<td>This green LED lights upon power-on of S5U1C63000H2.</td>
</tr>
<tr>
<td>10</td>
<td>Front panel</td>
<td>EMU</td>
<td>Emulation LED</td>
<td>This red LED lights when the target program is in running status.</td>
</tr>
<tr>
<td>11</td>
<td>Front panel</td>
<td>SLP/HLT</td>
<td>Halt LED</td>
<td>This yellow LED lights when the S1C63000 CPU executes the HALT or SLP instruction. This LED also lights when the peripheral circuit board has not been installed.</td>
</tr>
<tr>
<td>12</td>
<td>Front panel</td>
<td>PC15–0</td>
<td>Program counter indicator</td>
<td>These LEDs indicate the program counter (PC) value while the program is running and also hold the PC value at the break point while the program is breaking.</td>
</tr>
<tr>
<td>13</td>
<td>Front panel</td>
<td>RS232C</td>
<td>RS232C connector</td>
<td>This is a connector to connect a RS232C cable. Tightening the connector with screws is recommended while using.</td>
</tr>
<tr>
<td>14</td>
<td>Rear panel</td>
<td>DC 5V</td>
<td>DC input connector</td>
<td>This is a connector to connect the DC cable of the AC adapter dedicated for S5U1C63000H2.</td>
</tr>
<tr>
<td>15</td>
<td>Rear panel</td>
<td>POWER</td>
<td>Power switch</td>
<td>Turns the S5U1C63000H2 power on and off.</td>
</tr>
</tbody>
</table>
2.5 Setting the Dip Switch

The S5U1C63000H2 works with a personal computer that runs Windows as a host. With a general computer that meets the condition, the serial transfer rate set at the factory (9600 bps) is good for use. In case the rate is changed, the transfer rate between the host computer can be changed by this switch. The switch also sets a self diagnostic function, which is equipped in the S5U1C63000H2, working or not working at the power on. Figure 2.5.1 shows the dip switch.

**Fig. 2.5.1 Dip switch**

<table>
<thead>
<tr>
<th>Setting baud rate</th>
<th>Baud rate setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1–3</td>
<td>SW4</td>
</tr>
<tr>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>OPEN</td>
<td>ON</td>
</tr>
<tr>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>OPEN</td>
<td>ON</td>
</tr>
<tr>
<td>Other settings</td>
<td>Do not set.</td>
</tr>
</tbody>
</table>

**Note:** The setting at the host end is recommended to be "9600 bps, 8-bit character, 1 stop bit, no parity".

<table>
<thead>
<tr>
<th>Setting the self diagnostic function</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW8</td>
<td>Self diagnosis On</td>
</tr>
<tr>
<td>ON</td>
<td>Self diagnosis Off (factory setting)</td>
</tr>
</tbody>
</table>

**Note:** When the S5U1C63000H2 is started with the self diagnosis on, it takes approx. 5 minutes to be ready for use.

Open means that the switch lever is at upper side.
On means that it is at lower side.
CHAPTER 3  CONNECTION

This chapter describes the connection between the S5U1C63000H2 and a host computer and the Peripheral circuit board (S5U1C63xxxP).

3.1 AC Cable

The S5U1C63000H2 package includes a dedicated AC cable (3 poles type) and an AC adapter. The AC cable is connected into the AC inlet on the AC adapter. The common ground frame line should be used for connecting the S5U1C63000H2 and the host computer as shown in Figure 3.1.1.

3.2 DC Cable

The DC output cable of the AC adapter is connected to the DCIN (DC 5 V input) terminal as shown in Figure 3.1.1.

3.3 Connection with Host Personal Computer

Figure 3.3.1 shows the external view of the RS232C cable connector and Table 3.3.1 shows the signal specifications of the RS232C cable.

<table>
<thead>
<tr>
<th>Terminal No.</th>
<th>Signal name</th>
<th>Signal meaning</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>TXD</td>
<td>Transmit data from HOST to ICE</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RXD</td>
<td>Receive data from ICE to HOST</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RTS</td>
<td>Request to send from HOST</td>
<td>Normally used as ON</td>
</tr>
<tr>
<td>8</td>
<td>CTS</td>
<td>Clear to send from ICE</td>
<td>Normally used as ON</td>
</tr>
<tr>
<td>5</td>
<td>SG</td>
<td>Signal ground</td>
<td></td>
</tr>
</tbody>
</table>

Connect S5U1C63000H2 to the personal computer using the supplied RS232C cable and tighten the connector screws to fix the cable.
3.4 Installing Peripheral Circuit Board (S5U1C63xxxP)

By installing the S5U1C63xxxP peripheral circuit board (to be separately sold) into a slot of the S5U1C63000H2, a debug system can be made corresponding to each device of the S1C63 Family. Figure 3.4.1 shows installing method of the peripheral circuit board. The S5U1C63000H2 is equipped with a main control board and a LCD drive board.

Fig. 3.4.1 Installing method of the peripheral circuit board

(1) Unfasten the screws located on the left and right sides of the front panel of the S5U1C63000H2 by turning them counterclockwise, then remove the front panel.

(2) Insert the peripheral circuit board into the uppermost slot and push it using the jig attached with the S5U1C63000H2 as shown in Figure 3.4.2.

Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the peripheral circuit board has been firmly fitted into the internal slot of the S5U1C63000H2, remove the jig.

Fig. 3.4.2 Installing the peripheral circuit board

(3) Dismounting peripheral circuit board

Set the jig into position as shown in Figure 3.4.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides and pull the peripheral circuit board out of the S5U1C63000H2.

Fig. 3.4.3 Dismounting the peripheral circuit board

(4) Mounting the front panel

Mount the front panel removed at the step (1) on the main case by pushing and turning two screws located at both side.

(5) The jig has a magnet for keeping under the bottom plate of the case while not in use.
CHAPTER 4  GETTING STARTED

There are two operation modes in the S5U1C63000H2. One is ICE mode to be started with the debugger in connection with a host machine (the ICE/RUN switch on the front panel is set to ICE side) and the other one is free run mode to run a target program without a host machine (the ICE/RUN switch is set to RUN side).

4.1 Operation in ICE Mode

After the S5U1C63000H2 and the host machine is connected with the RS232C cable and the ICE/RUN switch is set to ICE side, turn the host machine and S5U1C63000H2 power on. It enables the S5U1C63000H2 to be controllable by the host machine and the debugger can be executed on the host. Following shows the operation sequence of the S5U1C63000H2 after power-on.

(1) Turning the S5U1C63000H2 power on
   The power LED (green) is on, and the SLP/HLT LED (yellow) is momentary on. The PC8 and PC4 LEDs (red) go on (program counter is 110H).

(2) Starting the debugger
   Upon starting the debugger on the host, the SLP/HLT LED (yellow) goes momentary on.

(3) Execution of a target program
   When the debugger starts execution of a target program, the EMU LED (red) is turned on to indicate the emulation mode. While the target program is executed, the PC LEDs (red) indicate the current program counter value. When the SLP or HLT instruction is executed, the SLP/HLT LED (yellow) goes on and the PC LEDs (red) stop.

(4) Occurrence of a break
   When the target program stops at the break point set with the debugger, the EMU LED (red) goes off and the PC LEDs (red) stops at the break address. The break address means the program counter of next execution.

4.2 Operation in Free Run Mode

By turning the S5U1C63000H2 power on after the ICE/RUN switch located on the front panel is set to RUN side, the S5U1C63000H2 enters in the free run mode that executes the target program continuously. Following shows the execution flow of the target program in the free run mode.

(1) Turning the S5U1C63000H2 power on
   The power LED (green) is on, and the SLP/HLT LED (yellow) is momentary on. PC8 and PC4 LEDs (red) go on (program counter is 110H).

(2) Setting data from flash memory
   The S5U1C63000H2 read the configuration information and various mask option information for each model from the built-in flash memory and set them to the controller. The target program is also read from the flash memory and transferred to the built-in emulation memory.

(3) Execution of the target program
   The S5U1C63000H2 executes the target program from the reset address. The PC LEDs (red) indicate the current program counter position during execution. When the SLP or HALT instruction is executed, the SLP/HLT LED (yellow) goes on and the PC LEDs (red) stop.
Notes on free run mode

(1) Any configuration information, various mask information and target program have not been written in the flash memory built into the S5U1C63000H2 at the time of ex-factory. Even though the S5U1C63000H2 enters in the free run mode without the data, it does not execute any target program and while the program counter on the front panel indicates the reset address of 110H. Therefore, it is necessary to write a target program, configuration information and various mask option information into the flash memory in the ICE mode before setting the free run mode.

(2) In the free run mode, the break functions and the trace functions cannot be used. The free run mode only execute a target program and display the current program counter with the LEDs on the front panel. The BRKIN terminal on the front panel becomes invalid.

(3) In the case any incorrect access exceeding configured program size or data RAM size is occurred by reason of a improper target program, the S5U1C63000H2 immediately stops at the program counter, where the incorrect access is made, by the LEDs on the front panel. In order to reset this situation, the power should be off. Before the free run of the target program is carried out again, the program must be completely debugged on the ICE mode. In the case any control to exceed program sizes such as jump or call to outside of the program, it stops before the access to an incorrect area. In the case any control to exceed data size such as read or write into outside of the data RAM area, it stops after the access to the incorrect area.

(4) The S5U1C63000H2 may takes approx. 5 minutes after it is turned on until it starts execution of the target program.
CHAPTER 5  OPERATION AND FUNCTION OF S5U1C63000H2

This chapter describes operations, functions in detail and restrictions in the emulation mode of the S5U1C63000H2.

5.1 General of Operation

Figure 5.1.1 shows the functional block diagram of S5U1C63000H2.

The S5U1C63000H2 has a processor to control in-circuit emulation, which processes the ICE commands. The function to execute or stop target programs by the S1C63000 CPU is called emulation, of which control is done by the emulation control portion.

Operation that the S1C63000 CPU is working (specified by the G command) and single step operation (specified by the S or N commands) are called emulation mode, on which the EMU LED goes on and program counter display LEDs real timely indicate the program counter of the program running. The other status is called standby mode, which turns off the EMU LED and makes the program counter display LEDs show program counter position at the break.

The target program to be executed with the S1C63000 CPU is stored in the emulation program memory and data RAM area of the S1C63000 CPU is assigned to the emulation data memory. Loading a program from the flash memory or the host is done by the S5U1C63000H2 control processor in the standby mode. The trace control portion records execution bus cycle of the S1C63000 CPU and consists of a memory of 8,192 words × 120 bits. Such large size memory enables the register value inside the S1C63000 CPU to be real timely recorded. The tracing is done in the emulation mode and it is analyzed by the S5U1C63000H2 control processor in the standby mode.

The break control portion compares the bus condition of the S1C63000 CPU with break points and stops the execution of the target program upon coincident. The break can be also real timely made by register values of the S1C63000 CPU. While a target program is running, the target monitor portion of the S5U1C63000H2 control processor monitors executing program counter value of the S1C63000 CPU and RAM contents at watching points. The monitored result is displayed as on-the-fly information. The S1C63000 CPU can real timely execute the target program while the information is displayed.
5.2 Break Function

- **Forced break**
  The debugger on the host machine can forced break the emulation. This function is useful when the program counter does not proceed by executing the SLP or HALT instruction in a single step process.

- **Break commands**
  Some break commands are available to set various breaking conditions. A break occurs when the break condition specified by the command and status of the S1C63000 CPU are met.

- **Break by accessing to undefined area**
  This break occurs when the target program accesses an address exceeding the ROM capacity of the actual chip. The break is also occurred when any address other than the RAM area or mapped I/O area of the actual chip is accessed.

- **Break by accessing write protect area**
  This break occurs when the target program writes data to the read only memory such as a character generator ROM. The memory contents are protected even this break occurs.

- **Break by incorrect stack accessing**
  This break occurs when the target program makes incorrectly stacking operation exceeding the defined stack area in the S1C63000 CPU.

- **BRKIN terminal**
  When a signal is input to the BRKIN terminal, a break occurs at the falling edge of the signal.

5.3 Monitoring Terminals

- **TRGOUT output terminal**
  A low level pulse is output at the T3 state of the clock when the trace trigger condition and the bus cycle are met.

  ![Fig. 5.3.1 TRGOUT terminal output](image)

- **STOPOUT output terminal**
  A low level is output when the S1C63000 CPU is suspended (by execution of the HALT or SLP instructions). This terminal also outputs low level during break.

  ![Fig. 5.3.2 STOPOUT terminal output](image)
● **TRCIN input terminal**
  By connecting a signal line of the target system to this terminal, trace information is stored into the trace memory. "1" is written to the trace memory when it is not connected or the signal is at high level, and "0" is written to the trace memory when the signal is at low level. The signal is sampled at the rising edge of T4 state.

● **BRKIN input terminal**
  A break occurs when a low level signal is input to this terminal while the target program is running. To use this terminal for the break function, the low level pulse must be 20 msec or longer. By connecting the TRGOUT output terminal to the BRKIN input terminal, breaks can be occur according to the trace trigger conditions.

### 5.4 Display During Execution and During Break

The S5U1C63000H2 control processor monitors the execution status of the S1C63000 CPU while the target program is running. It displays the S1C63000 CPU’s execution status in every 500 msec when the on-the-fly display mode is specified. Program counter value that are displayed during break show the address to be executed in next step. Values in all registers are at the time of the break.

The LED’s (PC15–PC0) on the front panel indicate the executed program counter value during execution, and stops at the break address when a break occurs.

### 5.5 Break Commands

The S5U1C63000H2 has abundant break functions.

1. **PC break**
   This break function is specified by the BP command. When the program counter of the S1C63000 CPU coincides with the specified address, a break occurs before executing the instruction. Multiple PC values (up to maximum size of program memory) can be specified as break points.

2. **PC sequential break**
   This break function is specified by the BS command. The break occurs when the PC of the S1C63000 CPU counts three addresses in specified order. The pass count can be specified for the last address. The sequence (address 1 coincidence) → (address 2 coincidence) → (address 3 counted by specified times) breaks the execution.

3. **Break by data access**
   This break function is specified by the BD command. The break occurs immediately after the target program accesses the data memory in the specified condition (AND condition of address, data and read/write operation). It is possible to specify a range for the address condition, a mask in bit units for the data condition and a mask for the read/write condition. This specification can set one break point only.

4. **Break by register value**
   This break function is specified by the BR command. When the register values of the S1C63000 CPU coincides with the specified values, a break occurs immediately after the instruction is executed. An AND condition of A/B registers, E/I/C/Z flags and X/Y registers can be specified. It is also possible to specify masking on each register. This specification can set one break point only.

The above break functions, (1), (2), (3), (4), can be independently specified. When the target program is executed with all specified commands, BP, BS, BD, BR, breaks occur by meeting any condition.
5.6 Target Interrupt and Break

When an interrupt in the target program and a break are simultaneously occurred, the target interrupt is prioritized. The break occurs after completing the stack operation of the interrupt. The program counter at the break shows the top address of the interrupt handler routine. When the target program is restarted, it executes from the top address of the interrupt handler routine.

It is the same when "I (interrupt flag) = 1" is set as the break condition by the BR command. The break occurs when the I flag goes 1. However if an interrupt occurs simultaneously, the contents of the flags after the break is displayed as "EICZ:0000" (the I flag is reset) because of the prioritized interrupt process.

5.7 Trace Function

In the execution of the emulation mode, information of the S1C63000 CPU (PC, instruction code, data RAM address, data content and CPU register value) is stored into the trace memory at every CPU bus cycle. The trace memory has a capacity of 8,192 cycles, which can store the latest instructions up to 4,096 in 2 bus cycles instruction and 2,048 in 4 bus cycles instruction.

Figure 5.7.1 shows the trace function. When the trace memory is full, old information is erased and new information is overwritten. TP called trace pointer shows that the point of 0 means the earliest instruction and the break point means the latest information. The maximum value of the TP is 8,191.
5.8 Trace Mode

There are following three trace modes.

(1) All bus cycle trace mode
   In this trace mode, all bus cycles are traced during run emulation and step emulation until a break occurs.

(2) Specified PC range trace mode
   In this mode, bus cycles within the specified range (or outside the specified range) are traced during run emulation and step emulation until a break occurs. This function is useful for cases of tracing objective work data only or removing WAIT routine from the trace.

(3) Single delay trigger
   In this mode, starting a run emulation starts tracing all bus cycles. When the emulation hit the trace trigger condition, the trace continues for the specified bus cycles, and then it stops. The trace information is displayed after a break.

In the debugger, one of the above modes can be selected by the TM command.

5.9 Trace Trigger Point

In the S5U1C63000H2, a trace trigger point can be specified independent of breaking points. The trace trigger point is specified as the program counter conditions of the S1C63000 CPU. A low level pulse is output from the TRGOUT terminal with the timing of T3 upon coincidence of the specified value and the program counter. The information of the trace trigger point is also stored into the trace memory. In the single delay trigger mode, the trace trigger point becomes a condition for stopping the trace.

5.10 Coverage Function

The S5U1C63000H2 can retrieve and display the address information of the program accessed at the execution. The confirmation of portions whether failure analysis or debugging is completed or not can be done by checking the program through reference of the coverage information after running the program for a long time. This function is specified by the CV or CVC commands.

5.11 Measurement of Execution Time

The S5U1C63000H2 has a function to measure the time from start to break of target programs or to count the bus cycles. This function is set by the MD command.

(1) Time measurement mode
   (a) Range of time measurement
       1 µsec to 1*(2^{31} -1) µsec (= 2,147 sec = 36 minutes)
   (b) Measurement error
       ±1 µsec
   (c) Units of time display
       Micro second (µsec)

(2) Bus cycle count mode
   (a) Range of cycle measurement
       1 bus cycle to (2^{31} -1) bus cycles (= 2*10^9 bus cycles)
   (b) Measurement error
       0 cycle
5.12 Self Diagnosis Function

In the S5U1C63000H2, it is possible to select whether the self diagnosis at power on is executed or not.

(1) No self diagnosis mode (DSW8: on, factory setting)
When the DIP switch 8 on the front panel of the S5U1C63000H2 is set to on, the S5U1C63000H2 becomes ready to accept commands without the self diagnosis after power on.

(2) Self diagnosis mode (DSW8: open)
When the switch is set to open, the S5U1C63000H2 execute following self diagnosis after power on, and then it becomes ready to accept commands.

(a) ROM test
   Check-sum test of the firmware
(b) RAM test
   Read/write test of the RAM in the S5U1C63000H2
(c) Flash memory test
   Check sum test of the flash memory
(d) Emulation test
   Tests the break function by executing a run emulation for a few steps on the emulation memory.

The self diagnosis takes about five minutes after power on.
If an error is displayed while testing, it is considered to be failure of the hardware. Please consult us.

5.13 Restrictions on Emulation

(1) Timer operation in standby mode
In the emulation with the peripheral circuit board connected to the S5U1C63000H2, the S1C63000 CPU is ordinarily at the idle status (standby mode) as shown in Section 5.1. In the standby mode, the S5U1C63000H2 executes the monitor program and the peripheral circuit board is in stop status. The S5U1C63000H2 executes the target program by the G command and returns to the monitor program after a break occurs.

In the models having a timer and a watch dog timer, the timer is operated only when the target program is executed if the timer is active. Therefore, in the single step operation, a real time counting cannot be done with the timers in the S1C63xxx.
(2) **Interrupt in standby mode**
In the standby mode, interrupt requests from the target system is reserved. The interrupt while the monitor program is being executed is accepted at the execution of the target program. For instance, when an interrupt request from the target system is generated while breaking, the interrupt is accepted immediately after the target program restarts if the interrupt is enabled in the S1C6300 CPU.

(3) **Interrupt at single step operation**
Interrupts during single step operation can be enabled or disabled using the MD command. Each operation is as follows.

- **When interrupt is enabled**
  If an interruption request is generated while a target program step is executed by the S or N commands, the interrupt processing is done at the time of the instruction execution, and the execution stops after fetching the vector address of the interrupt. Therefore, next single step operation executes the interrupt handler routine. When the HALT or SLP instructions are executed by the S or N commands, the commands are executed until a interrupt is occurred. In this status, a forced break input from the host computer suspends the execution.

- **When interrupt is disabled**
  Interrupt processing are not executed by the S command. Therefore, the execution of the HALT or SLP instructions is immediately suspended, and the program counter indicates an address next to the HALT or SLP instructions. The N command operates similar to the S command in the execution of the main routine, however, it enables interrupts regardless of the setting by the MD command in the execution of the sub-routine.

(4) **Data read from undefined RAM area**
When a data RAM (ROM) area or an I/O area that is not available in the actual IC chip is read, the read data becomes indefinite. Read data from the actual IC is also indefinite, however it is different from the S5U1C63000H2.

(5) **Detection of SP1 incorrect stack access**
It is possible to detect any incorrect stack access to out of SP1 area by specifying the SP1 area with the BSP command.
The S1C63000 CPU has a queue register and takes stack value in advance in order to make high speed process of the stacking operation for the CALR instruction and interrupts. Therefore, when a value is returned from the top address of the stack, it takes the stack value beyond the top address and write it into the queue register. This operation works without any problem, however, the queue register has an indefinite value. In order not to make this process incorrect access, it is necessary to add three addresses onto the real using SP1 area.

(6) **Data read break**
In the execution of "INT addr6" instruction, setting break on the data read condition may break program running, because dummy read cycle of a memory specified by addr6 operand is added. For instance, when the break at read cycle is set by the break data set command (BD), the dummy read hits the break condition.
(7) Register (data) break

The register (data) value after completion of the break operation may differ from the original setting register (data) condition for the break. For instance, in the timing chart to set sequentially 5 and 6 into the A register, if the A register is 5 as a register break condition;

![Timing Chart](image)

The S5U1C63000H2 judges the register data at the point of "↑", and judges that the A register is 5 at the point of ②. When the program is broken at this point, it has executed the next command of "ld %a, 6", therefore, the break is occurred after the A register is set to 6. This means that the A register content has been changed to 6 when the content is refereed after the break. This is also applied to the break by accessing to undefined area function.

(8) Register (data) break and hardware interrupt

The register (data) value after completion of the break operation may differ from the original setting register (data) condition for the break. Furthermore, when a hardware interrupt is occurred in this point, the break address shifts to the top address of the interrupt handler routine. For instance, in the timing chart to set sequentially 5 and 6 into the A register, if the A register is 5 as a register break condition, and a hardware interrupt is occurred while executing "ld %a, 5";

![Timing Chart](image)

In the timing chart above, if the interrupt is occurred (at the falling edge) at the point of ①, the S1C63000 CPU outputs IACK to show the execution of the interruption response cycle. The interrupt processing can not be stopped while this IACK is at low level. Therefore, the S5U1C63000H2 can not stop the interrupt in spite of its judgment that the A register becomes 5 at the point of ② because the IACK is at low level, and the break is occurred after jumping to the interrupt vector address.
CHAPTER 6  NOTES ON USING

Pay attention to the following matters for proper use of the S5U1C63000H2.

6.1 Notes on Operations

(1) Connection and disconnection between units
Make sure that the S5U1C63000H2 and the personal computer are off when installing the peripheral circuit board (S5U1C63xxxP), connecting cables and disconnecting them. Specially, the connection of the target cable with the power on may make permanent destruction of IC’s inside due to its CMOS structure.

(2) Power on, off
When the power of the S5U1C63000H2 is on again after off, remain off condition for 10 seconds or more. The power on without such interval may result in incorrect power-on-reset operation and/or working the circuit breaker of the S5U1C63000H2.

(3) Peripheral circuit board (S5U1C63xxxP)
A peripheral circuit board is required for operation of the S5U1C63000H2. The S5U1C63000H2 package does not include peripheral circuit board that needs to be separately provided. If the S5U1C63000H2 is turned on without peripheral circuit board installed, the "HLT/SLP" LED on the front panel of the S5U1C63000H2 goes on and the LEDs to indicate the program counter value show 110H.

(4) Over current protection
If the power of the S5U1C63000H2 is on under the condition that VDD and VSS are short-circuited on the target system, the power LED does not turn on due to cut off of the output current working the over current protection in the dedicated AC adapter. The circuit breaker cuts the power at the load current of 3 A or more on the target system.

6.2 Differences from Actual IC

(1) Initialization of RAM
Data RAM of the actual IC becomes indefinite value, however, of the S5U1C63000H2 is initialized to 0AH. Therefore, the initialization must be done in the target program, and any program depending on the initial value must not be made.

(2) Initialization of registers
In the actual IC, registers have indefinite values at power on and keep values prior to the reset except the program counter (PC), the interruption flag (I) and the extension flag (E). However, the S5U1C63000H2 is initialized to 0AH (4-bit), 0AAH (8-bit) and 0AAAAH (16-bit) at the power on and at the software reset by the command of the debugger. Because of this, each register must be initialized, and any program depending on the initial value must not be made. The reset switch on the peripheral circuit board and the hardware reset input from the I/O connector keep values prior to the reset as the actual IC.

(3) Access to undefined area
In the S5U1C63000H2, the access to the undefined area causes break. However, the S5U1C63000H2 has RAM for the undefined area, and the break occurs after accessing to the undefined area, so that it can writes any value into the undefined area. If execution of the target program is restarted after the break by accessing to undefined area, it works with non-existing memory. Therefore, any program to read/write into the undefined area must not be made.

(4) Data dump
The S5U1C63000H2 uses a peripheral circuit board clock for access to RAM, ROM, LCD and I/O area with the data dump command. When the I/O area is read in the target program, there may have a time delay until the correct value is obtained due to the parasitic capacitance and the pull-up/down resistors of each I/O terminal. Therefore, the value read on the target program may differ from the value read by the dump command.
CHAPTER 7 MAINTENANCE AND WARRANTY

7.1 Diagnosis Test

The self diagnosis test is executed by setting SW8 of the DIP switch to OPEN and starting the debugger after power of the S5U1C63000H2 on.

Debugger for S1C63 Ver x.xx
Copyright(C) SEIKO EPSON CORP. xxxx
Connecting with ICE ............
DIAG test, please wait 5 min. .. done ← ➀
Parameter file name : xxxxxxxxx.par
  Version : xx
  Chip name : xxxxx
CPU version    : x.x
PRC board version : x.x
LCD board version : x.x
EXT board version : x.x
ICE hardware version : x.x
ICE software version : x.x
DIAG test      : OK.
Map ......................... done
Initialize .................... done
>

When an error is detected, the error message is output at the point of ➀ instead of “done”. If an error message is output, stop using the S5U1C63000H2 because it may have a hardware failure. This diagnosis test takes approx. 5 minutes for completion because of its precise inspection. Even in the free run mode, it takes approx. 5 minutes for the self diagnosis test before the target program is executed.

7.2 Warranty

Please refer to the warranty card attached to the unit for the warranty details.
CHAPTER 8  TROUBLE SHOOTING

Following shows some hardware errors and their possible causes.

- **A message of "connecting with ICE...failure" is displayed at the execution of the debugger.**
  - Is power of S5U1C63000H2 on?
  - Is circuit breaker (CB) off?
  - Is host cable connected correctly?
  - Is DIP switch of S5U1C63000H2 set correctly?
  - Is baud rate between host and ICE set correctly?
  - Is target cable connected correctly?
  - Is various board (peripheral circuit board, LCD board) inserted firmly?

- **The circuit breaker (CB) operates and the power LED goes off when the S5U1C63000H2 power is turned on.**
  - Is target cable connected correctly?
  - Is VDD or VSS short-circuited on a target?

Refer to "S5U1C63000A Manual" for operations of the debugger.
CHAPTER 9  SPECIFICATIONS OF LCD BOARD

9.1 Introduction

9.1.1 General description of LCD board
The LCD board provides on a board the peripheral circuits (LCD driver) of the S1C63 Family microcomputers other than the core CPU. The board can work as an emulator corresponding to each model of the S1C63 Family by installing into the S5U1C63000H2 along with a S1C63 Family peripheral circuit board (S5U1C63xxxP). This board may be set for each model by loading mask option data (generated by the function option generator) using the ICE command.

9.1.2 External view of LCD board

![Fig. 9.1.2.1 External view of LCD board](image_url)
9.2 Precautions on Using

Follow the precautions described below to ensure that the LCD board is used properly. Note, however, that some functions described here may not be available with some models. For details, refer to the technical manual for each model.

9.2.1 Notes on operations

Always be sure to power off all connected equipment before connecting or disconnecting the cable.

9.2.2 Difference from an actual IC

It is necessary to well know following differences from an actual IC on functions and characteristics. Unless there are considered, successful operation on the S5U1C63000H2 with the LCD board may not be reproduced on the actual IC.

(1) Initialization

In the actual IC, contents of the segment memory are indefinite at system reset and the LCD drive waveform output is also indefinite in response to this. It means that the segment memory and the LCD drive waveform are coincident even though both are indefinite. However, in this board, the segment memory and the LCD drive waveform output are not coincident. Therefore, any initialization routine that surely clears (or sets) the segment memory after the system reset must be installed.

(2) LCD segment RAM (for models that have fixed assignment of LCD segments to memory bits)

In the actual IC, when reading a segment memory address that includes bits not assigned for LCD segment, the non-assigned bits are always read as 0. However, in this board, the non-assigned bits in the segment memory can be read and write as a memory. Therefore, when reading such address, the non-assigned bits in the word (4 bits) must be ignored.

(3) Power supply range in external LCD power mode

When the LCD power is supplied from an external source in the external LCD power mode, following voltage formula must be satisfied. These terminals are located in the connector of the peripheral circuit board.

- For models that use VSS as GND level
  \[ V_{SS} < V_{C1} < V_{C2} < V_{C3} < V_{C4} < V_{C5} \leq V_{DD} \ (= +5 \text{ V}) \]

- For models that use VDD as GND level
  \[ V_{SS} < V_{L5} < V_{L4} < V_{L3} < V_{L2} < V_{L1} \leq V_{DD} \ (= +5 \text{ V}) \]

(4) Drive capability of SEG and COM terminals

The output drive capability of the SEG and COM terminals in this board is higher than those of the actual IC. The S5U1C63000H2 can not be used for evaluation of the electrical characteristics. The system should be design in consideration of the electrical characteristics described on the technical manual of each model.

(5) LCD drive voltage

The LCD drive voltage in this board may differ from that of the actual IC.
9.3 Connection with Target System

Use the connection cables (100-pin/50-pin × 2 flat type, 34-pin flat type) supplied for the connection between the LCD board and target systems.

Fig. 9.3.1 Connection with target system
### Pin layout of connectors

#### CN-4 connectors (100-pin/50-pin × 2 flat type)

<table>
<thead>
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<th>No.</th>
<th>Name</th>
<th>Function</th>
<th>No.</th>
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#### CN-5 connector (34-pin × 2 flat type)

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Note that some pin names are not existed in the actual IC depending on the model.

The COM0–COM7 terminals are available in the both connectors CN4-1 and CN5, either can be used.
9.4 Product Specifications

Following shows the specifications of the LCD board components.

- **LCD board**
  - Dimension: 254 mm (wide) × 144.8 mm (depth) × 13 mm (height) (including screws)
  - Weight: Approx. 220 g
  - Power supply: DC 5 V ±5%, less than 1 A (supplied from S5U1C63000H2 main unit)

- **LCD cable**
  - Onboard connector: KEL8830E-100-170L
    3M3431-5002LCSC
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Telex: 65542 EPSC0 HK

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Telex: 24444 EPSONTB

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