S1C33L05
32-bit Single Chip Microcomputer

● 32-bit S1C33000 RISC Core
● Low Power
● Multiply Accumulation
● Built-in 16K-byte RAM
● 10-bit ADC
● Built-in LCD Controller
● Built-in USB1.1 Function Controller
● Built-in SDRAM Controller

■ DESCRIPTION
The S1C33L05 is a Seiko Epson original 32-bit microcomputer that features high speed, low power consumption, and low-voltage operation. The S1C33L05 consists of an S1C33000 32-bit RISC type CPU as its core, peripheral circuits including a bus control unit, DMA controller, interrupt controller, timers, serial interface with FIFO, A/D converter, a color STN LCD controller that supports 64K color display, SDRAM controller, USB1.1 function controller, sequential ROM interface, MMC (SPI mode) interface and NAND flash interface, and also an embedded RAM. Two oscillation circuits and a PLL are also included, supporting advanced operation, power-saving operation, and high-performance real-time clock functions. The S1C33L05 is ideal for portable products that require high-speed data processing. Especially it is suitable for the application processor embedded in PDAs, electronic dictionary and e-Book readers.

■ FEATURES

● Core CPU
  Seiko Epson original 32-bit RISC CPU S1C33000 built-in
  • Basic instruction set: 105 instructions (16-bit fixed size)
  • Sixteen 32-bit general-purpose register
  • 32-bit ALU and 8-bit shifter
  • Multiplication/division instructions and MAC (multiplication and accumulation) instruction are available
  • 20.83 ns of minimum instruction execution time at 48 MHz operation

● Internal memory
  General-purpose RAM.........................16K bytes (1-cycle-access)
  Video-RAM ........................................40K bytes (usable for general-purpose RAM, 2-cycle-access)

● Internal peripheral circuits
  OSC3 oscillation circuit/PLL ...............When PLL is disabled
  Crystall oscillator 5 MHz min. to 48 MHz max.
  Ceramic oscillator 48 MHz (fixed)
  External clock input 2 MHz min. to 48 MHz max.
  When PLL is enabled
  Crystal oscillator 20 MHz min. to 48 MHz max.
  Ceramic oscillator 48 MHz (fixed)
  External clock input 20 MHz min. to 48 MHz max.
  Generates the main clock for the bus and the CPU.
  The software controllable PLL multiplies the high-speed (OSC3) oscillation clock frequency.
  PLL input clock 10 MHz min. to 24 MHz max.
  PLL output clock 10 MHz min. to 48 MHz max.

  OSC1 oscillation circuit.......................Crystal oscillator or external clock input 32.768 kHz typ.
  Generates the source clock for the real-time clock function, etc.
Timers ....................................................... 8-bit timer 6 channels
16-bit timer 6 channels
Watchdog timer 1 channel (16-bit timer 0’s function)
Clock timer 1 channel (with alarm function)

Serial interface .......................................... 4 channels
Clock-synchronous system, asynchronous system and IrDA 1.0
interface are selectable.
Ch.0 is selectable between a built-in buffer type (a 4-byte receive-
data buffer and a 2-byte transmit-data buffer) and no buffer type.

A/D converter ............................................ 10 bits x 5 channels

LCD controller ........................................... 4 or 8-bit monochrome/color LCD interface
Panels supported
- Single-panel, single drive passive display
- 4/8-bit monochrome LCD interface
- 4/8-bit color LCD interface
Display modes
- 16-bpp mode: 64K colors or 64-level gray scale display
- 12-bpp mode: 4096 colors or 16-level gray scale display
- 8-bpp mode: 256 colors or 64-level gray scale display
- 4-bpp mode: 16 colors or 16-level gray scale display
- 2-bpp mode: 4 colors or 4-level gray scale display
- 1-bpp mode: 2 colors or 2-level gray scale display
* A 256 x 3 x 6-bit Look-Up Table (256K-color palette) is pro-
vided for displaying 256 colors simultaneously. The LUT can
be bypassed to send display data from VRAM directly to the
LCD.
* Gray scale display uses FRM (Frame Rate Modulation) and
dithering.

Resolution (programmable)
Typical resolutions when only the internal VRAM is used:
- 320 x 240 pixels in 4-bpp mode
- 160 x 240 pixels in 8-bpp mode
- 160 x 160 pixels in 12-bpp mode
Typical resolutions when an external VRAM is used via the
UMA:
- 320 x 240 pixels in 8-bpp mode
- 320 x 240 pixels in 16-bpp mode

SDRAM controller ..................................... 48 MHz synchronous clock max.
Supports up to 256M-bit (32MB) SDRAM with 16-bit data width.
16-stage IQB (32-byte Instruction Queue Buffer) and 2-stage
DQB (4-byte Data Queue Buffer) are provided.
Allows LCDC DMA controller to access SDRAM directly as an
external VRAM.

MMC (SPI mode) interface ....................... 1 channel
Supports 1 to 16-bit serial data transfer in master mode.
Compatible with MMC.
NAND flash interface ................................. Generates the #SMWE and #SMRE signals using the BCU signals to interface directly with SmartMedia cards or NAND flash memories. Supports 8/16-bit Nand flash devices. Also the Nand flash booting function and the ECC function when a Nand flash is read/written are supported.

Sequential ROM interface .......................... Supports MX23L12813 (manufactured by Macronix International Co., Ltd.). Generates the SQUALE, SQLALE and #SQRD signals using the BCU signals to interface directly with the sequential mask ROM.

USB1.1 function controller ......................... Endpoint: EP0, EPa, EPb, EPc, EPd (4 channels); FIFO: 1,024 bytes

DMA controller ....................................... High-speed DMA 4 channels
                                                 High-speed DMA Ch. 3 has been reserved for the internal USB1.1 function controller.
                                                 Intelligent DMA 128 channels

Interrupt controller ................................ Possible to invoke DMA
                                                 Input interrupt 10 types (programmable)
                                                 DMA controller interrupt 5 types
                                                 16-bit programmable timer interrupt 12 types
                                                 8-bit programmable timer interrupt 6 types
                                                 Serial interface interrupt 15 types
                                                 A/D converter interrupt 1 type
                                                 Clock timer interrupt 1 type
                                                 LCD controller interrupt 1 type
                                                 SPI interrupt 1 type
                                                 USB function controller interrupt 1 type

General-purpose input and output ports ... Shared with the I/O pins for internal peripheral circuits
                                                 Input port 9 bits (max.)
                                                 I/O port 69 bits (max.)
                                                 * The K54 and K65–K67 pins are not available in the S1C33L05.
                                                 * Two LED direct output (8 mA) ports (P27 and P26) are available.
                                                 * The number of the ports varies depending on the peripheral functions used.

● External bus interface

  BCU (bus control unit) built-in
  • 26-bit address bus (internal 28-bit processing)
  • 16-bit data bus (Data size is selectable from 8 bits and 16 bits in each area.)
  • Little/big-endian memory access; endian type may be set in each area.
  • Memory mapped I/O
  • Chip enable and wait control circuits built-in
  • Supports burst ROM.
Operating conditions and power consumption

Operating voltage ........................................
- Core (VDD) 1.65 V to 1.95 V (1.8 V ±0.15 V)
  (when crystal oscillator is used)
- 1.70 V to 1.90 V (1.8 V ±0.10 V)
  (when ceramic oscillator is used)
- I/O (VDD, AVDD) 2.70 V to 3.60 V
  (when USB is not used)
- 3.00 V to 3.60 V
  (when USB is used)

Operating clock frequency ........................
- CPU 48 MHz max. Note 1
- Bus (BCU) 40 MHz max.
- LCD controller 48 MHz max.
- USB function controller 48 MHz
- SDRAM 48 MHz

Operating temperature ..............................
- -40 to 85°C (when crystal oscillator is used)
- 0 to 70°C (when ceramic oscillator is used)

Power consumption ...................................
- During SLEEP 12 µW typ.
- During HALT 18 mW typ.
  (48 MHz, LCDC and USB not included)
- During execution 42 mW typ. Note 2
  (48 MHz, LCDC and USB not included)
- LCD controller
  - During display 1.8 mW typ.
    (LCDC clock = 8 MHz, 16 bpp, IVRAM mode,
     VDD, LCDC block only)
- USB controller
  - Idle state 14 mW typ.
    (VDD, USB block only)

Supply form

Plastic package ........................................
- QFP21-176pin (24 mm × 24 mm × 1.4 mm, 0.5-mm pitch)

Die form .................................................
- 167-PAD (5.25 mm × 4.85 mm, 100 µm pitch)

Notes: 1. Set the #X2SPD pin to "0" when running the CPU with a 40 MHz or more system clock. Also make sure that the internal bus operating clock frequency does not exceed 40 MHz.

2. The values of power consumption during execution were measured when a test program that consisted of 55% load instructions, 23% arithmetic operation instructions, 1% mac instruction, 12% branch instructions and 9% ext instruction was being continuously executed.
**Fig. 1 S1C33L05 Functional Block Diagram**
## PIN LAYOUT

![Fig. 2 Pin Layout Diagram (QFP21-176pin)](image)

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin name</th>
<th>No.</th>
<th>Pin name</th>
<th>No.</th>
<th>Pin name</th>
<th>No.</th>
<th>Pin name</th>
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**Bold:** The pin (signal) name of a default setup.

Fig. 2 Pin Layout Diagram (QFP21-176pin)
**S1C33L05**

[BASIC EXTERNAL CONNECTION DIAGRAM](#)

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**Fig. 3 Basic External Connection Diagram**

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### Notes:

1. Oscillation characteristics vary depending on conditions (components used, board pattern, etc.). The values in the above table are shown only for reference and not guaranteed. In particular, ceramic oscillation is extremely sensitive to influence of external components and printed-circuit boards. Before using a ceramic resonator, please be sure to contact Murata Manufacturing Co., Ltd. for further information on conditions of use for ceramic resonators. Furthermore, this chip supports only 48-MHz ceramic resonators. Do not use ceramic resonators with any other frequency.

2. Capacitance built into the ceramic resonator

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### Key Components:

- **Crystal resonator**
- **Gate capacitor**
- **Drain capacitor**
- **Feedback resistor**
- **Drain resistor**
- **Resistor**
- **Capacitor**

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### Ceramic Options:

- **Ceramic (CSTCW48M0X11+***

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### S1C33L05

- [The potential of the substrate (back of the chip) is Vss.]