EPSON

# S1C33301

## 32-bit Single Chip Microcomputer

- 32-bit S1C33000 RISC Core
- Low Power Consumption
- Multiply Accumulation
- Built-in 8K-byte RAM
- 10-bit ADC
- 4-ch. SIO
- High-speed DMA, Intelligent DMA

## ■ DESCRIPTION

The S1C33301 is a Seiko Epson original 32-bit microcomputer. It features high speed, low power consumption, and low-voltage operation, and is ideal for portable products that require high-speed data processing. The S1C33301 consists of an S1C33000 32-bit RISC type CPU as its core, peripheral circuits including a bus control unit, DMA controller, interrupt controller, timers, serial interface with FIFO, A/D converter, and SmartMedia interface, and also RAM. A high-speed oscillation circuit, PLL, and a low-speed oscillation circuit are also included, supporting advanced operation, power-saving operation, and high-performance realtime clock functions. Use of the internal MAC (multiplication and accumulation) function in combination with the A/D converter also facilitates the design of systems requiring DSP functions, such as speech recognition and synthesis applications.

## ■ FEATURES

- CMOS LSI 32-bit parallel processing ..... S1C33000 RISC Core
- Main clock ..... 50MHz (Max., up to 33MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 6 channels and 16 bits × 6 channels
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 4 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
  Ch.0 is selectable between a built-in buffer type (a 4 bytes of receive-data buffer and a 2 bytes of transmit-data buffer) and no buffer type.
- SmartMedia interface ..... 1 channel
  Allows direct connection of a SmartMedia
- 10-bit A/D converter ..... Successive approximation type
  8 input channels (QFP15-128pin)
  4 input channels (PFBGA-121pin)
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits (QFP15-128pin)
  9 bits (PFBGA-121pin)
  I/O port : 47 bits (QFP15-128pin)
  44 bits (PFBGA-121pin)
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 40 types

- External bus interface ..... 26-bit address bus, 16-bit data bus, 7 chip enable pins
  SRAM and Burst ROM may be connected directly.
- Shipping form ..... QFP15-128pin, PFBGA-121pin
- Supply voltage ..... Core voltage : 1.65 to 1.95V (1.8±0.15V)
  I/O voltage : 2.70 to 3.60V (3.0/3.3±0.3V)
- Power consumption ..... SLEEP state : 5.4µW (1.8V, 50MHz)
  RUN state : 40mW (1.8V, 50MHz)

## ■ BLOCK DIAGRAM

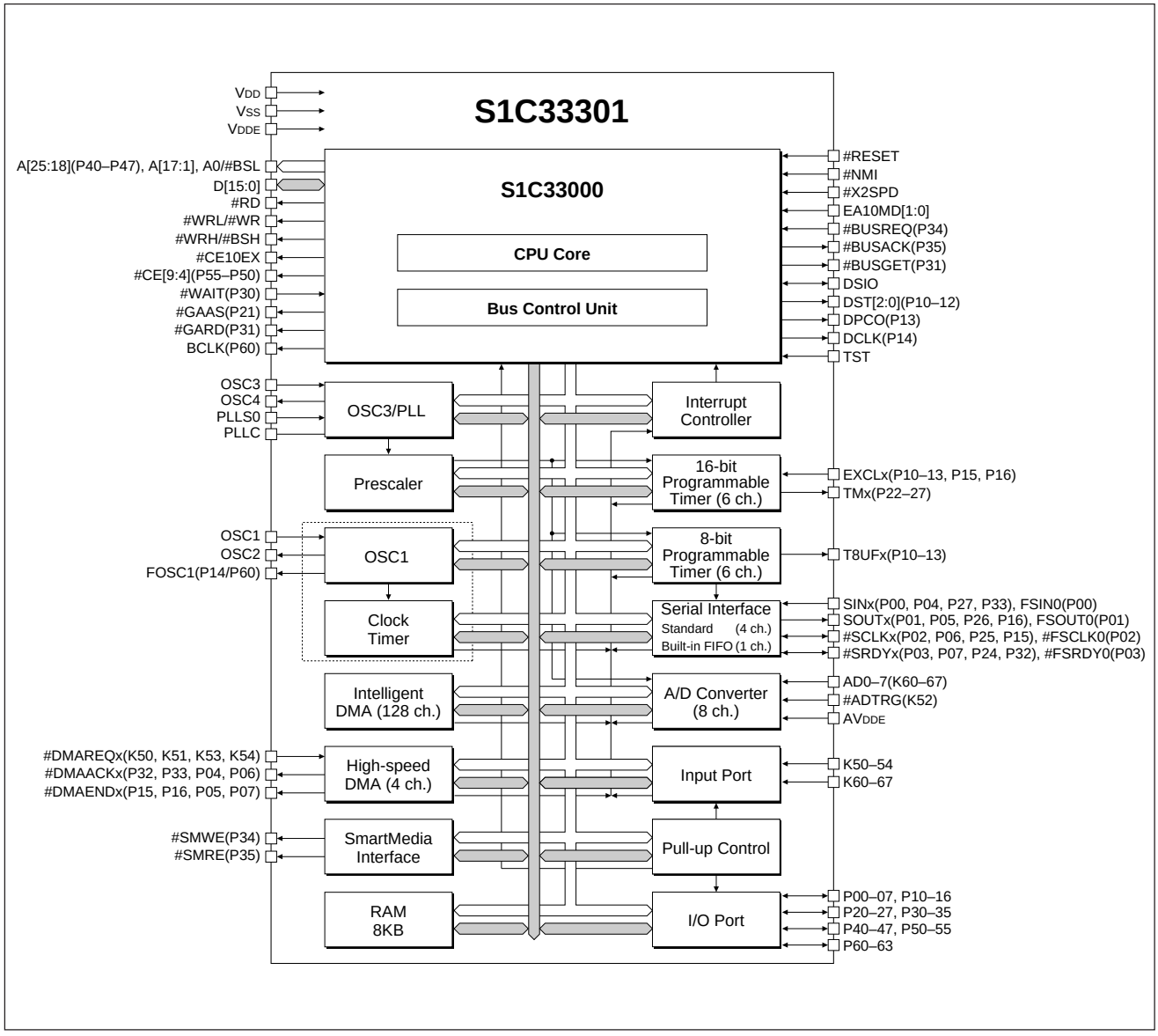
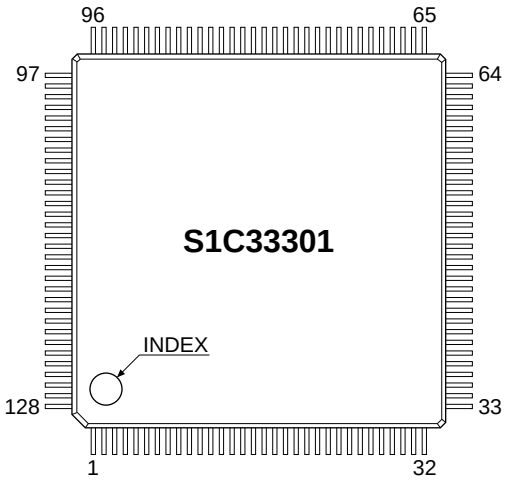



Fig. 1 S1C33301 Functional Block Diagram

## ■ PIN LAYOUT

**QFP15-128pin**



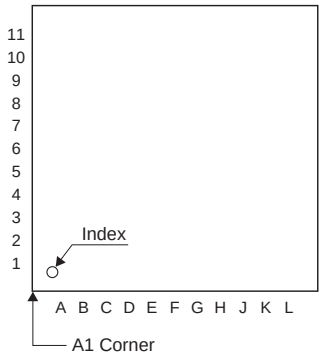

| No. | Pin name | No. | Pin name | No. | Pin name | No. | Pin name |
|---|---|---|---|---|---|---|---|
| 1 | **A0**(#BSL) | 33 | **#RESET** | 65 | **#CE6**(#CE7&8/P52) | 97 | **P24**(TM2/#SRDY2) |
| 2 | **A1** | 34 | **P30**(#WAIT/#CE4&5) | 66 | **#CE7**(#RAS0/#CE13/#RAS2/P53) | 98 | **P25**(TM3/#SCLK2) |
| 3 | **VSS** | 35 | **P31**(#BUSGET/#GARD) | 67 | **#CE8**(#RAS1/#CE14/#RAS3/P54) | 99 | **P26**(TM4/SOUT2) |
| 4 | **A2** | 36 | **P32**(#DMAACK0/#SRDY3) | 68 | **#CE9**(#CE17/#CE17&18/P55) | 100 | **P27**(TM5/SIN2) |
| 5 | **A3** | 37 | **P33**(#DMAACK1/SIN3) | 69 | **VSS** | 101 | **VSS** |
| 6 | **A4** | 38 | **VSS** | 70 | **D8** | 102 | **K50**(#DMAREQ0) |
| 7 | **A5** | 39 | **OSC4** | 71 | **D9** | 103 | **K51**(#DMAREQ1) |
| 8 | **A6** | 40 | **OSC3** | 72 | **D10** | 104 | **K52**(#ADTRG) |
| 9 | **A7** | 41 | **#X2SPD** | 73 | **D11** | 105 | **K53**(#DMAREQ2) |
| 10 | **VDD** | 42 | **P34**(#BUSREQ/#CE6/#SMWE) | 74 | **VDDE** | 106 | **K54**(#DMAREQ3) |
| 11 | **A8** | 43 | **P35**(#BUSACK/#SMRE) | 75 | **D12** | 107 | **DSIO** |
| 12 | **A9** | 44 | **D0** | 76 | **D13** | 108 | **DST0**(P10/EXCL0/T8UF0) |
| 13 | **A10** | 45 | **D1** | 77 | **D14** | 109 | **DST1**(P11/EXCL1/T8UF1) |
| 14 | **A11** | 46 | **VDDE** | 78 | **D15** | 110 | **DST2**(P12/EXCL2/T8UF2) |
| 15 | **A12** | 47 | **D2** | 79 | **A22**(P43) | 111 | **VDDE** |
| 16 | **A13** | 48 | **D3** | 80 | **A23**(P42) | 112 | **DPCO**(P13/EXCL3/T8UF3) |
| 17 | **A14** | 49 | **D4** | 81 | **#LCAS**(P41/A24) | 113 | **DCLK**(P14/FOSC1) |
| 18 | **VDDE** | 50 | **D5** | 82 | **#HCAS**(P40/A25) | 114 | **P15**(EXCL4/#DMAEND0/#SCLK3) |
| 19 | **A15** | 51 | **D6** | 83 | **P00**(SIN0/FSIN0) | 115 | **P16**(EXCL5/#DMAEND1/SOUT3) |
| 20 | **A16** | 52 | **D7** | 84 | **P01**(SOUT0/FSOUT0) | 116 | **VSS** |
| 21 | **A17** | 53 | **VDD** | 85 | **P02**(#SCLK0/#FSCLK0) | 117 | **OSC2** |
| 22 | **A18**(P47) | 54 | **#WRL**(#WR/#WE) | 86 | **P03**(#SRDY0/#FSRDY0) | 118 | **OSC1** |
| 23 | **A19**(P46) | 55 | **#WRH**(#BSH) | 87 | **VDD** | 119 | **VDD** |
| 24 | **A20**(P45) | 56 | **#RD** | 88 | **P04**(SIN1/#DMAACK2) | 120 | **K60**(AD0) |
| 25 | **A21**(P44) | 57 | **#CE10EX**(#CE9&10EX) | 89 | **P05**(SOUT1/#DMAEND2) | 121 | **K61**(AD1) |
| 26 | **#NMI** | 58 | **BCLK**(P60/FOSC1) | 90 | **P06**(#SCLK1/#DMAACK3) | 122 | **K62**(AD2) |
| 27 | **EA10MD0** | 59 | **P61** | 91 | **P07**(#SRDY1/#DMAEND3) | 123 | **K63**(AD3) |
| 28 | **EA10MD1** | 60 | **P62** | 92 | **VSS** | 124 | **K64**(AD4) |
| 29 | **PLLS0** | 61 | **P63** | 93 | **P20**(#DRD) | 125 | **K65**(AD5) |
| 30 | **PLLC** | 62 | **VSS** | 94 | **P21**(#DWE/#GAAS) | 126 | **K66**(AD6) |
| 31 | **VSS** | 63 | **#CE4**(#CE11/#CE11&12/P50) | 95 | **P22**(TM0) | 127 | **K67**(AD7) |
| 32 | **TST** | 64 | **#CE5**(#CE15/#CE15&16/P51) | 96 | **P23**(TM1) | 128 | **AVDDE** |

**Bold**: The terminal (signal) name of a default setup.

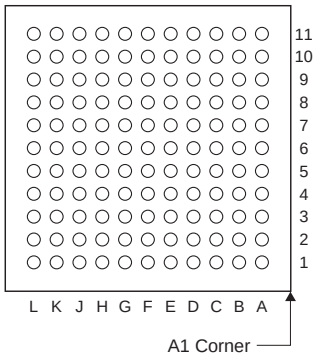
Fig. 2 Pin Layout Diagram (QFP15-128pin)

**PFBGA-121pin**

Top View




Bottom View




| | A | B | C | D | E | F | G | H | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11 | **VSS** | **P23** (TM1) | **P20** (#DRD) | **VDD** | **P01** (SOUT0/ FSOUT0) | **D15** | **D13** | **D10** | **D8** | **#CE7** (#RAS0/#CE13/ #RAS2/P53) | **VSS** |
| 10 | **P25** (TM3/ #SCLK2) | **P24** (TM2/ #SRDY2) | **P21** (#DWE/ #GAAS) | **P05** (SOUT1/ #DMAEND2) | **P02** (#SCLK0/ #FSCLK0) | **A22** (P43) | **VDDE** | **D9** | **#CE8** (#RAS1/ #CE14/ #RAS3/P54) | **#CE6** (#CE7&8/P52) | **#CE5** #CE15/ #CE15&16/ P51) |
| 9 | **K50** (#DMAREQ0) | **P26** (TM4/SOUT2) | **P22** (TM0) | **P06** (#SCLK1/ #DMAACK3) | **P03** (#SRDY0/ #FSRDY0) | **A23** (P42) | **D12** | **D11** | **#CE9** (#CE17/ #CE17&18/ P55) | **#CE4** (#CE11/ #CE11&12/ P50) | **BCLK** (P60/FOSC1) |
| 8 | **K52** (#ADTRG) | **K51** (#DMAREQ1) | **P27** (TM5/SIN2) | **P07** (#SRDY1/ #DMAEND3) | **P04** (SIN1/ #DMAACK2) | **#LCAS** (P41/A24) | **D14** | **#RD** | **#CE10EX** (#CE9&10EX) | **#WRH** (#BSH) | **#WRL** (#WR/#WE) |
| 7 | **DSIO** | **K54** (#DMAREQ3) | **K53** (#DMAREQ2) | **DST0** (P10/EXCL0/ T8UF0) | **VSS** | **#HCAS** (P40/A25) | **D5** | **VSS** | **D7** | **D6** | **VDD** |
| 6 | **VDDE** | **DST1** (P11/EXCL1/ T8UF1) | **DCLK** (P14/FOSC1) | **DPCO** (P13/EXCL3/ T8UF3) | **DST2** (P12/EXCL2/ T8UF2) | **P00** (SIN0/FSIN0) | **D0** | **D1** | **D4** | **D2** | **D3** |
| 5 | **OSC2** | **VSS** | **P16** (EXCL5/ #DMAEND1/ SOUT3) | **P15** (EXCL4/ #DMAEND0/ #SCLK3) | **A10** | **VDDE** | **A19** (P46) | **P34** (#BUSREQ/ #CE6/ #SMWE) | **P35** (#BUSACK/ #SMRE) | **#X2SPD** | **VDDE** |
| 4 | **OSC1** | **K60** (AD0) | **VSS** | **VDD** | **A8** | **A13** | **A18** (P47) | **P30** (#WAIT/ #CE4&5) | **P31** (#BUSGET/ #GARD) | **P33** (#DMAACK1/ SIN3) | **OSC3** |
| 3 | **K61** (AD1) | **K63** (AD3) | **A2** | **A5** | **A6** | **A12** | **A17** | **#NMI** | **#RESET** | **P32** (#DMAACK0/ #SRDY3) | **OSC4** |
| 2 | **AVDDE** | **K62** (AD2) | **A0** (#BSL) | **A3** | **VDD** | **A11** | **A15** | **A21** (P44) | **EA10MD0** | **PLLS0** | **TST** |
| 1 | **VSS** | **A1** | **A4** | **A7** | **A9** | **A14** | **A16** | **A20** (P45) | **EA10MD1** | **PLLC** | **VSS** |

**Bold**: The terminal (signal) name of a default setup.

Fig. 3 Pin Layout Diagram (PFBGA-121pin)

NOTICE:
No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 2003, All right reserved.

**SEIKO EPSON CORPORATION**
ELECTRONIC DEVICES MARKETING DIVISION
**IC Marketing & Engineering Group**

**ED International Marketing Department**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5117

■ EPSON Electronic Devices Website
**http://www.epsondevice.com**

Document code: 404625001
First issue July, 2003
Printed November, 2003 in Japan Ⓛ