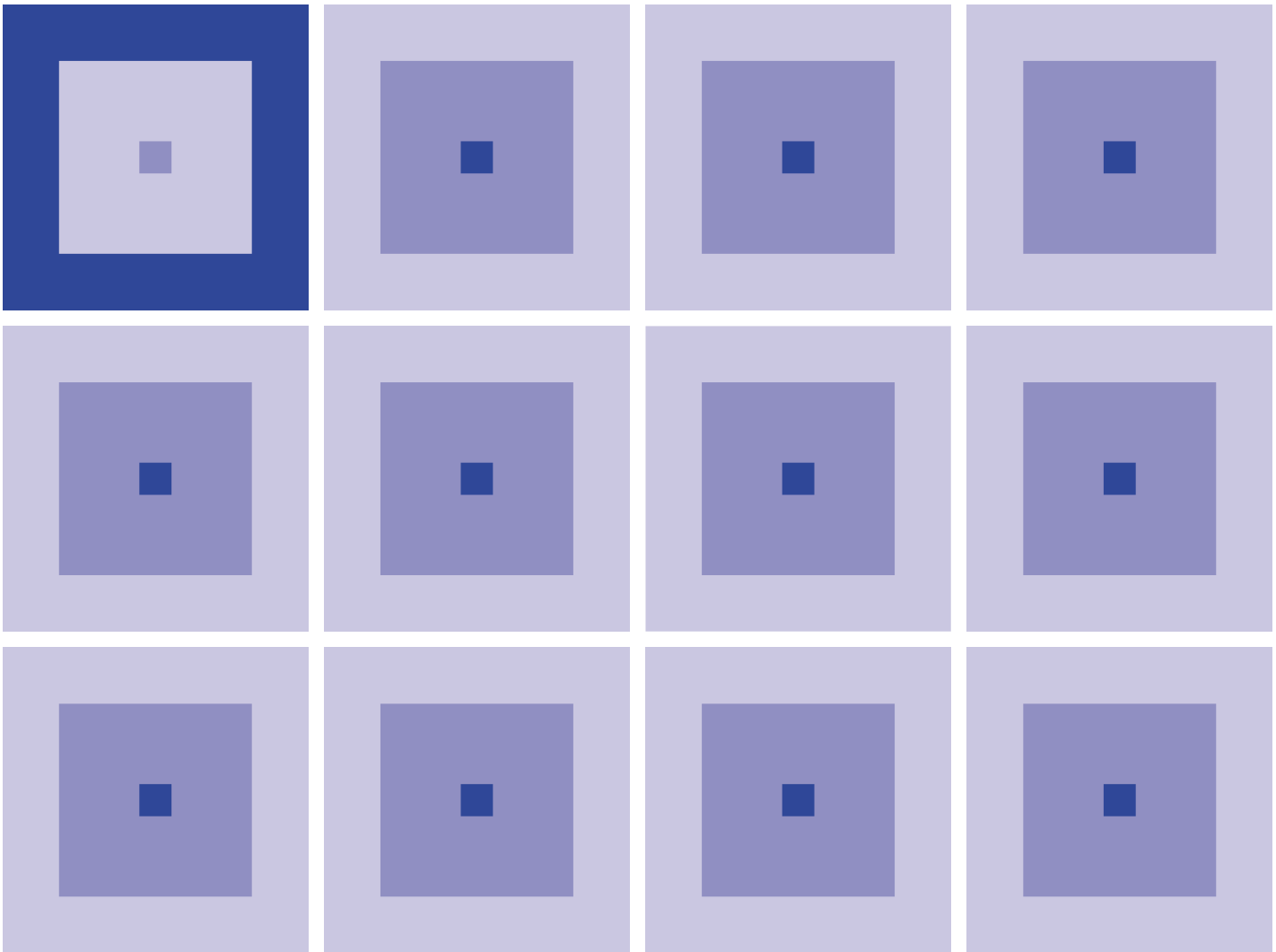
EPSON

EMBEDDED ARRAY

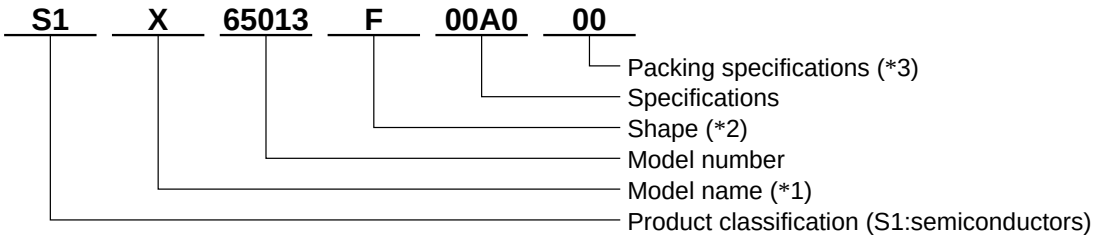
S1X60000 Series
DESIGN GUIDE



SEIKO EPSON CORPORATION

Configuration of product number

●DEVICES



*1: Model name

K	Standard Cell
L	Gate Array
X	Embedded Array

*2: Shape

B	Assembled on board, COB, BGA
C	Plastic DIP
D	Bare Chip
F	Plastic QFP
H	Ceramic DIP
L	Ceramic QFP

M	Plastic SOP
R	TAB–QFP
T	Tape Carrier (TAB)
2	TSOP (Standard Bent)
3	TSOP (Reverse Bent)

*3: Packing Specifications

14th	15th	Packing Specifications
0	0	Besides tape & reel
0	A	TCP BL 2 directions
0	B	Tape & reel Back
0	C	TCP BR 2 directions
0	D	TCP BT 2 directions
0	E	TCP BD 2 directions
0	F	Tape & reel FRONT
0	G	TCP BT 4 directions
0	H	TCP BD 4 directions
0	J	TCP SL 2 directions
0	K	TCP SR 2 directions
0	L	Tape & reel LEFT
0	M	TCP ST 2 directions
0	N	TCP SD 2 directions
0	P	TCP ST 4 directions
0	Q	TCP SD 4 directions
0	R	Tape & reel RIGHT
9	9	Specs not fixed

S1X60000 Series Table of Contents

Chapter 1 Overview

Epson's S1X60000 series consists of ultra high speed, super integrated CMOS type embedded arrays manufactured by the 0.25 µm process.

1.1 Features

1.1.1 Outline of the S1X60000 Series

- Integration 27.4k gates/mm^2
- Operating Speed

◎ Internal gates
107 ps (2.5 V, Typ.), 140 ps (2.0 V, Typ.)
(2 input NAND, F/O = 1, Standard Wiring Load)

◎ Input buffers
F/O = 2, Standard Wiring Load, Typ. Condition

Voltage	Operating Speed			Unit
	X TYPE	XF TYPE		
	3.3 V Input Buffer (XHIBC)	3.3 V Input Buffer (XFHIBC)	5 V Tolerant Fail-Safe Input Buffer (XFHIBB)	
3.3 V/2.5 V	260	260	270	ps

Voltage	Operating Speed			Unit
	X TYPE	XF TYPE		
	2.5 V/2.0 V Input Buffer (XIBC)	2.5 V/2.0 V Input Buffer (XFLIBC)	5 V Tolerant Fail-Safe Input Buffer	
2.5 V	270	270	—	ps
2.0 V	360	360	—	ps

◎ Output buffers
C_L = 15pF, Typ.Condition

Voltage	Operating Speed			Unit
	X TYPE	XF TYPE		
	3.3 V Output Buffer (XHOB3AT)	3.3 V Output Buffer (XFHOB3AT)	5 V Torelant Fail-Safe Output Buffer (XFHOBF3AT)	
3.3 V/2.5 V	1.5	1.5	1.9	ns

Voltage	Operating Speed			Unit
	X TYPE	XF TYPE		
	2.5 V/2.0 V Output Buffer (XOB3AT)	2.5 V/2.0 V Output Buffer (XFLOB3AT)	5 V Torelant Fail-Safe Output Buffer	
2.5 V	1.6	1.6	—	ns
2.0 V	2.3	2.3	—	ns

- Process 0.25 µm, 3/4/5 layered metalization
- I/F Levels CMOS LVTTL compatible
- Input Modes CMOS, LVTTL, CMOS Schmitt, LVTTL Schmitt,
  PCI-3 V, Gated input, Fail-Safe input
  5 V Tolerant Fail-Safe Input (XF Type only)
  May be provided with internal pull-up and pull-down resistors (2 resistance values for each)
- Output Modes Normal, 3-state, Bi-directional, and Fail-Safe outputs, PCI-3 V, 5 V Tolerant Fail-Safe output (XF Type only)
- Drive Output I_{OL} = 0.1, 1, 3, 6 or 12 mA selectable (HV_{DD} = 3.3 V)
  I_{OL} = 0.1, 3, 6, or 9 mA selectable (V_{DD} or LV_{DD} = 2.5 V)
  I_{OL} = 0.05, 0.3, 1, 2, or 3 mA selectable (V_{DD} or LV_{DD} = 2.0 V)
- Memory
  ◎ Basic Cell type RAM
  Asynchronous, 1 port; Asynchronous, 2 ports
  Synchronous, 1 port; Synchronous, 2 ports

  ◎ Standard type RAM
  Synchronous, 1 port; Synchronous, dual ports

  ◎ High Density type RAM
  Synchronous, 1 port

  ◎ ROM
  Synchronous
- Built-in level shifter for operation with dual supply voltages
  Internal logic: Operates with low voltage
  Input/output buffers: Can be interfaced with high and low voltages

1.1.2 Internal Structure of the S1X60000 Series

The S1X60000 series is constructed with an MSI cell area and an input/output buffer circuit area, as shown in Figure 1-1.

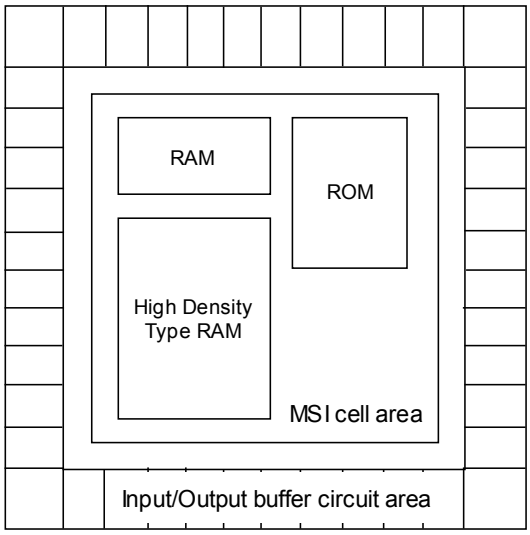


Figure 1-1 Outline Structure of the S1X60000 Series

Various MSI cells and memory blocks can be located in the MSI cell area, depending on the desired circuit. These cells can be interconnected in order to implement the desired circuit. The input/output buffer area contains input buffers, output buffers, bi-directional buffers, and power supply cells. In this area, signals are exchanged between external circuits and the units of the S1X60000 series.

1.1.3 Structure and Types of MSIs

The S1X60000 series is available in Basic Cell type MSI for embedded arrays.

Memory is also available in various types in addition to the Basic Cell type RAM. These include a highly integrated Cell Based type RAM (with 1 port, dual ports, or high density 1 port) and a ROM. The most suitable memory type can be selected in accordance with customer needs.

For details on MSI cell types, refer to Chapter 3, “MSI Cells.” For details on memory, refer to Chapter 6, “Memory Block.”

1.1.4 Structure of 5 V Tolerant Fail-Safe Cells

The 5 V tolerant Fail-Safe cells of the S1X60000 series allow 5.0 V interfacing without requiring a dedicated power supply.

1.1.5 Structure and Types of Input/Output Buffers

The S1X60000 series has two available types of input/output buffers: standard type input/output buffers (X type) and 5 V tolerant Fail-Safe input/output buffers (XF type). Therefore, customers can choose the type that best suits their system specifications. (Note that combined use of the X and XF types is not allowed.)
For details about input/output buffers, see Chapter 4, “Types of Input/Output Buffers and Their Use (X Type),” and Chapter 5, “Types of Input/Output Buffers and Their Use (XF Type).”

1.2 Electrical Characteristics and Specifications

1.2.1 When Using Standard type Input/Output Buffers (X Type)

Table 1-1 Absolute Maximum Ratings (for a Single Power Supply)

(V_{SS} = 0 [V])

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.3 to +3.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.5[*1]	V
Output Voltage	V_O	-0.3 to V_{DD} + 0.5[*1]	V
Output Current/Pin	I_{OUT}	±30	mA
Storage Temperature	T_{stg}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

Table 1-2 Absolute Maximum Ratings (for Dual Power Supplies)

(V_{SS} = 0 [V])

Parameter	Symbol	Limits	Unit
Power Supply Voltage	HV_{DD}[*3]	-0.3 to +4.0	V
	LV_{DD}[*3]	-0.3 to +3.0	V
Input Voltage	HV_I	-0.3 to HV_{DD} + 0.5[*1]	V
	LV_I	-0.3 to LV_{DD} + 0.5[*2]	V
Output Voltage	HV_O	-0.3 to HV_{DD} + 0.5[*1]	V
	LV_O	-0.3 to LV_{DD} + 0.5[*2]	V
Output Current/Pin	I_{OUT}	±30	mA
Storage Temperature	T_{stg}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

*3: $HV_{DD} \geq LV_{DD}$

Table 1-3 Recommended Operating Conditions (for a Single Power Supply at V_{DD} = 2.5 V)

(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	2.30	2.50	2.70	V
Input Voltage	V_I	-0.3	—	V_{DD} + 0.3 *1	V
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input Rising Time *4	t_{ri}	—	—	50	ns
Normal Input Falling Time *4	t_{fa}	—	—	50	ns
Schmitt Input Rising Time *4	t_{ri}	—	—	5	ms
Schmitt Input Falling Time *4	t_{fa}	—	—	5	ms

Notes *1: Possible to use up to 3.9 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

*2: The ambient temperature range is recommended for T_j = 0 to +85 [°C].

*3: The ambient temperature range is recommended for T_j = -40 to +125 [°C].

*4: This is the finite time during which power supply voltage changes from 10% to 90% or vice versa.

Table 1-4 Recommended Operating Conditions (for a Single Power Supply at V_{DD} = 2.0 V)

(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	1.80	2.00	2.20	V
Input Voltage	V_I	-0.3	—	V_{DD} + 0.3 *1	V
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input Rising Time *4	t_{ri}	—	—	100	ns
Normal Input Falling Time *4	t_{fa}	—	—	100	ns
Schmitt Input Rising Time *4	t_{ri}	—	—	10	ms
Schmitt Input Falling Time *4	t_{fa}	—	—	10	ms

Notes *1: Possible to use up to 3.9 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

*2: The ambient temperature range is recommended for T_j = 0 to +85 [°C].

*3: The ambient temperature range is recommended for T_j = -40 to +125 [°C].

*4: This is the finite time during which power supply voltage changes from 10% to 90% or vice versa.

Table 1-5 Recommended Operating Conditions (for Dual Power Supplies)

(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	2.30	2.50	2.70	V
Input Voltage	HV_I	-0.3	—	HV_{DD} + 0.3 *1	V
	LV_I	-0.3	—	LV_{DD} + 0.3 *2	V
Ambient Temperature	T_a	0 -40	25 25	70 *3 85 *4	°C
Normal Input Rising Time *5	t_{ri}	—	—	50	ns
Normal Input Falling Time *5	t_{fa}	—	—	50	ns
Schmitt Input Rising Time *5	t_{ri}	—	—	5	ms
Schmitt Input Falling Time *5	t_{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.9 V of N channel open drain bi-directional buffers and input buffers.
*2: Possible to use up to 3.9 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.
*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].
*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].
*5: This is the finite time during which power supply voltage changes from 10% to 90% or vice versa.

Table 1-6 Recommended Operating Conditions (for Dual Power Supplies)

(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	1.80	2.00	2.20	V
Input Voltage	HV_I	-0.3	—	HV_{DD} + 0.3 *1	V
	LV_I	-0.3	—	LV_{DD} + 0.3 *2	V
Ambient Temperature	T_a	0 -40	25 25	70 *3 85 *4	°C
Normal Input Rising Time *5	Ht_{ri}	—	—	50	ns
	Ht_{ra}	—	—	100	
Normal Input Falling Time *5	Ht_{ri}	—	—	50	ns
	Ht_{ra}	—	—	100	
Schmitt Input Rising Time *5	Ht_{ri}	—	—	5	ms
	Ht_{ra}	—	—	10	
Schmitt Input Falling Time *5	Ht_{ri}	—	—	5	ms
	Ht_{ra}	—	—	10	

Notes *1: Possible to use up to 3.9 V of N channel open drain bi-directional buffers and input buffers.
*2: Possible to use up to 3.9 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.
*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].
*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].
*5: This is the finite time during which power supply voltage changes from 10% to 90% or vice versa.

Table 1-7 Electrical Characteristics

(HV_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1 mA (Type S), -1 mA (Type M), -3 mA (Type 1), -6 mA (Type 2), -12 mA (Type 3) HV_{DD} = Min.		HV_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA (Type S), 4 mA (Type M), 3 mA (Type 1), 6 mA (Type 2), 12 mA (Type 3) HV_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, HV_{DD} = Max.		2.2	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, HV_{DD} = Min.		—	—	0.8	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		1.4	—	2.7	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.3	—	—	V
High Level Input Voltage	V_{IH2}	LVTTL Level, HV_{DD} = Max		2.0	—	—	V
Low Level Input Voltage	V_{IL2}	LVTTL Level, HV_{DD} = Min		—	—	0.8	V
High Level Input Voltage	V_{T2+}	LVTTL Schmitt		1.1	—	2.4	V
Low Level Input Voltage	V_{T2-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H2}	LVTTL Schmitt		0.1	—	—	V
High Level Input Voltage*2	V_{IH3}	PCI Level, HV_{DD} = Max.		1.8	—	—	V
Low Level Input Voltage*2	V_{IL3}	PCI Level, HV_{DD} = Min.		—	—	0.9	V
Pull-up Resistance	P_{PU}	V_I = 0V	Type 1	30	60	(120)*1 144	kΩ
			Type 2	60	120	(240)*1 288	kΩ
Pull-down Resistance	P_{PD}	V_I = HV_{DD}	Type 1	30	60	(120)*1 144	kΩ
			Type 2	60	120	(240)*1 288	kΩ
High Level Output Current*2	I_{OH3}	PCI Response	V_{OH} = 0.90 V, HV_{DD} = Min. V_{OH} = 2.52 V, HV_{DD} = Max.	-36 —	— —	— -115	mA
Low Level Output Current*2	I_{OL3}	PCI Response	V_{OL} = 1.80 V, HV_{DD} = Min. V_{OL} = 0.65 V, HV_{DD} = Max.	48 —	— —	— 137	mA
High Level Maintenance Current	I_{BHH}	Bus Hold Response	V_{IN} = 2.0 V HV_{DD} = Min.	—	—	-20	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response	V_{IN} = 0.8 V HV_{DD} = Min.	—	—	17	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response	V_{IN} = 0.8 V HV_{DD} = Max.	-350	—	—	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response	V_{IN} = 2.0 V HV_{DD} = Max.	210	—	—	µA
Input Terminal Capacitance	C_I	f = 1 MHz, HV_{DD} = 0 V		—	—	10	pF
Output Terminal Capacitance	C_O	f = 1 MHz, HV_{DD} = 0 V		—	—	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, HV_{DD} = 0 V		—	—	10	pF

Notes *1: The value enclosed in ( ) indicates a resistance value when T_a = 0 to +70°C.
*2: Compliant with PCI Standard Rev. 2.2

Table 1-8 Electrical Characteristics

(V_{DD} or LV_{DD} = 2.5 V ± 0.2 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1 mA (Type S), -1 mA (Type M), -3 mA (Type 1), -6 mA (Type 2), -9 mA (Type 3) V_{DD} = Min.		V_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1 mA (Type S), 1 mA (Type M), 3 mA (Type 1), 6 mA (Type 2), 9 mA (Type 3) V_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		1.7	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		—	—	0.7	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.8	—	1.9	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.5	—	1.3	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.1	—	—	V
Pull-up Resistance	P_{PU}	V_I = 0 V	Type 1	20	50	(100)*1 120	kΩ
			Type 2	40	100	(200)*1 240	kΩ
Pull-down Resistance	P_{PD}	V_I = HV_{DD}	Type 1	20	50	(100)*1 120	kΩ
			Type 2	40	100	(200)*1 240	kΩ
High Level Maintenance Current	I_{BHH}	Bus Hold Response	V_{IN} = 1.7 V V_{DD} = Min.	—	—	-5	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response	V_{IN} = 0.5 V V_{DD} = Min.	—	—	5	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response	V_{IN} = 0.5 V V_{DD} = Max.	-280	—	—	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response	V_{IN} = 1.7 V V_{DD} = Max.	170	—	—	µA
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF

Note *1: The value enclosed in ( ) indicates a resistance value when T_a = 0 to +70°C.

Table 1-9 Electrical Characteristics

(V_{DD} or LV_{DD} = 2.0 V ± 0.2 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.05 mA (Type S), -0.3 mA (Type M), -1 mA (Type 1), -2 mA (Type 2), -3 mA (Type 3) V_{DD} = Min.		V_{DD} -0.2	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.05 mA (Type S), 0.3 mA (Type M), 1 mA (Type 1), 2 mA (Type 2), 4 mA (Type 3) V_{DD} = Min.		—	—	0.2	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		1.6	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		—	—	0.3	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.4	—	1.6	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.3	—	1.4	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0	—	—	V
Pull-up Resistance	P_{PU}	V_I = 0 V	Type 1	30	70	200	kΩ
			Type 2	60	140	400	kΩ
Pull-down Resistance	P_{PD}	V_I = V_{DD}	Type 1	30	70	200	kΩ
			Type 2	60	140	400	kΩ
High Level Maintenance Current	I_{BHH}	Bus Hold Response	V_{IN} = 1.6 V V_{DD} = Min.	—	—	-2	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response	V_{IN} = 0.3 V V_{DD} = Min.	—	—	2	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response	V_{IN} = 0.3 V V_{DD} = Max.	-100	—	—	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response	V_{IN} = 1.6 V V_{DD} = Max.	100	—	—	µA
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF

1.2.2 When Using 5 V Tolerant Fail-Safe Input/Output Buffers (XF Type)

Table 1-10 Absolute Maximum Ratings (for Dual Power Supplies)

(V_{SS} = 0 [V])

Parameter	Symbol	Limits	Unit
Power Supply Voltage	HV_{DD} *3	-0.3 to +4.0	V
	LV_{DD} *3	-0.3 to +2.5	V
Input Voltage	HV_I	-0.3 to HV_{DD} + 0.5 *1	V
	LV_I	-0.3 to LV_{DD} + 0.5 *2	V
Output Voltage	HV_o	-0.3 to HV_{DD} + 0.5 *1	V
	LV_o	-0.3 to LV_{DD} + 0.5 *2	V
Output Current/Pin	I_{out}	±30	mA
Storage Temperature	T_{stg}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers and input buffers, and -0.3 V to 5.5 V of 5 V Tolerant Fail-Safe cells.

*2: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

*3: $HV_{DD} \geq LV_{DD}$

Table 1-11 Recommended Operating Conditions (for Dual Power Supplies)

(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	2.30	2.50	2.70	V
Input Voltage	HV_I	-0.3	—	HV_{DD} + 0.3 *1	V
	LV_I	-0.3	—	LV_{DD} + 0.3 *2	V
Ambient Temperature	T_a	0 -40	25 25	70 *3 85 *4	°C
Normal Input Rising Time *5	t_{ri}	—	—	50	ns
Normal Input Falling Time *5	t_{fa}	—	—	50	ns
Schmitt Input Rising Time *5	t_{ri}	—	—	5	ms
Schmitt Input Falling Time *5	t_{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.9 V of N channel open drain bi-directional buffers and input buffers and up to 5.5 V of 5 V Tolerant Fail-Safe cells.

*2: Possible to use up to 3.9 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

*5: This is the finite time during which power supply voltage changes from 10% to 90% or vice versa.

Table 1-12 Recommended Operating Conditions (for Dual Power Supplies)

(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	1.80	2.00	2.20	V
Input Voltage	HV_I	-0.3	—	HV_{DD} + 0.3 *1	V
	LV_I	-0.3	—	LV_{DD} + 0.3 *2	V
Ambient Temperature	T_a	0 -40	25 25	70 *3 85 *4	°C °C
Normal Input Rising Time *5	t_{ri}	—	—	50	ns
Normal Input Falling Time *5	t_{ra}	—	—	50	ns
Schmitt Input Rising Time *5	t_{ri}	—	—	5	ms
Schmitt Input Falling Time *5	t_{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.9 V of N channel open drain bi-directional buffers and input buffers and up to 5.5 V of 5 V Tolerant Fail-Safe cells.

*2: Possible to use up to 3.9 V of N channel open drain bi-directional buffers, input buffers, and Fail-Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

*5: This is the finite time during which power supply voltage changes from 10% to 90% or vice versa.

Table 1-13 Electrical Characteristics (1/2)

(HV_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
Input Leakage Current (5 V Tolerant Fail-Safe Cell)	I_{LIF}	V_{IN} = 5.5 V		-10	—	10	µA
Off State Leakage Current (5 V Tolerant Fail-Safe Cell)	I_{OZF}	V_{IN} = 5.5 V		-10	—	10	µA
High Level Output Voltage (Ordinary Cell)	V_{OH1}	I_{OH} = -0.1 mA (Type S), -1 mA (Type M), -3 mA (Type 1), -6 mA (Type 2), -12 mA (Type 3) HV_{DD} = Min.		HV_{DD} -0.4	—	—	V
High Level Output Voltage (5 V Tolerant Fail-Safe Cell)	V_{OH2}	I_{OH} = -3 mA (Type 1), -6 mA (Type 2), -12 mA (Type 3) HV_{DD} = Min.		HV_{DD} -1.0	—	—	V
Low Level Output Voltage	V_{OL1}	I_{OL} = -0.1 mA (Type S), -1 mA (Type M), -3 mA (Type 1), -6 mA (Type 2), -12 mA (Type 3) HV_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, HV_{DD} = Max.		2.2	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, HV_{DD} = Min.		—	—	0.8	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		1.4	—	2.7	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.3	—	—	V
High Level Input Voltage	V_{IH2}	LVTTL Level, HV_{DD} = Max.		2.0	—	—	V
Low Level Input Voltage	V_{IL2}	LVTTL Level, HV_{DD} = Min.		—	—	0.8	V
High Level Input Voltage	V_{T2+}	LVTTL Schmitt		1.1	—	2.4	V
Low Level Input Voltage	V_{T2-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H2}	LVTTL Schmitt		0.1	—	—	V
High Level Input Voltage*2	V_{IH3}	PCI Level, HV_{DD} = Max.		1.8	—	—	V
Low Level Input Voltage*2	V_{IL3}	PCI Level, HV_{DD} = Min.		—	—	0.9	V
Pull-up Resistance	P_{PU}	V_I = 0 V	TYPE 1	30	60	(120)*1 144	kΩ
			TYPE 2	60	120	(240)*1 288	kΩ
Pull-down Resistance	P_{PD}	V_I = HV_{DD}	TYPE 1	30	60	(120)*1 144	kΩ
			TYPE 2	60	120	(240)*1 288	kΩ

Note *1: The value enclosed in ( ) indicates a resistance value when T_a = 0 to +70°C.

*2: Compliant with PCI Standard Rev. 2.2

Table 1-13 Electrical Characteristics (2/2)

(HV_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Level Output Voltage *2	I_{OH3}	PCI V_N = 0.90 V, HV_{DD} = Min.	-36	—	—	mA
		Response V_{OH} = 2.52 V, HV_{DD} = Max.	—	—	-115	mA
Low Level Output Voltage *2	I_{OL3}	PCI V_{OL} = 1.80 V, HV_{DD} = Min.	48	—	—	mA
		Response V_{OL} = 0.65 V, HV_{DD} = Max.	—	—	-137	mA
High Level Maintenance Current	I_{BHH}	Bus Hold / Response V_{IN} = 2.0 V, HV_{DD} = Min.	—	—	-20	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold / Response V_{IN} = 0.8 V, HV_{DD} = Min.	—	—	17	µA
High Level Reversal Current	I_{BHHO}	Bus Hold / Response V_{IN} = 0.8 V, HV_{DD} = Max.	-350	—	—	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold / Response V_{IN} = 2.0 V, HV_{DD} = Max.	210	—	—	µA
Input Terminal Capacitance	C_I	f = 1 MHz, HV_{DD} = 0 V	—	—	12	pF
Output Terminal Capacitance	C_o	f = 1 MHz, HV_{DD} = 0 V	—	—	12	pF
Input/Output Terminal Capacitance	C_{Io}	f = 1 MHz, HV_{DD} = 0 V	—	—	12	pF

Note *2: Compliant with PCI Standard Rev. 2.2

Table 1-14 Electrical Characteristics

(LV_{DD} = 2.5 V ± 0.2 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
High Level Output Voltage	V_{OH1}	I_{OH} = -0.1 mA (Type S), -1 mA (Type M), -3 mA (Type 1), -6 mA (Type 2), -9 mA (Type 3) LV_{DD} = Min.		LV_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL1}	I_{OL} = 0.1 mA (Type S), 1 mA (Type M), 3 mA (Type 1), 6 mA (Type 2), 9 mA (Type 3) V_{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		1.7	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		—	—	0.7	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.8	—	1.9	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.5	—	1.3	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.1	—	—	V
Pull-up Resistance	P_{PU}	V_I = 0 V	TYPE 1	20	50	(100)*1 120	kΩ
			TYPE 2	40	100	(200)*1 240	kΩ
Pull-down Resistance	P_{PD}	V_I = LV_{DD}	TYPE 1	20	50	(100)*1 120	kΩ
			TYPE 2	40	100	(200)*1 240	kΩ
High Level Maintenance Current	I_{BHH}	Bus Hold Response	V_{IN} = 1.7 V V_{DD} = Min.	—	—	-5	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response	V_{IN} = 0.7 V V_{DD} = Min.	—	—	5	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response	V_{IN} = 0.5 V V_{DD} = Max.	-280	—	—	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response	V_{IN} = 1.7 V V_{DD} = Max.	170	—	—	µA
Input Terminal Capacitance	C_I	f = 1 MHz, LV_{DD} = 0 V		—	—	12	pF
Output Terminal Capacitance	C_o	f = 1 MHz, LV_{DD} = 0 V		—	—	12	pF
Input/Output Terminal Capacitance	C_{Io}	f = 1 MHz, LV_{DD} = 0 V		—	—	12	pF

Note *1: The value enclosed in ( ) indicates a resistance value when T_a = 0 to +70°C.

Table 1-15 Electrical Characteristics

(LV_{DD} = 2.0 V ± 0.2 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-5	—	5	µA
Off State Leakage Current	I_{OZ}	—		-5	—	5	µA
High Level Output Voltage	V_{OH1}	I_{OH} = -0.05 mA (Type S), -0.3 mA (Type M), -1 mA (Type 1), -2 mA (Type 2), -3 mA (Type 3) LV_{DD} = Min.		LV_{DD} -0.2	—	—	V
Low Level Output Voltage	V_{OL1}	I_{OL} = 0.05 mA (Type S), 0.3 mA (Type M), 1 mA (Type 1), 2 mA (Type 2), 3 mA (Type 3) LV_{DD} = Min.		—	—	0.2	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max.		1.6	—	—	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min.		—	—	0.3	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.4	—	1.6	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.3	—	1.4	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0	—	—	V
Pull-up Resistance	P_{PU}	V_I = 0 V	TYPE 1	30	70	200	kΩ
			TYPE 2	60	140	400	kΩ
Pull-down Resistance	P_{PD}	V_I = LV_{DD}	TYPE 1	30	70	200	kΩ
			TYPE 2	60	140	400	kΩ
High Level Maintenance Current	I_{BHH}	Bus Hold Response	V_{IN} = 1.6 V LV_{DD} = Min.	—	—	-2	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response	V_{IN} = 0.3 V LV_{DD} = Min.	—	—	2	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response	V_{IN} = 0.3 V LV_{DD} = Max.	-100	—	—	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response	V_{IN} = 1.6 V LV_{DD} = Max.	100	—	—	µA
Input Terminal Capacitance	C_I	f = 1 MHz, LV_{DD} = 0 V		—	—	12	pF
Output Terminal Capacitance	C_o	f = 1 MHz, LV_{DD} = 0 V		—	—	12	pF
Input/Output Terminal Capacitance	C_{Io}	f = 1 MHz, LV_{DD} = 0 V		—	—	12	pF

1.3 Estimating the Quiescent Current

The quiescent current for cells in the S1X60000 series can be roughly estimated using the equation shown below.

When calculating the quiescent current, please assume ambient temperature (T_a) = chip temperature (T_j).

The quiescent current depends on the off current of each transistor. Because the quiescent current for the entire chip cannot easily be calculated simultaneously, divide the chip into several blocks in the calculation of the quiescent current, and use the sum total of all blocks as the chip's quiescent current.

$$I_{DDS} (T_j = 85°C) = I_{QBC} + I_{QBM} + I_{QIO}$$

1.3.1 Quiescent Current in the Random Logic Part (I_{QBC})

Table 1-16 lists the quiescent current per 1K gate in the S1X60000 series.

Table 1-16 Quiescent Current per 1K Gate (T_j = 85°C)

	V_{DD} = 2.70 V	V_{DD} = 2.20 V	Unit
I_{QBC}	7.94×10^{-7}	6.35×10^{-7}	A

1.3.2 Quiescent Current of Basic Cell Type RAM (I_{QBM})

The quiescent current values of the primary Basic Cell type RAMs in the S1X60000 series are listed in Table 1-17. (To find quiescent current when V_{DD} = 2.20 V and T_j = 85°C, multiply the values shown below by 0.8.)

(For the quiescent current values of RAMs not listed here, use the quiescent current value of the RAM that is closest in structure to those RAMs. If more detailed information on quiescent current values is required, please contact the sales division of Epson.)

Table 1-17 Quiescent Current Values of Basic Cell Type RAM
(Common to 1 port RAM and 2 port RAM, V_{DD} = 2.70 V, T_j = 85°C)

- Asynchronous RAM

	64 Word	128 Word	256 Word	512 Word	Unit
8 Bit	2.19×10^{-6}	3.73×10^{-6}	6.82×10^{-6}	12.99×10^{-6}	A
16 Bit	3.08×10^{-6}	5.24×10^{-6}	9.54×10^{-6}	18.16×10^{-6}	A
32 Bit	4.87×10^{-6}	8.25×10^{-6}	14.99×10^{-6}	28.48×10^{-6}	A
64 Bit	8.46×10^{-6}	14.27×10^{-6}	25.89×10^{-6}	49.14×10^{-6}	A

- Synchronous RAM

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	2.19×10^{-6}	3.73×10^{-6}	5.27×10^{-6}	6.82×10^{-6}	A
16 Bit	3.08×10^{-6}	5.24×10^{-6}	7.39×10^{-6}	9.54×10^{-6}	A
24 Bit	3.98×10^{-6}	6.74×10^{-6}	9.51×10^{-6}	12.27×10^{-6}	A
32 Bit	4.87×10^{-6}	8.25×10^{-6}	11.62×10^{-6}	14.99×10^{-6}	A

1.3.3 Quiescent Current of Input/Output Buffers (I_{QIO})

The quiescent current values flowing in input/output buffers can be roughly estimated by using the values listed in Table 1-18 for the calculation formula shown on the next page.

(Make sure the input signals for the input and bi-directional buffers are fixed to V_{SS} or V_{DD} (LV_{DD} or HV_{DD}). If buffers with pull-up and pull-down resistors have been selected, leave the pins open.)

For systems with dual power supplies, calculate the quiescent current for the H- and L-voltage buffers separately.

Note: When connecting V_{DD} (LV_{DD} or HV_{DD}) to the NC pin, be sure to add the number of NC pins (as power supply cells) to the number of input/output cells.

Table 1-18 Quiescent Current Value per Input/Output Buffer (T_j = 85° C)

	Quiescent Current Value	Unit
V_{DD} = 3.60V	200×10^{-9}	A
V_{DD} = 2.70V	50×10^{-9}	A
V_{DD} = 2.20V	45×10^{-9}	A

Quiescent current value of input / output buffer = (values in Table 1-18)
× (number of output cells + number of bi-directional cells
+ number of V_{DD} (HV_{DD} or LV_{DD}) power supply cells)

Calculation example: Find the quiescent current value for the following case.

- Power supply voltage: HV_{DD} / LV_{DD} = 3.3 V / 2.5 V
- I/O cells

V_{SS}:	12
HV_{DD}:	12
LV_{DD}:	12
H-voltage input cells:	30
H-voltage output cells:	40
H-voltage bi-directional cells:	60
L-voltage input cells:	30
L-voltage output cells:	20
L-voltage bi-directional cells:	40

- Basic Cell type 2 port RAM: 256 words × 16 bits, 4 pcs. (Synchronous RAM)
  128 words × 8 bits, 6 pcs. (Synchronous RAM)
- Cell Based Logic: 1240k gates

Because this is a dual power supply system, first find the quiescent current for the LV_{DD} system.

From Table 1-16, the quiescent current value of the Cell-Based Logic is

$I_{QBC} = 7.94 \times 10^{-7} \times 1240 = 984.56 \times 10^{-6}$ [A] (V_{DD} = 2.7 V, T_j = 85°C)

Next, find the quiescent current value of the Basic Cell type RAMs. From Table 1-17, the quiescent current value per piece of RAM is

256 Word × 16 Bit ... 9.54×10^{-6} [A]

128 Word × 8 Bit ... 3.73×10^{-6} [A]

Therefore, the quiescent current value of the Basic Cell type RAMs is

$$I_{QBM} = (9.54 \times 10^{-6} \times 4) + (3.73 \times 10^{-6} \times 6)$$
$$= 38.16 \times 10^{-6} + 22.38 \times 10^{-6}$$
$$= 60.54 \times 10^{-6} \text{ [A]} \quad (V_{DD} = 2.7 \text{ V}, T_j = 85°C)$$

Next, find the quiescent current value of the input/output buffers using the equation for quiescent current values shown above.

$I_{QIO} = 50 \times 10^{-9} \times (20 + 40 + 12) = 3.60 \times 10^{-6}$ [A]

From the quiescent current values obtained thus far, find the quiescent current value of the LV_{DD} system.

$$I_Q (LV_{DD}) = I_{QBC} + I_{QBM} + I_{QIO}$$
$$= 984.56 \times 10^{-6} + 60.54 \times 10^{-6} + 3.6 \times 10^{-6}$$
$$= 1048.7 \times 10^{-6} \text{ [A]}$$

Next, find the quiescent current value of the HV_{DD} system. To find the quiescent current value of the HV_{DD} system, simply calculate the quiescent current flowing in the input/output buffers.

$I_Q (HV_{DD}) = 200 \times 10^{-9} \times (40 + 60 + 12) = 22.40 \times 10^{-6}$ [A]

From the above calculation results, the quiescent current values to be obtained in this example are

$I_Q (LV_{DD}) = 1048.7 \times 10^{-6}$ [A]

$I_Q (HV_{DD}) = 22.40 \times 10^{-6}$ [A]

1.3.4 Temperature Characteristics of Quiescent Current

The quiescent current values at temperatures other than T_j = 85[°C] can be approximately calculated using the equation shown below.
(However, this only applies when T_j = -40 to 85 [°C]. When T_j = 125°C, use a temperature coefficient of 7 to calculate the equation below. When T_j = 85 to 125 [°C], please contact the nearest Epson office or distributor.

$$I_{DDS}(T_j) = I_{DDS}(T_j = 85°C) \times \text{temperature coefficient}$$
$$= I_{DDS}(T_j = 85°C) \times 10^{\frac{T_j - 85}{60}}$$

(However, T_j = 0 to 125°C)

Calculation example:

For a chip whose quiescent current is 630 [µA] when V_{DD} = 2.5 V ± 0.2 V and T_j = 85 [°C], calculate the approximate value of quiescent current when T_j = 50 [°C] as follows:

$$I_{DDS}(T_j = 50°C) = I_{DDS}(T_j = 85°C) \times 10^{\frac{50 - 85}{60}}$$
$$= 630 \times 0.261$$
$$= 164.43 \text{ [µA]}$$

For dual-power supply systems, the sum of quiescent currents for the voltages used constitutes the total amount of quiescent current.

(HI_{DDS} + LI_{DDS})

1.4 Embedded Array Development Flow

The embedded arrays are developed jointly by customers and Epson. Customers perform work based on the cell libraries and various design materials supplied by Epson. This work includes system design, circuit design, and pattern design.

Before these designs can be interfaced to Epson, customers are requested to check them based on the data release checklist included herein. After completion of that check, the necessary data and documentation may be presented to Epson.

Customers conduct simulations of said designs using EDA software or EPITS* available on hand, and Epson undertakes subsequent work following placement and routing.

Note *: EPITS is Epson's ASIC library that runs on MS-Windows NT4.0 and SUN-Solaris platforms.

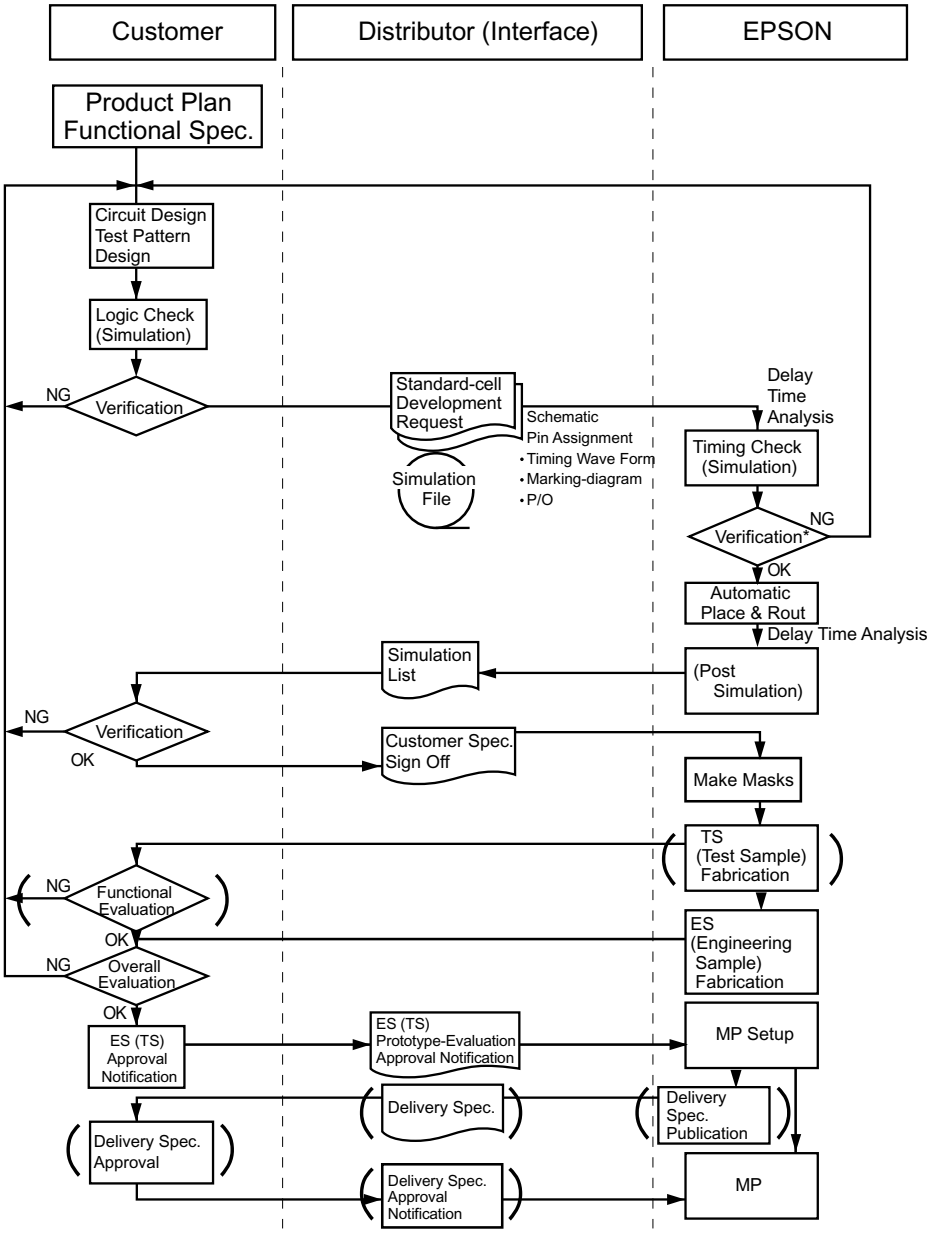
EPITS currently supports the following types of EDA software:

- Verilog-XL (*1)
- Design Compiler (*2)

Note *1: Verilog-XL is a registered trademark of Cadence Design Systems Corporation, USA.
*2: Design Compiler is a registered trademark of Synopsys, Inc., USA.

For more information, please contact the sales division of Epson.

The process flow of the embedded array development process is shown below.



Operations enclosed in ( ) are performed only when so requested by customers.

Chapter 2 Estimating the Gate Density

This chapter describes the procedure for estimating the circuit size after cutting out circuits from the customer's system, and then estimating an approximate bulk size. The precautions to be taken when performing this work are also described.

2.1 Dividing Up Logic Between Chips

When cutting out circuits from the customer's system, care must be taken with respect to the following points.

- Precautions to be taken

  (1) Logic size to be integrated (Gate count)

  (2) Number of I/O pins required (Pin count)

  (3) Package to be used

  (4) Power consumption

Generally speaking, as the circuit size increases, so does the power consumption of the circuit and the number of input/output pins on it. If the circuit size is significantly large, the circuit may be divided into multiple chips rather than being integrated into a single chip. This helps reduce the total cost and the power consumption of the circuit.

2.2 Estimating the Gate Counts Used

The circuit size is estimated by counting the total number of basic cells for each cell (BC counts). The "Embedded Array S1X60000 Series MSI Cell Library" lists the BC counts of each cell. Refer to this manual to obtain the sum total of BC counts for a circuit.

2.3 Estimating the Number of Input/Output Pins

After the number of gates used in cells has been estimated, calculate the number of actually used input/output pins. When performing this calculation, make sure the test pins and power supply pins on Basic Cell type RAM and Cell Based-type RAM and ROM are included in the pin counts. To estimate the number of power supply pins, use the method described in Section 9.11, "Pin Layout and Simultaneous Operation."

2.4 Bulk List

The optimum master (Bulk) is determined from the gate counts used, RAM, functional cells, number of input/output pins (including power supply pins), and package to be used.

Table 2-1 lists the primary Bulks in the S1X60000 series.

Table 2-1 List of Representative Bulks

Bulk	BC Counts	PAD Counts	Basic Cell Arrays		Cell Usage Efficiency		
			X direction	Y direction	3 layers	4 layers	5 layers
A	99,220	112	605	164	60	70	80
B	171,720	148	795	216	60	70	80
C	284,394	188	1,023	278	50	65	75
D	400,290	224	1,213	330	50	65	75
E	595,362	272	1,481	402	50	65	75
F	831,572	284	1,747	476	40	50	60
G	1,234,820	344	2,129	580	40	50	60
H	1,587,754	388	2,413	658	40	50	60
I	1,902,960	424	2,643	720	40	50	60
J	2,519,604	488	3,043	828	40	50	60

Chapter 3 MSI Cells

3.1 MSI Cell Types

Below is a list of the functions of the MSI cell types in the S1X60000 series.

For more information, please contact the sales division of Epson.

List of cell functions in the S1X60000 series

- BUFFER
- INVERTER
- DELAY LINE
- AND GATE
  INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
  INPUT (5/6/8)
- NAND GATE
  INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
  INPUT (5/6/8)
- OR GATE
  INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
  INPUT (5/6/8)
- NOR GATE
  INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
  INPUT (5/6/8)
- EXCLUSIVE OR/NOR
  INPUT (2/3)
- AND-NOR GATES
  2-AND-NOR INPUT (3/4/6/8)
  3-AND-NOR INPUT (4/6)
- AND-OR GATES
  2-AND-OR INPUT (3/4/5/6/8)
  3-AND-OR INPUT (4/5/6)
  4-AND-OR INPUT (8)
- OR-AND GATES
  2-OR-AND INPUT (3/4/5/6/8)
  3-OR-AND INPUT (4/5/6)
  4-OR-AND INPUT (8)
- OR-NAND GATES
  2-AND-OR INPUT (3/4/8)
  3-AND-OR INPUT (4/6)

- MULTI-FUNCTION GATES
  2-OR 2-AND 4-INPUT OR GATE
  2-AND 2-OR 4-INPUT AND GATE
  2-OR 2-NAND 4-INPUT OR GATE
  2-AND 2-NOR 4-INPUT AND GATE
- MAJORITY GATES
  2 of 3/Inverted 2 of 3
- TEST Function
  Special Delay Cell for AC Testing
  Test Mode Control Circuit
- CLOCK Tree
  ROOT BUFFER
  BUFFER/INVERTER
- GATED CLOCK
  2-INPUT AND GATE
  2-INPUT OR GATE
  2-INPUT NAND GATE
  2-INPUT NOR GATE
  INVERTER
  SELECTOR/MULTIPLEXER
- FLIP FLOPS
  D-FLIP FLOP
    SET/RESET
    SYNCHRONOUS
    Enabled
    OUTPUT Q
    NEGATIVE CLOCK
    SCAN
    QUADRUPLE (Reset/Reset and Q Output Only)
    OCTAL (Reset/Reset and Q Output Only)
  JK-FLIP FLOP
    SET/RESET
    OUTPUT Q
    SCAN
  RS-FLIP FLOP
    NAND-TYPE/NOR-TYPE
- LATCHES
  PRESET/RESET
  OUTPUT M
  NEGATIVE CLOCK
  QUADRUPLE (Reset/Reset and M Output Only)
  OCTAL with Enable
- ADDER
  1-Bit Full Adder/Power (2/4)
  4-Bit Full Adder
  4-Bit Full Adder with Fast Carry

- COMPARATORS
  4-Bit Magnitude Comparator with Enable
  8-Bit Magnitude Comparator with Enable
- COUNTERS
  4Bit Binary Up Counter with Reset, Load and Enable
  4Bit Binary Up Counter with Reset and Enable
  4Bit Binary Up/Down Counter with Load and Enable
  4Bit Binary Up/Down Counter with Reset, Load and Enable
- DECODERS
  3-LINE to 8-LINE
  2-LINE to 4-LINE
  ENABLE
- SELECTORS/MULTIPLEXERS
  2-LINE to 1-LINE
  4-LINE to 1-LINE
  ENABLE
  QUADRUPLE 2-LINE to 1-LINE
  ENABLE
  NEGATIVE OUTPUT
- SHIFT REGISTERS
  8-Bit SI/PO Shift Register with Reset
  8-Bit SI/PO PI/SO Shift Register with Reset, Load and Enable
  4-Bit SI/PO PI/SO Shift Register with Reset, Load and Enable
  4-Bit Bi-Directional Universal Shift Register with Reset
- BUS CELLS
  LATCH (QUADRUPLE/OCTAL)
  1Bit RAM
  3-STATE BUFFER
  -Low ENABLE/High ENABLE
  BUS Driver

Chapter 4 Types of Input/Output Buffers and Their Use (X Type)

This chapter describes in detail how the input buffers, output buffers, and bi-directional buffers of the SIX60000 series (X Type) are constructed.

4.1 Types of Input/Output Buffers

The S1X60000 series (X type) offers a wide selection of cells to choose from depending on the input interface level, whether Schmitt trigger input is needed and pull-up/pull-down resistors are included, output drive capability, and whether noise reduction measures are incorporated.
Choose the input/output buffers that best suit your system by considering the items described below. Note that there are two methods of using input/output buffers: when operating buffers with a single power supply (2.5 V or 2.0 V), or operating buffers with dual power supplies (3.3 V/2.5 V, or 3.3 V/2.0 V).

4.1.1 Selecting input/output buffers

(1) Selecting an input buffer

a) Whether the necessary interface level is CMOS level or LVTTL level

b) Whether Schmitt trigger input is needed (i.e., whether hysteresis characteristics are required)

c) Whether internal pull-up/pull-down resistors are needed

(2) Selecting an output buffer

a) Necessary amounts of output drive currents (I_{OL}/I_{OH})

b) Whether noise reduction measures are needed

c) Whether a bus hold circuit is needed

(3) Selecting a bi-directional buffer

Consider items (1) and (2) above to select a bi-directional buffer.

- Input interface level

(1) When HV_{DD} = 3.3 V

Input level

LVTTL level, CMOS level, LVTTL Schmitt, CMOS Schmitt, PCI-3V*

Output level

CMOS level, PCI-3V*

(2) When V_{DD} or LV_{DD} = 2.5 V

Input level

CMOS level, CMOS Schmitt

Output level

CMOS level

(3) When V_{DD} or LV_{DD} = 2.0 V

Input level

CMOS level, CMOS Schmitt

Output level

CMOS level

Note: LVTTL level input cannot be used for single-power supply systems.
* For the PCI interface, please contact the sales division of Epson.

- Output drive capability

  See Tables 1-7, 1-8, and 1-9 for electrical characteristics.

- Pull-up/pull-down resistors

  See Tables 1-7, 1-8, and 1-9 for electrical characteristics.

4.1.2 Bus Hold Circuit

To ensure that the output pins and bi-directional pins will not enter a high-impedance state, S1X60000 (X Type) series has available an input/output buffer that comes equipped with a bus hold facility to hold the data at the output pins.

However, because the bus hold circuit's retention capability is suppressed so as not to adversely affect the ordinary operation of the cell, do not use the output data held by the circuit as valid data. The retained data may easily change state when any data is supplied from an external circuit.

For the bus hold circuit's output retention current, refer to Table 1-7 through 1-9.

4.2 Input/Output Buffers for a Single Power Supply

When the input/output buffers are used with a single power supply, the useful power supply voltage is 2.5 V or 2.0 V only.

4.2.1 Input Buffers

Table 4-1 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	V_{DD} = 2.5 V	V_{DD} = 2.0 V	
Type 1	50	70	kΩ
Type 2	100	140	kΩ

Table 4-2 Input Buffers List

Cell Name*1	Input Level	Whether Pull-up/Pull-down Resistors are Included
XIBC XIBCP# XIBCD#	CMOS CMOS CMOS	None Pull-up resistor included Pull-down resistor included
XIBH XIBHP# XIBHD#	CMOS Schmitt CMOS Schmitt CMOS Schmitt	None Pull-up resistor included Pull-down resistor included

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-1).

4.2.2 Output Buffers

Tables 4-4 and 4-6 list the output buffers.

Table 4-3 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}*1/I_{OL}*2		Unit
	V_{DD} = 2.5 V	V_{DD} = 2.0 V	
Type S	-0.1/0.1	-0.05/0.05	mA
Type M	-1/1	-0.3/0.3	mA
Type 1	-3/3	-1/1	mA
Type 2	-6/6	-2/2	mA
Type 3	-9/9	-3/3	mA

Notes *1: V_{OH} = V_{DD} - 0.4 V (V_{DD} = 2.5 V) or V_{DD} - 0.2 V (V_{DD} = 2.0 V)

*2: V_{OL} = 0.4 V (V_{DD} = 2.5 V) or 0.2 V (V_{DD} = 2.0 V)

Table 4-4 Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name*1, *2
Normal output	Type S Type M Type 1 Type 2 Type 3	XOB#T
Normal output for high speed	Type 3	XOB3AT
Normal output for low noise	Type 3	XOB3BT
3-state output	Type S Type M Type 1 Type 2 Type 3	XTB#T
3-state output for high speed	Type 3	XTB3AT
3-state output for low noise	Type 3	XTB3BT
3-state output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XTB$HT
3-state output for high speed (Bus hold circuit)	Type 3	XTB3AHT
3-state output for low noise (Bus hold circuit)	Type 3	XTB3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-4, the output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-5 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL} *1		Unit
	V_{DD} = 2.5 V	V_{DD} = 2.0 V	
Type 1	3	1	mA
Type 2	6	2	mA
Type 3	9	3	mA

Note *1: V_{OL} = 0.4 V (V_{DD} = 2.5 V) or V_{DD} - 0.2 V (V_{DD} = 2.0 V)

Table 4-6 N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name*1, *2
Normal output	Type 1 Type 2 Type 3	XOD#T

Notes *1: The # denotes 1, 2, or 3 with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-5).

*2: In addition to the configurations in Table 4-6, the N channel open drain output buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

4.2.3 Bi-directional Buffers

Tables 4-7 and 4-8 list bi-directional buffers.

Table 4-7 Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
CMOS	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XBC#T
	Bi-directional output for high speed	Type 3	XBC3AT
	Bi-directional output for low noise	Type 3	XBC3BT
CMOS Schmitt	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XBH#T
	Bi-directional output for high speed	Type 3	XBH3AT
	Bi-directional output for low noise	Type 3	XBH3BT
CMOS	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XBC$HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XBC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XBH$HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XBH3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-7, the bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-8 N channel Open drain Bi-directional Buffers List

Input Level	Function	I_{OL}	Cell Name[*1, *2]
CMOS	Bi-directional output	Type 1 Type 2 Type 3	XBDC#T
CMOS Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XBDH#T

Notes *1: The # denotes 1, 2, or 3 with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-5).

*2: In addition to the configurations shown in Table 4-8, the N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.2.4 Fail-Safe Cells

4.2.4.1 Overview

The S1X60000 series (X type) Fail-Safe cells allow signals above the power supply voltage to be interfaced, even while power is supplied.

Furthermore, no leakage current flows in those cells, despite the fact that the signals are interfaced while the power is cut off. Therefore, they provide greater freedom of design than ever before.

(In dual-power supply systems, these are used as LV_{DD} system cells.)

4.2.4.2 Features

(1) The Fail-Safe cells can be positioned as desired by customers.

(2) Even when input signals above the power supply voltage are applied while power is supplied, no input leakage current flows. (For input buffers or bi-directional buffers with pull-up resistors, however, a small input leakage current of approximately 30 µA may flow due to their circuit configuration.)

(3) Even when input signals are applied from the outside while the power is cut off, no input leakage current flows.

(4) Fail-Safe cells with two different input levels, the CMOS level and the CMOS Schmitt level, are available.

(5) Because the Fail-Safe cells are completely CMOS structured, the power consumption can be suppressed to a minimum.

4.2.4.3 Usage Precautions

(1) About input I/O cells

- For input buffers without resistors or with pull-down resistors, ordinary input buffers may be used directly as Fail-Safe cells.
- If input buffers with pull-up resistors are needed, always be sure to use Fail-Safe cells (however, a small input leakage current of approximately 30 µA may flow due to their circuit configuration).

(2) About output I/O cells

- Provided that the output buffers are placed in High-Z state or the bi-directional buffers are placed in input mode, no input leakage current may flow even when input signals above the power supply voltage are applied while power is supplied.
- If signals above the power supply voltage are applied while the bi-directional buffers are placed in output mode, an input leakage current flows as in ordinary input/output buffers. The same applies when pull-up resistors above the power supply voltage exist outside the chip.
  (If a High logic level above the power supply voltage is needed, use open drain type input/output buffers, with pull-up resistors added external to the chip in order to pull-up the logic level High.)

(3) Although the Fail-Safe cells can receive high voltage signals above the LSI's operating voltage, be aware that the signal voltages applied to the Fail-Safe cells must never exceed their rated maximum voltage.

4.2.4.4 List of Cells

Table 4-9 Fail-Safe Input Buffers List

Cell Name[*1, *2]	Input Level	Whether Pull-up Resistors are Included
XIBBP#	CMOS	Pull-up resistor included
XIBGP#	CMOS Schmitt	Pull-up resistor included

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-1).

Table 4-10 Fail-Safe Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
3-state output	Type 1 Type 2	XTBF#T
3-state output for high speed	Type 3	XTBF3AT
3-state output for low noise	Type 3	XTBF3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2 respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-10, the Fail-Safe output buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-11 Fail-Safe Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
CMOS	Bi-directional output	Type 1 Type 2	XBB#T
	Bi-directional output for high speed	Type 3	XBB3AT
	Bi-directional output for low noise	Type 3	XBB3BT
CMOS Schmitt	Bi-directional output	Type 1 Type 2	XBG#T
	Bi-directional output for high speed	Type 3	XBG3AT
	Bi-directional output for low noise	Type 3	XBG3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-11, the Fail-Safe bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.2.5 Gated Cells

4.2.5.1 Overview

The S1X60000 series (X type) Gated I/O cell is the first product that allows inputs to pins to be placed in the floating, or High-Z, state without the use of pull-up or pull-down circuits. Moreover, the power supply on the high voltage side (HV_{DD}) in a dual power supply design can be cut off. There are two types of cells to choose from depending on whether a High level control signal or Low level control signal shuts off the power supply. Therefore, customers can choose the desired type of cell according to their circuit design.

4.2.5.2 Features

(1) The Gated cells can be positioned as desired by customers. There are no limitations on the number of cells used or the locations in which they are placed. As a result, freedom of design is increased.

(2) The power supply on the high voltage side (HV_{DD}) in a dual power supply design can be cut off. However, because special measures must be taken for this cut off, please contact the sales division of Epson.

(3) Inputs can be placed in the High-Z state without the use of pull-up or pull-down circuits.

(4) Due to circuit structure, the input level of the Gated I/O cell in a dual power supply system is not HV_{DD} system but LV_{DD} system CMOS level.

(5) There are two types of cells to choose from depending on whether a High level control signal or Low level control signal shuts off the power supply.

(6) Because the Gated cells are completely CMOS structured, the power consumption can be suppressed to a minimum.

4.2.5.3 Usage Precautions

(1) To place inputs in the High-Z state through the use of Gated I/O cells, inputs to pins must be shut off by using Gated I/O cell control signals before they enter the High-Z state. If inputs are placed in the High-Z state without performing this control, large current may flow into the cell as in ordinary cells, causing it to break down. Conversely, the same problem may occur when using Gated I/O cell control to connect inputs (in the High-Z state) to pins. In such a case, the logic level latched into the device's internal circuit cannot be guaranteed.

(2) When the power supply on the high voltage side (HV_{DD}) is to be cut off by using a Gated I/O cell, the same processing as described in (1) is required. This processing must be performed; otherwise, the logic level latched to the device's internal circuit cannot be guaranteed. Moreover, because special measures must be taken for cut-off, please contact the sales division of Epson.

4.2.5.4 List of Cells

Table 4-12 Gated Input Buffers List

Cell Name[*1]	Input Level	Whether Pull-up/Pull-down Resistors are Included
XIBA XIBAP# XIBAD#	CMOS (AND Type)	None Pull-up resistor included Pull-down resistor included
XIBO XIBOP# XIBOD#	CMOS (OR Type)	None Pull-up resistor included Pull-down resistor included

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-1).

Table 4-13 Gated Bi-directional Buffers List

Input Level		Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
CMOS	AND Type	Bi-directional output	Type 1 Type 2 Type 3	XBA#T
		Bi-directional output for high speed	Type 3	XBA3AT
		Bi-directional output for low noise	Type 3	XBA3BT
	OR Type	Bi-directional output	Type 1 Type 2 Type 3	XBO#T
		Bi-directional output for high speed	Type 3	XBO3AT
		Bi-directional output for low noise	Type 3	XBO3BT

Notes *1: The # denotes 1, 2, or 3, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-13, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.3 Dual Power Supply Input/Output Buffers

If your system uses dual power supplies, use input/output buffers designed exclusively for operation with dual power supplies. (In this case, be careful not to use input/output buffers designed for operation with a single power supply.)

Moreover, input/output buffers for a single power supply system and those for a dual power supply system cannot be used in combination. However, the test buffer (XITST1) can be used in both single power supply and dual power supply systems. (Combined use with the XF type of input/output buffers is also not allowed.)

(1) HV_{DD} input/output buffers

The HV_{DD} input/output buffers are available in several types. These include input buffers that accept as input 3.3 V signals, output buffers that output 3.3 V amplitude signals, and bi-directional buffers that accept as input 3.3 V signals or output 3.3 V amplitude signals.

(2) LV_{DD} input/output buffers

The LV_{DD} input/output buffers are available in several types. These include input buffers that accept as input 2.5 V (or 2.0 V) signals, output buffers that output 2.5 V (or 2.0 V) amplitude signals, and bi-directional buffers that accept as input 2.5 V (or 2.0 V) signals or output 2.5 V (or 2.0 V) amplitude signals. For LV_{DD} bi-directional buffers, do not apply voltages above LV_{DD}. This is due to the fact that, if HV_{DD} signals are supplied to those buffers, an excessive current flows in their internal protective diode, causing their quality to degrade (in such a case, use the Fail-Safe cells described in Section 4.3.4, “Fail-Safe Cells”).

4.3.1 Input Buffers

(1) HV_{DD} input buffers

The input buffers are configured using only input cells.

The HV_{DD} input buffers consist of a first input stage configured with an HV_{DD} input circuit and a next stage configured with an LV_{DD} circuit, so that HV_{DD} signals are converted into LV_{DD} signals before being fed into the MSI cell.

Table 4-15 lists the HV_{DD} input buffers.

Table 4-14 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value (HV_{DD} = 3.3 V)	Unit
Type 1	60	kΩ
Type 2	120	kΩ

Table 4-15 HV_{DD} Input Buffers List

Cell Name*1	Input Level	Whether Pull-up/Pull-down Resistors are Included
XHIBC XHIBCP# XHIBCD#	CMOS CMOS CMOS	None Pull-up resistor Pull-down resistor
XHIBT XHIBTP# XHIBTD#	LVTTL LVTTL LVTTL	None Pull-up resistor Pull-down resistor
XHIBH XHIBHP# XHIBHD#	CMOS Schmitt CMOS Schmitt CMOS Schmitt	None Pull-up resistor Pull-down resistor
XHIBS XHIBSP# XHIBSD#	LVTTL Schmitt LVTTL Schmitt LVTTL Schmitt	None Pull-up resistor Pull-down resistor
XHIBPB XHIBPBP# XHIBPBD#	PCI-3V PCI-3V PCI-3V	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-14).

(2) LV_{DD} input buffers

The input buffers are configured using only input cells. Table 4-17 lists the LV_{DD} input buffers.

Table 4-16 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	LV_{DD} = 2.5 V	LV_{DD} = 2.0 V	
Type 1	50	70	kΩ
Type 2	100	140	kΩ

Table 4-17 LV_{DD} Input Buffers List

Cell Name*1	Input Level	Whether Pull-up/Pull-down Resistors are Included
XLIBC XLIBCP# XLIBCD#	CMOS CMOS CMOS	None Pull-up resistor Pull-down resistor
XLIBH XLIBHP# XLIBHD#	CMOS Schmitt CMOS Schmitt CMOS Schmitt	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-16).

4.3.2 Output Buffers

(1) HV_{DD} output buffers

Tables 4-19 and 4-21 list the HV_{DD} output buffers.

Table 4-18 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}*1/I_{OL}*2 (HV_{DD} = 3.3V)	Unit
Type S	-0.1/0.1	mA
Type M	-1/1	mA
Type 1	-3/3	mA
Type 2	-6/6	mA
Type 3	-12/12	mA

Note *1: $V_{OH} = HV_{DD}$ - 0.4 V

*2: V_{OL} = 0.4 V

Table 4-19 HV_{DD} Output Buffers List

Function	I_{OL}/I_{OH}	Cell Name*1, *2
Normal output	Type S Type M Type 1 Type 2 Type 3	XHOB#T
Normal output for high speed	Type 3	XHOB3AT
Normal output for low noise	Type 3	XHOB3BT
Normal output fot PCI	PCI-3V	XHOBPBT
3-state output	Type S Type M Type 1 Type 2 Type 3	XHTB#T
3-state output for high speed	Type 3	XHTB3AT
3-state output for low noise	Type 3	XHTB3BT
3-state output fot PCI	PCI-3V	XHTBPBT
3-state output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XHTB$HT
3-state output for high speed (Bus hold circuit)	Type 3	XHTB3AHT
3-state output for low noise (Bus hold circuit)	Type 3	XHTB3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-19, the output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-20 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}*1 (HV_{DD} = 3.3V)	Unit
Type 1	3	mA
Type 2	6	mA
Type 3	12	mA

Note *1: V_{OL} = 0.4 V

Table 4-21 HV_{DD} N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name*1, *2
Normal output	Type 1 Type 2 Type 3	XHOD#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-20).

*2: In addition to the configurations shown in Table 4-21, the HV_{DD} N channel open drain output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} output buffers

Tables 4-23 and 4-25 list the LV_{DD} output buffers.

Table 4-22 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}*1/I_{OL}*2		Unit
	LV_{DD} = 2.5 V	LV_{DD} = 2.0 V	
Type S	-0.1/0.1	-0.05/0.05	mA
Type M	-1/1	-0.3/0.3	mA
Type 1	-3/3	-1/1	mA
Type 2	-6/6	-2/2	mA
Type 3	-9/9	-3/3	mA

Notes *1: V_{OH} = LV_{DD} - 0.4 V (LV_{DD} = 2.5 V) or LV_{DD} - 0.2 V (LV_{DD} = 2.0 V)

*2: V_{OL} = 0.4 V (LV_{DD} = 2.5 V) or 0.2 V (LV_{DD} = 2.0 V)

Table 4-23 LV_{DD} Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name*1, *2
Normal output	Type S Type M Type 1 Type 2 Type 3	XLOB#T
Normal output for high speed	Type 3	XLOB3AT
Normal output for low noise	Type 3	XLOB3BT
3-state output	Type S Type M Type 1 Type 2 Type 3	XLTB#T
3-state output for high speed	Type 3	XLTB3AT
3-state output for low noise	Type 3	XLTB3BT
3-state output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XLTB$HT
3-state output for high speed (Bus hold circuit)	Type 3	XLTB3AHT
3-state output for low noise (Bus hold circuit)	Type 3	XLTB3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-23, the output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-24 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}*1		Unit
	LV_{DD} = 2.5 V	LV_{DD} = 2.0 V	
Type 1	3	1	mA
Type 2	6	2	mA
Type 3	9	3	mA

Note *1: V_{OL} = 0.4 V (LV_{DD} = 2.5 V) or 0.2 V (LV_{DD} = 2.0 V)

Table 4-25 LV_{DD} N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name*1, *2
Normal output	Type 1 Type 2 Type 3	XLOD#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-24).

*2: In addition to the configurations shown in Table 4-25, the N channel open drain output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.3.3 Bi-directional Buffers

(1) HV_{DD} bi-directional buffers

Tables 4-26 and 4-27 list the HV_{DD} bi-directional buffers.

Table 4-26 HV_{DD} Bi-directional Buffers List (1/2)

Input Level	Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
LVTTL	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XHBT#T
	Bi-directional output for high speed	Type 3	XHBT3AT
	Bi-directional output for low noise	Type 3	XHBT3BT
CMOS	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XHBC#T
	Bi-directional output for high speed	Type 3	XHBC3AT
	Bi-directional output for low noise	Type 3	XHBC3BT
PCI	Bi-directional output for PCI	PCI-3V	XHBPBT
LVTTL Schmitt	Bi-directional	Type S Type M Type 1 Type 2 Type 3	XHBS#T
	Bi-directional output for high speed	Type 3	XHBS3AT
	Bi-directional output for low noise	Type 3	XHBS3BT
CMOS Schmitt	Bi-directional	Type S Type M Type 1 Type 2 Type 3	XHBH#T
	Bi-directional output for high speed	Type 3	XHBH3AT
	Bi-directional output for low noise	Type 3	XHBH3BT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-26, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-26 List of HV_{DD} Bi-directional Buffers List (2/2)

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
LVTTL	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XHBT#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XHBT3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XHBT3BHT
CMOS	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XHBC#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XHBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XHBC3BHT
LVTTL Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XHBS#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XHBS3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XHBS3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XHBH#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XHBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XHBH3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-26, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-27 HV_{DD} N channel Open drain Bi-directional Buffers List

Input Level	Function	I_{OL}	Cell Name*1, *2
LVTTL	Bi-directional output	Type 1 Type 2 Type 3	XHBDT#T
CMOS	Bi-directional output	Type 1 Type 2 Type 3	XHBDC#T
LVTTL Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XHBDS#T
CMOS Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XHBDH#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-20).

*2: In addition to the configurations shown in Table 4-27, the HV_{DD} N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} bi-directional buffers

Tables 4-28 and 4-29 list the LV_{DD} bi-directional buffers.

Table 4-28 LV_{DD} Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
CMOS	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XLBC#T
	Bi-directional output for high speed	Type 3	XLBC3AT
	Bi-directional output for low noise	Type 3	XLBC3BT
CMOS Schmitt	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XLBH#T
	Bi-directional output for high speed	Type 3	XLBH3AT
	Bi-directional output for low noise	Type 3	XLBH3BT
CMOS	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XLBC$HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XLBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XLBC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XLBH$HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XLBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XLBH3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-28, the bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-29 LV_{DD} N channel Open drain Bi-directional Buffers List

Input Level	Function	I_{OL}	Cell Name*1, *2
CMOS	Bi-directional output	Type 1 Type 2 Type 3	XLBDC#T
CMOS Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XLBDH#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-24).

*2: In addition to the configurations shown in Table 4-29, the N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.3.4 Fail-Safe Cells

4.3.4.1 Overview

The dual power supply Fail-Safe cells are outlined in Section 4.2.4.1, "Overview" (the Fail-Safe cells used in the dual power supply specification are LV_{DD} cells).

4.3.4.2 Features

For the features of the dual power supply Fail-Safe cells, refer to Section 4.2.4.2, "Features."

4.3.4.3 Usage Precautions

For precautions to be taken when dual power supply Fail-Safe cells are used, refer to Section 4.2.4.3, "Usage Precautions."

4.3.4.4 List of Cells

Table 4-30 Fail-Safe Input Buffers List

Cell Name[*1]	Input Level	Whether Pull-up Resistors are Included
XLIBBP#	CMOS	Pull-up Resistors
XLIBGP#	CMOS Schmitt	Pull-up Resistors

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-16).

Table 4-31 Fail-Safe Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
3-state output	Type 1 Type 2	XLTBF#T
3-state output for high speed	Type 3A	XLTBF3AT
3-state output for low noise	Type 3B	XLTBF3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-31, the Fail-Safe output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-32 Fail-Safe Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
CMOS	Bi-directional output	Type 1 Type 2	XLBB#T
	Bi-directional output for high speed	Type 3	XLBB3AT
	Bi-directional output for low noise	Type 3	XLBB3BT
CMOS Schmitt	Bi-directional output	Type 1 Type 2	XLBG#T
	Bi-directional output for high speed	Type 3	XLBG3AT
	Bi-directional output for low noise	Type 3	XLBG3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-32, the Fail-Safe bi-directional buffers may be configures with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.3.5 Gated Cells

4.3.5.1 Overview

The dual power supply Gated cells are outlined in Section 4.2.5.1, "Overview." (The Gated cells for the dual power supply specification are HV_{DD} cells.)

4.3.5.2 Features

For the features of the dual power supply Gated cells, refer to Section 4.2.5.2, "Features."

4.3.5.3 Usage Precautions

For the precautions to be taken when dual power supply Gated cells are used, refer to Section 4.2.5.3, "Usage Precautions."

4.3.5.4 List of Cells

Table 4-33 Gated Cell Input Buffers List

Cell Name*1, *2	Input Level	Whether Pull-up/Pull-down Resistors are
XHIBA XHIBAP# XHIBAD#	CMOS (AND Type)	None Pull-up resistor Pull-down resistor
XHIBO XHIBOP# XHIBOD#	CMOS (OR Type)	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-14).

Table 4-34 Gated Cell Bi-directional Buffers List

Input Level		Function	I_{OH}/I_{OL}	Cell Name*1, *2
CMOS	AND Type	Bi-directional output	Type 1 Type 2 Type 3	XHBA#T
		Bi-directional output for high speed	Type 3	XHBA3AT
		Bi-directional output for low noise	Type 3	XHBA3BT
	OR Type	Bi-directional output	Type 1 Type 2 Type 3	XHBO#T
		Bi-directional output for high speed	Type 3	XHBO3AT
		Bi-directional output for low noise	Type 3	XHBO3BT

Notes *1: The # denotes 1, 2, or 3, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-34, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.4 Dual Power Supplies Guidelines

The S1X60000 series allows each input/output buffer to be interfaced with 3.3 V, 2.5 V, or 2.0 V signals as desired, using a dual power supply system. The internal cell area operates using a 2.5 V or 2.0 V single power supply.

4.4.1 Method of Adapting to Dual Power Supplies

The S1X60000 series allows input/output buffers to be interfaced with the signals of voltages that differ from the internal operating voltage. There are two methods for interfacing with different power supply voltages.

- For a single power supply

  In a single power supply system, it is possible to apply input signals of voltages higher than the power supply voltage, using N channel open drain type buffers or Fail-Safe cells. However, high voltage signals above the power supply voltage cannot be output. This problem can be solved through the combined use of N channel open drain type buffers and external pull-up resistors.

- For dual power supplies

  By using input buffers designed exclusively for operation with dual power supplies, it is possible to apply input signals of voltages higher than the internal operating voltage. Similarly, high voltage signals above the internal operating voltage can be output using dual power supply output buffers.

4.4.2 Power Supplies for Dual Power Operation

If your circuit is to be operated using two different power supplies, use two power supply cells: HV_{DD} and LV_{DD}. Specifically, HV_{DD} may be used for HV_{DD} input/output buffers, and LV_{DD} may be used for LV_{DD} input/output buffers and internal cells. The power supply voltages must always satisfy the equation below.

$HV_{DD} \geq LV_{DD}$

If $HV_{DD} < LV_{DD}$, operation of the internal circuit cannot be guaranteed. The operating conditions specified below are recommended.

HV_{DD} = 3.3 V, LV_{DD} = 2.5 V
HV_{DD} = 3.3 V, LV_{DD} = 2.0 V

4.4.3 Turning On/Off Dual Power Supplies

For chips designed to dual power supply specifications, make sure the power is turned on and off in the order specified below.

When turning on: LV_{DD} (internal) → HV_{DD} (I/O section) → input signals applied
When turning off: Input signals off → HV_{DD} (I/O section) → LV_{DD} (internal)

Note 1: Avoid keeping only HV_{DD} turned on (for 1 sec or more) while LV_{DD} is turned off, so as not to degrade the chip's reliability.

Note 2: When turning HV_{DD} back on after it was off, always be sure to initialize the circuit following power on. This is necessary to ensure the internal circuit state in the event of power supply noise or the like.

Chapter 5 Types of Input/Output Buffers and Their Use (XF Type)

This chapter describes in detail how the input buffers, output buffers, and bi-directional buffers of the SIX6000 series (XF Type) are constructed.

5.1 Types of Input/Output Buffers

The S1X60000 series (XF type) offers a wide selection of cells to choose from depending on the input interface level, whether Schmitt trigger input is needed and pull-up/pull-down resistors are included, output drive capability, and whether noise reduction measures are incorporated.
Choose the input/output buffers that best suit your system by considering the items described below. Note that input/output buffers of this type can only be used with dual power supplies (3.3 V/2.5 V or 3.3 V/2.0 V).

5.1.1 Selecting input/output buffers

(1) Selecting an input buffer

a) Whether 5 V interfacing is needed

b) Whether the necessary interface level is CMOS level or LVTTL level

c) Whether Schmitt trigger input is needed (i.e., whether hysteresis characteristics are required)

d) Whether internal pull-up/pull-down resistors are needed

(2) Selecting an output buffer

a) Whether 5 V pull-up resisters external to the chip are needed

b) Necessary amounts of output drive currents (I_{OL}/I_{OH})

c) Whether noise reduction measures are needed

d) Whether a bus hold circuit is needed

(3) Selecting a bi-directional buffer

Consider items (1) and (2) above to select a bi-directional buffer.

- Input interface level

(1) When HV_{DD} = 3.3 V

Input level

LVTTL level, CMOS level, LVTTL Schmitt, CMOS Schmitt, PCI-3V*

Output level

CMOS level, PCI-3V*

(2) When LV_{DD} = 2.5 V

Input level

CMOS level, CMOS Schmitt

Output level

CMOS level

(3) When LV_{DD} = 2.0 V

Input level

CMOS level, CMOS Schmitt

Output level

CMOS level

Note: * For the PCI interface, please contact the sales division of Epson.

- Output drive capability

  See Tables 1-13, 1-14, and 1-15 for electrical characteristics.

- Pull-up/pull-down resistors

  See Tables 1-13, 1-14, and 1-15 for electrical characteristics.

5.1.2 Bus Hold Circuit

To ensure that the output pins and bi-directional pins will not enter a high-impedance state, the S1X60000 series (XF Type) has available an input/output buffer that comes equipped with a bus hold facility to hold the data at the output pins.

However, because the bus hold circuit's retention capability is suppressed so as not to adversely affect the ordinary operation of the cell, do not use the output data held by the circuit as valid data. The retained data may easily change state when any data is supplied from an external circuit.

For the bus hold circuit's output retention current, refer to Table 1-13 through 1-15.

5.2 Dual Power Supply Input/Output Buffers

The input/output buffers of the S1X60000 series (XF type) can only be used in a dual power supply system. (These buffers cannot be used in combination with the X type of input/output buffers.)

(1) HV_{DD} input/output buffers

The HV_{DD} input/output buffers are available in several types. These include input buffers that accept as input 3.3 V signals, output buffers that output 3.3 V amplitude signals, and bi-directional buffers that accept as input 3.3 V signals or output 3.3 V amplitude signals. Moreover, 5 V tolerant Fail-Safe cells are available, which allow 5.0 V amplitude signals to be applied.

(2) LV_{DD} input/output buffers

The LV_{DD} input/output buffers are available in several types. These include input buffers that accept as input 2.5 V (or 2.0 V) signals, output buffers that output 2.5 V (or 2.0 V) amplitude signals, and bi-directional buffers that accept as input 2.5 V (or 2.0 V) signals or output 2.5 V (or 2.0 V) amplitude signals. For LV_{DD} bi-directional buffers, do not apply voltages above LV_{DD}. This is due to the fact that, if HV_{DD} signals are supplied to those buffers, an excessive current flows in their internal protective diode, causing their quality to degrade (in such a case, use the Fail-Safe cells described in Section 5.2.4, “Fail-Safe Cells”).

5.2.1 Input Buffers

(1) HV_{DD} input buffers

The input buffers are configured using only input cells.

The HV_{DD} input buffers consist of a first input stage configured with an HV_{DD} input circuit and a next stage configured with an LV_{DD} circuit, so that HV_{DD} signals are converted into LV_{DD} signals before being fed into the MSI cell (internal cell area).

Table 5-2 lists the HV_{DD} input buffers.

Table 5-1 Rated Pull-up/Pull-down-Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value (HV_{DD} = 3.3 V)	Unit
Type 1	60	kΩ
Type 2	120	kΩ

Table 5-2 HV_{DD} Input Buffers List

Cell Name*1	Input Level	Whether Pull-up/Pull-down Resistors are Included
XFHIBC XFHIBCP# XFHIBCD#	CMOS CMOS CMOS	None Pull-up resistor Pull-down resistor
XFHIBT XFHIBTP# XFHIBTD#	LVTTL LVTTL LVTTL	None Pull-up resistor Pull-down resistor
XFHIBH XFHIBHP# XFHIBHD#	CMOS Schmitt CMOS Schmitt CMOS Schmitt	None Pull-up resistor Pull-down resistor
XFHIBS XFHIBSP# XFHIBSD#	LVTTL Schmitt LVTTL Schmitt LVTTL Schmitt	None Pull-up resistor Pull-down resistor
XFHIBPB XFHIBPBP# XFHIBPBD#	PCI-3V PCI-3V PCI-3V	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 5-1).

(2) LV_{DD} input buffers

The input buffers are configured using only input cells. Table 5-4 lists the LV_{DD} input buffers.

Table 5-3 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	LV_{DD} = 2.5 V	LV_{DD} = 2.0 V	
Type 1	50	70	kΩ
Type 2	100	140	kΩ

Table 5-4 LV_{DD} Input Buffers List

Cell Name*1	Input Level	Whether Pull-up/Pull-down Resistors are Included
XFLIBC XFLIBCP# XFLIBCD#	CMOS CMOS CMOS	None Pull-up resistor Pull-down resistor
XFLIBH XFLIBHP# XFLIBHD#	CMOS Schmitt CMOS Schmitt CMOS Schmitt	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 5-3).

5.2.2 Output Buffers

(1) HV_{DD} output buffers

Tables 5-6 and 5-8 list the HV_{DD} output buffers.

Table 5-5 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}*1/I_{OL}*2 (HV_{DD} = 3.3V)	Unit
Type S	-0.1/0.1	mA
Type M	-1/1	mA
Type 1	-3/3	mA
Type 2	-6/6	mA
Type 3	-12/12	mA

Note *1: $V_{OH} = HV_{DD}$ - 0.4 V

*2: V_{OL} = 0.4 V

Table 5-6 HV_{DD} Output Buffers List

Function	I_{OL}/I_{OH}	Cell Name*1, *2
Normal output	Type S Type M Type 1 Type 2 Type 3	XFHOB#T
Normal output for high speed	Type 3	XFHOB3AT
Normal output for low noise	Type 3	XFHOB3BT
Normal output fot PCI	PCI-3V	XFHOBPBT
3-state output	Type S Type M Type 1 Type 2 Type 3	XFHTB#T
3-state output for high speed	Type 3	XFHTB3AT
3-state output for low noise	Type 3	XFHTB3BT
3-state output fot PCI	PCI-3V	XFHTBPBT
3-state output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFHTB$HT
3-state output for high speed (Bus hold circuit)	Type 3	XFHTB3AHT
3-state output for low noise (Bus hold circuit)	Type 3	XFHTB3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-5).

*2: In addition to the configurations shown in Table 5-6, the HV_{DD} output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-7 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}*1 (HV_{DD} = 3.3V)	Unit
Type 1	3	mA
Type 2	6	mA
Type 3	12	mA

Note *1: V_{OL} = 0.4 V

Table 5-8 HV_{DD} N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name*1, *2
Normal output	Type 1 Type 2 Type 3	XFHOD#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-7).

*2: In addition to the configurations shown in Table 5-8, the HV_{DD} N channel open drain output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} output buffers

Tables 5-10 and 5-12 list the LV_{DD} output buffers.

Table 5-9 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}*1/I_{OL}*2		Unit
	LV_{DD} = 2.5 V	LV_{DD} = 2.0 V	
Type S	-0.1/0.1	-0.05/0.05	mA
Type M	-1/1	-0.3/0.3	mA
Type 1	-3/3	-1/1	mA
Type 2	-6/6	-2/2	mA
Type 3	-9/9	-3/3	mA

Notes *1: V_{OH} = LV_{DD} - 0.4 V (LV_{DD} = 2.5 V) or LV_{DD} - 0.2 V (LV_{DD} = 2.0 V)

*2: V_{OL} = 0.4 V (LV_{DD} = 2.5 V) or 0.2 V (LV_{DD} = 2.0 V)

Table 5-10 LV_{DD} Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name*1, *2
Normal output	Type S Type M Type 1 Type 2 Type 3	XFLOB#T
Normal output for high speed	Type 3	XFLOB3AT
Normal output for low noise	Type 3	XFLOB3BT
3-state output	Type S Type M Type 1 Type 2 Type 3	XFLTB#T
3-state output for high speed	Type 3	XFLTB3AT
3-state output for low noise	Type 3	XFLTB3BT
3-state output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFLTB$HT
3-state output for high speed (Bus hold circuit)	Type 3	XFLTB3AHT
3-state output for low noise (Bus hold circuit)	Type 3	XFLTB3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-9).

*2: In addition to the configurations shown in Table 5-10, output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-11 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}*1		Unit
	LV_{DD} = 2.5 V	LV_{DD} = 2.0 V	
Type 1	3	1	mA
Type 2	6	2	mA
Type 3	9	3	mA

Note *1: V_{OL} = 0.4 V (LV_{DD} = 2.5 V) or 0.2 V (LV_{DD} = 2.0 V)

Table 5-12 LV_{DD} N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name*1, *2
Normal output	Type 1 Type 2 Type 3	XFLOD#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-11).

*2: In addition to the configurations shown in Table 5-12, the LV_{DD} N channel open drain output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

5.2.3 Bi-directional Buffers

(1) HV_{DD} bi-directional buffers

Tables 5-13 and 5-14 list the HV_{DD} bi-directional buffers.

Table 5-13 HV_{DD} Bi-directional Buffers List (1/2)

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
LVTTL	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XFHBT#T
	Bi-directional output for high speed	Type 3	XFHBT3AT
	Bi-directional output for low noise	Type 3	XFHBT3BT
CMOS	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XFHBC#T
	Bi-directional output for high speed	Type 3	XFHBC3AT
	Bi-directional output for low noise	Type 3	XFHBC3BT
PCI	Bi-directional output for PCI	PCI-3V	XFHBPBT
LVTTL Schmitt	Bi-directional	Type S Type M Type 1 Type 2 Type 3	XFHBS#T
	Bi-directional output for high speed	Type 3	XFHBS3AT
	Bi-directional output for low noise	Type 3	XFHBS3BT
CMOS Schmitt	Bi-directional	Type S Type M Type 1 Type 2 Type 3	XFHBH#T
	Bi-directional output for high speed	Type 3	XFHBH3AT
	Bi-directional output for low noise	Type 3	XFHBH3BT

Notes *1: The # denotes 1, 2, or 3, with the I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-5).

*2: In addition to the configurations shown in Table 5-13, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-13 List of HV_{DD} Bi-directional Buffers List (2/2)

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
LVTTL	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFHBT#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XFHBT3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XFHBT3BHT
CMOS	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFHBC#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XFHBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XFHBC3BHT
LVTTL Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFHBS#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XFHBS3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XFHBS3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFHBH#HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XFHBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XFHBH3BHT

Notes *1: The # denotes 1, 2, or 3, with the I_{OH}/I_{OL} values corresponding to Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-5).

*2: In addition to the configurations shown in Table 5-13, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-14 HV_{DD} N channel Open drain Bi-directional Buffers List

Input Level	Function	I_{OL}	Cell Name*1, *2
LVTTL	Bi-directional output	Type 1 Type 2 Type 3	XFHBDT#T
CMOS	Bi-directional output	Type 1 Type 2 Type 3	XFHBDC#T
LVTTL Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XFHBDS#T
CMOS Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XFHBDH#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-7).

*2: In addition to the configurations shown in Table 5-14, the HV_{DD} N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} bi-directional buffers

Tables 5-15 and 5-16 list the LV_{DD} bi-directional buffers.

Table 5-15 LV_{DD} Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
CMOS	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XFLBC#T
	Bi-directional output for high speed	Type 3	XFLBC3AT
	Bi-directional output for low noise	Type 3	XFLBC3BT
CMOS Schmitt	Bi-directional output	Type S Type M Type 1 Type 2 Type 3	XFLBH#T
	Bi-directional output for high speed	Type 3	XFLBH3AT
	Bi-directional output for low noise	Type 3	XFLBH3BT
CMOS	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFLBC$HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XFLBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XFLBC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	Type M Type 1 Type 2 Type 3	XFLBH$HT
	Bi-directional output for high speed (Bus hold circuit)	Type 3	XFLBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	Type 3	XFLBH3BHT

Notes *1: Note that # denotes S, M, 1, 2, or 3; $ denotes M, 1, 2, or 3 with their I_{OH}/I_{OL} values corresponding to Type S, Type M, Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-9).

*2: In addition to the configurations shown in Table 5-15, the LV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-16 LV_{DD} N channel Open drain Bi-directional Buffers List

Input Level	Function	I_{OL}	Cell Name[*1, *2]
CMOS	Bi-directional output	Type 1 Type 2 Type 3	XFLBDC#T
CMOS Schmitt	Bi-directional output	Type 1 Type 2 Type 3	XFLBDH#T

Notes *1: The # denotes 1, 2, or 3, with the I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-11).

*2: In addition to the configurations shown in Table 5-16, the LV_{DD} N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

5.2.4 Fail-Safe Cells

5.2.4.1 Overview

The S1X60000 series (XF Type) Fail-Safe cells allow signals above the power supply voltage to be interfaced, even while power is supplied.
Furthermore, no leakage current flows in those cells, despite the fact that the signals are interfaced while the power is cut off. Therefore, they provide greater freedom of design than ever before. (These cells are used as LV_{DD} system cells.)

5.2.4.2 Features

(1) The Fail-Safe cells can be positioned as desired by customers. There are no limitations on the number of cells that can be used or the locations in which they can be placed.

(2) Even when input signals above the power supply voltage are applied while power is supplied, no input leakage current flows.
(For input buffers or bi-directional buffers with pull-up resistors, however, a small input leakage current of approximately 30 µA may flow due to their circuit configuration.)

(3) Even when input signals are applied from the outside while the power is cut off, no input leakage current flows.

(4) Fail-Safe cells with two different input levels, the CMOS level and the CMOS Schmitt level, are available.

(5) Because the Fail-Safe cells are completely CMOS structured, the power consumption can be suppressed to a minimum.

5.2.4.3 Usage Precautions

(1) About input I/O cells

- For input buffers without resistors or with pull-down resistors, ordinary input buffers may be used directly as Fail-Safe cells.
- If input buffers with pull-up resistors are needed, always be sure to use Fail-Safe cells (however, a small input leakage current of approximately 30 µA may flow due to their circuit configuration).

(2) About output I/O cells

- Provided that the output buffers are placed in High-Z state or the bi-directional buffers are placed in input mode, no input leakage current may flow even when input signals above the power supply voltage are applied while power is supplied.
- If signals above the power supply voltage are applied while the bi-directional buffers are placed in output mode, an input leakage current flows as in ordinary input/output buffers. The same applies when pull-up resistors above the power supply voltage exist outside the chip.
  (If a High logic level above the power supply voltage is needed, use open drain type input/output buffers, with pull-up resistors added external to the chip in order to pull up the logic level High.)

(3) Although the Fail-Safe cells can receive high voltage signals above the LSI's operating voltage, be aware that the signal voltages applied to the Fail-Safe cells must never exceed their rated maximum voltage.

5.2.4.4 List of Cells

Table 5-17 Fail-Safe Input Buffers List

Cell Name*1	Input Level	Whether Pull-up Resistors are Included
XFLIBBP#	CMOS	Pull-up resistor included
XFLIBGP#	CMOS Schmitt	Pull-up resistor included

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 5-3).

Table 5-18 Fail-Safe Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name*1, *2
3-state output	Type 1 Type 2	XFLTBF#T
3-state output for high speed	Type 3	XFLTBF3AT
3-state output for low noise	Type 3	XFLTBF3BT

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 5-9).

*2: In addition to the configurations shown in Table 5-18, the Fail-Safe output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-19 Fail-Safe Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
CMOS	Bi-directional output	Type 1 Type 2	XFLBB#T
	Bi-directional output for high speed	Type 3	XFLBB3AT
	Bi-directional output for low noise	Type 3	XFLBB3BT
CMOS Schmitt	Bi-directional output	Type 1 Type 2	XFLBG#T
	Bi-directional output for high speed	Type 3	XFLBG3AT
	Bi-directional output for low noise	Type 3	XFLBG3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2, respectively (for details, refer to Table 5-9).

*2: In addition to the configurations shown in Table 5-19, the Fail-Safe bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

5.2.5 Gated Cells

5.2.5.1 Overview

The S1X60000 series (XF Type) Gated I/O cell is the first product that allows inputs to pins to be placed in the floating, or High-Z, state without the use of pull-up or pull-down circuits. Moreover, the power supply on the high voltage side (HV_{DD}) can be cut off. There are two types of cells to choose from depending on whether a High-level control signal or Low-level control signal shuts off the power supply. Therefore, customers can choose the desired type of cell according to their circuit design.
(These cells are used as HV_{DD} system cells.)

5.2.5.2 Features

(1) The Gated cells can be positioned as desired by customers. There are no limitations on the number of cells used or the locations in which they are placed. As a result, freedom of design is increased.

(2) It is also possible to cut off the power supply on the high- voltage side (HV_{DD}). However, because special measures must be taken for cut-off, please contact the sales division of Epson.

(3) Inputs can be placed in High-Z state without the use of pull-up or pull-down circuits.

(4) Due to circuit structure, the input level of the Gated I/O cell is not HV_{DD} system but LV_{DD} system CMOS level.

(5) There are two types of cells to choose from depending on whether a High-level control signal or Low-level control signal shuts off the power supply.

(6) Because the Gated cells are completely CMOS structured, the power consumption can be suppressed to a minimum.

5.2.5.3 Usage Precautions

(1) To place inputs in the High-Z state through the use of Gated I/O cells, inputs to pins must be shut off by using Gated I/O cell control signals before they enter the High-Z state. If inputs are placed in the High-Z state without performing this control, large current may flow into the cell as in ordinary cells, causing it to break down. Conversely, the same problem may occur when using Gated I/O cell control to connect inputs (in the High-Z state) to pins. In such a case, the logic level latched into the device's internal circuit cannot be guaranteed.

(2) When the power supply on the high voltage side (HV_{DD}) is to be cut off by using a Gated I/O cell, the same processing as described in (1) is required. This processing must be performed; otherwise, the logic level latched to the device's internal circuit cannot be guaranteed. Moreover, because special measures must be taken for cut off, please contact the sales division of Epson.

5.2.5.4 List of Cells

Table 5-20 Gated Input Buffers List

Cell Name[*1, *2]	Input Level	Whether Pull-up/Pull-down Resistors are Included
XFHIBA XFHIBAP# XFHIBAD#	CMOS (AND Type)	None Pull-up resistor Pull-up included
XFHIBO XFHIBOP# XFHIBOD#	CMOS (OR Type)	None Pull-up resistor Pull-up included

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 5-1).

Table 5-21 Gated Bi-directional Buffers List

Input Level		Function	I_{OH}/I_{OL}	Cell Name[*1, *2]
CMOS	AND Type	Bi-directional output	Type 1 Type 2 Type 3	XFHBA#T
		Bi-directional output for high speed	Type 3	XFHBA3AT
		Bi-directional output for low noise	Type 3	XFHBA3BT
	OR Type	Bi-directional output	Type 1 Type 2 Type 3	XFHBO#T
		Bi-directional output for high speed	Type 3	XFHBO3AT
		Bi-directional output for low noise	Type 3	XFHBO3BT

Notes *1: The # denotes 1, 2, or 3, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, and Type 3, respectively (for details, refer to Table 5-5).

*2: In addition to the configurations shown in Table 5-21, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

5.2.6 5 V Tolerant Fail-Safe Cells

5.2.6.1 Overview

The 5 V tolerant Fail-Safe cells of the S1X60000 series (XF type) allow 5.0 V interfacing without requiring a dedicated power supply.
Moreover, 5.0 V input signals can be received even while the HV_{DD} power supply is cut off, allowing for greater freedom of design than ever. (However, the LV_{DD} power supply must have voltage of 2.5 V or 2.0 V applied to it.)

5.2.6.2 Features

(1) There are no restrictions on the number of cells used or their placement, thus allowing customers to place the cells as required.

(2) Without having to install a dedicated power supply, 5.0 V signals from external sources can be interfaced.

(3) No input leakage current flows even when 5.0 V signals are applied from external sources while the cell is in output mode for High level signal output. Input leakage current does not occur even in input buffers that include pull-up resistors.

(4) No input leakage current occurs even when 5.0 V input signals are applied while the HV_{DD} power supply is cut off. (However, the LV_{DD} power supply must have voltage of 2.5 V or 2.0 V applied to it.)

(5) Two types of cells (one for CMOS level and one for CMOS Schmitt level) have been released.

(6) Because the Fail-Safe cells are completely CMOS-structured, power consumption can be minimized.

5.2.6.3 Usage Precautions

(1) To apply 5.0 V input signals while the HV_{DD} power supply is cut off, always make sure the LV_{DD} power supply has voltage of 2.5 V or 2.0 V applied to it. This is necessary due to the circuit structure of the cell.

(2) About the input I/O cells

- When 5.0 V input signals are to be applied while the HV_{DD} power supply is cut off, control pin “C” must always be pulled Low before 5.0 V input signals are applied.
- In other than cut off mode, the control signal must always be held high. If a Low level input is applied to the cell terminal while the control signal remains at Low levels, current may flow continuously into the input buffer.

(3) About the output I/O cells

- No 5.0 V High level signals are output from the cell due to its circuit structure. Therefore, if 5.0 V outputs are needed, add 5.0 V pull-up resistors external to the chip.

5.2.6.4 List of Cells

Table 5-22 5 V Tolerant Fail-Safe Input Buffers List

Cell Name*1	Input Level	Whether Pull-up/Pull-down Resistors are Included
XFHIBB XFHIBBP# XFHIBBD#	CMOS CMOS CMOS	None Pull-up resistors Pull-down resistors
XFHIBG XFHIBGP# XFHIBGD#	CMOS Schmitt CMOS Schmitt CMOS Schmitt	None Pull-up resistors Pull-down resistors

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 5-1).

Table 5-23 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}*1/I_{OL}*2 (HVDD = 3.3 V)	Unit
Type 1	-3/3	mA
Type 2	-6/6	mA
Type 3	-12/12	mA

Notes *1: $V_{OH} = HV_{DD} - 1.0$ V

*2: $V_{OL} = 0.4$ V

Table 5-24 5 V Tolerant Fail-Safe Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name*1, *2
Normal output	Type 1 Type 2	XFHOBF#T
Normal output for high speed	Type 3	XFHOBF3AT
Normal output for low noise	Type 3	XFHOBF3BT
3-state output	Type 1 Type 2	XFHTBF#T
3-state output for high speed	Type 3	XFHTBF3AT
3-state output for low noise	Type 3	XFHTBF3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2, respectively (for details, refer to Table 5-23).

*2: In addition to the configurations shown in Table 5-24, the 5 V Tolerant Fail-Safe output buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 5-25 5 V Tolerant Fail-Safe Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name*1, *2
CMOS	Bi-directional output	Type 1 Type 2	XFHBB#T
	Bi-directional output for high speed	Type 3	XFHBB3AT
	Bi-directional output for low noise	Type 3	XFHBB3BT
CMOS Schmitt	Bi-directional output	Type 1 Type 2	XFHBG#T
	Bi-directional output for high speed	Type 3	XFHBG3AT
	Bi-directional output for low noise	Type 3	XFHBG3BT

Notes *1: The # denotes 1, or 2, with the I_{OH}/I_{OL} values corresponding to Type 1, and Type 2, respectively (for details, refer to Table 5-23).

*2: In addition to the configurations shown in Table 5-25, the 5 V Tolerant Fail-Safe bi-directional buffers may be configures with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

5.3 Dual Power Supplies Guidelines

The S1X60000 series (XF Type) allows each input/output buffer to be interfaced with 5.0 V, 3.3 V, 2.5 V, or 2.0 V signals as desired, using a dual power supply system. The internal cell area operates using a 2.5 V or 2.0 V single power supply.

5.3.1 Method of Adapting to Dual Power Supplies

In the S1X60000 series (XF Type), it is possible to apply input signals of voltages higher the internal operating voltage using HV_{DD} input buffers. Similarly, high voltage signals above the internal operating voltage can be output using dual power supply output buffers.

5.3.2 Power Supplies for Dual Power Operation

If your circuit is to be operated using two different power supplies, use two power supply cells: HV_{DD} and LV_{DD}. Specifically, HV_{DD} may be used for HV_{DD} input/output buffers, and LV_{DD} may be used for LV_{DD} input/output buffers and internal cells. The power supply voltages must always satisfy the equation below.

$HV_{DD} \geq LV_{DD}$

If $HV_{DD} < LV_{DD}$, operation of the internal circuit cannot be guaranteed. The operating conditions specified below are recommended.

HV_{DD} = 3.3 V, LV_{DD} = 2.5 V
HV_{DD} = 3.3 V, LV_{DD} = 2.0 V

5.3.3 Turning On/Off Dual Power Supplies

For chips designed to dual power supply specifications, make sure the power is turned on and off in the order specified below.

When turning on: LV_{DD} (internal) → HV_{DD} (I/O section) → input signals applied

When turning off: Input signals off → HV_{DD} (I/O section) → LV_{DD} (internal)

Note 1: Avoid keeping only HV_{DD} turned on (for 1 sec or more) while LV_{DD} is turned off, so as not to degrade the chip's reliability.

Note 2: When turning HV_{DD} back on after it was off, always be sure to initialize the circuit following power on. This is necessary to ensure the internal circuit state in the event of power supply noise or the like.

5.3.4 Interface with external devices

See the tables shown below when connecting input/output buffers to external LSIs.

5.3.4.1 When power is supplied to HV_{DD}

Table 5-26 Example of Connection to 3.3 V System LSIs

LSIs to which connected	S1X60000 series	Whether connectable	Remarks
3.3 V system output buffer	3.3 V input buffer	○	—
	5 V tolerant Fail-Safe input buffer	○	—
3.3 V system input buffer	3.3 V output buffer	○	—
	5 V tolerant Fail-Safe output buffer	○	Add a 3.3 V pull-up resistor as necessary.
3.3 V system bi-directional buffer	3.3 V bi-directional buffer	○	—
	5 V tolerant Fail-Safe bi-directional buffer	○	Add a 3.3 V pull-up resistor as necessary.

Table 5-27 Example of Connection to 5.0 V System LSIs

LSIs to which connected	S1X60000 series	Whether connectable	Remarks
5.0 V system output buffer	3.3 V input buffer	×	—
	5 V tolerant Fail-Safe input buffer	○	—
5.0 V system input buffer	3.3 V output buffer	×	However, connection to 5.0 V TTL cells is possible.
	5 V tolerant Fail-Safe output buffer	○	A 5.0 V external pull-up resistor is required. (Not required for 5.0 V TTL cells)
5.0 V system bi-directional buffer	3.3 V bi-directional buffer	×	—
	5 V tolerant Fail-Safe bi-directional buffer	○	A 5.0 V external pull-up resistor is required.

5.3.4.2 When power is not supplied to HV_{DD} (LV_{DD} = 2.5 V or 2.0 V)

Note that the following description assumes a case where signals are supplied from external LSIs to the buffer, even while the HV_{DD} power supply is cut off.

Table 5-28 Example of Connection to 3.3 V System LSIs

LSIs to which connected	S1X60000 series	Whether connectable	Remarks
3.3 V system output buffer	3.3 V input buffer	○	Be sure to use Gated cells. However, input buffers with pull-up resistors cannot be used.
	LV_{DD} Fail-Safe input buffer	○	For input buffers with pull-up resistors, note that input leakage current of about 30 µA will flow.
	5 V tolerant Fail-Safe input buffer	○	—
3.3 V system bi-directional buffer	3.3 V bi-directional buffer	×	—
	5 V tolerant Fail-Safe bi-directional buffer	○	Add a 3.3 V pull-up resistor as necessary.

Table 5-29 Example of Connection to 5.0 V System LSIs

LSIs to which connected	S1X60000 series	Whether connectable	Remarks
5.0 V system output buffer	3.3 V input buffer	×	—
	LV_{DD} Fail-Safe input buffer	×	—
	5 V tolerant Fail-Safe input buffer	○	—
5.0 V system bi-directional buffer	3.3 V bi-directional buffer	×	—
	5 V tolerant Fail-Safe bi-directional buffer	○	A 5.0 V external pull-up resistor is required.

Chapter 6 Memory Blocks

The S1X 60000 Series supports memory blocks.This memory block comes in the following types classified by memory capacity and function:

(1) Basic Cell type RAM (1 port or 2 port), asynchronous type

(2) Basic Cell type RAM (1 port or 2 port), synchronous type

(3) Standard type 1 port RAM, synchronous type

(4) Standard type dual port RAM, synchronous type

(5) High density type 1 port RAM, synchronous type

(6) Mask ROM, synchronous type

6.1 Basic Cell Type RAM (Asynchronous)

The S1X60000 Series supports 1 port RAM and 2 port RAM.

6.1.1 Features

(1) 1 port RAM

- Asynchronous to clock
- Fully static operation
- 1 read/write address port, 1 input data port, 1 output data port
- RAM configurations supported:Word Depth = 16 to 512 (incremental by 16 words) Bit Width = 1 to 64 (incremental by 1 bit)
- Maximum size: 32 K bits/module

(2) 2 port RAM

- Asynchronous to clock
- Fully static operation
- 1 read address port, 1 write address port, 1 input data port, 1 output data port
- RAM configurations supported: Word Depth = 16 to 512 (incremental by 16 words) Bit Width = 1 to 64 (incremental by 1 bit)
- Maximum size: 32 K bits/module

6.1.2 RAM Word/Bit Configuration and Simulation Model Selection

RAM delay parameters change depending on the word/bit structure. Simulation models have been prepared using performance characteristics indicative to the RAM word/bit configuration.

The 1 port RAM and 2 port RAM word/bit structure simulation models are shown in Tables 6-1 and 6-2 respectively.

For RAM with word/bit structures exceeding the limitations in the tables below, use combinations of multiple RAMs.

Table 6-1 Simulation Model Selection Chart (1 port RAM Word/Bit Structure)

Word depth / Bit width	16 to 64	80 to 128	144 to 192	208 to 256	272 to 320	336 to 384	400 to 448	464 to 512
1 to 16	RAM1P1	RAM1P5	RAM1P9	RAM1P13	RAM1P17	RAM1P21	RAM1P25	RAM1P29
17 to 32	RAM1P2	RAM1P6	RAM1P10	RAM1P14	RAM1P18	RAM1P22	RAM1P26	RAM1P30
33 to 48	RAM1P3	RAM1P7	RAM1P11	RAM1P15	RAM1P19	RAM1P23	RAM1P27	RAM1P31
49 to 64	RAM1P4	RAM1P8	RAM1P12	RAM1P16	RAM1P20	RAM1P24	RAM1P28	RAM1P32

Table 6-2 Simulation Model Selection Chart (2 port RAM Word/Bit Structure)

Word depth / Bit width	16 to 64	80 to 128	144 to 192	208 to 256	272 to 320	336 to 384	400 to 448	464 to 512
1 to 16	RAM2P1	RAM2P5	RAM2P9	RAM2P13	RAM2P17	RAM2P21	RAM2P25	RAM2P29
17 to 32	RAM2P2	RAM2P6	RAM2P10	RAM2P14	RAM2P18	RAM2P22	RAM2P26	RAM2P30
33 to 48	RAM2P3	RAM2P7	RAM2P11	RAM2P15	RAM2P19	RAM2P23	RAM2P27	RAM2P31
49 to 64	RAM2P4	RAM2P8	RAM2P12	RAM2P16	RAM2P20	RAM2P24	RAM2P28	RAM2P32

6.1.3 RAM Size

The X direction size, Y direction size, and number of BCs used in the RAM are calculated using the formulas below. The formulas below do not include the interconnect region contained in the RAM.

(1) 1 port RAM

Size in the X direction: $RX = 3 \times Word/2 + 20$

Size in the Y direction: $RY = 2 \times Bit + 12$ $(16 \leq word \leq 256)$

$RY = 2 \times Bit + 13$ $(256 < word \leq 512)$

Number of BCs: $RAMBCS = RX \times RY$

Table 6-3 An Example of the Structure of 1 port RAM and Number of BCs

Bit width / Word depth	8	16	32	64
64	3,248 (116 × 28)	5,104 (116 × 44)	8,816 (116 × 76)	16,240 (116 × 140)
128	5,936 (212 × 28)	9,328 (212 × 44)	16,112 (212 × 76)	29,680 (212 × 140)
256	11,312 (404 × 28)	17,776 (404 × 44)	30,704 (404 × 76)	56,560 (404 × 140)
512	22,852 (788 × 29)	35,460 (788 × 45)	60,676 (788 × 77)	111,108 (788 × 141)

(2) 2 port RAM

Size in the X direction: $RX = 3 \times Word/2 + 20$

Size in the Y direction: $RY = 2 \times Bit + 15$ ($16 \leq word \leq 256$)

$RY = 2 \times Bit + 17$ ($256 < word \leq 512$)

Number of BCs: $RAMBCS = RX \times RY$

Table 6-4 An Example of the Structure of 2 port RAM and Number of BCs

Bit width / Word depth	8	16	32	64
64	3,596 (116 × 31)	5,452 (116 × 47)	9,164 (116 × 79)	16,588 (116 × 143)
128	6,572 (212 × 31)	9,964 (212 × 47)	16,748 (212 × 79)	30,316 (212 × 143)
256	12,524 (404 × 31)	18,988 (404 × 47)	31,916 (404 × 79)	57,772 (404 × 143)
512	26,004 (788 × 33)	38,612 (788 × 49)	63,828 (788 × 81)	114,260 (788 × 145)

6.1.4 Investigating RAM Placement on Master Slice

When investigating RAM placement on a master slice, please insure that sufficient area is available in both the X direction (column) and the Y direction (row). When loading RAM onto a chip, it is necessary to insure that the capacity of the master exceeds the required RAM area in both the X and Y directions.

When multiple RAMs are used, RAM blocks are placed adjacent to each other either horizontally or vertically. The wiring areas around RAM are not included in the equation shown in the previous section. It is therefore not possible to determine the advantages and disadvantages of placing RAM on the master slice based on values obtained by simply adding RXSIZE and RYSIZE to the sizes in the X and Y directions, respectively. As shown in Figure 6-1, add the interconnecting area of Bit/2 BC (round up to the nearest whole number) to X direction and every 1 BC to the upper and lower of Y direction, then the regarding master slice selection should be decided to mount or not.

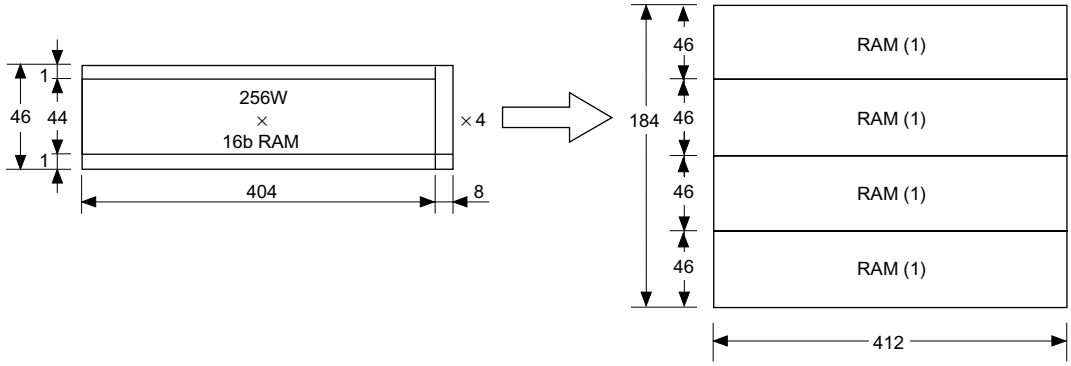


Figure 6-1 Example of RAM Layout

6.1.5 Explanation of Functions

(1) 1 port RAM

Table 6-5-1 1 port RAM Signals

Signal Name	I/O	FUNCTION
CS	IN	Chip select signal, H: RAM active
RW	IN	Read/write signal, H: Read, L: Write
A0, A1, ..., A (m-1)	IN	Read/write address port, A0: LSB
D0, D1, ..., D (n-1)	IN	Data input port, D0: LSB
Y0, Y1, ..., Y (n-1)	OUT	Data output port, Y0: LSB

Table 6-5-2 FI, FO of 1 port RAM

	FI												FO
	A0	**A1**	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**CS**	**RW**	**D***	**Y***
16 to 64	1LU	1LU	1LU	1LU	1LU	1LU				1LU	1LU	2LU	28.9LU
80 to 128	1LU	1LU	1LU	1LU	1LU	1LU	1LU			1LU	1LU	2LU	28.9LU
144 to 256	1LU	2LU	2LU	2LU	1LU	1LU	1LU	1LU		1LU	1LU	2LU	28.9LU
272 to 512	1LU	2LU	2LU	2LU	2LU	2LU	2LU	1LU	1LU	1LU	1LU	2LU	28.9LU

K of Y* corresponds “IN4”

Table 6-6 1 port RAM Truth Table

CS	RW	A0, A1 ... A (m-1)	Y0, Y1 ... Y (n-1)	Mode
0	X	X	Unknown	Wait
1	0	Stable	Unknown	Write
1	1	Stable	Read Data	Read

X: High or Low

- **Data Read**

  The data is read by holding CS at High and RW at High and setting the address.

- **Data Write**

  The data can be written in either of the following two ways:

  (1) Holding CS at High, setting the address, and sending a negative pulse to RW.

  (2) Holding RW at Low, setting the address, and sending a positive pulse to CS.

  When either method is used, the data is latched to the RAM at the trailing edge of the pulse.

- **The Wait State**

  When CS is Low, the 1 port RAM enters a wait state and only maintains the data. The current consumed by the RAM is merely the leakage current, and is almost zero.

(2) 2 port RAM

Table 6-7-1 2 port RAM Signals

Signal Name	I/O	Function
CS	IN	Chip select signal, H: RAM active
RD	IN	Read signal, H: Read enable
WR	IN	Write signal, H: Write enable
RA0, ... RA (m-1)	IN	Read address port, RA0: LSB
WA0, ... WA (m-1)	IN	Write address port, WA0: LSB
D0, D1, ... D (n-1)	IN	Data input port, D0: LSB
Y0, Y1, ... Y (n-1)	OUT	Data output port, Y0: LSB

Table 6-7-2 FI, FO of 2 port RAM

	FI													FO
	RA0/ WA0	RA1/ WA1	RA2/ WA2	RA3/ WA3	RA4/ WA4	RA5/ WA5	RA6/ WA6	RA7/ WA7	RA8/ WA8	CS	RD	WR	D*	Y*
64	1LU	1LU	1LU	1LU	1LU	1LU				1LU	1LU	1LU	2LU	28.9LU
128	1LU	1LU	1LU	1LU	1LU	1LU	1LU			1LU	1LU	1LU	2LU	28.9LU
256	1LU	2LU	2LU	2LU	1LU	1LU	1LU	1LU		1LU	1LU	1LU	2LU	28.9LU
512	1LU	2LU	2LU	2LU	2LU	2.1LU	2LU	1LU	1LU	1LU	1LU	1LU	2LU	28.9LU

K of Y* corresponds "IN4"

Table 6-8 2 port RAM Truth Table

CS	RD	WR	RA0, ... RA (n-1)	WA0, ..., WA (m-1)	Y0, ... Y (n-1)	Mode
0	X	X	X	X	Unknown	Wait
1	0	0	X	X	Unknown	Wait
1	0	1	X	Stable	Unknown	Write
1	1	0	Stable	X	Read Data	Read
1	1	1	Stable	Stable	Read Data	Read & Write

X: High or Low

- **Data Read**

The data is read by holding CS at High and RD at High and setting the read address.

- **Data Write**

The data can be written in either of the following two ways:

(1) Holding CS at High, setting the write address, and sending a positive pulse to WR.

(2) Holding WR at High, setting the write address, and sending a positive pulse to CS.

- **Data Read/Write**

When reading is done at the same time as writing, it is possible by performing the respective methods simultaneously. However, these two operations cannot be performed simultaneously on the same address. The read cycle access time described at Section 6.1.6 applies to data for which the writing has already been completed.

- **The Wait State**

The 2 port RAM enters a wait state in either of the situations below, and does nothing but maintain its data. The current consumed by the RAM is merely the leakage current, and is almost 0.

(1) CS is Low.

(2) CS is High, RD is Low, and WR is Low.

6.1.6 Delay Parameters

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-9 1 port/2 port RAM Read Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	4.605	—	5.239	—	5.519	—	6.203	—	ns
Address access time	t_{ACC}	—	4.605	—	5.239	—	5.519	—	6.203	
CS access time	t_{ACS}	—	4.605	—	5.239	—	5.519	—	6.203	
RW access time	t_{ARW}	—	4.605	—	5.239	—	5.519	—	6.203	
CS active time	t_{RCS}	4.605	—	5.239	—	5.519	—	6.203	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

Table 6-9 1 port/2 port RAM Read Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	5.668	—	6.302	—	6.581	—	7.266	—	ns
Address access time	t_{ACC}	—	5.668	—	6.302	—	6.581	—	7.266	
CS access time	t_{ACS}	—	5.668	—	6.302	—	6.581	—	7.266	
RW access time	t_{ARW}	—	5.668	—	6.302	—	6.581	—	7.266	
CS active time	t_{RCS}	5.668	—	6.302	—	6.581	—	7.266	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-9 1 port/2 port RAM Read Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.731	—	7.365	—	7.644	—	8.328	—	ns
Address access time	t_{ACC}	—	6.731	—	7.365	—	7.644	—	8.328	
CS access time	t_{ACS}	—	6.731	—	7.365	—	7.644	—	8.328	
RW access time	t_{ARW}	–	6.731	—	7.365	—	7.644	—	8.328	
CS active time	t_{RCS}	6.731	—	7.365	—	7.644	—	8.328	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

Table 6-9 1 port/2 port RAM Read Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	7.794	—	8.428	—	8.707	—	9.391	—	ns
Address access time	t_{ACC}	—	7.794	—	8.428	—	8.707	—	9.391	
CS access time	t_{ACS}	—	7.794	—	8.428	—	8.707	—	9.391	
RW access time	t_{ARW}	—	7.794	—	8.428	—	8.707	—	9.391	
CS active time	t_{RCS}	7.794	—	8.428	—	8.707	—	9.391	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-9 1 port/2 port RAM Read Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	8.856	—	9.490	—	9.770	—	10.454	—	ns
Address access time	t_{ACC}	—	8.856	—	9.490	—	9.770	—	10.454	
CS access time	t_{ACS}	—	8.856	—	9.490	—	9.770	—	10.454	
RW access time	t_{ARW}	–	8.856	—	9.490	—	9.770	—	10.454	
CS active time	t_{RCS}	8.856	—	9.490	—	9.770	—	10.454	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

Table 6-9 1 port/2 port RAM Read Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	9.919	—	10.553	—	10.832	—	11.517	—	ns
Address access time	t_{ACC}	—	9.919	—	10.553	—	10.832	—	11.517	
CS access time	t_{ACS}	—	9.919	—	10.553	—	10.832	—	11.517	
RW access time	t_{ARW}	—	9.919	—	10.553	—	10.832	—	11.517	
CS active time	t_{RCS}	9.919	—	10.553	—	10.832	—	11.517	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-9 1 port/2 port RAM Read Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	10.982	—	11.616	—	11.895	—	12.579	—	ns
Address access time	t_{ACC}	—	10.982	—	11.616	—	11.895	—	12.579	
CS access time	t_{ACS}	—	10.982	—	11.616	—	11.895	—	12.579	
RW access time	t_{ARW}	–	10.982	—	11.616	—	11.895	—	12.579	
CS active time	t_{RCS}	10.982	—	11.616	—	11.895	—	12.579	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

Table 6-9 1 port/2 port RAM Read Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	12.045	—	12.679	—	12.958	—	13.642	—	ns
Address access time	t_{ACC}	—	12.045	—	12.679	—	12.958	—	13.642	
CS access time	t_{ACS}	—	12.045	—	12.679	—	12.958	—	13.642	
RW access time	t_{ARW}	—	12.045	—	12.679	—	12.958	—	13.642	
CS active time	t_{RCS}	12.045	—	12.679	—	12.958	—	13.642	—	
Output hold time after address change	t_{OH}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after CS disable	t_{OHCS}	0.093	—	0.153	—	0.212	—	0.272	—	
Output hold time after RW disable	t_{OHRW}	0.093	—	0.153	—	0.212	—	0.272	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-10 1 port/2 port RAM Write Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	2.776	—	3.624	—	4.520	—	5.396	—	ns
Write pulse width	t_{WP}	1.347	—	2.223	—	3.101	—	3.977	—	
CS active time	t_{WCS}	1.347	—	2.223	—	3.101	—	3.977	—	
Address setup time	t_{AS}	0.481	—	0.481	—	0.481	—	0.481	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.671	—	2.374	—	3.078	—	3.781	—	

Table 6-10 1 port/2 port RAM Write Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	2.924	—	3.799	—	4.677	—	5.553	—	ns
Write pulse width	t_{WP}	1.425	—	2.300	—	3.178	—	4.054	—	
CS active time	t_{WCS}	1.425	—	2.300	—	3.178	—	4.054	—	
Address setup time	t_{AS}	0.561	—	0.561	—	0.561	—	0.561	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.731	—	2.434	—	3.138	—	3.841	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-10 1 port/2 port RAM Write Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.092	—	3.968	—	4.846	—	5.722	—	ns
Write pulse width	t_{WP}	1.513	—	2.389	—	3.267	—	4.143	—	
CS active time	t_{WCS}	1.513	—	2.389	—	3.267	—	4.143	—	
Address setup time	t_{AS}	0.641	—	0.641	—	0.641	—	0.641	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.791	—	2.495	—	3.198	—	3.901	—	

Table 6-10 1 port/2 port RAM Write Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.273	—	4.148	—	5.026	—	5.902	—	ns
Write pulse width	t_{WP}	1.614	—	2.489	—	3.367	—	4.243	—	
CS active time	t_{WCS}	1.614	—	2.489	—	3.367	—	4.243	—	
Address setup time	t_{AS}	0.721	—	0.721	—	0.721	—	0.721	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.851	—	2.555	—	3.258	—	3.961	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-10 1 port/2 port RAM Write Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.397	—	4.272	—	5.150	—	6.026	—	ns
Write pulse width	t_{WP}	1.679	—	2.554	—	3.432	—	4.308	—	
CS active time	t_{WCS}	1.679	—	2.554	—	3.432	—	4.308	—	
Address setup time	t_{AS}	0.780	—	0.780	—	0.780	—	0.780	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.895	—	2.593	—	3.296	—	4.000	—	

Table 6-10 1 port/2 port RAM Write Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.558	—	4.443	—	5.311	—	6.188	—	ns
Write pulse width	t_{WP}	1.764	—	2.639	—	3.517	—	4.394	—	
CS active time	t_{WCS}	1.764	—	2.639	—	3.517	—	4.394	—	
Address setup time	t_{AS}	0.856	—	0.856	—	0.856	—	0.856	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.952	—	2.650	—	3.353	—	4.057	—	

(1) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C)

Table 6-10 1 port/2 port RAM Write Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.720	—	4.595	—	5.473	—	6.349	—	ns
Write pulse width	t_{WP}	1.850	—	2.725	—	3.603	—	4.479	—	
CS active time	t_{WCS}	1.850	—	2.725	—	3.603	—	4.479	—	
Address setup time	t_{AS}	0.932	—	0.932	—	0.932	—	0.932	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.009	—	2.707	—	3.410	—	4.113	—	

Table 6-10 1 port/2 port RAM Write Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.880	—	4.755	—	5.633	—	6.509	—	ns
Write pulse width	t_{WP}	1.935	—	2.810	—	3.688	—	4.564	—	
CS active time	t_{WCS}	1.935	—	2.810	—	3.688	—	4.564	—	
Address setup time	t_{AS}	1.007	—	1.007	—	1.007	—	1.007	—	
Address hold time	t_V	0.938	—	0.938	—	0.938	—	0.938	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.066	—	2.764	—	3.467	—	4.170	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-11 1 port/2 port RAM Read Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	4.356	—	4.956	—	5.220	—	5.868	—	ns
Address access time	t_{ACC}	—	4.356	—	4.956	—	5.220	—	5.868	
CS access time	t_{ACS}	—	4.356	—	4.956	—	5.220	—	5.868	
RW access time	t_{ARW}	—	4.356	—	4.956	—	5.220	—	5.868	
CS active time	t_{RCS}	4.356	—	4.956	—	5.220	—	5.868	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

Table 6-11 1 port/2 port RAM Read Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	5.362	—	5.961	—	6.226	—	6.873	—	ns
Address access time	t_{ACC}	—	5.362	—	5.961	—	6.226	—	6.873	
CS access time	t_{ACS}	—	5.362	—	5.961	—	6.226	—	6.873	
RW access time	t_{ARW}	—	5.362	—	5.961	—	6.226	—	6.873	
CS active time	t_{RCS}	5.362	—	5.961	—	6.226	—	6.873	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-11 1 port/2 port RAM Read Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.367	—	6.967	—	7.231	—	7.878	—	ns
Address access time	t_{ACC}	—	6.367	—	6.967	—	7.231	—	7.878	
CS access time	t_{ACS}	—	6.367	—	6.967	—	7.231	—	7.878	
RW access time	t_{ARW}	—	6.367	—	6.967	—	7.231	—	7.878	
CS active time	t_{RCS}	6.367	—	6.967	—	7.231	—	7.878	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

Table 6-11 1 port/2 port RAM Read Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	7.372	—	7.972	—	8.236	—	8.884	—	ns
Address access time	t_{ACC}	—	7.372	—	7.972	—	8.236	—	8.884	
CS access time	t_{ACS}	—	7.372	—	7.972	—	8.236	—	8.884	
RW access time	t_{ARW}	—	7.372	—	7.972	—	8.236	—	8.884	
CS active time	t_{RCS}	7.372	—	7.972	—	8.236	—	8.884	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-11 1 port/2 port RAM Read Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	8.378	—	8.977	—	9.242	—	9.889	—	ns
Address access time	t_{ACC}	—	8.378	—	8.977	—	9.242	—	9.889	
CS access time	t_{ACS}	—	8.378	—	8.977	—	9.242	—	9.889	
RW access time	t_{ARW}	—	8.378	—	8.977	—	9.242	—	9.889	
CS active time	t_{RCS}	8.378	—	8.977	—	9.242	—	9.889	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

Table 6-11 1 port/2 port RAM Read Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	9.383	—	9.983	—	10.247	—	10.894	—	ns
Address access time	t_{ACC}	—	9.383	—	9.983	—	10.247	—	10.894	
CS access time	t_{ACS}	—	9.383	—	9.983	—	10.247	—	10.894	
RW access time	t_{ARW}	—	9.383	—	9.983	—	10.247	—	10.894	
CS active time	t_{RCS}	9.383	—	9.983	—	10.247	—	10.894	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-11 1 port/2 port RAM Read Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	10.388	—	10.988	—	11.252	—	11.900	—	ns
Address access time	t_{ACC}	—	10.388	—	10.988	—	11.252	—	11.900	
CS access time	t_{ACS}	—	10.388	—	10.988	—	11.252	—	11.900	
RW access time	t_{ARW}	—	10.388	—	10.988	—	11.252	—	11.900	
CS active time	t_{RCS}	10.388	—	10.988	—	11.252	—	11.900	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

Table 6-11 1 port/2 port RAM Read Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	11.394	—	11.993	—	12.257	—	12.905	—	ns
Address access time	t_{ACC}	—	11.394	—	11.993	—	12.257	—	12.905	
CS access time	t_{ACS}	—	11.394	—	11.993	—	12.257	—	12.905	
RW access time	t_{ARW}	—	11.394	—	11.993	—	12.257	—	12.905	
CS active time	t_{RCS}	11.394	—	11.993	—	12.257	—	12.905	—	
Output hold time after address change	t_{OH}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after CS disable	t_{OHCS}	0.099	—	0.163	—	0.226	—	0.289	—	
Output hold time after RW disable	t_{OHRW}	0.099	—	0.163	—	0.226	—	0.289	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-12 1 port/2 port RAM Write Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	2.617	—	3.444	—	4.275	—	5.104	—	ns
Write pulse width	t_{WP}	1.275	—	2.102	—	2.933	—	3.762	—	
CS active time	t_{WCS}	1.275	—	2.102	—	2.933	—	3.762	—	
Address setup time	t_{AS}	0.455	—	0.455	—	0.455	—	0.455	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.581	—	2.246	—	2.911	—	3.577	—	

Table 6-12 1 port/2 port RAM Write Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	2.766	—	3.594	—	4.424	—	5.253	—	ns
Write pulse width	t_{WP}	1.348	—	2.176	—	3.006	—	3.835	—	
CS active time	t_{WCS}	1.348	—	2.176	—	3.006	—	3.835	—	
Address setup time	t_{AS}	0.531	—	0.531	—	0.531	—	0.531	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.638	—	2.303	—	2.968	—	3.633	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-12 1 port/2 port RAM Write Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	2.926	—	3.754	—	4.584	—	5.413	—	ns
Write pulse width	t_{WP}	1.432	—	2.260	—	3.090	—	3.919	—	
CS active time	t_{WCS}	1.432	—	2.260	—	3.090	—	3.919	—	
Address setup time	t_{AS}	0.607	—	0.607	—	0.607	—	0.607	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.694	—	2.360	—	3.025	—	3.690	—	

Table 6-12 1 port/2 port RAM Write Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.096	—	3.923	—	4.754	—	5.583	—	ns
Write pulse width	t_{WP}	1.527	—	2.354	—	3.185	—	4.014	—	
CS active time	t_{WCS}	1.527	—	2.354	—	3.185	—	4.014	—	
Address setup time	t_{AS}	0.682	—	0.682	—	0.682	—	0.682	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.751	—	2.416	—	3.082	—	3.747	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-12 1 port/2 port RAM Write Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.213	—	4.041	—	4.872	—	5.701	—	ns
Write pulse width	t_{WP}	1.588	—	2.416	—	3.247	—	4.076	—	
CS active time	t_{WCS}	1.588	—	2.416	—	3.247	—	4.076	—	
Address setup time	t_{AS}	0.738	—	0.738	—	0.738	—	0.738	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.793	—	2.453	—	3.118	—	3.784	—	

Table 6-12 1 port/2 port RAM Write Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.366	—	4.194	—	5.024	—	5.853	—	ns
Write pulse width	t_{WP}	1.669	—	2.497	—	3.327	—	4.156	—	
CS active time	t_{WCS}	1.669	—	2.497	—	3.327	—	4.156	—	
Address setup time	t_{AS}	0.810	—	0.810	—	0.810	—	0.810	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.847	—	2.507	—	3.172	—	3.837	—	

(2) 2.5 V Specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C)

Table 6-12 1 port/2 port RAM Write Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.518	—	4.345	—	5.176	—	6.005	—	ns
Write pulse width	t_{WP}	1.750	—	2.577	—	3.408	—	4.237	—	
CS active time	t_{WCS}	1.750	—	2.577	—	3.408	—	4.237	—	
Address setup time	t_{AS}	0.881	—	0.881	—	0.881	—	0.881	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.900	—	2.560	—	3.226	—	3.891	—	

Table 6-12 1 port/2 port RAM Write Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	3.670	—	4.498	—	5.329	—	6.157	—	ns
Write pulse width	t_{WP}	1.830	—	2.658	—	3.489	—	4.317	—	
CS active time	t_{WCS}	1.830	—	2.658	—	3.489	—	4.317	—	
Address setup time	t_{AS}	0.953	—	0.953	—	0.953	—	0.953	—	
Address hold time	t_{AH}	0.887	—	0.887	—	0.887	—	0.887	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	1.954	—	2.614	—	3.280	—	3.945	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-13 1 port/2 port RAM Read Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.804	—	7.736	—	8.134	—	9.109	—	ns
Address access time	t_{ACC}	—	6.804	—	7.736	—	8.134	—	9.109	
CS access time	t_{ACS}	—	6.804	—	7.736	—	8.134	—	9.109	
RW access time	t_{ARW}	—	6.804	—	7.736	—	8.134	—	9.109	
CS active time	t_{RCS}	6.804	—	7.736	—	8.134	—	9.109	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

Table 6-13 1 port/2 port RAM Read Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	8.450	—	9.382	—	9.781	—	10.755	—	ns
Address access time	t_{ACC}	—	8.450	—	9.382	—	9.781	—	10.755	
CS access time	t_{ACS}	—	8.450	—	9.382	—	9.781	—	10.755	
RW access time	t_{ARW}	—	8.450	—	9.382	—	9.781	—	10.755	
CS active time	t_{RCS}	8.450	—	9.382	—	9.781	—	10.755	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-13 1 port/2 port RAM Read Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	10.096	—	11.028	—	11.427	—	12.402	—	ns
Address access time	t_{ACC}	—	10.096	—	11.028	—	11.427	—	12.402	
CS access time	t_{ACS}	—	10.096	—	11.028	—	11.427	—	12.402	
RW access time	t_{ARW}	—	10.096	—	11.028	—	11.427	—	12.402	
CS active time	t_{RCS}	10.096	—	11.028	—	11.427	—	12.402	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

Table 6-13 1 port/2 port RAM Read Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	11.743	—	12.675	—	13.074	—	14.048	—	ns
Address access time	t_{ACC}	—	11.743	—	12.675	—	13.074	—	14.048	
CS access time	t_{ACS}	—	11.743	—	12.675	—	13.074	—	14.048	
RW access time	t_{ARW}	—	11.743	—	12.675	—	13.074	—	14.048	
CS active time	t_{RCS}	11.743	—	12.675	—	13.074	—	14.048	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-13 1 port/2 port RAM Read Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	13.389	—	14.321	—	14.720	—	15.694	—	ns
Address access time	t_{ACC}	—	13.389	—	14.321	—	14.720	—	15.694	
CS access time	t_{ACS}	—	13.389	—	14.321	—	14.720	—	15.694	
RW access time	t_{ARW}	—	13.389	—	14.321	—	14.720	—	15.694	
CS active time	t_{RCS}	13.389	—	14.321	—	14.720	—	15.694	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

Table 6-13 1 port/2 port RAM Read Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	15.036	—	15.967	—	16.366	—	17.341	—	ns
Address access time	t_{ACC}	—	15.036	—	15.967	—	16.366	—	17.341	
CS access time	t_{ACS}	—	15.036	—	15.967	—	16.366	—	17.341	
RW access time	t_{ARW}	—	15.036	—	15.967	—	16.366	—	17.341	
CS active time	t_{RCS}	15.036	—	15.967	—	16.366	—	17.341	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-13 1 port/2 port RAM Read Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	16.682	—	17.614	—	18.013	—	18.987	—	ns
Address access time	t_{ACC}	—	16.682	—	17.614	—	18.013	—	18.987	
CS access time	t_{ACS}	—	16.682	—	17.614	—	18.013	—	18.987	
RW access time	t_{ARW}	—	16.682	—	17.614	—	18.013	—	18.987	
CS active time	t_{RCS}	16.682	—	17.614	—	18.013	—	18.987	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

Table 6-13 1 port/2 port RAM Read Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	18.328	—	19.260	—	19.659	—	20.633	—	ns
Address access time	t_{ACC}	—	18.328	—	19.260	—	19.659	—	20.633	
CS access time	t_{ACS}	—	18.328	—	19.260	—	19.659	—	20.633	
RW access time	t_{ARW}	—	18.328	—	19.260	—	19.659	—	20.633	
CS active time	t_{RCS}	18.328	—	19.260	—	19.659	—	20.633	—	
Output hold time after address change	t_{OH}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after CS disable	t_{OHCS}	0.182	—	0.257	—	0.332	—	0.407	—	
Output hold time after RW disable	t_{OHRW}	0.182	—	0.257	—	0.332	—	0.407	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-14 1 port/2 port RAM Write Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	4.807	—	6.341	—	7.878	—	9.413	—	ns
Write pulse width	t_{WP}	2.720	—	4.254	—	5.791	—	7.326	—	
CS active time	t_{WCS}	2.720	—	4.254	—	5.791	—	7.326	—	
Address setup time	t_{AS}	0.696	—	0.696	—	0.696	—	0.696	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.652	—	3.712	—	4.773	—	5.834	—	

Table 6-14 1 port/2 port RAM Write Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.008	—	6.542	—	8.079	—	9.614	—	ns
Write pulse width	t_{WP}	2.822	—	4.356	—	5.893	—	7.428	—	
CS active time	t_{WCS}	2.822	—	4.356	—	5.893	—	7.428	—	
Address setup time	t_{AS}	0.795	—	0.795	—	0.795	—	0.795	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.744	—	3.804	—	4.866	—	5.926	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-14 1 port/2 port RAM Write Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.238	—	6.772	—	8.309	—	9.844	—	ns
Write pulse width	t_{WP}	2.953	—	4.487	—	6.024	—	7.559	—	
CS active time	t_{WCS}	2.953	—	4.487	—	6.024	—	7.559	—	
Address setup time	t_{AS}	0.894	—	0.894	—	0.894	—	0.894	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.836	—	3.897	—	4.958	—	6.019	—	

Table 6-14 1 port/2 port RAM Write Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.497	—	7.031	—	8.568	—	10.103	—	ns
Write pulse width	t_{WP}	3.113	—	4.647	—	6.184	—	7.719	—	
CS active time	t_{WCS}	3.113	—	4.647	—	6.184	—	7.719	—	
Address setup time	t_{AS}	0.993	—	0.993	—	0.993	—	0.993	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.928	—	3.989	—	5.050	—	6.111	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-14 1 port/2 port RAM Write Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.711	—	7.245	—	8.752	—	10.317	—	ns
Write pulse width	t_{WP}	3.223	—	4.757	—	6.294	—	7.829	—	
CS active time	t_{WCS}	3.223	—	4.757	—	6.294	—	7.829	—	
Address setup time	t_{AS}	1.097	—	1.097	—	1.097	—	1.097	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	3.009	—	4.069	—	5.131	—	6.191	—	

Table 6-14 1 port/2 port RAM Write Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.941	—	7.475	—	9.012	—	10.547	—	ns
Write pulse width	t_{WP}	3.353	—	4.887	—	6.424	—	7.959	—	
CS active time	t_{WCS}	3.353	—	4.887	—	6.424	—	7.959	—	
Address setup time	t_{AS}	1.197	—	1.197	—	1.197	—	1.197	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	3.098	—	4.159	—	5.220	—	6.281	—	

(3) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C)

Table 6-14 1 port/2 port RAM Write Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	6.171	—	7.705	—	9.242	—	10.777	—	ns
Write pulse width	t_{WP}	3.483	—	5.017	—	6.554	—	8.089	—	
CS active time	t_{WCS}	3.483	—	5.017	—	6.554	—	8.089	—	
Address setup time	t_{AS}	1.297	—	1.297	—	1.297	—	1.297	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	3.188	—	4.249	—	5.310	—	6.371	—	

Table 6-14 1 port/2 port RAM Write Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	6.400	—	7.934	—	9.471	—	11.006	—	ns
Write pulse width	t_{WP}	3.613	—	5.147	—	6.684	—	8.219	—	
CS active time	t_{WCS}	3.613	—	5.147	—	6.684	—	8.219	—	
Address setup time	t_{AS}	1.396	—	1.396	—	1.396	—	1.396	—	
Address hold time	t_{AH}	1.391	—	1.391	—	1.391	—	1.391	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	3.278	—	4.339	—	5.400	—	6.461	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-15 1 port/2 port RAM Read Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	6.455	—	7.339	—	7.717	—	8.642	—	ns
Address access time	t_{ACC}	—	6.455	—	7.339	—	7.717	—	8.642	
CS access time	t_{ACS}	—	6.455	—	7.339	—	7.717	—	8.642	
RW access time	t_{ARW}	—	6.455	—	7.339	—	7.717	—	8.642	
CS active time	t_{RCS}	6.455	—	7.339	—	7.717	—	8.642	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

Table 6-15 1 port/2 port RAM Read Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	8.017	—	8.901	—	9.279	—	10.204	—	ns
Address access time	t_{ACC}	—	8.017	—	8.901	—	9.279	—	10.204	
CS access time	t_{ACS}	—	8.017	—	8.901	—	9.279	—	10.204	
RW access time	t_{ARW}	—	8.017	—	8.901	—	9.279	—	10.204	
CS active time	t_{RCS}	8.017	—	8.901	—	9.279	—	10.204	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-15 1 port/2 port RAM Read Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	9.579	—	10.463	—	10.841	—	11.766	—	ns
Address access time	t_{ACC}	—	9.579	—	10.463	—	10.841	—	11.766	
CS access time	t_{ACS}	—	9.579	—	10.463	—	10.841	—	11.766	
RW access time	t_{ARW}	—	9.579	—	10.463	—	10.841	—	11.766	
CS active time	t_{RCS}	9.579	—	10.463	—	10.841	—	11.766	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

Table 6-15 1 port/2 port RAM Read Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	11.141	—	12.025	—	12.403	—	13.328	—	ns
Address access time	t_{ACC}	—	11.141	—	12.025	—	12.403	—	13.328	
CS access time	t_{ACS}	—	11.141	—	12.025	—	12.403	—	13.328	
RW access time	t_{ARW}	—	11.141	—	12.025	—	12.403	—	13.328	
CS active time	t_{RCS}	11.141	—	12.025	—	12.403	—	13.328	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-15 1 port/2 port RAM Read Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	12.703	—	13.587	—	13.965	—	14.889	—	ns
Address access time	t_{ACC}	—	12.703	—	13.587	—	13.965	—	14.889	
CS access time	t_{ACS}	—	12.703	—	13.587	—	13.965	—	14.889	
RW access time	t_{ARW}	—	12.703	—	13.587	—	13.965	—	14.889	
CS active time	t_{RCS}	12.703	—	13.587	—	13.965	—	14.889	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

Table 6-15 1 port/2 port RAM Read Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	14.264	—	15.149	—	15.527	—	16.451	—	ns
Address access time	t_{ACC}	—	14.264	—	15.149	—	15.527	—	16.451	
CS access time	t_{ACS}	—	14.264	—	15.149	—	15.527	—	16.451	
RW access time	t_{ARW}	—	14.264	—	15.149	—	15.527	—	16.451	
CS active time	t_{RCS}	14.264	—	15.149	—	15.527	—	16.451	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-15 1 port/2 port RAM Read Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	15.826	—	16.711	—	17.089	—	18.013	—	ns
Address access time	t_{ACC}	—	15.826	—	16.711	—	17.089	—	18.013	
CS access time	t_{ACS}	—	15.826	—	16.711	—	17.089	—	18.013	
RW access time	t_{ARW}	—	15.826	—	16.711	—	17.089	—	18.013	
CS active time	t_{RCS}	15.826	—	16.711	—	17.089	—	18.013	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

Table 6-15 1 port/2 port RAM Read Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle	t_{RC}	17.388	—	18.272	—	18.651	—	19.575	—	ns
Address access time	t_{ACC}	—	17.388	—	18.272	—	18.651	—	19.575	
CS access time	t_{ACS}	—	17.388	—	18.272	—	18.651	—	19.575	
RW access time	t_{ARW}	—	17.388	—	18.272	—	18.651	—	19.575	
CS active time	t_{RCS}	17.388	—	18.272	—	18.651	—	19.575	—	
Output hold time after address change	t_{OH}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after CS disable	t_{OHCS}	0.192	—	0.271	—	0.351	—	0.430	—	
Output hold time after RW disable	t_{OHRW}	0.192	—	0.271	—	0.351	—	0.430	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-16 1 port/2 port RAM Write Cycle (1/8)

Parameter	Signal	RAM1P1/ RAM2P1		RAM1P2/ RAM2P2		RAM1P3/ RAM2P3		RAM1P4/ RAM2P4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	4.560	—	6.016	—	7.474	—	8.930	—	ns
Write pulse width	t_{WP}	2.580	—	4.036	—	5.494	—	6.950	—	
CS active time	t_{WCS}	2.580	—	4.036	—	5.494	—	6.950	—	
Address setup time	t_{AS}	0.661	—	0.661	—	0.661	—	0.661	—	
Address hold time	t_V	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.516	—	3.522	—	4.529	—	5.535	—	

Table 6-16 1 port/2 port RAM Write Cycle (2/8)

Parameter	Signal	RAM1P5/ RAM2P5		RAM1P6/ RAM2P6		RAM1P7/ RAM2P7		RAM1P8/ RAM2P8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	4.750	—	6.206	—	7.664	—	9.120	—	ns
Write pulse width	t_{WP}	2.677	—	4.133	—	5.591	—	7.047	—	
CS active time	t_{WCS}	2.677	—	4.133	—	5.591	—	7.047	—	
Address setup time	t_{AS}	0.754	—	0.754	—	0.754	—	0.754	—	
Address hold time	t_V	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.603	—	3.609	—	4.616	—	5.623	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-16 1 port/2 port RAM Write Cycle (3/8)

Parameter	Signal	RAM1P9/ RAM2P9		RAM1P10/ RAM2P10		RAM1P11/ RAM2P11		RAM1P12/ RAM2P12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	4.969	—	6.424	—	7.882	—	9.338	—	ns
Write pulse width	t_{WP}	2.802	—	4.257	—	5.715	—	7.171	—	
CS active time	t_{WCS}	2.802	—	4.257	—	5.715	—	7.171	—	
Address setup time	t_{AS}	0.848	—	0.848	—	0.848	—	0.848	—	
Address hold time	t_{AH}	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.691	—	3.697	—	4.704	—	5.710	—	

Table 6-16 1 port/2 port RAM Write Cycle (4/8)

Parameter	Signal	RAM1P13/ RAM2P13		RAM1P14/ RAM2P14		RAM1P15/ RAM2P15		RAM1P16/ RAM2P16		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.214	—	6.670	—	8.128	—	9.584	—	ns
Write pulse width	t_{WP}	2.953	—	4.409	—	5.867	—	7.323	—	
CS active time	t_{WCS}	2.953	—	4.409	—	5.867	—	7.323	—	
Address setup time	t_{AS}	0.942	—	0.942	—	0.942	—	0.942	—	
Address hold time	t_{AH}	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.778	—	3.784	—	4.791	—	5.798	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-16 1 port/2 port RAM Write Cycle (5/8)

Parameter	Signal	RAM1P17/ RAM2P17		RAM1P18/ RAM2P18		RAM1P19/ RAM2P19		RAM1P20/ RAM2P20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5,418	—	6.873	—	8.331	—	9.788	—	ns
Write pulse width	t_{WP}	3.058	—	4.513	—	5,971	—	7.428	—	
CS active time	t_{WCS}	3.058	—	4.513	—	5,971	—	7.428	—	
Address setup time	t_{AS}	1.041	—	1.041	—	1.041	—	1.041	—	
Address hold time	t_{AH}	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.854	—	3.860	—	4.867	—	5.874	—	

Table 6-16 1 port/2 port RAM Write Cycle (6/8)

Parameter	Signal	RAM1P21/ RAM2P21		RAM1P22/ RAM2P22		RAM1P23/ RAM2P23		RAM1P24/ RAM2P24		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.635	—	7.091	—	8.549	—	10.005	—	ns
Write pulse width	t_{WP}	3.181	—	4.637	—	6.095	—	7.551	—	
CS active time	t_{WCS}	3.181	—	4.637	—	6.095	—	7.551	—	
Address setup time	t_{AS}	1.135	—	1.135	—	1.135	—	1.135	—	
Address hold time	t_{AH}	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	2.940	—	3.946	—	4.953	—	5.959	—	

(4) 2.0 V Specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C)

Table 6-16 1 port/2 port RAM Write Cycle (7/8)

Parameter	Signal	RAM1P25/ RAM2P25		RAM1P26/ RAM2P26		RAM1P27/ RAM2P27		RAM1P28/ RAM2P28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	5.853	—	7.309	—	8.767	—	10.223	—	ns
Write pulse width	t_{WP}	3.304	—	4.760	—	6.218	—	7.674	—	
CS active time	tV	3.304	—	4.760	—	6.218	—	7.674	—	
Address setup time	tV	1.230	—	1.230	—	1.230	—	1.230	—	
Address hold time	t_{AH}	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{DS}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	tV	3.025	—	4.031	—	5.038	—	6.044	—	

Table 6-16 1 port/2 port RAM Write Cycle (8/8)

Parameter	Signal	RAM1P29/ RAM2P29		RAM1P30/ RAM2P30		RAM1P31/ RAM2P31		RAM1P32/ RAM2P32		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle	t_{WC}	6.071	—	7.527	—	8.985	—	10.441	—	ns
Write pulse width	t_{WP}	3.427	—	4.883	—	6.341	—	7.797	—	
CS active time	t_{WCS}	3.427	—	4.883	—	6.341	—	7.797	—	
Address setup time	t_{AS}	1.325	—	1.325	—	1.325	—	1.325	—	
Address hold time	t_{AH}	1.319	—	1.319	—	1.319	—	1.319	—	
Data setup time	t_{D}S	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	3.110	—	4.116	—	5.123	—	6.130	—	

6.1.7 Timing Charts

(1) 1 port RAM

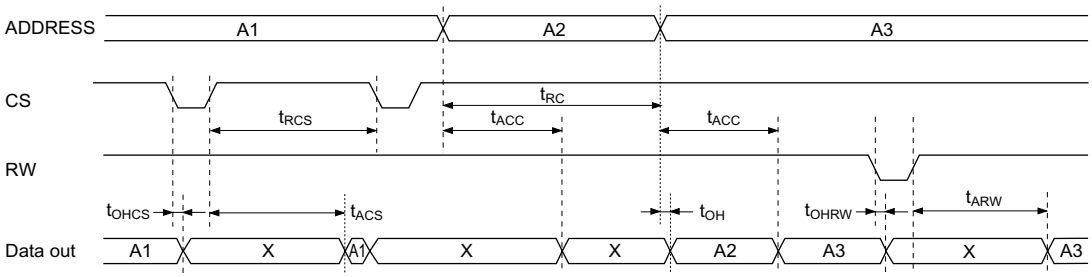


Figure 6-2 Read Cycle

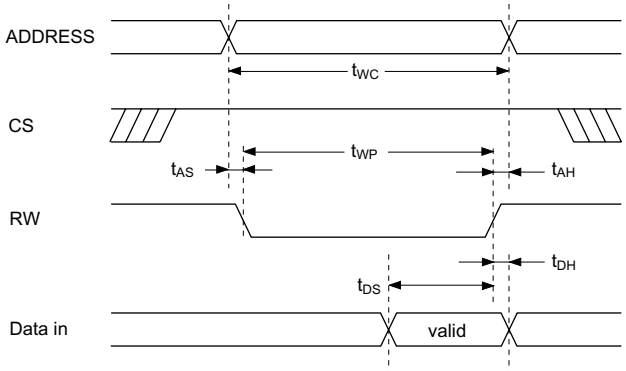


Figure 6-3 Write Cycle (RW Control)

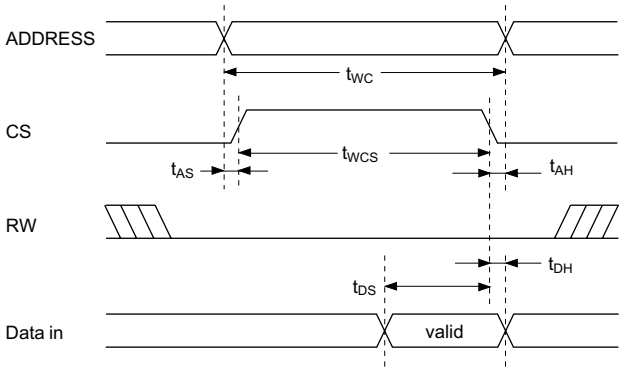


Figure 6-4 Write Cycle (CS Control)

(2) 2 port RAM

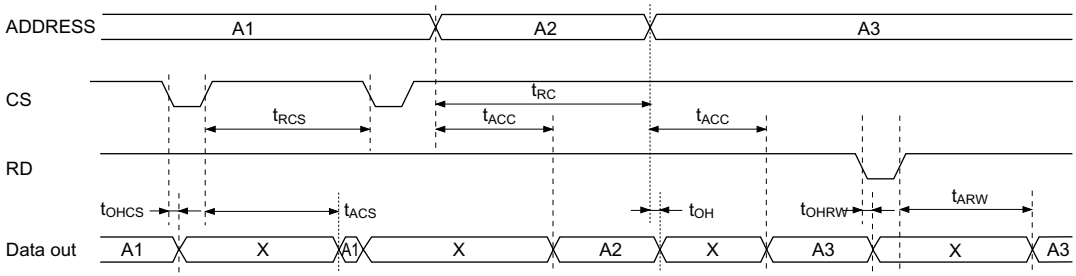


Figure 6-5 Read Cycle

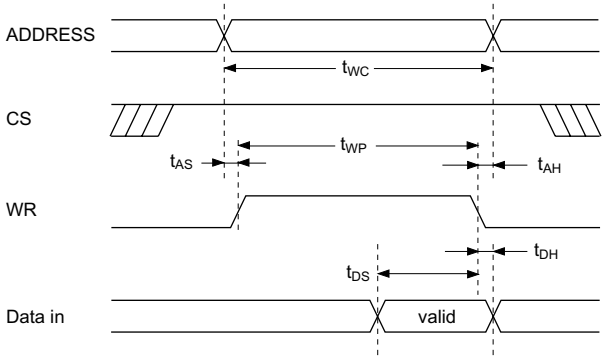


Figure 6-6 Write Cycle (WR Control)

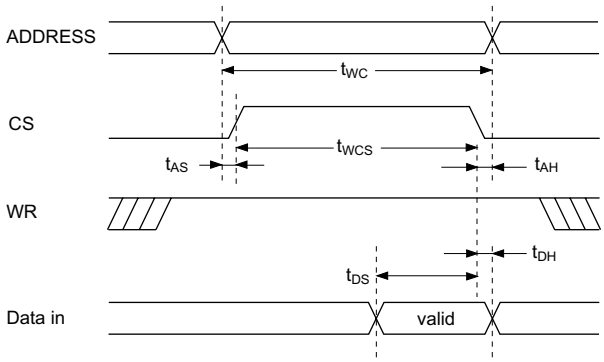


Figure 6-7 Write Cycle (CS Control)

6.2 Basic Cell Type RAM (Synchronous Type)

The S1X60000 series supports clock synchronous RAM, in addition to the clock asynchronous RAM described in 6.1. This type of RAM has latches in its chip select, write enable, address, and data input parts, allowing for clock synchronized, high-speed operation.

6.2.1 Features

- Clock synchronous 1 port and 2 port RAM are available.
- Memory contain latches in the chip select, write enable, address, and data input parts, allowing for clock synchronized, high speed operation.
- The data input and the data output ports are separated.
- Words can be configured from 16 to 256 words in 4-word increments, while bits can be configured between 1 to 32 bits in 1-bit increments.
- Maximum configuration: 8 Kbits per module

6.2.2 Word/Bit Configurations and Cell Names of the RAM

The delay parameters of the clock synchronous RAM vary with its word/bit configurations. Therefore, Epson has cells corresponding to available individual word/bit configurations. When using the clock synchronous RAM, please inform Epson whether the RAM used is 1 port or 2 port and how it is word/bit configured.

The cell names available for the typical word/bit configurations of 1 port and 2 port RAM sticks are listed on Tables 6-17 and 6-18, respectively. The cell names for synchronous RAM sticks are assigned by the naming rules described below according to the Word/Bit Configurations.

1 port RAM “SJ XXX YY”

2 port RAM “SK XXX YY” XXX: Number of words (hex), YY: Number of bits (hex)

If any synchronous RAM whose word/bit configurations exceed the acceptable range is required, use multiple instances of synchronous RAM in combination as needed for the intended application.

Table 6-17 Cell Names Available for Various Word/Bit Configurations of 1 port RAM (Clock Synchronous Type)

	64 Word	128 Word	192 Word	256 Word
8 Bit	SJ04008	SJ08008	SJ0C008	SJ10008
16 Bit	SJ04010	SJ08010	SJ0C010	SJ10010
24 Bit	SJ04018	SJ08018	SJ0C018	SJ10018
32 Bit	SJ04020	SJ08020	SJ0C020	SJ10020

Table 6-18 Cell Names Available for Various Word/Bit Configurations of 2 port RAM (Clock Synchronous Type)

	64 Word	128 Word	192 Word	256 Word
8 Bit	SK04008	SK08008	SK0C008	SK10008
16 Bit	SK04010	SK08010	SK0C010	SK10010
24 Bit	SK04018	SK08018	SK0C018	SK10018
32 Bit	SK04020	SK08020	SK0C020	SK10020

6.2.3 RAM Sizes

The RAM sizes in the X and Y directions and the number of basic cells used are calculated using the following equations, respectively.

(1) 1 port RAM

Size in X direction: $RX = \underline{27 + 7 \times \text{number of words} / 4 + 8}$

Size in Y direction: $RY = \underline{\alpha + 7 \times \text{number of bits} \times 2 + 2}$

Number of basic cells: $RAMBCS = RX \times RY$

Note that $\alpha = 3$ when $16 \leq$ number of words ≤ 32, or 4 when $36 \leq$ number of words ≤ 256.

Table 6-19 Typical Configuration of 1 port RAM and Number of Basic Cells

	8 Bit	16 Bit	24 Bit	32 Bit
32 Word	2,548	4,004	5,460	6,916
64 Word	4,263	6,615	8,967	11,319
128 Word	7,511	11,655	15,799	19,943
256 Word	14,007	21,735	29,463	37,191

(2) 2 port RAM

Size in X direction: $RX = \underline{24 + 7 \times \text{number of words} / 4 + 8}$

Size in Y direction: $RY = \underline{\alpha + 7 \times \text{number of bits} \times 2 + 2}$

Number of basic cells: $RAMBCS = RX \times RY$

Note that $\alpha = 4$ when $16 \leq$ number of words ≤ 32, or 6 when $36 \leq$ number of words ≤ 256.

Table 6-20 Typical Configuration of 2 port RAM and Number of Basic Cells

	8Bit	16Bit	24Bit	32Bit
32Word	2,552	3,960	5,368	6,776
64Word	4,464	6,768	9,072	11,376
128Word	7,936	12,032	16,128	20,224
256Word	14,880	22,560	30,240	37,920

6.2.4 Investigating RAM Placement on Master Slice

To determine whether the RAM (Clock Synchronous Type) can be mounted on each master, refer to the description in Section 6.1.4.

6.2.5 Functional Description

6.2.5.1 1 port RAM (Clock Synchronous Type)

(1) Input/output signals and block diagram

Table 6-21 Signal Description of a 1 port RAM (Clock Synchronous Type)

Input/output signal		Description
Symbol	**Name**	
CK	Clock input	The rising edge (L(H) on the clock input (CK) latches chip select (XCS), write enable (XWE), address inputs (A0 to An), and data inputs (D0 to Dn) into the internal logic of the RAM.
XCS	Chip select	Latched by the rising edge on the clock input (CK). When XCS is latched Low, chip select is enabled.
XWE	Write enable	Latched by the rising edge on the clock input (CK). When XWE is latched Low, write is enabled; when High, read is enabled.
A0 to An	Address input	Latched by the rising edge on the clock input (CK).
D0 to Dn	Data input	Latched by the rising edge on the clock input (CK). The data is written into memory cells when write enable (XWE) = Low.
Y0 to Yn	Data output	During readout, the data from memory cells are output after a specified access time has elapsed from the rising edge on the clock input (CK). During write, the write data is output from these pins synchronously with the CK. Therefore, note that during the writing of data, previously read data is not retained.

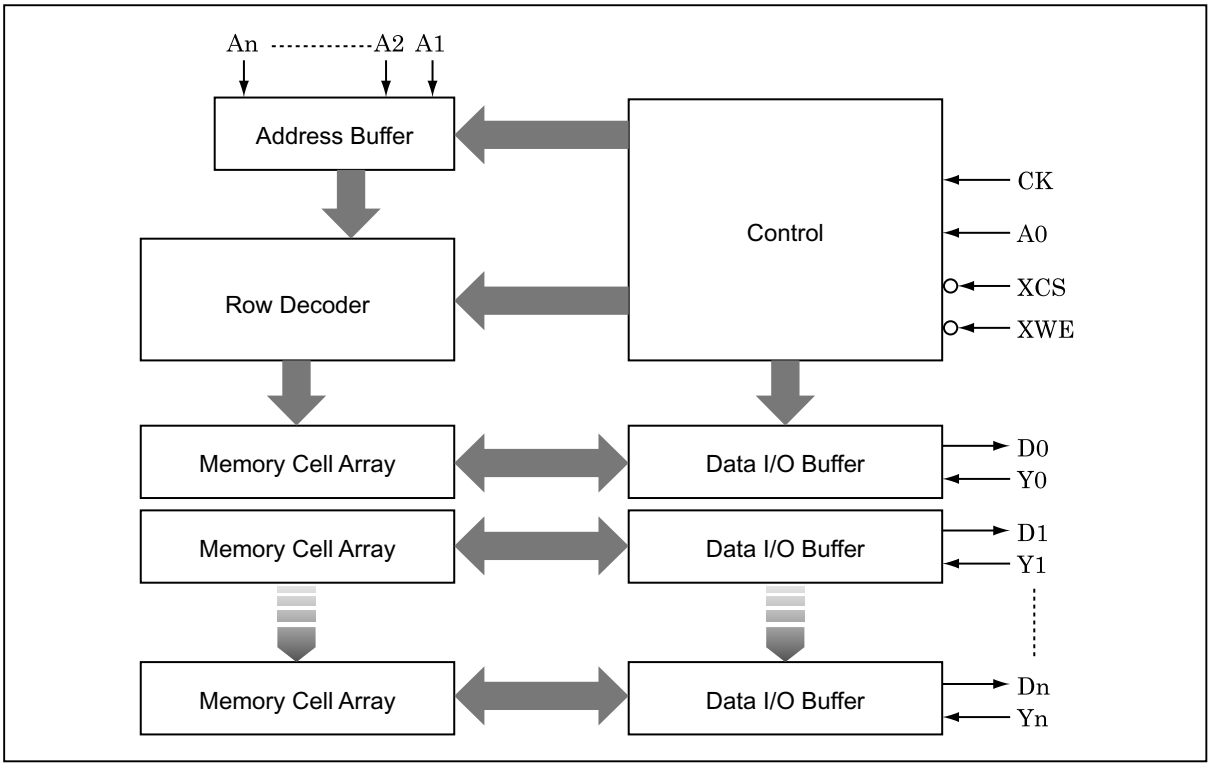


Figure 6-8 Block Diagram of a 1 port RAM (Clock Synchronous Type)

(2) Circuit operation

To write to the RAM, enable (L) chip select (XCS) and write enable (XWE) and then setting address inputs (A0 to An) and data inputs (D0 to Dn) before the clock input (CK) increases. When the clock input increases, all of the chip select, write enable, address inputs, and data inputs are latched, thereby initializing a write operation. The write data is output from the data output pins (Y0 to Yn) until the next time the clock input increases.

To read from the RAM, enable (L) chip select (XCS) and disable (H) write enable (XWE), and then setting address inputs (A0 to An) before the clock input (CK) increases. When the clock input increases, all of the chip select, write enable, and address inputs are latched, thereby initializing a read operation. During this period, data is sent out from the output pins (Y0 to Yn) after a specified access time has elapsed from the rising edge on the clock input.

Table 6-22 Truth Table for Operation of 1 port RAM (Clock Synchronous Type)

CK	XCS	XWE	Output status'	Operation mode
L → H	L	H	Read Data	Read
L → H	L	L	Write Data	Write
L → H	H	L or H	Data Hold	Standby

6.2.5.2 2 port RAM (Clock Synchronous Type)

(1) Input/output signals and block diagram

The first port is write only, and the second port is read only. The RAM has a clock input pin for each port, which can be operated independently with given frequencies and timings.

If write enable (XWA) for the first port and read enable (XRB) for the second port both are latched High, the RAM is in standby.

Table 6-23 Signal Description of 2 port RAM (Clock Synchronous Type)

Signals for the first port (write only)

Input/output signal		Description
Symbol	**Name**	
CKA	Clock input	The rising edge (L(H) on the clock input (CKA) latches write enable (XWA), address inputs (AA0 to AAn), and data inputs (D0 to Dn) into the internal logic of the RAM.
XWA	Write enable	Latched by the rising edge on the clock input (CKA). When XWE is latched Low, a write operation starts.
AA0 to AAn	Address input	Latched by the rising edge on the clock input (CKA)
D0 to Dn	Data input	Latched by the rising edge on the clock input (CKA). When write enable (XWA) = Low, data is written into memory cells.

Signals for the second port (read only)

Input/output signal		Description
Symbol	**Name**	
CKB	Clock input	The rising edge (L(H) on the clock input (CKB) latches read enable (XRB) and address inputs (AB0 to ABn) into the internal logic of the RAM.
XRB	Read enable	Latched by the rising edge on the clock input (CKB). When XRB is latched Low, a read operation starts.
AB0 to ABn	Address input	Latched by the rising edge on the clock input (CKB).
Y0 to Yn	Data output	Data from memory cells are output, after a specified access time has elapsed, from the rising edge of the clock input (CKB).

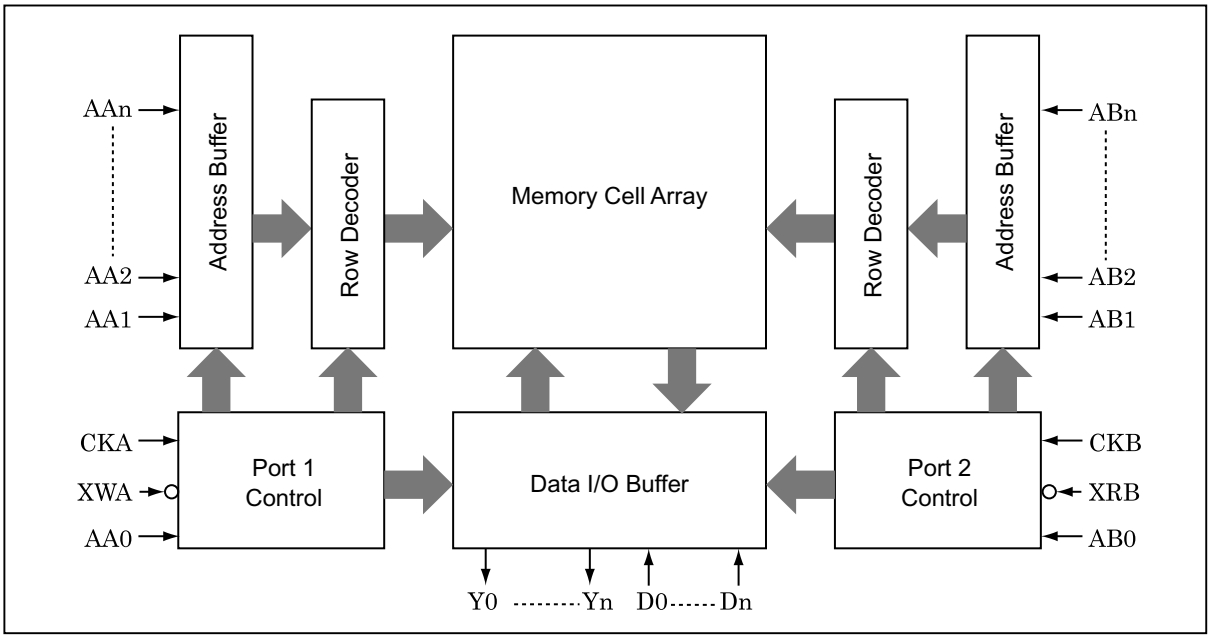


Figure 6-9 Block Diagram of a 2 port RAM (Clock Synchronous Type)

(2) Circuit operation

To write to the RAM, enable (L) write enable (XWA) and then setting address inputs (AA0 to AAn) and data inputs (D0 to Dn) before the clock input (CKA) increases. When the clock input (CKA) increases, all of the write enable (XWA), address inputs (AA0 to AAn), and data inputs (D0 to Dn) are latched, thereby initializing a write operation.

To read from the RAM, enable (L) read enable (XRB) and then setting address inputs (AB0 to ABn) before the clock input (CKB) increases. When the clock input (CKB) increases, all of the read enable (XRB) and address inputs (AB0 to ABn) are latched, thereby initializing a read operation. During this period, data is sent out from the output pins (Y0 to Yn), after a specified access time has elapsed, from the rising edge on the clock input (CKB).

Table 6-24 Truth Table for Operation of 2 port RAM (Clock Synchronous Type)

(Truth table for operation of the first port (write only))

CKA	XWA	Operation mode
L → H	H	Standby
L → H	L	Write

(Truth table for operation of the second port (read only)

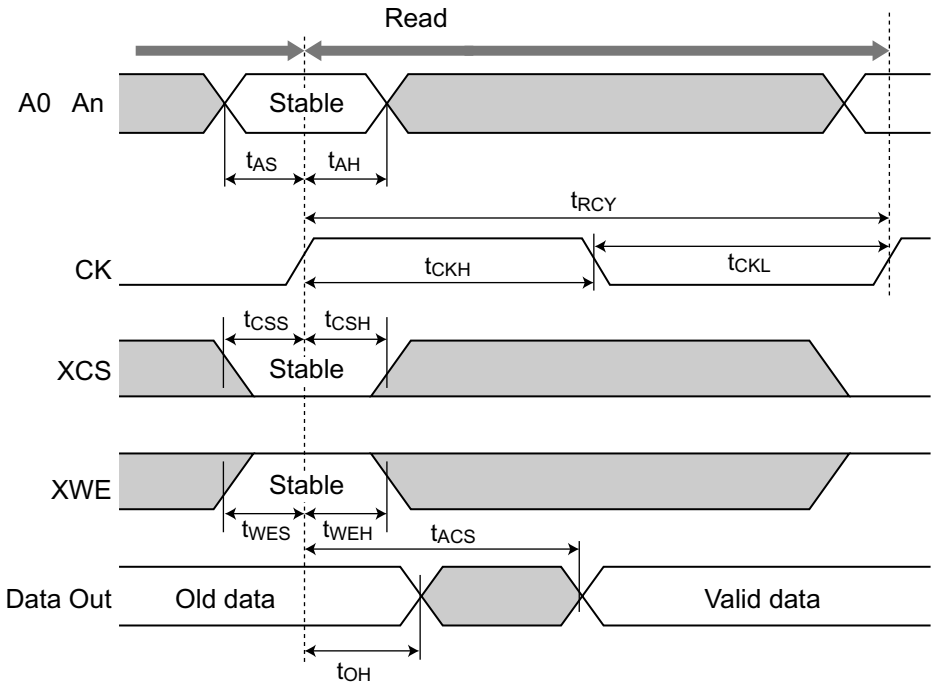
CKB	XRB	Output status	Operation mode
L → H	H	Data Hold	Standby
L → H	L	Read Data	Read

If a write to and a read from are simultaneously attempted for the same memory, the write operation is given priority. Data is written to the memory normally, but no result is returned for the read data request.

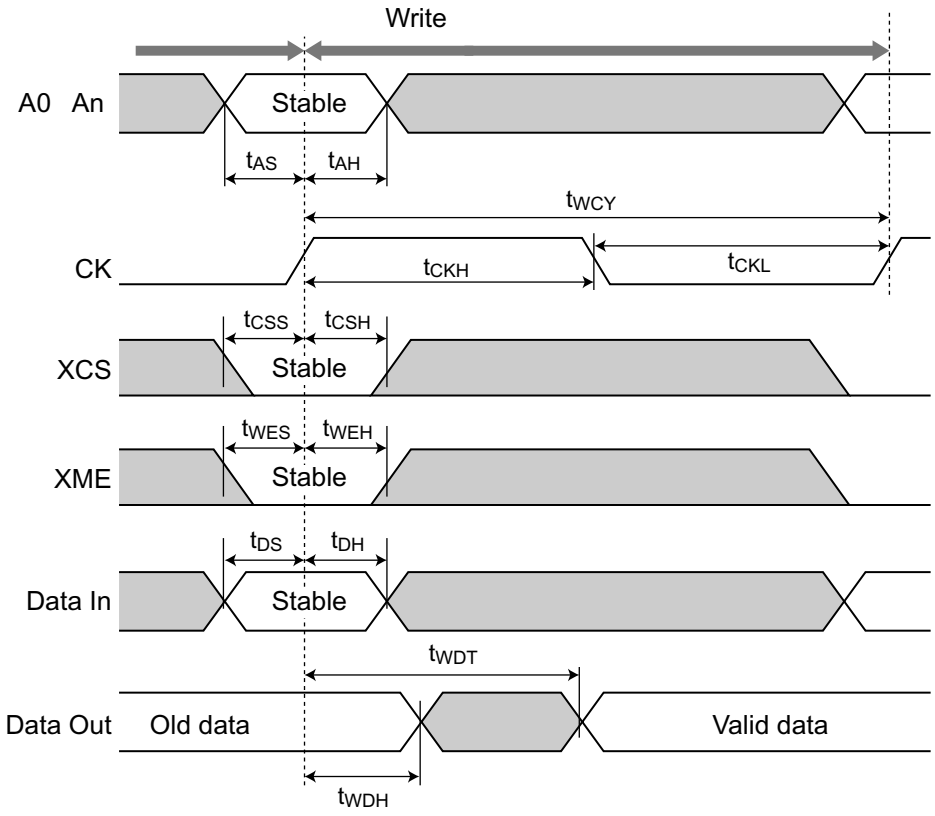
6.2.6 Timing Charts

(1) 1 port RAM

- Read Cycle

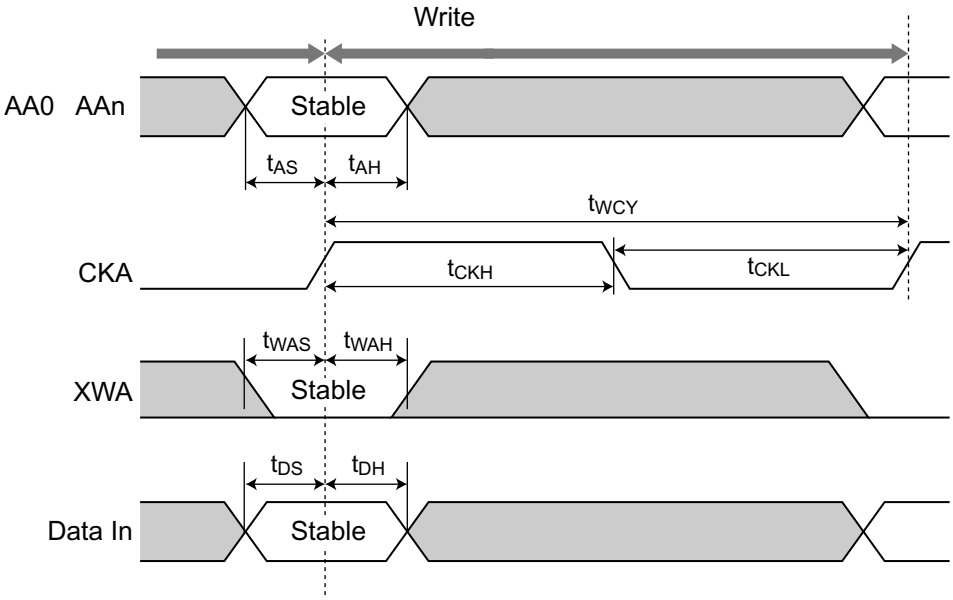


- Write Cycle

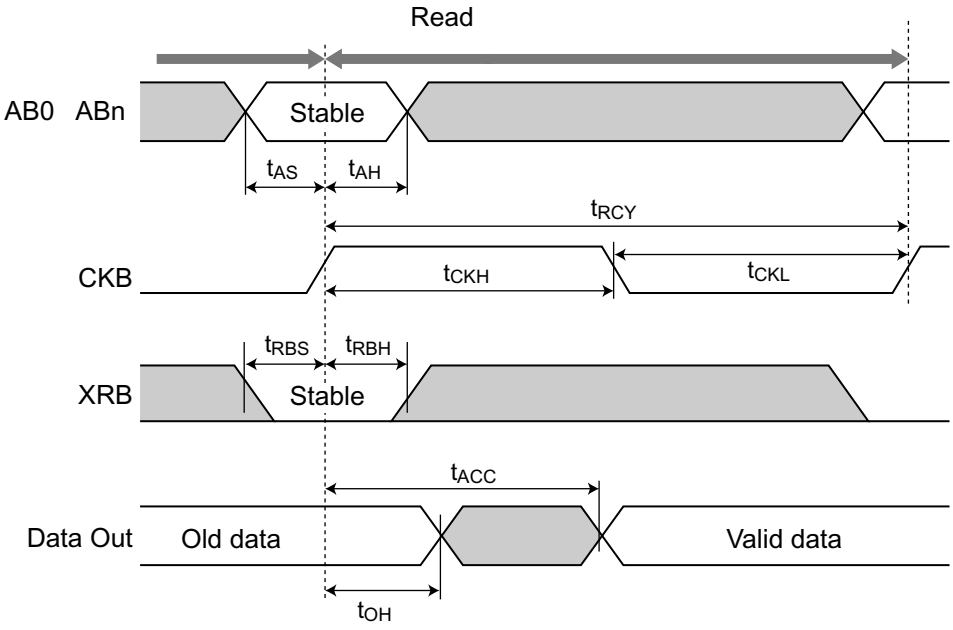


(2) 2 port RAM

- First port



- Second port



6.2.7 Delay Parameters

(1) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C) 64 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	3.957	—	4.023	—	4.110	—	4.193	ns
Read cycle time	t_{RCY}	3.957	—	4.023	—	4.110	—	4.193	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.624	—	0.650	—	0.666	—	0.680	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.602	—	3.712	—	3.826	—	3.940	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.299	—	1.338	—	1.367	—	1.397	—	
Write data through time	t_{WDT}	—	3.602	—	3.712	—	3.826	—	3.940	

(2) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C) 64 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	3.743	—	3.806	—	3.887	—	3.966	ns
Read cycle time	t_{RCY}	3.743	—	3.806	—	3.887	—	3.966	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.669	—	0.696	—	0.713	—	0.728	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.407	—	3.512	—	3.619	—	3.727	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.391	—	1.433	—	1.465	—	1.497	—	
Write data through time	t_{WDT}	—	3.407	—	3.512	—	3.619	—	3.727	

(3) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C) 128 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	4.995	—	5.060	—	5.132	—	5.241	ns
Read cycle time	t_{RCY}	4.995	—	5.060	—	5.132	—	5.241	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.641	—	0.659	—	0.675	—	0.693	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.685	—	3.807	—	3.909	—	4.018	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.341	—	1.376	—	1.426	—	1.433	—	
Write data through time	t_{WDT}	—	3.685	—	3.807	—	3.909	—	4.018	

(4) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C) 128 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	4.725	—	4.787	—	4.855	—	4.958	ns
Read cycle time	t_{RCY}	4.725	—	4.787	—	4.855	—	4.958	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.686	—	0.706	—	0.723	—	0.742	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.486	—	3.601	—	3.698	—	3.801	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.437	—	1.474	—	1.528	—	1.536	—	
Write data through time	t_{WDT}	—	3.486	—	3.601	—	3.698	—	3.801	

(5) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C) 192 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	6.076	—	6.133	—	6.198	—	6.268	ns
Read cycle time	t_{RCY}	6.076	—	6.133	—	6.198	—	6.268	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.652	—	0.671	—	0.690	—	0.705	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.748	—	3.857	—	3.970	—	4.077	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.372	—	1.407	—	1.440	—	1.467	—	
Write data through time	t_{WDT}	—	3.748	—	3.857	—	3.970	—	4.077	

(6) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C) 192 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	5.748	—	5.802	—	5.863	—	5.929	ns
Read cycle time	t_{RCY}	5.748	—	5.802	—	5.863	—	5.929	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.698	—	0.719	—	0.739	—	0.756	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.546	—	3.649	—	3.755	—	3.857	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.470	—	1.507	—	1.543	—	1.572	—	
Write data through time	t_{WDT}	—	3.546	—	3.649	—	3.755	—	3.857	

(7) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = -40 to +85°C) 256 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	7.004	—	7.073	—	7.138	—	7.208	ns
Read cycle time	t_{RCY}	7.004	—	7.073	—	7.138	—	7.208	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.652	—	0.672	—	0.690	—	0.705	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.794	—	3.901	—	4.004	—	4.118	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.398	—	1.431	—	1.464	—	1.491	—	
Write data through time	t_{WDT}	—	3.794	—	3.901	—	4.004	—	4.118	

(8) 2.5 V specifications (V_{DD} = 2.3 to 2.7 V, T_a = 0 to +70°C) 256 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	6.626	—	6.690	—	6.752	—	6.818	ns
Read cycle time	t_{RCY}	6.626	—	6.690	—	6.752	—	6.818	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.698	—	0.720	—	0.739	—	0.756	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	3.589	—	3.690	—	3.787	—	3.895	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE setup time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write data hold time	t_{WDH}	1.498	—	1.534	—	1.568	—	1.598	—	
Write data through time	t_{WDT}	—	3.589	—	3.690	—	3.787	—	3.895	

(9) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C) 64 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	5.630	—	5.725	—	5.848	—	5.966	ns
Read cycle time	t_{RCY}	5.630	—	5.725	—	5.848	—	5.966	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.758	—	0.789	—	0.808	—	0.825	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	5.125	—	5.282	—	5.445	—	5.607	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.577	—	1.624	—	1.660	—	1.697	—	
Write data through time	t_{WDT}	—	5.125	—	5.282	—	5.445	—	5.607	

(10) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C) 64 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	5.341	—	5.431	—	5.548	—	5.660	ns
Read cycle time	t_{RCY}	5.341	—	5.431	—	5.548	—	5.660	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.802	—	0.836	—	0.856	—	0.874	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ04008/ SK04008		SJ04010/ SK04010		SJ04018/ SK04018		SJ04020/ SK04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	4.862	—	5.011	—	5.165	—	5.319	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.670	—	1.720	—	1.758	—	1.797	—	
Write data through time	t_{WDT}	—	4.862	—	5.011	—	5.165	—	5.319	

(11) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C) 128 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	7.108	—	7.200	—	7.302	—	7.458	ns
Read cycle time	t_{RCY}	7.108	—	7.200	—	7.302	—	7.458	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.778	—	0.800	—	0.820	—	0.841	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	5.243	—	5.417	—	5.563	—	5.718	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.629	—	1.671	—	1.732	—	1.741	—	
Write data through time	t_{WDT}	—	5.243	—	5.417	—	5.563	—	5.718	

(12) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C) 128 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	6.743	—	6.831	—	6.928	—	7.075	ns
Read cycle time	t_{RCY}	6.743	—	6.831	—	6.928	—	7.075	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.823	—	0.847	—	0.868	—	0.891	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ08008/ SK08008		SJ08010/ SK08010		SJ08018/ SK08018		SJ08020/ SK08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	4.974	—	5.139	—	5.277	—	5.425	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.725	—	1.769	—	1.834	—	1.843	—	
Write data through time	t_{WDT}	—	4.974	—	5.139	—	5.277	—	5.425	

(13) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C) 192 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	8.646	—	8.727	—	8.820	—	8.919	ns
Read cycle time	t_{RCY}	8.646	—	8.727	—	8.820	—	8.919	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.792	—	0.815	—	0.837	—	0.857	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	5.333	—	5.489	—	5.648	—	5.801	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.666	—	1.709	—	1.748	—	1.782	—	
Write data through time	t_{WDT}	–	5.333	–	5.489	–	5.648	–	5.801	

(14) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C) 192 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	8.203	—	8.280	—	8.368	—	8.462	ns
Read cycle time	t_{RCY}	8.203	—	8.280	—	8.368	—	8.462	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.838	—	0.863	—	0.887	—	0.907	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ0C008/ SK0C008		SJ0C010/ SK0C010		SJ0C018/ SK0C018		SJ0C020/ SK0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	5.060	—	5.207	—	5.359	—	5.504	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.764	—	1.809	—	1.851	—	1.887	—	
Write data through time	t_{WDT}	—	5.060	—	5.207	—	5.359	—	5.504	

(15) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = -40 to +85°C) 256 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	9.967	—	10.064	—	10.156	—	10.256	ns
Read cycle time	t_{RCY}	9.967	—	10.064	—	10.156	—	10.256	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.792	—	0.815	—	0.837	—	0.857	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	5.398	—	5.551	—	5.697	—	5.859	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.698	—	1.738	—	1.777	—	1.811	—	
Write data through time	t_{WDT}	—	5.398	—	5.551	—	5.697	—	5.859	

(16) 2.0 V specifications (V_{DD} = 1.8 to 2.2 V, T_a = 0 to +70°C) 256 words

1 port/2 port RAM read cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access time	t_{ACS}, t_{ACC}	—	9.455	—	9.548	—	9.636	—	9.730	ns
Read cycle time	t_{RCY}	9.455	—	9.548	—	9.636	—	9.730	—	
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB setup time	t_{RBS}	1.500	—	1.500	—	1.500	—	1.500	—	
XRB hold time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output hold time	t_{OH}	0.873	—	0.899	—	0.924	—	0.945	—	

1 port/2 port RAM write cycle AC characteristics table

Parameter	Symbol	SJ10008/ SK10008		SJ10010/ SK10010		SJ10018/ SK10018		SJ10020/ SK10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WCY}	5.121	—	5.266	—	5.405	—	5.559	—	ns
Clock high pulse width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock low pulse width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS setup time	t_{CSS}	1.500	—	1.500	—	1.500	—	1.500	—	
XCS hold time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address setup time	t_{AS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE setup time	t_{WES}	1.500	—	1.500	—	1.500	—	1.500	—	
XWE hold time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA setup time	t_{WAS}	1.500	—	1.500	—	1.500	—	1.500	—	
XWA hold time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address hold time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data hold time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data setup time	t_{DS}	1.500	—	1.500	—	1.500	—	1.500	—	
Write data hold time	t_{WDH}	1.798	—	1.841	—	1.882	—	1.918	—	
Write data through time	t_{WDT}	—	5.121	—	5.266	—	5.405	—	5.559	

6.3 Standard Type 1 port RAM

6.3.1 Features

- For this type of RAM, the circuit and layout pattern are exclusively designed as 1 port RAM in order to reduce the area that the RAM occupies. (Three AL layers are used.)
- Can be configured in a wide range of memory capacities (128 to 64k bits), and provides superior flexibility for selection of the height to width ratio of the layout shape. Furthermore, if large capacity memory is required, multiple pieces of memory macros may be used.
- Can be accessed at High speed and consumes less current than other RAMs of the same class.
- The chip select, write enable, byte write enable, address, and data input/output parts contain a latch circuit, making the RAM capable of clock synchronized, high speed operation.
- The data input port and data output port are separate.
- A byte write function is included, allowing the bits of write data to be selected in byte units.
- The data output part contains a latch circuit, so that readout data is output continuously until the next read cycle.

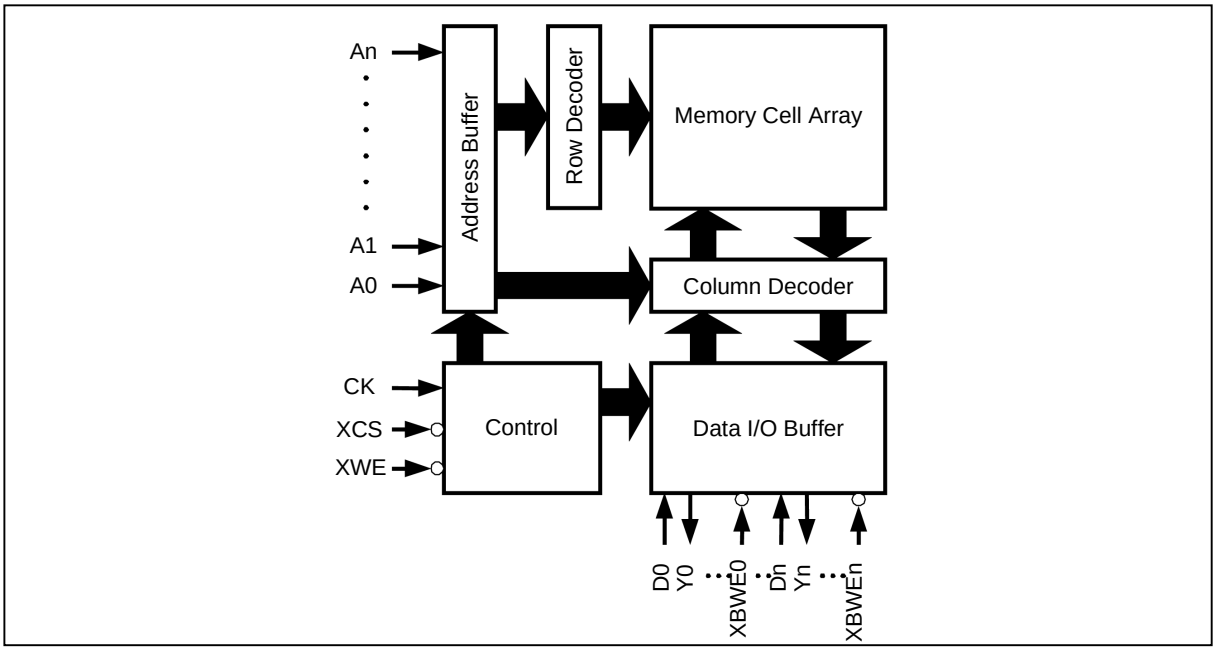
6.3.2 RAM Sizes

The sizes of standard type 1 port RAMs vary in a complicated manner depending on the word/bit configurations. For detailed information on RAM sizes, please contact the sales division of Epson.

6.3.3 Input Signals and Block Diagrams

Input/output signal		Description
Symbol	**Name**	
CK	Clock input	Chip select (XCS), write enable (XWE), byte write enable (XBWEn), address input (A0 to An), and data input (D0 to Dn) are latched into the rising edge (Low to High transition) of the clock input (CK). Memory is activated when the latched chip select signal is Low. While memory is active, data is written to memory when the latched write enable signal is Low, or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCS	Chip select	Latched into the rising edge of the clock input (CK). When the latched value is Low, memory is activated.
XWE	Write enable	Latched into the rising edge of the clock input (CK). Memory is activated for write operation when the latched value is Low, or for read operation when the latched value is High.
XBWEn	Byte write enable	Latched into the rising edge of the clock input (CK). Each byte of data is assigned one byte write enable signal. Only data bytes with Low byte XBWEn when XWE is Low, are written to memory. XBWE0 for D0–D7 XBWE1 for D8–D15 XBWE2 for D16–D23 XBWE3 for D24–D31
A0 to An	Address input	Latched into the rising edge of the clock input (CK).
D0 to Dn	Data input	The write data is latched into the rising edge of the clock input (CK) and written to memory cells.
Y0 to Yn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CK). During writing, the latched write data is output from these pins.

Block Diagram



S1X60K 1 port RAM (Byte Write Option)

6.3.4 Truth Table of Device Operation

For writing, assert chip select (XCS), write enable (XWE), and byte write enable (XBWE0 to XBWE3) (by pulling them Low), and set the address inputs (A0 to An) and data inputs (D0 to Dn) before the clock input (CK) goes High. All of the chip select, write enable, byte write enable, address input, and data input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data output pins (Y0 to Yn). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

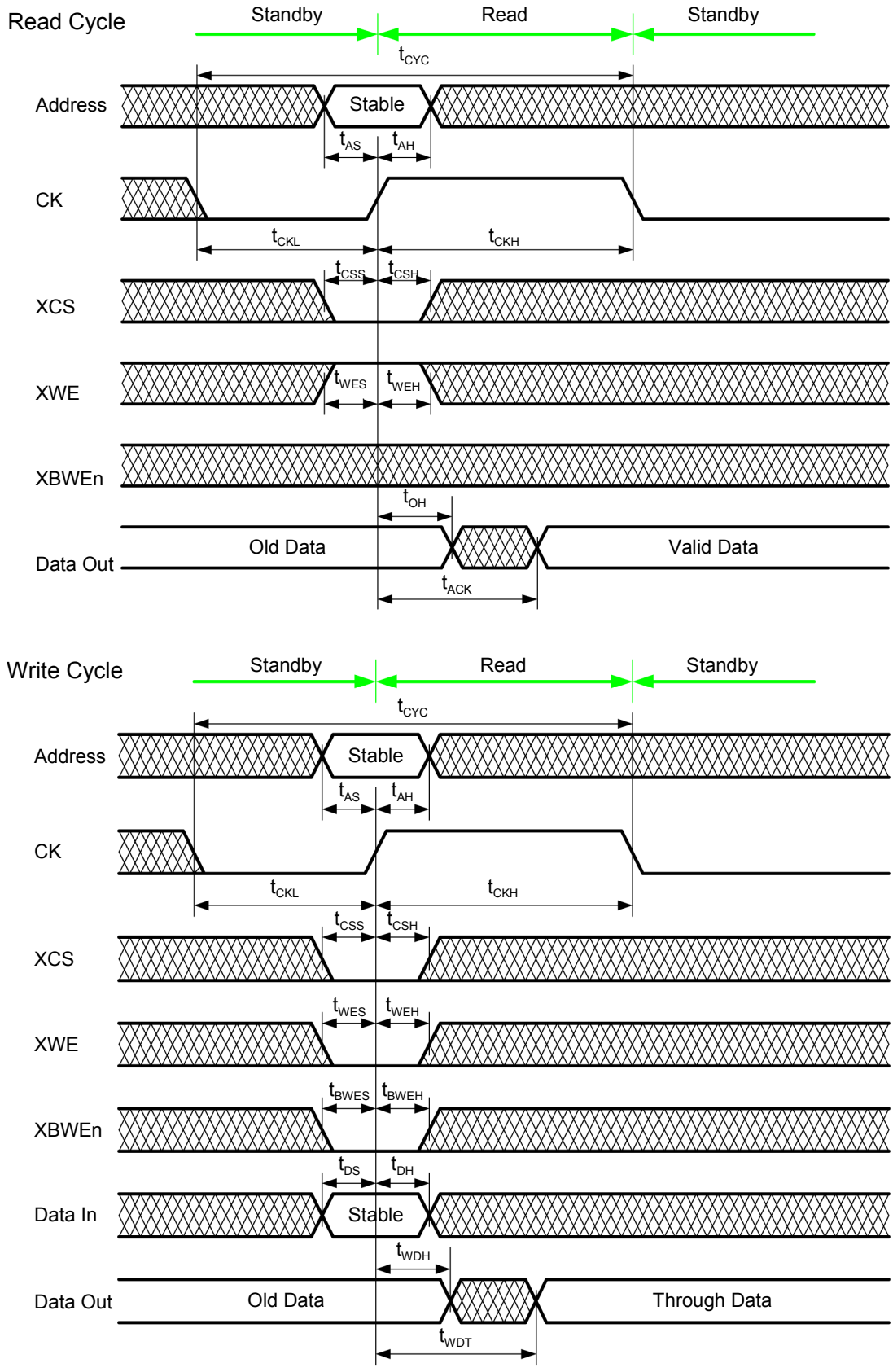
For reading, assert chip select (XCS) and deassert write enable (XWE) (by pulling XCS Low and XWE High), and set the address inputs (A0 to An) before the clock input (CK) goes High. All of the chip select, write enable, and address input, and data input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the data output pins (Y0 to Yn) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either reading or writing, data appears at the data output pins even after the operation has been completed and the memory is placed in standby state.

Truth Table of Standard Type 1 port RAM Operation

CK	XCS	XWE	XBWE0	XBWE1	XBWE2	XBWE3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data hold	Standby
L → H	L	H	X	X	X	X	—	Read Data	Read
L → H	L	L	L	L	L	L	D0 to D31	Write Data	Write all bytes
L → H	L	L	L	H	H	H	D0 to D7	Write Data (*1)	Write 1st byte
L → H	L	L	H	L	H	H	D8 to D15	Write Data (*1)	Write 2nd byte
L → H	L	L	H	H	L	H	D16 to D23	Write Data (*1)	Write 3rd byte
L → H	L	L	H	H	H	L	D24 toD31	Write Data (*1)	Write 4th byte
L → H	L	L	H	H	H	H	—	Write Data (*1)	Unable to write
L → H	H	X	X	X	X	X	—	Data hold	Standby
H → L	X	X	X	X	X	X	—	Data hold	Standby

Note *1: The state of the data outputs (Y0 to Yn) reflects the values supplied to the data inputs (D0 to Dn). However, only the data bytes selected using byte write enable (XBWE0 to XBWE3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

6.3.5 Timing Charts



6.3.6 Electrical Characteristics

Power consumption (Memory Configuration: 8 k Words × 8 Data)

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	1000	—	—	700	—	nA
Active Current	IDDA	—	160	—	—	130	—	μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	125	—	—	75	MHz
CK Access Time	t_{ACK}	—	3.4	6.2	—	4.8	9.6	nS
CK High Width Time	t_{CKH}	4.0	—	—	6.6	—	—	nS
CK Low Width Time	t_{CKL}	3.2	—	—	4.4	—	—	nS
Cycle Time	t_{CYC}	8.0	—	—	13.2	—	—	nS
CS Setup Time	t_{CSS}	2.6	—	—	4.2	—	—	nS
CS Hold Time	t_{CSH}	0	—	—	0	—	—	nS
Address Setup Time	t_{AS}	2.6	—	—	4.2	—	—	nS
Address Hold Time	t_{AH}	0	—	—	0	—	—	nS
WE Setup Time	t_{WES}	2.6	—	—	4.2	—	—	nS
WE Hold Time	t_{WEH}	0	—	—	0	—	—	nS
BWE Setup Time	t_{BWES}	2.6	—	—	4.2	—	—	nS
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	nS
Output Hold Time	t_{OH}	1.0	—	—	1.8	—	—	nS
Data Setup Time	t_{DS}	2.6	—	—	4.2	—	—	nS
Data Hold Time	t_{DH}	0	—	—	0	—	—	nS
Write Data Hold Time	t_{WDH}	0.3	—	—	0.5	—	—	nS
Write Data Through Time	t_{WDT}	—	—	3.0	—	—	4.2	nS

Power Consumption (Memory Configuration: 8 k Words × 8 Data)

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—	—	—	—	nA
Active Current	IDDA	—	160	—	—	130	—	μA/MHz

AC Characteristic

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	135	—	—	78	MHz
CK Access Time	t_{ACK}	—	3.4	5.8	—	4.8	9.2	nS
CK High Width Time	t_{CKH}	3.8	—	—	6.4	—	—	nS
CK Low Width Time	t_{CKL}	3.0	—	—	4.0	—	—	nS
Cycle Time	t_{CYC}	7.6	—	—	12.8	—	—	nS
CS Setup Time	t_{CSS}	2.4	—	—	4.0	—	—	nS
CS Hold Time	t_{CSH}	0	—	—	0	—	—	nS
Address Setup Time	t_{AS}	2.4	—	—	4.0	—	—	nS
Address Hold Time	t_{AH}	0	—	—	0	—	—	nS
WE Setup Time	t_{WES}	2.4	—	—	4.0	—	—	nS
WE Hold Time	t_{WEH}	0	—	—	0	—	—	nS
BWE Setup Time	t_{BWES}	2.4	—	—	4.0	—	—	nS
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	nS
Output Hold Time	t_{OH}	1.0	—	—	1.8	—	—	nS
Data Setup Time	t_{DS}	2.4	—	—	4.0	—	—	nS
Data Hold Time	t_{DH}	0	—	—	0	—	—	nS
Write Data Hold Time	t_{WDH}	0.3	—	—	0.5	—	—	nS
Write Data Through Time	t_{WDT}	—	—	2.8	—	—	4.0	nS

6.4 Standard Type Dual Port RAM

6.4.1 Features

- For this type of RAM, the circuit and layout pattern are exclusively designed as dual port RAM in order to reduce the area that the RAM occupies. (Three AL layers are used.)
- Can be configured in a wide range of memory capacities (1k to 64k bits), and provides superior flexibility for selection of the height to width ratio of the layout shape. Furthermore, if large-capacity memory is required, multiple pieces of memory macros may be used.
- Can be accessed at High speed and consumes less current than other RAMs of the same class.
- A byte write function is included, allowing the bits of write data to be selected in byte units.
- The chip select, write enable, byte write enable, address, and data input/output parts contain a latch circuit, making the RAM capable of clock-synchronized, high-speed operation.
- The data input port and data output port are separated.
- The data output part contains a latch circuit, so that readout data is output continuously until the next read cycle.

6.4.2 RAM Sizes

The sizes of standard type dual port RAMs vary in a complicated manner depending on the word/bit configurations. For detailed information on RAM sizes, please contact the sales division of Epson.

6.4.3 Input Signals and Block Diagrams

Ports 1 and 2 are each capable of performing read and write operations. Each port comes equipped with a clock input pin, allowing them to be operated with different frequencies or timing independently of each other.

Be aware that no memory cells can be accessed from two ports at the same time. If arbitration facilities, busy signals, or the like are required to resolve conflicts, configure a necessary circuit in the gate-array section external to the macro. (If accessed at the same time, the read or write operation in that cycle and the data in the accessed memory cell become indeterminate.)

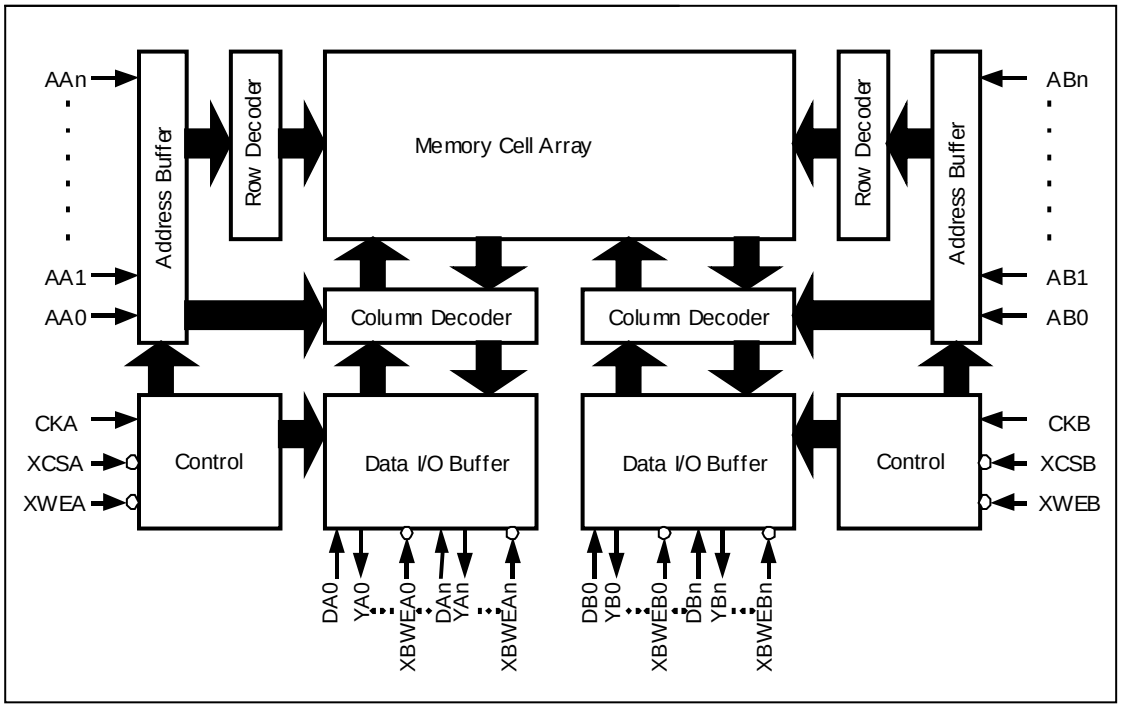
Port-1 signals (read/write)

Input/output signal		Description
Symbol	**Name**	
CKA	Clock input	Chip select (XCSA), write enable (XWEA), byte write enable (XBWEAn), address input (AA0 to AAn), and data input (DA0 to DAn) are latched into the rising edge (Low to High transition) of the clock input (CKA). Memory is activated when the latched chip select signal is Low. While the memory is active, data is written to memory when the latched write enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCSA	Chip select	Latched into the rising edge of the clock input (CKA). Memory is activated when the latched value is Low.
XWEA	Write enable	Latched into the rising edge of the clock input (CKA). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEAn	Byte write enable	Latched into the rising edge of the clock input (CKA). Each byte of data is assigned one byte write enable signal. Only data bytes with Low byte XBWEAn when XWEA is Low are written to memory. XBWEA0 for DA0–DA7 XBWEA1 for DA8–DA15 XBWEA2 for DA16–DA23 XBWEA3 for DA24–DA31
AA0 to AAn	Address input	Latched into the rising edge of the clock input (CKA).
DA0 to DAn	Data input	The write data is latched into the rising edge of the clock input (CKA) and written to memory cells.
YA0 to YAn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CKA). During writing, the latched write data is output from these pins.

Port-2 signals (read/write)

Input/output signal		Description
Symbol	**Name**	
CKB	Clock input	Chip select (XCSB), write enable (XWEB), byte write enable (XBWEBn), address input (AB0 to ABn), and data input (DB0 to DBn) are latched into the rising edge (Low to High transition) of the clock input (CKB). Memory is activated when the latched chip select signal is Low. While the memory is active, data is written to memory when the latched write enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCSB	Chip select	Latched into the rising edge of the clock input (CKB). Memory is activated when the latched value is Low.
XWEB	Write enable	Latched into the rising edge of the clock input (CKB). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEBn	Byte write enable	Latched into the rising edge of the clock input (CKB). Each byte of data is assigned one byte write enable signal. Only data bytes with Low byte XBWEBn when XWEB is Low are written to memory. XBWEB0 for DB0–DB7 XBWEB1 for DB8–DB15 XBWEB2 for DB16–DB23 XBWEB3 for DB24–DB31
AB0 to ABn	Address input	Latched into the rising edge of the clock input (CKB).
DB0 to DBn	Data input	The write data is latched into the rising edge of the clock input (CKB) and written to memory cells.
YB0 to YBn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CKB). During writing, the latched write data is output from these pins.

Block Diagram



S1X60K Dual Port RAM (Byte Write Option)

6.4.4 Truth Table of Device Operation

For writing, assert chip select (XCSA or XCSB), write enable (XWEA or XWEB), and byte write enable (XBWEA0 to XBWEA3 or XBWEB0 to XBWEB3) (by pulling them Low), and set the address inputs (AA0 to AAn or AB0 to ABn) and data inputs (DA0 to DAn or DB0 to DBn) before the clock input (CKA or CKB) goes High. All of the chip select, write enable, byte write enable, address input, and data input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data output pins (YA0 to YAn or YB0 to YBn). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

For reading, assert chip select (XCSA or XCSB) and deassert write enable (XWEA or XWEB) (by pulling XCSA or XCSB Low and XWEA or XWEB High), and set the address inputs (AA0 to AAn or AB0 to ABn) before the clock input (CKA or CKB) goes High. All of the chip select, write enable, and address-input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the output pins (YA0 to YAn or YB0 to YBn) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either read or write, data appears at the data output pins even after the operation has completed and the memory is placed in standby state.

Port-1 truth table

CKA	XCSA	XWEA	XBWEA0	XBWEA1	XBWEA2	XBWEA3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data hold	Standby
L → H	L	H	X	X	X	X	—	Read Data	Read
L → H	L	L	L	L	L	L	DA0–DA31	Write Data	Write all bytes
L → H	L	L	L	H	H	H	DA0–DA7	Write Data (*1)	Write 1st byte
L → H	L	L	H	L	H	H	DA8–DA15	Write Data (*1)	Write 2nd byte
L → H	L	L	H	H	L	H	DA16–DA23	Write Data (*1)	Write 3rd byte
L → H	L	L	H	H	H	L	DA24–DA31	Write Data (*1)	Write 4th byte
L → H	L	L	H	H	H	H	—	Write Data (*1)	Unable to write
L → H	H	X	X	X	X	X	—	Data hold	Standby
H → L	X	X	X	X	X	X	—	Data hold	Standby

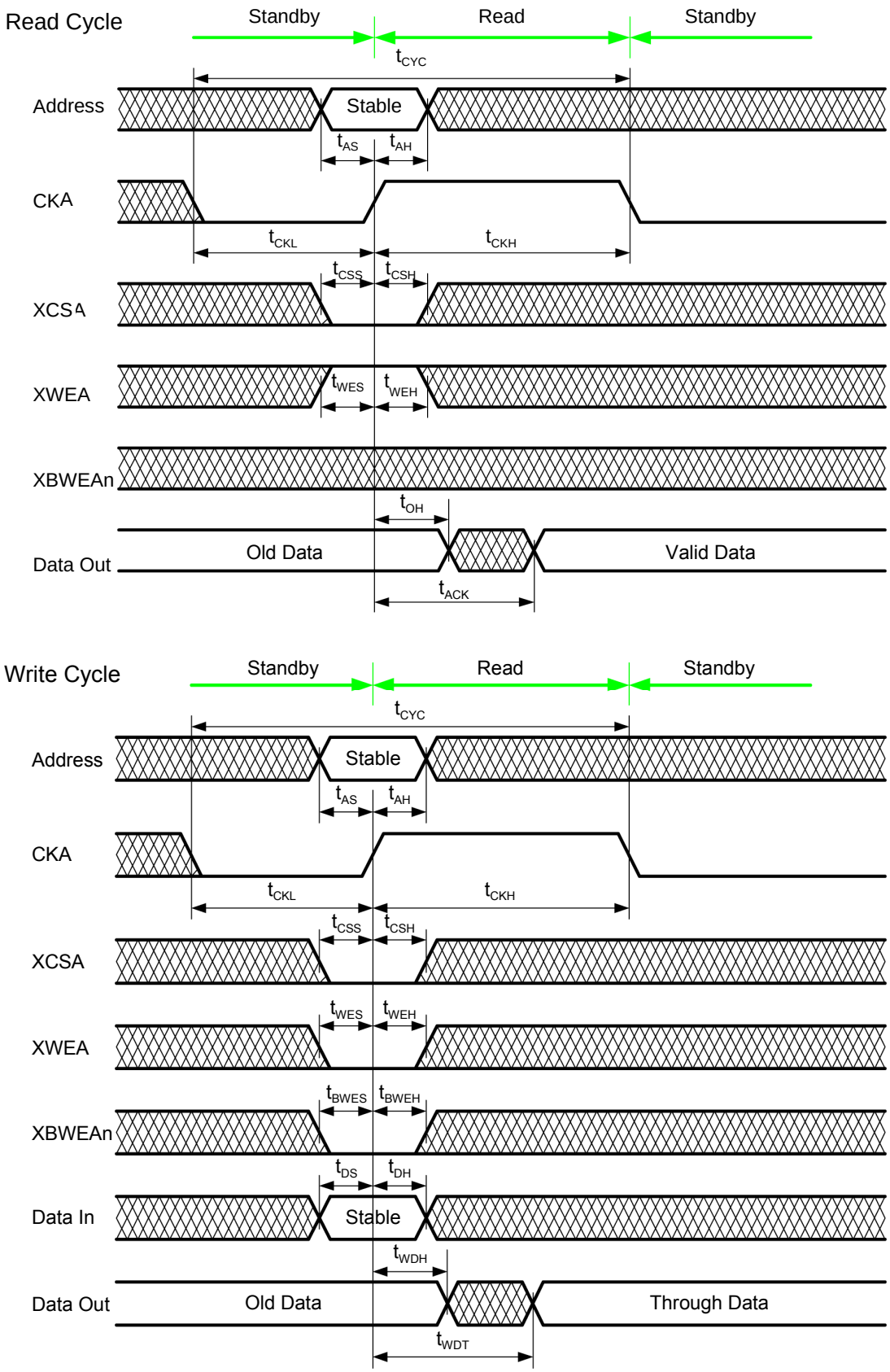
Port-2 truth table

CKB	XCSB	XWEB	XBWEB0	XBWEB1	XBWEB2	XBWEB3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data hold	Standby
L → H	L	H	X	X	X	X	—	Read Data	Read
L → H	L	L	L	L	L	L	DB0–DB31	Write Data	Write all bytes
L → H	L	L	L	H	H	H	DB0–DB7	Write Data (*1)	Write 1st byte
L → H	L	L	H	L	H	H	DB8–DB15	Write Data (*1)	Write 2nd byte
L → H	L	L	H	H	L	H	DB16–DB23	Write Data (*1)	Write 3rd byte
L → H	L	L	H	H	H	L	DB24–DB31	Write Data (*1)	Write 4th byte
L → H	L	L	H	H	H	H	—	Write Data (*1)	Unable to write
L → H	H	X	X	X	X	X	—	Data hold	Standby
H → L	X	X	X	X	X	X	—	Data hold	Standby

Note *1: The state of the data outputs (YA0 to YAn or YB0 to YBn) reflects the values supplied to the data inputs (DA0 to DAn or DB0 to DBn).
However, only the data bytes selected using byte write enable (XBWEA0 to XBWEA3 or XBWEB0 to XBWEB3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

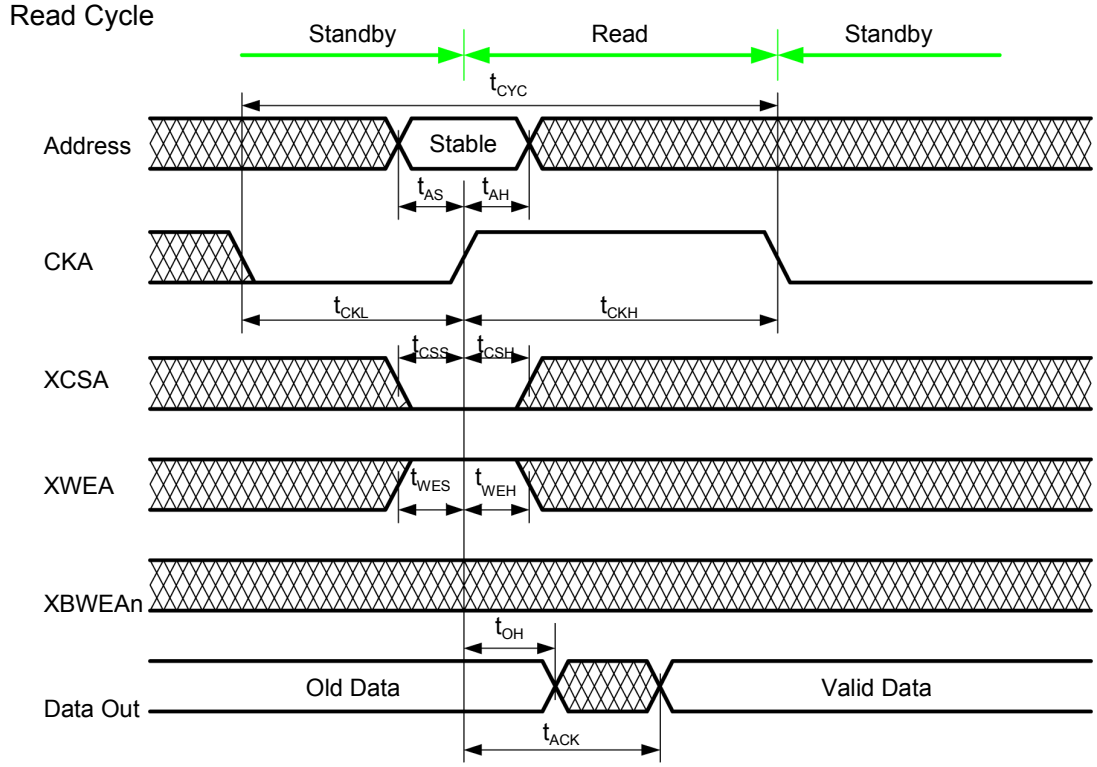
6.4.5 Timing Charts

Port 1

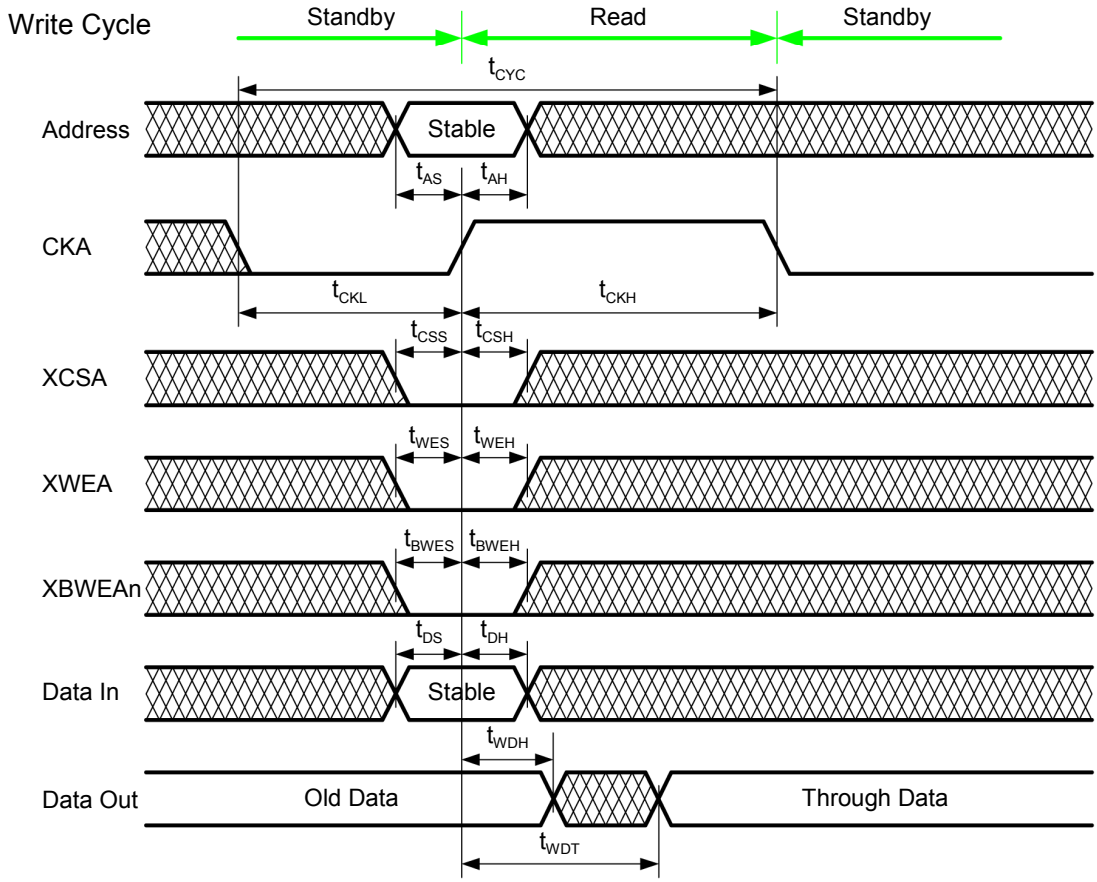


Port 2

Read Cycle



Write Cycle



6.4.6 Electrical Characteristics

Power Consumption (Memory Configuration: 8 k Words × 8 Data)

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—		—		nA
Active Current	IDDA	—	260	—		210		μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	119	—	—	71	MHz
CK Access Time	t_{ACK}	—	4.0	7.2	—	5.4	10.8	nS
CK High Width Time	t_{CKH}	4.2	—	—	7.0	—	—	nS
CK Low Width Time	t_{CKL}	3.6	—	—	5.4	—	—	nS
Cycle Time	t_{CYC}	8.4	—	—	14.0	—	—	nS
CS Setup Time	t_{CSS}	3.8	—	—	5.0	—	—	nS
CS Hold Time	t_{CSH}	0	—	—	0	—	—	nS
Address Setup Time	t_{AS}	3.8	—	—	5.0	—	—	nS
Address Hold Time	t_{AH}	0	—	—	0	—	—	nS
WE Setup Time	t_{WES}	3.8	—	—	5.0	—	—	nS
WE Hold Time	t_{WEH}	0	—	—	0	—	—	nS
BWE Setup Time	t_{BWES}	3.8	—	—	5.0	—	—	nS
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	nS
Output Hold Time	t_{OH}	1.0	—	—	2.0	—	—	nS
Data Setup Time	t_{DS}	3.8	—	—	5.0	—	—	nS
Data Hold Time	t_{DH}	0	—	—	0	—	—	nS
Write Data Hold Time	t_{WDH}	0.3	—	—	0.5	—	—	nS
Write Data Through Time	t_{WDT}	—	—	3.8	—	—	5.2	nS

Power Consumption (Memory Configuration: 8 k Words × 8 Data)

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—		—		nA
Active Current	IDDA	—	260	—		210		μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	128	—	—	74	MHz
CK Access Time	t_{ACK}	—	4.0	6.8	—	5.4	10.4	nS
CK High Width Time	t_{CKH}	4.0	—	—	6.8	—	—	nS
CK Low Width Time	t_{CKL}	3.6	—	—	5.0	—	—	nS
Cycle Time	t_{CYC}	8.0	—	—	13.6	—	—	nS
CS Setup Time	t_{CSS}	3.8	—	—	4.8	—	—	nS
CS Hold Time	t_{CSH}	0	—	—	0	—	—	nS
Address Setup Time	t_{AS}	3.8	—	—	4.8	—	—	nS
Address Hold Time	t_{AH}	0	—	—	0	—	—	nS
WE Setup Time	t_{WES}	3.8	—	—	4.8	—	—	nS
WE Hold Time	t_{WEH}	0	—	—	0	—	—	nS
BWE Setup Time	t_{BWES}	3.8	—	—	4.8	—	—	nS
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	nS
Output Hold Time	t_{OH}	1.0	—	—	2.0	—	—	nS
Data Setup Time	t_{DS}	3.8	—	—	4.8	—	—	nS
Data Hold Time	t_{DH}	0	—	—	0	—	—	nS
Write Data Hold Time	t_{WDH}	0.3	—	—	0.5	—	—	nS
Write Data Through Time	t_{WDT}	—	—	3.6	—	—	5.0	nS

6.5 High Density Type 1 port RAM

6.5.1 Features

- For this type of RAM, the circuit and layout pattern are exclusively designed as 1 port RAM in order to reduce the area that the RAM occupies.
- Can be accessed at High speed and consumes less current than other RAMs of the same class.
- The chip select, write enable, address, data and byte write enable input parts contain a latch circuit, making the RAM capable of clock synchronized, high speed operation.
- The data input port and data output port are separated.
- A byte write function is included, allowing the bits of write data to be selected in byte units.
- The data output part contains a latch circuit, allowing readout data to be output continuously until the next read cycle.

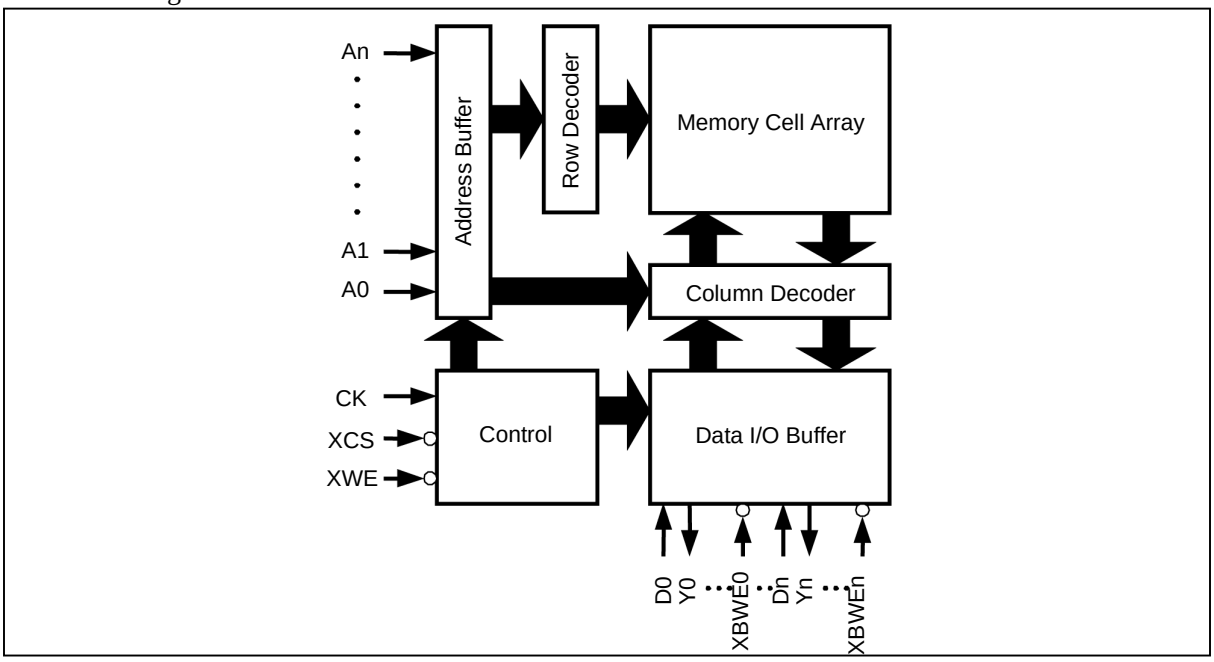
6.5.2 RAM Sizes

The sizes of high density type 1 port RAMs vary in a complicated manner, depending on the word/bit configurations. For detailed information on RAM sizes, please contact the sales division of Epson.

6.5.3 Input/Output Signals and Block Diagrams

Input/output signal		Description
Symbol	Name	
CK	Clock input	Chip select (XCS), write enable (XWE), byte write enable (XBWEn), address input (A0 to An), and data input (D0 to Dn) are latched into the rising edge (Low to High transition) of the clock input (CK). Memory is activated when the latched chip select signal is Low. While the memory is active, data is written to memory when the latched write enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCS	Chip select	Latched into the rising edge of the clock input (CK). Memory is activated when the latched value is Low.
XWE	Write enable	Latched into the rising edge of the clock input (CK). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEn	Byte write enable	Latched into the rising edge of the clock input (CK). Each byte of data is assigned one byte write enable signal. Only data bytes with Low XBWEn when XWE is Low are written to memory. XBWE0 for D0 to D7 XBWE1 for D8 to D15 XBWE2 for D16 to D23 XBWE3 for D24 to D31
A0 to An	Address input	Latched into the rising edge of the clock input (CK).
D0 to Dn	Data input	The write data is latched into the rising edge of the clock input (CK) and written to memory cells.
Y0 to Yn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CK). During writing, the latched write data is output from these pins.

Block Diagram



S1X60K High Density 1 port RAM (Byte Write option)

6.5.4 Truth Table of Device Operation

For writing, assert chip select (XCS), write enable (XWE), and byte write enable (XBWE0 to XBWE3) (by pulling them Low), and set the address inputs (A0 to An) and data inputs (D0 to Dn) before the clock input (CK) goes High. All of the chip select, write enable, byte write enable, address input, and data input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data output pins (Y0 to Yn). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

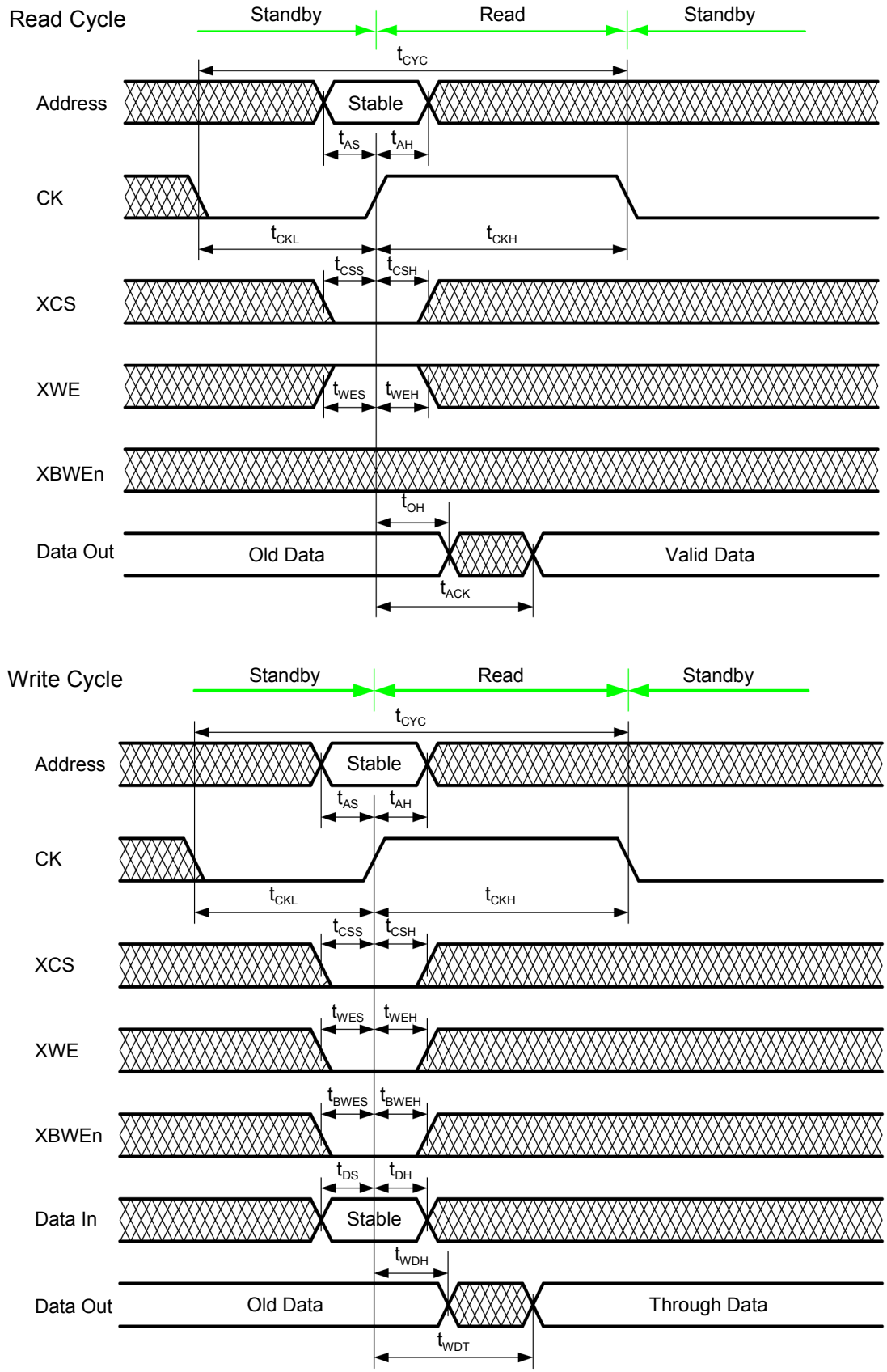
For reading, assert chip select (XCS) and deassert write enable (XWE) (by pulling XCS Low and XWE High), and set the address inputs (A0 to An) before the clock input (CK) goes High. All of the chip select, write enable, and address input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the data output pins (Y0 to Yn) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either read or write, data appears at the data output pins even after the operation has completed and the memory is placed in standby state.

Truth Table of High Density Type 1 port RAM Operation

CK	XCS	XWE	XBWE0	XBWE1	XBWE2	XBWE3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data hold	Standby
L → H	L	H	X	X	X	X	—	Read Data	Read
L → H	L	L	L	L	L	L	D0 to D31	Write Data	Write all bytes
L → H	L	L	L	H	H	H	D0 to D7	Write Data (*1)	Write 1st byte
L → H	L	L	H	L	H	H	D8 to D15	Write Data (*1)	Write 2nd byte
L → H	L	L	H	H	L	H	D16 to D23	Write Data (*1)	Write 3rd byte
L → H	L	L	H	H	H	L	D24 to D31	Write Data (*1)	Write 4th byte
L → H	L	L	H	H	H	H	—	Write Data (*1)	Unable to write
L → H	H	X	X	X	X	X	—	Data hold	Standby
H → L	X	X	X	X	X	X	—	Data hold	Standby

Note *1: The state of data outputs (Y0 to Yn) reflects the values supplied to data inputs (D0 to Dn). However, only the data bytes selected using byte write enable (XBWE0 to XBWE3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

6.5.5 Timing Charts



6.5.6 Electrical Characteristics

Power Consumption (Memory Configuration: 32 k Words × 16 Data)

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—	—	—	—	nA
Active Current	IDDA	—	250	—	—	200	—	μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	71	—	—	40	MHz
CK Access Time	t_{ACK}	—	5.8	10.8	—	8.2	17.2	ns
CK High Width Time	t_{CKH}	7.0	—	—	12.2	—	—	ns
CK Low Width Time	t_{CKL}	3.6	—	—	4.0	—	—	ns
Cycle Time	t_{CYC}	14.0	—	—	24.4	—	—	ns
CS Setup Time	t_{CSS}	2.2	—	—	3.8	—	—	ns
CS Hold Time	t_{CSH}	0	—	—	0	—	—	ns
Address Setup Time	t_{AS}	2.2	—	—	3.8	—	—	ns
Address Hold Time	t_{AH}	0	—	—	0	—	—	ns
WE Setup Time	t_{WES}	2.2	—	—	3.8	—	—	ns
WE Hold Time	t_{WEH}	0	—	—	0	—	—	ns
BWE Setup Time	t_{BWES}	2.2	—	—	3.8	—	—	ns
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	ns
Output Hold Time	t_{OH}	2.6	—	—	4.0	—	—	ns
Data Setup Time	t_{DS}	2.2	—	—	3.8	—	—	ns
Data Hold Time	t_{DH}	0	—	—	0	—	—	ns
Write Data Hold Time	t_{WDH}	1.0	—	—	1.2	—	—	ns
Write Data Through Time	t_{WDT}	—	—	4.0	—	—	6.6	ns

Power Consumption (Memory Configuration: 32 k Words × 16 Data)

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—	—	—	—	nA
Active Current	IDDA	—	250	—	—	200	—	μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	76	—	—	42	MHz
CK Access Time	t_{ACK}	—	5.8	10.0	—	8.2	16.4	ns
CK High Width Time	t_{CKH}	6.6	—	—	11.8	—	—	ns
CK Low Width Time	t_{CKL}	3.2	—	—	3.8	—	—	ns
Cycle Time	t_{CYC}	13.2	—	—	23.6	—	—	ns
CS Setup Time	t_{CSS}	2.2	—	—	3.8	—	—	ns
CS Hold Time	t_{CSH}	0	—	—	0	—	—	ns
Address Setup Time	t_{AS}	2.0	—	—	3.8	—	—	ns
Address Hold Time	t_{AH}	0	—	—	0	—	—	ns
WE Setup Time	t_{WES}	2.0	—	—	3.8	—	—	ns
WE Hold Time	t_{WEH}	0	—	—	0	—	—	ns
BWE Setup Time	t_{BWES}	2.0	—	—	3.8	—	—	ns
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	ns
Output Hold Time	t_{OH}	2.6	—	—	4.0	—	—	ns
Data Setup Time	t_{DS}	2.0	—	—	3.8	—	—	ns
Data Hold Time	t_{DH}	0	—	—	0	—	—	ns
Write Data Hold Time	t_{WDH}	1.0	—	—	1.2	—	—	ns
Write Data Through Time	t_{WDT}	—	—	3.8	—	—	6.2	ns

6.6 Mask ROM

6.6.1 Features

- The circuit and layout pattern are exclusively designed as mask ROM in order to reduce the area that it occupies (Three AL layers are used.)
- Because data is programmed into memory at nearly the end of the manufacturing process (HOLA), TAT can be reduced.
- Can be configured in a wide range of memory capacities (1 k to 256 k bits), and provides superior flexibility for selection of the height to width ratio of the layout shape. Furthermore, if large-capacity memory is required, multiple pieces of memory macros may be used.
- Can be accessed at High speed and consumes less current than other ROMs of the same class.
- Can operate with Low voltage over a wide voltage range.
- The chip select and address-input parts contain a latch circuit, making the ROM capable of clock synchronized, high speed operation.
- The data output part contains a latch circuit, allowing readout data to be output continuously until the next read cycle.

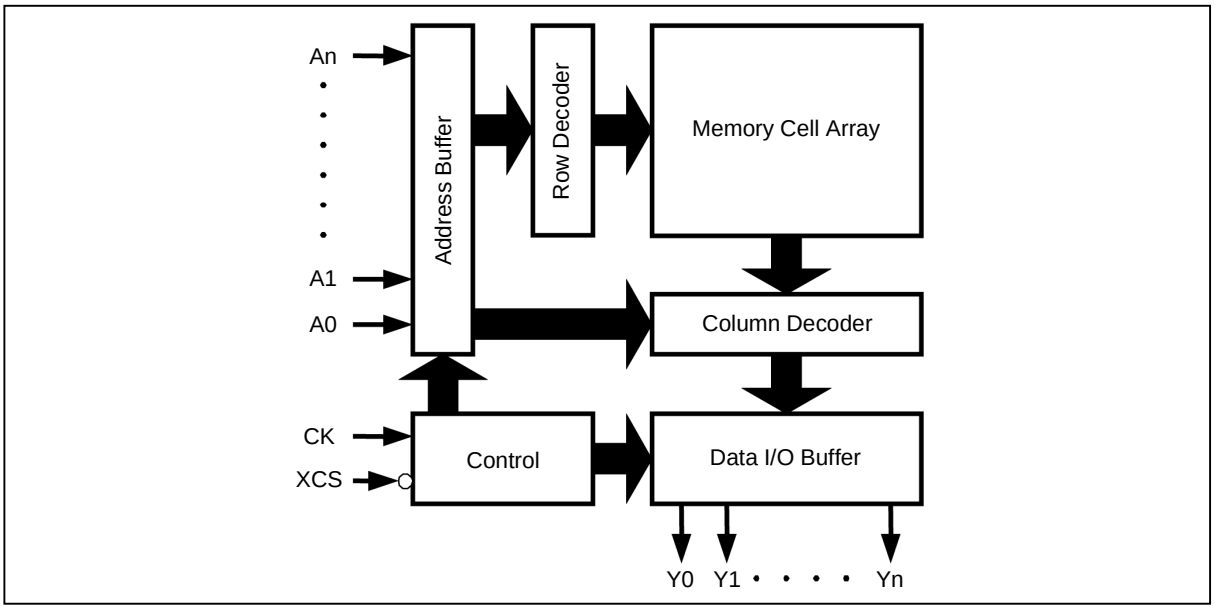
6.6.2 ROM Sizes

The ROM sizes vary in a complicated manner depending on the word/bit configurations. For detailed information on ROM sizes, please contact the sales division of Epson.

6.6.3 Input/Output Signals and Block Diagrams

Input/output signal		Description
Symbol	Name	
CK	Clock input	Chip select (XCS) and address input (A0–An) are latched into the rising edge (Low to High transition) of the clock input (CK). When the latched chip select signal is Low, memory is activated for read operation.
XCS	Chip select	Latched into the rising edge of the clock input (CK). When this latched value is Low, memory is activated for read operation.
A0 to An	Address input	Latched into the rising edge of the clock input (CK).
Y0 to Yn	Data output	The data readout from memory cells is output from these pins a finite access time after the rising edge of the clock input (CK).

Block Diagram



S1X60000 Mask ROM

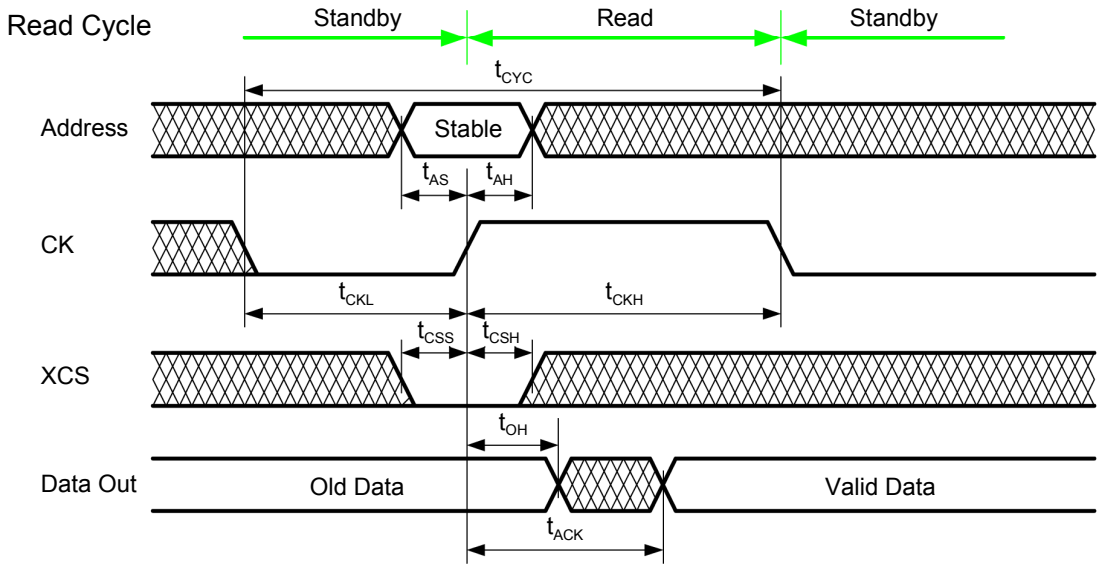
6.6.4 Truth Table of Device Operation

For reading, assert chip select (XCS) (by pulling it Low), and set the address inputs (A0 to An) before the clock input (CK) goes High. The chip select and address input signals are latched into the rising edge of the clock, at which time memory is activated for read operation. During this period, data is output from the data output pins a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. Even after the read operation has completed and the memory is placed in standby state, data remains displayed at the data output pins.

Truth Table of ROM Operation

CK	XCS	Output State	Operation Mode
L	X	Data hold	Standby
L → H	L	Read Data	Read
L → H	H	Data hold	Standby
H → L	X	Data hold	Standby

6.6.5 Timing Charts



6.6.6 Electrical Characteristics

Power Consumption (Memory Configuration: 32 k Words × 8 Data)

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—	—	—	—	nA
Active Current	IDDA	—	175	—	—	130	—	μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V -40 to +85°C			2.0 V ± 0.2 V -40 to +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	66	—	—	40	MHz
CK Access Time	t_{ACK}	—	5.4	9.4	—	7.0	14.0	ns
CK High Width Time	t_{CKH}	7.6	—	—	12.4	—	—	ns
CK Low Width Time	t_{CKL}	2.8	—	—	3.2	—	—	ns
Cycle Time	t_{CYC}	15.2	—	—	24.8	—	—	ns
CS Setup Time	t_{CSS}	2.6	—	—	3.0	—	—	ns
CS Hold Time	t_{CSH}	0	—	—	0	—	—	ns
Address Setup Time	t_{AS}	2.6	—	—	3.0	—	—	ns
Address Hold Time	t_{AH}	0	—	—	0	—	—	ns
Output Hold Time	t_{OH}	1.0	—	—	2.0	—	—	ns

Power Consumption (Memory Configuration: 32 k Words × 16 Data)

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby Current	IDDS	—	—	—	—	—	—	nA
Active Current	IDDA	—	175	—	—	130	—	μA/MHz

AC Characteristics

Parameter	Symbol	2.5 V ± 0.2 V 0 to +70°C			2.0 V ± 0.2 V 0 to +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fc	—	—	71	—	—	42	MHz
CK Access Time	t_{ACK}	—	5.4	8.6	—	7.0	13.2	ns
CK High Width Time	t_{CKH}	7.0	—	—	12.0	—	—	ns
CK Low Width Time	t_{CKL}	2.6	—	—	3.0	—	—	ns
Cycle Time	t_{CYC}	14.0	—	—	24.0	—	—	ns
CS Setup Time	t_{CSS}	2.4	—	—	2.8	—	—	ns
CS Hold Time	t_{CSH}	0	—	—	0	—	—	ns
Address Setup Time	t_{AS}	2.4	—	—	2.8	—	—	ns
Address Hold Time	t_{AH}	0	—	—	0	—	—	ns
Output Hold Time	t_{OH}	1.0	—	—	2.0	—	—	ns

6.7 Access to Nonexistent Addresses Inhibited

When some RAMs with an intermediate word configuration (e.g., 48 or 88 words) are used, there is a possibility of accessing nonexistent addresses.

In the actual IC, if nonexistent addresses are accessed for reading, the target word lines do not exist and all word lines are turned off, resulting in all bit lines being placed in a floating state. For this reason, the following problems may occur:

(1) Because read operation is performed while all bit lines are left floating, all bits of RAM output become “indeterminate.”

(2) Because read operation is performed while all bit lines are left floating, a path is created in part of the circuit through which current can flow. Although the amount of this current depends on the RAM configuration and size, it causes the operating and quiescent currents of the entire IC to vary.

Therefore, we recommend that access to nonexistent addresses be inhibited.

In logic simulation, the presence of nonexistent addresses is checked synchronously with the rising edge of the clock during read/write operation and, when access to any nonexistent address is attempted, a timing error is output.

Chapter 7 Propagation Delay and Timing

7.1 Accuracy of the Propagation Delay Time

The propagation delay time, T_{pd}, varies with the LSI's power supply voltage, ambient temperature, and process conditions. It also varies with circuit configurations such as the output load (e.g., wiring capacitance or fan-out counts), distorted input waveforms, input logic levels, and mirror effects.

For the S1X60000 series, a delay calculator has been introduced that helps minimize these fluctuating factors, in order to provide a highly accurate delay time calculation environment. Therefore, be aware that the results obtained using this delay calculator do not necessarily match the propagation delay times calculated by customers from the values listed in the "S1X60000 Series Cell Library" by following the simplified calculation procedure described below.

7.2 Calculating the Propagation Delay Time

The calculation formulas shown below provide a simple means of calculating the propagation delay time. This calculation formula is such that the larger the load capacitance, the greater the delay error, so that the resulting values are smaller than those obtained using the delay calculator. Therefore, the values calculated here can only be used as a guide.

(1) Delay time of input cells and internal cells

The delay time of input cells and internal cells, T_{pd}, is calculated as the sum total of the cell's inherent delay time when nonloaded, T_0, and the load delay caused by the wiring load capacitance and input load capacitance connected to the cell outputs. Consequently, the propagation delay time, T_{pd}, is calculated using the equation below.

$$T_{pd} = T_0 + K \times (\Sigma \text{ Load A} + \text{Load B}) \text{ ..... (Equation 7-1)}$$

where, T_0 : cell's inherent delay when nonloaded [ps]
K : load delay coefficient [ps/LU]
Load A: input capacitance of the connected cell [LU]
Load B: wiring load capacitance [LU]

Note 1: The values of T_0 and K vary with the LSI's operating voltage, ambient temperature, and process conditions. For these parameters, use the values listed in the "S1X60000 Series Cell Library."

Note 2: The unit "LU" stands for Load Unit. In the S1X60000 series, the gate capacitance at the input pin of the inverter cell (IN1) is defined as 1 LU.

(2) Delay time of the output cells

The delay time of the output cells, T_{pd}, is calculated from the output cell's inherent delay time when nonloaded, T_0, and the load capacitance connected to the external output pins, C_L, by using the equation below.

$$T_{pd} = T_0 + K \times C_L / 10 \text{ ..... (Equation 7-2)}$$

where, T_0 : output cell's inherent delay when nonloaded [ps]
K : output cell's load delay coefficient [ps/10 pF]
CL: load capacitance connected to the external output pins [pF]

7.3 Virtual Wiring Capacitance

As placement and routing performed in the circuit design phase are not based on the circuit's connection information, the length of the wiring connected as a load to the circuit has not yet been determined. For this reason, in the pre placement and routing stages, the propagation delay time is calculated using the wiring capacitances (referred to as the "virtual wiring capacitances") that have been prepared through statistical processing.

For the S1X60000 series, a wide selection of virtual wiring capacitances per branch of output are available to choose from depending on the number of wiring layers and Gate counts. These virtual wiring capacitances are listed in Tables 7-1.

Table 7-1 Virtual Wiring Capacitances per Branch

(Unit: LU)

Gate counts	3-layer wiring	4-layer wiring	5-layer wiring
1000	2.056	2.062	2.057
5000	2.063	2.068	2.064
10000	2.071	2.076	2.072
20000	2.087	2.092	2.088
40000	2.119	2.125	2.120
60000	2.152	2.157	2.153
80000	2.184	2.190	2.185
100000	2.217	2.222	2.218
200000	2.379	2.385	2.380
400000	2.703	2.710	2.704
600000	3.027	3.035	3.029
800000	3.351	3.360	3.353
1000000	3.675	3.685	3.677
1200000	3.999	4.010	4.001
1400000	4.323	4.335	4.326
1600000	4.648	4.660	4.650
1800000	4.972	4.985	4.974
2000000	5.296	5.310	5.299

Examples of calculation of the propagation delay time

(1) Delay time of input cells and internal cells

The following describes the procedure for calculating the approximate amount of propagation delay time in each path, using the circuits in Figure 7-1 as an example.

Table 7-2 lists various characteristic values excerpted from the "S1X60000 Series Cell Library." The circuits shown below amount to a total of 20,000 gates in circuit size.

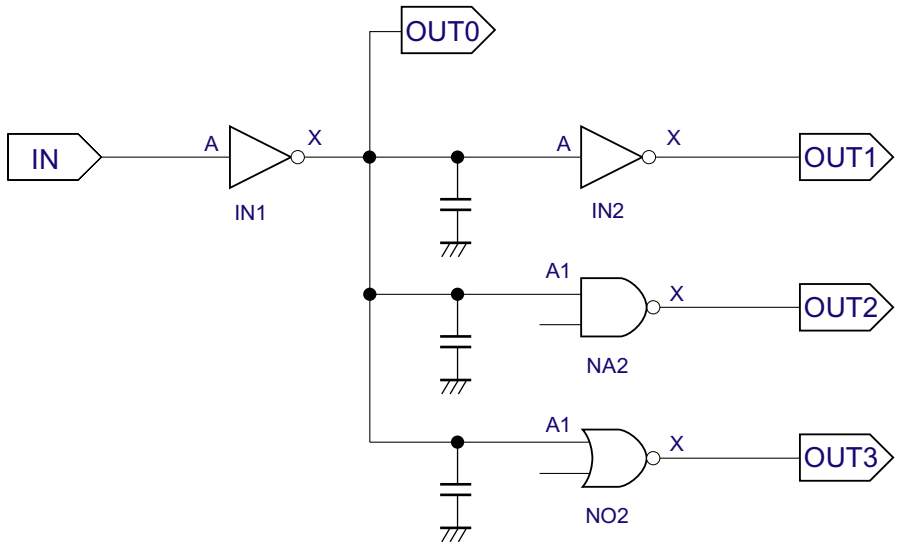


Figure 7-1 Example Circuits for Calculation of the Internal Cell Propagation Delay Time

Table 7-2 Delay Characteristics of Each Cell (Power Supply Voltage: 2.5 V)

Cell	Input		Output		Delay Characteristics (Typ.)				
	Pin	Fan-in [LU]	Pin	Fan-out [LU]	From	To	Parameter	T_0 [ps]	K [ps/LU]
IN1	A	1.0	X	14.4	A	X	t_{pLH}	43	18.7
							t_{pHL}	44	10.2
IN2	A	2.0	X	28.9	A	X	t_{pLH}	36	9.3
							t_{pHL}	37	5.1
NA2	A1	0.9	X	14.2	A	X	t_{pLH}	57	18.9
							t_{pHL}	50	16.0
NO2	A1	1.1	X	7.3	A	X	t_{pLH}	56	36.0
							t_{pHL}	53	10.2

IN2 (pin A), NA2 (pin A1), and NO2 (pin A1) are connected to output pin X of the cell IN1. Therefore, from Table 7-2, the total amount of the input load capacitance of the cells, Load A, is found to be as follows:

$$\sum \text{Load A} = \text{IN2 (fan-in of pin A)} + \text{NA2 (fan-in of pin A1)} + \text{NO2 (fan-in of pin A1)}$$
$$= 2.0 + 0.9 + 1.1 = 4.0 \text{ [LU]}$$

In addition, the wiring load capacitance, Load B, is calculated using the virtual wiring capacitances. Here, assuming that placement and routing are performed using 3 layer wiring, the virtual wiring capacitances of 20,000 gates in circuit size are found to be 2.087 [LU] from Table 7-1. Because output pin X of the cell L1INX1 branches to three inputs, the wiring load capacitance, Load B, is calculated as follows:

Load B = 2.087 × 3 = 6.261 [LU]

Therefore, the delay in IN1 under Typ. conditions is calculated using Equation 7-1 as shown below.

Here, the symbol "↑" denotes the rise, and the symbol "↓" denotes the fall. The rise and fall here refer to the rising and falling transitions at output pin X.

$$T_{pd}(A\downarrow \rightarrow X\uparrow) = T_0(\uparrow) + K(\uparrow) \times (\sum \text{Load A} + \text{Load B})$$
$$= 43 + 18.7 \times (4.0 + 6.261)$$
$$= 234.9 \text{ [ps]}$$

$$T_{pd}(A\uparrow \rightarrow X\downarrow) = T_0(\downarrow) + K(\downarrow) \times (\sum \text{Load A} + \text{Load B})$$
$$= 44 + 10.2 \times (4.0 + 6.261)$$
$$= 148.7 \text{ [ps]}$$

Next, calculate the path delay from IN to OUT1, OUT2, and OUT3. In this case, because OUT1, OUT2, and OUT3 are in a nonloaded state, the cell's inherent delay must be added to the above delay value. In the calculation of this path delay, furthermore, care must be taken with respect to the rise and fall of each output.

1) Delay in IN → OUT1 path = IN1 (A → X delay) + IN2 (A → X delay)

$$T_{pd}(IN\uparrow \rightarrow OUT1\uparrow) = T_{pd}(IN\uparrow \rightarrow OUT0\downarrow) + T_{pd}(OUT0\downarrow \rightarrow OUT1\uparrow)$$
$$= 148.7 + 36$$
$$= 184.7 \text{ [ps]}$$

$$T_{pd}(IN\downarrow \rightarrow OUT1\downarrow) = T_{pd}(IN\downarrow \rightarrow OUT0\uparrow) + T_{pd}(OUT0\uparrow \rightarrow OUT1\downarrow)$$
$$= 234.9 + 37$$
$$= 271.9 \text{ [ps]}$$

2) Delay in IN → OUT2 path = IN1 (A → X delay) + NA2 (A1 → X delay)

$$T_{pd}(IN\uparrow \rightarrow OUT2\uparrow) = T_{pd}(IN\uparrow \rightarrow OUT0\downarrow) + T_{pd}(OUT0\downarrow \rightarrow OUT2\uparrow)$$
$$= 148.7 + 57$$
$$= 205.7 \text{ [ps]}$$

$$T_{pd}(IN\downarrow \rightarrow OUT2\downarrow) = T_{pd}(IN\downarrow \rightarrow OUT0\uparrow) + T_{pd}(OUT0\uparrow \rightarrow OUT2\downarrow)$$
$$= 234.9 + 50$$
$$= 284.9 \text{ [ps]}$$

3) Delay in IN → OUT3 path = IN1 (A → X delay) + NO2 (A1 → X delay)

$$T_{pd}(IN\uparrow \rightarrow OUT3\uparrow) = T_{pd}(IN\uparrow \rightarrow OUT0\downarrow) + T_{pd}(OUT0\downarrow \rightarrow OUT3\uparrow)$$
$$= 148.7 + 59$$
$$= 204.7 \text{[ps]}$$

$$T_{pd}(IN\downarrow \rightarrow OUT3\downarrow) = T_{pd}(IN\downarrow \rightarrow OUT0\uparrow) + T_{pd}(OUT0\uparrow \rightarrow OUT3\downarrow)$$
$$= 234.9 + 53$$
$$= 287.9 \text{ [ps]}$$

(2) Delay time of output cells

The following describes the procedure for calculating the approximate amount of propagation delay time, using the circuits in Figure 7-2 as an example. The output pin has a capacitance of 100 pF added external to the chip.

Table 7-3 lists various characteristic values of dual power supply output cells excerpted from the cell library.

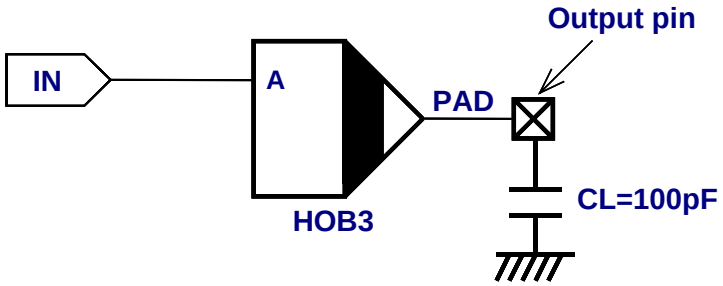


Figure 7-2 Example Circuit for Calculation of the External Cell Propagation Delay Time

Table 7-3 Delay Characteristics of Output Cells (Power Supply HV_{DD} = 3.3 V / LV_{DD} = 2.5 V)

Cell Name	Input		Output		Delay Characteristics (Typ.)				
	Pin	Fan-In [LU]	Pin	Fan-Out [LU]	From	To	Parameter	T_0 [ps]	K [ps/10pF]
HOB3	A	3.3	PAD	—	A	PAD	t_{pLH}	2406	166.7
							t_{pHL}	1712	211.6

The delay time in the output cell HOB3 under Typ. conditions is calculated using Equation 7-2, as shown below.

Here, the symbol "↑" denotes a rise, and the symbol "↓" denotes a fall. Here, these refer to the rising and falling transitions at the PAD for the output pin.

$$T_{pd}(IN\uparrow \rightarrow PAD\uparrow) = T_0(\uparrow) + K(\uparrow) \times 100\,(pF) / 10$$
$$= 2406 + 166.7 \times 100\,(pF) / 10$$
$$= 4073\ [ps]$$

$$T_{pd}(IN\downarrow \rightarrow PAD\downarrow) = T_0(\downarrow) + K(\downarrow) \times 100\,(pF) / 10$$
$$= 1712 + 211.6 \times 100\,(pF) / 10$$
$$= 3828\ [ps]$$

7.4 Fluctuations in Propagation Delay Time

The T_0 and K values used to calculate the propagation delay time in input and internal cells (shown in Equation 7-1) and in output cells (shown in Equation 7-2) vary with the operating voltage and ambient temperature, as well as with process conditions. The "S1X60000 Series MSI Cell Library" lists these values for Max., Typ., and Max. conditions, respectively. These conditions are defined below for your reference.

Min. condition: V_{DD} = highest value, T_a = lowest value, process = Fast
Typ. condition: V_{DD} = center value, T_a = 25°C, process = center value
Max. condition: V_{DD} = lowest value, T_a = highest value, process = Slow

The Min. and Max. condition propagation delays are important in confirming that circuit delays are within the desired range of specifications even when V_{DD}, Ta, or the process varies.

Coefficient M that represents a variation in Min/Max condition propagation delays can be calculated from Typ conditions by using Equation 7-3 below.

$$M = MV \times MT \times MP \quad \text{..... (Equation 7-3)}$$

where, MV: coefficient of power supply voltage fluctuation
MT: coefficient of ambient temperature fluctuation
MP: coefficient of process fluctuation

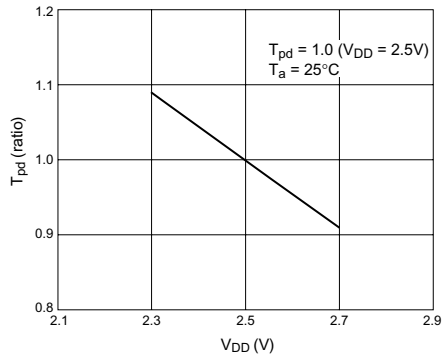
Table 7-4 shows the standard coefficient of delay variations (M); Figure 7-3 shows a graph indicating the MV and MT of MSI cells.

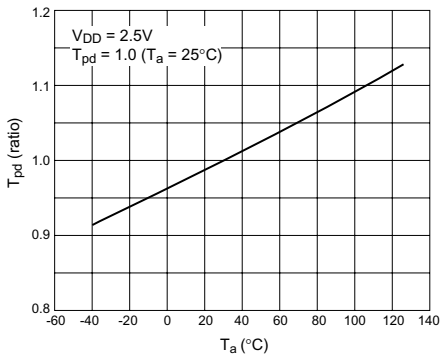
For other than the standard power supply voltage and ambient temperature ranges listed in Table 7-4, please contact the sales division of Epson.

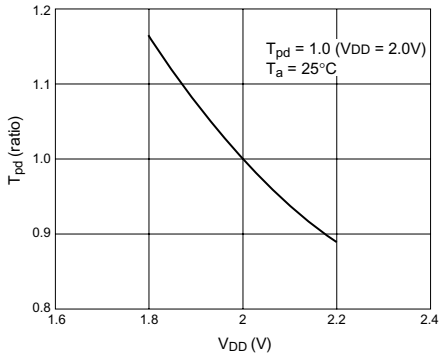
Table 7-4 Coefficient of Delay Variations (M)

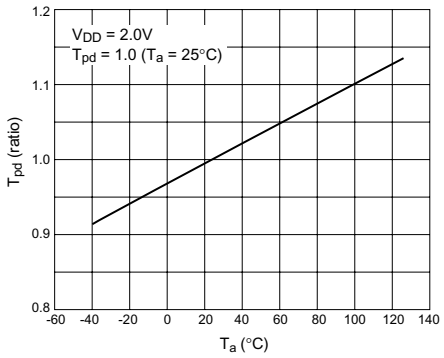
Conditions		M Value (T_a = 0 to +70°C*1)			M value (T_a = -40 to +85°C*2)		
		Min.	Typ.	Max.	Min.	Typ.	Max.
Input/output buffers	HV_{DD} = 3.3 V±0.3 V	0.72	1.00	1.39	0.68	1.00	1.44
	V_{DD} or LV_{DD} = 2.5 V±0.2 V	0.72	1.00	1.45	0.68	1.00	1.53
	V_{DD} or LV_{DD} = 2.0 V±0.2 V	0.69	1.00	1.53	0.65	1.00	1.56
MSI cells	V_{DD} = 2.5 V±0.2 V	0.75	1.00	1.40	0.70	1.00	1.48
	V_{DD} = 2.0 V±0.2 V	0.72	1.00	1.48	0.68	1.00	1.56

*1: This temperature range is based on the assumption that T_j = 0 to +85°C.
*2: This temperature range is based on the assumption that T_j = -40 to +125°C.









Propagation Delay vs.
Power Supply Voltage Characteristics

Propagation Delay vs.
Ambient Temperature Characteristics

Figure 7-3 Delay Characteristics of MSI Cells

7.5 Setup and Hold Times of the Flip-Flop (FF)

If the configured circuit is to operate properly with the desired logic, the timing of the signals applied to the sequential circuit of the FF or of an MSI built with FFs is important. The setup and hold times of FFs are closely related to this signal timing. Any data that is supplied after the setup time or that has changed state within the hold time cannot be written into the FF circuit properly. Therefore, these setup and hold times must be taken into consideration in the timing design.

(1) Minimum pulse width

This refers to the minimum length of time or the width from the leading to the trailing edge of an input pulse waveform in an FF or an MSI built with FFs. If a pulse narrower than that value is applied to the input, it may not only have no effect as a signal, but may also cause the FF to operate erratically.

There are the following three definitions of the minimum pulse width:

- Minimum pulse width of a clock signal
- Minimum pulse width of a set signal
- Minimum pulse width of a reset signal

(2) Setup time

For data to be properly read into an FF or an MSI built with FFs, the state of the data must be set before the active edge of the clock pulse changes. The time required for this is referred to as the “setup time.”

(3) Hold time

For data to be properly read into an FF or an MSI built with FFs, the state of the data must be maintained for some time after the active edge of the clock pulse is entered. The time required for this is referred to as the “hold time.”

(4) Release time (setup)

A finite length of time must elapse before the clock pulse can change state after the state of the set/reset input is released in an FF or an MSI built with FFs. This time is referred to as the “release time (setup).”

(5) Removal time (hold)

The state of the set/reset input must be maintained for some time after the clock pulse is entered in an FF or an MSI built with FFs. This time is referred to as the “removal time (hold).”

(6) Set/reset setup time (recovery)

A finite length of time must elapse before the reset input can be driven high after the state of the set input is released in an FF or an MSI built with FFs. This time is referred to as the “set/reset setup time.”

(7) Set/reset hold time (recovery)

The signal state must be maintained for some time before the set signal is driven high after the reset signal is driven high in an FF or an MSI built with FFs. This time is referred to as the “set/reset hold time.”

For details regarding the timing error message during the simulation, refer to the manual of each tool.

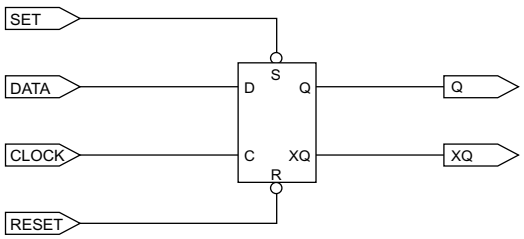


Figure 7-4 DFSR

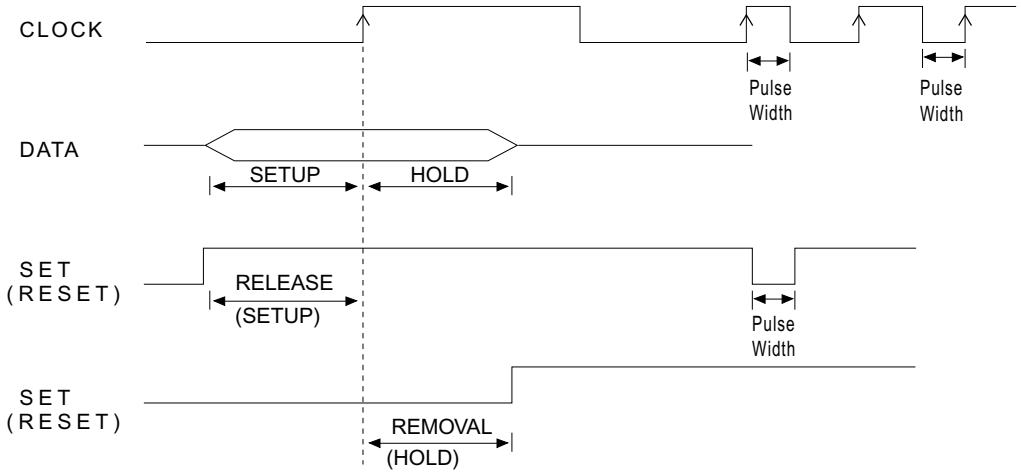


Figure 7-5 Timing Waveform 1 (for Definitions (1) to (5))

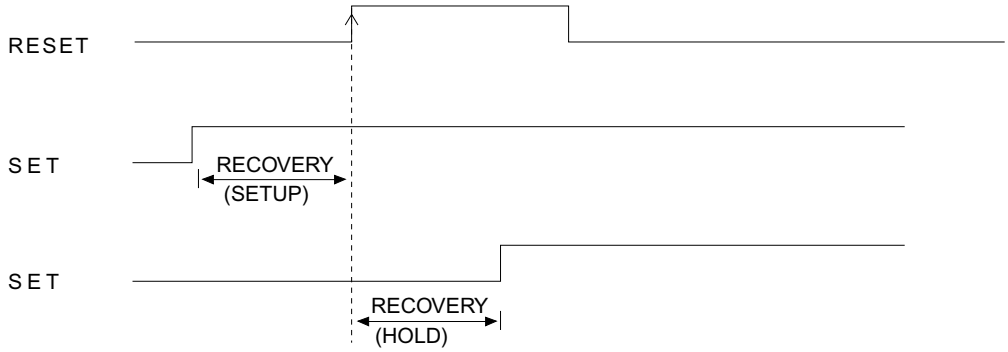


Figure 7-6 Timing Waveform 2 (for Definitions (6) to (7))

The setup/hold times of FFs in the S1X60000 series are listed in the "S1X60000 Series MSI Cell Library" in the form shown in Table 7-1. When actually using the S1X60000 series, please refer to the characteristics of each cell.

Chapter 8 Estimating Power Consumption

Virtually no current flows through the chip of a CMOS LSI when it is not in operation. However, during operation it consumes an amount of power corresponding to its operating frequency. The greater the power consumption, the higher the LSI chip temperature. An excessively high chip temperature adversely affects LSI quality.

Therefore, the power consumption of LSI chips must be calculated to verify whether it is within the range of the chip's permissible power consumption.

This chapter describes the procedure for calculating the power consumption of all chips in the S1X60000 series of products.

8.1 Calculation of Power Consumption

The power consumption of CMOS circuits generally depends on the circuit's operating frequency, load capacitance, and power supply voltage (this does not include special products such as analog circuits in which a steady state current flows in the chip).

To calculate the power consumption of the entire chip, first find the power consumption of each block of the internal circuit, and then find the sum total for all blocks of the internal circuit. Next, find the power consumption of the input and output buffers. The sum total of these is the total amount of power consumption to be obtained.

The total amount of power consumption, P_{total}, is calculated using the equation below.

$$P_{total} = P_{int} + P_i + P_o$$

where, P_{int} : power consumption of the internal circuit
P_i : power consumption of the input buffers
P_o : power consumption of the output buffers

8.1.1 Internal Cells (P_{int})

The power consumption of internal cells varies with the gate counts used, efficiency of cell usage, operating clock frequency, and percentage of cells operating with that clock frequency, and is calculated using the equation below.

$$P_{int} = \sum_{i=1}^{K} \{(Nb \times U) \times fi \times Spi \times Kpint\} \text{ [W]}$$

where, Nb : total BC counts of the circuit
U : efficiency of cell usage
fi : operating clock frequency of I'th cell [MHz]
Spi : ratio of BCs to all cells operating with clock frequency fi [MHz] (Although this ratio varies with the content of each system, it may generally be considered to be in the range of 20% to 30%.)
Kpint: power consumption per BC (listed in Table 8-1)

Table 8-1 Kpint per BC of the S1X60000 Series

V_{DD} (TYP)	Kpi
V_{DD} = 2.5 V, LV_{DD} = 2.5 V	0.18 µW / MHz
V_{DD} = 2.0 V, LV_{DD} = 2.0 V	0.11 µW / MHz

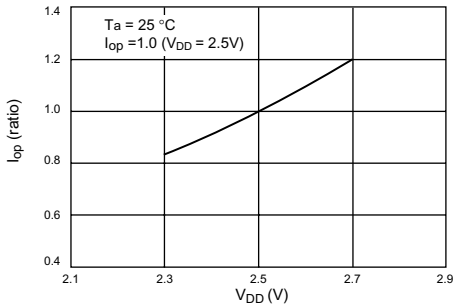


Figure 8-1

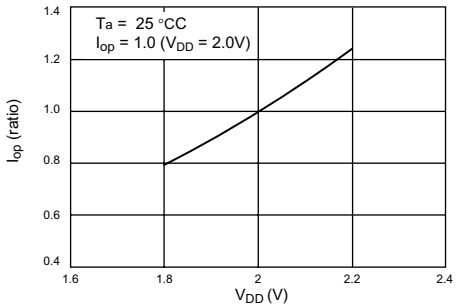


Figure 8-2

8.1.2 Input Buffers (P_i)

The power consumption of input buffers is obtained as the sum total of the frequencies of the input signals supplied to the respective buffers, f [MHz], multiplied by Kpi [µW/MHz].

$$P_i = \sum_{i=1}^{K} (Kpi \times fi) \ [\mu W]$$

where, fi : operating frequency of I'th input buffer [MHz]
Kpi: voltage coefficient of the input buffer (see Table 8-2)

Table 8-2 Kpi for Input Cells in the S1X60000 Series

V_{DD} (TYP)	Kpi
HV_{DD} = 3.3 V	3.8 µW / MHz
V_{DD} = 2.5 V, LV_{DD} = 2.5 V	2.6 µW / MHz
V_{DD} = 2.0 V, LV_{DD} = 2.0 V	1.6 µW / MHz

8.1.3 Output Buffers (P_o)

The power consumption of output buffers differs between DC load (e.g., resistive load or when connected to TTL devices) and AC load (e.g., capacitive load or when connected to CMOS devices).

If the DC power consumption and AC power consumption are assumed to be P_{DC} and P_{AC}, respectively, then the power consumption of the output buffers to be obtained, P_o, is expressed by the equation below.

$$P_o = P_{AC} + P_{DC}$$

8.1.3.1 AC Power Consumption (P_{AC})

With an AC load, the power consumption of the output buffers can be roughly calculated using the equation below.

$$P_{AC} = \sum_{i=1}^{K} \{fi \times C_L \times (V_{DD})^2\}$$

where, fi : operating frequency of the output buffer [Hz]
C_L : output load capacitance [F]
V_{DD}: power supply voltage [V]

8.1.3.2 DC Power Consumption (P_{DC})

With a DC load, the power consumption of the output buffers can be roughly calculated using the equation below.

$$P_{DC} = P_{DCH} + P_{DCL}$$

where, $P_{DCH} = |I_{OH}| \times (V_{DD}^* - V_{OH})$
$P_{DCL} = I_{OL} \times V_{OL}$

Here, the ratio of P_{DCH} to P_{DCL} is determined by the duty cycle of the output signal.

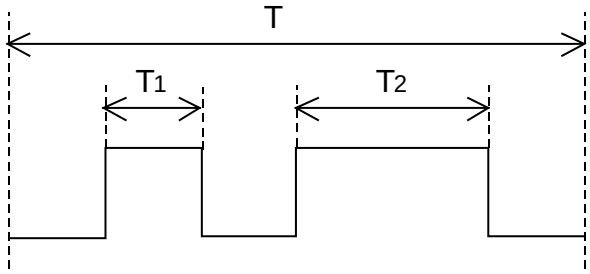


Figure 8-3 Example of a Duty Cycle

Using Figure 8-3 as an example, we find

$$\text{Duty H} = (T_1 + T_2) / T$$
$$\text{Duty L} = (T - T_1 - T_2) / T$$

From the above,

$$P_{DC} = P_{DCH} + P_{DCL}$$
$$= \sum_{i=1}^{K} \{ (V_{DD}^* - V_{OH}i) \times I_{OH}i \times \text{Duty H} \} + \sum_{i=1}^{K} [V_{OL}i \times I_{OL}i \times \text{Duty L}]$$

* For dual power supplies, V_{DD} represents HV_{DD} or LV_{DD}.

8.2 Limitations on Power Consumption

The chip temperature of LSIs increases according to their power consumption. When encapsulated in a package, the LSI's chip temperature may be calculated from its ambient temperature, T_a, the thermal resistance of the package, $\theta j\text{-}a$, and the power dissipation of the LSI, PD.

$$\text{Chip temperature } (T_j) = T_a + (PD \times \theta j\text{-}a) \text{ [°C]}$$

When used under normal conditions, make sure the chip temperature (T_j) is 125°C or less.

See Table 8-3 for the thermal resistance of each type of package. The thermal resistance values shown in this table vary significantly depending on how the chip is mounted on the board and whether it is forcibly air cooled.

Table 8-3 Thermal Resistance of Each Type of Package (Suspended Singly)

ALLOY42

Package Type	Pin Counts	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	100	110(°C/W)	75	60	55
QFP5	128	110	75	60	55
QFP8	128	65	—	—	—
QFP8	208	45	—	—	—
QFP12	48	230	—	—	—
QFP13	64	170	—	—	—
QFP14	80	110	—	—	—
QFP15	100	115	50	45	35
QFP20	144	85	70	50	40
TQFP14	80	100	—	—	—
TQFP14	100	100	—	—	—
TQFP15	100	110	—	—	—

CFLGA (mounted on the board, free of wind)

Package Type	Customer's Board Size	Chip Size		
		3.82 mm x 3.82 mm	5.73 mm x 5.73 mm	9.55 mm x 9.55 mm
CFLGA424	75 mm	44.0 (°C/W)	32.9	24.6
	50 mm	46.9	36.4	27.8
	30 mm	61.1	50.1	42.1
CFLGA307	75 mm	44.0	33.1	24.9
	50 mm	47.1	37.4	28.5
	30 mm	61.7	51.5	43.1
CFLGA239	75 mm	44.0	33.1	25.1
	50 mm	47.3	38.3	29.2
	30 mm	62.2	52.9	43.9
CFLGA152	75 mm	44.8	34.4	—
	50 mm	48.8	39.7	—
	30 mm	63.3	53.9	—
CFLGA104	75 mm	45.5	35.6	—
	50 mm	50.3	41.1	—
	30 mm	64.3	54.9	—

Cu-L/F

Package Type	Pin Counts	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	80	85 (°C/W)	55	45	40
QFP5	100	80	55	35	30
QFP5	128	80	55	35	30
QFP8	160	45	32	25	23
QFP8	256	50	—	—	—
QFP10	304	35	20	16	—
QFP12	48	175	120	90	80
QFP13	64	130	80	55	50
QFP14	80	110	—	—	—
QFP15	100	90	—	—	—
QFP20	184	65	—	—	—
QFP21	176	55	—	—	—
QFP21	216	55	—	—	—
QFP22	208	45	35	25	23
QFP22	256	45	35	25	23
QFP23	184	40	—	—	—
QFP23	240	40	—	—	—
TQFP12	48	165	—	—	—
TQFP13	64	140	—	—	—
TQFP15	128	105	—	—	—
TQFP24	144	80	—	—	—
HQFP5	128	60	—	—	—
HQFP8	160	32	19	12	10
H2QFP8	208	34	—	—	—
H2QFP23	240	30	—	—	—
H3QFP15	128	85	—	—	—

PBGA

Package Type	Pin Counts	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
PBGA	225	72 (°C/W)	46	37	—
PBGA	256	53	33	25	—
PBGA	388	45	—	—	—

Chapter 9 Circuit Design

9.1 Basic Circuit Configuration

9.1.1 Inserting Input/Output Buffers

Signals outside and inside an LSI can only be exchanged via input/output buffers. Always be sure to insert input or output buffers between the external pins and the internal cells of an LSI.

This is necessary because CMOS LSIs are extremely susceptible to static electricity, and the input/output buffers contain a circuit that protects them against static electricity.

9.1.2 Limitations on Logic Gate Output Load

CMOS circuits are such that, as the load capacitance of the output increases, so does the propagation delay time of signals (t_{pd}). At the same time, the rise and fall times of signal waveforms (t_{slew}) increase.

If logic gates have an excessively large output load capacitance, signal delay may concentrate at a specific circuit node, thereby limiting the operating speed or deteriorating the simulation accuracy of the logic gate's propagation delay time, which in turn could cause the logic gate to operate erratically. Furthermore, because the change period of signals is extended, the logic gate may become susceptible to noise.

To ensure that logic gates have an appropriate load in the circuit design stage, limitations known as "Fan-Out" limits are provided to limit the load that can be connected to the logic gate. The input pins of logic gates each have a specific input capacitance defined as the "Fan-In," which is a relative quantity referenced to the input capacitance of inverter cell (IN1) =1. On the other hand, Fan-Out limits are expressed as the sum total of Fan-In counts, which can be connected to the output pin of each logic gate. In the design of your circuit, make sure the sum total of the Fan-In counts connected to the output pin of each logic gate will not exceed the Fan-Out limits for that output pin. For logic gates such as clock lines that operate at high speed (operating frequency of 60 MHz or higher), make sure the load on their output pins is approximately half the ordinary Fan-Out limits.

The output-pin load capacitance of logic gates in an actual LSI consists of the input capacitance of gates in the next stage plus the wiring capacitance of signals. Because the exact wiring capacitance is determined through placement and routing in the circuit, a large load capacitance may be applied to specific nodes during placement and routing, depending on how the work is performed. The load condition at each circuit node can be verified from the output results of t_{slew}. If the output results suggest that the load condition exceeds the rated value, customers may be requested to correct the circuit in order to suppress the load to within the limits. To suppress increases in load capacitance after placement and routing work has been performed, minimize circuit branches at a single node or, if branching, use buffers with large Fan-Out.

9.1.3 Wired Logic Forbidden

Because the S1X60000 series cells use CMOS transistors, they cannot be configured with wired logic as in bipolar transistors. As a result, the output pins of cells cannot be connected together, as shown in Figure 9-1. Only in the bus circuit configuration is it possible to connect the output pins together.

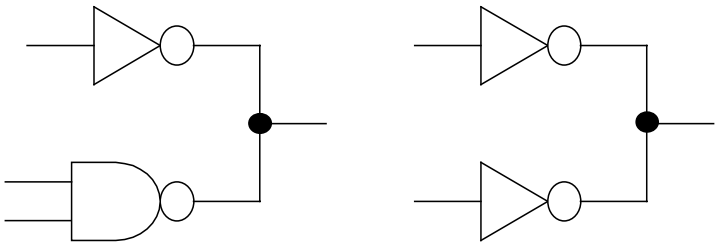


Figure 9-1 Examples of Forbidden Wired Logic

9.1.4 Synchronized Design Recommended

For the logic circuit design, we recommend synchronized design in which all registers are basically clocked from a common timing signal source. Synchronized design provides numerous advantages. For example, it is suitable for high speed circuits because register to register operations can easily be timed. It can make use of various EDA tools, such as Clock Tree Synthesis, DFT, and STA. In addition, because it does not depend on technology-inherent characteristics, circuits can easily be reused.

Ideally speaking, synchronized circuits have the following characteristics:

1. All registers in the circuit operate with either the rising or falling edge of a single clock signal.
2. No feedback loops are based on a combinational circuit (see Figure 9-2).
3. No pulse generator circuits that make use of a circuit delay are included (see Figure 9-3).
4. Other than the system reset, no asynchronous resets are used (this also applies to asynchronous sets).

Although in reality it may be difficult to design a circuit in which registers are clocked by a single clock signal, we recommend using as few clock signals as possible. The greater the number of clock signals used and the greater the complexity of the mutual relationships between them, the more time is required for circuit design, including the operation of said EDA tools, and the less likely it is to obtain satisfactory output results.

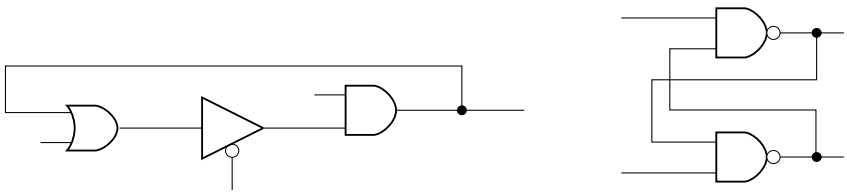


Figure 9-2 Example of a Feedback Loop

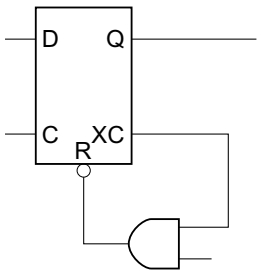


Figure 9-3 Example of a Delay-Based Pulse-Generator Circuit

9.2 Use of Differentiating Circuits Forbidden

The propagation delay time of each element in an LSI, t_{pd}, varies depending on the working environment (e.g., voltage and temperature) and manufacturing conditions. For this reason, care must be taken in the use of differentiating circuits that make use of the difference in relative t_{pd} times(see Figure 9-4), as a sufficient pulse width may not be obtained depending on the working environment and manufacturing conditions, causing the circuit to operate erratically.

When a differentiating circuit is needed, avoid using the circuit shown in Figure 9-4 and, instead, use a circuit built with FFs like the one shown in Figure 9-5.

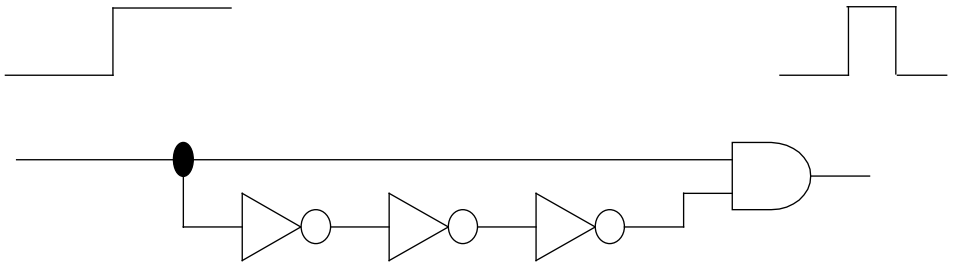


Figure 9-4 Example of a Bad Differentiating Circuit

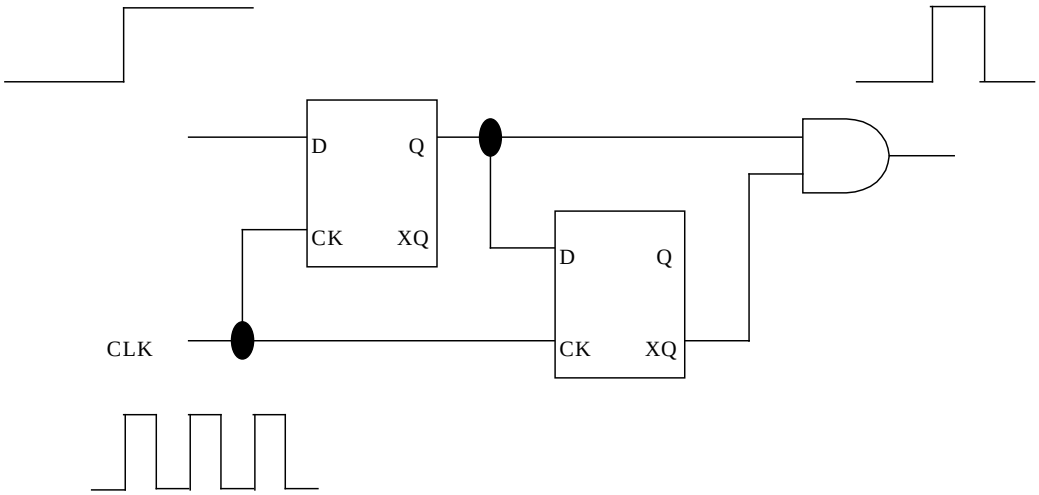


Figure 9-5 Example of a Differentiating Circuit Built with FFs

9.3 Clock Tree Synthesis

9.3.1 Overview

Clock Tree Synthesis is a service that allows a tree of buffers to be inserted automatically in order to optimize the skew and delay values of clock lines. When circuits are designed by customers, they often insert clock trees as a means of adjusting the Fan-Out of clock lines or for other purposes. In such a case, because clock trees are placed and routed so as to be suitable for the placement and routing tool, the clock skew and wiring delay tend to increase. Therefore, we recommend that buffers not be inserted in clock lines for Fan-Out adjustment purposes; instead, we recommend that you receive this service from Epson.

For circuits that also contain gated cells **(simple gates)** in clock lines, Clock Tree Synthesis helps optimize the skew and delay values of clock lines.

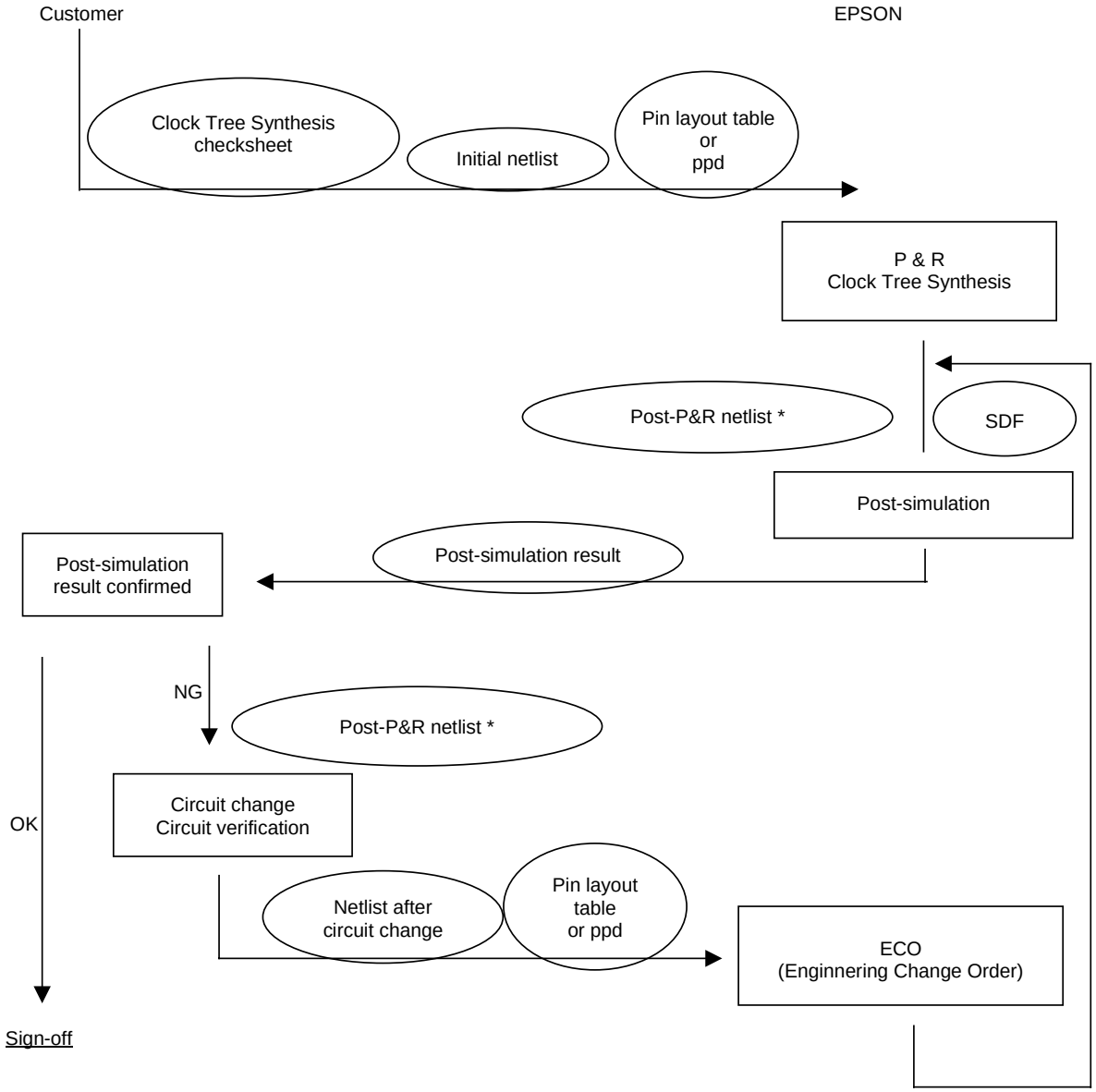
Before Clock Tree Synthesis can be applied, customers are requested to insert dedicated buffers or dedicated gated cells in clock lines for the following three purposes:

(1) To determine the location at which Clock Tree Synthesis is applied

(2) To perform temporary wiring level simulation (pre-simulation) using the predicted delay values of clock trees to be inserted

(3) To back annotate after replacing the inserted clock trees with delay information, in order to perform precise post-simulation

9.3.2 Design Flow



(ECO is a method for performing placement and routing only in locations where the circuit has been changed.)

[Notes]

- The post-P&R netlist contains buffers that have been added in Clock Tree Synthesis.
- Post-simulation uses the netlist and sdf, which contain the buffers that have been added in Clock Tree Synthesis.
- If the result of post-simulation is No Good (NG), correct the post-P&R netlist. If the initial netlist has been corrected, P&R must be reexecuted.
- If circuit changes are made to the clock net part (dedicated buffer, dedicated gated cell, and DEF), P&R must basically be reexecuted. If it is necessary to change the clock net part, please consult with Epson.

9.3.3 Applying Clock Tree Synthesis

Refer to Table 9-2, "Dedicated Buffers," for the selection of Clock Tree Synthesis only buffers, and to Table 9-3, "Cell Names of Dedicated Gating Cells," for the selection of Clock Tree Synthesis only gating cells. In addition, after gaining an understanding of the Limitations and Notes in Section 9.3.4, refer to Reference Circuit Diagram 1 when inserting the dedicated buffers or dedicated gating cells that you've selected.

For logic synthesis based design, because the dedicated buffers and dedicated gating cells cannot be automatically inserted, use direct language descriptions. In such a case, to ensure that the clock line in which dedicated buffers or dedicated gating cells have been inserted will not have other buffers or the like synthesized in it, execute the following command in the Design Compiler:

set_dont_touch_network clock_*name*

Table 9-1 Criteria for Appropriate Skew Values

Standard Fan-Out Counts	Without Gating Cells	With Gating Cells
0 to 500	±200 ps	±300 ps
500 to 3000	±250 ps	±400 ps
3000 to 10000	±300 ps	±500 ps
10000 or more	±350 ps	±600 ps

Notes:

- The criteria for appropriate skew values change according to the circuit size, wiring congestion, and number of clock lines.
- Make sure the number of gated cells inserted is not more than 20, and that the number of stages does not exceed one.
- The above criteria for appropriate skew values when gating cells are included apply to cases in which not more than 20 gating cells are inserted and there are not more than one stage.
- If more gating cells are inserted so as to exceed the limit of three stages, skew-derived timing errors may occur during post-simulation. To avoid delays in development schedules, try to minimize the number of gating cells used.

Table 9-2 Dedicated Buffers

S1X60000 Series		
Cell Name	**T_0 Max (ns)**	**Standard Fan-Out Counts**
CRBF2	2.00	0 to 500
CRBF3	3.00	500 to 3000
CRBF4	4.00	3000 to 10000
CRBF5	5.00	10000 or more
CRBF6	6.00	
CRBF7	7.00	
CRBF8	8.00	

Notes:

- The pre-simulation time K value (delay due to Fan-Out) for these cells is set to 0.

- The Fan-Out counts for these cells are set to infinite.
- The delay values relative to the Fan-Out counts fluctuate depending on the design size and usage efficiency. Therefore, use them for reference purposes only in the design of a circuit.

Table 9-3 Cell Names of Dedicated Gating Cells

Circuit Configuration (Function)	Cell Name
AND	CAD2V
OR	COR2V
2-1 Selector	CAO24AV
NAND	CNA2V
NOR	CNO2V
2-1 Selector	CAN24AV
INVERTER	CGIN4
Latch-based AND	CLAD2V
Latch-based OR	CLOR2V
Latch-based AND with test pin	CLPSAD2V
Latch-based OR with test pin	CLPSOR2V

The Gating Cells available include latch-based gating cells. When using this type of cell, there is no propagation of switching glitches in the clock wiring. Consequently, the clock signal is stabilized.

Refer to the "S1X60000 Series MSI Cell Library" for the functional configuration of latch-based gating cells.

Notes:

- The pre-simulation time delay value (T_0) for these cells is set to 0.
- The pre-simulation time K value (delay values due to Fan-Out) for these cells is set to 0.
- The Fan-Out counts for these cells are set to infinite.

9.3.4 Limitations and Notes

- When Clock Tree Synthesis is applied, the number of gates in the circuit for which it is applied increases by approximately 10% to 30%.
- If a large number of gating cells are inserted, skew derived timing errors may occur during post-simulation. To avoid causing delays in development schedules, try to minimize the number of gating cells used.
- The dedicated buffers and dedicated gating cells can only be used in Clock Tree Synthesis, and cannot be used for any other purposes.
- Clock Tree Synthesis can also be used for data lines and control, or for other signal lines. However, applying Clock Tree Synthesis to a large number of nets results in an increase in the skew or delay. Therefore, make sure Clock Tree Synthesis is not applied to more than 10 nets, and that it is applied only to critical nets with large Fan-Out.
- If Clock Tree Synthesis is applied to nets with small Fan-Out, the delay or skew may increase. Make sure Clock Tree Synthesis is applied only to nets with a Fan-Out of several tens or more.
- If the clock line contains any cell other than the dedicated gating cells, skew may occur during pre-simulation. Therefore, make sure only the dedicated gating cells are inserted in the clock line.
- Always be sure to use the dedicated gating cells in combination with the dedicated buffers. Note that if only the dedicated gating cells are used inadvertently, the skew and delay values cannot be optimized.
- As the number of dedicated gating cells inserted in one clock net increases, so do the skew and delay values. Therefore, limit the number of dedicated gating cells inserted in one clock net to a maximum of 20.
- As the number of stages comprised of dedicated gating cells increases, so do the skew and delay values. Therefore, limit the number of stages comprised of dedicated gating cells to a maximum of one.
- Skew adjustment, by default, is applied to cells such as DFFs and latch cells that contain clock pins. If skew adjustment is required for other than DFFs and latch cells, i.e., cells without clock pins, please contact Epson.
- If the net for which Clock Tree Synthesis is used is connected to megacell input pins, skew adjustment is not applied beyond the megacell input pins.
- Do not insert the dedicated buffers in two or more stages. Note that if the clock net contains dedicated buffers, the skew and delay cannot be optimized.

9.3.5 Clock Tree Synthesis Checksheet

When applying Clock Tree Synthesis, customers are requested to provide Epson with the following information. Your cooperation is appreciated.

● Target Skew Value and Target Delay Value

Instance Name of CRBF*	Target Skew Value (Max.) (SIM condition: Max.)	Target Delay Value (Min./Max.) (SIM condition: Max.)

Notes:
- The target values are used for reference purposes only when they are applied to Clock Tree Synthesis, and cannot be guaranteed to be satisfied.

1. Is the number of clock lines within 10? Yes • No
2. Does the clock net contain dedicated gating cells? Yes • No
   If you answered Yes to both of the above two questions, please answer questions 3 to 8 below.
3. Is the number of dedicated gating cells included in each clock net within 20? Yes • No
4. Is the number of stages comprised of dedicated gating cells within 1? Yes • No
5. Does the clock net contain dedicated buffers? Yes • No
6. Does the clock net contain any cell other than the dedicated gating cells? Yes • No
   If Yes, write the cell name below.

   _____

   [Notes]
   - If 3-input ANDs are handled as special gating cells, for example, the 3-input ANDs in all clock lines are handled as special gating cells.
   - DFFs and latches cannot be handled as special gating cells.
7. Do you want skew adjustment to be applied to other than DFFs and latches? Yes • No
   If Yes, specify the cell names and input-pin names.

   Cell name: _____ Pin name: _____ Cell name: _____ Pin name: _____

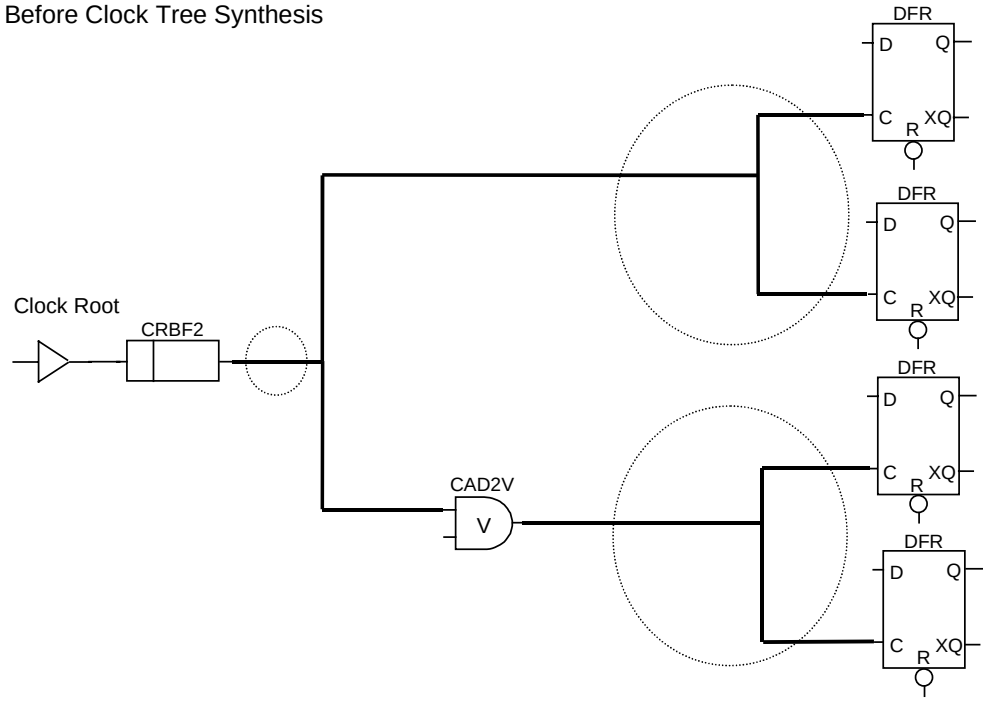
   [Notes]
   - If you specify inverters to be skew-adjusted, for example, the inverter cells in all clock lines are adjusted for skew.
8. Does any circuit configuration like Reference Circuit Diagram 2 included herein exist? Yes • No

   [Notes]
   - The clock net for both DFFs, one in part A and one in part B of the diagram, cannot be optimized for skew. If the DFFs in both parts A and B must be adjusted for skew, add dummy cells “CAO24AV” as shown in Reference Circuit Diagram 2.
9. Does any circuit configuration like Reference Circuit Diagram 3 included herein exist? Yes • No

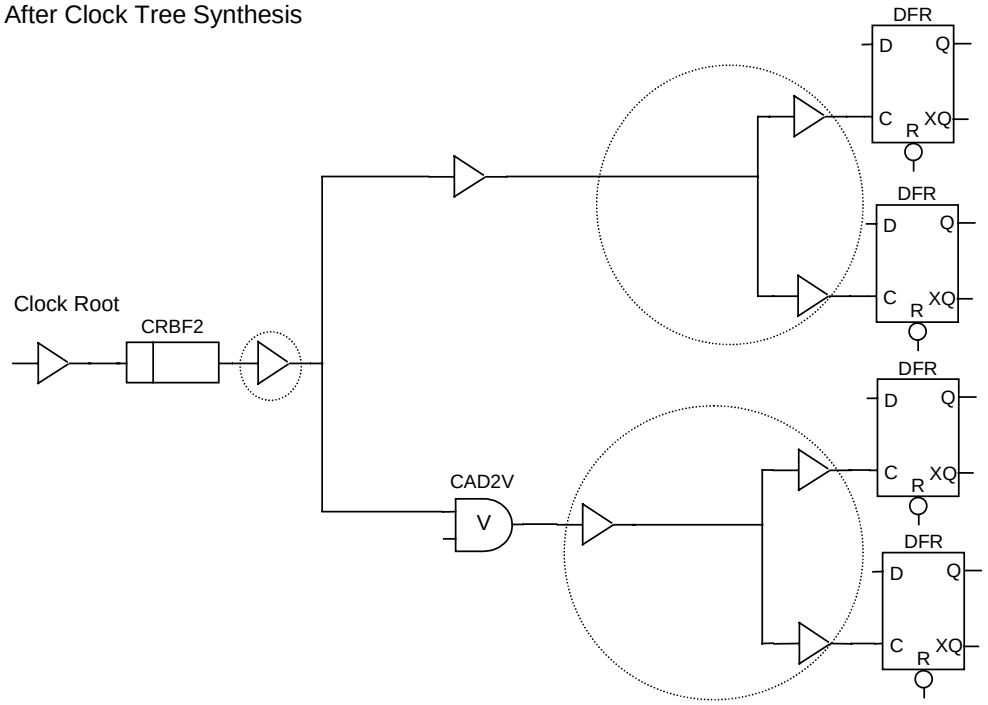
   [Notes]
   - The DFF in part A of the diagram is driven from both clock roots A and B. The DFF in part A cannot be adjusted for skew in both clock roots A and B. The “CRBF” for clock root B in Reference Circuit Diagram 3 must be deleted.

9.3.6 Attached Materials

9.3.6.1 Concept of the Implementation of Clock Tree Synthesis



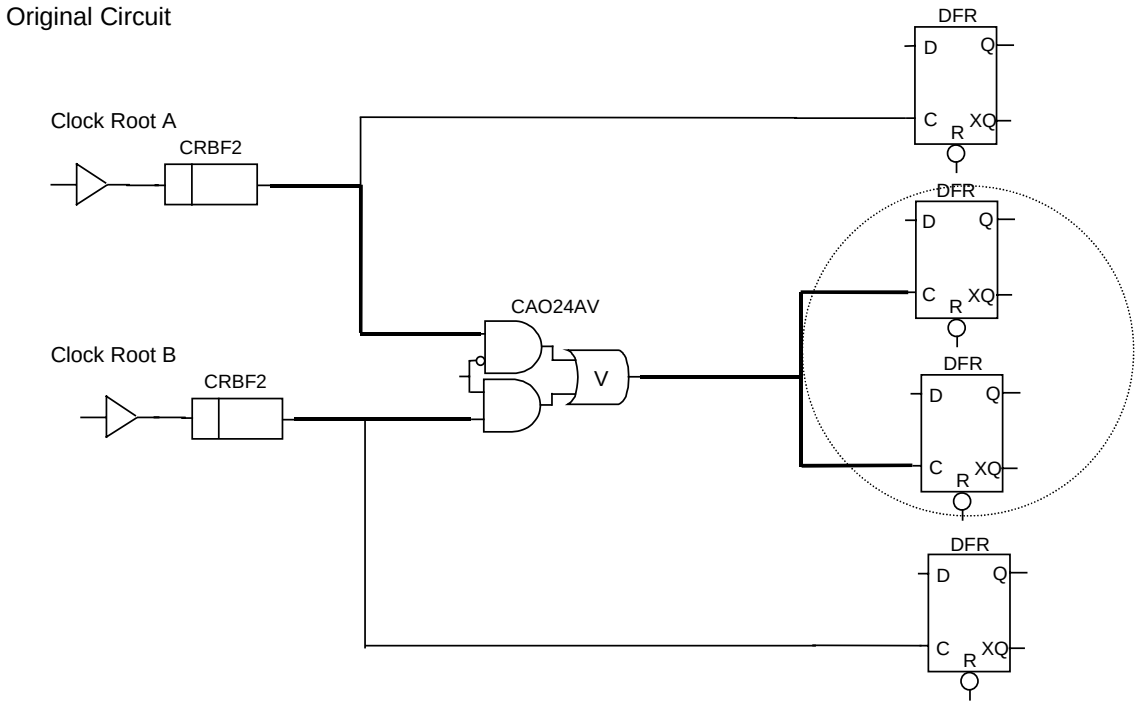
Clock Tree Synthesis optimizes the skew value for the thick-lined parts.



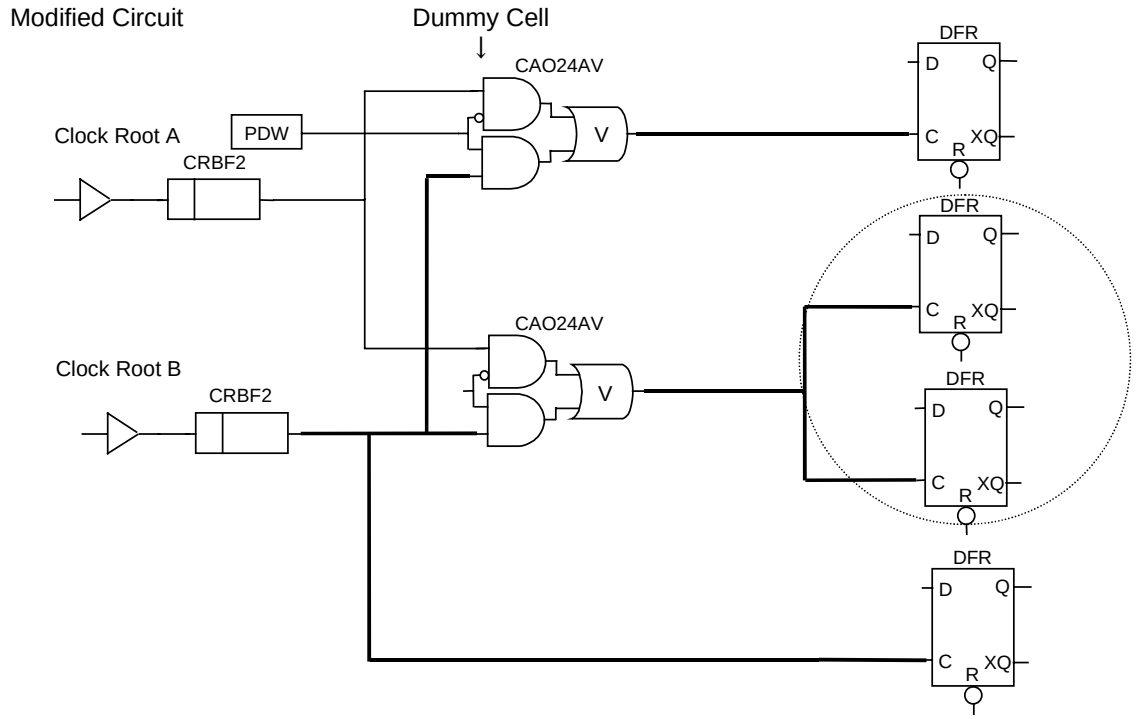
Reference Circuit Diagram 1

When Clock Tree Synthesis is applied, buffers are inserted within the dotted circles of the above circuit.

9.3.6.2 Example of Handling of a Problem Circuit–1



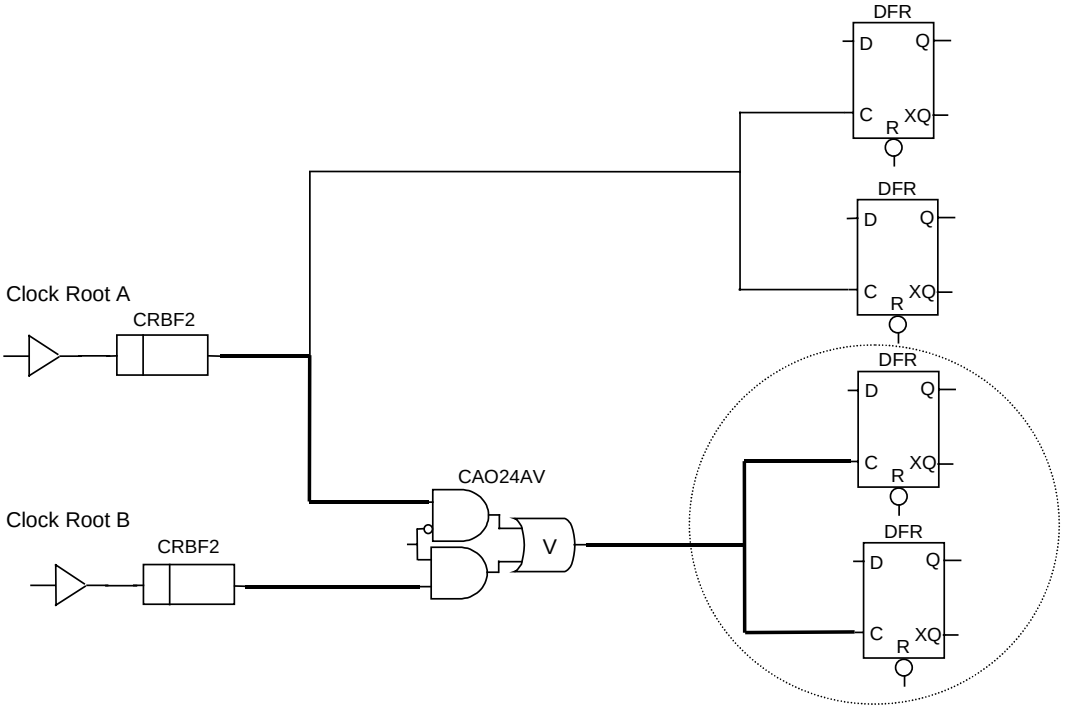
Clock Tree Synthesis cannot be executed for the DFFs connected in the thick-lined part, as they are driven from both clock roots A and B.



Reference Circuit Diagram 2

The DFFs within the dotted circle of the original circuit are driven from both clock roots A and B. Clock Tree Synthesis cannot be applied to any circuit in this manner. In the case of a circuit such as that in this example, insert a dummy cell "CAO24AV," as shown in the corrected circuit. In such a case, Clock Tree Synthesis optimizes the skew value of the thick-lined part of the circuit.

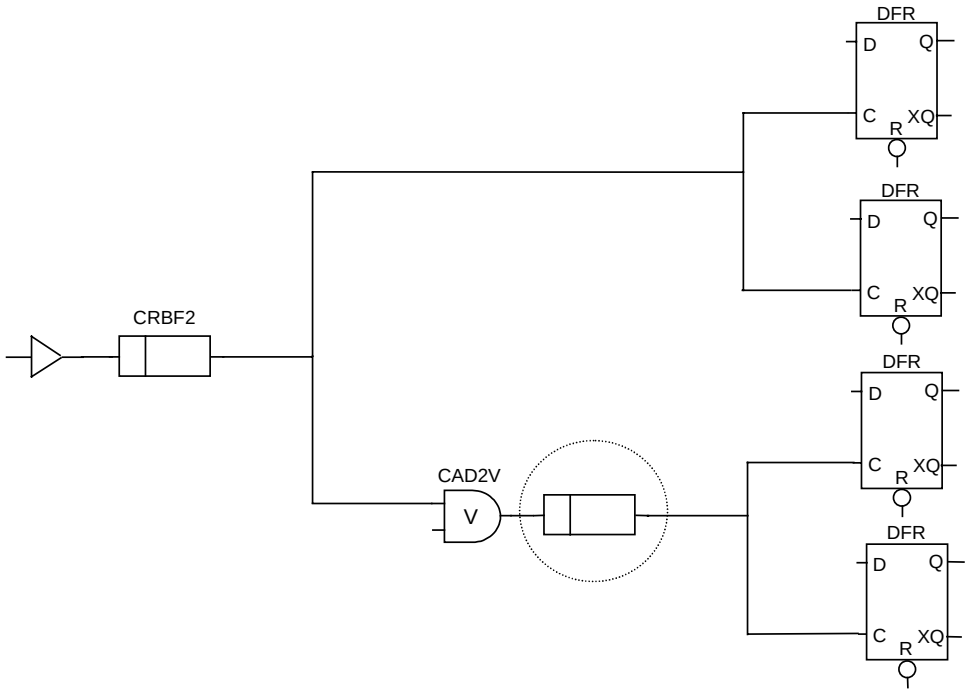
9.3.6.3 Example of Handling of a Problem Circuit–2



Reference Circuit Diagram 3

In the above circuit, the DFFs within the dotted circle are driven from both clock roots A and B. Clock Tree Synthesis cannot be applied to any circuit in this manner. In the case of a circuit such as that in this example, delete the cell "CRBF2" that is inserted in clock root B.

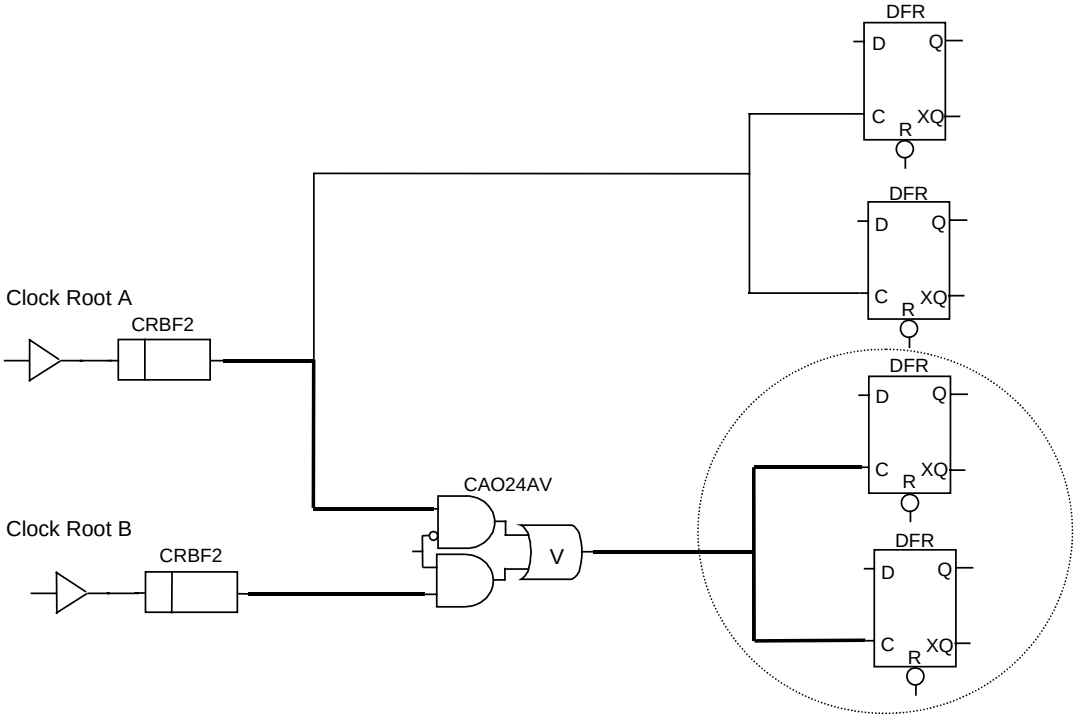
9.3.6.4 Problem Circuit 1



Reference Circuit Diagram 4

In the above circuit, the cell "CRBF2" is inserted in the stage following that of the CAD2V cell, which comprises multiple dedicated buffer stages. The CRBF2 cell in the stage following that of the CAD2V cell is unnecessary; therefore, it should be deleted.

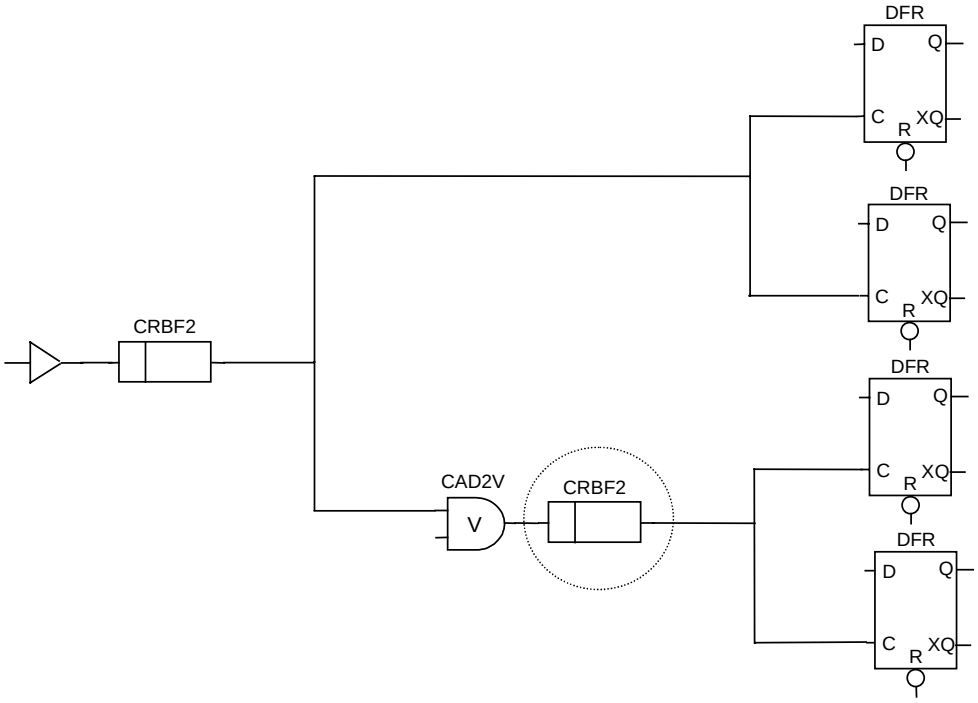
9.3.6.5 Problem Circuit 2



Reference Circuit Diagram 5

In the above circuit, the DFFs within the dotted circle are driven from both clock roots A and B. Clock Tree Synthesis cannot be applied to any circuit in this manner. In the case of a circuit such as that in this example, delete the cell “CRBF2” that is inserted in clock root B.

9.3.6.6 Problem Circuit 3



Reference Circuit Diagram 6

In the above circuit, the cell “CRBF2” is inserted in the stage following that of the CAD2V cell, which comprises multiple dedicated-buffer stages. The CRBF2 cell in the stage following that of the CAD2V cell is unnecessary; therefore, it should be deleted.

9.4 Designing Fast Operating Circuits

For fast operating circuits (operating frequency of 60 MHz or more), due to the reduced per-cycle time, the operable delay time has a small margin with respect to the propagation delay time. Therefore, devise appropriate countermeasures to minimize propagation delays by taking the precautions described below into consideration in the design of a circuit.

<Countermeasures for minimizing propagation delay>

- Avoid using NOR gates to configure the circuit. Instead, use NAND gates.*1
- Do not use a number of multi input logic elements unless absolutely necessary.*1
- For circuit parts with large branch counts, use tree structures that require few branches per drive element.*2
  Reduce the branch counts to a maximum of 10 or less.
- For fast operating logic elements (operating frequency of approximately 60 MHz), or for circuits with strict delay specifications, make sure the load on their output pins is approximately half or 1/3 of the ordinary Fan-Out limits in the design of a circuit.*2
- For logic elements connected at entry to separate modules or connected to macros and I/Os, select the high drive type.*2
- Remove restrictions, as much as possible, from circuit parts with large timing margins. (Because optimization by synthesis tends to start from paths with strict timing constraints, the run time can be reduced by deleting unnecessary timing constraints as much as possible. If circuits that have small timing margins or are in violation of timing specification exist in your design, please consult Epson before conducting synthesis.)

Notes) *1: Because the drive capability differs between the High and Low logic levels, delay time in the circuit may be smaller when the circuit is configured with NAND gates than when it is configured with NOR gates. Similarly, delay time in the circuit can be reduced by eliminating the use of multi-input logic elements in the circuit.

*2: In the circuit layout of the actual LSI, the load capacitance not only consists of the input capacitance of the next-stage element, but also includes the wiring capacitance of signals. Because the exact wiring capacitance is determined by placement and routing in the circuit, a specific node may be subjected to large load capacitance as a result of placement and routing. To suppress increases in load capacitance following placement and routing work, reduce the number of circuit branches at a single node as much as possible.

9.5 Metastable State

If the input signals for flip-flops or latch cells are in violation of timing specifications (such as the clock and data setup and hold times, or the clock and set/reset release or removable times), the output signals of the flip-flops or latch cells may be oscillating or at an intermediate voltage level, neither High nor Low, for a certain period of time. The instable state of output signals as in this case is referred to as the "metastable" state.

The metastable state ends after the elapse of a certain length of time, and the output is fixed to the High or Low level. However, because this fixed output level does not depend on the level of the input data, the output is indeterminate.

If the setup/hold or release/removal timing specification cannot be met, be sure to incorporate corrective measures in circuit design in order to ensure that such an instable state will not propagate to the entire circuit.

For the S1X60000 series, the duration of the metastable time in cases in which the designated values of the setup/hold or release/removal times cannot be satisfied is defined as a standard value, as follows:

$$\text{Metastable time} = T_{pd} \times 6$$

where, T_{pd}: delay time from the active edge of the clock or set/reset signal for a flip-flop or latch cell, until its output changes.

Because delay values in such a metastable state are not taken into consideration during logic simulation, always make sure a circuit being designed satisfies the timing specification.

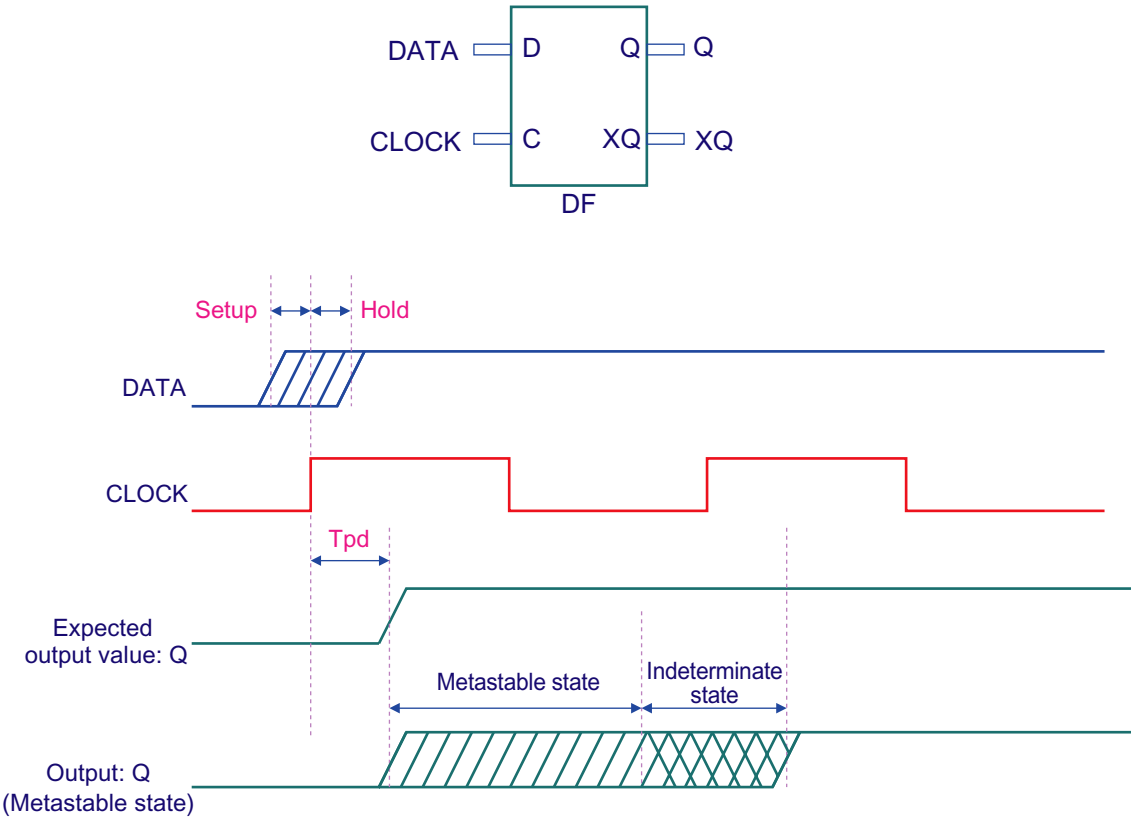


Figure 9-6 Metastable State of the DF

9.6 Configuration of the Internal Bus

The bus circuit is configured using 3-state logic circuits; therefore, one of the outputs connected to the bus is driven active (while the other output is placed in the high impedance state) through manipulation of the control signals for the bus, allowing one transmission signal line to be time shared.

The following describes the precautions to be taken when configuring an internal bus circuit using internal tri-state buffers.

- Bus cells can only be used in a bus circuit, and not in any other circuit (see Table 9-4 for the bus cells in the S1X60000 series).
- When configuring a bus circuit, add the bus latch cell *BLT.*
- Of the bus cells connected to one bus, only one output can be in an active state (logic 0 or 1), and all other bus-cell outputs must be placed in the high impedance (Hi-Z) state.*1
- The number of bus cells that can be connected to one bus must be within the Fan-Out limits.*2
- The bus circuit tends to have a large propagation delay time due to Fan-Out, making it unsuitable for high speed operation.*2
- The data retained by a bus latch cell can only be used to prevent the bus from floating, and cannot be used as a logic signal.*3
- When creating test patterns, exercise caution to ensure that the initial state of the bus can be determined easily.*4
- Make sure control signals for the bus change state only once within one cycle.

Notes) *1: If two or more of the bus cells connected to one bus are in an active state (logic 0 or 1) at the same time, the output voltage may not only become instable, but may also cause a steady current to flow between V_{DD} and GND. This limitation should always be taken into consideration.

*2: If an excessively large load is placed on the internal bus, the signal rise and fall times increase due to the increased wiring length and increased number of driven cells. This may result in a difference between the delay time in logic simulation and the delay time in the actual device.

*3: Even though all of the bus cells connected to one bus enter a high impedance (Hi-Z) state, data is retained by a bus latch cell. However, the latch's holding capability is restrained so as not to adversely affect operation. Do not use the retained output data as valid data.

*4: Configure the bus so as to improve its testability by, for example, adding test pins in order to increase the bus' controllability.

Table 9-4 Bus Cells Available in the S1X60000 Series

Cell Type	Celle Name		
	1 BIT	**4 BIT**	**8 BIT**
Bus latches	BLT 1	BLT 4	BLT 8
Bus driver	TSB, TSB 4, TSB8, TSBP	T 244H	T 244
Inverting bus driver	TSV, TSV 4, TSV8, TSVP	T 240H	T 240
Transparent laches with reset and 3-state output	—	T 373H	T 373
D-flip flops with reset and 3-state output	—	T 374H	T 374
1-bit RAM	RM 1	—	—

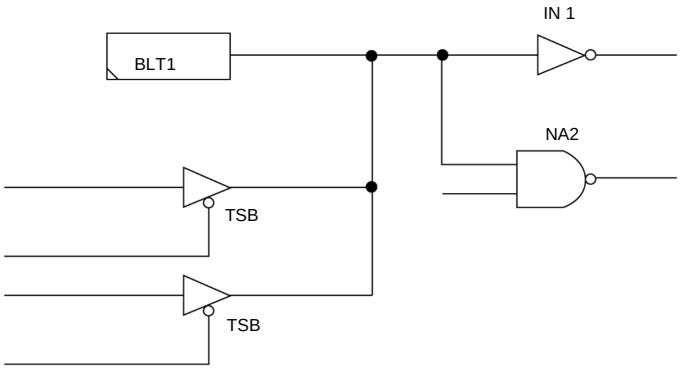


Figure 9-7 Typical Configuration of a Bus Cell Circuit

9.7 Preventing Contention with External Buses

In a system built using gate arrays and other LSIs, if they are connected in a bus configuration, take appropriate measures, in addition to the precautions described in Section 9.6, “Configuration of the Internal Bus,” by inserting pull-up/pull-down resistors, for example. To prevent external buses from floating, input/output cells with pull-up/pull-down resistors or input/output cells with a bus hold function (*) may be used.

Note that if appropriate measures are not taken prior to use, due to the indeterminate input level, functional failure or increased input leakage current may be encountered.

*: Bus hold circuit

Input/output buffers with a bus hold function are available in the S1X60000 series. To prevent the output pins or bi-directional pins from entering a high impedance state, these buffers hold the data at the output pins intact.

However, because the bus hold circuit’s holding capability is restrained so as not to adversely affect normal operation, do not use the retained output data as valid data. In the event any data is supplied from the outside, the retained data may change state easily.

For details on the bus hold circuit’s output retention current, refer to the electrical characteristics specified in this manual.

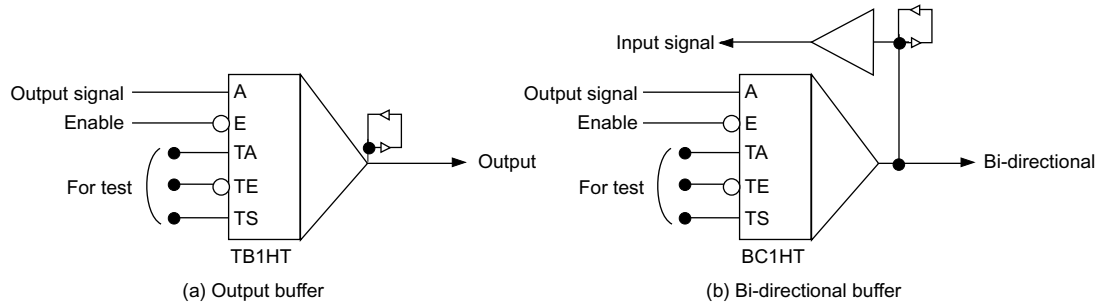


Figure 9-8 Example of a Bus Hold Circuit Symbol

9.8 Hazard Protection

Circuits or decoder cells comprised of a combination of NAND and NOR gates tend to generate very short pulses, depending on the difference in propagation delays between those gates. These short pulses are known as a “hazard.” If such a hazard enters the clock or reset pins of an FF (flip-flop), it causes the FF to operate erratically.

For circuits in which such a hazard is likely to occur, therefore, protective measures must be taken by, for example, devising a circuit configuration that prevents the hazard from propagating or using a decoder circuit provided with an “Enable” pin.

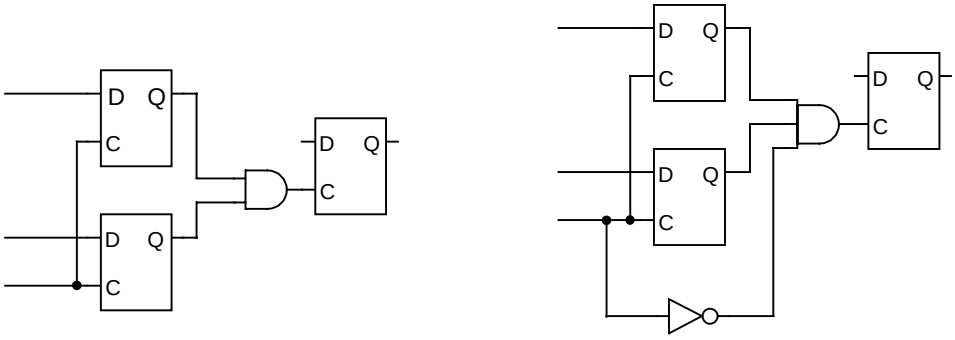


Figure 9-9 Example of Hazard Protection

9.9 Oscillation Circuits

9.9.1 Configuration of Oscillation Circuits

Two types of dedicated oscillation cells are used to configure an oscillation circuit: one for a crystal oscillation, and one for an CR oscillation. Furthermore, there are two types of cells for crystal oscillation use, a steadily oscillating type and an intermittently oscillating type, and either type can be placed in an internal cell area or an I/O cell area. The oscillation circuit may be configured in various ways, depending on which type of oscillation cell is used, as shown below.

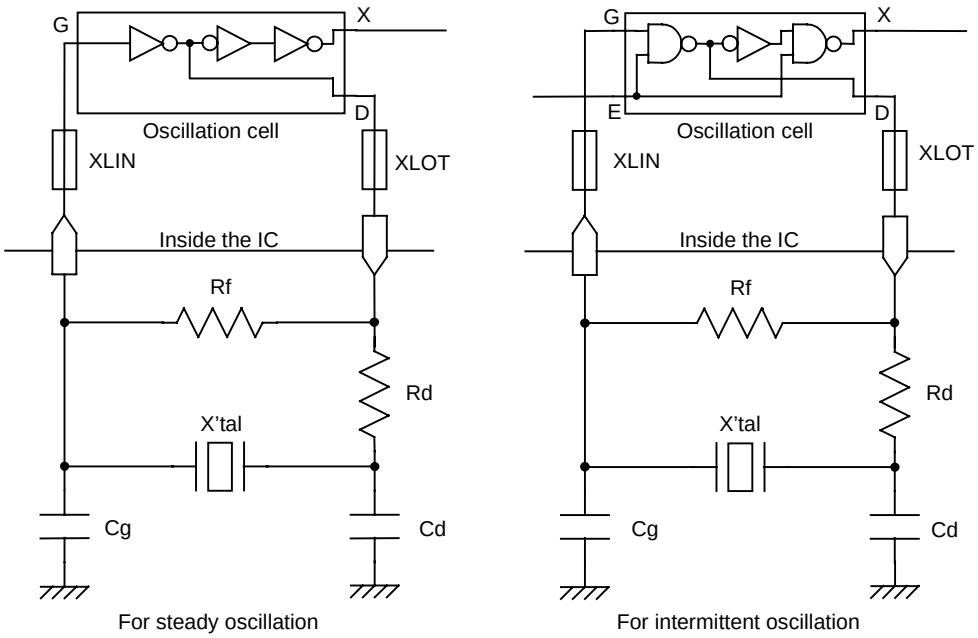


Figure 9-10 Crystal Oscillation Circuit (Internal Cell Type)

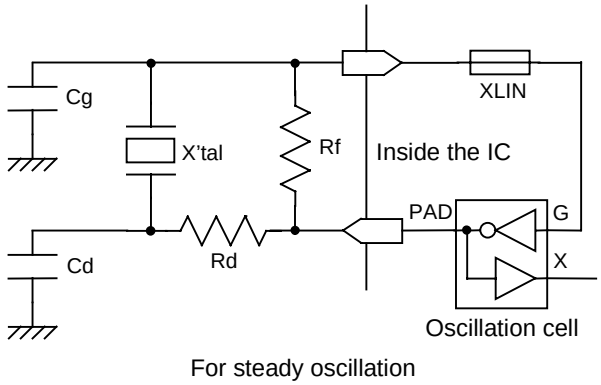


Figure 9-11 Crystal Oscillation Circuit (I/O Cell Type)

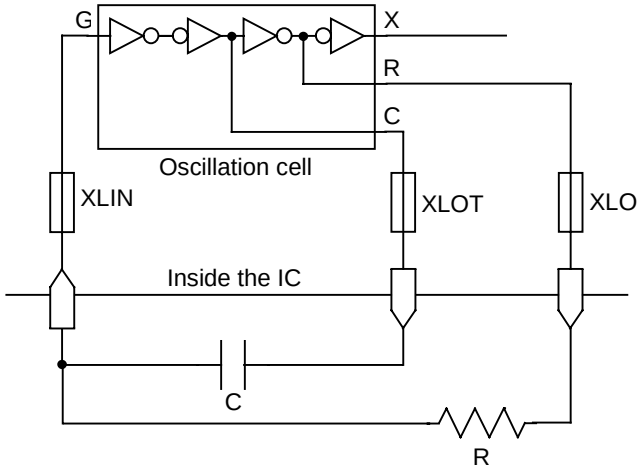


Figure 9-12 CR Oscillation Circuit

9.9.2 Notes Regarding the Use of Oscillation Circuits

(1) Pin layout

- The input/output pins of the oscillation circuit must be placed close to each other, and must be enclosed with the power supply pins (V_{DD}, V_{SS}) at both ends.
- The input/output pins of the oscillation circuit must be placed away from other output pins. In particular, they must be separated from outputs that are in phase or are 180 degrees out of phase with the oscillation waveform. Make sure these outputs are placed on the other side of the package, opposite the oscillation circuit.
- The input/output pins of the oscillation circuit must be placed away from other input pins such as a clock input, which operate at high speed.
- The input/output pins of the oscillation circuit must be placed as close to the center of one edge of the package as possible.
- When incorporating two or more oscillation circuits in the design, make sure those oscillation circuits are placed apart from each other in order to prevent interference.
- When using area array packages such as BGA, consult the sales division of Epson for the pin layout of the package.

(2) Test pattern generation

For details on how to create test patterns for designs using an oscillation circuit, refer to Section 11.5, "Notes Regarding the Use of Oscillation Circuits," in Chapter 11, "Test Pattern Generation."

(3) Selecting oscillation cells

The oscillation frequencies available with the oscillation cells are in the range of several tens of kHz to tens of MHz. For more information, contact the sales division of Epson.

(4) Setting external resistor and capacitor values

The oscillation characteristics of an oscillation circuit depend on its constituent elements (IC, X'tal, Rf, Rd, Cg, Cd, and board). Therefore, before determining the values of external Rf, Rd, Cg, or Cd, sufficiently evaluate those components while they are mounted on the actual board. In this way, attempt to select the most appropriate values for those components.

(5) Guaranteed level

The oscillation characteristics of an oscillation circuit depend on its constituent elements (IC, X'tal, Rf, Rd, Cg, Cd, and board). Therefore, Epson cannot guarantee the oscillation performance and characteristics of oscillation circuits designed by customers. The oscillation characteristics of those oscillation circuits must be verified by customers themselves through sufficient evaluation using ES samples.

(6) Oscillation circuit configuration in a dual power supply system

The oscillation circuit in a dual power supply system can basically be configured in the same way as a single power supply system. In this configuration, the oscillation cells are connected to the LV_{DD} power supply. For the input/output cells XLIN and XLOT used in this configuration, therefore, select those labeled "XLLIN" and "XLLOT". Moreover, when using 5 V Tolerant I/O cells, please be sure to use XFLLIN and XFLLOT, respectively.

9.10 Restrictions and Constraints on VHDL/Verilog-HDL Netlist

The VHDL/Verilog-HDL netlist to be interfaced to Epson shall be a pure gate level netlist (not containing function and description of operation). The restrictions and constraints in developing Epson ASIC using VHDL/Verilog-XL are as follows.

9.10.1 Common Restrictions and Constraints

(1) Names of external pin (I/O pin)

- Use only upper case letters.
- Number of characters: 2 to 32
- Bus description is prohibited.
- Usable characters: Alphanumeric characters and "_." Use an alphabetical letter at the head.
- Examples of prohibited character strings:

  2 INPUT: A digit is at the head.

  \2INPUT: "\" is at the head.

  InputA: Lower case letters are included.

  INPUTA: "" is at the head.

  INA[3:0]: A bus is used for the name of the external pin.

  INA[3]: A bus is used for the name of the external pin.

(2) Names of internal pin (including bus net names)

Upper and lower case letters can be used in combination, except the following.

Combinations of the same words expressed in upper and lower case letters, such as "_RESET_" and "_Reset_."

- Number of characters: 2 to 32
- Usable characters: Alphanumeric characters, "_", "_[]_" (Verilog bus blanket), and "_()_" (VHDL bus blanket) with an alphabetical letter at the head.

(3) Module names

In systems, module names are discriminated between the uppercase and lowercase. In design rules, however, mixed use of uppercase and lowercase module names is prohibited.

Example: Mixed use of "AND" and "And"

Because cells are case-sensitive, be careful about upper and lower case when you enter module names.

(4) Bus description is prohibited at the most significant place of the module.

Examples:

DATA [0:3], DATA [3], and DATA [2] are prohibited.
DATA0, DATA1, and DATA2 are all allowed.

(5) You can use I/O cells of the same library series, but cannot combine those of different series.

(6) It is not possible to describe operations in behaviors, in RTL, or in the C language. Such descriptions existing in the netlist are invalid.

(7) Precision of the time scale of the library of each series is 1ps.

9.10.2 Restrictions and Constraints for Verilog Netlist

(1) Descriptions using the functions “assign” and “tran” are prohibited in the gate level Verilog netlist.

(2) Descriptions of connection with cell pin names are recommended in the Verilog netlist.

Examples:

Possible: IN2 inst_1 (.A(inst_2),.X(inst_3))
Not Possible: IN2 inst_1(net1, net2)

(3) You cannot use the Verilog command “force” as a description of flip-flop operation.

Example: force logic .singal = 0

(4) The time scale description is added at the head of the gate-level netlist generated by the Synopsys design compiler. Set it at the value described in the Epson Verilog library. Time scale of each series is 1ps.

Example: `timescale 1ps/1ps

(5) Epson prohibits combination of a bus single port name and a name that includes “__”, such as the following, in the same module.

input A [0]
wire \A [0]

(6) The following letter strings are reserved for Verilog, which cannot be used as a user-defined name.

always	and	assign	begin	buf	bufif0
bufif1	case	design	default	defparam	disable
else	end	endcase	endfunction	endmodule	endtask
event	for	force	forever	fork	function
highz0	highz1	if	initial	inout	input
integer	join	large	medium	module	nand
negedge	nor	not	notif0	notif1	or
output	parameter	posedge	pull0	pull1	reg
release	repeat	scalared	small	specify	strong0
strong1	supply0	supply1	task	time	tri
tri0	tri1	trinand	trior	trireg	vectored
wait	wand	weak0	weak1	while	wire
wor	xor	xnor			

9.10.3 Restrictions and Constraints on VHDL Netlist

(1) In addition to the constraints in 9.10.1 (1), the following letter strings are also prohibited. Because the simulation is performed using TEXTIO package, the name of functions used in TEXTIO package cannot be defined for users.

INPUTA_: "_" is used at the end.

INPUT_ _A: "_" is used twice or more in succession.

read: Used in the system.

write: Used in the system.

(2) The following letter strings are reserved for VHDL, which cannot be used as a user-defined name.

abs	access	after	alias	all
and	architecture	array	assert	attribute
begin	block	body	buffer	bus
case	component	configuration	constant	disconnect
downto	else	elsif	end	entity
exit	file	for	function	generate
generic	guarded	if	in	inout
is	label	library	linkage	loop
map	mod	nand	new	next
nor	not	null	of	on
open	or	others	out	package
port	procedure	process	range	record
register	rem	report	return	select
severity	signal	subtype	then	to
transport	type	units	until	use
variable	wait	when	while	with
xor				

(3) To use Epson utilities and tools, it is necessary to change the VHDL format into the Verilog format. Therefore, the letter strings reserved for Verilog in 9.10.2 (6) are also prohibited.

9.10.4 Description of Oscillation Cell and AC/DC Test Circuit Cell L1TCIR2

It is recommended that oscillation cells be described after being turned into instances, and that the dont_touch attribute be attached to the input and output nets by using the set_dont_touch command, in order to ensure that no buffers are inserted into the oscillation cells' external-pin connecting nets when synthesized.

As AC/DC test circuit cell L1TCIR2 are available as hard macros, it is recommended that they be entered in the form of gate descriptions, as shown in the examples below.

– Example of Verilog-HDL description –

```
L1OSC1 inst1 (.G(gate_in), .D(drain_out), .X(clk_out) );
L1TCIR2 inst2 (.TM0(i_net0), .TM1(i_net1), .TM2(i_net2), .TM3(i_net3),
               .TST(i_net4), .MS(MS), .TD(TD), .TE(TE), .TS(TS), .TAC(TAC) );
```

– Example of VHDL description –

```
inst1 : L1OSC1 port map (G ⇒ gate_in, D ⇒ drain_out, X ⇒ clk_out);
inst2 : L1TCIR2 port map (TM0 ⇒ i_net0, TM1 ⇒ i_net1, TM2 ⇒ i_net2,
                          TM3 ⇒ i_net3, TST ⇒ i_net4,
                          MS ⇒ MS, TD ⇒ TD, TE ⇒ TE, TS ⇒ TS, TAC ⇒ TAC );
```

9.10.5 Clock Buffer Description

When performing hierarchical design, please make sure that the clock root buffers are inserted in the upper layers (to the extent possible), so that gated cells will not have multiple linked stages.

For clock root buffers and gated cells, it is recommended that gated cells be written directly in RTL description.

When using Epson gate libraries in RTL simulation, please make sure a sufficient input delay is allowed in the test patterns you create, as there will be some delay in the clock root buffers.

– Verilog description –

```
module TOP (CLK, RESET, ....., );
  input CLK, RESET, ... ;
  output OUT1, OUT2, ... ;


LIBCY pad1 (.PAD(CLK), .X(iCLK) );
L1CRBF2 U0_L1CRBF2 (.A(iCLK), .X(wCLK) );
   .
   .

CLKGEN U_CLKGEN (.CLK(wCLK), .ACLK(ACLK), .BCLK(BCLK) ...);
AIF U_AIF (.ACLK(ACLK), .....);
BIF U_BIF (.BCLK(BCLK), .....);

endmodule


module CLKGEN (CLK, ACLK, BCLK);
input CLK;
output ACLK, BCLK ;

LICAD2X4 GATEDCLKAND0 (.A1(CLK), .A2(A_gate),.X(ACLK) );
LICAD2X4 GATEDCLKAND1 (.A1(CLK), .A2(B_gate),.X(BCLK) );

  ...

endmodule
```

```
– VHDL description –
library IEEE;
library s1x60000_typ;

use IEEE.std_logic_1164.all
use s1x60000_typ.primitives_tables.all;
use s1x60000_typ.mos_switches.all;

entity TOP is
 port ( CLK   ; in std_logic ;
       RESET ; in std_logic ;
       ...
      );
end TOP;
architecture RTL of TOP is

  component LIBCY
    port (PAD : in std_logic; X: out std_logic);
  end component;
  component LICRBF2
    port (A : in std_logic; X: out std_logic);
  component CLKGEN
    port ( CLK, ACLK, BCLK : in std_logic; ... );
  end component;
  component AIF
    port (....  );
  end component;
  signal
    wCLK, .....;

  begin

  PAD1 : LIBCY port map ( PAD⇒ CLK, X⇒ iCLK );
  PAD2 :
  U_CLKGEN : CLKGEN port map ( CLK⇒ wCLK, ACLK⇒ ACLK, ... );
  U_AIF :  AIF port map (ACLK⇒ ACLK, ... );

end RTL;
```

9.11 Pin Layout and Simultaneous Operation

This section describes the points to be noted in the layout of pins and the procedure for adding power supplies for simultaneous output-buffer operation.

9.11.1 Estimating the Number of Power Supply Pins

The necessary number of power supply pins must be estimated according to the LSI's power consumption and the number of output buffers. In particular, a rather large transient current flows through the output buffers when they switch on or off. The amount of this transient current is greater for output buffers with greater drive capability.

The number of power supply pins required for an LSI may be estimated with respect to its current consumption, as described below.

(1) For single power supply systems

Letting the current consumption be I_{DD} [mA], the number of power supply pins may be estimated with respect to this current consumption as follows:

$N_{IDD} \geq I_{DD} / 50$ (pairs): With the V_{DD} and V_{SS} pins counted as one pair, 50 mA per pair can be supplied.

Notes 1: There must be at least four pairs of power supply pins, that is, one pair on each side of the LSI.
I_{DD} represents a value equal to the power consumption obtained in Chapter 8, Section 8.1, "Calculation of Power Consumption," divided by the operating voltage.

2: If output buffers have DC loads connected to them with current steadily flowing, power supply pins must be added. For more information, contact the sales division of Epson.

(2) For dual power supply systems

Even for dual power supply systems, the allowable amount of current that can be flowed per pair of power supply pins (both HV_{DD} and LV_{DD} power supplies) is the same as that for single power supply systems. Calculate the necessary number of power supply pin pairs separately for the HV_{DD} and LV_{DD} power supplies.

(1) Number of HV_{DD} power supply pins

Letting the current consumption in the HV_{DD} power supply system be I_{DD} (HV_{DD}) [mA], the number of power supply pins, N_{IDD} (HV_{DD}), may be calculated with respect to this current consumption as follows:

N_{IDD} (HV_{DD}) $\geq I_{DD}$ (HV_{DD}) / 50: 50 mA per pin can be supplied

(2) Number of LV_{DD} power supply pins

Letting the current consumption in the LV_{DD} power supply system be I_{DD} (LV_{DD}) [mA], the number of power supply pins, N_{IDD} (LV_{DD}), may be calculated with respect to this current consumption as follows:

N_{IDD} (LV_{DD}) $\geq I_{DD}$ (LV_{DD}) / 50: 50 mA per pin can be supplied

(3) Number of V_{SS} power supply pins

N_{IDD} (V_{SS}) $\geq \{I_{DD}$ (HV_{DD}) + I_{DD} (LV_{DD})$\}$ / 50: 50 mA per pin can be supplied

Notes 1: For the power supply pins HV_{DD}, LV_{DD}, and V_{SS}, there must be at least four pairs of power supply pins, that is, one pair on each side of the LSI. I_{DD} represents a value equal to the power consumption obtained in Chapter 8, Section 8.1, "Calculation of Power Consumption," divided by the operating voltage.

2: If output buffers have DC loads connected to them with current steadily flowing, power supply pins must be added. For more information, contact the sales division of Epson.

3: If it is necessary to add a power supply due to simultaneous changes in output, add the HV_{DD}, LV_{DD}, and V_{SS} pins for each power supply system, separately for the HV_{DD} output buffers and the LV_{DD} output buffers.

Calculation example: The following shows an example of the procedure for estimating the number of power supply pins.

Here, the number of power supply pins is estimated using the power consumption obtained in Chapter 8 for an IC, which has the following power supply characteristics.

- Power-supply voltage: HV_{DD}/LV_{DD} = 3.3 V/2.5 V
- Power consumption: $P(HV_{DD})$ = 224 [mW]
  $P(LV_{DD})$ = 684 [mW]

(1) Estimating the number of HV_{DD} power supply pins

Letting the number of HV_{DD} power supply pins be $N_{IDD}(HV_{DD})$, then

$N_{IDD}(HV_{DD})$ = 224 [mW] / 3.3 [V] / 50 [mA]
= 1.36 [pins]

Because there must be at least one power supply pin on each side of the IC, the number of HV_{DD} power supply pins to be inserted is 4.

(2) Estimating the number of LV_{DD} power supply pins

Letting the number of LV_{DD} power supply pins be $N_{IDD}(LV_{DD})$, then

$N_{IDD}(LV_{DD})$ = 684 [mW] / 2.5 [V] / 50 [mA]
= 5.47 [pins]

Therefore, the number of LV_{DD} power supply pins to be inserted is 6.

(3) Estimating the number of V_{SS} power supply pins

Letting the number of V_{SS} power supply pins be $N_{IDD}(V_{SS})$, then

$N_{IDD}(V_{SS})$ = {224 [mW] / 3.3 [V] + 684 [mW] / 2.5 [V] } / 50 [mA]
= 6.83 [pins]

Therefore, the number of V_{SS} power supply pins to be inserted is 7 (however, we recommend that V_{SS} pins be placed in pairs with the HV_{DD} and LV_{DD} power supply pins).

Thus, the respective numbers of power supply pins are as follows.

HV_{DD} power supply pins: 4
LV_{DD} power supply pins : 6
V_{SS} power supply pins : 7

9.11.2 Simultaneous Operation and Adding Power Supplies

The noise generated by output buffers when they switch on or off simultaneously may cause the LSI to operate erratically. This section describes the simultaneous operation of output buffers and the points to be noted when placing pins in order to suppress the noise induced by simultaneous output operation.

9.11.2.1 Malfunction due to Simultaneous Operation

When a number of output buffers change state simultaneously, a transient charging and discharging of current occurs due to load capacitance. The charging and discharging acts upon the inductance of the lead frame or bonding wire on the system's substrate or package, resulting in the generation of noise.

The noise thus generated is expressed by the equation below.

$$Vn = L \times \frac{di}{dt} \quad \text{... Equation (1)}$$

where, Vn: noise power supply
L: power supply inductance component
$\frac{di}{dt}$: transient current

Here, because the transient current tends to increase in proportion to the number of simultaneously operating pins and their current drive capability and load capacitance, the voltage generated by the noise power supply varies depending on the following factors:

(1) Number of power supplies
(2) Number of simultaneously operating output buffers
(3) Drive capability of simultaneously operating output buffers
(4) Load capacitance of simultaneously operating output buffers

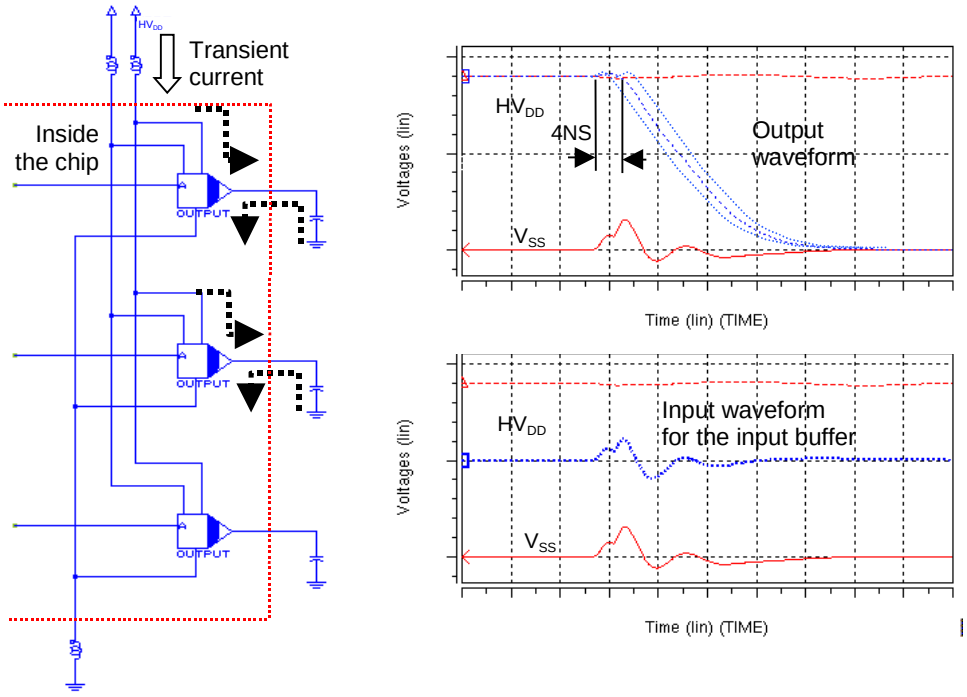


Figure 9-13 Noise due to Simultaneous Operation of Outputs

9.11.2.2 Definition of Simultaneous Operation of Outputs

The simultaneous operation of outputs refers to a phenomenon in which multiple output buffers change state in the same direction within a certain time (i.e., within 4 ns). The simultaneous operation of outputs is defined independently for each closed loop of power supplies.

The simultaneous operation of outputs in the same direction refers to the following operations:

(1) H → L, HZ → L, X → L, or H → X output signal operation

(2) L → H, HZ → H, X → H, or L → H output signal operation

where, HZ: high impedance

X: indeterminate

For bi-directional pins, the changeover of their functionality from input to output must also be taken into consideration.

9.11.2.3 Restrictions on Simultaneously Operating Output Buffers

The magnitude of the inductance of a closed loop in which output buffer charging and discharging current flows determines the magnitude of the generated noise. The inductance of a closed loop varies with the LSI's pin layout and the board on which the LSI is mounted. To suppress the noise generated by the simultaneous operation of outputs, exercise caution in pin layout.

A closed loop here refers to a pin layout in which output buffer pins are enclosed with the power supply pins at both ends.

Determine whether there is simultaneous operation of outputs independently for each closed loop of power supplies.

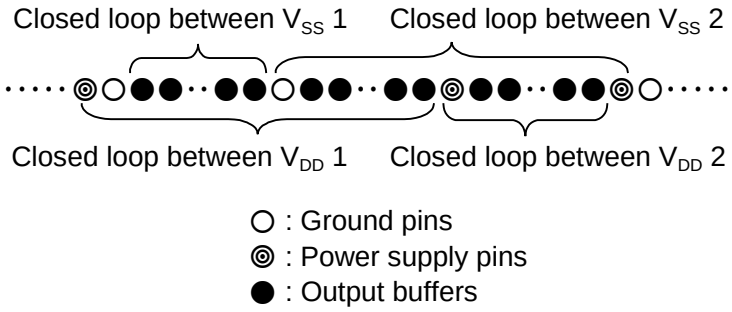


Figure 9-14 Closed Loops

Consider a case in which output buffers are placed in the manner shown above and change state simultaneously, resulting in the generation of noise. To prevent malfunction of the LSI due to noise in this case, determine whether the magnitude of noise is sufficiently large to cause malfunction from the number of output buffers and the load capacitance in each closed loop, using the coefficients in Tables 9-5 through 9-8 and the equation below.

$$\sum_{k} mk \leq 1 \quad \text{... Equation (2)}$$

where, mk: coefficient of each output buffer

For dual power supply systems, make this determination separately for the HV output cells in each closed loop between HV_{DD}'s, LV output cells in each closed loop between LV_{DD}'s, and for all output cells in each closed loop between V_{SS}'s.

Table 9-5 HV Output Cells, HV_{DD} = 3.3 V ± 0.3 V

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
Type S Type M Type 1	0.077	0.083	0.091	0.100	0.100
Type 2	0.100	0.111	0.125	0.143	0.143
Type 3	0.200	0.250	0.250	0.333	0.333

Table 9-6 HV Output Cells, HV_{DD} = 3.3 V ± 0.3 V (When Using PCI)

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
Type S Type M Type 1	0.125	0.143	0.167	0.167	0.167
Type 2	0.167	0.200	0.200	0.250	0.250
Type 3	0.250	0.333	0.333	0.333	0.333
PCI	0.167	0.200	0.200	0.250	0.250

Note: This applies when a PCI3V cell exists in the closed loop.

Table 9-7 LV Output Cells, V_{DD} or LV_{DD} = 2.5 V ± 0.2 V

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
Type S Type M Type 1	0.077	0.083	0.091	0.100	0.100
Type2	0.167	0.200	0.200	0.250	0.250
Type3	0.250	0.333	0.333	0.333	0.333

Table 9-8 LV Output Cells, V_{DD} or LV_{DD} = 2.0 V ± 0.2 V

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
Type S Type M Type 1	0.050	0.054	0.059	0.065	0.065
Type 2	0.084	0.100	0.100	0.125	0.125
Type 3	0.162	0.216	0.216	0.216	0.216

Calculation example: Determine whether the magnitude of noise is sufficiently large to cause malfunction due to the simultaneous operation of outputs under the following voltage and pin-layout conditions.

- Power supply voltage: 3.3 V/2.5 V
- Input interface : LVTTL for HV cells
  CMOS for LV cells

Pin No.	Cells Used	Output Load Capacitance (pF)
(1)	V_{SS}	
(2)	HV_{DD}	
(3)	LV_{DD}	
(4)	HV cells, Type 2	125
(5)	HV cells, Type 3	100
(6)	HV cells, Type 3	175
(7)	HV_{DD}	
(8)	LV cells, Type 1	75
(9)	LV cells, Type 3	150
(10)	LV_{DD}	
(11)	V_{SS}	

First, because Tables 9-5 and 9-7 are used, round the output load capacitances up to the nearest whole value.

(4) 125 pF → 150 pF

(5) 100pF → 100 pF

(6) 175 pF → 200 pF

(8) 75 pF → 100 pF

(9) 150 pF → 150 pF

- Make determination for the closed loop between HV_{DD}'s ((2) to (7))

  The HV output cells used in the closed loop between HV_{DD}'s are (4), (5), and (6).

  From the input interface and the power supply voltage, make determination using the coefficients given in Table 9-5.

  $\sum_{k} mk = 0.143 + 0.250 + 0.333 = 0.726$

  Thus, the result shows that the closed loop between HV_{DD}'s satisfies the determination criteria.

- Make determination for the closed loop between LV_{DD}'s ((3) to (10))

  The LV output cells used in the closed loop between LV_{DD}'s are (8) and (9).

  From the input interface and the power supply voltage, make determination using the coefficients given in Table 9-7.

  $\sum_{k} mk = 0.091 + 0.333 = 0.424$

  Thus, the result shows that the closed loop between LV_{DD}'s satisfies the determination criteria.

- Make determination for the closed loop between V_{SS}'s ((1) to (11))

  The output cells used in the closed loop between V_{SS}'s are (4), (5), (6), (8), and (9).

  From the input interface and the power supply voltage, make determination using the coefficients given in Table 9-5 for the HV output cells, and Table 9-7 for the LV output cells.

  $\sum_{k} mk = 0.143 + 0.250 + 0.333 + 0.091 + 0.333 = 1.150$

  Thus, the result shows that the noise restraints for malfunction due to the simultaneous operation of outputs are not met.

  Therefore, change the pin layout by moving V_{SS} at (11) to a position between (8) and (9) so that the cells in the closed loop between V_{SS}'s are (4), (5), (6), and (8).

Pin No.	Cells Used	Output Load Capacitance (pF)
(1)	V_{SS}	
(2)	HV_{DD}	
(3)	LV_{DD}	
(4)	HV cells, Type 2	125
(5)	HV cells, Type 3	100
(6)	HV cells, Type 3	175
(7)	HV_{DD}	
(8)	LV cells, Type 1	75
(11)	V_{SS} ← VSS moved to this point	
(9)	LV cells, Type 3	150
(10)	LV_{DD}	

  Make determination for the closed loop between V_{SS}'s in this pin layout.

  $\sum_{k} mk = 0.143 + 0.250 + 0.333 + 0.091 = 0.817$

  Thus, the result shows that the closed loop between V_{SS}'s satisfies the determination criteria.

  However, because V_{SS} has been moved, the closed loop between V_{SS}'s comprised of cells (9) and below the cells (9) requires caution.

9.11.3 Cautions and Notes Regarding the Pin Layout

When the package to be used has been decided, the pin layout on it must also be decided. For details on the power supply pins and the number of usable input/output pins on each package in the S1X60000 series, refer to the designated "pin layout table" fill-out sheet.

When the pin layout has been decided, please provide Epson with a "pin layout table" after entering your pin layout on the designated sheet. Because placement and routing work at Epson is performed in accordance with the "pin layout tables" received from customers, carefully inspect your pin layout table before presenting it to Epson.

When the designated "pin layout table" fill-out sheet is required, please contact Epson.

The pin layout table is one of the important specifications determining the quality of the LSI. It is particularly important to prevent noise induced malfunction of the LSI. Noise is a phenomenon that cannot easily be verified through simulation or the like.

To prevent your LSI from operating erratically for unknown reasons, we recommend that the contents below be thoroughly examined prior to the creation of your pin layout.

9.11.3.1 Fixed Power Supply Pins

Depending on package combinations, there are several pins that can only be used for power supplies. Furthermore, some of those pins are fixed for V_{DD} use, while others are fixed for V_{SS} use. Therefore, check the "pin layout table" fill-out sheet when selecting the package to use.

9.11.3.2 Cautions and Notes Regarding the Pin Layout

The pin layout may affect the logical functions or electrical characteristics of the LSI. Furthermore, pin layout is subject to restrictions for reasons related to the LSI assembly or cell or bulk configurations. Therefore, there are several parameters that require caution in the determination of pin layout. These parameters include power supply currents, the separation of input and output pins, critical signals, pull-up/pull-down resistance inputs, the simultaneous operation of outputs, and large-current drivers. The following describes these parameters.

(1) Power-supply currents (I_{DD}, I_{SS})

The power supply currents (I_{DD}, I_{SS}) specify the allowable value of the power supply current flowing in the power supply pins under operating conditions. If a current exceeding this allowable value flows in the power supply pins, the current density of the LSI's internal power supply wiring increases, causing the reliability of the LSI to degrade or the LSI to break down. Furthermore, the LSI's internal voltage increases or decreases by an amount equal to the magnitude of voltage that develops due to the current and wiring resistance. It causes the functional blocks of the LSI to operate erratically or adversely affects the DC and AC characteristics of the LSI.

To avoid these problems, the current density and the impedance of power supply wiring must be reduced. To this end, in the design of a circuit, estimate its power consumption and insert as many power supply pins as necessary to ensure that the current flowing in each power supply pin will not exceed the allowable value. For details on the power supply pins, refer to Section 9.11.1, "Estimating the Number of Power Supply Pins." In addition, make sure these power supply pins are well distributed, rather than being concentrated in one location.

It should be noted that the number of power supply pins ultimately required for the LSI is not simply the number of power supply pins determined above, but must also include the power supply pins that are added for noise protection purposes or the like. For details on the added power supply pins, refer to Section 9.11.2, "Simultaneous Operation and Adding Power Supplies."

(2) Noise generated by the operation of output cells

The noise generated by the operation of output cells is broadly classified into the two types specified below. To reduce these types of noise, it is helpful to install as many power supply pins as possible.

a) Noise generated in the power supply lines

The noise generated in the power supply lines presents a problem when there are multiple operating outputs. It causes the LSI's input threshold level to change, which in turn causes the LSI to operate erratically. This type of noise is generated by a large current flowing into the power supply lines due to the simultaneous operation of output cells.

Power supply noise in particular is affected by the inductance component of the circuit. Therefore, the LSI's equivalent circuit can be expressed as shown in Figure 9-15. When the output in this circuit diagram changes state from High to Low, a current flows from the output pin into the LSI, with the current flowing through the equivalent inductance L2 (due to the LSI package or the like) to the ground. At this time, the equivalent inductance L2 causes the voltage of the LSI's internal V_{SS} power supply line to change. A voltage fluctuation occurring in this V_{SS} power supply line is referred to here as the noise generated in the power supply line. Because this type of noise is caused mainly by the equivalent inductance L2, there is a tendency that the greater the surge of the power supply current, the greater the magnitude of the noise generated.

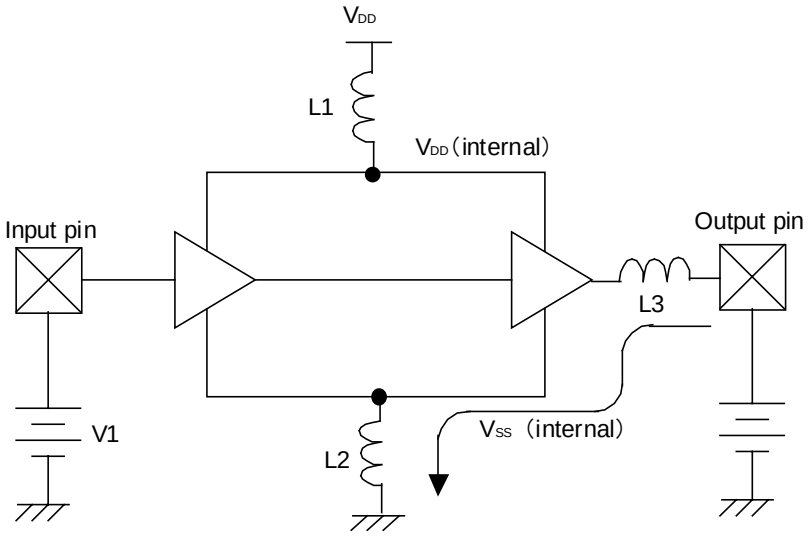


Figure 9-15 LSI Equivalent Circuit

b) Overshoot, undershoot, and ringing

Noises known as overshoot, undershoot, or ringing are generated by the equivalent inductance at the output pins. L3 in Figure 9-15 is an example of this equivalent inductance. Because inductance has the property of storing energy, even when the output goes Low or High, overshoots and undershoots are proportional to the magnitude of the current flowing in the output and the change in rate of the current due to the stored energy.

The most efficient means of reducing overshoots and undershoots is the use of output cells with a small drive capability. Overshoots and undershoots tend to decrease as the load capacitance increases. Therefore, be particularly careful when using cells with a large drive capability.

(3) Isolating input and output pins

Separating the group of input pins from the group of output pins in design of the pin layout is an important technique for reducing the effect of noise.

Because the input pins and the bi-directional pins set for input are susceptible to noise, make sure they do not coexist with output pins in design of the pin layout. To this end, separate the group of input pins, the group of output pins, and the group of bi-directional pins according to the power supply pins (V_{DD}, V_{SS}) when placing each group of pins.

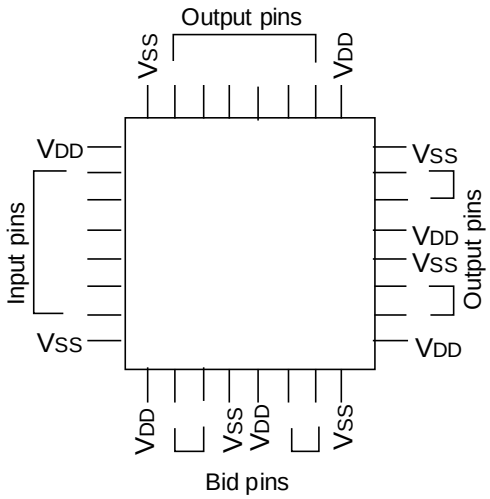


Figure 9-16 Example of Separating Input and Output Pins

(4) Critical signals

For critical signals such as input pins for clock and output pins operating at high speed, observe the precautions described below when placing pins.

a) The clock and reset pins that are required to reduce the effects of noise must be placed away from the output pins at positions near the power supply pins. (Figure 9-17)

b) The input/output pins of the oscillation circuit (OSCIN, OSCOUT) must be placed close to each other, enclosed with the power supply pins (V_{DD}, V_{SS}). In addition, make sure that no output pins synchronous with the oscillation circuit are placed near these pins. (Figure 9-18)

c) Input and output pins operating at high speed must be placed near the center of one edge of the chip (package). (Figure 9-17)

d) If the delay from specific input pins to specific output pins has only a minimal margin with respect to the customer specification, these input and output pins must be placed close to each other. (Figure 9-17)

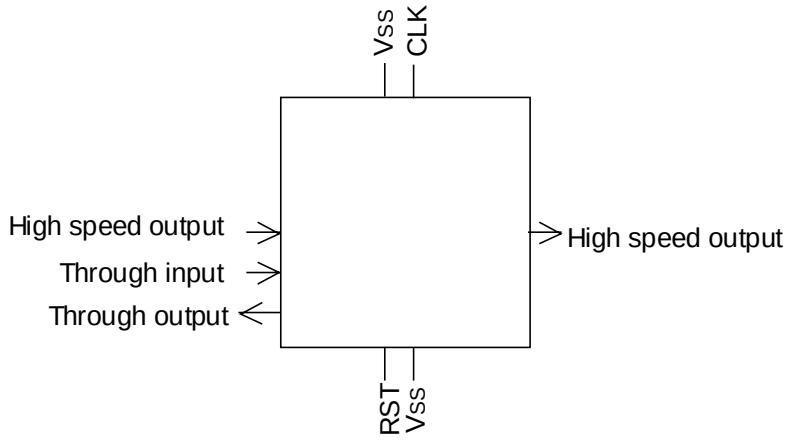


Figure 9-17 Example 1 of a Layout for Critical Signals

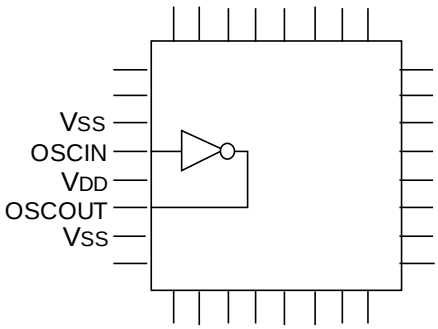


Figure 9-18 Example 2 of a Layout for Critical Signals

(5) Pull-up/pull-down resistor inputs

The pull-up/pull-down resistance values are rather large, ranging from several 10 k to several 100 kΩ, and have dependency on the power supply voltage for reasons related to their structure.

Therefore, when using these inputs as test pins or for other purposes while they are left open, note the precautions described below, as these pins become susceptible to power supply noise and could cause the LSI to operate erratically.

a) The pull-up/pull-down resistor inputs must be placed as far as possible from the high speed input signal pins (e.g., clock input pins). (Figure 9-19)

b) The pull-up/pull-down resistor inputs must be placed away from the output signal pins (particularly large-current output pins). (Figure 9-20)

In addition to the precautions on pin layout, take the following points into consideration as well.

- Pull-up/pull-down resistor inputs must be processed on the circuit board (PCB) as much as possible.
- Pull-up/pull-down resistors with small resistance values are preferable.

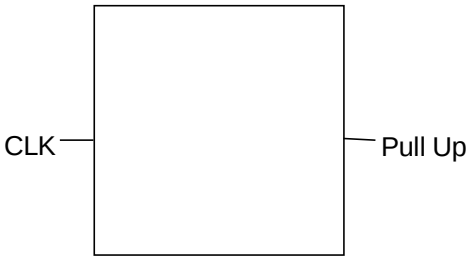


Figure 9-19 Example 1 of Placement of Pull-up/Pull-down Resistors

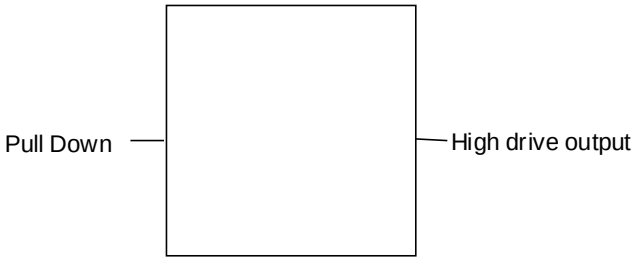


Figure 9-20 Example 2 of Placement of Pull-up/Pull-down Resistors

(6) Simultaneous operation of outputs

When multiple output pins operate simultaneously, they tend to generate noise, causing the LSI to operate erratically. When it is necessary to operate a number of output pins simultaneously, add power supply pins to the group of output pins that change state simultaneously, in order to prevent noise induced malfunction of the LSI. For details on the number of power supply pins to add and the procedure for placing the additional power supply pins, refer to Section 9.11.2, "Simultaneous Operation and Adding Power Supplies."

As a means of reducing said noise, cells for delay use may be added in a stage preceding one group of output pins. This helps to reduce the number of output cells that change state simultaneously, thereby reducing the amount of noise generated. (Figure 9-22)

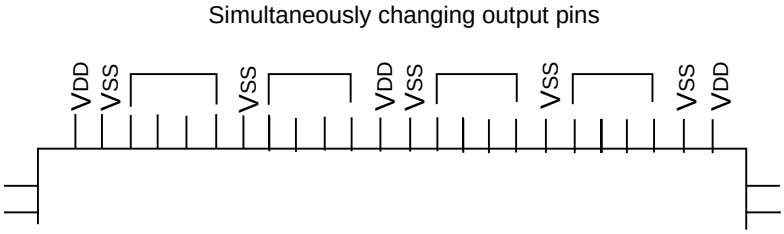


Figure 9-21 Example of Adding Power Supply Pins

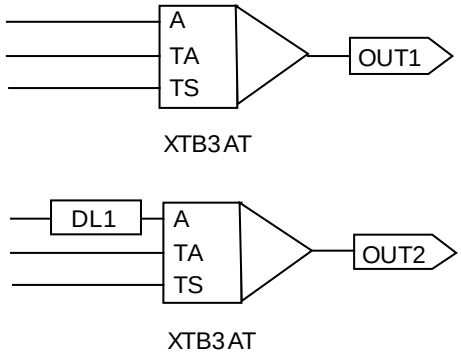


Figure 9-22 Example of Adding Delay Cells

(7) Large current drivers

When using the output of large current drivers (I_{OL} = 12 mA, PCI), observe the restrictions described below when placing pins.

a) Constraints on Strengthening the power supplies

Large current drivers have large drive capability; therefore, the amount of noise generated by their output buffers during operation is also large. This noise may cause the LSI to operate erratically.

When using large current drivers, add power supply pins near their pins in order to secure the power supply needed for the large current drivers. (Figure 9-23)

b) Low noise pre-drivers

To reduce the amount of noise generated by the output buffers of large current drivers during operation, low noise type output and bi-directional buffers available from Epson may be used. For details, refer to Chapter 4, "Types of Input/Output Buffers and Their Use (X Type)" and Chapter 5, "Types of Input/Output Buffers and Their Use (XF Type)."

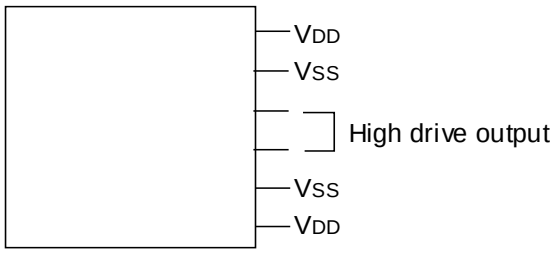


Figure 9-23 Example of Strengthening Power Supplies

(8) Other precautions

a) Non-connection (NC) pins

Normally, leave the NC pins open on the circuit board. When making connections to NC pins as when mounting devices on a printed circuit board, make sure the pins are connected to V_{SS} (GND).

Note that when NC pins are connected to signal wiring or V_{DD} (HV_{DD} or LV_{DD}), leakage current may occur inside the chip. (See Section 1.3.3, "Quiescent Currents of Input/Output Buffers (I_{QIO})," in Chapter 1.)

b) Tab hanger pins

Tab hanger pins are pins on the package that are connected directly to the LSI substrate. These pins are tied to the V_{SS} (GND) level without being furnished with external power supplies for the aforementioned reasons. Normally, leave these pins open on the board.

9.11.4 Example of the Recommended Pin Layout

Pin layout is an important factor in ensuring that the LSI operates normally. The following shows a pin layout diagram (Figure 9-24) based on the information given in this chapter. Refer to this example in determining the pin layout.

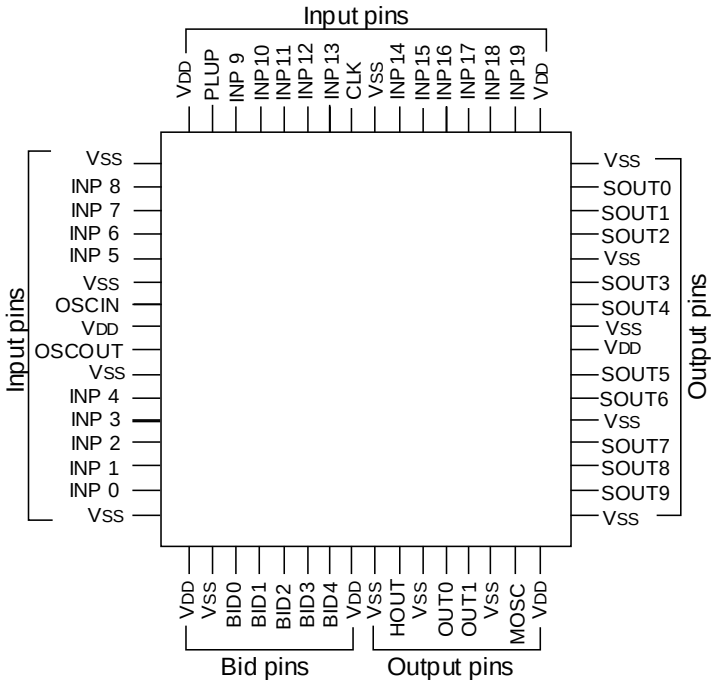


Figure 9-24 Example of the Recommended Pin Layout

Input pins are placed on the top and left sides of the package, with the output pins changing simultaneously on its right sides, and the bi-directional pins and other output pins changing simultaneously on its bottom side.

Table 9-9 Pin Layout Example

Placement	Pin Name	Explanation of Pin Name	Detailed Explanation of the Placement of Each Pin
Upper edge	PLUP	Input pins with pull-up	Placed at positions less affected by noise
	CLK	Input pins for the clock	Placed near the center of the edge of the package or near the power supply pins
Left edge	OSCIN	Oscillator pin	Placed near the center of the edge of the package or near the power supply pins
	OSCOUT	Oscillator pin	Placed near the center of the edge of the package or near the power supply pins
	INP0–19	Input pins	Placed apart from other pins, divided by power supply pins
Right edge	SOUT0–9	Simultaneously changing output pins	Placed apart from other pins, divided by power supply pins, with power supply pins added
Bottom edge	BID0–4	Bi-directional pins	Placed apart from other pins, divided by power supply pins
	MOSC	Oscillator monitor output pin	Placed near the power supply pins away from the oscillator pins
	HOUT	High-drive output pin	Power supply pins placed nearby
	OUT0-1	Output pins	Placed apart from other pins, divided by power supply pins
Overall edges	V_{DD}	V_{DD} power supply pins	
	V_{SS}	V_{SS} (GND) power supply pins	

9.12 About Power Supply Cutoff (X Type)

When S1X60000 series cells (X Type) are used to create a chip designed to power supply Cut-off specifications, note the following.

9.12.1 For Single Power Supply Systems

(1) In cases in which input signals from the outside also enter High-Z state when the power supply is cut

Basically, all types of input/output buffers can be used. Even in cases in which input/output buffers are separated by pairs of power supply pins and the power supply for part of the area is to be cut off, all types of input/output buffers can be used unless signals from the outside are applied.

(However, this is possible providing that the power supplies for all of the related circuits, including the internal cell area, are cut-off.)

(2) In cases in which input signals from the outside are applied when the power supply is cut off or pull-up resistors are incorporated external to the chip

If input signals from the outside are applied while the power supply is cut off, leakage current may occur, depending on the type of input/output buffer used.

Therefore, the following types of input/output buffers cannot be used in this design:

- Input buffers with pull-up resistors. However, this does not include Fail-Safe cells.
- Output buffers other than Fail-Safe buffers. However, the Open drain type can be used.
- Bi-directional buffers other than Fail-Safe buffers. However, the Open drain type can be used.

(Even in cases in which input/output buffers are separated by pairs of power supply pins and the power supply for part of the area is to be cut off, the input/output buffers listed above cannot be used in the relevant area.)

9.12.2 For Dual Power Supply Systems

(1) In cases in which LV_{DD} is cut off while HV_{DD} remains on

In this design, the output mode of the HV_{DD} output buffers or HV_{DD} bi-directional buffers may become uncontrollable. In the worst case scenario, current may even continue to flow into those buffers. Therefore, the power supply cannot be cut off in this design.

(2) In cases in which HV_{DD} is cut off while LV_{DD} remains on

a) If inputs from the outside also enter High-Z state when the HV_{DD} power supply is cut off

- LV_{DD} cells

  If the LV inputs also enter High-Z state, use cells that include pull-up/pull-down resistors.

  No specific restrictions apply if LV inputs do not enter High-Z state.

- HV_{DD} cells

  Be sure to use Gated cells. Current can be prevented from flowing at the initial input stage by setting control pin “C” high or low in the internal circuit.

b) If input signals from the outside are applied when the HV_{DD} power supply is cut off or pull-up resistors are incorporated external to the chip

- LV_{DD} cells

  When LV inputs enter the High-Z state, use cells that include pull-up/pull-down resistors.

  No specific restrictions apply if the LV inputs do not enter High-Z state.

- HV_{DD} cells

  For output buffers, use Open drain type cells.

  For input buffers, also be sure to use Gated cells. (Note that input buffers with pull-up/pull-down resistors cannot be used.) Current can be prevented from flowing at the initial input stage by setting control pin "C" high or low in the internal circuit. Bi-directional buffers cannot be used in this mode.

  For details on the Gated mentioned above, refer to Section 4.2.5, "Gated Cells." Even in cases in which input/output buffers are separated by pairs of power supply pin and the power supply for part of the area is to be cut-off, no input/output buffers other than those mentioned above can be used in the relevant area.

(3) In cases in which both HV_{DD} and LV_{DD} are cut-off

a) If inputs from the outside also enter High-Z state when the power supplies are cut-off

Basically, all types of input/output buffers can be used. Even in cases in which input/output buffers are separated by pairs of power supply pins and the power supplies for part of the area are to be cut off, all types of input/output buffers can be used unless signals from the outside are applied.

(However, this is possible provided that the power supplies for all of the related circuits, including the internal cell area, are cut off.)

b) If input signals from the outside are applied when the power supplies are cut-off or pull-up resistors are incorporated external to the chip

- LV_{DD} cells

  If input signals from the outside are applied while the power supplies are cut-off, leakage current may occur, depending on the type of input/output buffer used.

  Therefore, the following types of input/output buffers cannot be used in this design:
  - Input buffers with pull-up resistors. However, this does not include Fail-Safe cells.
  - Output buffers other than Fail-Safe buffers. However, the Open drain type can be used.
  - Bi-directional buffers other than Fail-Safe buffers. However, the Open drain type can be used.

- HV_{DD} cells

  As with LV_{DD} cells, leakage current may occur depending on the type of input/output buffer used. The following types of input/output buffers cannot be used in this design.
  - Input buffers with pull-up resistors
  - Output buffers other than Open drain buffers
  - Bi-directional buffers other than Open drain buffers

  (Even in cases in which input/output buffers are separated by pairs of power supply pins and the power supplies for part of the area are to be cut-off, the input/output buffers mentioned above cannot be used in the relevant area.)

9.13 About Power Supply Cutoff (XF Type)

When S1X60000 series cells (XF Type) are used to create a chip designed to power supply Cut-off specifications, note the following.

9.13.1 Cell Types Usable during Cut-off

(1) In cases in which LV_{DD} is cut-off while HV_{DD} remains on

In this design, the output mode of the HV_{DD} output buffers or HV_{DD} bi-directional buffers may become uncontrollable. In the worst case scenario, current may even continue to flow into those buffers. Therefore, the power supply cannot be cut off in this design.

(2) In cases in which HV_{DD} is cut off while LV_{DD} remains on

a) If inputs from the outside also enter High-Z state when the HV_{DD} power supply is cut-off

- LV_{DD} cells

  If the LV inputs also enter High-Z state, use cells that include pull-up/pull-down resistors.

  No specific restrictions apply if LV inputs do not enter High-Z state.

- HV_{DD} cells

  Be sure to use Gated cells. Current can be prevented from flowing at the initial input stage by setting control pin “C” high or low in the internal circuit.

- 5 V Tolerant Fail Safe cells

  All 5 V tolerant Fail Safe cells can be used. It is possible to shut off current flowing in the input circuit by setting control pin “C” low in the internal circuit. (In this case, a high-level signal is forwarded to output pin “X.”)

  Note that control pin “C” for 5 V tolerant Fail Safe cells must always be fixed high during normal operation.

b) If input signals from the outside are applied when the HV_{DD} power supply is cut-off or pull-up resistors are incorporated external to the chip

- LV_{DD} cells

  If the LV inputs also enter High-Z state, use cells that include pull-up/pull-down resistors.

  No specific restrictions apply if the LV inputs do not enter High-Z state.

- HV_{DD} cells

  (1) When handling HV_{DD} input signals, be sure to use Open drain type of cells for output buffers.

  Also be sure to use Gated cells for input buffers. Bi-directional buffers cannot be used in this mode.

  (2) When handling 5.0 V input signals or using external 5.0 V pull up resistors, no HV_{DD} cells can be used.

- 5 V Tolerant Fail Safe cells

  All 5 V tolerant Fail Safe cells can be used. It is possible to shut off current flowing in the input circuit by setting control pin "C" Low in the internal circuit. (In this case, a High level signal is forwarded to output pin "X.") HV_{DD} input signals and 5.0 V input signals are both accepted.

  Note that control pin "C" for 5 V tolerant Fail-Safe cells must always be fixed high during normal operation.

(3) In cases in which both HV_{DD} and LV_{DD} are cut-off

a) If inputs from the outside also enter High-Z state when the power supplies are cut-off

Basically, all types of input/output buffers can be used. Even in cases in which input/output buffers are separated by pairs of power supply pins and the power supplies for part of the area are to be cut off, all types of input/output buffers can be used unless signals from the outside are applied.

(However, this is possible provided that the power supplies for all of the related circuits, including the internal cell area, are cut-off.)

b) If input signals from the outside are applied when the power supplies are cut-off or pull-up resistors are incorporated external to the chip

- LV_{DD} cells

  If input signals from the outside are applied while the power supplies are cut-off, leakage current may occur, depending on the type of input/output buffer used. Therefore, the following types of input/output buffers cannot be used in this design:

  - Input buffers with pull-up resistors. However, this does not include Fail-Safe cells.
  - Output buffers other than Fail-Safe buffers. However, the Open drain type can be used.
  - Bi-directional buffers other than Fail-Safe buffers. However, the Open drain type can be used.

- HV_{DD} cells

  (1) For HV_{DD} input signals, leakage current may occur depending on the type of input/output buffer used, as with LV_{DD} cells. The following types of input/output buffers cannot be used in this design.

  - 3V-PCI cells and input buffers with pull-up resistors
  - Output buffers other than Open drain buffers
  - Bi-directional buffers other than Open drain buffers

  (Even in cases in which input/output buffers are separated by pairs of power supply pins and the power supplies for part of the area are to be cut off, the input/output buffers mentioned above cannot be used in the relevant area.)

  (2) When handling 5.0 V input signals or using external 5.0 V pull up resistors, no HV_{DD} cells can be used.

- 5 V Tolerant Fail Safe cells

  (1) When handling HV_{DD} input signals, all 5 V tolerant Fail Safe cells can be used.
  Note that control pin “C” for 5 V tolerant Fail-Safe cells must always be fixed high during normal operation.

  (2) When handling 5.0 V input signals or using external 5.0 V pull up resistors, no HV_{DD} cells can be used.

Chapter 10 Circuit Design that Takes Testability into Account

When ICs are shipped from the Epson factory, they are tested for product fitness through the use of an LSI tester. This requires that circuits be designed in consideration of the testability of the IC. Therefore, be sure to take the points specified below into consideration in the design of a circuit. The contents described here do not apply to combined use with JTAG circuits. If JTAG circuits are desired, refer to Section 10.8, "Boundary Scan Design," and create test patterns that are capable of performing DC testing. Furthermore, if test circuits cannot be added, contact the sales division of Epson for confirmation.

10.1 Consideration Regarding Circuit Initialization

Although a number of flip-flops (FFs) are used in a circuit, the initial state of all FFs is X (indeterminate) when the circuit is tested using an LSI tester or simulated on a simulator. For this reason, depending on the circuit configuration, the circuit cannot be initialized or requires a huge number of test patterns for initialization. To avoid this problem, in the design of a circuit, be sure to use FFs with reset inputs or other means in order to enable the circuit to be initialized easily.

10.2 Consideration Regarding Compressing the Test Patterns

As the circuit size increases, so does the size of test patterns. Be aware, however, that the size of test patterns is subject to the following limitations imposed by the use of an LSI tester.

Number of events per test pattern : Up to 256K events
Number of test patterns : Up to 30
Total number of events in all test patterns: Up to 1M events

These limitations apply to test patterns for DC testing, including test patterns for Z inspection, test patterns for test circuits, and test patterns for ROM or megacells prepared by Epson. For details on the number of ROM or megacell test patterns and the number of events in those test patterns, contact the sales division of Epson. For RAM test patterns, note that although the reference patterns prepared by customers are subject to said limitations, the test patterns for complete RAM pattern verification prepared by Epson are not subject to limitations.

In the design of a circuit, be sure to use an appropriate means of improving the circuit's testability and thereby reducing the number of necessary test patterns by, for example, installing test pins that enable a clock to be input in the middle of a multi stage counter, or by adding test pins that allow the LSI's internal signals to be monitored.

10.3 Test Circuit Which Simplifies DC and AC Testing

For the S1X60000 series, customers are expected to configure a test circuit and add it to the test circuit in order to allow shipment testing such as DC and AC testing by Epson to be performed efficiently. If a test circuit cannot be added to your circuit, please contact Epson for confirmation.

10.3.1 Configuration of Test Circuits

Figure 10-1 shows the configuration of the test-mode control circuit "TCIR2" recommended by Epson.

Figure 10-2 shows a typical test circuit with a test mode control circuit "TCIR2" and a 2 word × 2 bit (this configuration is for illustrative purpose only) RAM test circuit. Refer to these circuits and (1) through (4) below when configuring a test circuit. If RAM or functional cells are included in your circuit, also refer to Section 10.4, "Memory Block Test Circuits," and Section 10.6, "Function Cell Test Circuits."

(1) Adding and selecting pins for testing

To configure pins for testing, add the four types of test pins specified below.
For these test pins, select appropriate cells or buffers available.

- Test enable input pin : 1 pin
- Test mode select input pin : 4 pins
- Monitor output pin for AC testing: 1 pin
- Monitor output pin for DC testing: 1 pin

Table 10-1 Test Pins Constraints

Test Pin Type	Number of Pins	Name of Pins (ex.)	Constraints, Notes, etc.
Test enable input pin	1 pin	TSTEN	Dedicated input pin. Use ITST1 for the input buffer. H: test mode; L: normal mode
Test mode select input pin	4 pins	INP0 to INP3	Input pin shareable with the user functions, but cannot be shared with bi-directional pins. Avoid sharing this pin with other input pins that have a critical path.
Monitor output pin for AC testing	1 pin	OUT3	Input pin shareable with the user functions, but cannot be shared with N-channel open drain cells. Type S and Type M are not available.
Monitor output pin for DC testing	1 pin	OUT4	Input shareable with the user functions, but cannot be shared with bidirectional, 3-state terminal or N-channel open drain pins.
Output and input/output pins	—	—	Output buffer with test mode (bi-directional buffer used)

- DC testing

  This test checks whether all input and output pins satisfy the designated specifications for DC characteristics. If no test circuits are included, customers will be requested to create test patterns to enable measurement of DC characteristics, which may require a huge number of man-hours. Use of a test circuit facilitates the creation of test patterns and therefore makes it easy to measure DC characteristics.

- AC testing

  This test involves measuring pin to pin delays (delays in input pins to output pins). If the actual operating frequency cannot be inspected using an LSI tester, the operating speed will be guaranteed by measuring the delay in a specific path. If the Epson-recommended test circuit "TCIR2" is used, variations between lots will be

evaluated by measuring the dedicated AC path using an AC test monitor output pin. Because the recommended test circuit "TCIR2" does so by judging the difference in measured values between the tested device's delay and the bypass delay, consistent delay measurement that is not dependent on the intra chip location of the test circuit or measurement conditions external to the chip is always possible.

(2) Adding and connecting a test-mode control circuit

a: Add a test mode control circuit (TCIR2).

b: Connect output X pin and LG pin for the input buffer (ITST1) of the dedicated test-mode input pin to the input TST pin and ILG pin of the "TCIR2".

c: Connect the outputs for the input buffers of test-mode select input pins to the input pins of the test mode control circuit "TCIR2".

- Connect the X pin for the INP0 input buffer to the TM0 pin of the "TCIR2".
- Connect the X pin for the INP1 input buffer to the TM1 pin of the "TCIR2".
- Connect the X pin for the INP2 input buffer to the TM2 pin of the "TCIR2".
- Connect the X pin for the INP3 input buffer to the TM3 pin of the "TCIR2".

d: Connect the output pins of the test-mode control circuit "TCIR2" to the input pins of the input/output buffers.

- Connect the output pin (TAC) of the TCIR2 to the TA pin of the input/output buffer of the AC test monitor output pin (OUT3).
- Connect the output pin (OLG) of the TCIR2 to the TA pins of the input/output buffer of the DC test monitor output pin (OUT4).
- Connect the output pin (TD) of the TCIR2 to the TA pins of all input/output buffers other than the AC and DC test monitor output pins (OUT3 and OUT4).
- Connect the output pin (TE) of the TCIR2 to the TE pins of the input/output buffers for the 3-state pin (OUT2) and bi-directional pin (BID1).
- Connect the output pin (TS) of the TCIR2 to the TS pins of all input/output buffers.
- Use the output pin (MS) of the TCIR2 for control of each macro when RAM or function cells are included in your circuit.

e: Even if the signals connected to the TA, TE, or TS pins of input/output buffers exceed the Fan-Out limits, the violation of the Fan-Out limits can be ignored without causing any problem.

(3) Typical examples for setting test mode

a: DC test

- Quiescent current measurement mode *1

  TSTEN ... High

  *1: When the macros to be installed include a quiescent current measurement mode, that measurement mode must be prepared separately.

- Output characteristic (V_{OH}/V_{OL}) measurement mode

  TSTEN ... High
  INP0 ... Low
  INP1 ... High or Low
  INP2 ... Low
  Measured pins*2 ... High or Low

*2: This includes all output and all bi-directional pins other than the DC test monitor output pin.

- Input characteristic (V_{IH}/V_{IL}) measurement mode

TSTEN	... High
Measured pins *3	... Low
Non-measured pin	... High
DC test monitor output pin	... High or Low

*3: All input and all bi-directional pins (except TSTEN) must be tested.

- Leakage current measurement mode

TSTEN	... High
INP0	... High
INP1	... Low
INP2	... High
Measured pins*4	... High or Low
3-state and Nch open drain pins	... High impedance

*4: This includes all 3-state output and all bi-directional pins other than INP0-2.

b: Dedicated AC test

- Dedicated AC path measurement mode

TSTEN	... High
INP0	... Low
INP1	... Low
INP2 *5	... Change to High or Low (input signal for the measured device)
INP3 *5	... Select High (delay cell delay) or Low (bypass delay) (Measured device select pin)
AC test monitor output pin	... Outputs a signal corresponding to input for INP2.

*5: After selecting the measured device using INP3, change INP2 to High or Low in the next and subsequent events. In a pattern in which INP2 and INP3 change state simultaneously, delays cannot be measured accurately. Refer to Figure 10-3, “Example of the Generation of a Test Pattern When There is a Test Option.”

c: Macro test

- Macro-test mode

TSTEN	... High
INP0	... High
INP1	... Low
INP2	... Low
Macro control pin in test mode*6	... Depends on the macro function
Macro watch pin in test mode*6	... Depends on the macro operation

*6: This pin is assigned for macro control or watch in test mode.

Table 10-2 Truth Table for Test Circuit

INPUT						OUTPUT					
TST	**ILG**	**TM3**	**TM2**	**TM1**	**TM0**	**TS**	**TD**	**TE**	**TAC**	**OLG**	**MS**
0	×	×	×	×	×	0	0	0	0	0	0
1	1	×	×	×	×	1	×	×	×	1	×
1	0	×	×	×	×	1	×	×	×	0	×
1	×	×	1	1	1	1	1	1	1	×	0
1	×	×	1	1	0	1	1	1	1	×	0
1	×	×	1	0	1	1	1	1	1	×	0
1	×	×	0	1	1	1	1	1	1	×	0
1	×	×	0	0	1	1	1	0	1	×	1
1	×	×	0	1	0	1	1	0	1	×	0
1	×	0	1	0	0	1	0	0	1	×	0
1	×	0	0	0	0	1	0	0	0	×	0
1	×	1	1	0	0	1	0	0	1	×	0
1	×	1	0	0	0	1	0	0	0	×	0

(4) Generating the test patterns

To ensure that DC and AC testing are conducted efficiently, customers will be requested to design both a test circuit and a test pattern. Figure 10-3 shows a practical example of a test pattern for the example test circuit shown in Figure 10-2. Note the following points in generating the test pattern.

a. Generate a test pattern like the one shown in the example, separately from a pattern for circuit verification.

b. This test pattern must contain a description of all pins used in the circuit.

c. A test pattern for measuring both delay cell delay and bypass delay for AC testing is required. Referring to Figure 10-3, generate a test pattern that allows two pulses to be applied in each mode.

d. In a pattern for circuit verification as well, write test pins (TSTEN). In such a case, the input level at the test mode select pin (TSTEN) must be set to logic 0 for selecting normal mode.

e. When the input level for the test enable pin (TSTEN) is logic 1, all of the pull-up/pull-down resistors enter an inactive state.

(5) Circuit configuration of the test mode control circuit “TCIR2”

Shown in Figure 10-1 is the circuit configuration of the test mode control circuit “TCIR2” recommended by Epson. The TCIR2 places the entire circuit in test mode and provides an efficient means of conducting DC and AC testing for the LSI.

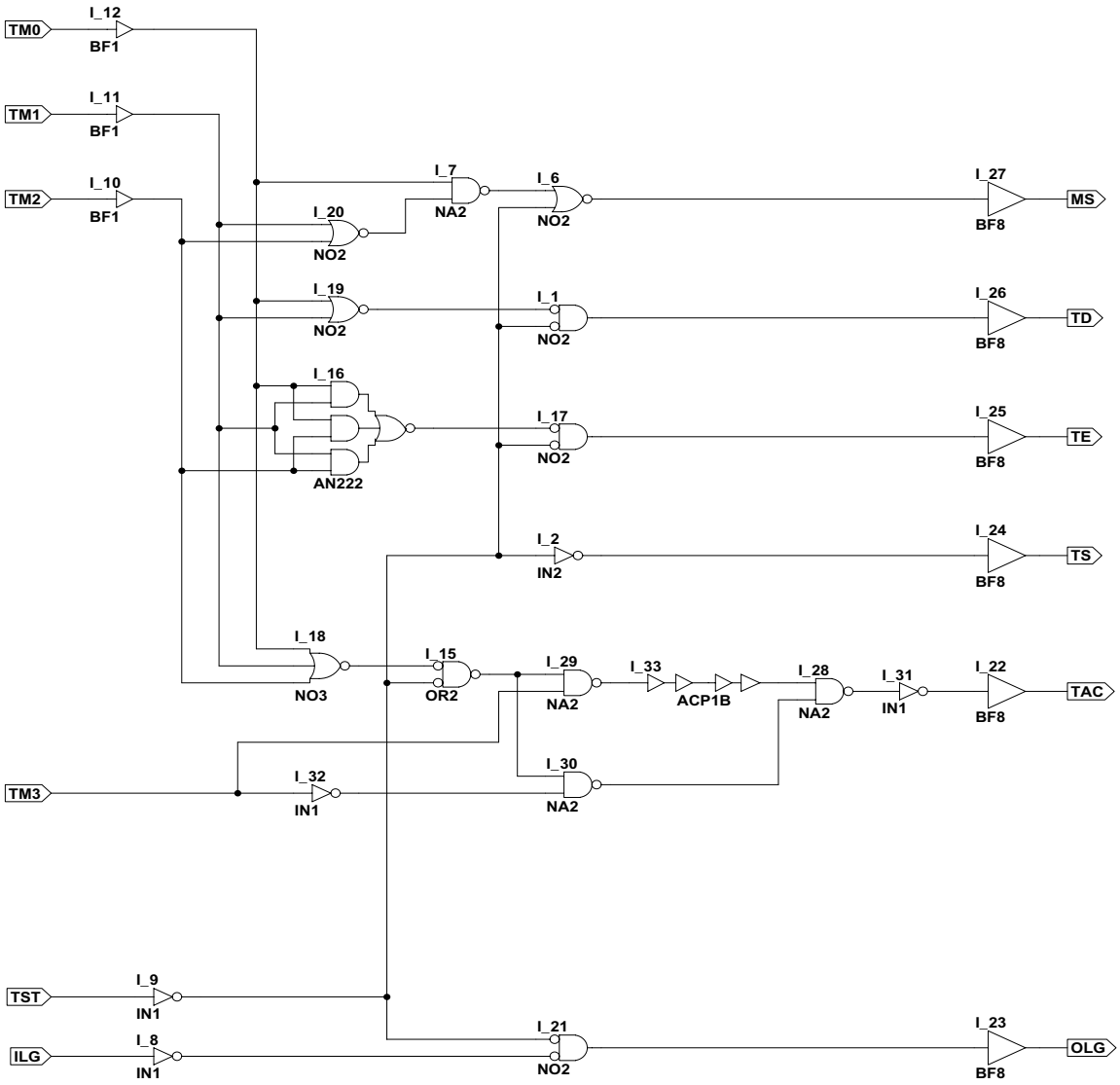


Figure 10-1 Internal Circuit of the TCIR2

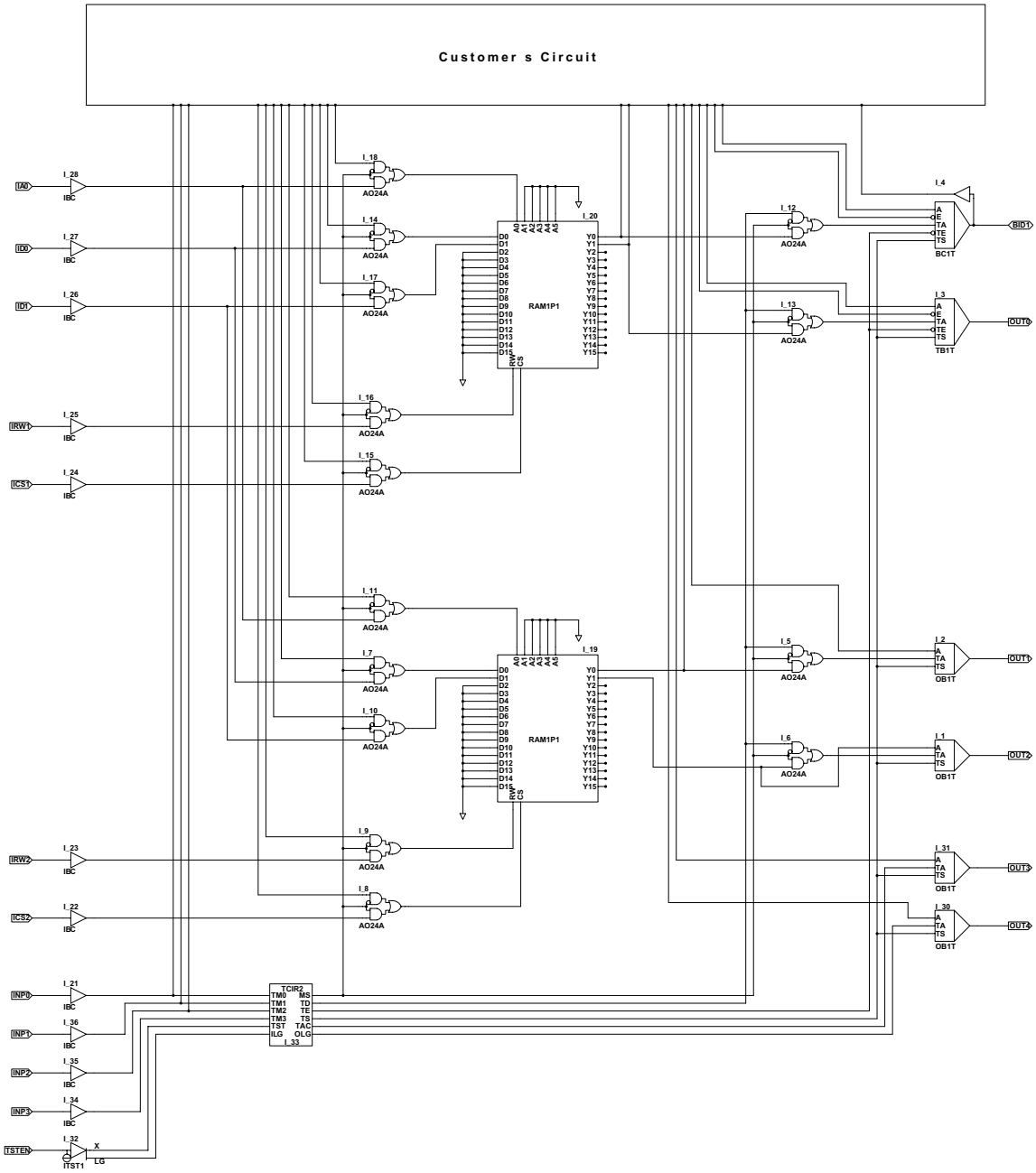


Figure 10-2 Example of a Test Circuit

● **Example of the APF format**

```
# EXAMPLE of Test Pattern for AC & DC Test by TCIR2
$RATE 200000
$RESOLUTION  0.001ns
$STROBE  185000
$NODE
TSTEN          ID   0
INP0           I    0
INP1           I    0
INP2           I    20000     #difference measurement
INP3           I    0
IA0            I    0
ID0            I    0
ID1            I    0
ICS1           I    0
ICS2           I    0
IRW1           I    0
IRW2           I    0
BID1           B    0
OUT0           O
OUT1           O
OUT2           O
OUT3           O
OUT4           O
$ENDNODE
$PATTERN
#       TIIIIIIIIIIIBOOOOO
#       SNNNNADDCCRRIUUUUU
#       TPPPP001SSWWDTTTTT
#       E0123   1212101234
#       N
#
#       IIIIIIIIIIIBOOOOO
#                 U
#
      0 00000.......XXXXXX
      1 10000.......LLLLLX:  Dedicated AC path measurement 1 (bypass)
      2 10010.......LLLLHX           ↑
      3 10000.......LLLLLX           ↑
      4 10001.......LLLLLX:  Dedicated AC path measurement 2 (delay path)
      5 10011.......LLLLHX           ↑
      6 10001.......LLLLLX           ↑
      7 11010.......0ZHHHX:  Off state leakage-current measurement
      8 11010.......1ZHHHX           ↑
      9 10000.......LLLLLX:  Output characteristic measurement
     10 10100.......HHHHHX           ↑
$ENDPATTERN
#
# EOF
```

Note: The '.' Denotes logic 1 or 0.

Figure 10-3 Example of the Generation of a Test Pattern When There is a Test Option

10.4 Memory Block Test Circuits

10.4.1 Basic Cell Type RAM

When a RAM is used it is necessary to test all bits before shipping the product. RAM terminals must be accessible via primary I/O pins.

RAM test circuitry can be implemented, which multiplexes existing pin functionality with direct RAM access functionality so as to avoid increasing the designs pin count.

No bi-directional pins can be used for input as they all are placed in an output state during RAM test. If input pins are inadequate, attach a control circuit to the target bi-directional TE pin.

Also, when multiple RAMs are used, we recommend that each RAM's pins be accessible via unique I/O pins. However, when the number of external I/O pins is inadequate, each RAM's pins may share common external I/O pins.

The example test circuit in Figure 10-2 performs normal operations unless in test mode; when placed in test mode, the circuit allows data to be written directly to RAM from external pins ICS1-2, IRW1-2, ID0-1, and IA0. At the same time, RAM output in this circuit can be read out to external pins AY0 and AY1.

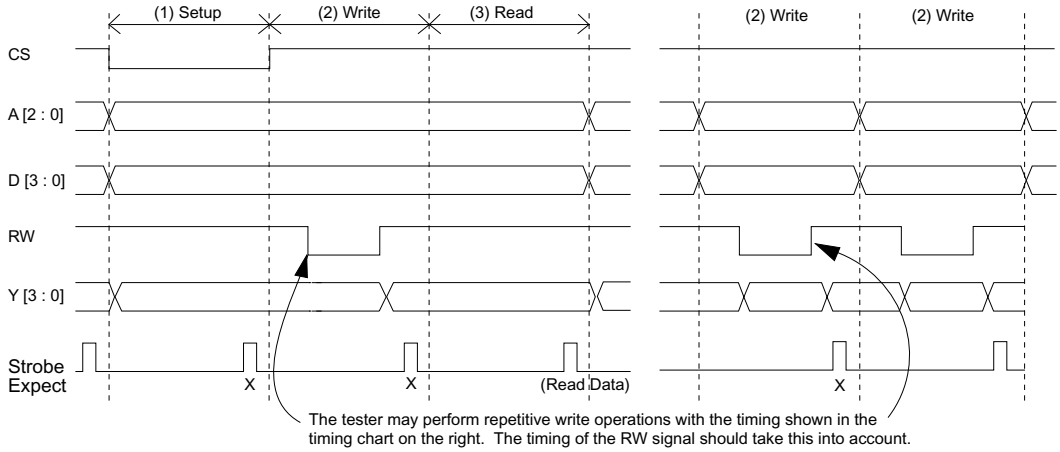
Although it is possible to share the RAM pins with bi-directional pins or 3-state output pins, it is necessary to tie the bi-directional pins to either an input or an output state during RAM test. However, please do not allocate an input buffer with a pull-up resistor to CS, because doing so would make it impossible to measure the quiescent current.

10.4.1.1 RAM Test Patterns

After incorporating RAM test circuitry, it is necessary to make test patterns for both the normal operating state and the test state of the chip. Checks are performed in the normal state to verify the connection with the customer's circuits, and are performed to insure that the test circuit is correct in the test state. Also, we request a test pattern to serve as a template when Epson generates the RAM test pattern. Note that there are asynchronous 1 port and 2 port types, and synchronous 1 port and 2 port types of Basic Cell type RAM, and for each of which the method of creating a test pattern differs. Figures 10-4 and 10-5 show the procedures for creating test patterns for asynchronous type RAM; Figures 10-6 and 10-7 show those for synchronous type RAM.

This pattern serves as a template for 1 port RAM tests.

• Timing Chart



• Example of APF Format

```
$RATE  200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA    I  0
INPB    I  0
INPC    I  0
INPD    I  0
INPE    I  0
INPF    I  0
INPG    I  0
INPH    N  20000 120000
INPI    I  0
  .
  .
OUTA    0
OUTB    0
OUTC    0
OUTD    0
  .
  .
$ENDNODE

$PATTERN
#              AAADDDDRC  YYYY
#              0120123WS  0123
#
          0    000101010..XXXX..
          1    0001010N1..XXXX..
          2    000101011..HLHL..
          3    101111110..XXXX..
          4    1011111N1..XXXX..
          5    101111111..HHHH..
          6    111010110..XXXX..
          7    1110101N1..XXXX..
          8    111010111..LHLH..
```

Please provide all I/O pins used in performing simulation.

Reference the timing chart below to set timing.

It is useful to place comments here.

When a sequence is necessary to set the test mode, input the pattern here.

[1] Access the lowest address, a middle address and the highest address.

[2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. In the next event, perform a write. In the third event, perform a read.

[3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a signal event.

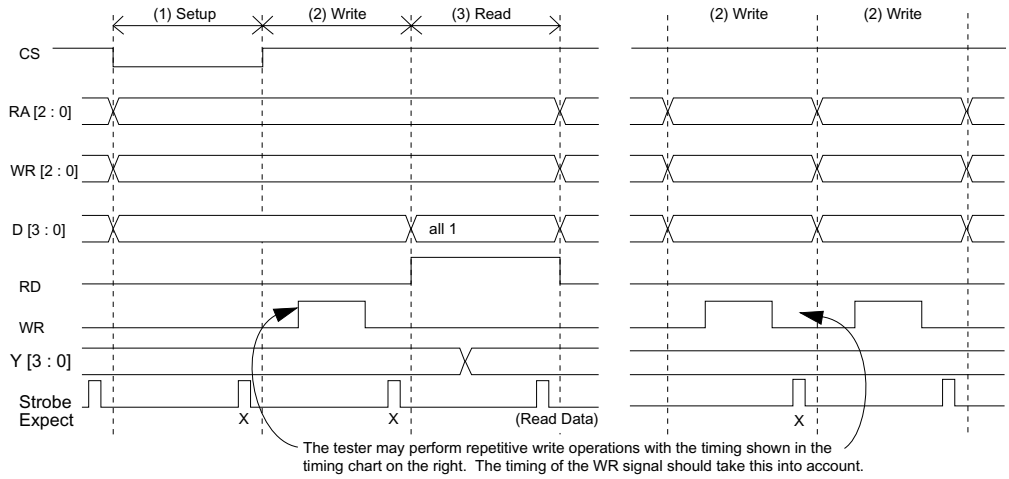
[4] Change the data to be written for each address tested.

[5] Verify that the results are the same as expected form the results of the simulations.

Figure 10-4 Generating 1 port RAM Test Pattern

This pattern serves as a template for 2 port RAM tests.

• Timing chart



• Example of APF Format

```
$RATE  200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA    I  0
INPB    I  0
INPC    I  0
INPD    I  0
INPE    I  0
INPF    I  0
INPG    I  0
INPH    I  0
INPI    I  0
INPJ    I  0
INPK    I  0
INPL    P  20000 120000
INPM    I  0
  .
  .
OUTA    0
OUTB    0
OUTC    0
OUTD    0
  .
  .
$ENDNODE

$PATTERN
#              RRRWWW
#              AAAAAADDDDRWC.YYYY..
#              0120120123DRS.0123..
#
          0    0000001010000.XXXX..
          1    0000001010OP1.XXXX..
          2    0000001111101.HLHL..
          3    1011011111000.XXXX..
          4    1011011111OP1.XXXX..
          5    1011010000101.HHHH..
          6    1111110101000.XXXX..
          7    1111110101OP1.XXXX..
          8    1111111111101.LHLH..
```

Please provide all I/O pins used in performing simulation.

Reference the timing chart below to set timing.

It is useful to place comments here.

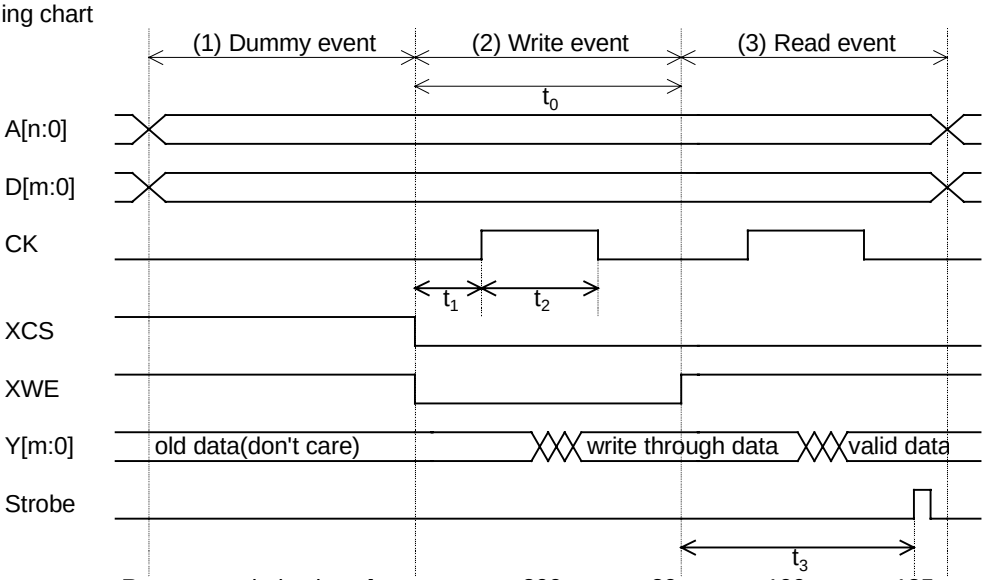
When a sequence is necessary to set the test mode, input the pattern here.

[1] Access the lowest address, a middle address and the highest address.
[2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. In the next event, perform a write. In the third event, perform a read.
[3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a signal event.
[4] Change the data to be written for each address tested.
[5] Verify that the results are the same as expected form the results of the simulations.
[6] Set all bits of data to "1" when reading. However, if all bits of the data to write are 1's, all bits of data during reading must be 0's.

Figure 10-5 Generating 2 port RAM Test Pattern

●This pattern serves as a test template.

• Timing chart



Recommended values for t_0 to t_3: t_0 = 200 ns, t_1 = 20 ns, t_2 = 100 ns, t_3 = 185 ns

• Example for APF format (16 words x 4 bits)

```
$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
$NODE
IA3  I  0
IA2  I  0
IA1  I  0
IA0  I  0
ICK  P  20000 120000
IXCS I  0
IXWE I  0
ID3  I  0
ID2  I  0
ID1  I  0
ID0  I  0
 ...
OY3  O
OY2  O
OY1  O
OY0  O
$ENDNODE

$PATTERN
#    AAAACXXDDDD···YYYY
#    3210KCW3210···3210
#         SE
  0  00000010000···XXXX
  1  0000P100000···XXXX
  2  0000P110000···LLLL
  3  01010010101···XXXX
  4  0101P100101···XXXX
  5  0101P110101···LHLH
  6  11110011111···XXXX
  7  1111P101111···XXXX
  8  1111P111111···HHHH
$ENDPATTERN
```

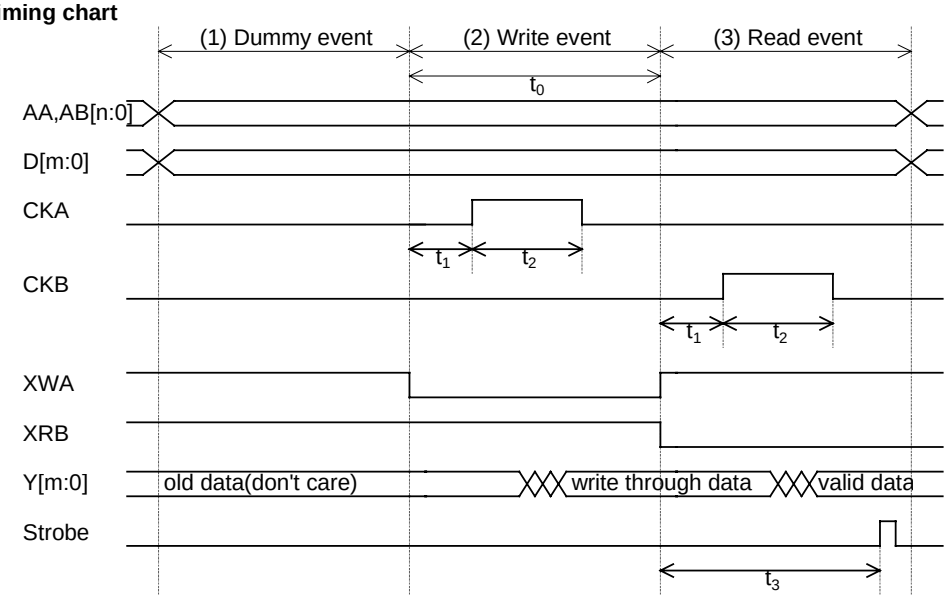
Be sure to write all I/O pins to ensure that simulations are performed.

(1) Access the test pattern for the dummy, write, and read events in one operation (one tester cycle) and perform the test three times: first the lower address, then the middle address, then the upper address.
(2) Set the address and data at the beginning of a dummy event, write the data in a write event, and read the data in a read event.
(3) Apply CK as a pulse (RZ waveform).
(4) Change the write data after each access operation.
(5) If there is a test mode setup sequence, be sure to insert it prior to event 0. (Event numbers need to be reassigned.)
(6) After creating a test pattern, always confirm its functionality through logic simulation. When simulated, the test pattern will produce an output during a dummy event (old data) and an output during a write event (write-through data). However, because these outputs do not need to be verified, we recommend that they be rewritten to indeterminate values before being interfaced to the tester.

Figure 10-6 Procedure for Creating Test Patterns for 1 port RAM (Synchronous) Test Pattern

●This pattern serves as a test template.

• Timing chart



Recommended values for t_0–t_3: t_0 = 200 ns, t_1 = 20 ns, t_2 = 100 ns, t_3 = 185 ns

• Example for APF format (16 words x 4 bits)

```
$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
$NODE
IA3   I  0
IA2   I  0
IA1   I  0
IA0   I  0
ICKA  P  20000 120000
IXWA  I  0
ID3   I  0
ID2   I  0
ID1   I  0
ID0   I  0
 ...
IAB3  I  0
IAB2  I  0
IAB1  I  0
IAB0  I  0
ICKB  P  20000 120000
IXRB  I  0
OY3   O
OY2   O
OY1   O
OY0   O
$ENDNODE

$PATTERN
#    AAAACXDDDD···AAAACXYYYY
#    AAAAKW3210···BBBBKR3210
#    3210AE    ···3210BB
  0  0000010000···000001XXXX
  1  0000P00000···000001XXXX
  2  0000010000···0000P0LLLL
  3  0101010101···010101XXXX
  4  0101P00101···010101XXXX
  5  0101010101···0101P0LHLH
  6  1111011111···111101XXXX
  7  1111P01111···111101XXXX
  8  1111011111···1111P0HHHH
$ENDPATTERN
```

Be sure to write all I/O pins to ensure that simulations are performed.

(1) Access the test pattern for the dummy, write, and read events in one operation (one tester cycle) and perform the test three times: first the lower address, then the middle address, then the upper address.
(2) Set the address and data at the beginning of a dummy event, write the data in a write event, and read the data in a read event.
(3) Apply CK as a pulse (RZ waveform).
(4) Change the write data after each access operation.
(5) If there is a test mode setup sequence, be sure to insert it prior to event 0. (Event numbers need to be reassigned.)
(6) After creating a test pattern, always confirm its functionality through logic simulation. When simulated, the test pattern will produce an output during a dummy event (old data) and an output during a write event (write-through data). However, because these outputs do not need to be verified, we recommend that they be rewritten to indeterminate values before being interfaced to the tester.

Figure 10-7 Procedure for Creating 2 port RAM (Synchronous) Test Pattern

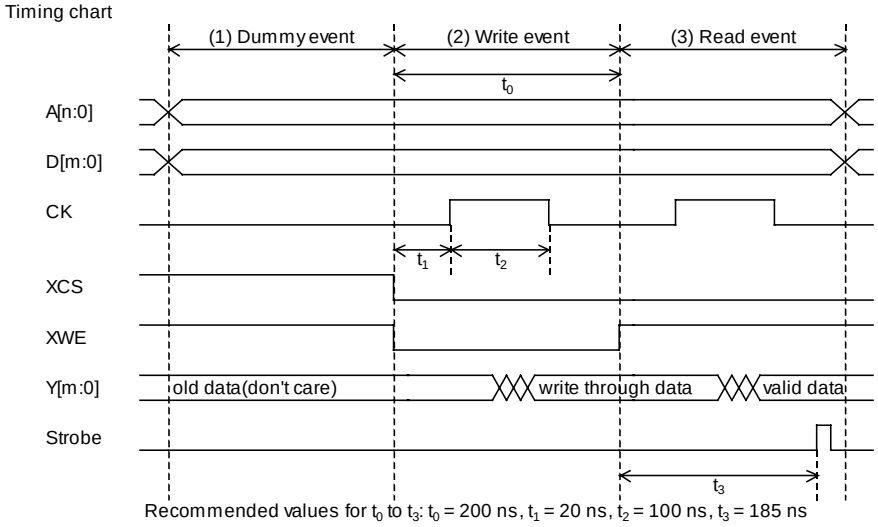
10.4.2 Standard Type 1 port RAM

For standard type 1 port RAM, as for Basic cell type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (Epson will use the test state test patterns as templates as it creates dedicated RAM test patterns.) (For details, refer to Section 10.4.1, "Basic Cell Type RAM.")

When creating test-state test patterns for standard-type 1 port RAM, please follow the prescribed procedure.

● **This pattern serves as a test template.**

• Timing chart



Recommended values for t_0 to t_3: t_0 = 200 ns, t_1 = 20 ns, t_2 = 100 ns, t_3 = 185 ns

• Example for APF format (16 words x 4 bits)

```
$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
$NODE
IA3  I  0
IA2  I  0
IA1  I  0
IA0  I  0
ICK  P  20000 120000
IXCS I  0
IXWE I  0
ID3  I  0
ID2  I  0
ID1  I  0
ID0  I  0
  ...
OY3  O
OY2  O
OY1  O
OY0  O
$ENDNODE

$PATTERN
#     AAAACXXDDDD...YYYY
#     3210KCW3210...3210
#          SE
  0   00000010000...XXXX
  1   0000P100000...XXXX
  2   0000P110000...LLLL
  3   01010010101...XXXX
  4   0101P100101...XXXX
  5   0101P110101...LHLH
  6   11110011111...XXXX
  7   1111P101111...XXXX
  8   1111P111111...HHHH
$ENDPATTERN
```

Be sure to write all I/O pins to ensure that simulations are performed.

(1) Access the test pattern for the dummy, write, and read events in one operation (one tester cycle) and perform the test three times: first the lower address, then the middle address, then the upper address.
(2) Set the address and data at the beginning of a dummy event, write the data in a write event, and read the data in a read event.
(3) Apply CK as a pulse (RZ waveform).
(4) Change the write data after each access operation.
(5) If there is a test mode setup sequence, be sure to insert it prior to event 0. (Event numbers need to be reassigned.)
(6) After creating a test pattern, always confirm its functionality through logic simulation. When simulated, the test pattern will produce an output during a dummy event (old data) and an output during a write event (write-through data). However, because these outputs do not need to be verified, we recommend that they be rewritten to indeterminate values before being interfaced to the tester.

Figure 10-8 Procedure for Creating Test Patterns for Standard type 1 port RAM

10.4.3 Standard Type Dual port RAM

For standard type dual port RAM, as for Basic cell type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (Epson will use the test state test patterns as templates as it creates dedicated RAM test patterns.) (For details, refer to Section 10.4.1, "Basic Cell Type RAM.")

When creating test state test patterns for standard type dual port RAM, although essentially the same procedure applies as is described in Section 10.4.2, "Standard Type 1 port RAM," please follow the specific procedure described below, so that test patterns will be created separately (depending on how the ports are used).

(1) When using as dual port RAM (reading and writing on both ports A and B), create the following two test patterns:*

- Test pattern 1: Write from port A, read from port A
- Test pattern 2: Write from port B, read from port B

(2) When using as 2 port RAM (writing on port A, reading on port B), create the following (one) test pattern.

- Test pattern 1: Write from port A, read from port B

(3) When using as 3 port RAM (reading and writing on port A, reading on port B), create the following two test patterns:*

- Test pattern 1: Write from port A, read from port A
- Test pattern 2: Write from port A, read from port B

* To prevent possible simultaneous access of the same address, please avoid writing the same test pattern for test patterns 1 and 2.

10.4.4 High Density Type RAM

For high density type RAM, as for Basic cell type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (The test state test patterns become a template which Epson will use as it creates dedicated RAM test patterns.) (For details, refer to Section 10.4.1, "Basic Cell Type RAM.")

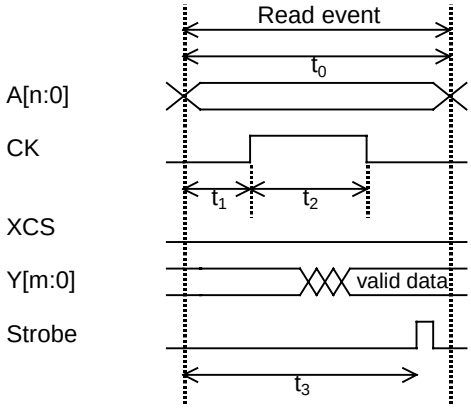
Regarding test state test patterns for the high density type RAM, essentially the same procedure applies as is described in Section 10.4.2, "Standard Type 1 port RAM."

10.4.5 Mask ROM

For mask ROM, as for Basic cell type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (For details, refer to Section 10.4.1, "Basic Cell Type RAM.")

When creating the mask ROM test state test patterns, please follow the procedure described below in order to ensure that data can be read out from all addresses.

• Timing chart



Recommended values for t_0–t_3: t_0 = 200 ns, t_1 = 20 ns, t_2 = 100 ns, t_3 = 185 ns

• Example for APF format (16 words x 4 bits)

```
$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
$NODE
IA3  I  0
IA2  I  0
IA1  I  0
IA0  I  0
ICK  P  20000 120000
IXCS I  0
 …
OY3  O
OY2  O
OY1  O
OY0  O
$ENDNODE

$PATTERN
#          AAAACX···YYYY
#          3210KC···3210
#                S
      0  0000P0···LLHH
      1  0001P0···LLHL
      2  0010P0···LLLL
      3  0011P0···LHLL
        ···
     12  1100P0···HHHL
     13  1101P0···HHLH
     14  1110P0···HLHH
     15  1111P0···LHHH
$ENDPATTERN
```

Be sure to write all I/O pins to ensure that simulations are performed.

(1) Perform read operations on all addresses, based on the read event shown above. Addresses may be changed in any order, as desired.
(2) CK must be applied as a pulse (RZ waveform). There is no need to stop the clock.
(3) If there is a test-mode setup sequence, be sure to insert it prior to event 0. (Event numbers need to be reassigned.)

Figure 10-9 Procedure for Creating Mask ROM Tes Patterns

10.5 Memory BIST Design

The S1X60000 series comes equipped with a memory self diagnostic circuit called the "Memory BIST (Built In Self Test)," which may be used as a test circuit for testing the LSI's internal memory. Use of the memory BIST provides numerous advantages, including those specified below.

- Eliminates the need for customers to design a memory test circuit
- Allows the number of external pins for memory testing to be reduced
- Capable of testing memory at an actual high operating speed
- Allows the time required for memory testing using an LST tester to be reduced

In addition, it offers versatile optional functions such as a bypass circuit (transparent circuit) for memory inputs, as a means of increasing fault detection rates for the entire chip.*1

Note *1: If fault detection rates are to be increased, the LSI must be modified so as to be suitable for SCAN testing following the insertion of a bypass circuit. If it is necessary to make the entire chip suitable for SCAN testing, a bypass circuit must also be optionally included in the memory BIST.

10.5.1 Outline of the Memory BIST Circuit Block

The memory BIST generates a circuit known as a "collar" in the periphery of the memory, and a circuit known as a "controller" that controls the collar. If multiple pieces of memory are included, multiple collars are generated that can be controlled by a single controller (for purposes of overhead reduction).

In addition, a bypass circuit or a fault diagnosis function may be added to inputs for memory as necessary. Under no circumstances can the number of elements inserted for memory inputs exceed the number of multiplexer stages, however. When the memory BIST is inserted, a circuit block becomes similar to that depicted in Figure 10-10, and a bypass circuit becomes similar to that depicted in Figure 10-11 (in both, memory BIST design is applied to synchronous type RAM).

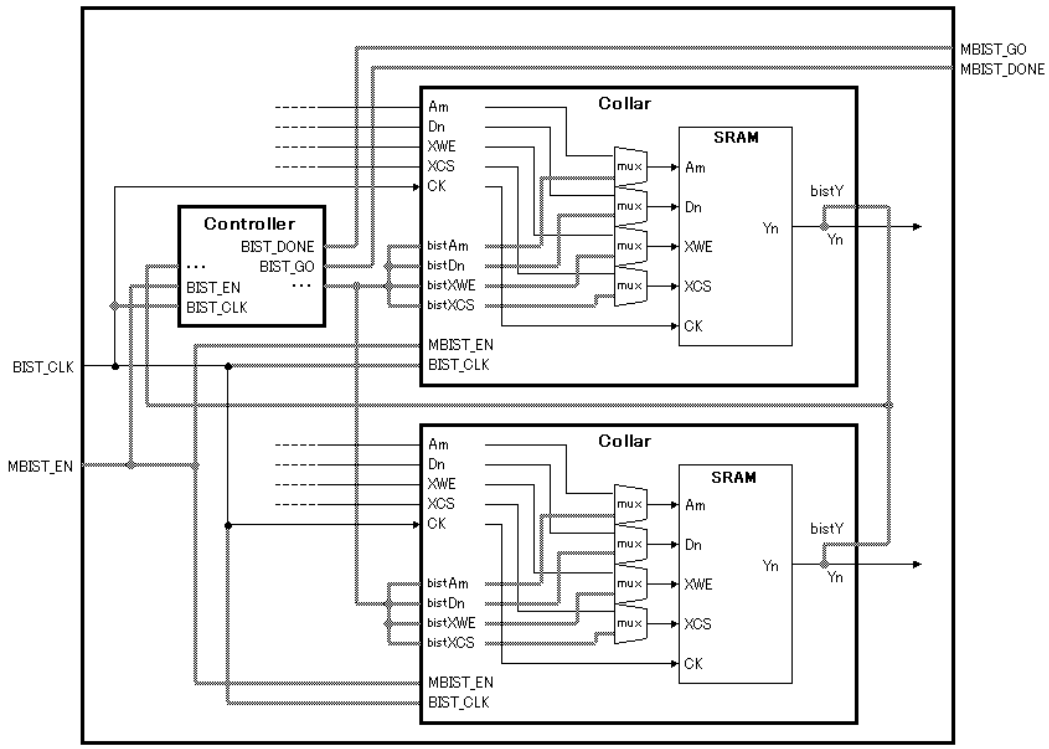


Figure 10-10 Block Diagram After Insertion of the Memory BIST Circuit

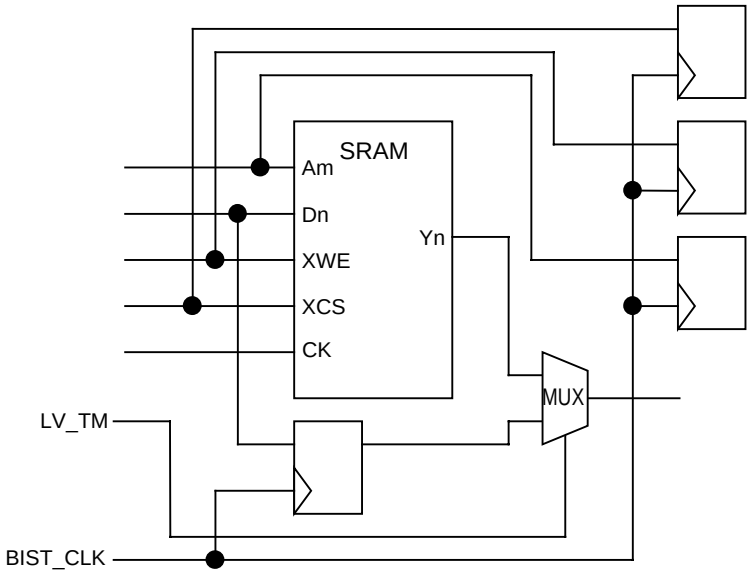


Figure 10-11 Bypass Circuit

10.5.2 Outline of the Memory BIST Circuit Test Sequence

Memory testing is started by applying a clock to the memory BIST and memory devices, and driving the enable signal (MBIST_EN) from Low to High. Immediately after testing begins, the test judge signal (MBIST_GO) goes High and the test end signal (MBIST_DONE) goes Low. Provided that the test is performed normally, the judge and end signals do not change state until completion of the test. Conversely, if any problem is encountered in the test, the judge signal goes Low (once the judge signal has gone Low, it never returns High). Testing is completed when the end signal goes High. If the judge signal is held High at this time, the test has terminated normally; if it is held Low, a problem has been encountered in the test. The test sequence of the memory BIST is similar to that depicted in Figure 10-12.

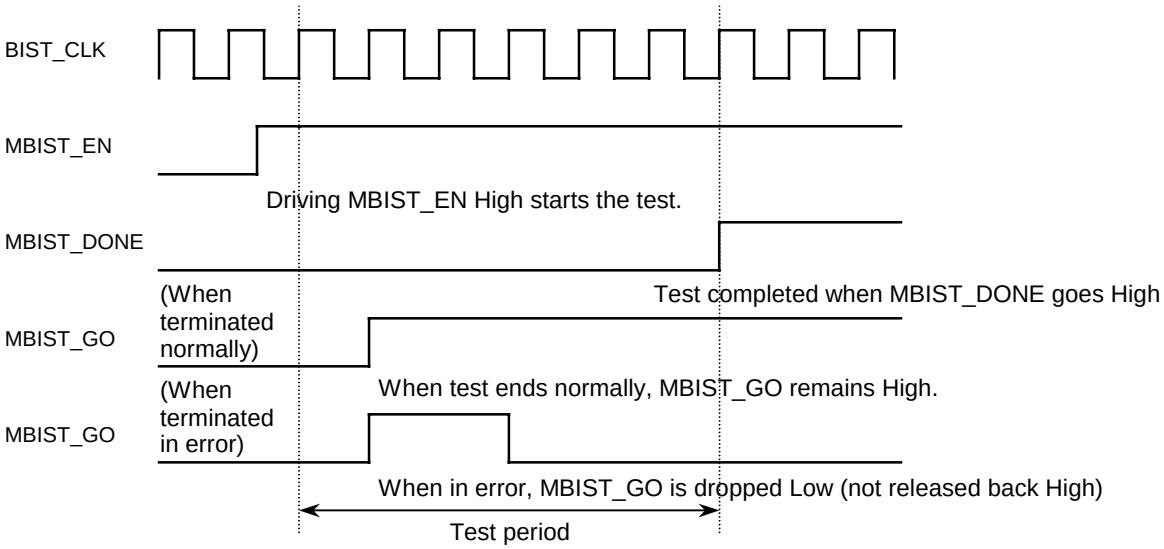


Figure 10-12 Test Sequence of the Memory BIST Circuit

10.5.3 Types of Memory Suitable for Memory BIST

The types of memory available from Epson that are suitable for the memory BIST are listed below.(*2)

- Synchronous 1 port/2 port SRAM of the basic cell type
- Synchronous 1 port/dual-port SRAM of the standard type
- High density type of synchronous 1 port SRAM
- Synchronous mask ROM(*3)

Notes *2: Certain types of memory other than those listed above are suitable for BIST. For more information, contact the sales division of Epson.

*3: For mask ROM, if ROM data is modified, the BIST circuit must be regenerated, as it contains the expected signatured values.

10.5.4 Estimating the Memory BIST Circuit Size

The circuit size of the memory BIST circuit varies significantly depending on the type and number of SRAMs, the test configuration, the BIST circuit options, and the limitations on logic synthesis. For more information, contact the sales division of Epson. For estimates, refer to Table 10-3, which lists the typical memory BIST circuits and circuit sizes in the respective cases.

Table 10-3 Circuit Sizes of Typical Memory BIST Circuits

Typical Memory Configuration	Number of Pcs.	Number of Collar Gates	Number of Controller Gates	Total
Synchronous 1 port 1024 words x 8 bits	5	1210	1553	2763
Synchronous 1 port 1024 words x 8 bits	10	2420	1723	4143
Synchronous 1 port 1024 words x 8 bits	20	4840	1888	6728
Synchronous 1 port 1024 words x 8 bits	40	9680	2219	11899
Synchronous 1 port 1024 words x 32 bits	5	2970	3471	6441
Synchronous 1 port 1024 words x 32 bits	10	5940	4081	10021
Synchronous 1 port 1024 words x 32 bits	20	11880	4624	16504
Synchronous 1 port 1024 words x 32 bits	40	23760	5766	29526
Synchronous Dual-port 1024 words x 8 bits	5	2500	1571	4071
Synchronous Dual-port 1024 words x 8 bits	10	5000	1745	6745
Synchronous Dual-port 1024 words x 8 bits	20	10000	1910	11910
Synchronous Dual-port 1024 words x 8 bits	40	2000	2254	22254
Synchronous Dual-port 1024 words x 32 bits	5	6335	3491	9826
Synchronous Dual-port 1024 words x 32 bits	10	12670	4102	16772
Synchronous Dual-port 1024 words x 32 bits	20	25340	4646	29986
Synchronous Dual-port 1024 words x 32 bits	40	50680	5802	56482

- The number of gates shown above is the result of logic synthesis performed using the Basic Cell type MSI cell.
- In each case, the circuit is configured with a single controller.
- In each case, a bypass circuit (for SCAN testing) is added.
- If 1 port and dual-port memory coexist, estimate the necessary number of gates by adding up both gate numbers for collar gates, or using dual port gate number alone for controller gates.

10.5.5 About Memory BIST Circuit Design

At Epson, memory BIST is inserted for the RTL or gate level netlists received from customers. To facilitate this operation, customers will be requested to exercise caution in the design of a circuit, as described below.

1) Test input/output pins for the memory BIST

   In memory BIST, BIST_CLK is normally substituted for by the memory clock (system clock). Therefore, the test input/output pins required for the memory BIST are basically the following three (*3):

   - MBIST_EN (mode set signal): Input pin ... Dedicated pin recommended (or can be shared with another pin if the necessary conditions are met)
   - MBIST_GO (test judge signal): Output pin ... Can be shared with another pin
   - MBIST_DONE (test end signal): Output pin ... Can be shared with another pin

Furthermore, if a bypass circuit is optionally included, the pin specified below is required. However, this pin is unnecessary if it is separately assigned when the entire chip is made suitable for SCAN testing.

- LV_TM (SCAN mode set signal): Input pin ... Can be shared with the SCAN mode set pin for the entire chip

To facilitate design, we recommend that MBIST_EN be provided as a dedicated pin. If it is necessary that MBIST_EN be shared with another pin, the entire circuit, including the customer's circuit, must be configured so as to satisfy the following initialization requirements:

- Memory BIST can be set to MBIST_EN = 0 (normal operation mode) and BIST_CLK (= memory clock) can be applied to at least two pulses.
- After the above operation has been conducted, the memory BIST can be set to MBIST_EN = 1 (BIST mode) and BIST_CLK (= memory clock) can be applied continuously.

2) Restrictions during normal operation

Circuits are added in the periphery of memory when memory BIST is applied, and this peripheral circuit must be initialized in normal operation, not just in BIST mode (unless it is initialized, the memory cannot be accessed during simulation). Therefore, the entire circuit, including the customer's circuit, must be configured so as to satisfy the following initialization requirements (*4):

- Memory BIST can be set to MBIST_EN = 0 (normal-operation mode) and BIST_CLK (= memory clock) can be applied to at least two pulses.

3) Skew adjustment of the memory clock

Because the memory BIST circuit (collars and controller) is comprised of multiple sequential circuits, clock skews must be adjusted between the memory's clock signal and the clock signals for the internal flip-flops of the BIST circuit (collars and controller). Therefore, make sure the clock for the memory to which memory BIST is to be applied is designed for optimization by Clock Tree Synthesis. For more detailed contents of the design, refer to the application cases described below.

(1) If multiple system clocks are associated with memory operation in the circuit, clock skews are generally adjusted by assigning one BIST controller to each clock (multiple BIST controllers as a whole). In such a case, the circuit must be configured so as to allow clock skews to be adjusted individually for each memory clock.

(2) Even when multiple system clocks are associated with memory operation in the circuit, if the clocks can be integrated into one line for operation in BIST mode, the memory BIST circuit can be configured with a single BIST controller. In such a case, the circuit must be configured so as to allow clock skews to be adjusted for all memory clocks in BIST mode.

(3) In cases in which multi-port memory has different clocks for the respective ports, the clock skews must be adjusted using a multiplexer. In such a case, insert a multiplexer for clocks other than the selected clock.

Notes *3: Although the BIST circuit requires BIST_CLK as its clock input when operating singly, BIST_CLK can normally be substituted for by the memory clock (system clock) or other internal clock, as initialization, skew adjustment, and the like are required. Furthermore, if the BIST circuit is configured with multiple BIST controllers, there must be as many MBIST_GO and MBIST_DONE outputs as the number of BIST controllers. For MBIST_EN input, however, a single input will suffice.

*4: This circuit configuration can also include initialization of the customer's own circuit. If the required circuit configuration cannot be designed, contact the sales division of Epson.

10.5.6 Other

- Memory BIST can be applied without concern for the restrictions associated with hierarchical design, regardless of where in the customer's circuit memory exists.
- It does not matter whether the customer's circuit contains memory for which memory BIST is applied or memory for which memory BIST is not applied.
- Before memory BIST can be inserted, customers will be requested to furnish Epson with temporary RTL or temporary netlists for the purpose of preliminary examination. A period of approximately three days is required for preliminary examination. Following completion of preliminary examination, a period of approximately one day is required for insertion of the BIST circuit. Furthermore, to facilitate insertion of memory BIST, customers are requested to present the checksheet attached herein, along with said temporary RTL or temporary netlists.

● Checksheet

(1) Have you prepared an outline drawing of the circuit blocks? Yes/No

(2) Have you specified the cells for memory BIST in the circuit? Yes/No

(3) Have you integrated memory clocks into one line for the purpose of BIST? Yes/No
(However, this is not an essential requirement.)

(4) Have you multiplexed clocks for multi-port memory for the purpose of BIST? Yes/No

(5) SRAM information

Memory Type	Instance Name of Memory	Net Name of Memory Clock *

*: If you've integrated clocks into one line or multiplexed clocks for the purpose of BIST, clearly specify the BIST mode.

(6) Test pin information

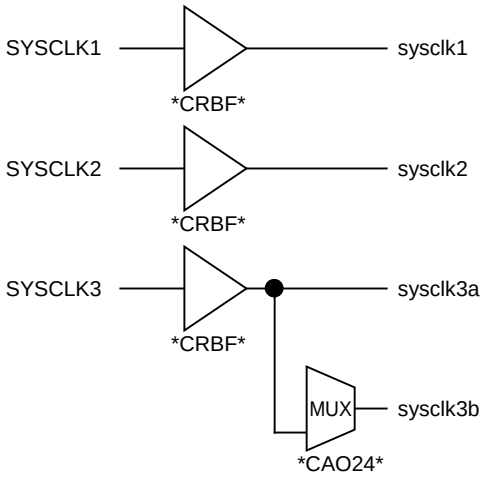
Pin Name	External Pin Name, etc.
BIST_CLK	Shared input pin name: Clock net name:, Instance name of module: Mode setting:
MBIST_EN	Dedicated input pin name: Net name:
MBIST_GO	Shared output pin name: Instance name of MUX:
MBIST_DONE	Shared output pin name: Instance name of MUX:

● Explanation of the checksheet

(1) Outline drawing of circuit blocks

Prepare an outline drawing for memory clock related circuits, like the one shown in Figure 10-13.

- When using separate memory clock lines (with clocks for multi-port memory used in common)



- When combining memory clocks into a single line (with clocks for multi-port memory used in common)

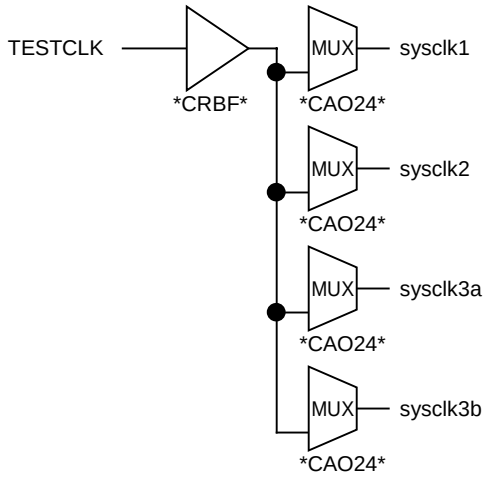
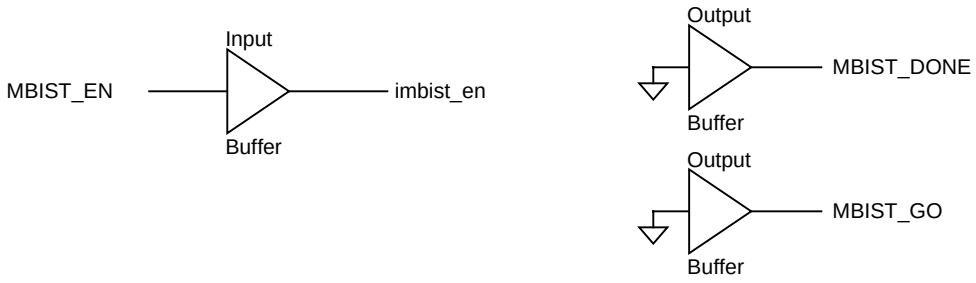


Figure 10-13 Outline Block Diagram

(2) Circuit description

In the design of a circuit, specify the dedicated memory BIST pins and multiplexers for shared pins in the RTL or netlist. At this time, make sure the dedicated input pins have their outputs written as “open,” and that the dedicated output pins have their inputs written as “pull-down.” Similarly, make sure the multiplexers for shared pins have their select signal written as “MBIST_EN” and their inputs on the BIST side written as “pull-down.” Figure 10-14 shows an image of a circuit description.

- When MBIST_EN, MBIST_GO, and MBIST_DONE are used as dedicated pins



- When MBIST_EN is used as a dedicated pin and MBIST_GO and MBIST_DONE are used as shared pins

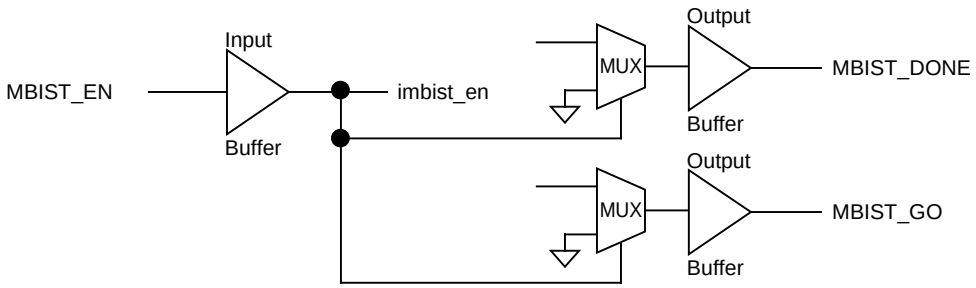


Figure 10-14 Image of a Circuit Description

(3) Memory clocks integrated into one line for the purpose of BIST

If the circuit uses multiple memory clocks and is configured so as to integrate those clocks into one line for operation in memory BIST mode, please notify Epson to that effect. In addition, provide detailed information on it in (5) and (6) below.

(4) Clocks for multi-port memory multiplexed for the purpose of BIST

If the circuit has multi-port memory, it is necessary that clocks for the respective ports be equal; otherwise, the clocks must be multiplexed for operation in memory BIST mode. If you've multiplexed these clocks, please notify Epson to that effect. In addition, provide detailed information on it in (5) and (6) below.

(5) SRAM information

Provide information on the SRAM as shown in the checksheet description examples below.

(6) Test pin information

Provide information on the test pin as shown in the checksheet description example below.

● Checksheet description example 1: Memory clocks integrated into one line (Multi port memory clocks multiplexed)

(1) Have you prepared an outline drawing of the circuit blocks? [Yes]/No

(2) Have you specified the cells for memory BIST in the circuit? [Yes]/No

(3) Have you integrated memory clocks into one line for the purpose of BIST? [Yes]/No
(However, this is not an essential requirement.)

(4) Have you multiplexed clocks for multi-port memory for the purpose of BIST? [Yes]/No

(5) SRAM information

Memory Type	Instance Name of Memory	Net Name of Memory Clock*
1 port 1024 words x 8 bits	top.sys1.sram1	sysclk1
1 port 1024 words x 8 bits	top.sys1.sram2	sysclk1
1 port 1024 words x 8 bits	top.sys2.sram3	sysclk2
1 port 1024 words x 8 bits	top.sys2.sram4	sysclk2
Dual-port 512 words x 16 bits	top.sys3.sram5	sysclk3a、sysclk3b

*: If you've integrated clocks into one line or multiplexed clocks for the purpose of BIST, clearly specify the BIST mode.

(6) Test pin information

Pin Name	External Pin Name, etc.
BIST_CLK	Shared-input-pin name: TESTCLK Clock net name: sysclk1; Instance name of module: sys1 Clock net name: sysclk2; Instance name of module: sys2 Clock net name: sysclk3a and sysclk3b; Instance name of module: sys3 Mode setting: TEST = 1, MBIST_EN = 1, with clocks integrated into one and multiplexed
MBIST_EN	Dedicated input pin name: MBIST_ENABLE Net name: imbist_en
MBIST_GO	Shared output pin name: SIGNAL1 Instance name of MUX: go_mux
MBIST_DONE	Shared output pin name: SIGNAL2 Instance name of MUX: done_mux

● Checksheet description example 2: Memory clocks not integrated into one (Multi port memory clocks multiplexed)

(1) Have you prepared an outline drawing of the circuit blocks? [Yes]/No

(2) Have you specified the cells for memory BIST in the circuit? [Yes]/No

(3) Have you integrated memory clocks into one line for the purpose of BIST? [Yes]/No
(However, this is not an essential requirement.)

(4) Have you multiplexed clocks for multi-port memory for the purpose of BIST? [Yes]/No

(5) SRAM information

Memory Type	Instance Name of Memory	Net Name of Memory Clock*
1 port 1024 words x 8 bits	top.sys1.sram1	sysclk1
1 port 1024 words x 8 bits	top.sys1.sram2	sysclk1
1 port 1024 words x 8 bits	top.sys2.sram3	sysclk2
1 port 1024 words x 8 bits	top.sys2.sram4	sysclk2
Dual-port 512 words x 16 bits	top.sys3.sram5	sysclk3a、sysclk3b

*: If you've integrated clocks into one line or multiplexed clocks for the purpose of BIST, clearly specify the BIST mode.

(6) Test-pin information

Pin Name	External Pin Name, etc.
BIST_CLK	Shared input pin name: SYSCLK1 Clock net name: sysclk1; Instance name of module: sys1 Mode setting: None
	Shared input pin name: SYSCLK2 Clock net name: sysclk2; Instance name of module: sys2 Mode setting: None
	Shared input pin name: SYSCLK3 Clock net name: sysclk3a, sysclk3b; Instance name of module: sys3 Mode setting: MBIST_EN = 1, with clocks multiplexed
MBIST_EN	Dedicated input pin name: MBIST_ENABLE Net name: imbist_en
MBIST_GO	Shared input pin name: SIGNAL1 Instance name of MUX: go_mux1
	Shared input pin name: SIGNAL2 Instance name of MUX: go_mux2
	Shared input pin name: SIGNAL3 Instance name of MUX: go_mux3
MBIST_DONE	Shared input pin name: SIGNAL4 Instance name of MUX: done_mux1
	Shared input pin name: SIGNAL5 Instance name of MUX: done_mux2
	Shared input pin name: SIGNAL6 Instance name of MUX: done_mux3

10.6 Function Cell Test Circuits

If function cells are used, a huge number of test patterns and a large amount of time are needed to confirm the operation of the entire circuit (including the customer's circuit). For this reason, customers are requested, as in the case of RAM, to design a test circuit so as to enable the function cells and the user circuit to be operated singly for the confirmation of circuit operation.

Please take the notes described below into consideration in the design of a test circuit. For more information, consult the Function Cell Design Guide.

10.6.1 Test Circuit Structures

(1) Add a test circuit so as to enable the function cells to be individually separated from the user circuit and measurements to be taken for each block, with the pins of the function cells led out to the IC's external pins.

(2) Even when inputs for the function cells are fixed to V_{SS} or V_{DD}, install a test circuit to allow inputs for testing.

(3) Even when the output pins of the function cells are unused, install a test circuit to enable all outputs of the function cells to be observed from the IC's external pins.

(4) Do not combine the multiple output or input pins of the function cells for use as a single test shared pin.

(5) Do not use a sequential circuit in the test circuit you are generating to test the function cells.

(6) Do not invert the input signals from the test input pins before they are supplied to the function cells. Nor can the output signals of the function cells be inverted before they are forwarded to the test output pins.

(7) If the input and output pins of the function cells are led out directly, as with the IC's pins, there is no need to install a test circuit.

10.6.2 Test Patterns

Broadly classified, the following are the three types of test patterns:

1) Test patterns for testing only the user circuit

2) Test patterns for testing the entire circuit

3) Test patterns for testing only the function cells

Of these test patterns, customers are requested to generate test patterns 1) and 2). It is not necessary for customers to generate test patterns 3). Existing test patterns at Epson will be used.

Note, however, that the function cell test patterns (Epson's test patterns) cannot be used by customers.

10.6.3 Test Circuit Data

This information is required when the function cells are tested during simulation and shipping inspection. Please provide Epson with the following information on your test circuit.

(1) Clearly specify which pins of the IC are connected to which function cell pins in test mode.

(2) If the test circuit is configured so as to enable multiple function cells to be tested on a single test pin, clearly specify the relationship between test modes and the function cell names selected.

(3) In particular, if multiple instances of the same function cell are used, assign the function cell names in the drawing serial numbers and clearly specify which function cells are connected to the test pin.

(4) Clearly specify how the circuit can be switched to test mode.

If function cells are used in your circuit, be sure to consult the Function Cell Design Guide in addition to this manual.

10.7 Scan Design

To prevent defective products from becoming mixed into the market, devices must be tested using test patterns that activate logic for testing. For large designs, however, this test method requires a huge number of man-hours. Scan design provides one means of solving this problem. When generating test patterns with increased fault detection rates, it is helpful to base design on certain rules and the execution of ATPG (Auto Test Pattern Generation).

This chapter describes the design rules to be followed in order to make the circuit suitable for scan testing (hereinafter referred to as “scan”) and to use the ATPG service from Epson. Because the implementation of scan is greatly affected by the design configuration, it is important to follow these rules from the beginning in the design of a circuit. If any design contrary to these rules is included, the purposes of ATPG may be impaired and customers may therefore be unable to use this service.

10.7.1 About the Scan Circuit

All registers (D-FFs, JK-FFs) included in your design are converted to scan type registers in order to create a scan path (full scan design). Then, through the use of this design, ATPG (Auto Test Pattern Generation) is executed. This helps to generate test patterns featuring a high fault detection rate.

Note: The test patterns generated by ATPG are not intended for the verification of design specifications. Transparent latches are not scanned.

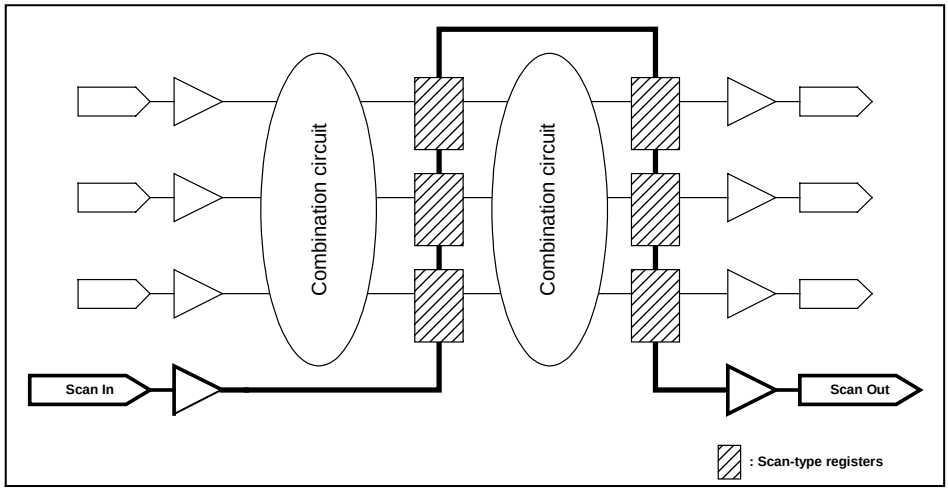
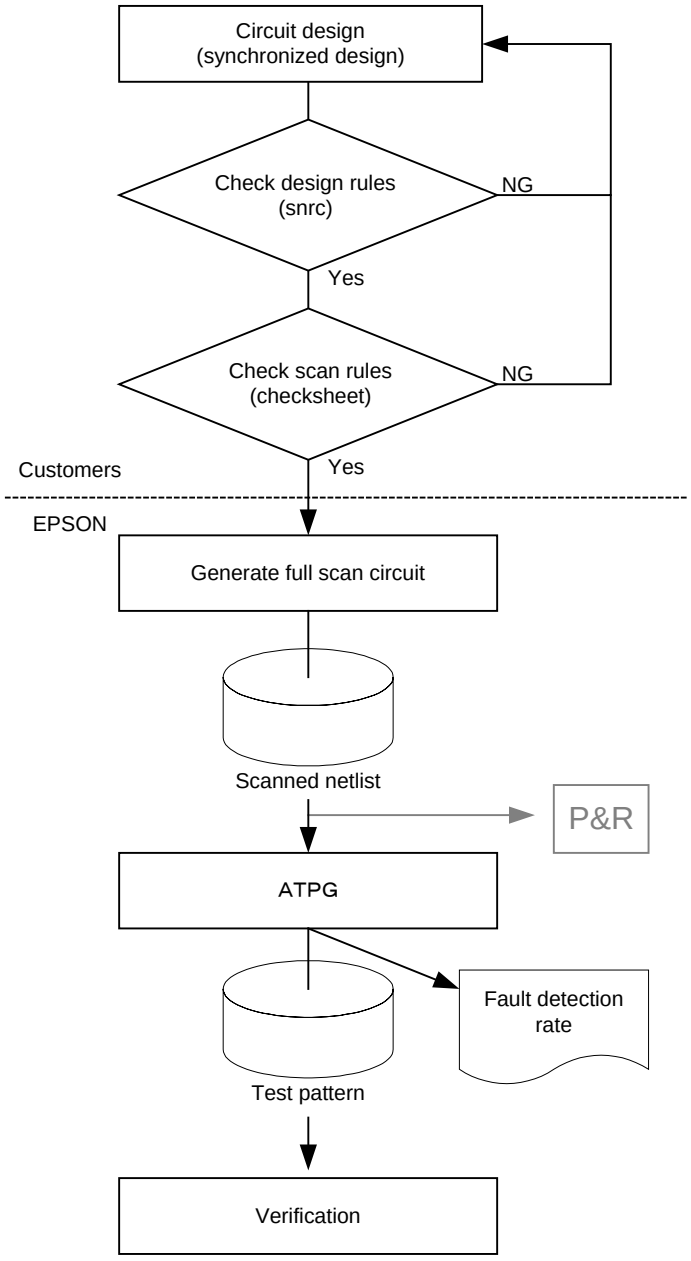


Figure 10-15 Example of a Scan Circuit

10.7.2 Scan Design Flow

The following shows the design flow in cases in which the circuit is scanned and ATPG is executed at Epson. To scan the circuit or execute ATPG yourself, consult the sales division of Epson.



Synchronized design is recommended. Unless scan rules are taken into consideration, the scan service cannot be used.

The basic elements of ASIC design are checked using the design rule checker "snrc," which is included with the Epson design kit EPITS.

Make sure the design rules for scan described in the next section are observed in your design.

The following must be provided to Epson:

- Gate-level netlist
- Scan design checksheet (attached at the end of this chapter)
- Clock Tree Synthesis checksheet (Refer to Section 9.3, "Clock Tree Synthesis.")

If a previously scan circuit is to be interfaced to Epson, consult Epson in advance.

Scan is implemented and ATPG is executed.

The generated netlists and test patterns are verified. The test patterns that have been confirmed as being good are used in shipping inspection.

Figure 10-16 Scan Design Flow

10.7.3 Design Rules

The following section describes the design rules to be followed in order for the scan service to be used. If the desired fault detection rate is 90% or higher, make sure all of the contents described herein are reflected in your design. In addition, when interfacing your design to Epson, make sure it is accompanied by the **Scan Design Checksheet** attached at the end of this chapter.

a. Scan external pins

For the circuit to be scanned, all of the external pins described below are required.

- Scan enable input pin (SCANEN) [Dedicated pin]

  This dedicated external input pin selects between the ordinary data path (parallel operation) and the scan path (shift operation). It cannot be shared with ordinary functions or other mode functions. Provide an input cell and external pin in the design for use as a dedicated external pin.

- Scan data input pins [Shareable]

  These external input pins are used to set data in the scan registers that have been incorporated into the design by scan. There must be several instances of these input pins corresponding to the number of scan registers. Prepare one input pin for every 300 to 500 scan registers. As many of these input pins as the number of scan-data output pins are required.

  These pins may be shared with external input pins that are used in normal operation. However, clock pins, asynchronous set/reset pins, and analog signal input pins cannot be used. Note that if any pin is shared, Fan-Out in its net increases. Avoid sharing pins for critical paths.

  The scan data input pins are connected to the external pins at Epson during scan of the design. Please specify the external input pin names that can be used for this connection. Unless specified, pin assignments will be made by Epson.

- Scan data output pins [Shareable]

  These external output pins are used to output the observation data from the scan registers that have been incorporated into the design by scan. There must be several instances of these output pins corresponding to the number of scan registers. Prepare one output pin for every 300 to 500 scan registers. As many of these output pins as the number of scan-data input pins are required.

  These pins may be shared with external output pins that are used in normal operation (two-state output pins are recommended). However, analog signal output pins cannot be used. Note that if any pin is shared, the number of cell stages in its net increases. Avoid sharing pins for critical paths.

  The scan-data output pins are connected to the external pins at Epson when the design is scanned. Please specify the external output-pin names that can be used for this connection. Unless specified, pin assignments will be made by Epson.

- Scan clock input pin [Same as an ordinary clock or dedicated pin]

  This clock input pin is used in the test patterns generated by ATPG. Because Epson scan cells employ the MUX scan type, this clock input pin must generally be the same system clock used in normal operation. However, if an internally generated clock exists, a dedicated clock pin for scan use may be required. For details, refer to paragraph b, “Clock design,” discussed later in this section.

- ATPG enable input pin (ATPGEN) [Dedicated pin]

  This external input pin activates ATPG run mode. If any design exists that requires that the state be fixed, or for the outputs of blocks (including those that become black boxes during simulation), functional macros, and RAM cells for which the internal logic becomes unstable, this pin must be used to fix (determine) the values. Unless this procedure is used, the fault detection rate decreases considerably.

  Prepare this external input pin as a dedicated pin.

b. Clock design

For the circuit to be scanned, clock design is very important. If the clock design is complicated, not only is the fault detection rate reduced, but the generated test pattern also becomes unstable. In such a case, the intended purposes of scan and ATPG cannot be achieved. Therefore, we basically recommend synchronized design. Follow the rules described below in the design of a clock.

Keep in mind, as well, that the clock lines require optimization by CTS (Clock Tree Synthesis). For details, refer to Section 9.3, "Clock Tree Synthesis."

- **Directly controllable structure from the outside** [Essential]

  The scan clock must propagate from an external input pin to the internal registers without being distorted in the clock waveform. Although it does not matter whether an internally generated clock is present during normal operation, there must logically be no internally generated clocks in ATPG run mode. Examples are shown in Figures 10-17 through 10-20.

  § Ideal clock

  Shown in Figure 10-17 is an example of an ideal clock design. If the circuit is designed from the beginning in such a way that the clock for all registers is supplied from an external input pin as in this case, processing the clock lines by CTS makes it unnecessary to correct them for purposes of scan design. Because clock line corrections affect the timing of the entire circuit, it is important to take scan design into consideration from the beginning of your design work.

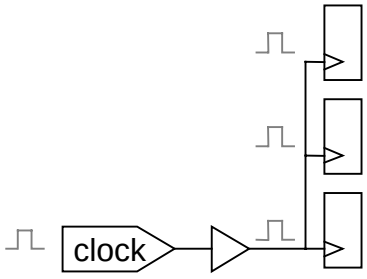


Figure 10-17 Ideal Clock

  § Processing of internally generated clocks 1

  If an internally generated clock is used, insert a circuit that bypasses the clock generating part (see Figure 10-18) and employ a design that applies CTS processing to ATPG run mode. However, employment of this processing requires caution, as MUX cells are added to the clock lines in that processing, which may make it difficult to adjust the timing with the clocks used for other circuit blocks.

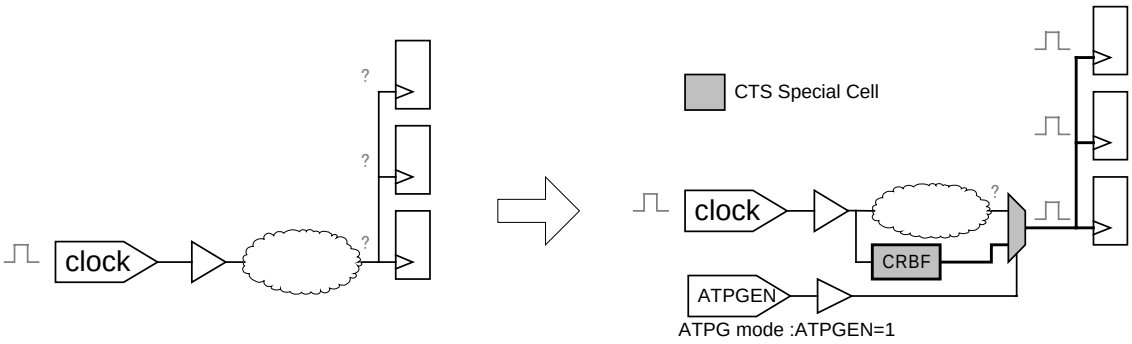


Figure 10-18 Processing of Internally Generated Clocks

§ Processing of internally generated clocks 2 (treatment of clock gating)

To avoid adding cells to the clock line for an internally generated clock, there is a method for controlling the enable line by which the clock signal is gated. An example is shown in Figure 10-19. Adoption of this method eliminates the need for MUX cells placed in the clock line as in Figure 10-18, and therefore helps create a design with relatively small clock skew.

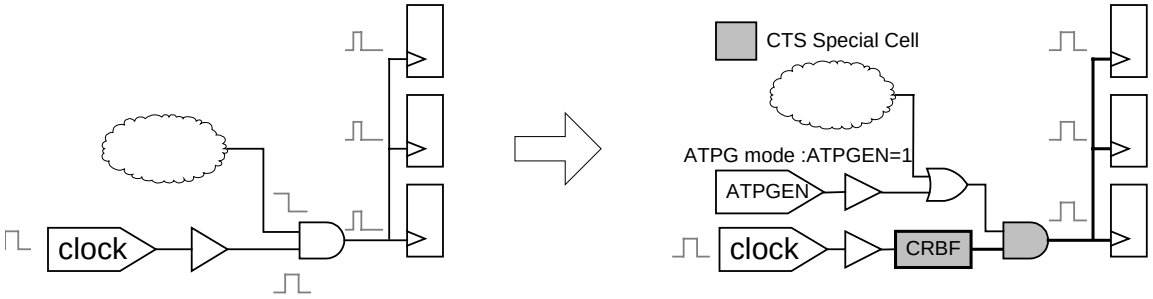


Figure 10-19 Treatment of Clock Gating

§ Relationship between multiple clock groups

For a design with multiple clock blocks including internally generated clocks, the usable treatment method may be limited, depending on the relationship between those clock blocks. Unless the circuit blocks using different clocks are physically interconnected, there will be no problems. However, caution must be exercised if for reasons of design specification they comprise either a false path (although physically connected, there is no logical communication during normal operation, or timing is not taken into consideration during logic synthesis) or a multi-cycle path (asynchronously communicating, with several latch misses tolerated).

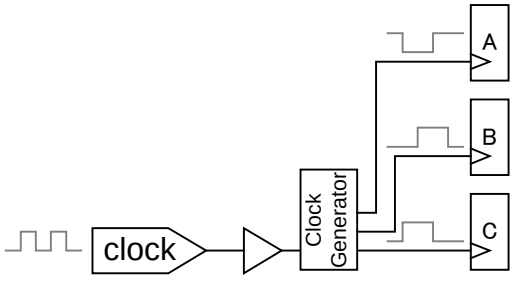


Figure 10-20 (a) Example with Multiple Internally Generated Clocks

Shown in Figure 10-20 (b) is an example of a corrective measure that can be taken in cases in which blocks A, B, and C are not physically interconnected. Because there are no physical connections, clocks can be processed collectively without causing a timing problem. If clock skews in each group are resolved by CTS, timing during ATPG run will be stabilized.

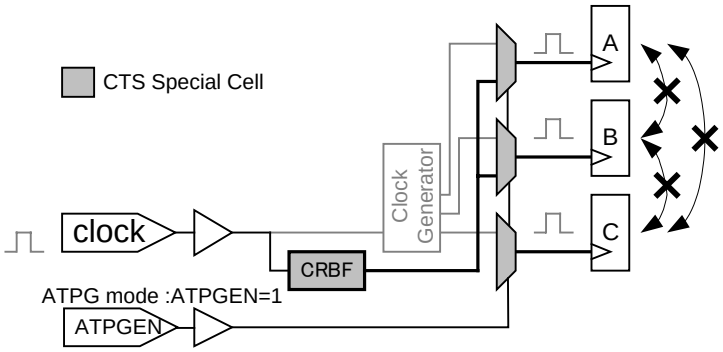


Figure 10-20 (b) Example of a Corrective Measure for Multiple Internally Generated Clocks 1 (When Blocks are Not Interconnected)

* Assumed in this example is a method that helps to efficiently create the scan chain by applying CTS processing to three clocks collectively.

However, if the blocks are physically connected, though there may be no problems from a specification perspective, corrective measures for ATPG must be taken. Figure 10-20 (c) shows an example of treatment in such a case. Because ATPG generates test patterns at random, they may cause an operation in which signals are communicated via a false path that is nonexistent in the specification. In such a case, the timings associated with the data paths between blocks A, B, and C cannot be guaranteed. Therefore, to ensure that the timings will be controlled for each internally generated clock, bypass these clocks on a one for one basis to external pins. In addition, *we recommend the use of dedicated pins* for these bypass clock pins. If the use of shared pins is unavoidable, the clock signals entering from those shared pins must be gated to prevent them from propagating to other than the registers (see Figure 10-20 (d)). In such a case, because the values of those nets are fixed, the fault-detection rate decreases.

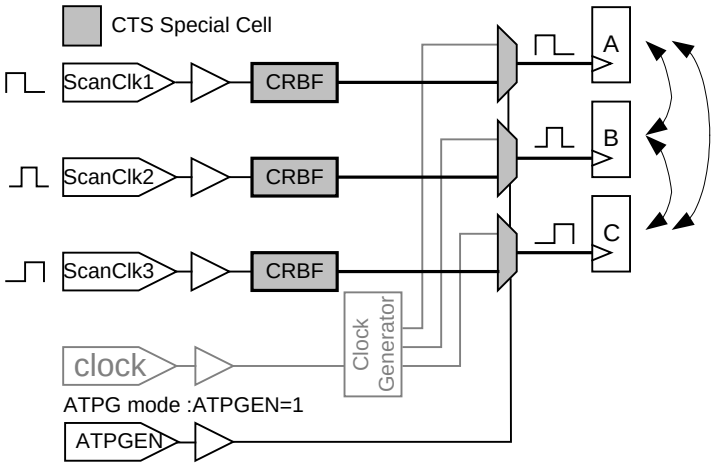


Figure 10-20 (c) Example of a Corrective Measure for Multiple Internally Generated Clocks 2 (When Blocks are Interconnected)

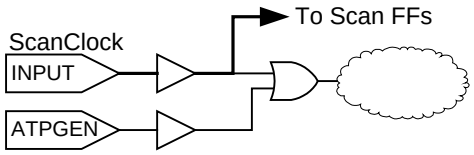


Figure 10-20 (d) Example of Scan-Clock Processing Using Shared Pins

- **As few clock lines as possible** [Recommended]

  If multiple clocks exist as in the above case, the amount of work to be performed by customers will increase, such as due to the need to change or add a design or an increase in the number of timing reverification items. Furthermore, the presence of multiple clocks may cause the length of test patterns to increase or the fault detection rate to drop. Reduce the number of clock blocks as much as possible in design. This should help increase the efficiency of work when testing is conducted later.

- **Minimized coexistence of rising and falling edges of a clock** [Recommended]

  If both rising and falling edges are used in each clock, the efficiency of scan operation and ATPG run may decrease. In some cases, the fault detection rate may drop. We recommend that scan clocks be designed using only one edge as much as possible.

- **Completely separated scan clock signals and data signals** [Recommended]

  Make sure the scan clock signals and data signals are completely separated. If the scan-clock signals affect the data lines, clock signals and data signals cannot be controlled independently of each other, and faults therefore cannot be detected.

c. Asynchronous set/reset signals of registers [Essential]

A circuit is recommended in which the asynchronous set/reset signals for the flip-flops and transparent latch cells can all be controlled directly from the outside. When asynchronous set/reset signals internally generated in the design are used, take the following into consideration:

- The signals cannot be asserted (= made active) for at least the period for which scanning remains enabled.
- When internally generated asynchronous set/reset signals are used, make sure they are fed directly from the flip-flop outputs without being routed via combinational circuits, to ensure that minimum pulses will not occur. If signals routed via combinational circuits are used, take the appropriate corrective measure by, for example, using gray code.

* Unless such a corrective measure is taken, problems such as reduced fault detection rates or unstable test patterns may occur.

d. Handling of transparent latches [Recommended]

Transparent latches are not converted into scan cells. Avoid using transparent latches as much as possible, as they are detrimental to improving the fault detection rate.

When transparent latches are used, take the following into consideration:

- For the clock signals, take corrective measures similar to those discussed in paragraph b, “Clock design.”
- Make sure the off-state levels of the transparent latches match those of other registers connected to the same clock line.

  Example: Through at the Low level when the FF is for a rise operation (Return To Zero), or through at the High level when the FF is for a fall operation (Return To One)

  However, if the scan clock is active on either edge or multiple instances of the scan clock exist, no improvements can be expected, depending on the design configuration. In such a case, take the corrective measure described below.
- If the above two points cannot be taken into consideration in your design, make sure the latches are fixed to the through state in ATPG run mode. At this time, care must be taken to avoid creating a feedback loop.

* Unless these corrective measures are taken, problems such as reduced fault-detection rates or unstable test patterns may occur.

e. Unusable cells or design [Essential]

In scan design, use of the cells specified below is inhibited.

<Cells the use of which is inhibited>

- RS latch cells
- Flip-flops with asynchronous set/reset functions
- Multi-bit flip-flop cells
- Scan type flip-flops

<Circuits the use of which is inhibited>

- Combinational feedback loops (including those routed via external bi-directional pins)
- Differentiation circuits (pulse generators)
- Self reset circuits
- Sequentially controlled ATPG mode (Use the ATPG enable input pin for control.)

* Unless these corrective measures are taken, problems such as reduced fault detection rates or unstable test patterns may occur.

f. When using functional macros or RAM cells [Recommended]

Because in ATPG functional macros and RAM cells are handled as black boxes, it is impossible to observe the stages preceding the macros and control those following the macros. Therefore, the fault detection rate is reduced considerably. To counteract this, we recommend inserting scanable flip-flops in locations immediately preceding and following the macro cells. This will bring about a significant improvement when the circuit is tested later (Figure 10-21 (a)). If this is impossible from a specification standpoint, add a mode in which the macros are bypassed and configure a circuit by which the output level can be fixed (Figure 10-21 (b)).

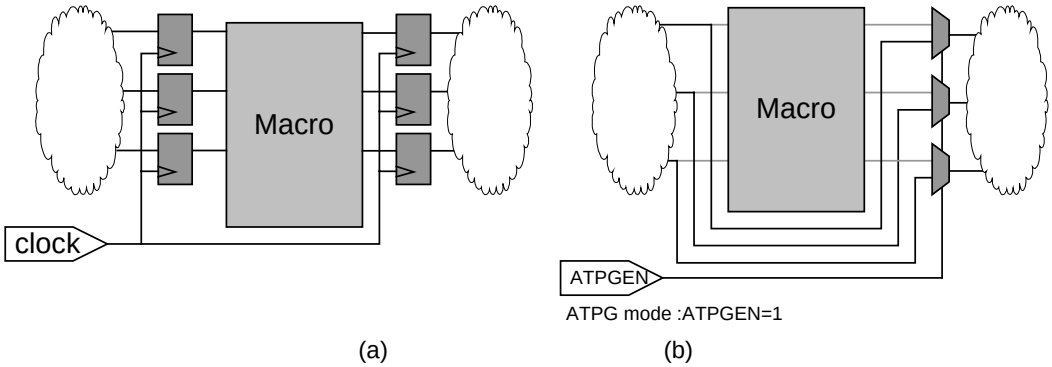


Figure 10-21 Example of Macro Cell Processing

g. Internal bus [Recommended]

Do not use bus circuits comprised of internal 3-state cells. Rather, we recommend that the circuit be designed using selector logic. When using said bus circuits, make sure they are fixed in such a way that the bus lines are not switched over and only one line is activated in ATPG run mode. (If bus circuits are used, the fault detection rate decreases, as such circuits have fixed values.)

h. External cells with various controls [Essential]

Some types of external input and external bi-directional cells available in the S1X60000 series come equipped with various control pins. These pins must be fixed using the ATPG enable input pin. Follow the procedure described below to process these pins.

- Gating signal (C pin)

  Fix this pin to the through state using the ATPG enable input pin (ATPGEN). (C = 1 when ATPGEN = active)

i. Other

- Approximately 7 days are required for scan work (scan insertion to verification) at Epson after netlists created in accordance with the design rules are received.
- In scan design, optimization by CTS is essential. Please make sure the **Clock Tree Synthesis Checksheet** attached in **Section 9.3, "Clock Tree Synthesis,"** is included with the netlists presented to Epson.

Scan Design Checksheet (1/2)

This checksheet includes the contents we would like you to confirm before using scan or ATPG services from Epson. Fill out this checksheet and present it to Epson. Without this checksheet, scan and ATPG services cannot be used.

Information on scan design and the results of the design check are provided below.

Date filled in: _____ (month) _____ (day) 200_____

Company name: _____

Your name: _____

- **Design information**
  - Top block name: _____
  - Desired fault-detection rate: _____%

- **Pin information**
  - ATPG enable pin names and active edges (rise/fall)

    Pin name 1: _____ (Rise/Fall)
    Pin name 2: _____ (Rise/Fall)
    Pin name 3: _____ (Rise/Fall)

  - Scan enable pin names and active levels (High/Low)

    Pin name 1: _____ (High/Low)
    Pin name 2: _____ (High/Low)
    Pin name 3: _____ (High/Low)

  - Scan clock input pin names and active levels (High/Low)

    Pin name 1: _____ (High/Low)
    Pin name 2: _____ (High/Low)
    Pin name 3: _____ (High/Low)

  - Scan data input pin name

    Pin name: _____

  - Scan data output pin name

    Pin name: _____

  - Asynchronous set/reset pin names and active levels (High/Low)

    Pin name 1: _____ (High/Low)
    Pin name 2: _____ (High/Low)
    Pin name 3: _____ (High/Low)

Scan Design Checksheet (2/2)

● **Check items (Mark the applicable items with a check.)**

- ☐ The scan clock pins have been treated in accordance with the design rules described in Section 10.7.3, paragraph b.
- ☐ Asynchronous set/reset signals of registers have been treated in accordance with the design rules described in Section 10.7.3, paragraph c.
- Transparent latches (Select one of the following.)
  - ☐ Not used
  - ☐ Treated in accordance with Section 10.7.3, paragraph d
  - ☐ Not treated in accordance with Section 10.7.3, paragraph d.
    A reduction in the fault-detection rate is acknowledged.
  - ☐ Other: _____
- ☐ Cells or circuits the use of which is inhibited as described in Section 10.7.3, paragraph e, do not exist.
- Functional macros or RAM cells (Select one of the following.)
  - ☐ Not used
  - ☐ Treated in accordance with Section 10.7.3, paragraph f
  - ☐ Not treated in accordance with Section 10.7.3, paragraph f.
    A reduction in the fault detection rate is acknowledged.
  - ☐ Other: _____
- Internal 3-state bus (Select one of the following.)
  - ☐ Not used
  - ☐ Treated in accordance with Section 10.7.3, paragraph g
  - ☐ Not treated in accordance with Section 10.7.3, paragraph g.
    A reduction in the fault-detection rate is acknowledged.
  - ☐ Other: _____
- External cells with various control pins (Select one of the following.)
  - ☐ Not used
  - ☐ Treated in accordance with Section 10.7.3, paragraph h
  - ☐ Not treated in accordance with Section 10.7.3, paragraph h.
    A reduction in the fault detection rate is acknowledged.
  - ☐ Other: _____
- Other

  _____

  _____

  _____

10.8 Boundary Scan Design

A boundary scan (JTAG) insertion service is available from Epson. When this service is used, an IEEE1149.1 compliant boundary scan circuit and a control circuit (TAP controller) are inserted in the periphery of the logic circuit. At the same time, BSDL files that contain information on those circuits are presented to customers. Because the inserted boundary scan function patterns are created by Epson, it is not necessary for customers to create patterns for the boundary scan circuit.

10.8.1 Boundary Scan Design Flow

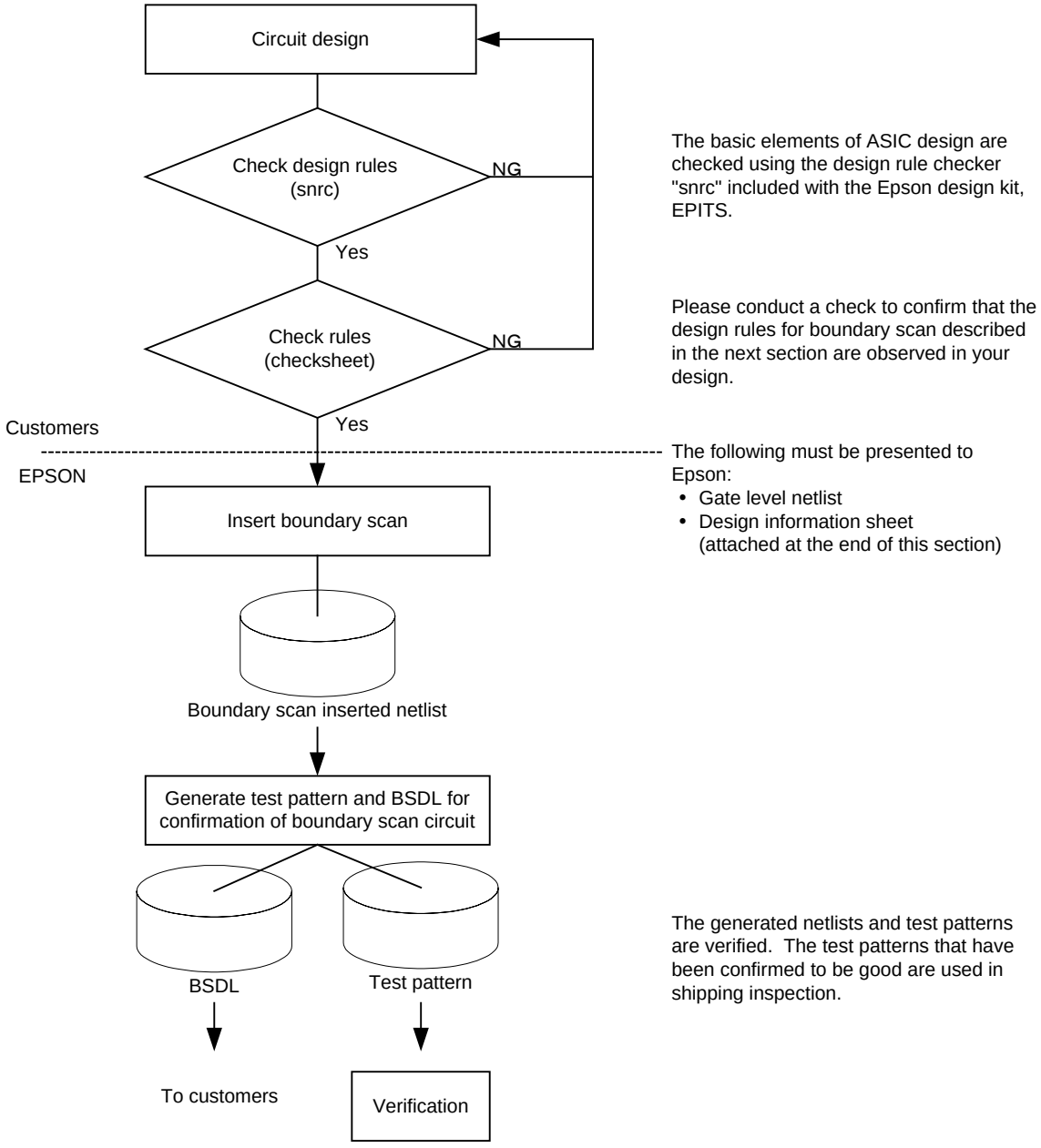


Figure 10-22 Boundary Scan Design Flow

10.8.2 Instructions

The JTAG instructions specified below are supported.

Table 10-4 Supported Instruction Codes

Instruction	Code
SAMPLE/PRELOAD	0...10
BYPASS	1...11
EXTEST	0...00
CLAMP	Selectable as desired(*1)
HighZ	Selectable as desired(*1)
IDCODE	0...01

Note *1: Unless explicitly specified, Epson will select the appropriate code. No duplicate codes can be specified.
Instruction bit sizes may be selected in the range of 2 to 32 bits. Unless explicitly specified, Epson will determine the appropriate instruction size.

10.8.3 Estimating the Number of Gates

The extent of the increase in the number of gates as a result of boundary scan insertion depends on the ASIC series used and the instructions and bit sizes supported. Estimate the approximate number of gates using the information given below.

Table 10-5 Gate Count Estimation (SOG Equivalent)

Boundary Scan Block	Gate Counts
TAP controllers + miscellaneous gates	Approx. 1000 (BCs)
Input pin	When using normal cells: Approx. 30 (BC/pin) When using dedicated observation cells: Approx. 15 (BC/pin)
2-state output pin	Approx. 35 (BC/pin)
3-state output pin	Approx. 65 (BC/pin)
Bi-directional pin	Approx. 95 (BC/pin)

10.8.4 Design Rules

For the boundary scan service to be used, it is necessary that customers' logic circuits be designed in observance of the restrictions described below. Before releasing data to Epson, please be sure to confirm the circuit information using the **Boundary Scan Checksheet** attached at the end of this chapter, and to fill out and present the Design Information Sheet to Epson. Please note that if any circuit violating the restrictions exists, this service cannot be used.

a. Coexistence with DC/AC easy to test circuits inhibited

Coexistence with the easy to test circuits described in **Section 10.3, "Test Circuit Which Simplifies DC and AC Testing,"** is inhibited. To be suitable for the boundary scan service, a design cannot have DC/AC easy to test circuits inserted in it.

b. Character strings usable for external pins

Due to the rules for the BSDL file format, external pin names are subject to the following limitations:

- Only alphanumeric characters (a to z, A to Z, 0 to 9) and the underscore (_) can be used.
- The characters are not case-sensitive (for example, CLK and clk are assumed to be the same).
- The first character must always be a letter (for example, 0CLK and _CLK are not accepted).
- The underscore cannot be used in succession (for example, SYS__CLK is not accepted).
- The character string cannot end with an underscore (for example, CLK_ is not accepted).

c. Preparation of dedicated external pins

The boundary scan circuit always requires five dedicated external pins. Insert these external pins in your design in accordance with the rules described below.

- Clock (TCK)

  This is a clock pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected.

- Mode select (TMS)

  This is a mode select pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected. For this input cell, use an input cell with pull-up.

- Data input (TDI)

  This is a scan data input pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected. For this input cell, use one with pull-up.

- Data output (TDO)

  This is a scan data output pin for the boundary scan circuit. Use a 3-state output cell and confirm that its input port is tied low to GND.

- Reset (TRST)

  This is an asynchronous reset pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected. For this input cell, use one with pull-up.

```
IBC U1 ( .PAD(TCK) );                          // IBC:     Normal input cell
IBCP1 U2 ( .PAD(TMS) );                        // IBCP1: Input cell with pull-up
IBCP1 U3 ( .PAD(TDI) );
IBCP1 U4 ( .PAD(TRST) );
TB1 U5 ( .PAD(TDO), .A(1'b0), .E(1'b0) );      // TB1:     3-state output cell
```

Figure 10-23 Example of Dedicated Pin Description (Written in verilog)

d. Regarding hierarchical blocks

Make sure the hierarchical blocks in the netlist are configured as shown below. Note that, following boundary scan insertion, hierarchical blocks such as a TAP controller are added.

- Place I/O cells in the top block.
- Place other logic cells in a sub-block one layer below that as much as possible.

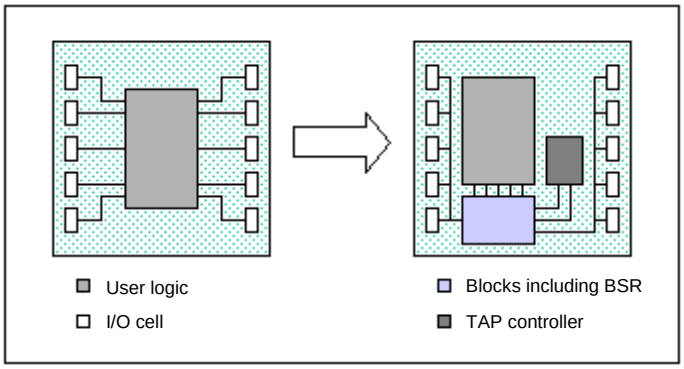


Figure 10-24 Image of a Hierarchical Block Configuration

e. Regarding I/O cell types

If the design includes one of the following types of I/O cells, the boundary scan service cannot be used:

- I/O cells with test mode
- Gated input cells
- Open drain output cells
- I/O cells with pull-up/pull-down registor

f. External pins handling analog signals

Boundary scan cells are not inserted for oscillation circuit input/output pins or external pins that handle analog signals.

g. Multibonding and multipads

If the design includes multibonding or multipads, the boundary scan service cannot be used.

Boundary Scan Checksheet

Please confirm the check items listed below before interfacing to Epson, and present the Design Information Sheet shown on the next page to Epson. Please note that if any circuit violating these check items exists or any information is omitted, the boundary scan service cannot be used.

Please confirm the following items before presenting netlists to Epson:

(a) The supported range of instructions complies with Table 10-4.

(b) The circuits described in Section 10.3, “Test Circuit Which Simplifies DC and AC Testing,” cannot coexist.

(c) Confirm that the external pin names comply with Section 10.8.4, paragraph b “Character strings usable for external pins.”

(d) Regarding dedicated pins

  (i) Conduct a check to confirm that five dedicated pins already exist in the netlist.

  (ii) For the TMS, TDI, and TRST equivalent pins, use input cells with pull-ups.

  (iii) For the TDO equivalent pin, use a 3-state output cell.

  (iv) Conduct a check to confirm that the dedicated pins are not shared with any other functions.

(e) Place I/O cells in the top layer.

(f) Do not use the I/O cells listed in Section 10.8.4, paragraph e.

(g) Boundary scan cells cannot be inserted for oscillation circuit input/output pins or external pins that handle analog signals.

(h) Conduct a check to confirm that multibonding and multipads are not used.

Design Information Sheet

(Fill out this sheet and present it to Epson by the time the design is released.)

Information on boundary scan design is provided below.

Date filled in: _____ (month) _____ (day) 200____

Company name: _____

Your name: _____

● **Design information**

➢ Top block name: _____

1. Desired instructions (Select the desired instructions.)
   - ■Essential instructions → Codes comply with Table 10-4.
   - □CLAMP instructions → Your desired code _____ (*1)
   - □HIGHZ instructions → Your desired code _____ (*1)
   - □IDCODE instructions Codes comply with Table 10-4.
2. Instruction bit size (Select the desired size.)
   - □Not specified → Determined by Epson
   - □Specified → Bit size _____ bits(*2)
3. Selection of boundary scan cells

   To choose the boundary scan cells to be inserted, supply the information specified below. Unless explicitly specified, the following will be applied at Epson:

   - Dedicated observation cells may be used, if necessary, for the system clock or asynchronous reset bits.
   - Boundary scan cells will not be inserted for input and output pins handling analog signals.

♦ External pin names for which dedicated observation cells are used

_____

♦ External pin names for which boundary scan cells are not to be inserted

_____

♦ Other

_____

♦ Dedicated pin information (Enter the pin names corresponding to each pin.)

TCK: _____ TMS: _____ TDI: _____ TDO: _____ TRST: _____

♦ User circuit information

System clock name: _____

Asynchronous reset signal name: _____

Top block name: _____

Sub block name(*3): _____

Notes *1 Do not select duplicate codes for any instruction. Unless explicitly specified, codes will be assigned by Epson. In addition, make sure the bit size matches that in Item 2, "Instruction bit size."

*2 Bit sizes can be specified in the range of 2 to 32 bits.

*3 Enter all sub blocks that exist immediately below the top block. If any buffers or delay elements inserted for delay adjustment or the like exist in the top block, enter their instance names.

Chapter 11 Test Pattern Generation

The test patterns received from customers to confirm IC specifications are not subject to many restrictions. Basically, any test patterns may be accepted when completed by a reasonable deadline and can be simulated individually with the IC alone. (For details, contact Epson.) For the shipping test, however, some restrictions are imposed depending on tester capability. Test patterns for the shipping test will be created from those received from customers to confirm IC specifications by modifying the patterns at Epson. Therefore, please consider the following restrictions when creating test patterns to confirm IC specifications.

11.1 Testability Consideration

Because test patterns are used for the shipping inspection of a product, they must be generated so as to enable the entire internal circuit of the LSI to be tested. If the LSI's internal circuit contains any untested part, there is a possibility of a defective product being shipped, as that part of the product cannot be tested during the shipping inspection.

Generally speaking, the entire internal circuit of the LSI cannot be tested easily. Therefore, it is important that the testability of the LSI be taken into consideration from the beginning of circuit design.

By inserting Epson-recommended test circuits in your design, the DC testing and various other conditions required for test patterns can be set easily. For details, refer to Section 10.3, "Test Circuit Which Simplifies DC and AC Testing," in Chapter 10.

11.2 Usable Input Waveforms

Test patterns are normally comprised of logic 0s and 1s. However, when circuit operation is simulated or the circuit is tested using an LSI tester, the input waveform can have a delay inserted or pulses generated in it. The following two types of waveforms can be used in the creation of test patterns.

- NRZ (Non Return to Zero)

  Normally used for signals other than the clock. This type of waveform can change state once per test period and can be given a delay.

- RZ (Return to Zero)

  Use this for clock signals and the like. Because this type of waveform can generate a positive or negative pulse within a test period, it aids in the efficient creation of clock signals. It can be given a delay, as with NRZ.

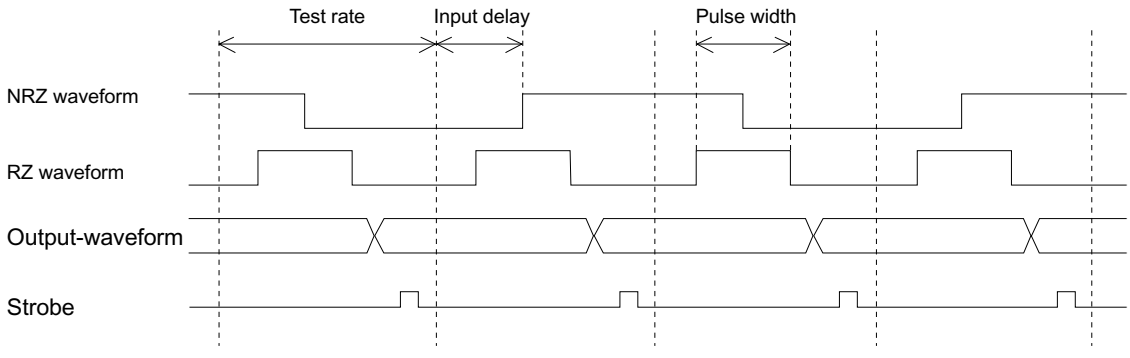


Figure 11-1 Limitations on Timing Settings

11.3 Constraints on Test Patterns

This chapter describes the restrictions on test patterns for the shipping test.

11.3.1 Test Rate and Event Counts

The following shows the test rate and event counts.

Test rate	: 100 ns or more, in 1 ns increments (typ.: 200 ns)
Number of events per test pattern	: Up to 256K events
Number of test patterns	: Up to 30 patterns
Total number of events in test patterns	: Up to 1M events

11.3.2 Input Delay

The following shows the restrictions related to input delays.

(a) Range of input delays

The input delay must be given in the range shown below. For the constraints on strobe points, refer to Section 11.3.5, “Strobes.”

$0 \text{ ns} \leq \text{input delay value} < \text{strobe point}$

(b) Phase difference in input delay

If the input delay requires a phase difference, add a difference of 3 ns or more.

(c) Types of input delays

There may be up to 8 types of input delays in one test pattern. 0 ns delays are counted as one type. Input delays with different waveforms (RZ or NRZ) or pulse widths must also be counted as being different even when their delay values are the same.

11.3.3 Pulse Width

The pulse width in an RZ waveform must be 15 ns or more.

11.3.4 Input Waveform Format

Input waveforms can take on the values 0, 1, P, or N. The values P and N represent pulse inputs in an RZ waveform. Furthermore, the values P and N can only be defined in a combination of (0, P) or (1, N) for the same pin in one test pattern. No other combinations can be used.

For bi-directional pins, an RZ waveform can be applied only when they do not have an output state in one test pattern.

11.3.5 Strobes

The strobe related constraints are as follows:

(a) Only one type of strobe can be defined in each test pattern.

(b) The minimum value of the strobe must be such that in all events, at least 30 ns elapses after all output signals have changed state pursuant to the applied input signal.

(c) The maximum value of the strobe must be smaller than the value of test rate – 15 ns.

(d) Define the strobe in 1 ns units.

11.4 Notes Regarding DC Testing

Test patterns are used not only for function testing, but also for DC testing in which output voltages and the like are measured. Make sure the following items of DC testing can be performed when creating test patterns. However, the test patterns described in this chapter need not be prepared when adopting those shown in Chapter 10, "Circuit Design that Takes Testability into Account."

DC testing is conducted in order to verify the DC parameters of the LSI. Measurements for DC testing are taken at the end of a measurement event. For this reason, the measured pins cannot have their state changed in accordance with the strobe position in the measurement event.

The following items of DC parameters are measured:

(a) Output characteristic test (V_{OH}, V_{OL})

The current drive capability of the output buffer is measured. The measured pin is driven to an output level at which measurement can be conducted, and the value of the voltage drop that occurs when the designated current load is applied to the pin is measured.

For the output-characteristic test to be performed, the test pattern must contain all possible states in which the measured pins can operate. Furthermore, those states must be sufficiently stable that they will not change even when the test rate is infinitely extended in the measurement event.

(b) Quiescent current test (I_{DDS})

The quiescent current is the leakage current that flows in the power supplies of the LSI when its inputs are in a steady state. Because the amount of this current is generally very small, it must be measured while no currents other than the leakage current are flowing. To meet this requirement, all of the conditions listed below must be satisfied. Note also that the test pattern must contain at least two points of events in which the quiescent current can be measured.

(1) All of the input pins shall be in a steady state.

(2) A High or Low level signal shall be applied to or output from the bi-directional pins.

(3) No oscillating or other operating parts shall exist in the circuit.

(4) The internal 3-state buffer (internal bus) shall not be left floating or have no data or signal contention.

(5) The RAM, ROM, and megacells shall not be in a current flowing state.

(6) A High level signal shall be applied to the input pins with pull-up resistors.

(7) A High level signal shall be applied to or output from the bi-directional pins with pull-up resistors.

(8) The bi-directional pins with pull-down resistors shall be in input mode or outputting a Low-level signal.

(c) Input current test

Measurements are taken of the inputs for the input buffers. The items measured in this test are the input leakage current and the pull-up/pull-down currents.

Measurements in this test are performed by applying V_{DD} or V_{SS} level voltage to the measured pin, and then measuring the amount of current flowing in the pin. This

means that a High or Low level voltage is applied to the measured pin during measurement. For example, if a V_{DD} level (High level) voltage is applied to the measured pin while input for it is held Low, the measured pin changes state from Low to High, causing the LSI to perform an unintended operation.

For the input-current test, in an event in which input for the measured pin is held High in the test pattern, measurements must be taken by applying a V_{DD} level voltage to the measured pin, and in an event in which input for the measured pin is held Low, measurement must be taken by applying a V_{SS} level voltage to the measured pin. Therefore, an input current test cannot be conducted unless the test pattern includes these states for the measured pin.

The input current test is further classified as follows:

(1) Input-leakage-current test (I_{IH}, I_{IL})

Measurements are taken of the input currents for the input buffers without pull-up/pull-down resistors.

The current flowing in the input buffer when a High level voltage is applied to the buffer is referred to as "I_{IH}," and is guaranteed by the maximum current value. For this test to be conducted, the test pattern must include an event in which the input for the measured pin is held High. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held High.

The current flowing in the input buffer when a Low level voltage is applied to the buffer is referred to as "I_{IL}," and is guaranteed by the maximum current value. For this test to be conducted, the test pattern must include an event in which the input for the measured pin is held Low. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held Low.

(2) Pull-up current test (I_{PU})

The current flowing in the input buffer is measured using a pull-up resistor when a Low level voltage is applied to the buffer. For this test to be conducted, the test pattern must include an event in which the input for the measured pin is held Low. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held Low.

(3) Pull-down current test (I_{PD})

The current flowing in the input buffer is measured using a pull-down resistor when a High level voltage is applied to the buffer. For this test to be conducted, the test pattern must include an event in which input for the measured pin is held High. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held High.

(4) Off state leakage current (I_{OZ})

Measurements are taken of the leakage current flowing in the open-drain or 3-state output buffer when its output enters a high impedance state. In this test, the measured pin is placed in a high impedance state and measurements are taken of current values by applying a V_{DD} level and V_{SS} level voltage to the measured pin, respectively. Therefore, the test pattern must include an event in which the measured pin enters a high impedance state.

11.5 Notes Regarding the Use of Oscillation Circuits

For systems using oscillation circuits (examples shown below), in general, because the oscillation inverter's drive capability is small and the oscillation circuit's output waveform is affected by the load in the measurement environment, the waveform does not precisely propagate to the gates in the stages following the oscillation circuit.

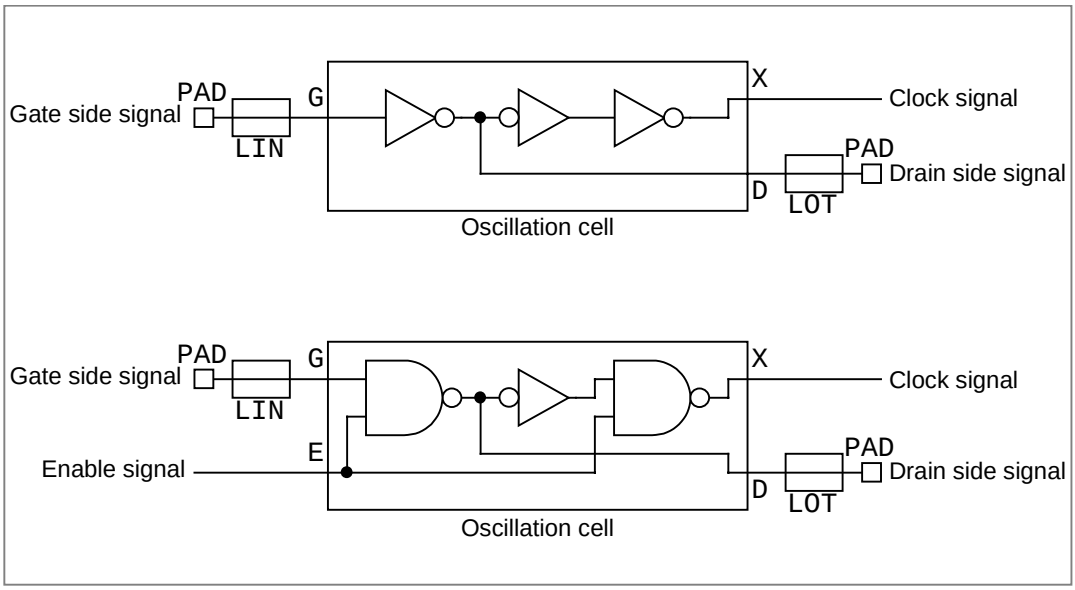


Figure 11-2 Examples of Oscillation Circuits

To reproduce the simulation state using a tester, therefore, a corrective measure is taken in which reverse drive is applied (i.e., by supplying a waveform to the drain pin that is in phase with the signal output to the drain).

If the oscillation inverter is comprised of an inverter, the reverse drive signal, i.e., the signal to be entered from the drain, can be produced simply by entering a signal 180 degrees out of phase with the signal being applied to the gate. If comprised of a NAND gate (known as an "intermittent oscillator" or "Gated OSC"), however, the signal to be entered cannot easily be determined from the gate signal alone. Therefore, the reverse drive waveform is determined based on the expected value of the drain pin.

In this method, if the input waveform is an NRZ waveform and has a strobe at the end of a test period, the expected value of the drain pin can be used directly for the input waveform to produce a reverse drive waveform. In the case of an RZ waveform, however, the expected value of the drain pin remains High or Low regardless of whether the pin is oscillating or turned off, and a reverse drive waveform cannot be determined by referring to the expected value of the drain pin.

For systems using intermittent oscillators, therefore, take the following into consideration:

1. Use of an RZ waveform for the input signal is inhibited.
2. The clock signal cannot have its state changed by changing the enable signal.

11.6 Regarding AC Testing

In AC testing, the elapsed time from when the state of any input pin changes until the change propagates to the output pin is measured. The measurement paths chosen by customers are used for AC testing. However, the test patterns described in this chapter need not be prepared when adopting those shown in Chapter 10, "Circuit Design that Takes Testability into Account."

11.6.1 Constraints Regarding Measurement Events

AC testing is normally conducted using a test method known as the binary research method. For the measured pin (i.e., an output pin the state of which has changed), there can be only one location within the measurement event at which the measured pin changes state. (No measurements can be taken at the pins from which RZ waveforms are output. Nor can measurements be taken in cases in which hazards are output in the measurement event.) Furthermore, the state changes of the signal that can be measured must be High to Low or Low to High (changes in which Z is involved cannot be measured).

It should also be noted that caution must be used in the selection of a measurement event in which no multiple output pins change state at the same time, or in which there is no signal contention between the bi-directional pins and the LSI tester. This is due to the fact that a simultaneous change in state or signal contention causes the LSI's power supply to fluctuate greatly, which affects the output waveform at the measured pin, making precise measurement impossible.

11.6.2 Constraints on the Measurement Location for AC Testing

Limit the measurement locations in AC testing to four.

11.6.3 Constraints Regarding the Path Delay Which is Tested

In the AC measurement path, the larger the delay, the greater the measurement accuracy. Make sure the delay time in the measured path is set to 30 ns or more, but does not exceed the strobe point under Max conditions of test simulation.

11.6.4 Other Constraints

(1) Do not specify paths from the oscillation circuit.

(2) Specify paths that do not pass through the internal 3-state circuit (internal bus).

(3) Do not specify paths in which there is any bi-directional cell between the input buffer and the output buffer of the measured path.

(4) If power supplies with two or more voltage ranges are used, limit the measured voltage in AC testing to one of those voltage ranges.

11.7 Test Patterns Constraints for Bi-directional Pins

Due to constraints on tester performance, the bi-directional pins cannot be switched between input and output modes more than twice per event. Therefore, make sure the test patterns created do not use RZ waveforms to control the switching of input/output modes for the bi-directional cells.

11.8 Notes on Device in a High Impedance State

At Epson, CMOS devices are subject to the limitation that, when the input pins are in a high impedance state, the device operation cannot be guaranteed and the high impedance state is inhibited during simulation.

To solve such high impedance related problems, I/O cells with pull-up/pull-down resistors are available from Epson. However, the propagation delays in the pull-up/pull-down resistors of these cells are not taken into consideration in simulation for the reasons specified below. Therefore, because operation cannot be precisely simulated, the non input state for the bi-directional pins with pull-up/pull-down resistors in input mode is also inhibited during simulation.

<Reasons that the propagation delays in pull-up/pull-down resistors are not considered>

Because the delay fluctuates significantly depending on the external load capacitance

Because the pull-up/pull-down resistors are used only to avoid floating gates due to the high-impedance state

At Epson, test patterns are checked for the above contents prior to simulation through the use of an appropriate tool. If state Z representing a high-impedance state is detected, customers are requested to correct the test pattern.

In such a case, for the aforementioned reasons, customers are also cautioned about the “Z” state on the bi-directional pins with pull-up/pull-down resistors, as well as for open drain bi-directional pins.

<Corrective measures>

When test patterns are checked, all occurrences of the Z state in the bi-directional pins are indicated by an error (not including the Z state appearing on the 3-state and open drain output pins).

As a means of correcting the input pattern, a utility program is available from Epson that replaces the Z state on the aforementioned bi-directional pins with logic 1 when they come equipped with a pull-up resistor, or logic 0 when they come equipped with a pull-down resistor.

If bi-directional pins in the X state are placed in input mode, the X state is propagated in simulation regardless of whether they have a pull-up or pull-down resistor, and is represented by “?” in the simulation result. Customers are requested to correct occurrences of “?” before conducting resimulation.

Table 11-1 Handling the Signal at the Bi-directional Pins in Simulation

Input Pattern	Input/Output Mode	Simulation	Simulation Result (Output Pattern)
“X”	Input Mode	“X”	“?”
“1”, “H”	Input Mode	“1”	“1”
“0”, “L”	Input Mode	“0”	“0”

Appendix A1 Electrical Characteristics Data (X Type)

A1.1 Characteristics of Input/Output Buffers (3.3 V operation)

A1.1.1 Input Buffer Characteristics (3.3 V ± 0.3 V)

- Standard type input buffers

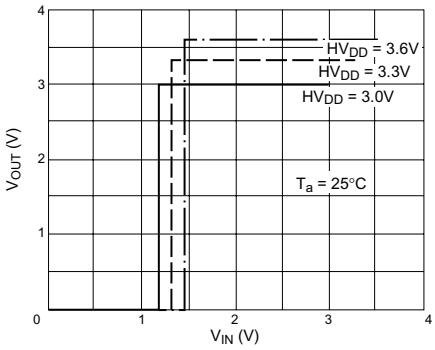


Figure A1-1 Input Characteristics (LVTTL)

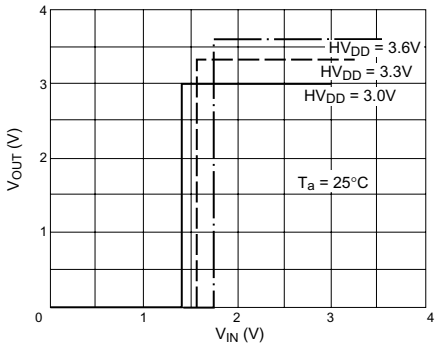


Figure A1-2 Input Characteristics (CMOS)

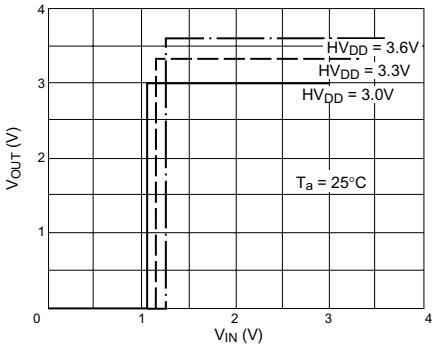


Figure A1-3 Input Characteristics (PCI-3 V)

- Schmitt-trigger type input buffers

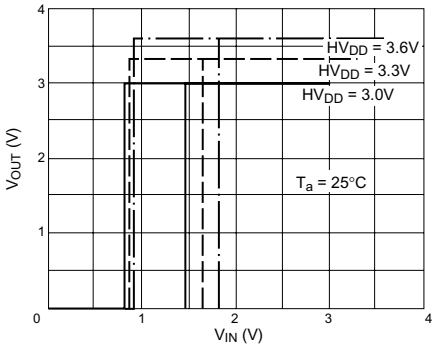


Figure A1-4 Input Characteristics (LVTTL Schmitt)

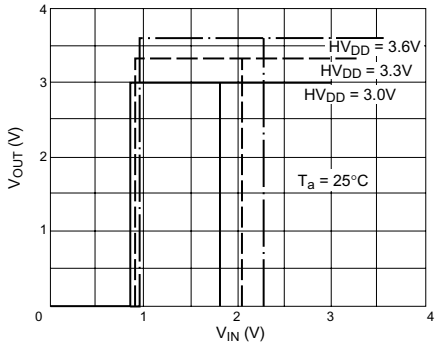


Figure A1-5 Input Characteristics (CMOS Schmitt)

A1.1.2 Input Through Current (3.3 V ± 0.3 V)

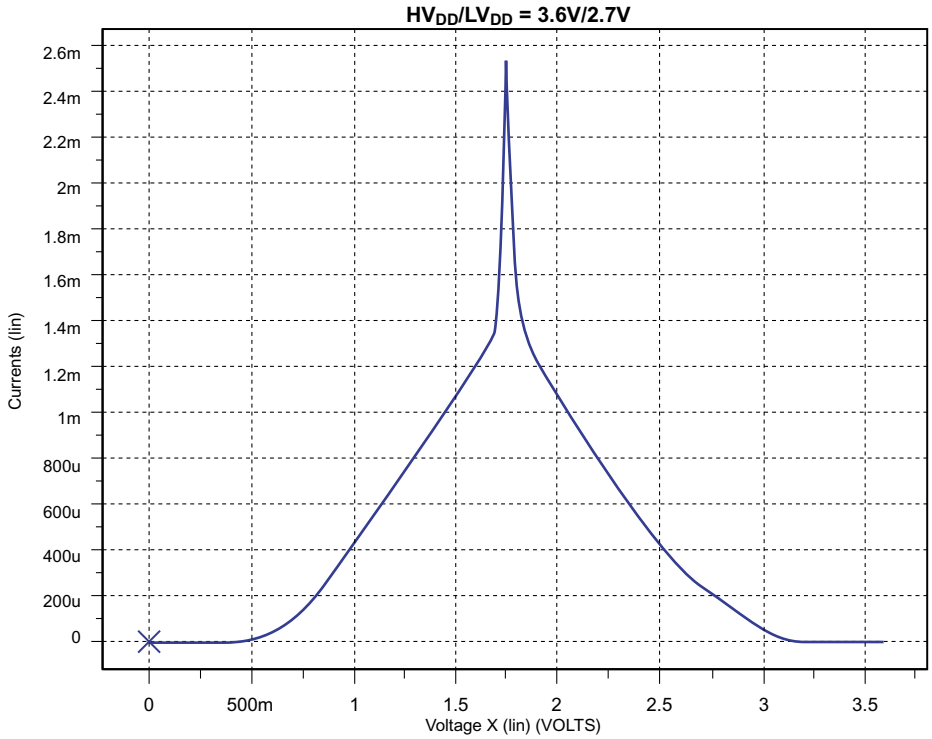


Figure A1-6 Input Through Current (CMOS)

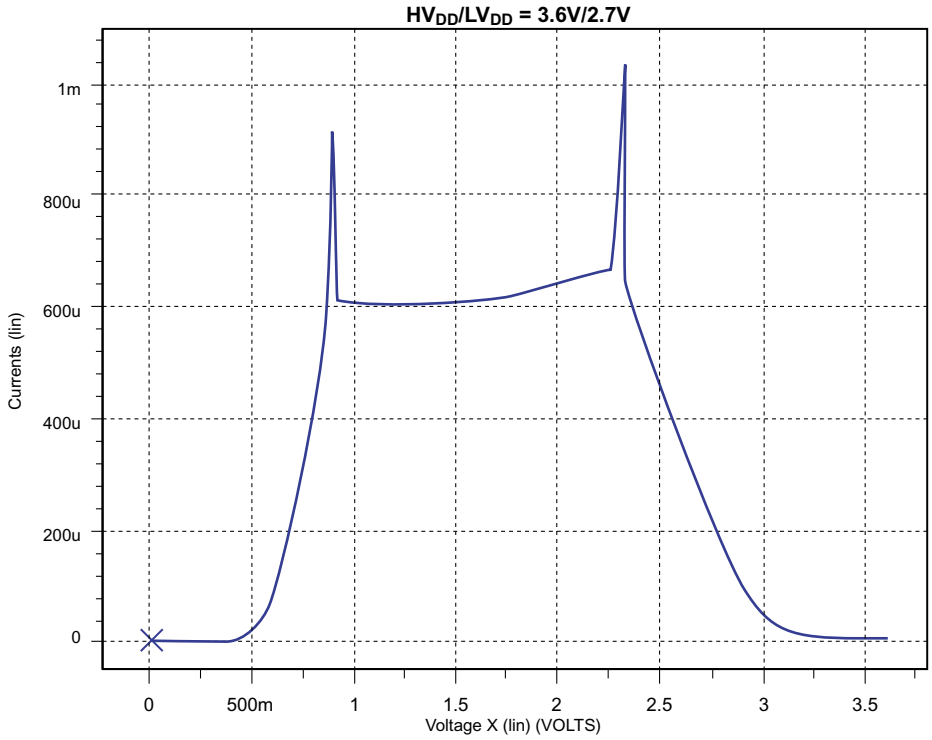


Figure A1-7 Input Through Current (CMOS Schmitt)

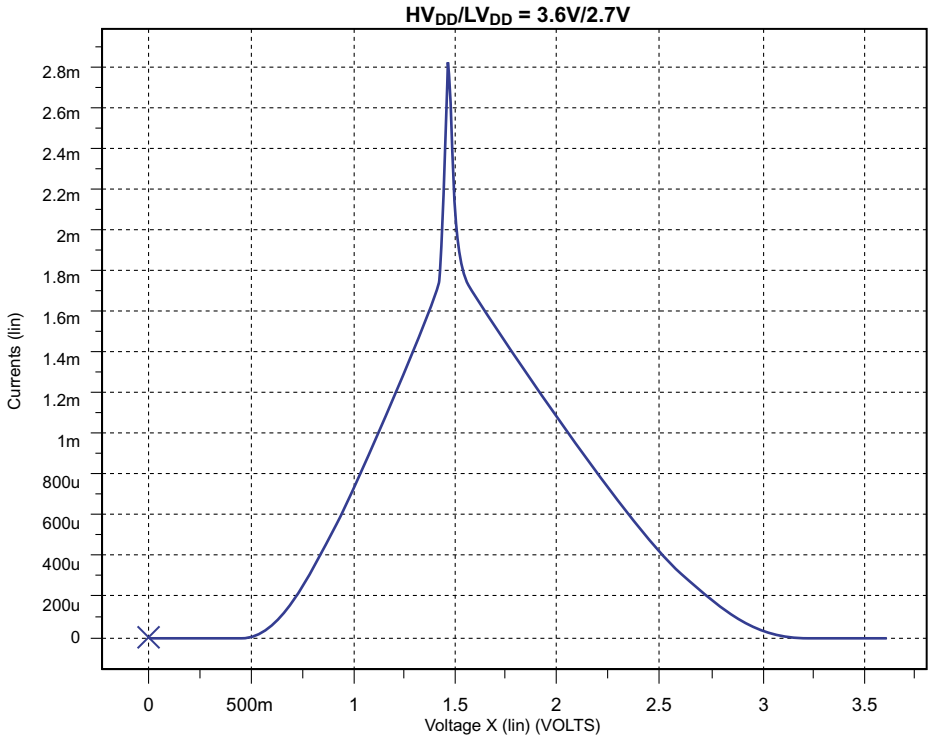


Figure A1-8 Input Through Current (LVTTL)

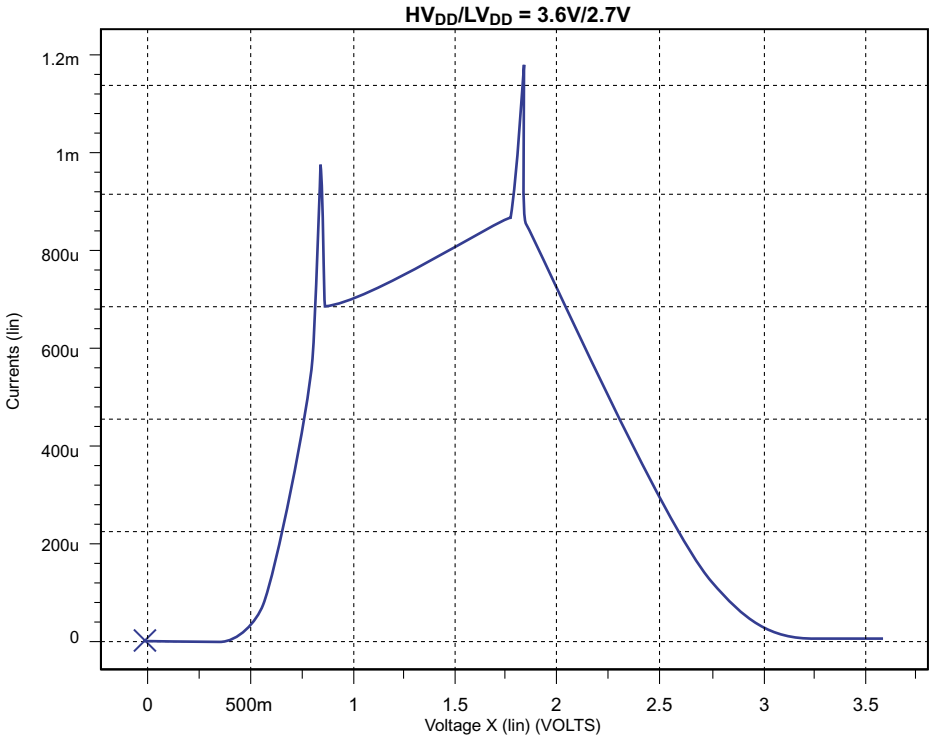


Figure A1-9 Input Through Current (LVTTL Schmitt)

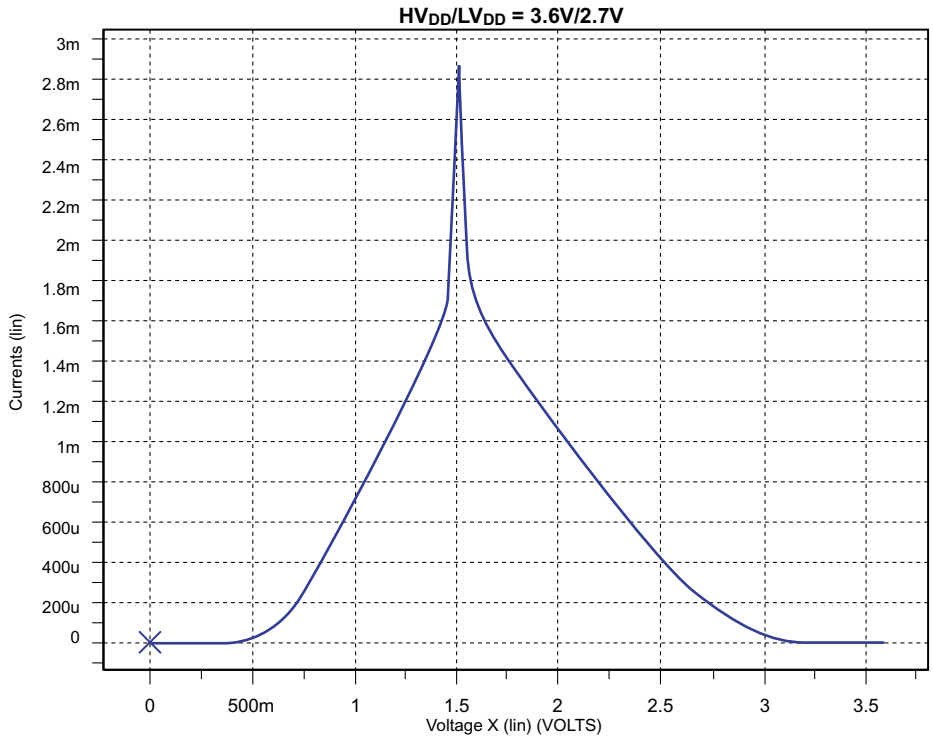


Figure A1-10 Input Through Current (PCI)

A1.1.3 Output Buffer Characteristics (3.3 V ± 0.3 V)

(1) List of output buffer specifications

Table A1-1 Output Current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type S	-0.1	0.1	mA
Type M	-1	1	mA
Type 1	-3	3	mA
Type 2	-6	6	mA
Type 3	-12	12	mA
PCI	Confirmed to the PCI Standard		mA

Note *1: $V_{OH} = HV_{DD}$-0.4 V (HV_{DD} = 3.3 V)

*2: V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

(2) IOL-VOL and IOH-VOH

● IOL-VOL

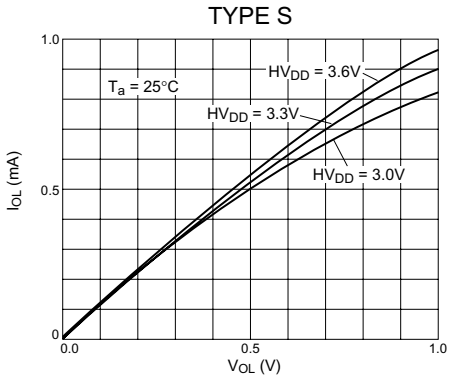


Figure A1-11

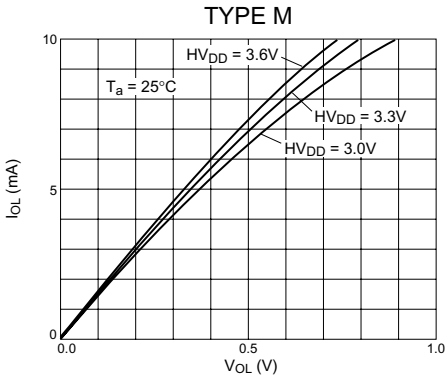


Figure A1-12

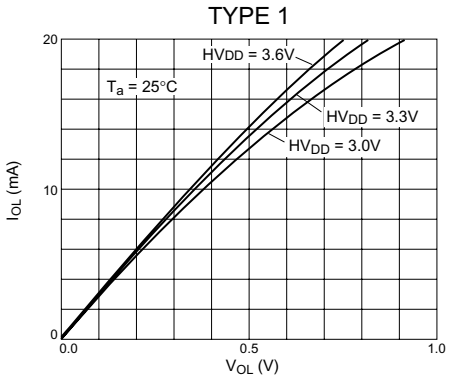


Figure A1-13

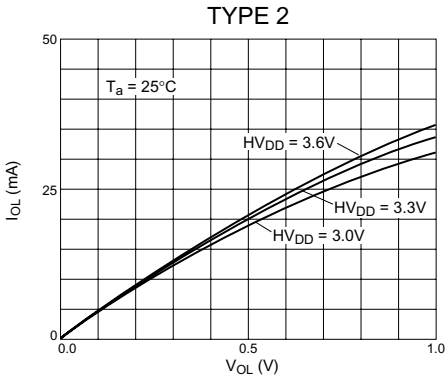


Figure A1-14

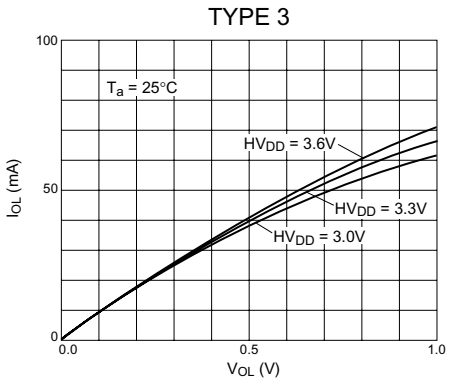


Figure A1-15

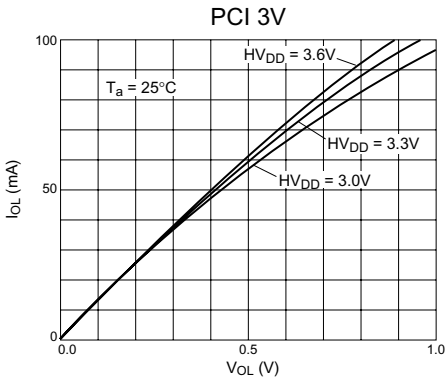


Figure A1-16

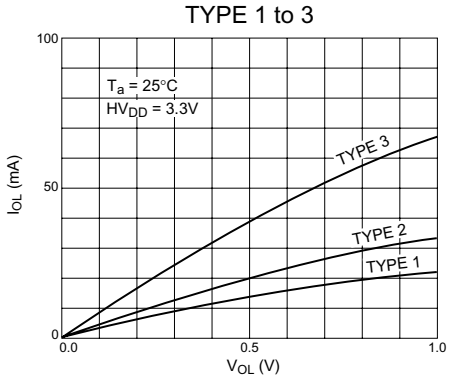


Figure A1-17

● I_{OH}-V_{OH}

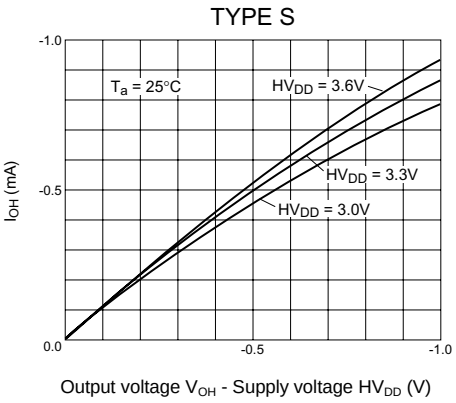


Figure A1-18

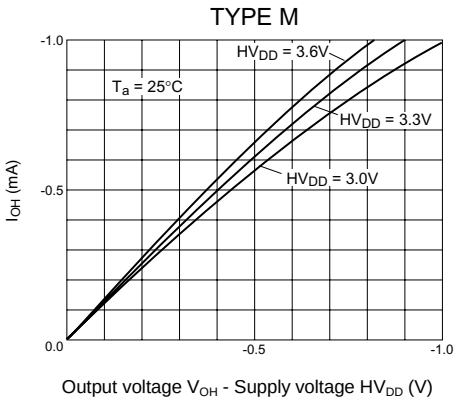


Figure A1-19

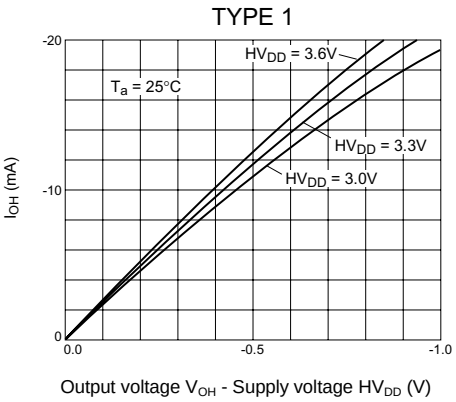


Figure A1-20

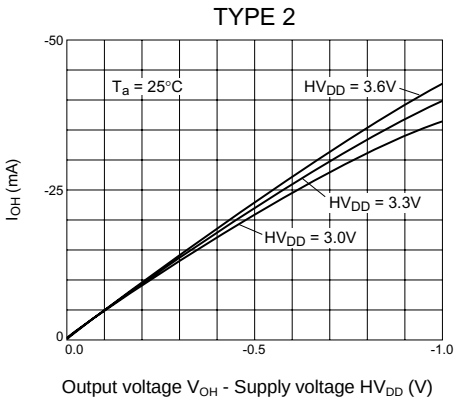


Figure A1-21

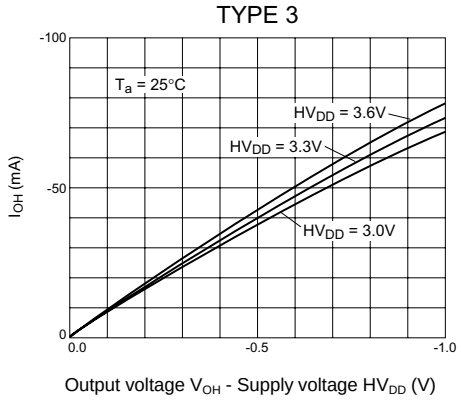


Figure A1-22

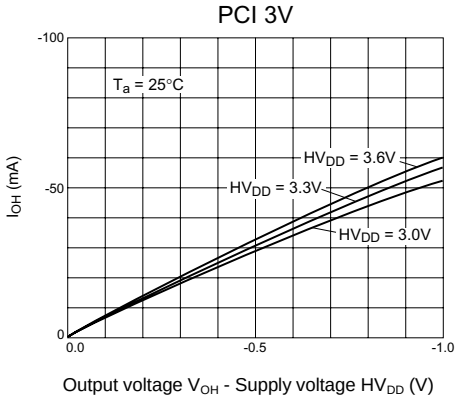


Figure A1-23

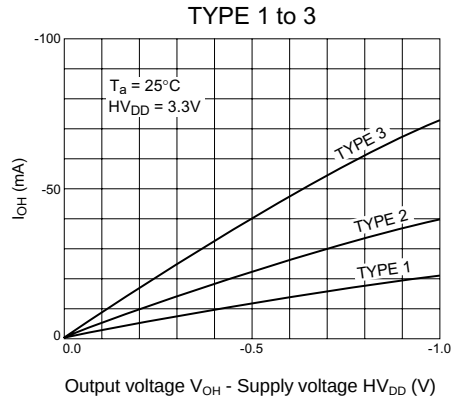


Figure A1-24

(3) I_{OL} and I_{OH} temperature characteristics

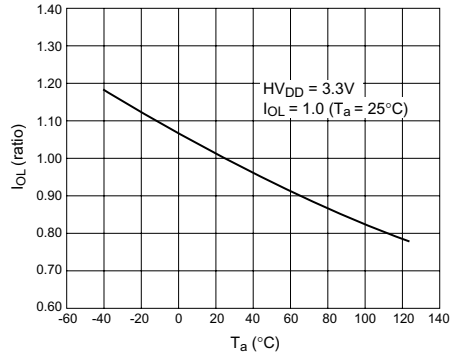


Figure A1-25

Ambient Temperature (T_a) - Output Current (I_{OL})

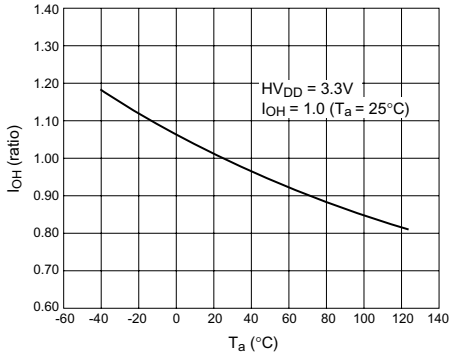


Figure A1-26

Ambient Temperature (T_a) - Output Current (I_{OH})

(4) Output delay time vs. Output load capacitance (C_L)

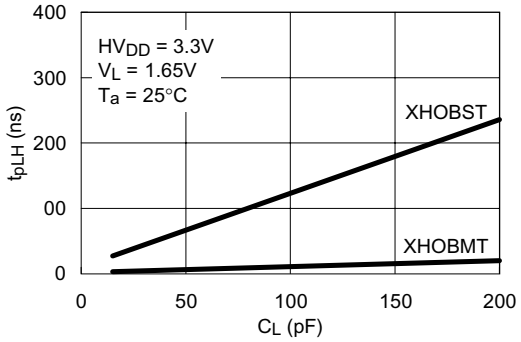


Figure A1-27

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

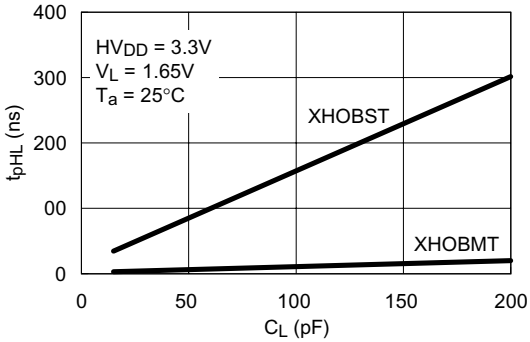


Figure A1-28

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

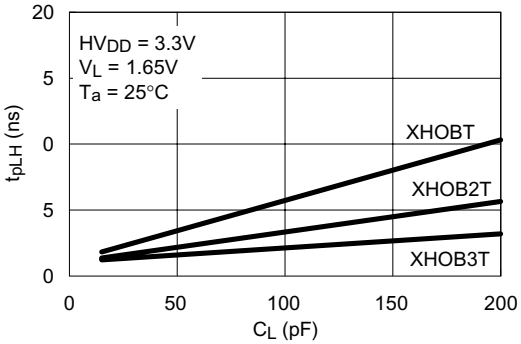


Figure A1-29

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

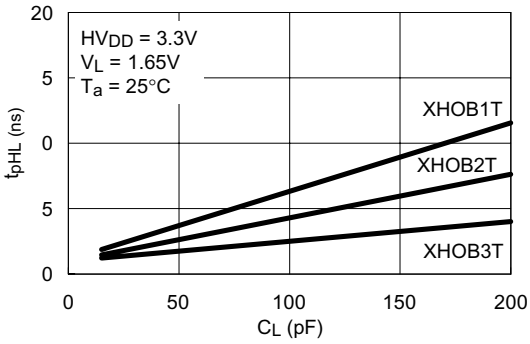


Figure A1-30

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

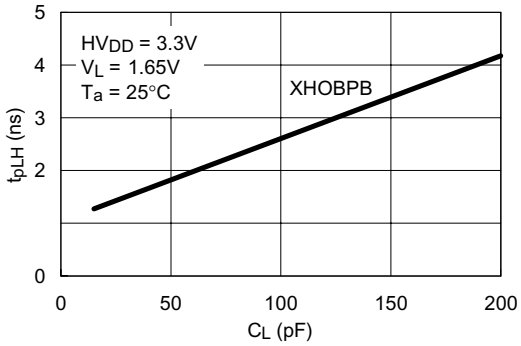


Figure A1-31

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

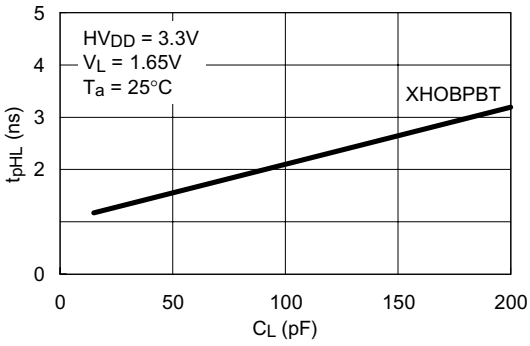


Figure A1-32

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

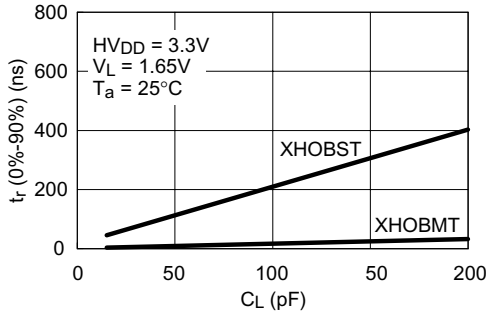


Figure A1-33

Rising Time (t_r) vs. Output Load Capacitance (C_L)

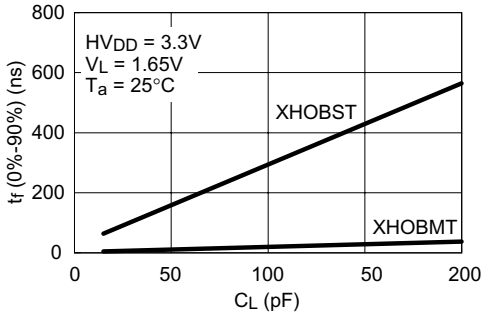


Figure A1-34

Falling Time (t_f) vs. Output Load Capacitance (C_L)

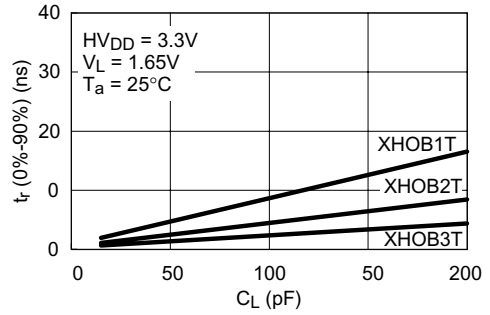


Figure A1-35

Rising Time (t_r) vs. Output Load Capacitance (C_L)

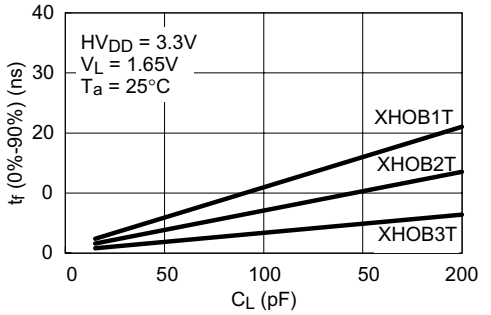


Figure A1-36

Falling Time (t_f) vs. Output Load Capacitance (C_L)

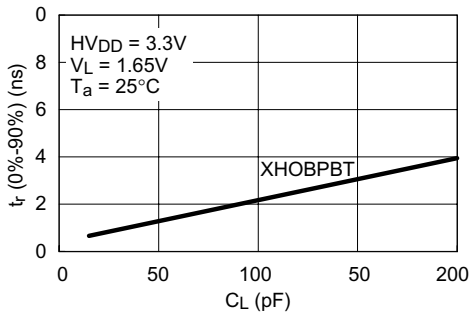


Figure A1-37

Rising Time (t_r) vs. Output Load Capacitance (C_L)

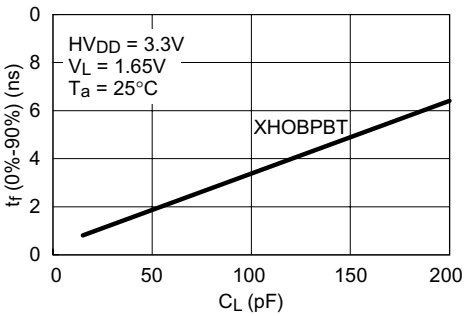


Figure A1-38

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down resistance

- Pull-up characteristics

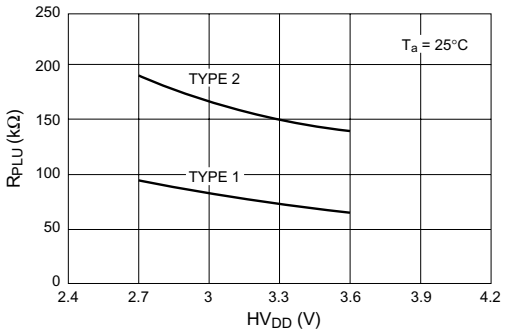


Figure A1-39

Pull-up Resistance (R_{PLU}) vs. HV_{DD}

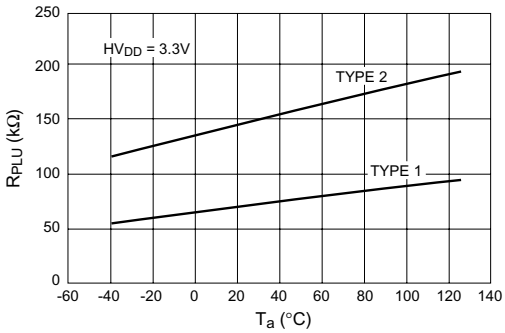


Figure A1-40

Pull-up Resistance (R_{PLU}) vs. Ambient Temperature

- Pull-down characteristics

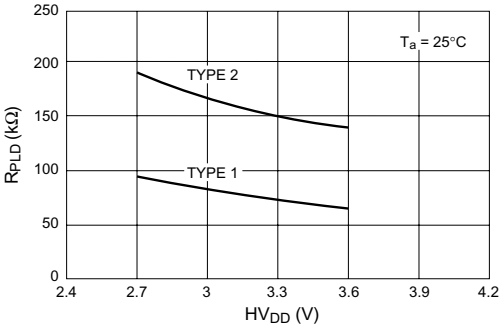


Figure A1-41

Pull-down Resistance (R_{PLD}) vs. HV_{DD}

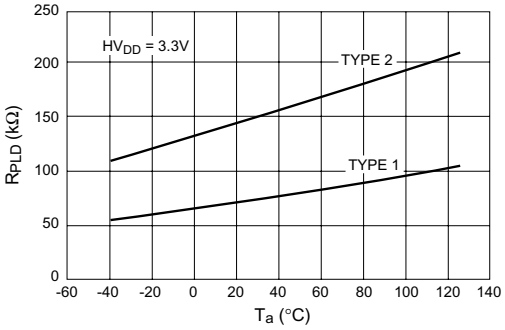


Figure A1-42

Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

(7) Output waveforms

- High Speed Type

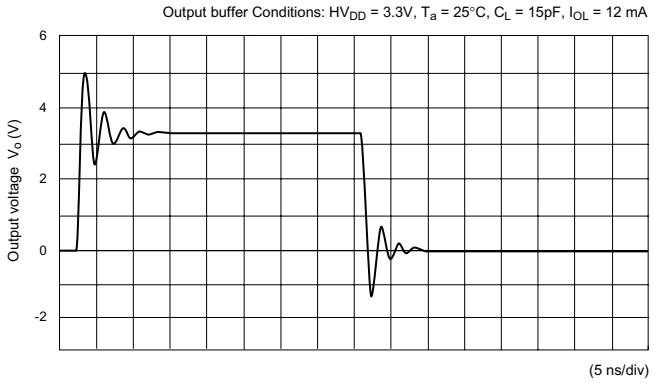


Figure A1-43 Output Waveform (XHOB3AT)

- Normal Type

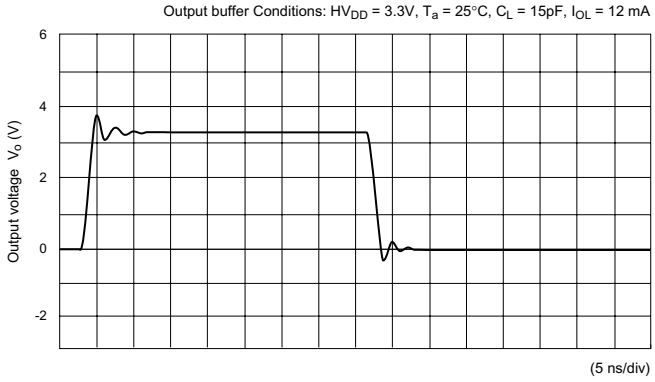


Figure A1-44 Output Waveform (XHOB3T)

- Low Noise Type

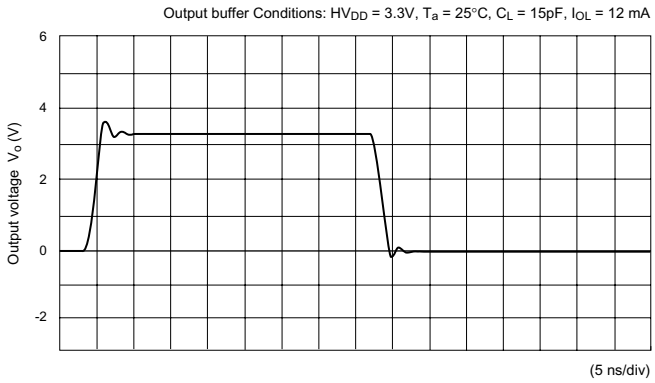


Figure A1-45 Output Waveform (XHOB3BT)

A1.2 Characteristics of Input/Output Buffers (2.5 V operation)

A1.2.1 Input Buffer Characteristics (2.5 V ± 0.2 V)

- Standard type input buffers

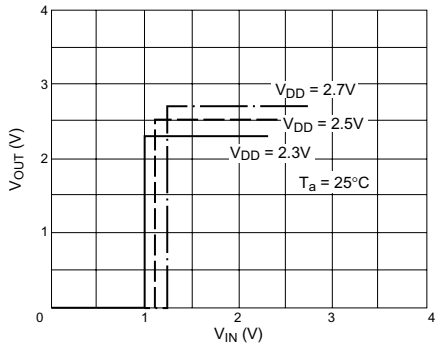


Figure A1-46 Input Characteristics (CMOS)

- Schmitt-trigger type input buffers

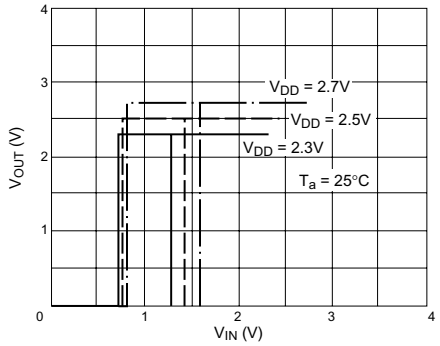


Figure A1-47 Input Characteristics (CMOS Schmitt)

A1.2.2 Input Through Current (2.5 V ± 0.2 V)

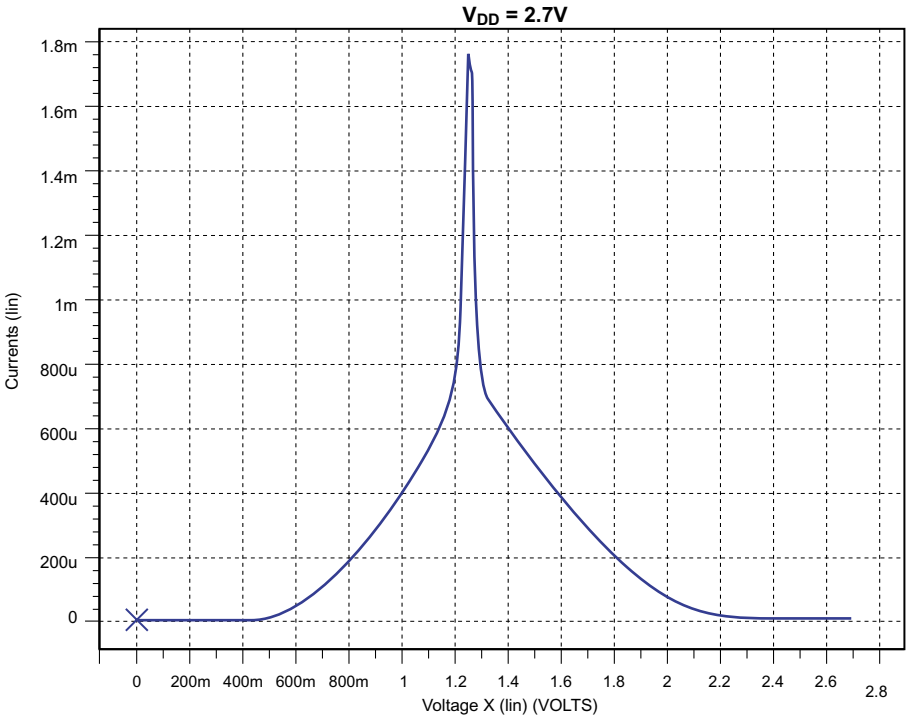


Figure A1-48 Input Through Current (CMOS)

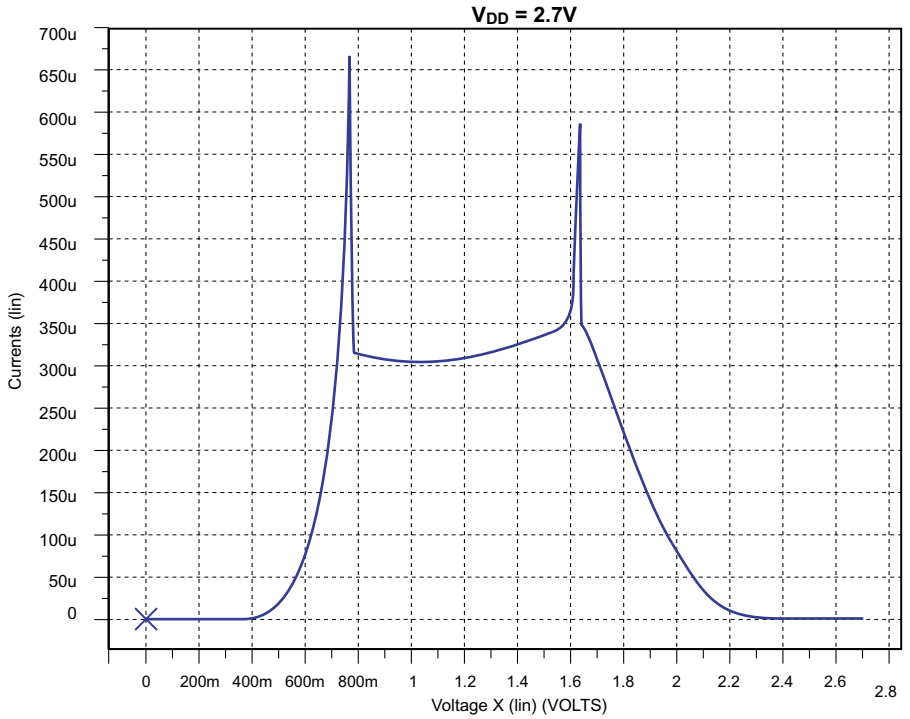


Figure A1-49 Input Through Current (CMOS Schmitt)

A1.2.3 Output Buffer Characteristics (2.5 V ± 0.2 V)

(1) List of output buffer specifications

Table A1-2 Output Current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type S	-0.1	0.1	mA
Type M	-1	1	mA
Type 1	-3	3	mA
Type 2	-6	6	mA
Type 3	-9	9	mA

Note *1: $V_{OH} = V_{DD} - 0.4$ V ($V_{DD} = 2.5$ V)

*2: $V_{OL} = 0.4$ V ($V_{DD} = 2.5$ V)

(2) IOL-VOL and IOH-VOH

● IOL-VOL

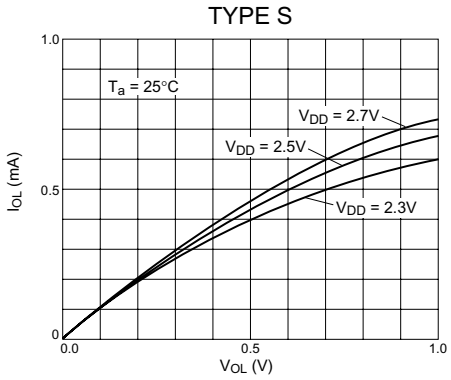


Figure A1-50

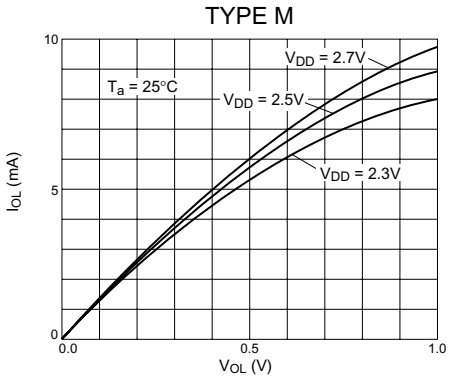


Figure A1-51

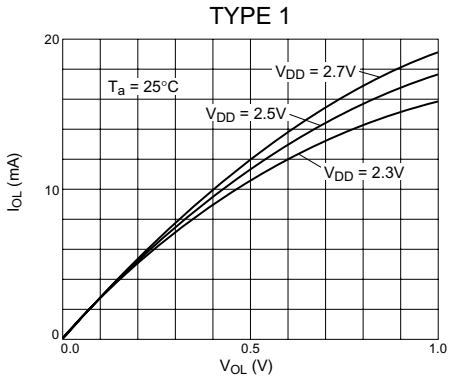


Figure A1-52

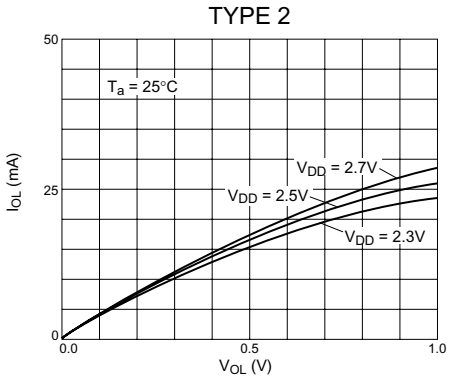


Figure A1-53

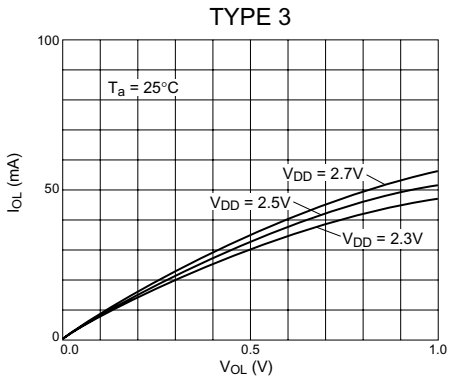


Figure A1-54

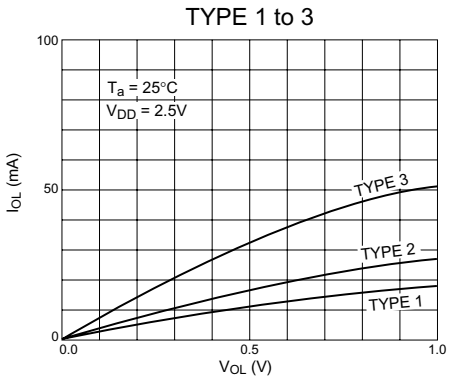


Figure A1-55

● IOH-VOH

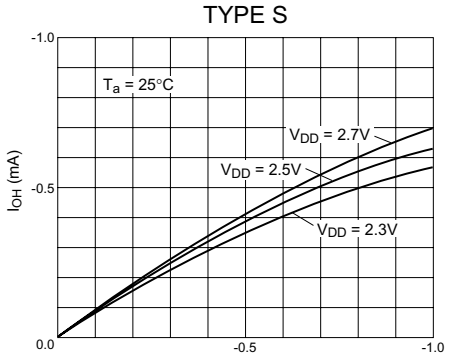


Figure A1-56

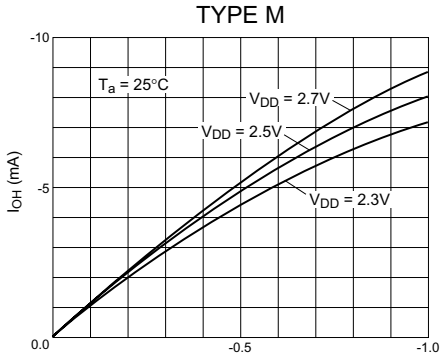


Figure A1-57

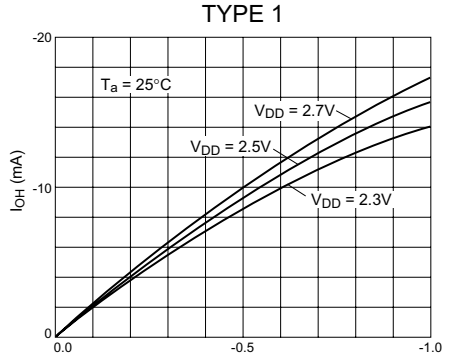


Figure A1-58

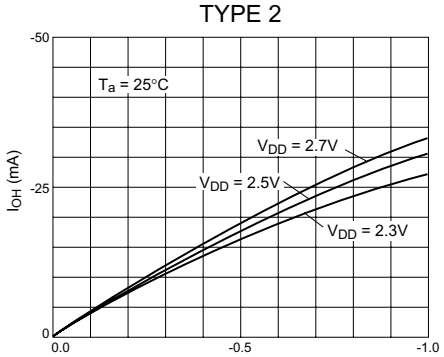


Figure A1-59

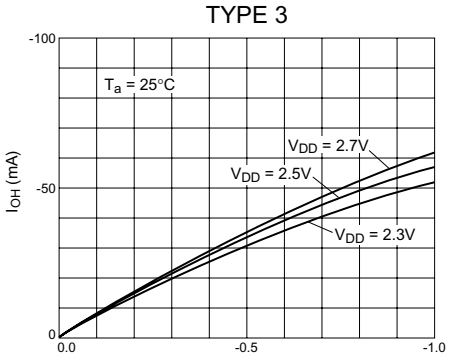


Figure A1-60

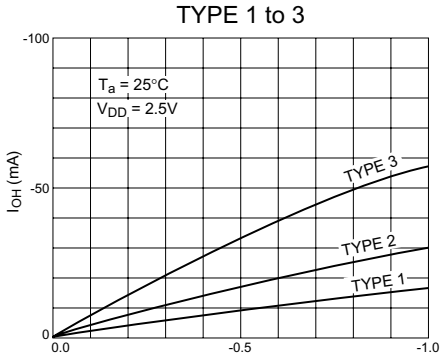


Figure A1-61

(3) I_{OL} and I_{OH} temperature characteristics

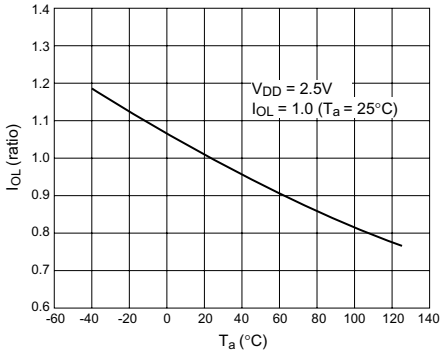


Figure A1-62

Ambient Temperature (T_a) - Output Current (I_{OL})

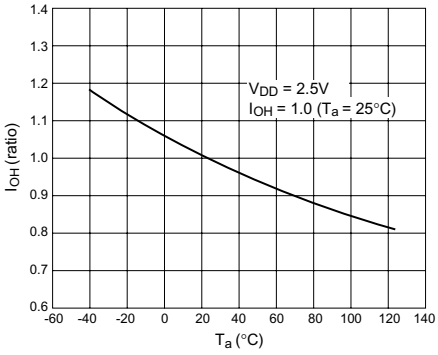


Figure A1-63

Ambient Temperature (T_a) - Output Current (I_{OH})

(4) Output delay time vs. Output load capacitance (C_L)

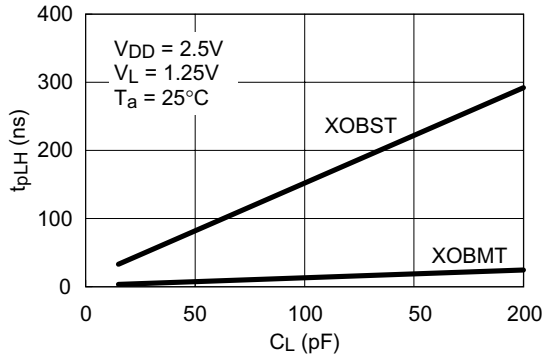


Figure A1-64

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

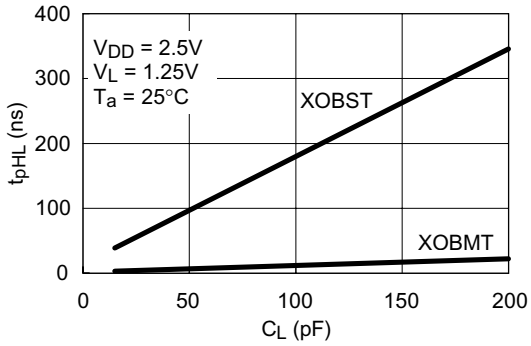


Figure A1-65

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

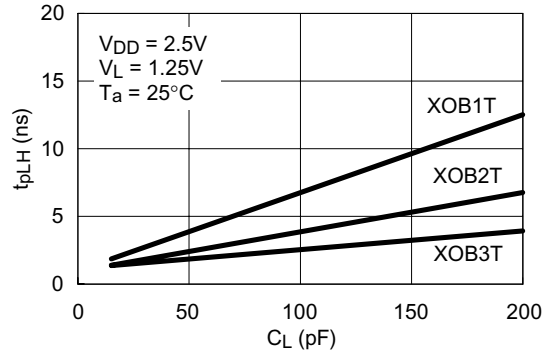


Figure A1-66

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

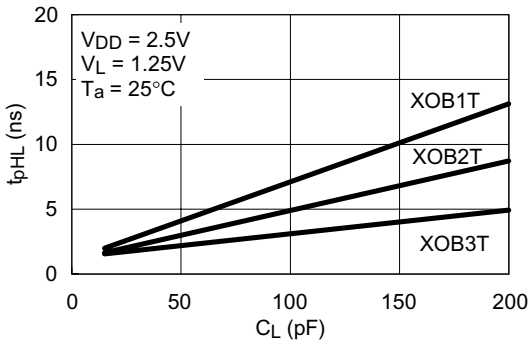


Figure A1-67

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

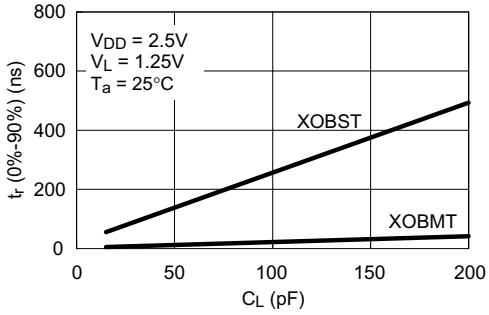


Figure A1-68

Rising Time (t_r) vs. Output Load Capacitance (C_L)

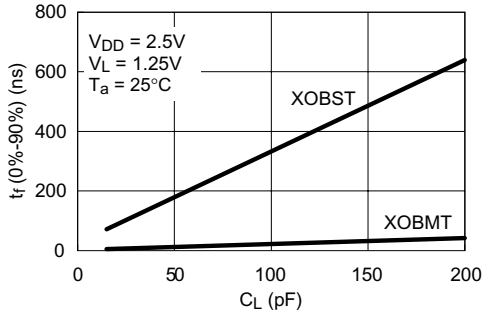


Figure A1-69

Falling Time (t_f) vs. Output Load Capacitance (C_L)

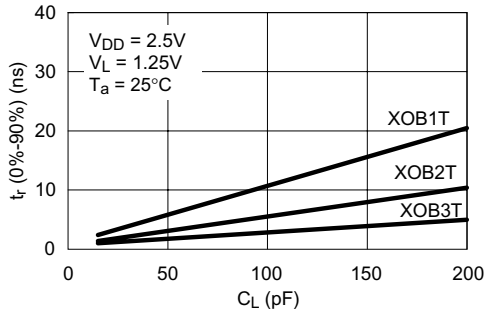


Figure A1-70

Rising Time (t_r) vs. Output Load Capacitance (C_L)

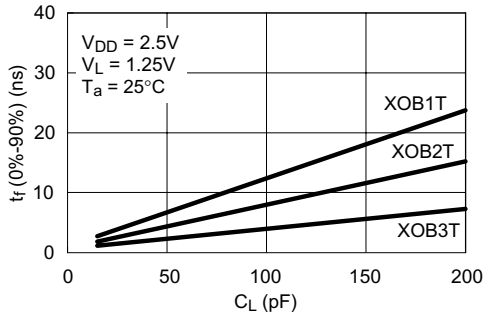


Figure A1-71

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down resistance

- Pull-up characteristics

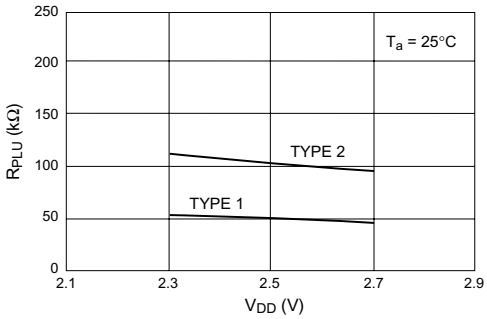


Figure A1-72

Pull-up Resistance (R_{PLU}) vs. V_{DD}

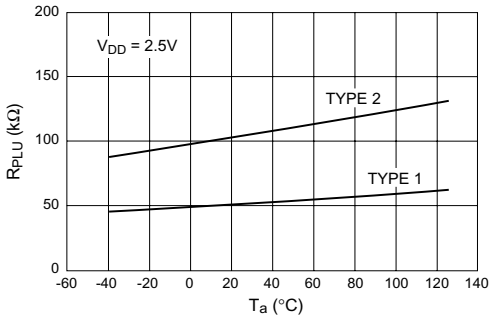


Figure A1-73

Pull-up Resistance (R_{PLU}) vs. Ambient Temperature

- Pull-down characteristics

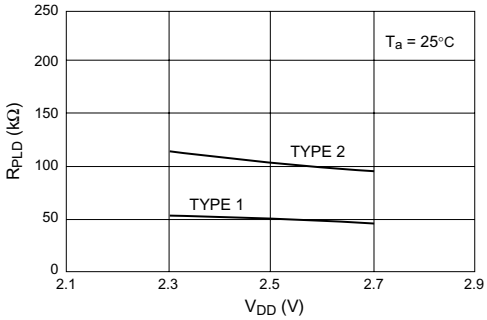


Figure A1-74

Pull-down Resistance (R_{PLD}) vs. V_{DD}

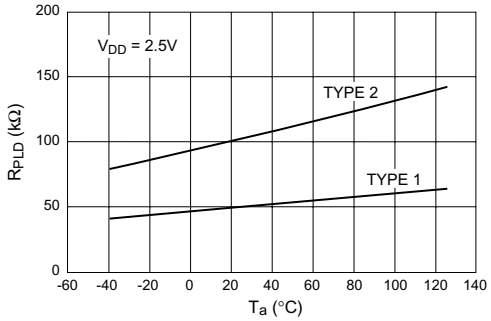


Figure A1-75

Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

(7) Output waveforms

- High Speed Type

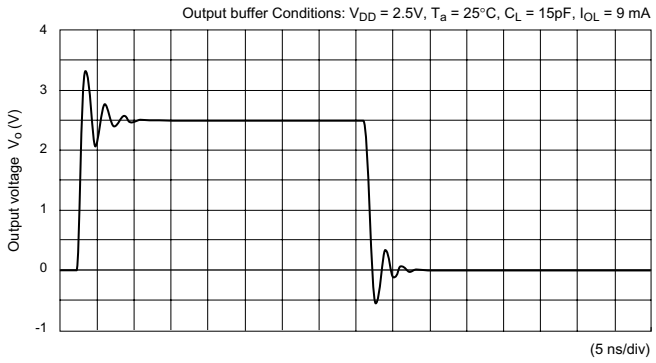


Figure A1-76 Output Waveform (XOB3AT)

- Normal Type

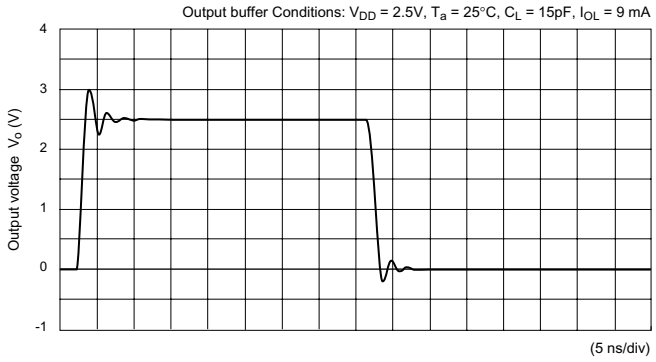


Figure A1-77 Output Waveform (XOB3T)

- Low Noise Type

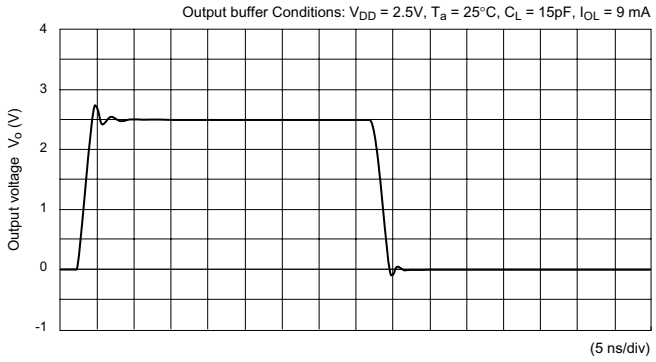


Figure A1-78 Output Waveform (XOB3BT)

A1.3 Characteristics of Input/Output Buffers (2.0 V operation)

A1.3.1 Input Buffer Characteristics (2.0 V ± 0.2 V)

- Standard type input buffers

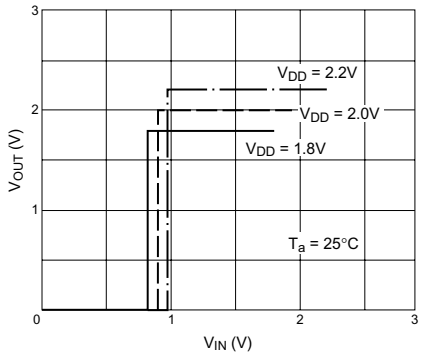


Figure A1-79 Input Characteristics (CMOS)

- Schmitt-trigger type input buffers

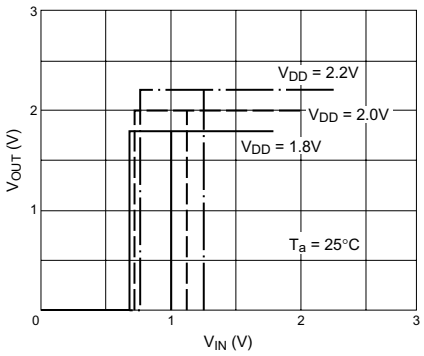


Figure A1-80 Input Characteristics (CMOS Schmitt)

A1.3.2 Input Through Current (2.0 V ± 0.2 V)

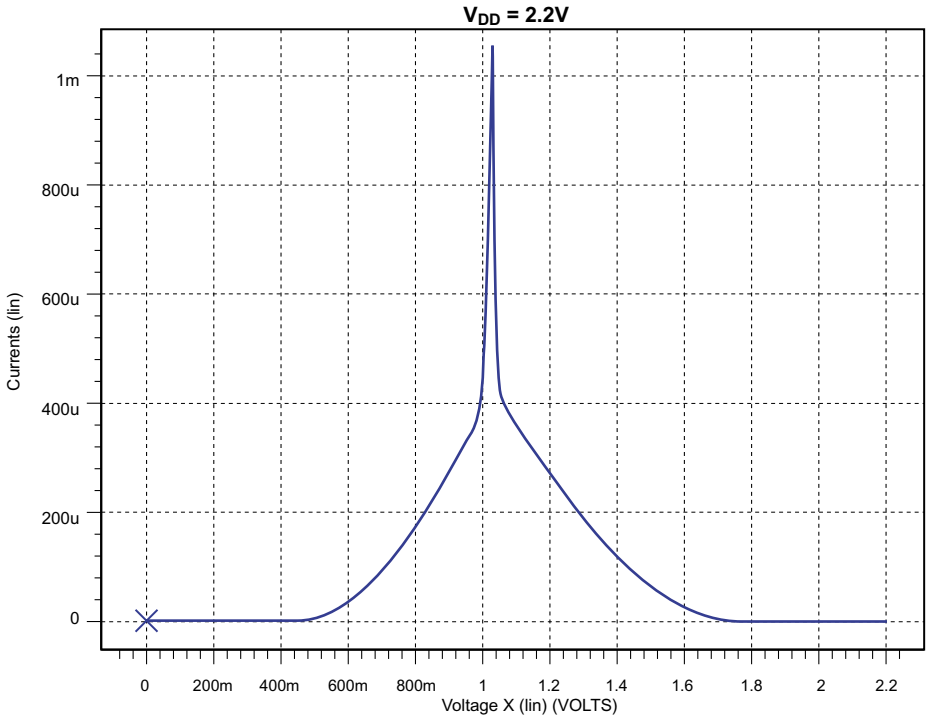


Figure A1-81 Input Through Current (CMOS)

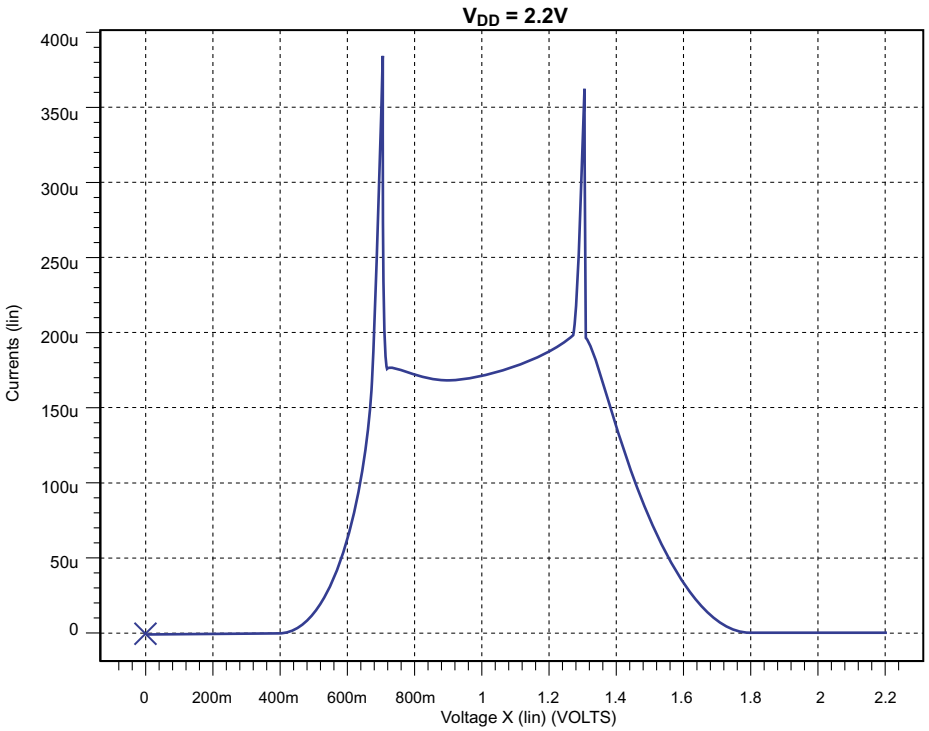


Figure A1-82 Input Through Current (CMOS Schmitt)

A1.3.3 Output Buffer Characteristics (2.0 V ± 0.2 V)

(1) List of output buffer specifications

Table A1-3 Output Current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type S	-0.05	0.05	mA
Type M	-0.3	0.3	mA
Type 1	-1	1	mA
Type 2	-2	2	mA
Type 3	-3	3	mA

Note *1: $V_{OH} = V_{DD} - 0.2$ V ($V_{DD} = 2.0$ V)

*2: $V_{OL} = 0.2$ V ($V_{DD} = 2.0$ V)

(2) IOH-VOL and IOH-VOH

- IOL-VOL

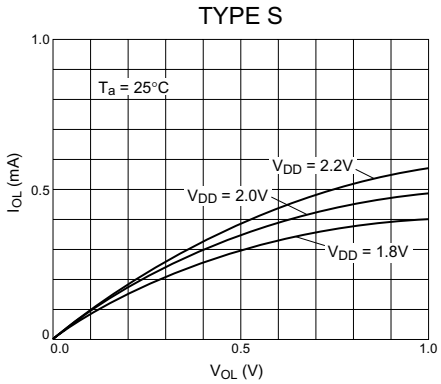


Figure A1-83

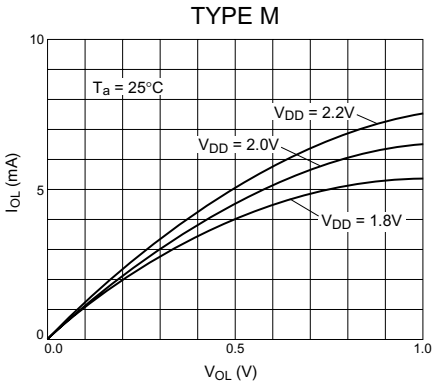


Figure A1-84

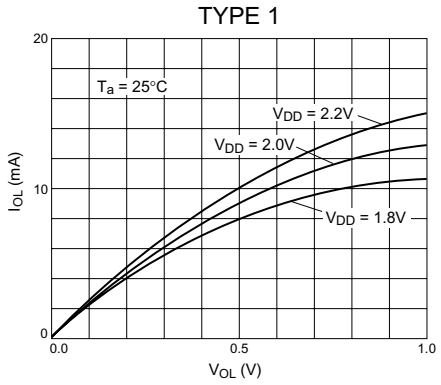


Figure A1-85

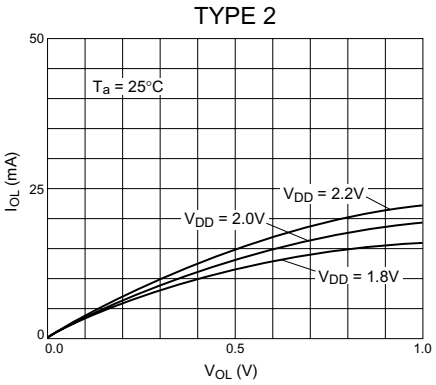


Figure A1-86

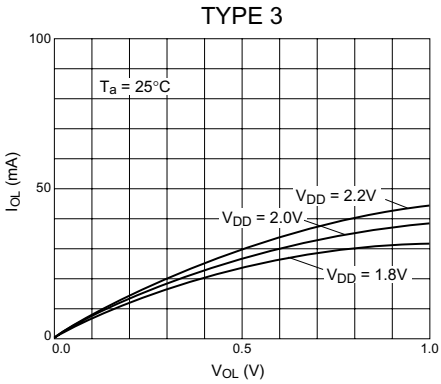


Figure A1-87

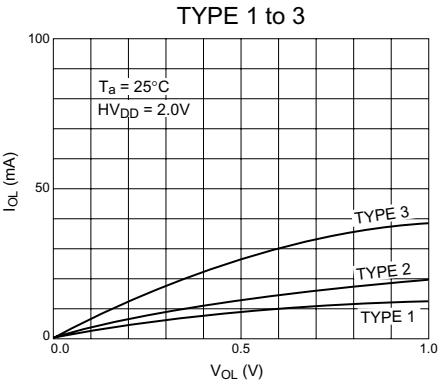


Figure A1-88

● IOH-VOH

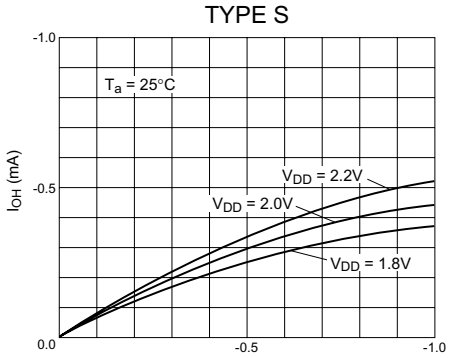


Figure A1-89

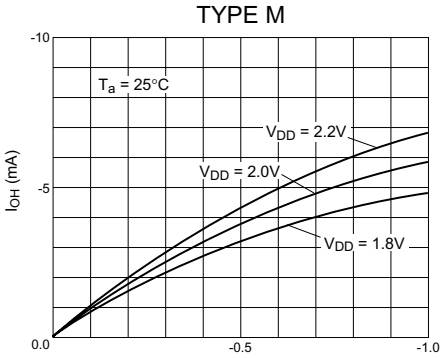


Figure A1-90

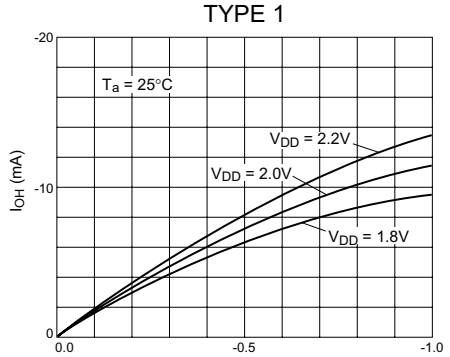


Figure A1-91

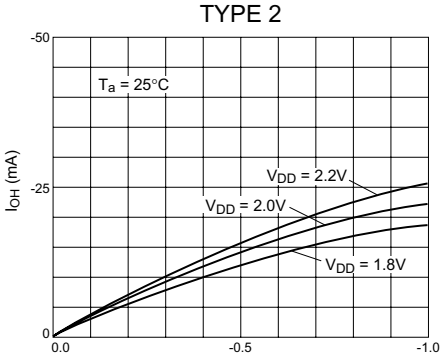


Figure A1-92

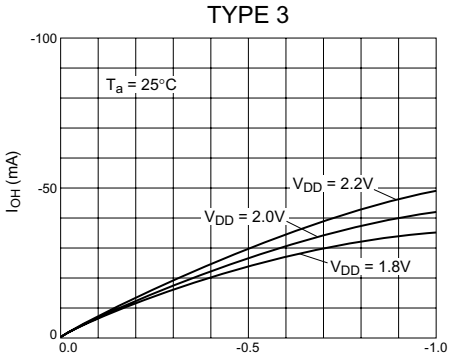


Figure A1-93

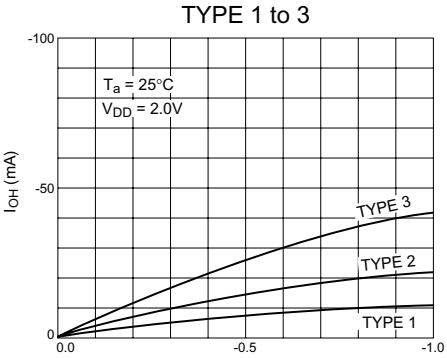


Figure A1-94

(3) I_{OL} and I_{OH} temperature characteristics

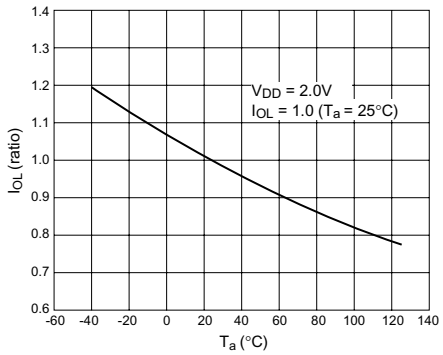


Figure A1-95

Ambient Temperature (T_a) - Output Current (I_{OL})

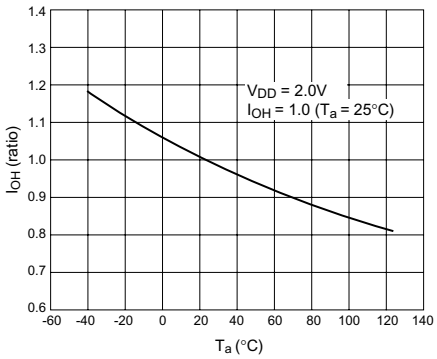


Figure A1-96

Ambient Temperature (T_a) - Output Current (I_{OH})

(4) Output delay time vs. Output load capacitance (C_L)

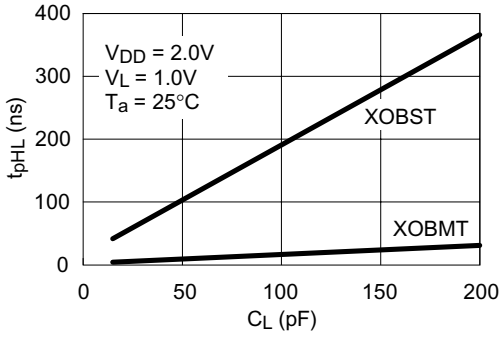


Figure A1-97

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

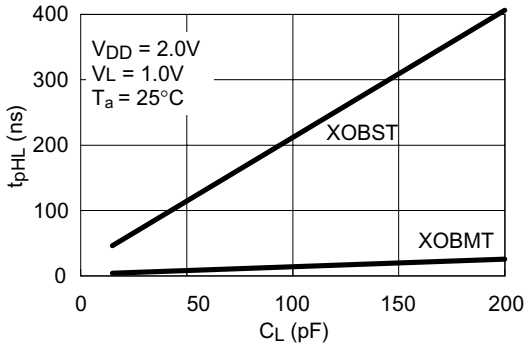


Figure A1-98

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

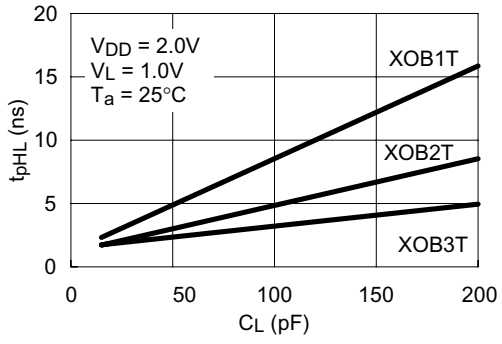


Figure A1-99

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

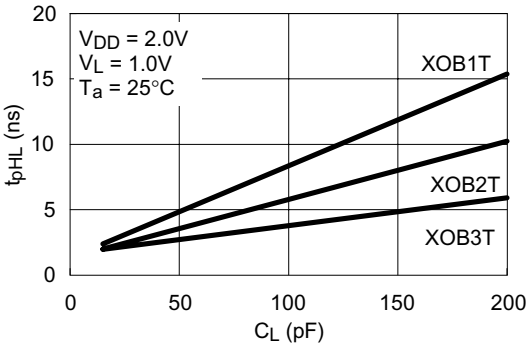


Figure A1-100

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

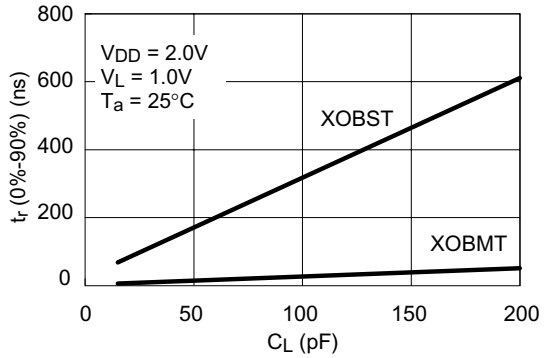


Figure A1-101

Rising Time (t_r) vs. Output Load Capacitance (C_L)

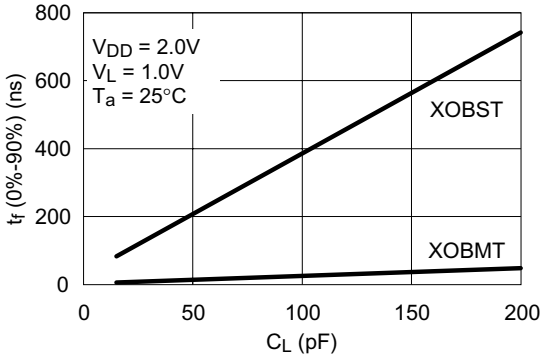


Figure A1-102

Falling Time (t_f) vs. Output Load Capacitance (C_L)

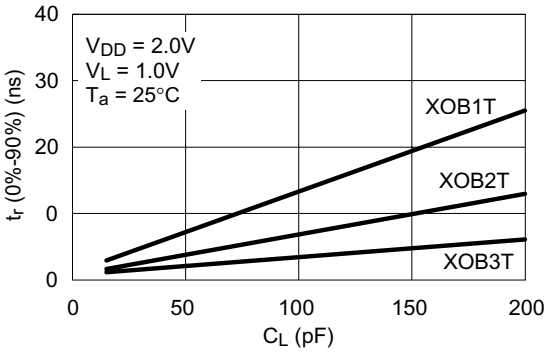


Figure A1-103

Rising Time (t_r) vs. Output Load Capacitance (C_L)

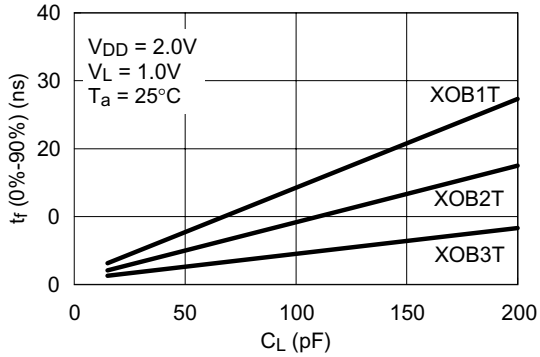


Figure A1-104

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down resistance

● Pull-up characteristics

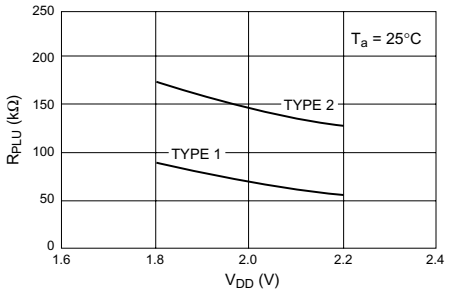


Figure A1-105

Pull-up Resistance (R_{PLU}) vs. V_{DD}

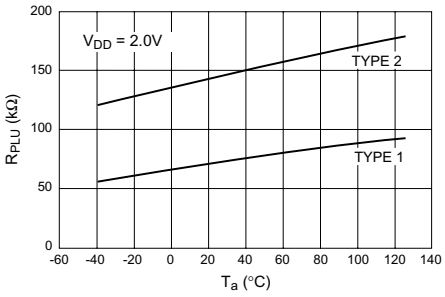


Figure A1-106

Pull-up Resistance (R_{PLU}) vs. Ambient Temperature

● Pull-down characteristics

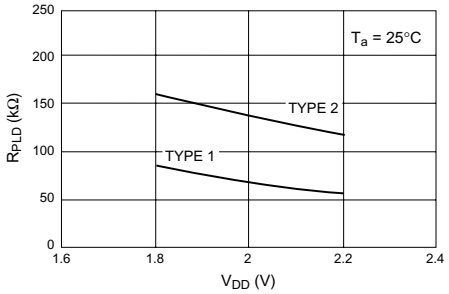


Figure A1-107

Pull-down Resistance (R_{PLD}) vs. V_{DD}

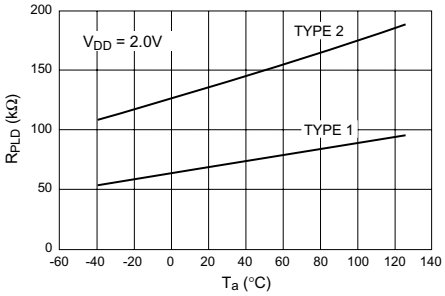


Figure A1-108

Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

(7) Output waveforms

- High Speed Type

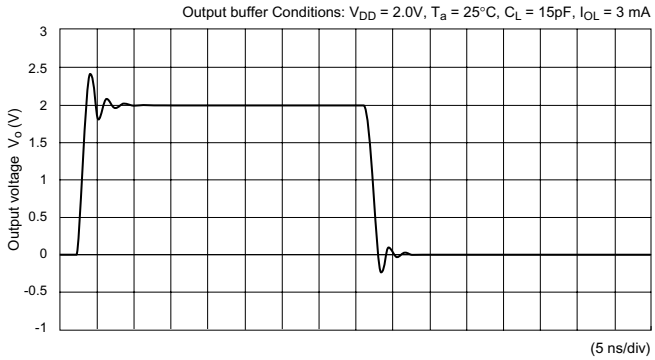


Figure A1-109 Output Waveform (XOB3AT)

- Normal Type

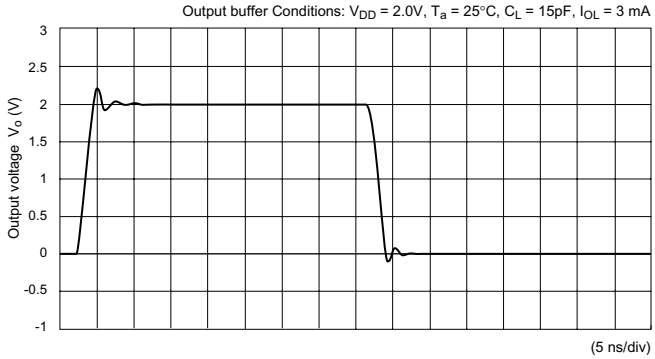


Figure A1-110 Output Waveform (XOB3T)

- Low Noise Type

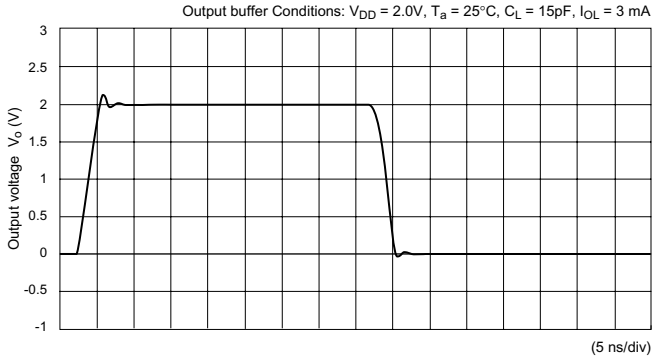


Figure A1-111 Output Waveform (XOB3BT)

Appendix A2 Electrical Characteristics Data (XF Type)

A2.1 Characteristics of Input/Output Buffers (3.3 V operation)

A2.1.1 Input Buffer Characteristics (3.3 V ± 0.3 V)

- Standard type input buffers

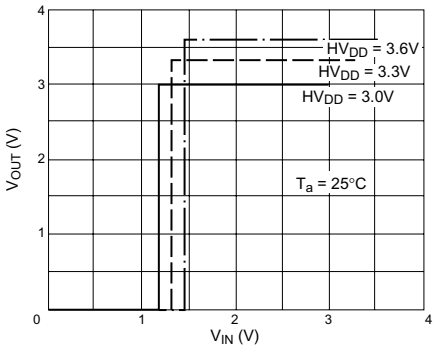


Figure A2-1 Input Characteristics (LVTTL)

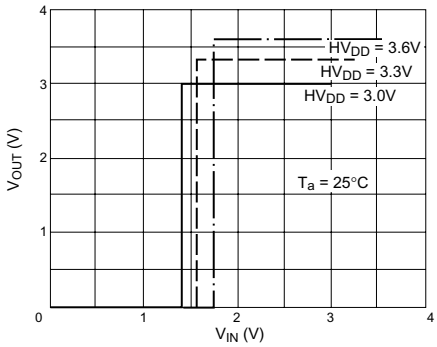


Figure A2-2 Input Characteristics (CMOS)

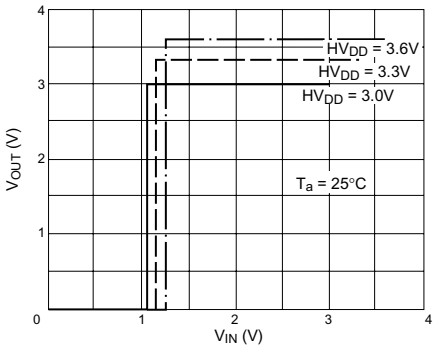


Figure A2-3 Input Characteristics (PCI-3V)

- Schmitt-trigger type input buffers

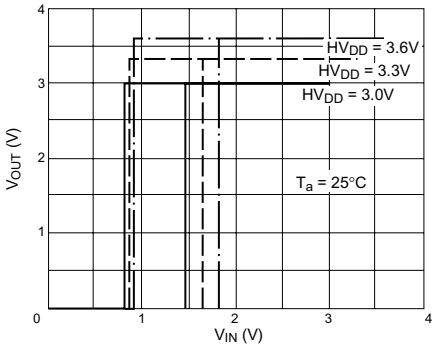


Figure A2-4 Input Characteristics (LVTTL Schmitt)

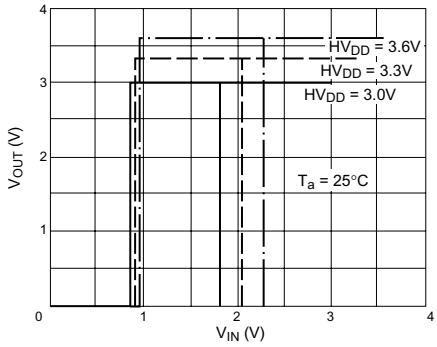


Figure A2-5 Input Characteristics (CMOS Schmitt)

A2.1.2 Input Through Current (3.3 V ± 0.3 V)

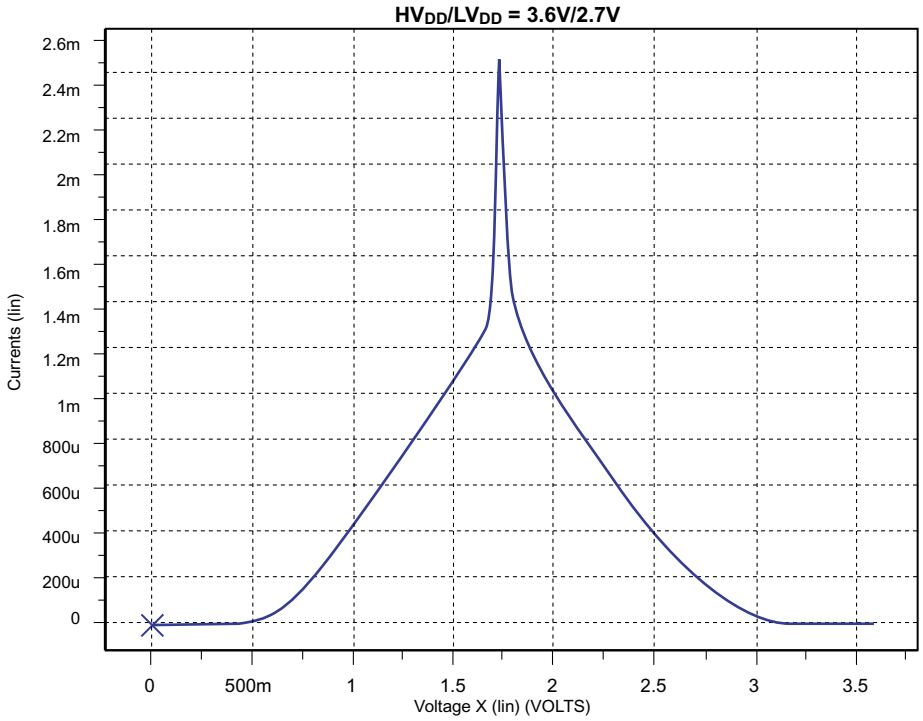


Figure A2-6 Input Through Current (CMOS)

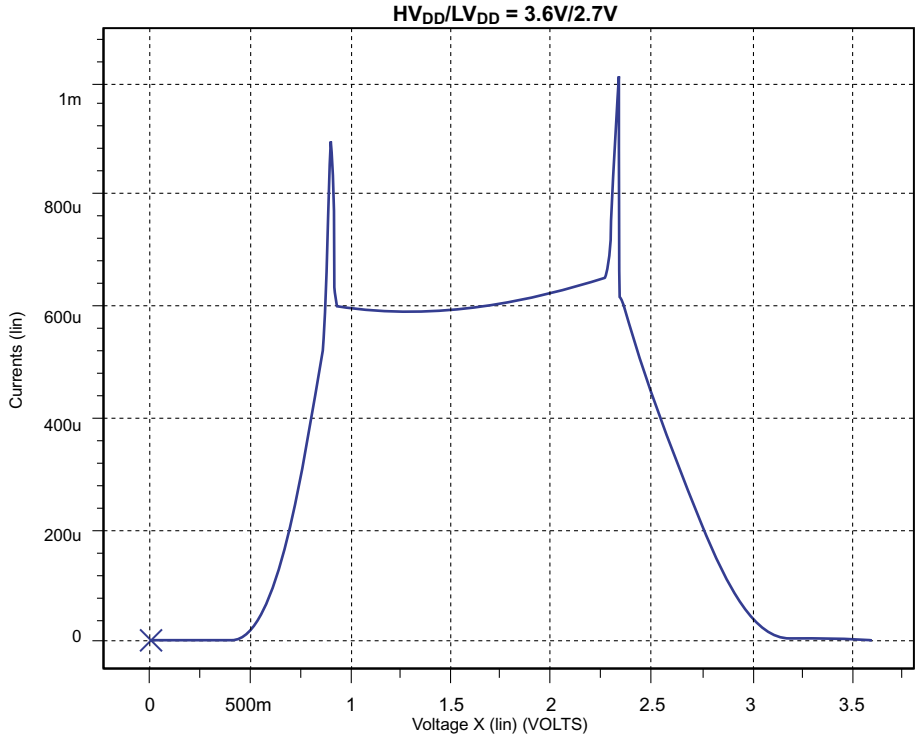


Figure A2-7 Input Through Current (CMOS Schmitt)

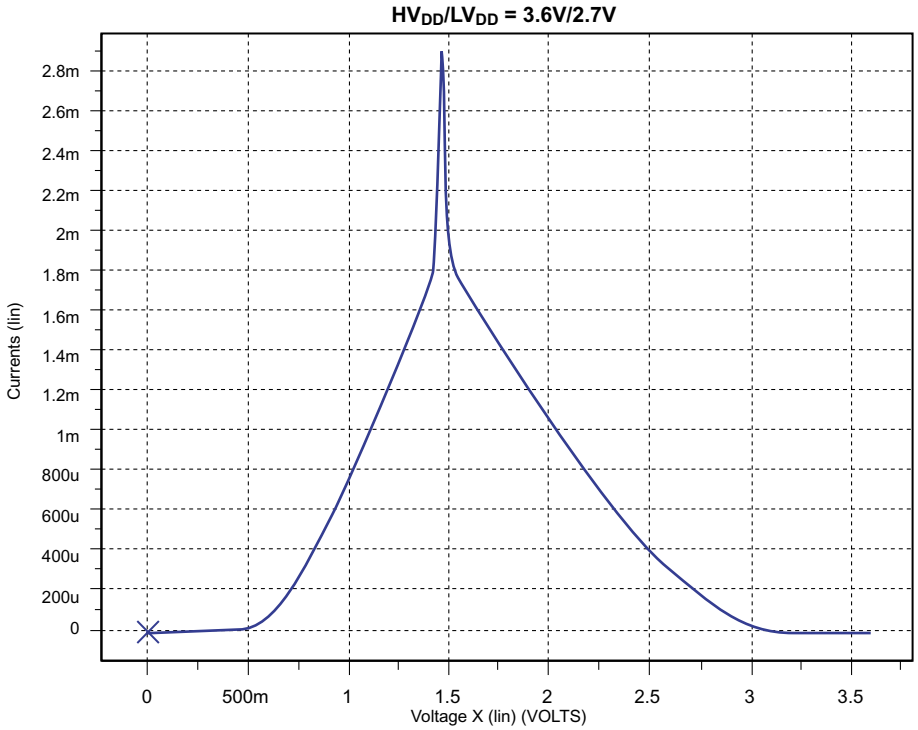


Figure A2-8 Input Through Current (LVTTL)

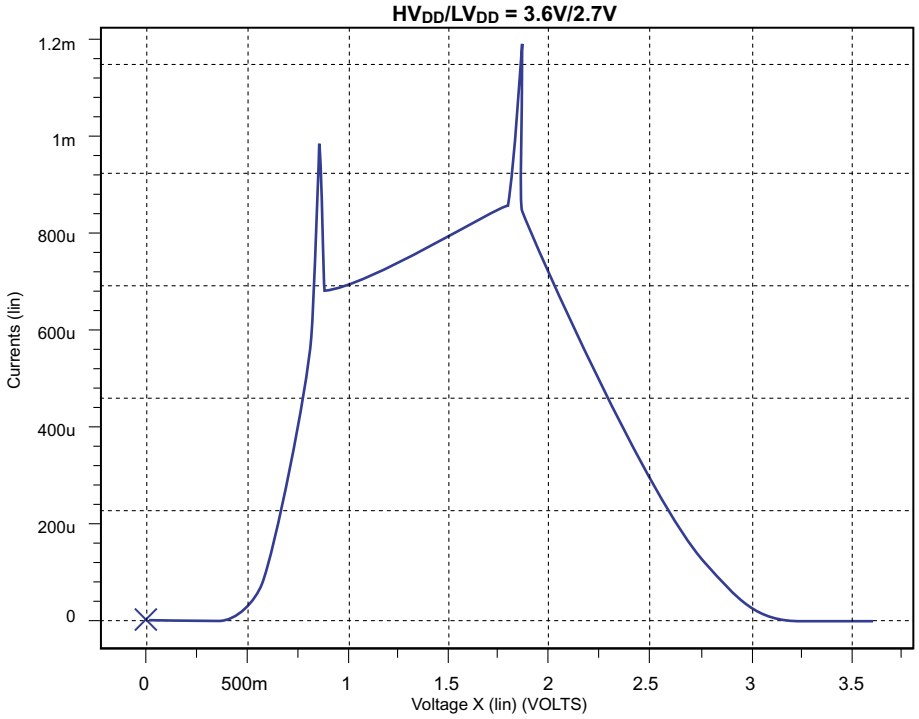


Figure A2-9 Input Through Current (LVTTL Schmitt)

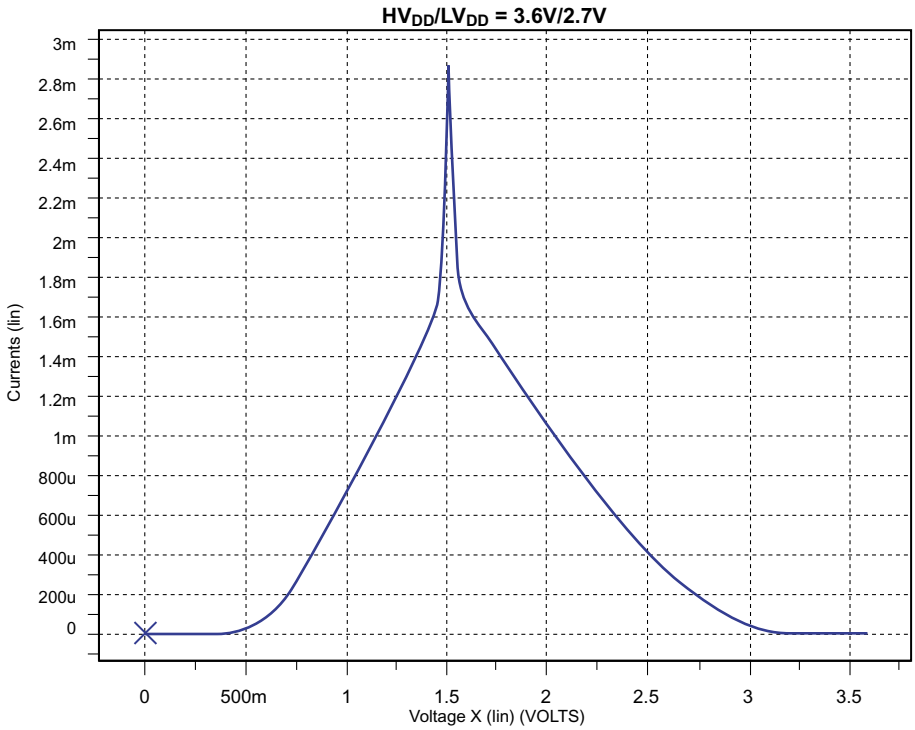


Figure A2-10 Input Through Current (PCI)

A2.1.3 Output Buffer Characteristics (3.3 V ± 0.3 V)

(1) List of output buffer specifications

Table A2-1 Output Current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type S	-0.1	0.1	mA
Type M	-1	1	mA
Type 1	-3	3	mA
Type 2	-6	6	mA
Type 3	-12	12	mA
PCI	Confirmed to the PCI Standard		mA

Note *1: $V_{OH} = HV_{DD} - 0.4$ V (HV_{DD} = 3.3V)

*2: V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

(2) IOL-VOL and IOH-VOH

● IOH-VOL

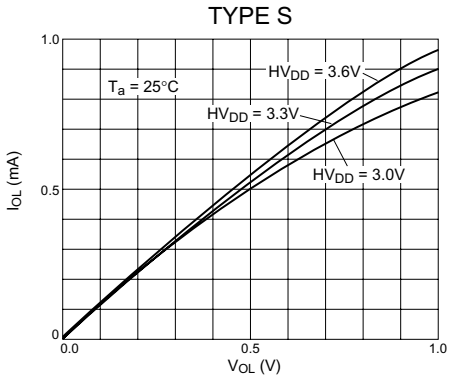


Figure A2-11

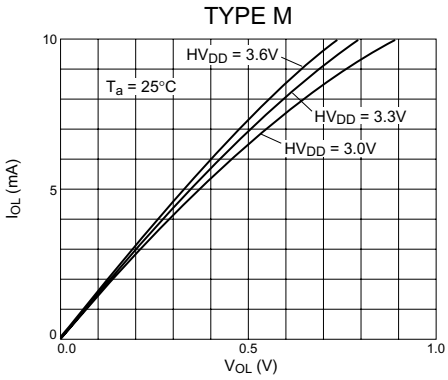


Figure A2-12

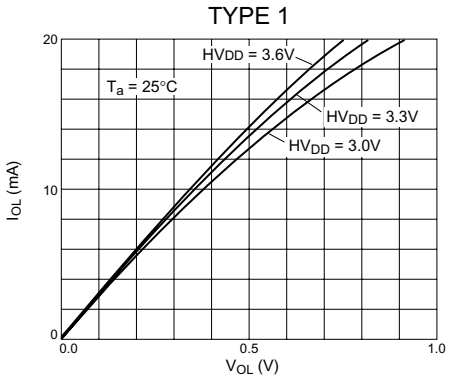


Figure A2-13

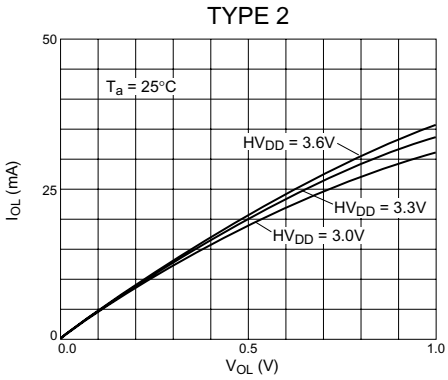


Figure A2-14

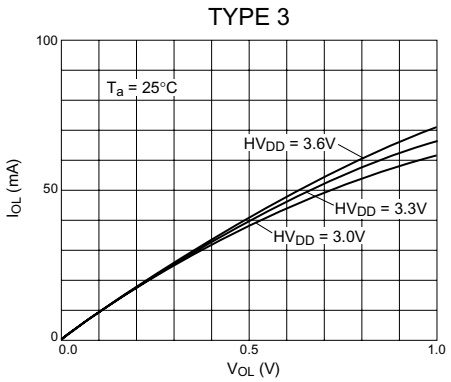


Figure A2-15

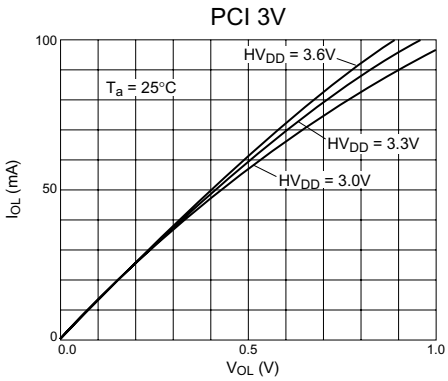


Figure A2-16

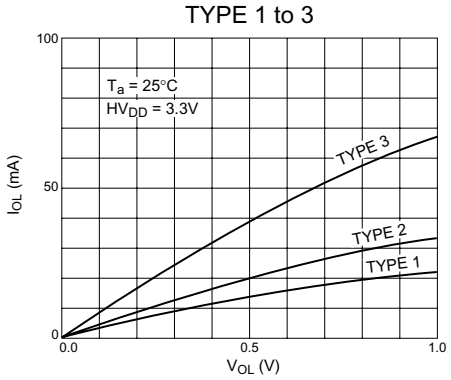


Figure A2-17

- I_{OH}-V_{OH}

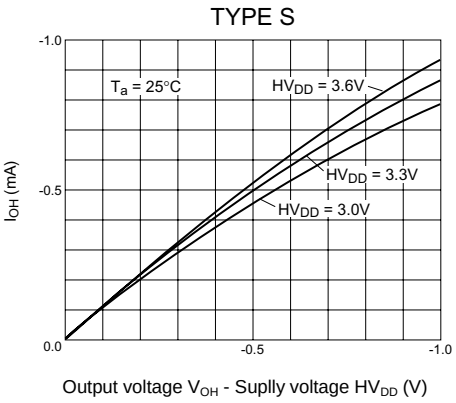


Figure A2-18

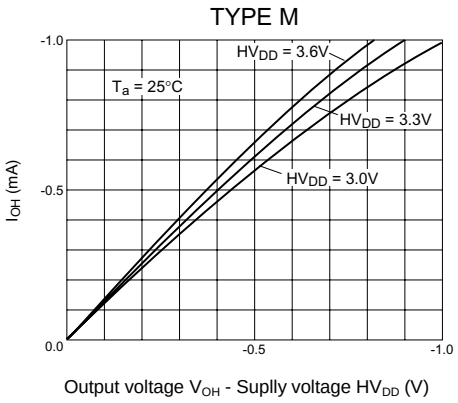


Figure A2-19

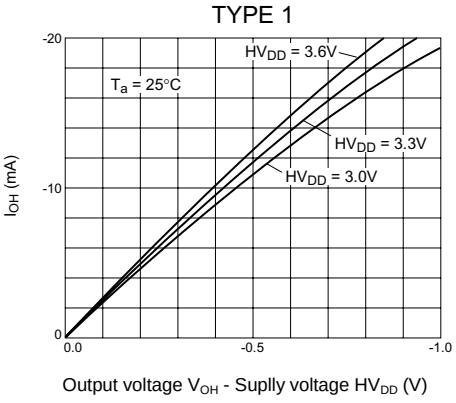


Figure A2-20

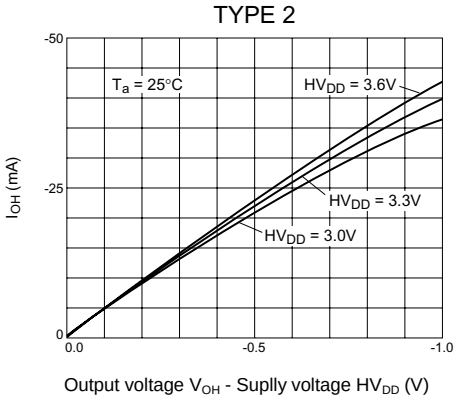


Figure A2-21

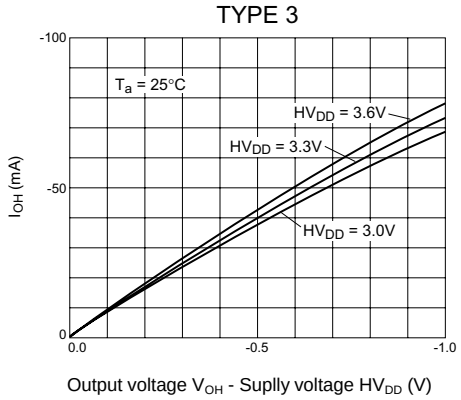


Figure A2-22

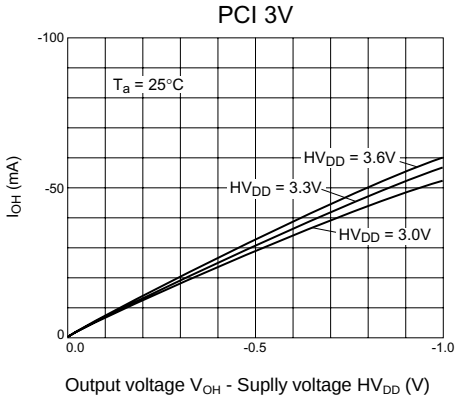


Figure A2-23

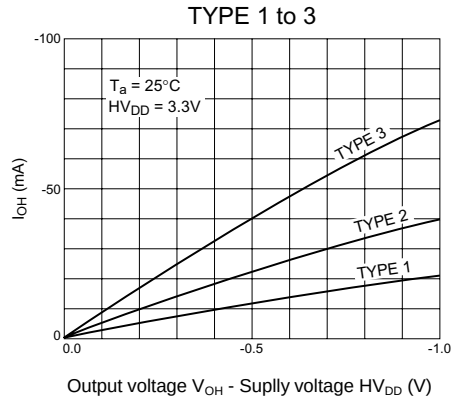


Figure A2-24

(3) I_{OL} and I_{OH} temperature characteristics

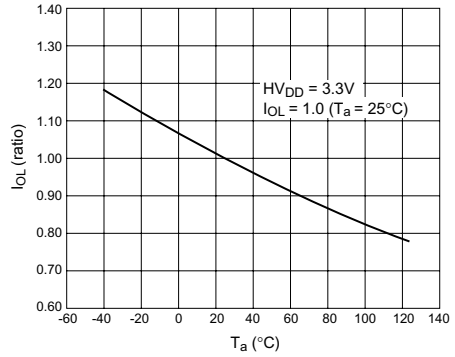


Figure A2-25

Ambient Temperature (T_a) - Output Current (I_{OL})

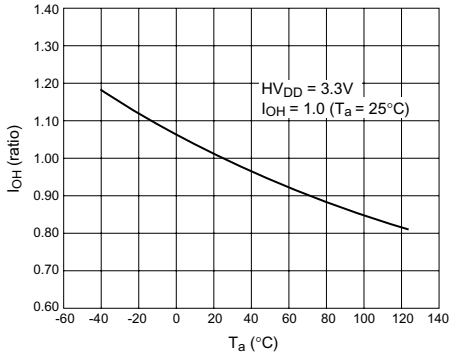


Figure A2-26

Ambient Temperature (T_a) - Output Current (I_{OH})

(4) Output delay time vs. Output load capacitance (C_L)

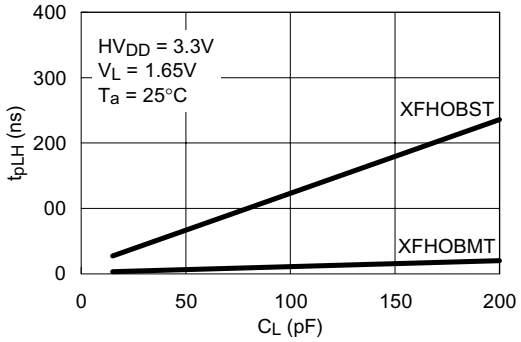


Figure A2-27

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

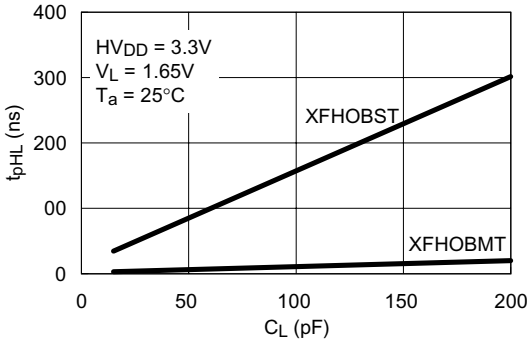


Figure A2-28

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

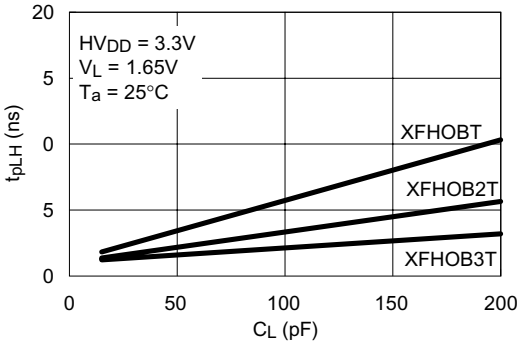


Figure A2-29

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

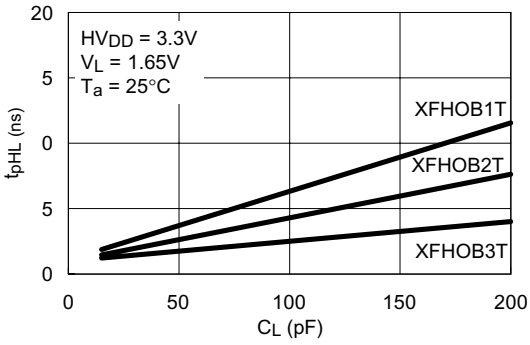


Figure A2-30

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

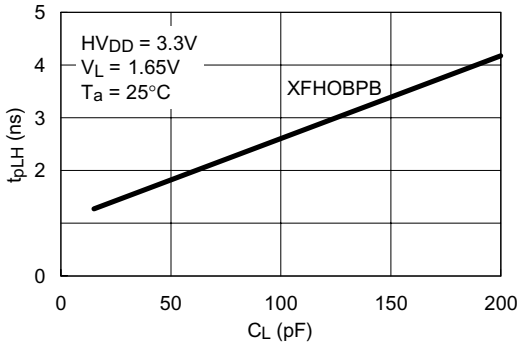


Figure A2-31

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

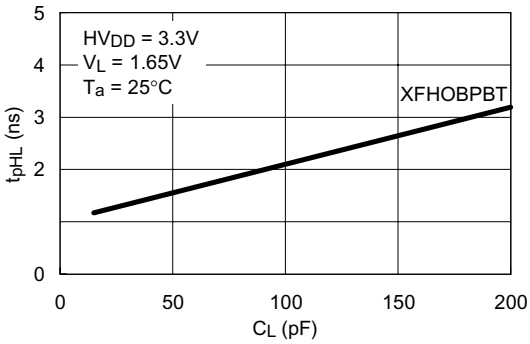


Figure A2-32

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

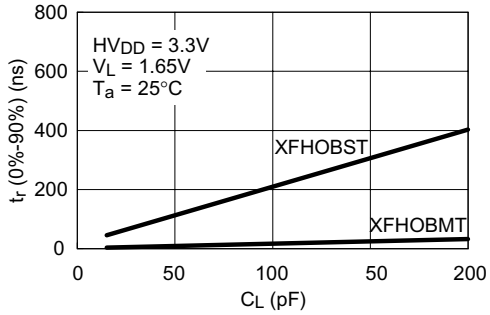


Figure A2-33

Rising Time (t_r) vs. Output Load Capacitance (C_L)

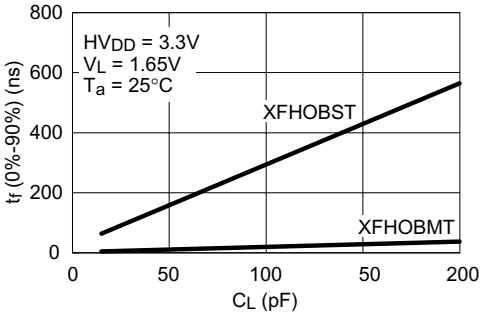


Figure A2-34

Falling Time (t_f) vs. Output Load Capacitance (C_L)

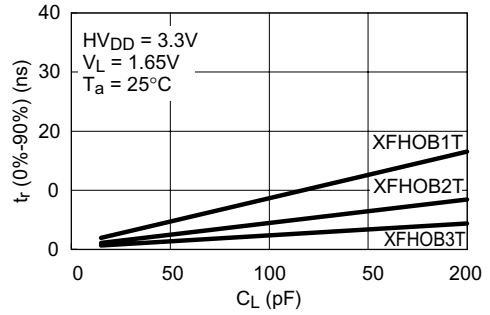


Figure A2-35

Rising Time (t_r) vs. Output Load Capacitance (C_L)

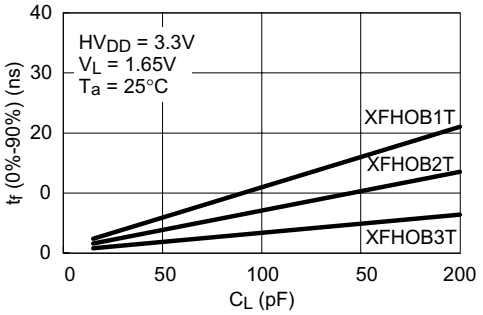


Figure A2-36

Falling Time (t_f) vs. Output Load Capacitance (C_L)

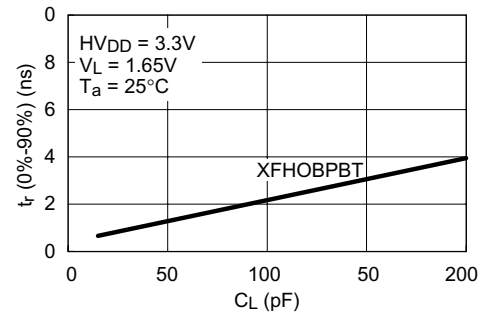


Figure A2-37

Rising Time (t_r) vs. Output Load Capacitance (C_L)

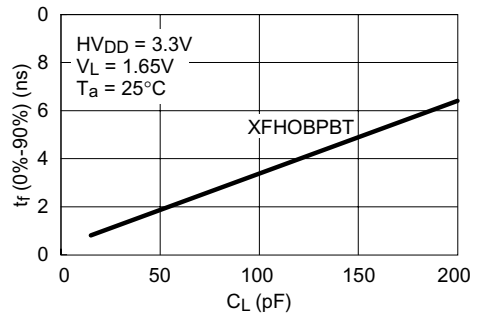


Figure A2-38

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down resistnace

- Pull-up characteristics

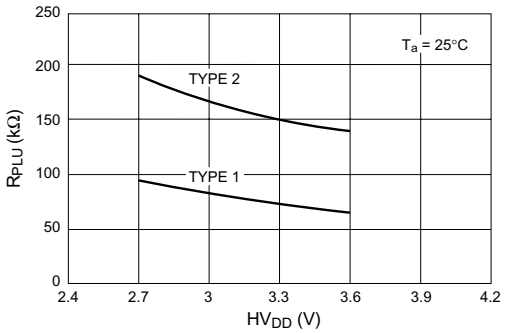


Figure A2-39

Pull-up Resistance (R_{PLU}) vs. HV_{DD}

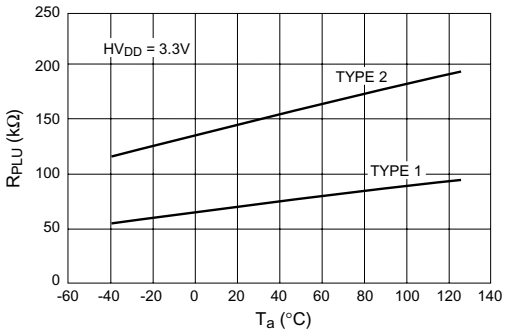


Figure A2-40

Pull-up Resistance (R_{PLU}) vs. Ambient Temperature

- Pull-down characteristics

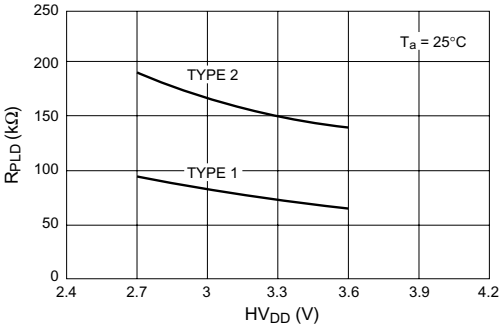


Figure A2-41

Pull-down Resistance (R_{PLD}) vs. HV_{DD}

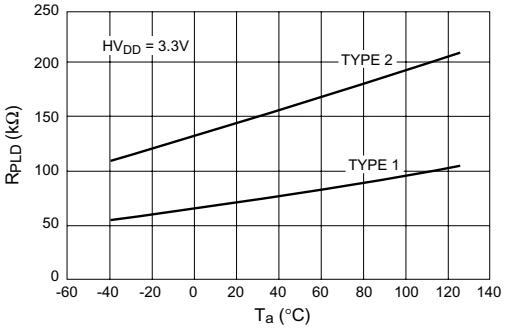


Figure A2-42

Pull-down Resistance (R_{PLD}) vs. Ambient Temperature

(7) Output waveforms

- High Speed Type

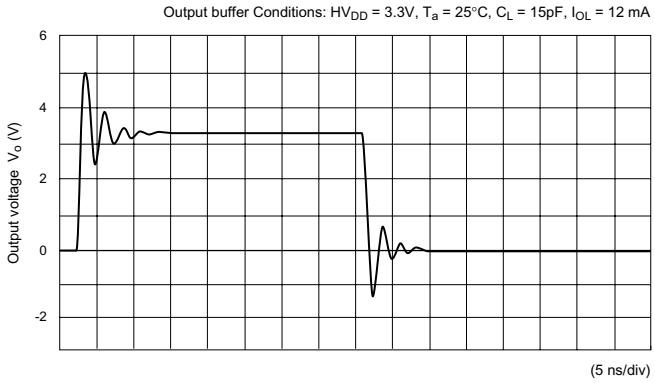


Figure A2-43 Output Waveform (XFHOB3AT)

- Normal Type

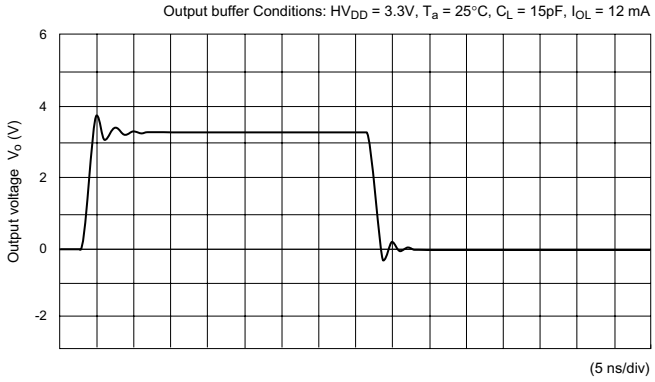


Figure A2-44 Output Waveform (XFHOB3T)

- Low Noise Type

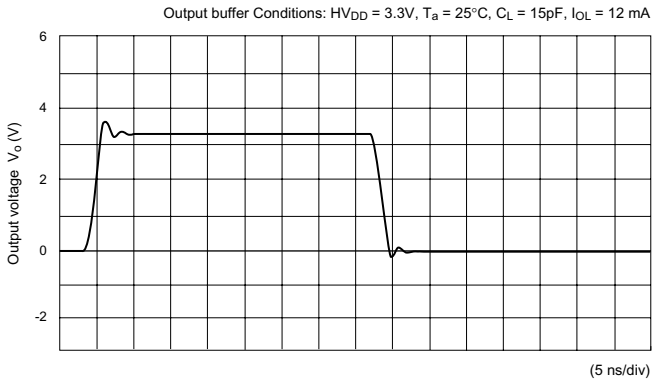


Figure A2-45 Output Waveform (XFHOB3BT)

A2.2 Characteristics of Input/Output Buffers (2.5 V operation)

A2.2.1 Input Buffer Characteristics (2.5 V ± 0.2 V)

- Standard type input buffers

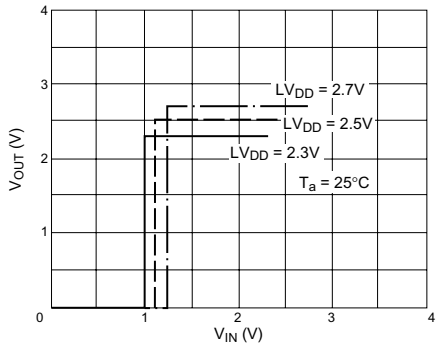


Figure A2-46 Input Characteristics (CMOS)

- Schmitt-trigger type input buffers

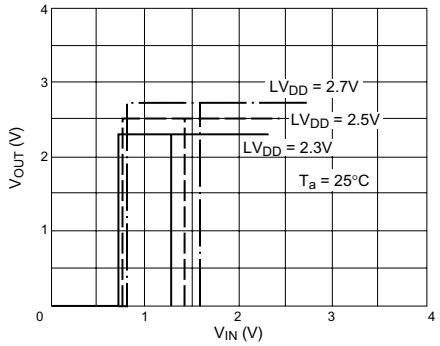


Figure A2-47 Input Characteristics (CMOS Schmitt)

A2.2.2 Input Through Current (2.5 V ± 0.2 V)

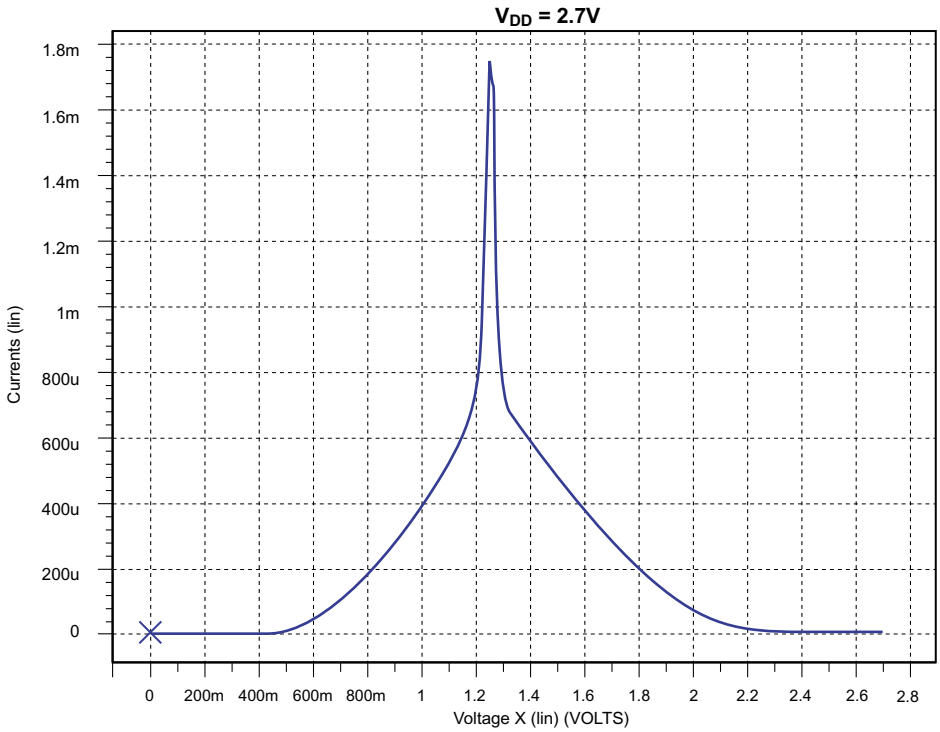


Figure A2-48 Input Through Current (CMOS)

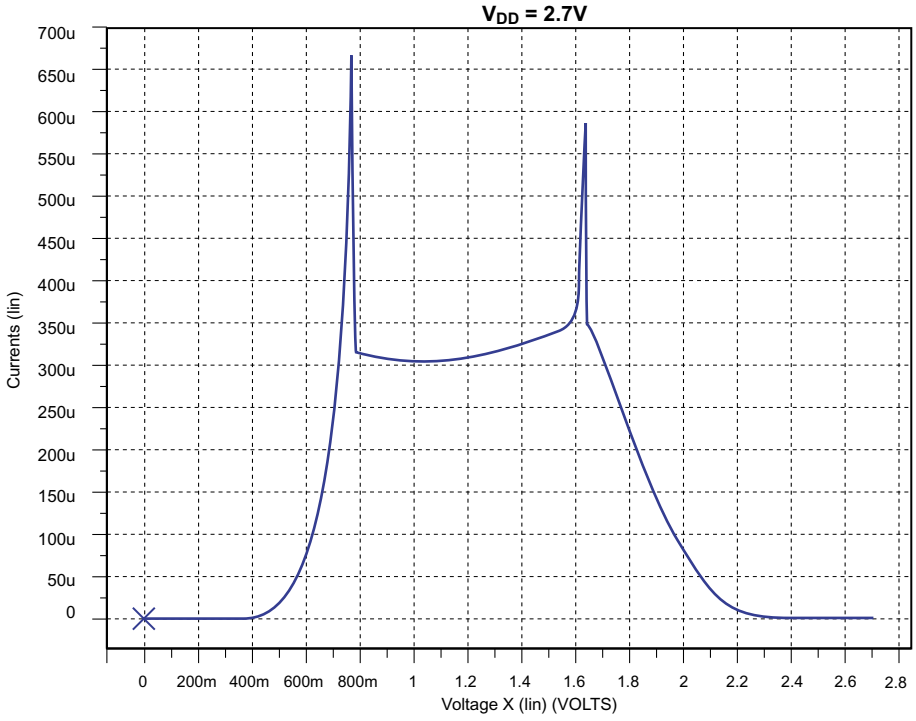


Figure A2-49 Input Through Current (CMOS Schmitt)

A2.2.3 Output Buffer Characteristics (2.5 V ± 0.2 V)

(1) List of output buffer specifications

Table A2-2 Output current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type S	-0.1	0.1	mA
Type M	-1	1	mA
Type 1	-3	3	mA
Type 2	-6	6	mA
Type 3	-9	9	mA

Note *1: $V_{OH} = V_{DD} - 0.4$ V ($V_{DD} = 2.5$ V)

*2: $V_{OL} = 0.4$ V ($V_{DD} = 2.5$ V)

(2) IOL-VOL and IOH-VOH

● IOL-VOL

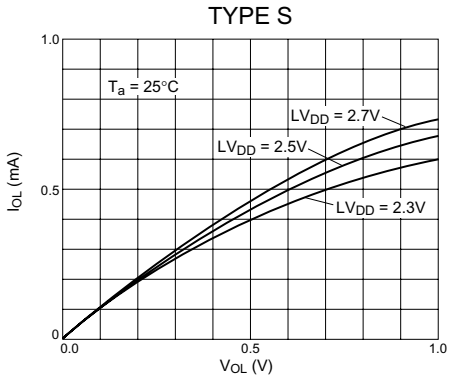


Figure A2-50

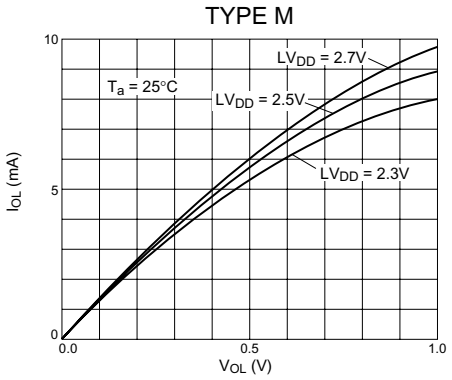


Figure A2-51

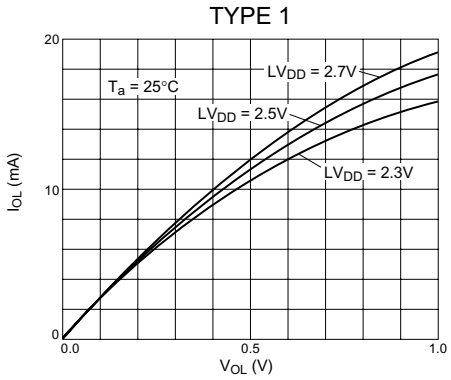


Figure A2-52

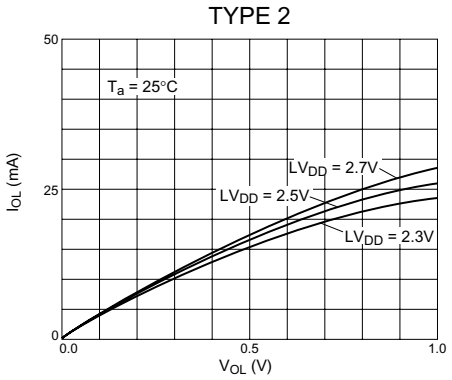


Figure A2-53

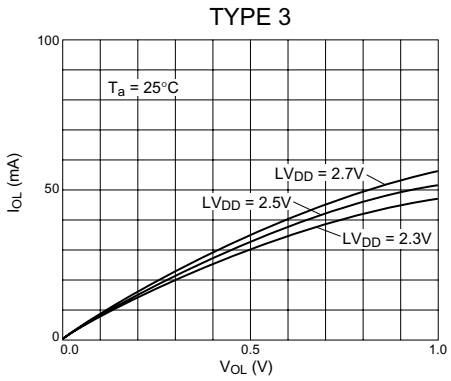


Figure A2-54

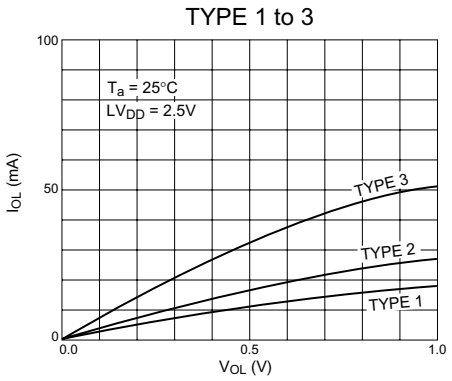


Figure A2-55

● IOH-VOH

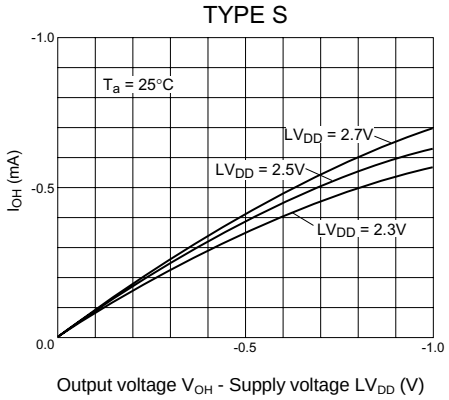


Figure A2-56

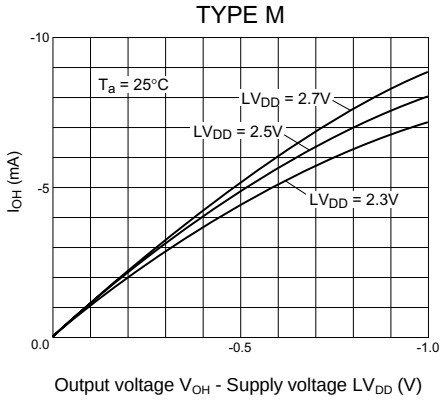


Figure A2-57

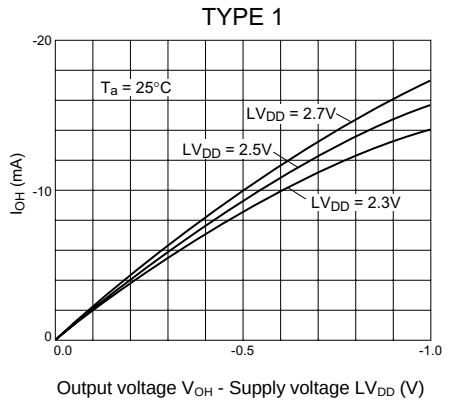


Figure A2-58

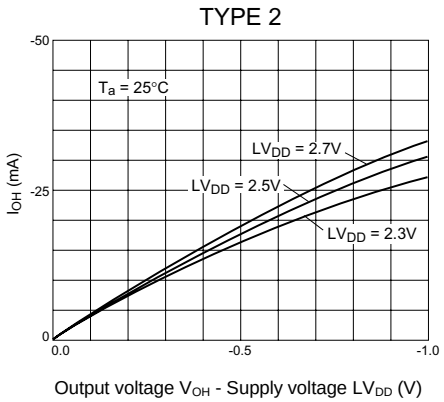


Figure A2-59

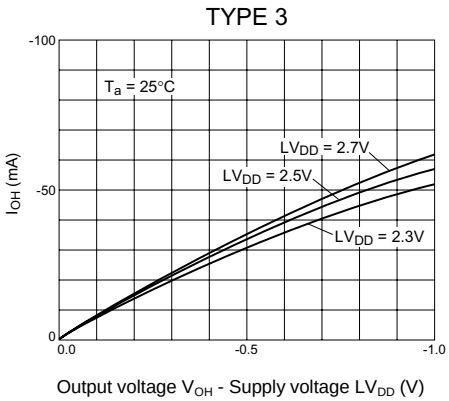
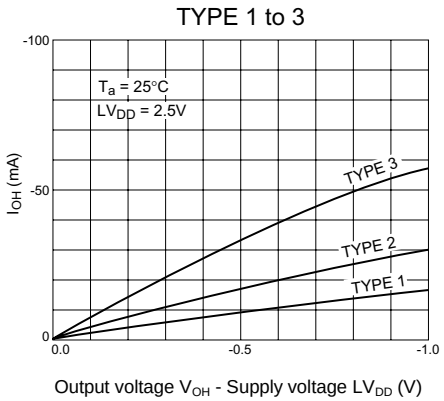


Figure A2-60



A2-61

(3) I_{OL} and I_{OH} temperature characteristics

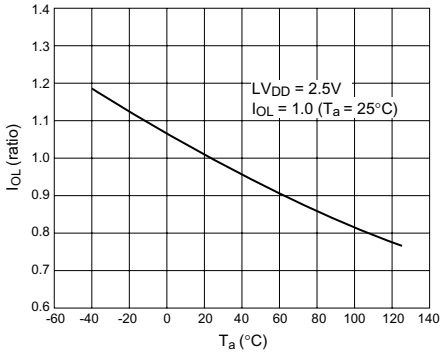


Figure A2-62

Ambient Temperature (T_a) - Output Current (I_{OL})

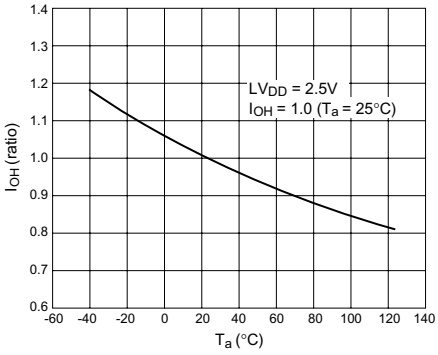


Figure A2-63

Ambient Temperature (T_a) - Output Current (I_{OH})

(4) Output delay time vs. Output load capacitance (C_L)

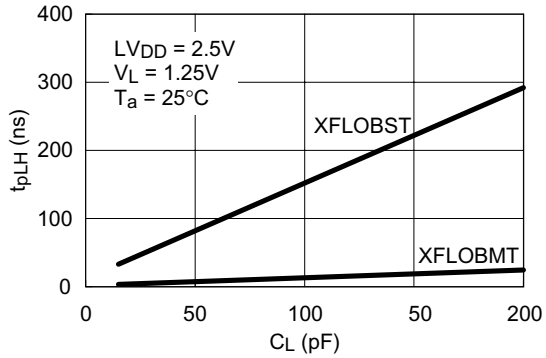


Figure A2-64

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

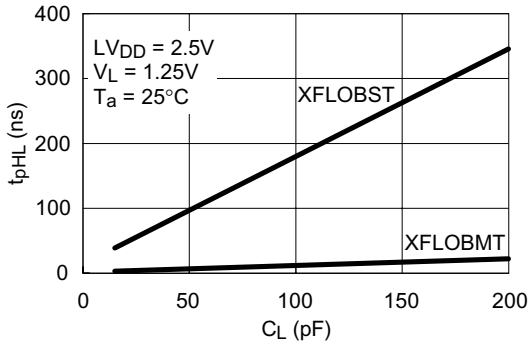


Figure A2-65

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

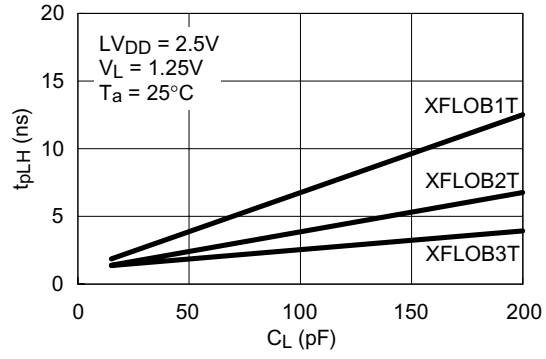


Figure A2-66

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

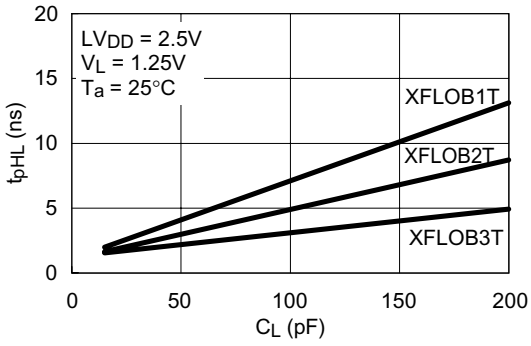


Figure A2-67

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

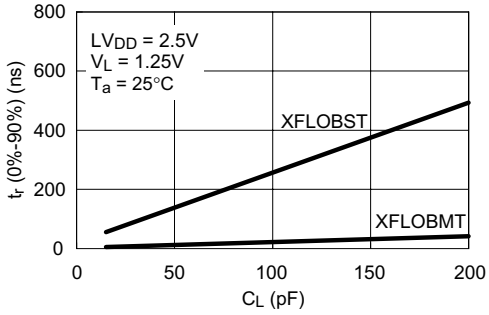


Figure A2-68

Rising Time (t_r) vs. Output Load Capacitance (C_L)

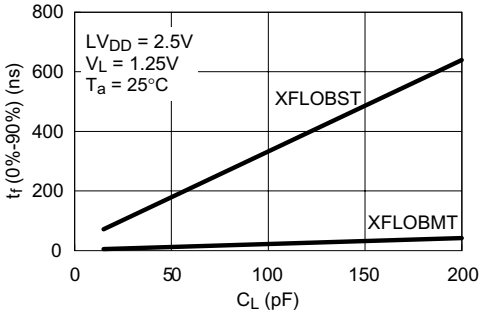


Figure A2-69

Falling Time (t_f) vs. Output Load Capacitance (C_L)

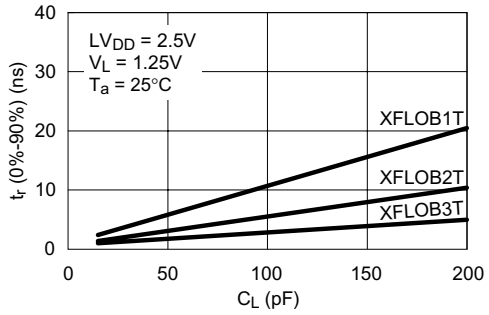


Figure A2-70

Rising Time (t_r) vs. Output Load Capacitance (C_L)

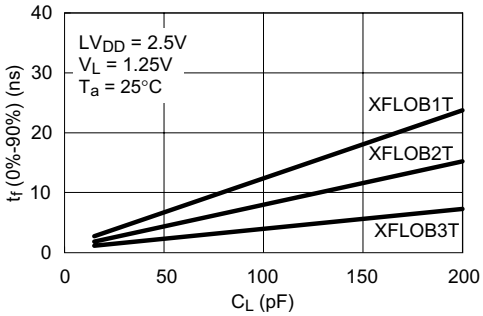


Figure A2-71

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down resistance

● Pull-up characteristics

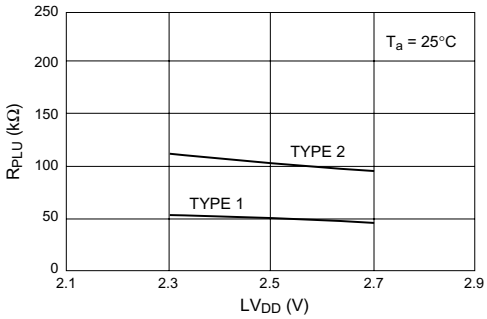


Figure A2-72

Pull-up Resistance (R_{PLU}) vs. LV_{DD}

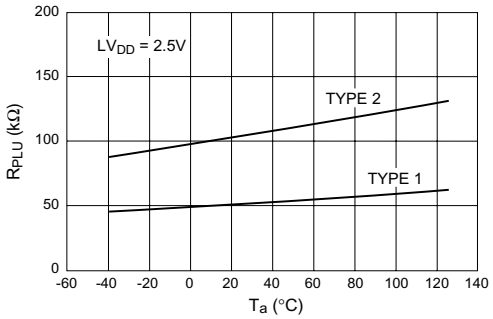


Figure A2-73

Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

● Pull-down characteristics

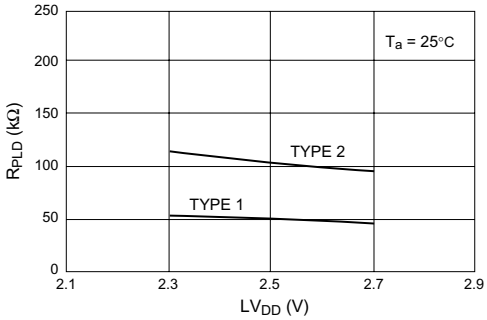


Figure A2-74

Pull-down Resistance (R_{PLD}) vs. LV_{DD}

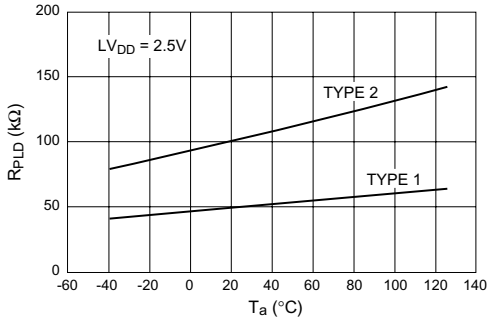


Figure A2-75

Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

(7) Output wavefors

- High Speed Type

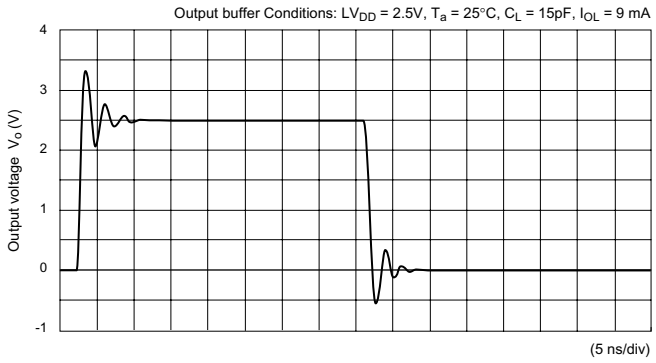


Figure A2-76 Output Waveform (XFLOB3AT)

- Normal Type

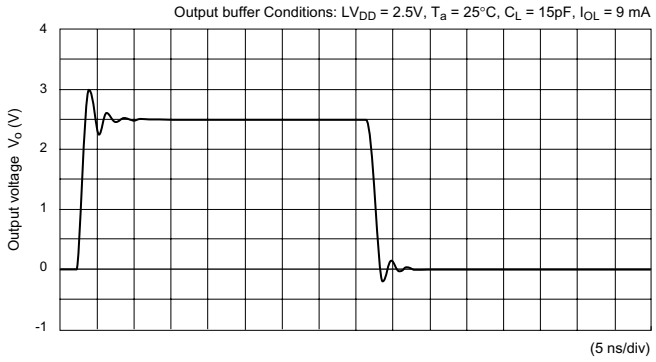


Figure A2-77 Output Waveform (XFLOB3T)

- Low Noise Type

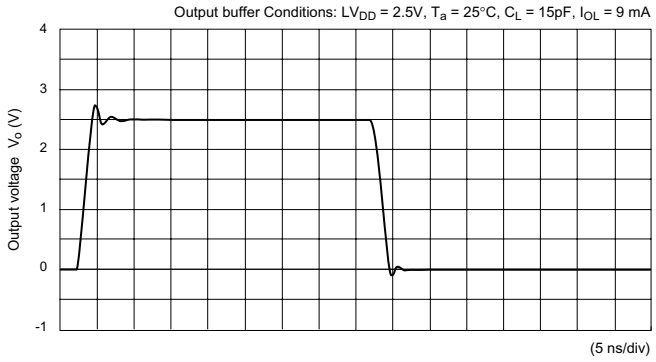


Figure A2-78 Output Waveform (XFLOB3BT)

A2.3 Characteristics of Input/Output Buffers (2.0 V operation)

A2.3.1 Input Buffer Characteristics (2.0 V ± 0.2 V)

- Standard type input buffers

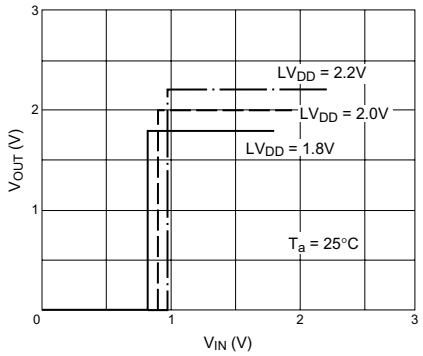


Figure A2-79 Input Characteristics (CMOS)

- Schmitt-trigger type input buffers

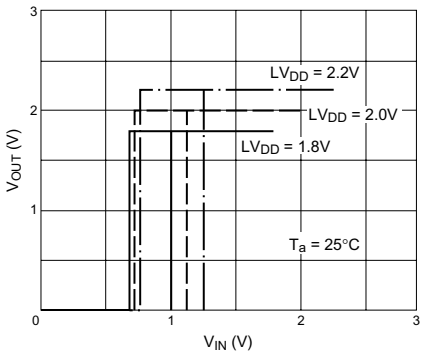


Figure A2-80 Input Characteristics (CMOS Schmitt)

A2.3.2 Input Through Current (2.0 V ± 0.2 V)

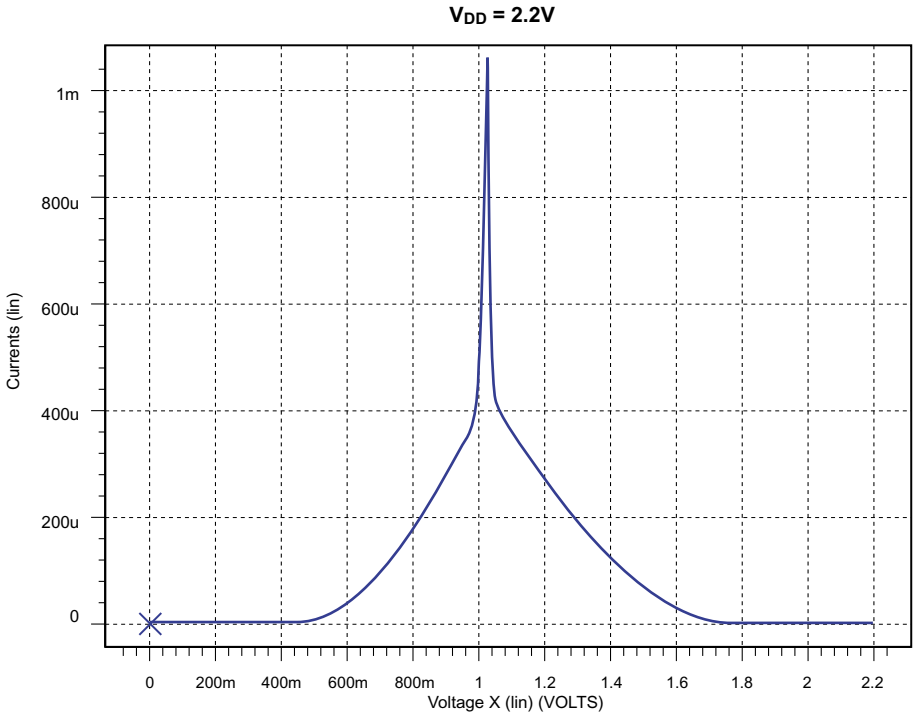


Figure A2-81 Input Through Current (CMOS)

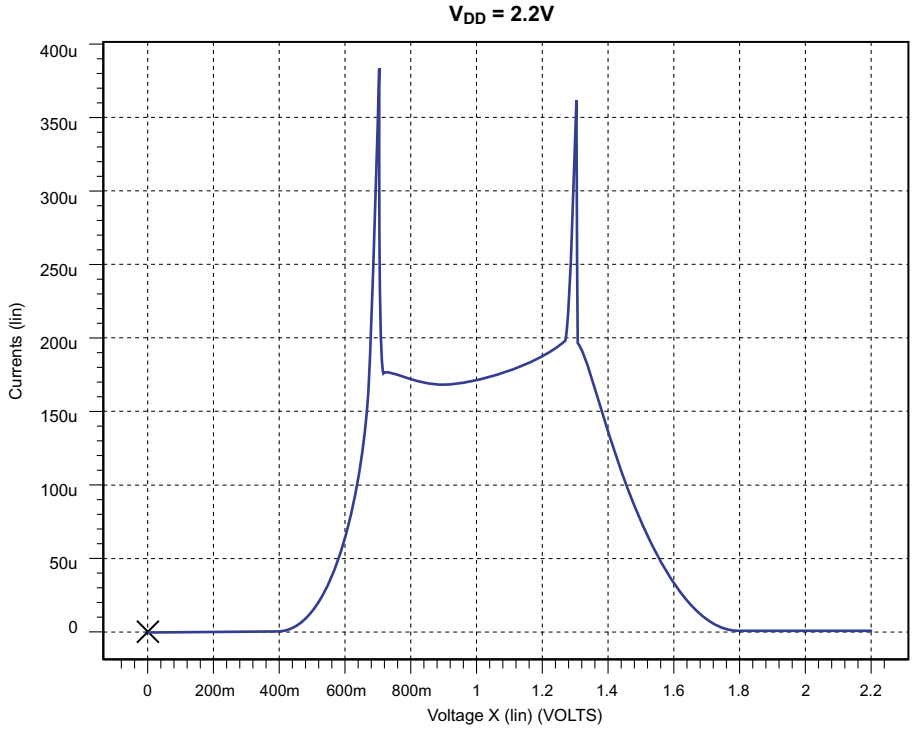


Figure A2-82 Input Through Current (CMOS Schmitt)

A2.3.3 Output Buffer Characteristics (2.0 V ± 0.2 V)

(1) List of output buffer specifications

Table A2-3 Output Current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type S	-0.05	0.05	mA
Type M	-0.3	0.3	mA
Type 1	-1	1	mA
Type 2	-2	2	mA
Type 3	-3	3	mA

Note *1: $V_{OH} = V_{DD} - 0.2$ V ($V_{DD} = 2.0$ V)

*2: $V_{OL} = 0.2$ V ($V_{DD} = 2.0$ V)

(2) I_{OL}-V_{OL} and I_{OH}-V_{OH}

● I_{OL}-V_{OL}

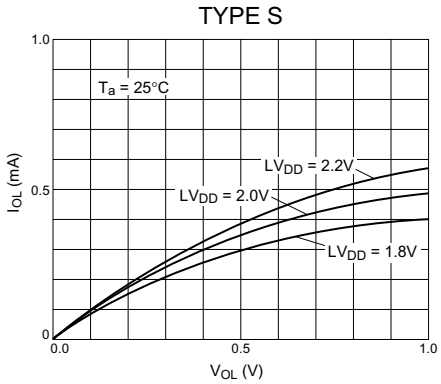


Figure A2-83

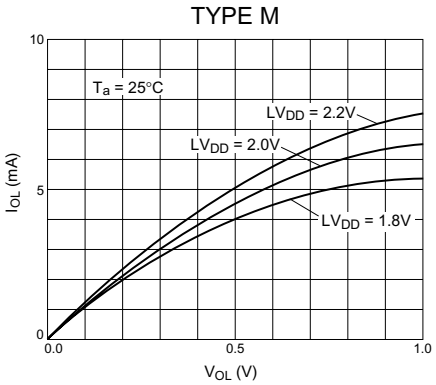


Figure A2-84

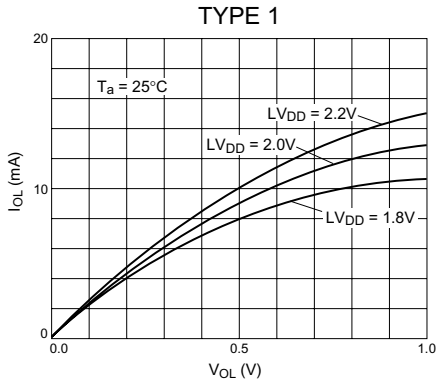


Figure A2-85

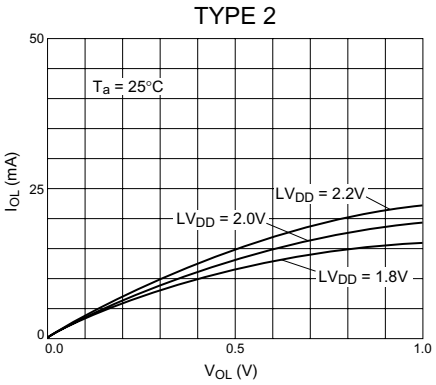


Figure A2-86

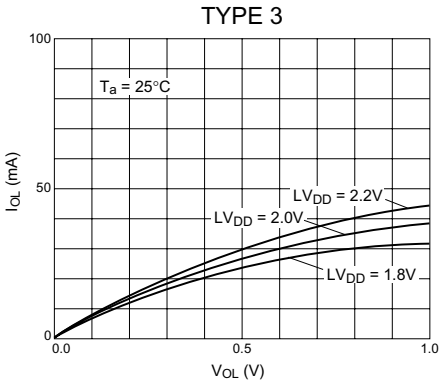


Figure A2-87

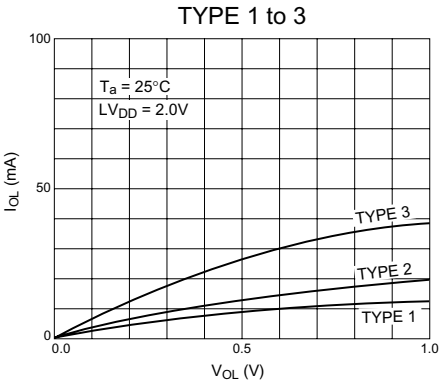


Figure A2-88

● IOH-VOH

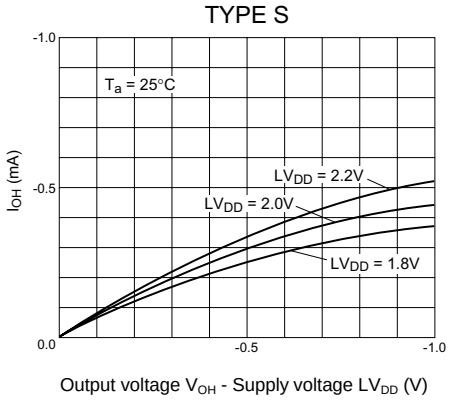


Figure A2-89

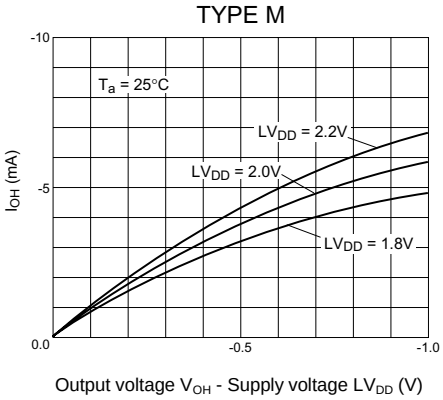


Figure A2-90

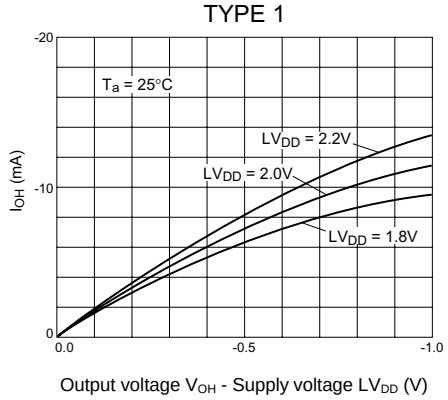


Figure A2-91

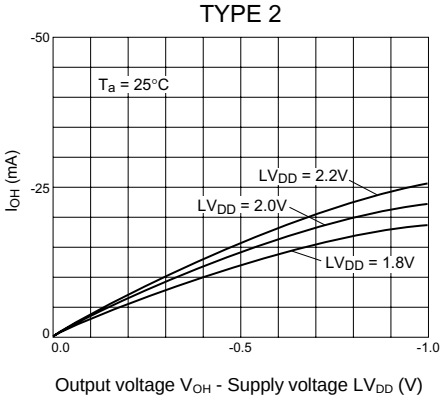


Figure A2-92

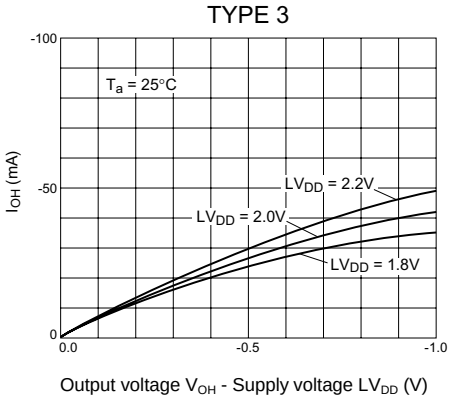


Figure A2-93

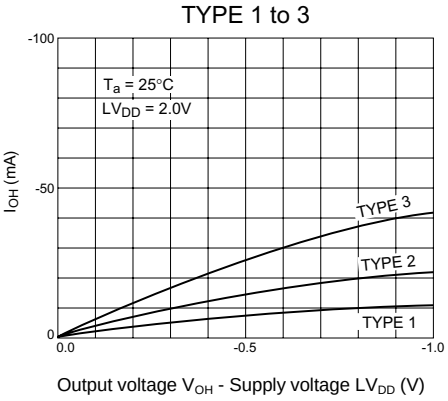


Figure A2-94

(3) I_{OL} and I_{OH} temperature characteristics

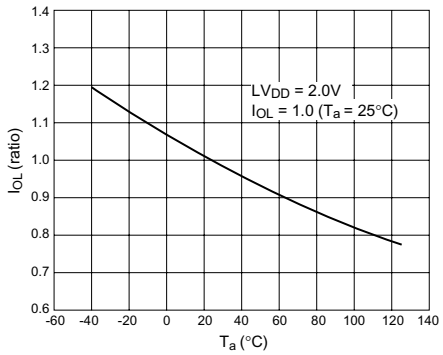


Figure A2-95

Ambient Temperature (T_a) - Output Current (I_{OL})

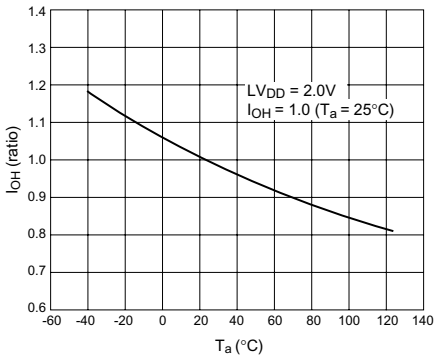


Figure A2-96

Ambient Temperature (T_a) - Output Current (I_{OH})

(4) Output delay time vs. Output load capacitance (C_L)

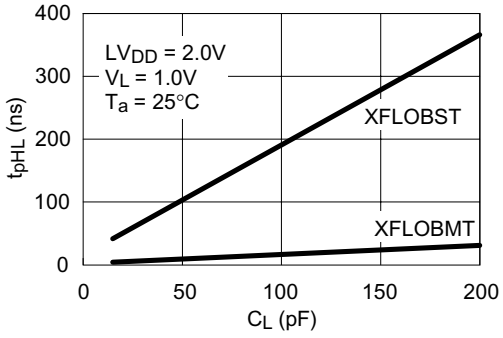


Figure A2-97

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

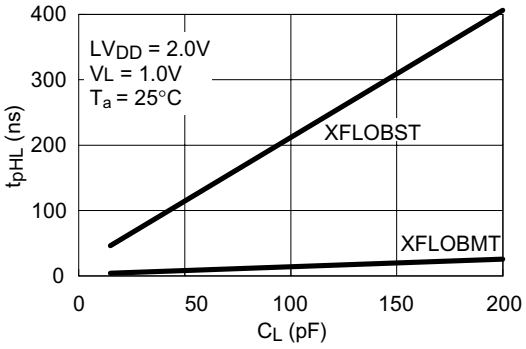


Figure A2-98

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

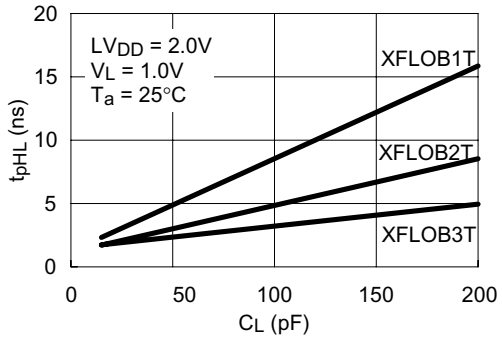


Figure A2-99

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

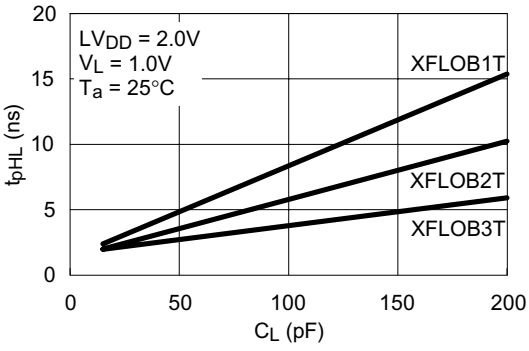


Figure A2-100

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

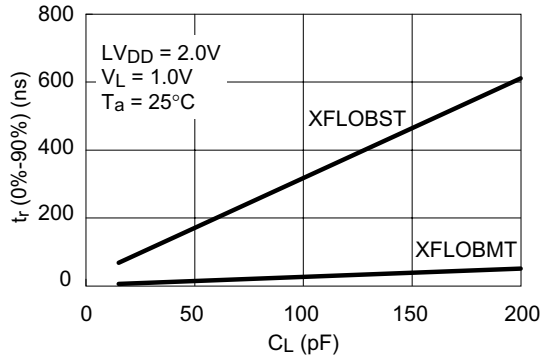


Figure A2-101

Rising Time (t_r) vs. Output Load Capacitance (C_L)

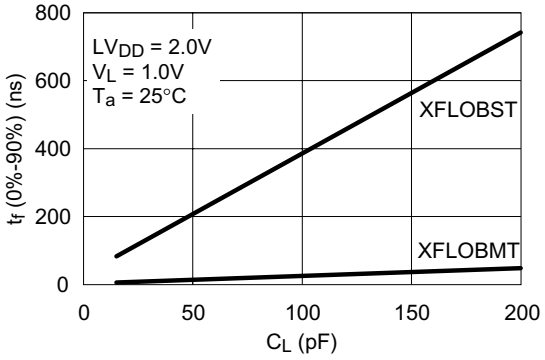


Figure A2-102

Falling Time (t_f) vs. Output Load Capacitance (C_L)

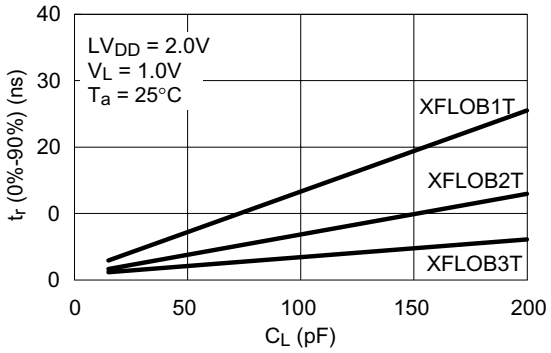


Figure A2-103

Rising Time (t_r) vs. Output Load Capacitance (C_L)

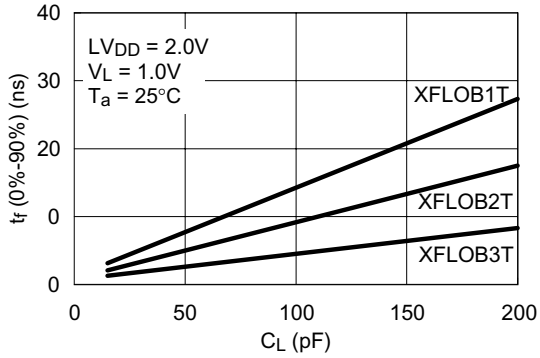


Figure A2-104

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down resistance

● Pull-up characteristics

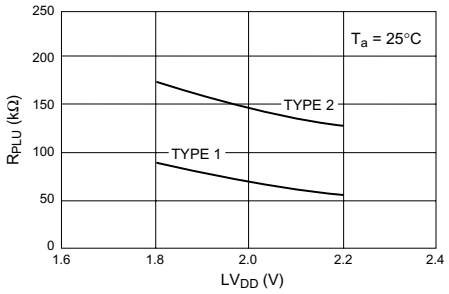


Figure A2-105

Pull-up Resistance (R_{PLU}) vs. LV_{DD}

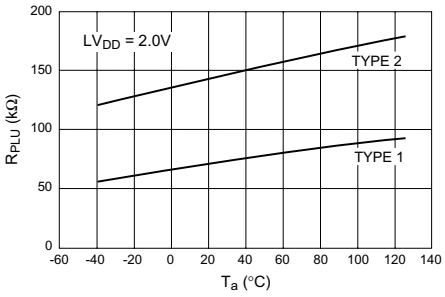


Figure A2-106

Pulll-up Resistance (R_{PLU}) vs. Ambient Temperature

● Pull-down characteristics

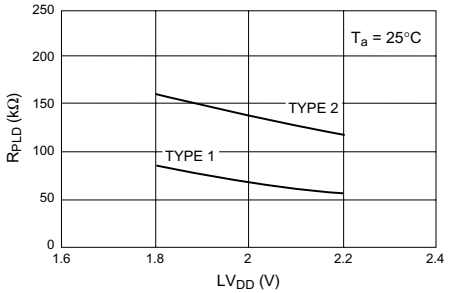


Figure A2-107

Pull-down Resistance (R_{PLD}) vs. LV_{DD}

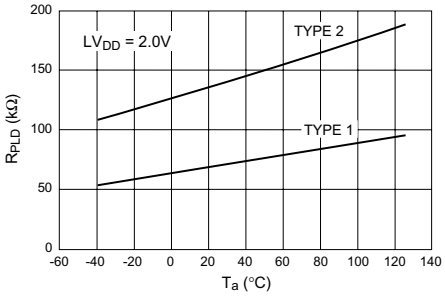


Figure A2-108

Pulll-down Resistance (R_{PLD}) vs. Ambient Temperature

(7) Output waveforms

- High Speed Type

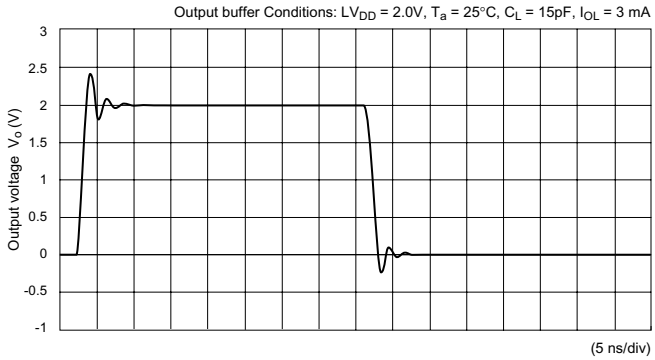


Figure A2-109 Output Waveform (XFLOB3AT)

- Normal Type

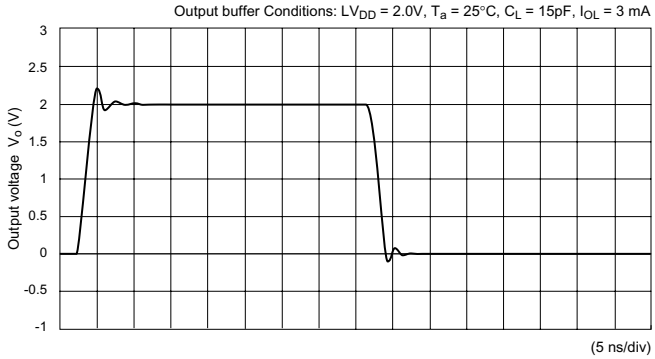


Figure A2-110 Output Waveform (XFLOB3T)

- Low Noise Type

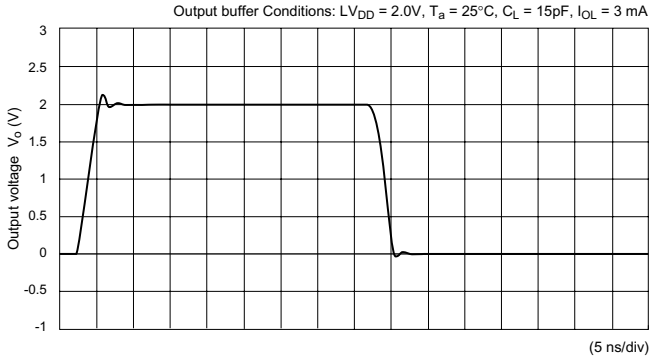


Figure A2-111 Output Waveform (XFLOB3BT)

A2.4 Characteristics of Input/Output Buffers (5 V Tolerant Fail-Safe Cell)

A2.4.1 Input Buffer Characteristics (3.3 V ± 0.3 V)

The input buffers comprised of 5 V tolerant Fail-Safe cells of the S1X60000 series exhibit the same characteristics as normal input buffers. Therefore, see Appendix 2.1.1, "Input Buffer Characteristics (3.3 V ± 0.3 V)."

A2.4.2 Input Through Current (3.3 V ± 0.3 V)

The input buffers comprised of 5 V tolerant Fail-Safe cells of the S1X60000 series exhibit the same characteristics as normal input buffers. Therefore, see Appendix 2.1.2, "Input Through Current (3.3 V ± 0.3 V)."

A2.4.3 Output Buffer Characteristics (3.3 V ± 0.3 V)

The 5 V tolerant Fail-Safe cells of the S1X60000 series include a control circuit (like the one shown in Figure A2-112) to enable 5 V interfacing. Therefore, note that the I_{OL} and I_{OH} characteristics of these cells differ from those of normal cells.

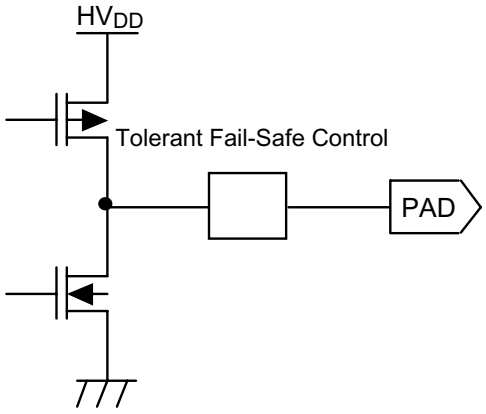


Figure A2-112 Output Buffer Structure of 5 V Tolerant Fail-Safe Cell

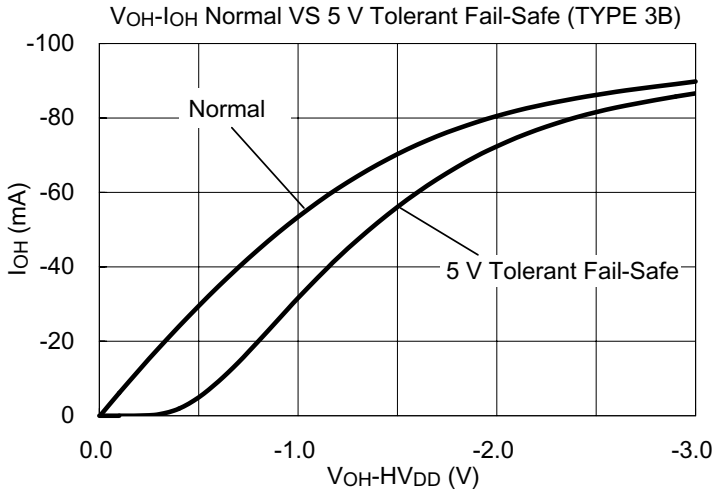


Figure A2-113 Comparison between 5 V Tolerant Fail-Safe Cells and Normal Cells

(1) List of output buffer specifications

Table A2-4 Output Current Characteristics

Type number	Output current		Unit
	I_{OH}*1	I_{OL}*2	
Type 1	-3	3	mA
Type 2	-6	6	mA
Type 3	-12	12	mA

Note *1: $V_{OH} = HV_{DD}$ - 1.0 V (HV_{DD} = 3.3 V)

*2: V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

(2) I_{OL}-V_{OL} and I_{OH}-V_{OH}

- I_{OL}-V_{OL}

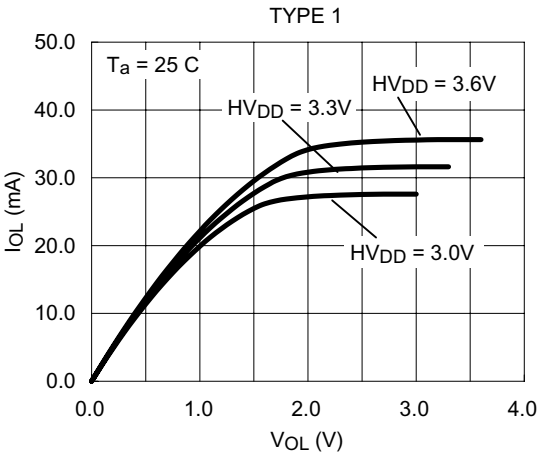


Figure A2-114

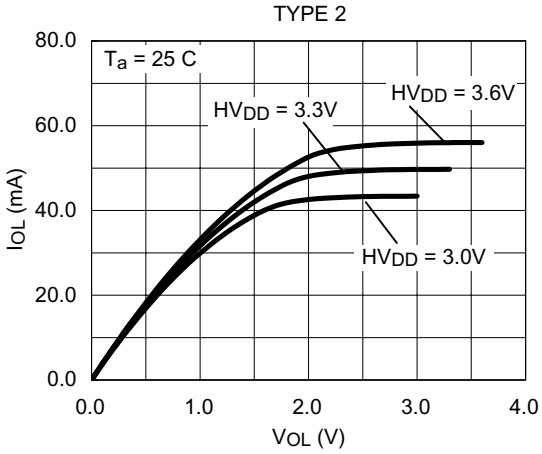


Figure A2-115

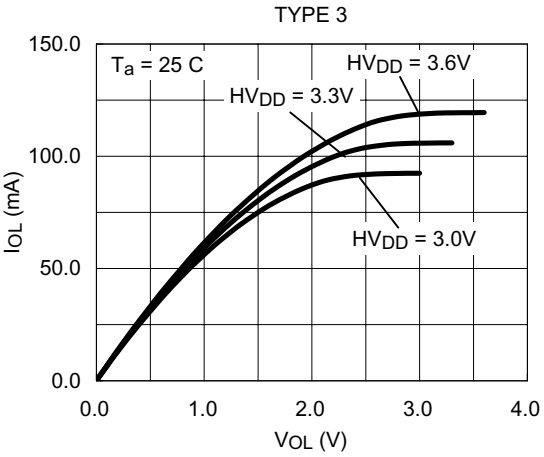


Figure A2-116

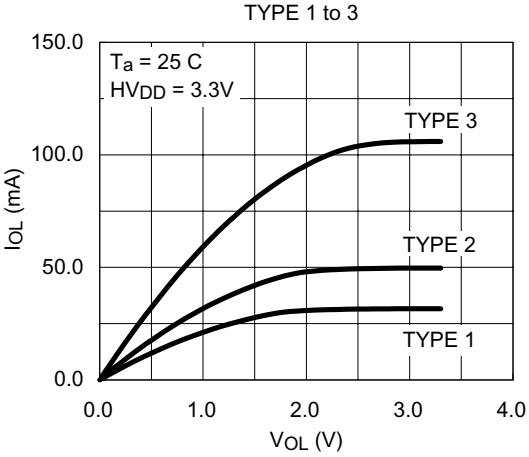


Figure A2-117

● IOH-VOH

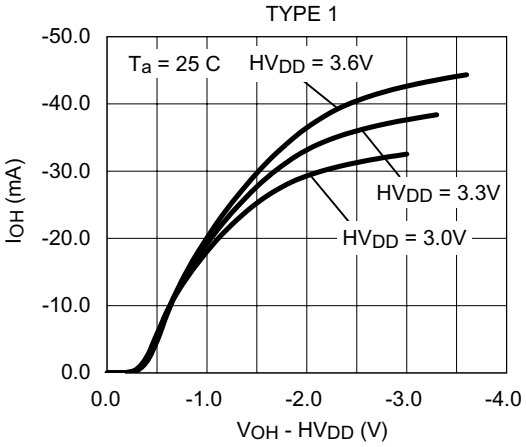


Figure A2-118

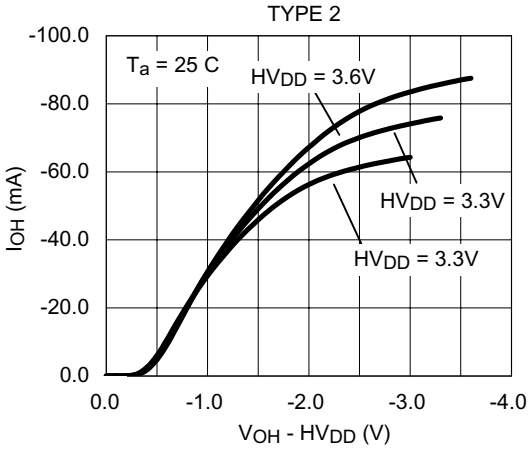


Figure A2-119

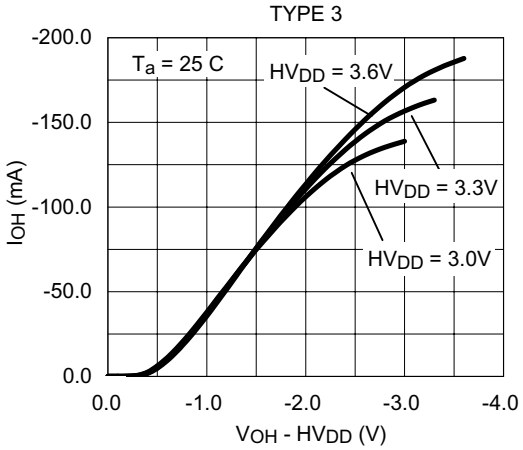


Figure A2-120

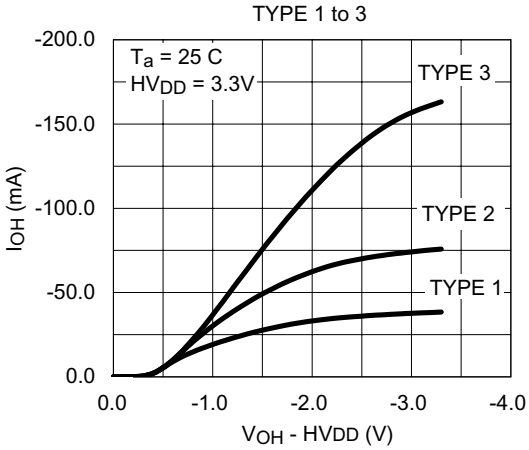


Figure A2-121

(3) I_{OL} and I_{OH} temperature characteristics

Because the temperature characteristics of I_{OL} and I_{OH} are the same as those of output buffers comprised of normal cells, see (3) Temperature Characteristics of I_{OL} and I_{OH} in Appendix 2.1.3, "Output Buffer Characteristics (3.3 V ± 0.3 V)."

(4) Output delay time vs. Output load capacitance (C_L)

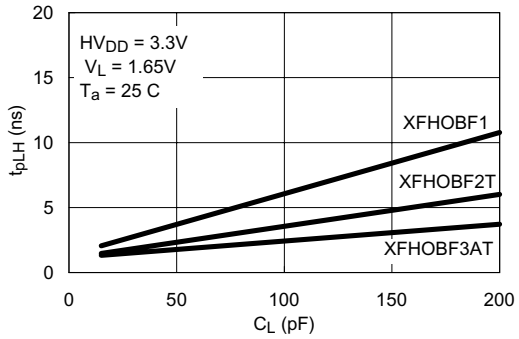


Figure A2-122

Output Delay Time (t_{pLH}) vs. Output Load Capacitance (C_L)

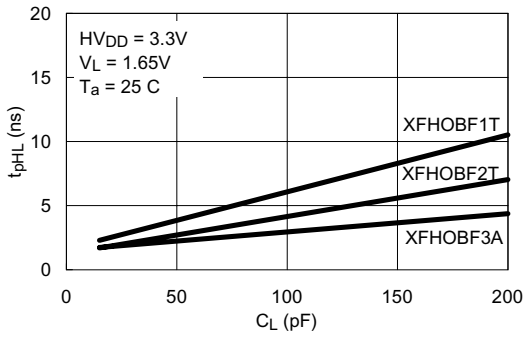


Figure A2-123

Output Delay Time (t_{pHL}) vs. Output Load Capacitance (C_L)

(5) Output buffer rising/falling time vs. Output load capacitance (C_L)

The 5 V tolerant Fail-Safe cells of the S1X60000 series include a control circuit (like the one shown in Figure A2-124) to enable 5 V interfacing. Therefore, note that the t_r and t_f characteristics of these cells differ from those of normal cells.

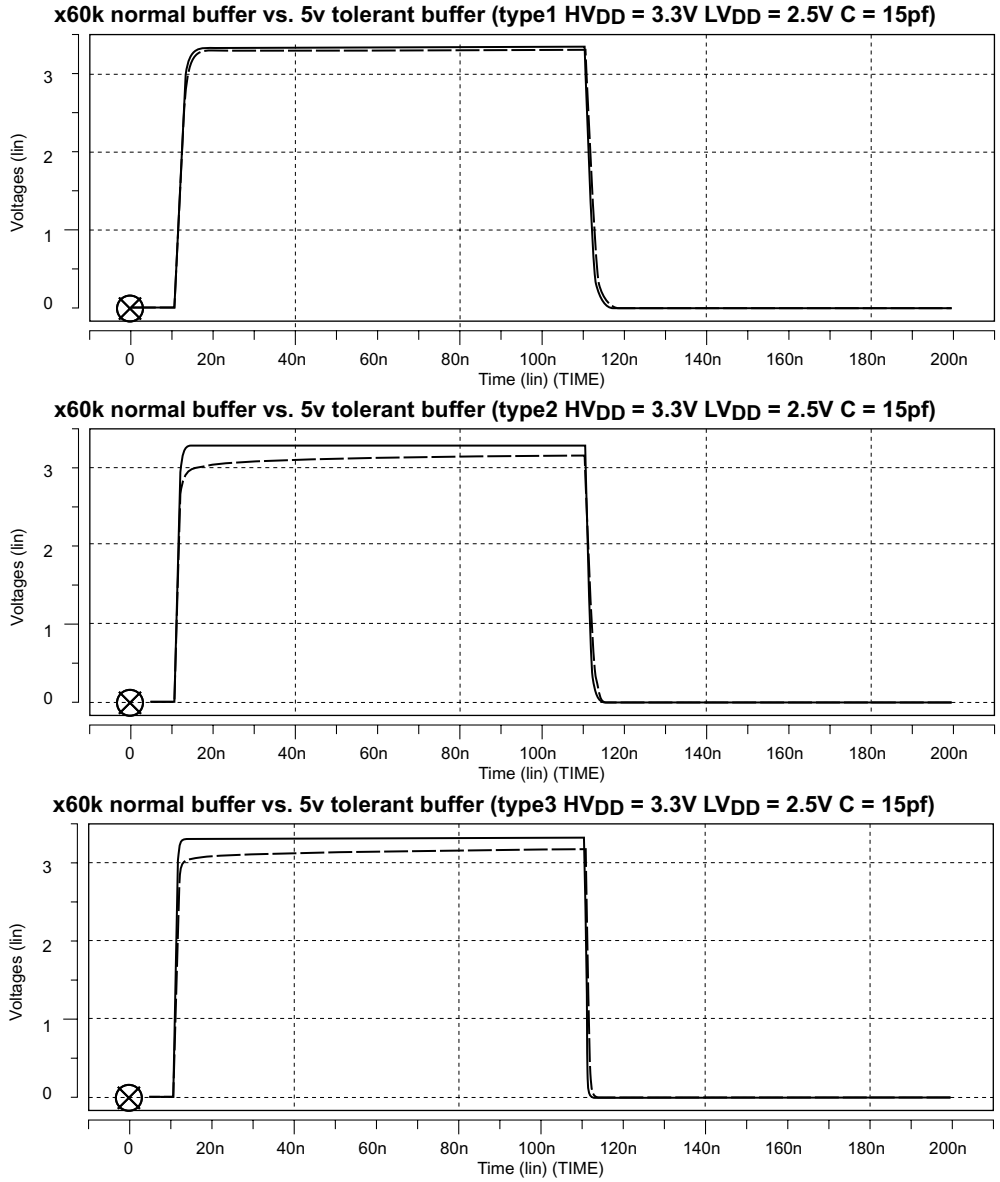


Figure A2-124 Comparison between 5 V Tolerant Fail-Safe Cells and Normal Cells

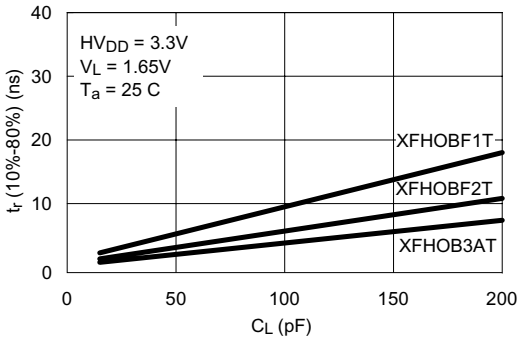


Figure A2-125

Rising Time (t_r) vs. Output Load Capacitance (C_L)

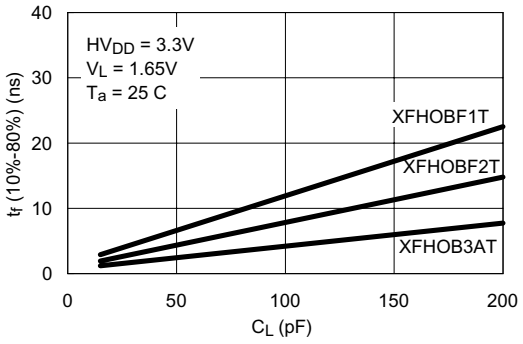


Figure A2-126

Falling Time (t_f) vs. Output Load Capacitance (C_L)

(6) Pull-up and pull-down characteristics

Because the pull-up/pull-down characteristics are the same as those of output buffers comprised of normal cells, see (6) Pull-up/Pull-down characteristics in Appendix 2.1.3, “Output Buffer Characteristics (3.3 V ± 0.3 V).”

(7) Output waveforms

- High Speed

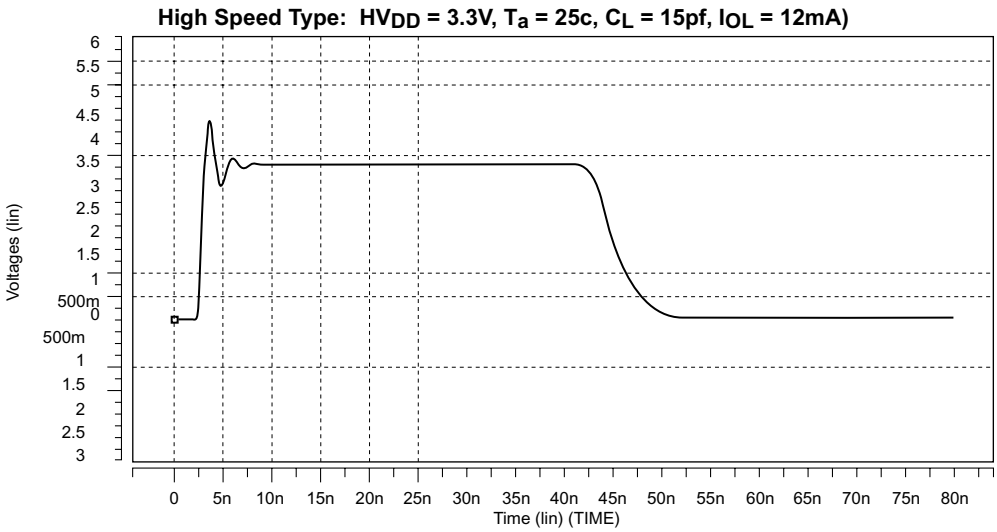


Figure A2-127 Output Waveform (XFHOBF3AT)

- Low Noise

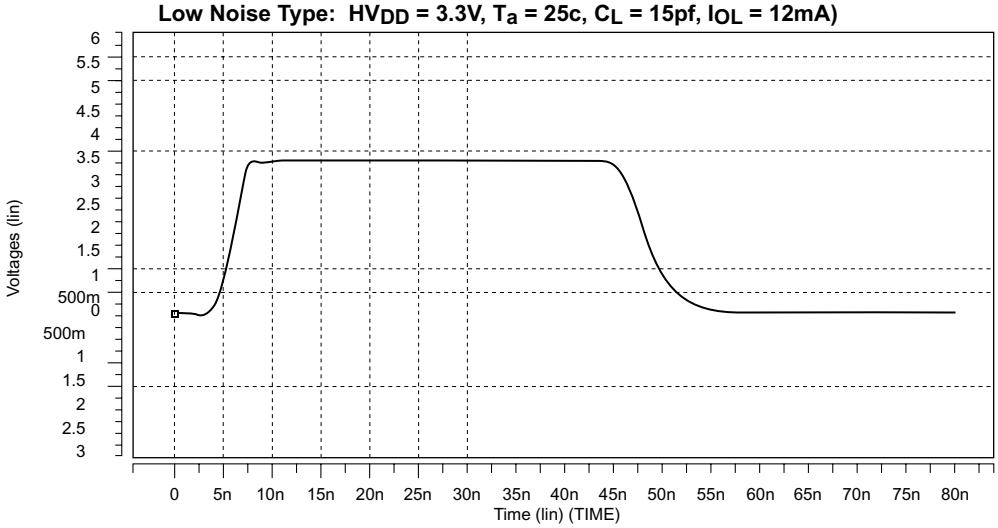


Figure A2-128 Output Waveform (XFHOBF3BT)

(8) Output waveforms (3.3 V interface)

The waveforms shown in Figures A2-130, A2-131, and A2-132 show output waveforms under the conditions in Figure A2-129.

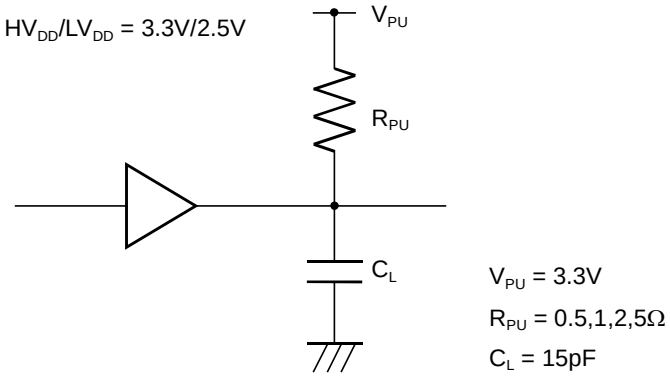


Figure A2-129 Evaluation Circuit

- Type 1

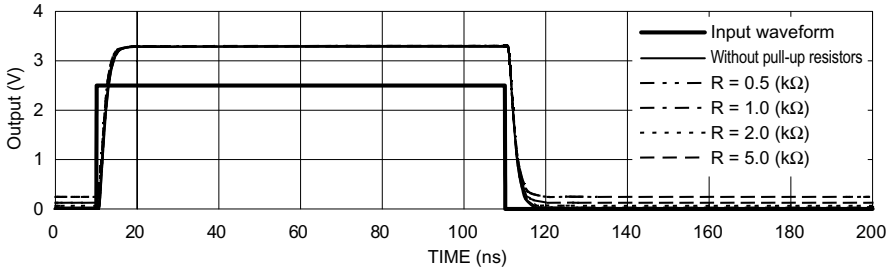


Figure A2-130 Output Waveforms (XFHOBF1T)

- Type 2

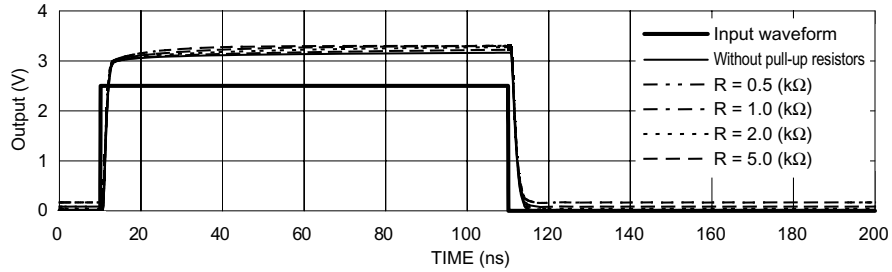


Figure A2-131 Output Waveforms (XFHOBF2T)

- Type 3

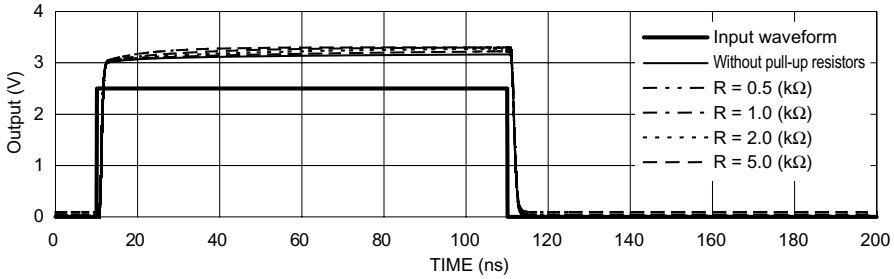


Figure A2-132 Output Waveforms (XFHOBF3AT)

(9) Output waveforms (5 V interface)

The waveforms shown in Figures A2-134, A2-135, and A2-136 show output waveforms under the conditions in Figure A2-133.

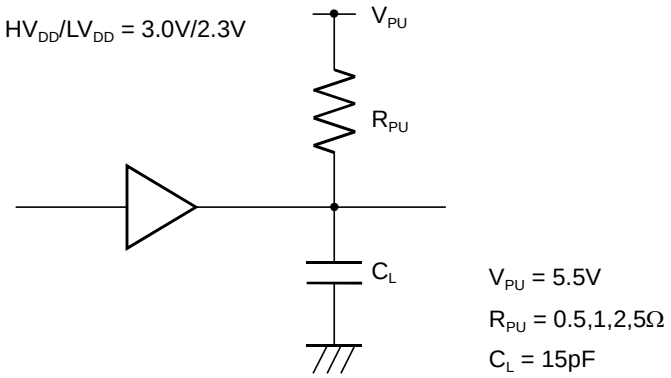


Figure A2-133 Evaluation Circuit

● Type 1

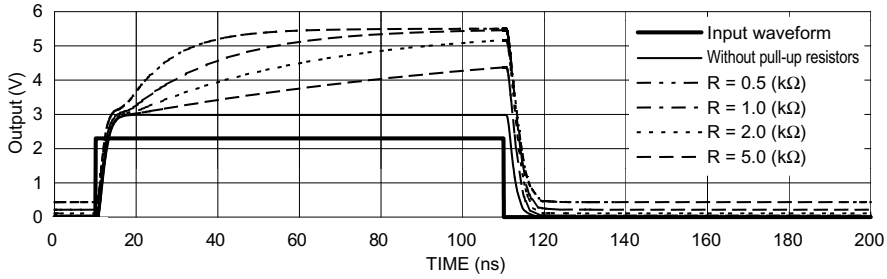


Figure A2-134 Output Waveforms (XFHOBF1T)

● Type 2

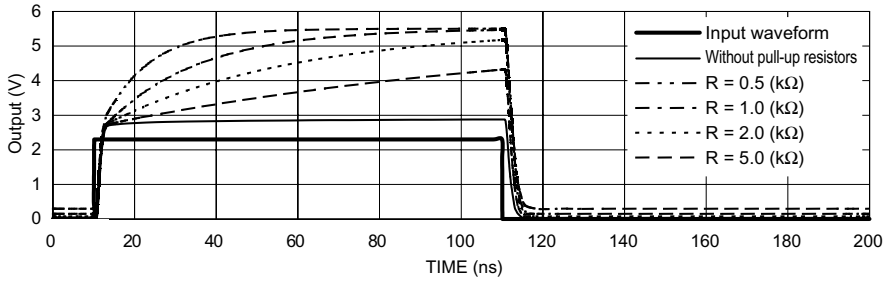


Figure A2-135 Output Waveforms (XFHOBF2T)

● Type 3

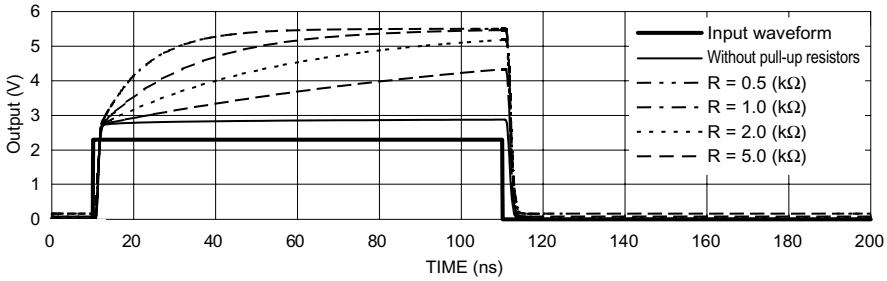


Figure A2-136 Output Waveforms (XFHOBF3AT)

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Document code: 404624401
First issue September, 2004
Printed in Japan ⓒB