FAQ for USB, ATA (Interface ICs) S1R72V series

CPU IF/DMA

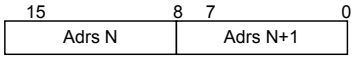
	Q	A	Applicable to: *1						
			V03	V05	V17	V27	V18	C05	H74
Q1-01	Please explain how to write/read transfer data to and from the main CPU.	Some registers and bits are for FIFO access. Transfer data by the PIO interface using these bits and registers. Or, use DMA.	○	○	○	○	○	○	○
Q1-02	Is the interrupt pin allowed to be wired OR with another LSI pin?	The interrupt output can be set to Hi-Z/Low by mode setting. However, the Hi-Z is output using the Tri-state buffer; thus pull-up by the voltage exceeding the CVDD is not allowed.	○	○	○	○	○	○	○
Q1-03	It is not possible to write to the CPU_Config register or ClkSelect register.	Check the setting of ModeProtect register. ModeProtect register setting enables or disables writing to the CPU_Config and ClkSelect register values.	○	○	○	○	○	○	○
Q1-04	Is the DMA data transfer to CPU possible without using the DACK pin?	Yes, possible. For example, set: DMA_Mode=1 DACK_Level=0: Pull up DACK pin (to inactive level). CS_Mode=0 These settings allow DMA data transfer by setting the DMA source and destination addresses to DMA0/1_Rd/WrData registers.	○	○	○	○	○	○	○
Q1-05	Is the CPU controllable by 16-bit access only?	**<See A1-05>**	○	○	○	○	○	○	○
Q1-06	Please explain how to set the IC endians.	Refer to the Appendix of the specification documents. Detailed description is also given in the CPU Connection Guide.	○	○	○	○	○	○	○
Q1-07	What is the CPU Cut Mode?	The CPU Cut Mode reduces the current consumption caused by external factors while the LSI is in Sleep state. For example, the CPU Cut Mode reduces current consumption by the CPU interface signals in the Sleep state, inhibiting external signal inputs to the LSI's input pins. Since this mode is intended to reduce the current consumption of input pins, output pins such as the interrupt signal pin operate regardless of the mode.	-	-	○	○	○	-	-
Q1-08	In the software to check the FIFO_RdRemain_H.RdRemainValid bit when reading FIFO data from USB, time-out is desired to set to avoid infinite loop.	Set the loop count to 5 times or more (7 times of more for V27). RdRemainValid=1 is confirmed at least once by reading FIFO_RdRemain_H five times. Exercise caution as RdRemainVlid=1 is not always confirmed by the fifth read.	○	○	○	○	○	○	○

<A1-05>

Yes, it is possible. However, exercise caution for the following two points when developing control softw

1. Register access
It is 16-bit access; thus when writing Address 0, data is simultaneously written to Address 1 as we

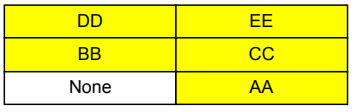
e.g. When writing data to register (Adrs N), data is also written to (Adrs N+1).



2. Access to FIFO data (Ignore the following description if the IC has FIFO_ByteWr registe
Take the following steps when writing odd-number byte data to FIF
(1) Do not let FIFO data be transferred (e.g. Disable USB data transfer by setting ForceNAK bit, et
(2) Add 1-byte dummy data at the top of odd-number byte/n[byte] data to write, and make it (n+1) even-number d
(3) Write (n+1) byte even-number data to FIFO using the FIFO_Wr registe
(4) Read the 1-byte dummy data at the top using the FIFO_ByteRd registe

e.g. If 5-byte odd-number data (AA~EE) need to be stored in

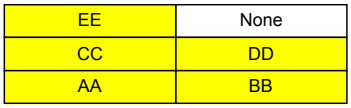
Add dummy data at the top, and write 6-byte data, (Dummy, AA)(BB, CC)(DD, EE).
(The left figure illustrates the FIFO status when step (3) mentioned above is performed)



Odd-number data is created in FIFO by reading out dummy data using FIFO_ByteRd register.
(The left figure illustrates the FIFO status when step (4) mentioned above is performed.)

To write data to FIFO by DMA, set the DMA_Count register to odd number and perform DMA transf

e.g. If 5-byte odd-number data (AA~EE) need to be stored in FIFO

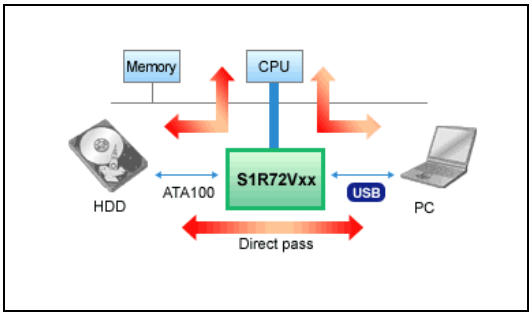


Set DMA count to "5" and transfer (AA, BB) (CC, DD) (EE, xx) by DMA, then odd-number data is created within FIFO. The 6th byte "xx" data is not written to FIFO.

IDE IF

Q2-01	Is PIO data transfer over IDE interface possible without accessing registers?	There are two ways to access the IDE device: - Use FIFO - Access registers For data transfer, FIFO is usable regardless of the IDE transfer modes, PIO, DMA, or Ultra. To use FIFO, set the transfer counts and IDE_Go.	○	○	-	-	-	○	○
Q2-02	Are V03, V05, C05, and H74 connectable with 5V IDE interface drive?	V03 and H74 interface voltages are 3.3V, and thus not controllable by 5V drive. Note: Some 3.3V interface drives have some 5V signals. They need to be converted to 3.3V.	○	○	-	-	-	○	○
Q2-03	Is it possible to use with another IC by setting the IDE interface to Hi-Z?	Yes, possible. Output is disabled by setting IDE_Config_1, ActiveIDE bits to "0." Disable all the registers to control the PU and PD of IDE	○	○	-	-	-	○	○
Q2-04	Please explain how to set pins when not using the IDE interface.	Set the logic levels of input and bi-directional pins using either one of the following methods: - Pull-up or pull-down on the board - Use internal pull-up or pull-down resistors (Validate them by using control registers)	○	○	-	-	-	○	○
Q2-05	Is the CF card connectable with the IDE interface?	Yes, it is connectable in True IDE Mode of CF card.	○	○	-	-	-	○	○
Q2-06	Is it possible to transfer data between CPU and IDE independently while transferring USB data?	Yes, possible.	○	○	-	-	-	○	○
Q2-07	Is it possible to transfer data between USB and IDE directly via the internal FIFO?	Direct data transfer is possible using the LSI internal FIFO. However, some operating systems do not allow such direct data transfer. **<See A2-07>**	○	○	-	-	-	○	-

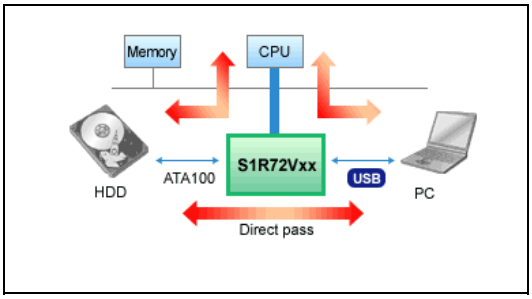
<A2-07>



USB Data Transfer

Q3-01	Is it possible to transfer data between USB and IDE directly via the internal FIFO?	Direct data transfer is possible using the LSI internal FIFO. To do this, however, the operating system must allow direct data transfer between the USB and IDE devices. If this is not the case, you need to prepare software that controls direct data transfer instead of the operating system. **<See A3-01>**	○	○	-	-	-	○	-

<A3-01>



Q3-02	Is it possible to process HDD data and then transfer them to USB?	Yes, possible. Do not directly transfer IDE data to USB, but save the processed data in the system memory first, and then transfer them to USB.	○	○	-	-	-	○	
Q3-03	Is it possible to rewrite the system firmware on the ROM (flash memory) using USB?	Yes, possible by software developed by the customer. A typical way to rewrite the flash using USB is to copy the system program code to RAM first, and then run the program on RAM.	○	○	○	○	○	○	-
Q3-04	When using USB to send data, is it necessary to write data to FIFO every time one data packet is sent?	No, not necessary. It is possible to write data to FIFO if it has available space, regardless of the packet data transfer.	○	○	○	○	○	○	-
Q3-05	Is it necessary to read data from FIFO every time one data packet is received when receiving data by USB?	No, not necessary. It is possible to read data if valid data exists in FIFO, regardless of the packet data reception.	○	○	○	○	○	○	-
Q3-06	Is high-bandwidth isochronous data transfer supported?	No, high-bandwidth is not supported.	○	○	○	○	○	○	-
Q3-07	Is OTG supported?	No, OTG is not supported.	○	○	○	○	○	○	-
Q3-08	Under what conditions do USB devices not respond to transactions?	USB devices do not respond to transactions in the following cases: - The device functions are not properly set. - Destination address is not valid. - Destination endpoint is not valid. - Packet from the host has an error.	○	○	○	○	○	○	-

USB Bus Line/Status

Q4-01	Please explain how to handle unused USB port pins.	Leave DP, DM, R1, and VBUS pins all open. If with host functions, also leave VBUSEN and VBUSFLG pins open.	○	○	○	○	○	○	-
Q4-02	When switching the device and host functions, the VBUS_Changed status is sometimes set even though no changes occur to VBUS pin. What caused this problem?	If the port shared by host and device is switched as follows while the VBUS pin is kept high, the VBUS_Changed status is set: Device => Host function (Change HostxDEVICE from "0" to "1") Host => Device function (Change HostxDEVICE from "1" to "0") This does not occur when VBUS pin is Low. **<See A4-02>**	-	○	○	○	○	○	-
Q4-03	Is the VBUS_Changed status set, if the VBUS pin changes its state from L to H or vice versa when the IC is used as a host?	It depends on the operation mode (1-port/2-port modes) of each IC. Please refer to the table below. <See **A4-03>**	-	○	○	○	○	○	-
Q4-04	The USB Device is not properly recognized by the USB Host. In the Device Manager, "Unknown device" or only "Mass Storage Class" not reflecting the descriptor is shown for the USB controller. What caused this problem?.	When connected with a PC, the USB Device takes the following steps to be recognized by the PC: 1. VBUS detection 2. DP pull-up 3. Chirp response to USB reset 4. Responds to standard requests (control transfer) If "Unknown device" is shown, problems are likely to exist in process 3 or 4. A packet is not transferred from the USB Host for a certain period of time immediately after the DP is pulled up, and thus the LSI detects the Suspend state first, and then gets ready for the USB reset later. If power management is implemented during Suspend, such as OSC halt, care must be taken to check if the OSC properly restarted its operation immediately after the USB reset detection. In case of the Mass Storage Class Device, it takes the following additional steps: 5. Responds to Mass Storage Class request (Control transfer) 6. Receives and processes CBW (Command by bulk transfer) 7. Transfers CSW (status by bulk transfer) If the Host PC recognizes the USB Device only as “Mass Storage Class,” problems are likely to exist in step 5, 6, or 7. **<See A4-04, 05>**	○	○	○	○	○	○	-
Q4-05	When connected with PC (Host), the device is recognized as FS device, not HS device. What caused this problem?	(1) Check if USB driver is installed on the USB Host EHCI driver needs to be installed on the PC (USB Host). In the case of Windows 2000, right click "My Computer," choose "Hardware tab," display "Device Manager," and expand the USB controller. If "Standard Enhanced PCI to USB Host Controller" is shown, the EHCI driver is installed. (2) Check if the USB Device outputs Device Chirp USB Device needs to output Device Chirp (K state) within the specified period of time after receiving USB RESET from USB Host. If this time limit is not met, Host will not recognize the connected equipment as HS Device. The specified time limits are as follows: When the USB Device receives USB RESET during non-SUSPEND state (during HS operation): 3.1[msec] to 6[msec] When the USB Device receives USB RESET during SUSPEND state: 2.5[usec] to 6[msec] For the time limits during FS operation and other detailed information, please refer to EL-27 and -28 in "USB-IF USB2.0 Electrical Test Specification Ver.1.03" (This document is downloadable from http://www.usb.org/developers/docs/.) **<See A4-04, 05>**	○	○	○	○	○	○	-
Q4-06	Which processes of USB Device firmware need to meet timing constraints?	1. Process when USB reset occurs during USB Suspend USB_Control.InSUSPEND bit needs to be cleared within 6ms. If not cleared within this time limit, the USB device is not recognized as HS but FS. 2. Process of Attach after detecting VBUS DP needs to be pulled up within 100ms after VBUS goes "High" only when using the USB Device as bus power. 3. Response time of control transfer Time limit to return data with data stage IN = 500[msec] Time limit to receive data with data stage OUT = 5[sec] Time limit to start status stage = 50[msec] 4. Time limit to move to test mode Test mode needs to be started within 3[msec] after the completion of status stage.	○	○	○	○	○	○	-

Q4-07	Do short-circuited DP and DM affect the LSI functions when VBUS power supply is used for battery charge?	No, short circuit is no problem. However, USB communications are not allowed.	○	○	○	○	○	○	-
Q4-08	Is it all right to connect a PC to the Device port while the LSI is powered off? Or is it all right to connect a USB Device to the Host port? Also, do DP and DM pins go Hi-Z when the LSI is powered off?	DP and DM pins do not go Hi-Z. But there should be no problem: In Device Mode: DP and DM pins on the Host side are specified Low (SE0); thus no problem. VBUS pin has a pull-down resister within the LSI and the resister consumes current, but does not damage or degrades the pin. In Host Mode: DP and DM pins are pulled down by LSI's own host termination. This retains unless the VBUS is supplied to Device side; thus no problem.	○	○	○	○	○	○	-
Q4-09	If the Host has two USB ports, is it possible to use them simultaneously?	V18 allows two equipment to be physically connected to both ports as USB devices and allows simultaneous data transfer. C05 also allows two equipment to be physically connected to both ports as USB devices, but does not allow simultaneous data transfer. V05, when used in 2-port mode, allows only one equipment to be used as a USB device. C05 and V05, when used in 1-port mode, do not allow two equipment to be connected simultaneously. **<See A4-09>**	-	○	-	-	○	○	-

<A4-02>

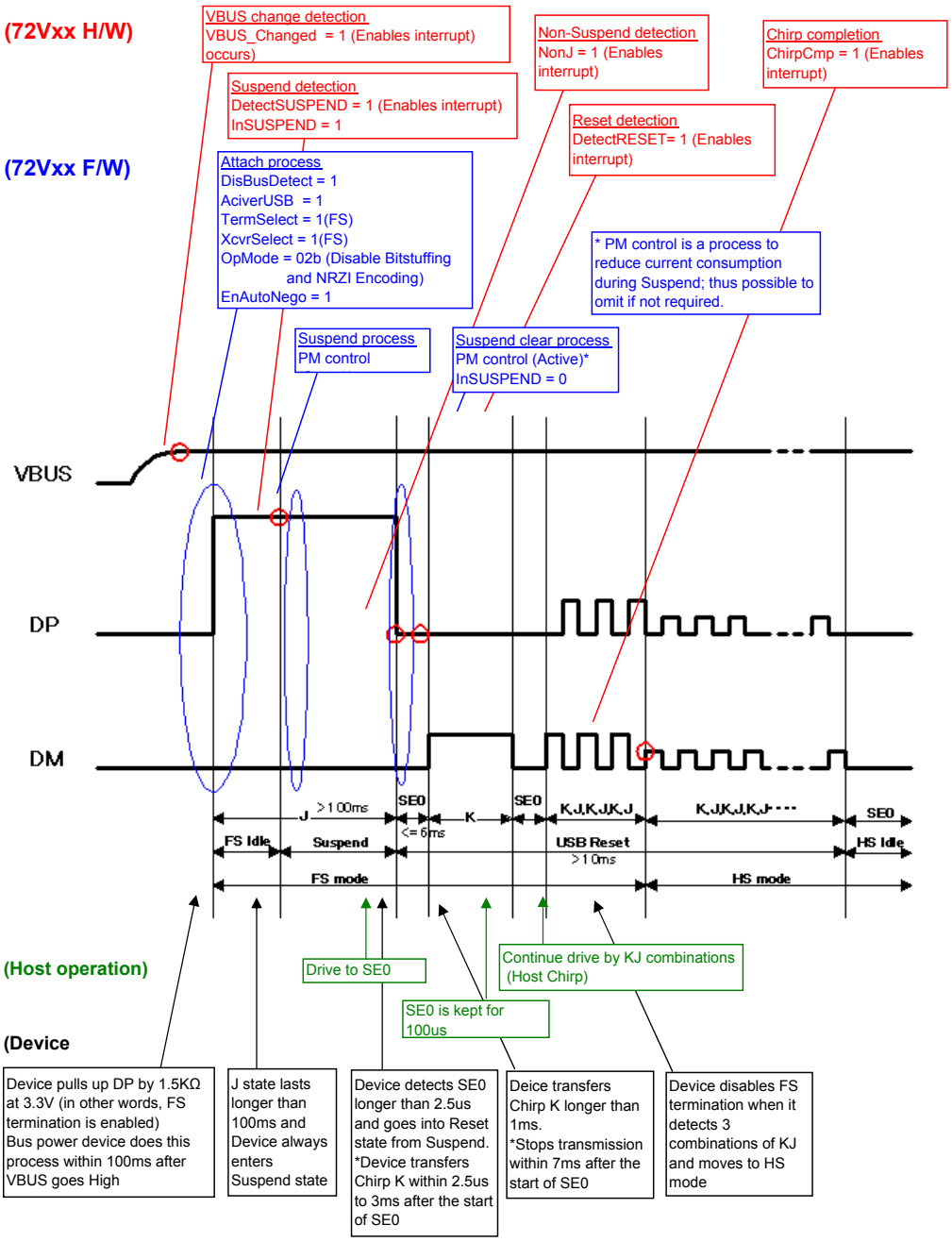
IC	Port used by both Host and Device	Mode	VBUS_Changed status
V05	Port B	2-port mode	Not set
		1-port mode	Set
V17	Single port	-	Set
V27	Single port	-	Set
V18	Port O	-	Set
C05	Port B	2-port mode	Not set
		1-port mode	Set

<A4-03>

IC	Mode	VBUS_Changed Status
V05	2-port mode	Set
	1-port mode	Not set
V17	-	Not set
V27	-	Not set
V18	Host/Host (*1)	Not set
	Device/Host (*1)	Set
C05	2-port mode	Set
	1-port mode	Not set

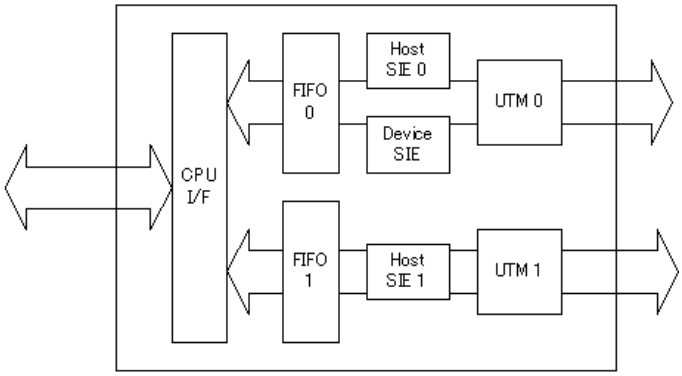
(*1) Indicates function state (Port0/Port1)

<A4-04, 05>

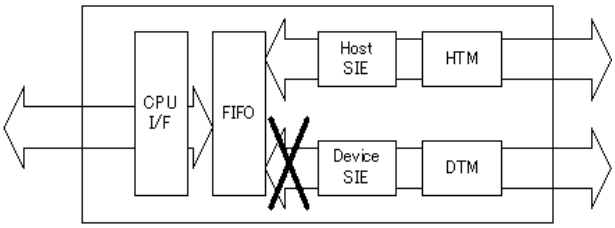

(72Vxx H/W)
VBUS change detection
VBUS_Changed = 1 (Enables interrupt) occurs)
Non-Suspend detection
NonJ = 1 (Enables interrupt)
Chirp completion
ChirpCmp = 1 (Enables interrupt)
Suspend detection
DetectSUSPEND = 1 (Enables interrupt)
InSUSPEND = 1
Reset detection
DetectRESET= 1 (Enables interrupt)
(72Vxx F/W)
Attach process
DisBusDetect = 1
AciverUSB = 1
TermSelect = 1(FS)
XcvrSelect = 1(FS)
OpMode = 02b (Disable Bitstuffing and NRZI Encoding)
EnAutoNego = 1
* PM control is a process to reduce current consumption during Suspend; thus possible to omit if not required.
Suspend process
PM control
Suspend clear process
PM control (Active)*
InSUSPEND = 0
VBUS
DP
DM
J
>100ms
SE0
<= 5ms
K
SE0
K,J,K,J,K,J
K,J,K,J,K,J
SE0
FS Idle
Suspend
USB Reset
>10ms
HS Idle
FS mode
HS mode
(Host operation)
Drive to SE0
Continue drive by KJ combinations (Host Chirp)
SE0 is kept for 100us
(Device
Device pulls up DP by 1.5KΩ at 3.3V (in other words, FS termination is enabled)
Bus power device does this process within 100ms after VBUS goes High
J state lasts longer than 100ms and Device always enters Suspend state
Device detects SE0 longer than 2.5us and goes into Reset state from Suspend.
*Device transfers Chirp K within 2.5us to 3ms after the start of SE0
Deice transfers Chirp K longer than 1ms.
*Stops transmission within 7ms after the start of SE0
Device disables FS termination when it detects 3 combinations of KJ and moves to HS mode

<A4-09>

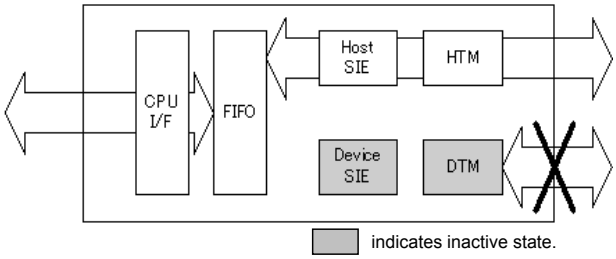
V18:
Each port has FIFO and is capable to transfer data independently.



C05:
Host and Device FIFOs are mutually exclusive. Simultaneous data transfer from multiple ports is not possible. (The following figure illustrates the Host transferring data.)



V05:
Host and Device cannot be simultaneously active (supplied clock).
However, an asynchronous interrupt like VBUS_Changed is usable.
(The following figure illustrates the Host in active state.)



Q4-10	Is it possible to set DP and DM pins to Hi-Z?	Yes, it is possible to set the DP and DM pins to Hi-Z by the following register setting: XcvrControl.OpMode* = 01b (Non-Driving) Use this setting when not connected by a cable unless otherwise specified. Even when a cable is used, use this setting to deliberately detach the equipment. However, because the DP and DM pins are in the Hi-Z state, bus activity detection function is invalid except VBUS. *D_XcvrControl, and H_XcvrControl names are used for other LSIs.	○	○	○	○	○	○	-
Q4-11	Does the power supply to VBUS pin always need to be 5V?	No, does not need to be 5V, as long as it is higher than the H-level trigger voltage described in the DC input characteristics section of the specifications.	○	○	○	○	○	○	-
Q4-12	If a common mode choke coil is inserted in DP and DM lines, what effect is expected?	Common mode choke coil reduces the current flowing in the same direction as differential signal line and prevents the occurrence of common mode noise. Phase and voltage differences of DP and DM signals are expected to be improved. It is not directly related to the improvement of eye pattern opening.	○	○	○	○	○	○	-
Q4-13	Is it all right to connect USB Host or Device when the IC is powered off?	No problem. When USB Host is connected: DP and DM pins are pulled down on the USB Host side. VBUS voltage is applied to VBUS pin (normally about 5V) but does not damage the pin. However, about 40uA current flows to VBUS pin from the USB Host due to the internal pull-down register of 125 kΩ, (Min. 110kΩ; Max. 150kΩ.) When USB Device is connected: DP and DM pins on the Host side are in the Hi-Z state; VBUS is not output and thus there should be no problem.	○	○	○	○	○	○	-

Q4-14	Are the 10Ω resistor and 1uF capacitor required as shown in the recommended circuit around the VBUS pin? Is it possible to change these resistance and capacitance values?	Yes, required. These are to protect the IC from the surge-like excessive voltage from the VBUS pin. These values are determined based on Epson's evaluation results of many different products on the market. If desired to change the values, pay attention to the following points: - Voltage applied to VBUS pin should not exceed the absolute maximum rating (6V) - VBUS pin is internally pulled down by 125kΩ (min. 110kΩ, max. 150kΩ), and thus its input level determined by the ratio to the external resistance must exceed the H-level trigger voltage of VBUS pin.	○	○	○	○	○	○	-
Q4-15	Is the VBUS pin on the IC for supplying power from the USB Host?	VBUS pin is not a pin to supply power to the IC. The pin is used to detect the connection with USB Host and it is internally pulled down by 125kΩ (Min. 110kΩ; Max. 150kΩ) resistance. When connected with USB Host, it consumes the amount of current corresponding to its resistance.	○	○	○	○	○	○	-

Board Design / External Components

Q5-01	Are there any decoupling capacitors possible to omit?	Regardless of whether or not there are unused function blocks, it is recommended to use decoupling capacitors for all power supply pins from the view point of stable power supply.	○	○	○	○	○	○	○
Q5-02	Is it all right to use a cable to connect the USB connector with the board where a USB controller IC is mounted?	It may degrade the signal integrity and thus not recommended.	○	○	○	○	○	○	-
Q5-03	Are there any points to pay attention when selecting an external VBUS power switch?	Switches capable of preventing reverse current are recommended.	-	○	○	○	○	○	-
Q5-04	Does the resistor connected to R1 pin need to be 6.2**kΩ**±1%?	Yes. It is the resistor to generate the reference current that determines the USB analog circuit characteristics. Too much margin will affect the analog characteristics, and thus it is recommended to meet the specified value.	○	○	○	○	○	○	-
Q5-05	Are the 10**Ω** resistor and 1uF capacitor required as shown in the recommended circuit around the VBUS pin? Is it possible to change these resistance and capacitance values?	Yes, required. These are to protect the IC from the surge-like excessive voltage from the VBUS pin. These values are determined based on Epson's evaluation results of a variety of products on the market. If desired to change the values, pay attention to the following points: - Voltage applied to VBUS pin should not exceed the absolute maximum rating (6V) - VBUS pin is internally pulled down to 125kΩ(min110kΩ, max150kΩ), and thus its input level must exceed the H-level trigger voltage of VBUS pin.	○	○	○	○	○	○	-
Q5-06	Please explain how to handle unused USB port pins.	Leave DP, DM, R1, and VBUS pins all open. If with host functions, also leave VBUSEN and VBUSFLG pins open.	○	○	○	○	○	○	-
Q5-07	Please explain how to handle the CLKIN pin when connecting a crystal oscillator with XI and XO pins.	When using a crystal oscillator, connect the CLKIN pin with GND.	-	-	○	○	-	-	-
Q5-08	Please explain how to handle XI and XO pins when inputting an external clock to CLKIN pin.	When clock is directly input to CLKIN pin, connect the XI pin with GND and leave the XO pin open.	-	-	○	○	-	-	-
Q5-09	When inputting an external clock to CLKIN pin, what AC characteristics and amplitude level need to be met by the clock?	When the clock is directly input to CLKIN pin, the clock needs to meet the same AC characteristics as the crystal oscillator. The frequency accuracy=±100ppm, Duty=45% to 55%. The amplitude level needs to be the same level of voltage supplied to the CVDD pin. (For more information, see "DC characteristics" in the data sheet.)	-	-	○	○	-	-	-
Q5-10	Please explain how to set the IC endians.	Refer to the Appendix of the specification documents. Detailed description is also given in the CPU Connection Guide.	○	○	○	○	○	○	○
Q5-11	If a common mode choke coil is inserted in DP and DM lines, what effect is expected?	Common mode choke coil reduces the current flowing in the same direction as differential signal line and prevents the occurrence of common mode noise. Phase and voltage differences of DP and DM signals are expected to be improved. It is not directly related to the improvement of eye pattern opening.	○	○	○	○	○	○	-

Crystal / Clock / Power Management

Q6-01	What frequency accuracy is required for the crystal oscillator to use?	USB2.0 High-Speed frequency accuracy is defined ±500ppm. The USB signal waveform is significantly affected by the input clock jitter and frequency accuracy, and thus Epson recommends a crystal oscillator with frequency accuracy within ±100ppm to ensure the signal integrity of end products.	○	○	○	○	○	○	-
Q6-02	The crystal oscillator does not oscillate though the IC is powered on.	The initial state of the IC when powered on is the Sleep Mode where the oscillator is inactive. To release the Sleep Mode, refer to Chapter 4 in the CPU Connection Guide for each IC.	○	○	○	○	○	○	○
Q6-03	Please explain how to handle the CLKIN pin when connecting a crystal oscillator with XI and XO pins.	When using a crystal oscillator, connect the CLKIN pin with GND.	-	-	○	○	-	-	-
Q6-04	Please explain how to handle XI and XO pins when inputting an external clock to CLKIN pin.	When clock is directly input to CLKIN pin, connect the XI pin with GND and leave the XO pin open.	-	-	○	○	-	-	-
Q6-05	When inputting an external clock to CLKIN pin, what AC characteristics and amplitude level need to be met by the clock?	When the clock is directly input to CLKIN pin, the clock needs to meet the same AC characteristics as the crystal oscillator. The frequency accuracy=±100ppm, Duty=45% to 55%. The amplitude level needs to be the same level as the voltage supplied to the CVDD pin. (For more information, see "DC characteristics" in the data sheet.)	-	-	○	○	-	-	-

Q6-06	Is it possible to use a ceramic oscillator instead of a crystal oscillator?	As for ceramic oscillators, Murata Manufacturing is now verifying the operation using Ceralock. For detailed information, please contact Murata.	○	○	○	○	○	○	-

Power Supply

Q7-01	What is the IC consumption current?	Please refer to the consumption current measurement data in the listing of related materials. For data not found in the listing, please contact EpsonUSBIC@exc.epson.co.jp.	○	○	○	○	○	○	○
Q7-02	Is it possible to power off only this IC whille USB is not used? What are the status of pins when the IC is powered off?	No, it is not possible to power off this IC only. The IC needs to be always powered on because the pins will not go Hi-Z. Current will flow towards power supply pins by the internal elements to protect each pin.	○	○	○	○	○	○	○
Q7-03	Is it all right to connect USB Host or Device when the IC is powered off?	No problem. When USB Host is connected: DP and DM pins are pulled down on the USB Host side. VBUS voltage is applied to VBUS pin (normally about 5V) but does not damage the pin. However, about 40uA current flows to VBUS pin from the USB Host due to the internal pull-down register of 125 kΩ (Min. 110kΩ; Max. 150kΩ). When USB Device is connected: DP and DM pins on the Host side are in the Hi-Z state; VBUS is not output and thus there should be no problem.	○	○	○	○	○	○	-
Q7-04	Multiple power supplies exist. Are there any constraints on the power-on and -off sequences?	Yes. Please follow the power-on and -off sequences described in the data sheet.	○	○	○	○	○	○	○
Q7-05	The specified power-on and -off sequences are not possible to follow. Are there any other allowable sequences or conditions?	If power-on and -off sequences are completed within a second, no specific sequences are required to follow..	○	○	○	○	○	○	○
Q7-06	Is it all right to use the same power supply as LVDD (1.8V) or HVDD (3.3V) for CVDD (1.8/3.3V)?	Yes, it is all right. However, exercise caution as LVDD is susceptible to noise that may affect the quality of USB eye patterns.	○	○	○	○	○	○	○
Q7-07	Is the VBUS pin on the IC for supplying power from the USB Host?	The VBUS pin is not a pin to supply power to the IC. The pin is used to detect the connection with USB Host and internally pulled down by 125kΩ (Min. 110kΩ; Max. 150kΩ) resistance. When connected with USB Host, it consumes the amount of current corresponding to its resistance.	○	○	○	○	○	○	-