Mar/27/2015

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S1C17 Family Technical Manual Errata

ITEM **LCD drive voltage**

Object manual	Document code	Object item	Page
S1C17701Technical Manual	411089905	26.4 Analog Circuit Characteristics	26-3
S1C17702Technical Manual	411581702	27.4 Analog Circuit Characteristics	27-3
S1C17704Technical Manual	411511903	26.4 Analog Circuit Characteristics	26-3
S1C17705/703Technical Manual	411706602	25.9 LCD Driver Characteristics	25-10
S1C17706Technical Manual	412026401	27.9 LCD Driver Characteristics	27-7

(Error)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1µF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1}		0.18V_{C5}		0.22V_{C5}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		0.39V_{C5}		0.43V_{C5}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		0.59V_{C5}		0.63V_{C5}	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		0.79V_{C5}		0.83V_{C5}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

(Correct)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1µF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1}		0.18V_{C5}		0.22V_{C5}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		0.39V_{C5}		0.43V_{C5}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		0.59V_{C5}		0.63V_{C5}	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		0.79V_{C5}		0.83V_{C5}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

V_{C5} and V_{C1}

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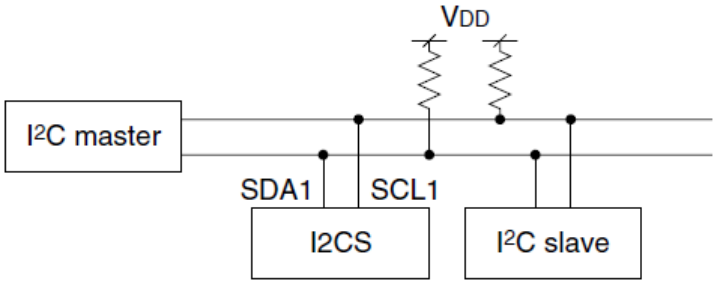
ITEM **I2C Slave Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	21.2 I2C Slave Input/Output Pins	21-2
S1C17611 Technical Manual	411882301	21.2 I2C Slave Input/Output Pins	21-2
S1C17706 Technical Manual	412026401	18.2 I2CS Input/Output Pins	18-1
S1C17002 Technical Manual	411554402	V.3.2 I2C Slave I/O Pins	V-3-2
S1C17003 Technical Manual	411635102	21.2 I2C Slave Input/Output Pins	21-2
S1C17803 Technical Manual	411820401	21.2 I2CS Input/Output Pins	21-2

(Addition)

Note: The pins go to high impedance status when the port function is switched. The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDDwith an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



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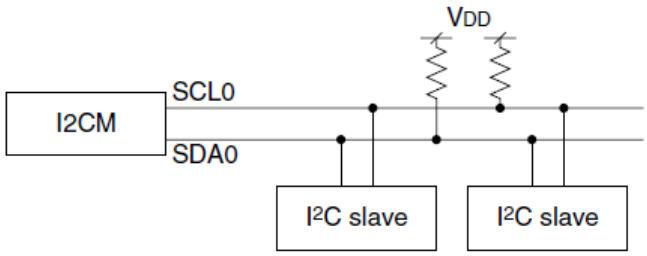
S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412301	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



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S1C17 Series Technical Manual Errata

ITEM 24.5 Intermittent Operation

Object manual	Document code	Object Item	Page
S1C17706	412026401	24.5 Intermittent Operation	24-3
		SVD Comparison Voltage Register	24-6

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(Error)

24.5 Intermittent Operation

Table 24.5.2 Selection of Detection Result Judgment Times in Intermittent Operation Mode

SVDSC[1:0]	Detection result Judgment
0x3	Continuous 4 times detection
0x2	Continuous 3 times detection
0x1	Continuous 2 times detection
0x0	Continuous 1 times detection

(Default:0x0)

Control Register Details

D[5:4] SVDSC:SVD Sampling Result Count Bits

Sets a number of times of the continuous logical 1 state in the detection result that causes the SVDIF/SVD_IFG register to be set to 1 when the intermittent operation mode.

Table 24.7.4 Selection of Detection Result Judgment Times in Intermittent Operation Mode

SVDSC[1:0]	Detection result Judgment
0x3	Continuous 4 times detection
0x2	Continuous 3 times detection
0x1	Continuous 2 times detection
0x0	Continuous 1 times detection

(Default:0x0)

(Correct)

24.5 Intermittent Operation

Table 24.5.2 Selection of Detection Result Judgment Times in Intermittent Operation Mode

SVDSC[1:0]	Detection result Judgment
0x3	Continuous **8** times detection
0x2	Continuous **4** times detection
0x1	Continuous 2 times detection

0x0	Continuous 1 times detection

(Default：0x0)

Control Register Details

D[5:4] SVDSC：SVD Sampling Result Count Bits

Sets a number of times of the continuous logical 1 state in the detection result that causes the SVDIF/SVD_IFG register to be set to 1 when the intermittent operation mode.

Table 24.7.4 Selection of Detection Result Judgment Times in Intermittent Operation Mode

SVDSC[1:0]	Detection result Judgment
0x3	Continuous **8** times detection
0x2	Continuous **4** times detection
0x1	Continuous 2 times detection
0x0	Continuous 1 times detection

(Default：0x0)

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S1C17 Series Technical Manual Errata

ITEM SEG Terminal Control Register			
Object manual	Document code	Object Item	Page
S1C17706	4120226401	SEG Terminal Control Register (LCD_SEGC)	21-25

Page 21-25 S1C17706 Technical Manual

(Error)

SEG Terminal Control Register (LCD_SEGC)

Setting

NCLINE[4:0]	Reverse line
0xf	31 lines
:	:
0x1	1line
0x0	Normal

D[4:0] SEG n Line[4:0] Reverse Drive Selection Bits

Enables the n-line AC reverse drive and sets the reverse lines

表 21.9,8 Selecting Reverse Lines

NLINE[4:0]	Reverse lines
0xF	31line
:	:
0x1	1line
0x0	Normal

(Correct)

SEG Terminal Control Register (LCD_SEGC)

Setting

NCLINE[4:0]	Reverse lines
0x1f	31 lines
:	:
0x1	1line
0x0	Normal

D[4:0] SEG n Line[4:0] Reverse Drive Selection Bits

Enables the n-line AC reverse drive and sets the reverse lines

表 21.9,8 Selecting Reverse Lines

NLINE[4:0]	Reverse lines
0x1F	31 lines
:	:
0x1	1line
0x0	Normal

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S1C17 Series Technical Manual Errata

ITEM			
Object manual	Document code	Object Item	Page
S1C17706	412026401	21.5.4 COM Outputs Partial Drive	21-11
Page 21-11 S1C17706 Technical Manual			
(Error) If the COM*DEN/LCD_COMC0-3 register is set to 1, any COM output can be output as the OFF waveforms (trun-off waveforms) regardless of the display data RAM. This can limit the number of required display positions and reduce power consumption.			
(Correct) If the COM*DEN/LCD_COMC0-3 register is set to **0**, any COM output can be output as the OFF waveforms (trun-off waveforms) regardless of the display data RAM. This can limit the number of required display positions and reduce power consumption.			

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S1C17 Series Technical Manual Errata

ITEM About the CBUFEN register of T16A/T16A2

Object manual	Document code	Object Item	Page
S1C17624/604/622/602/621 Technical Manual	411914902	13.8 Control Register Details	13-14 13-15
S1C17705/703 Technical Manual	411706602	10.8 Control Register Details	10-19
S1C17706 Technical Manual	412026401	10.8 Control Register Details	10-17
S1C17711 Technical Manual	411905602	10.8 Control Register Details	10-14
S1C17554/564 Technical Manual	411914402	11.8 Control Register Details	11-14
S1C17651 Technical Manual	412120600	12.8 Control Register Details	12-13

Page 13-14 13-15 S1C624/604/622/602/621 Technical Manual

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Page 12-13 S1C17651 Technical Manual

(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.

Page 13-14 13-15 S1C17705/703 Technical Manual

Page 10-14 S1C17711 Technical Manual

Page 11-14 S1C17554/564 Technical Manual

(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.