Apr/17/2017

errata_c17704_14

S1C17 Family Technical Manual Errata

ITEM **A part of shipping form is discontinued**			
Object manual	Document code	Object item	Page
S1C17704 Technical Manual	411511903	Shipping form	1-2

1.1 Features

(Error)

Shipping form

- TQFP24-144pin plastic package
  (16 mm × 16 mm × 1.0 mm, lead pitch: 0.4 mm)
- PFBGA6U96 package*
  (6 mm × 6 mm × 1.0 mm, ball pitch: 0.5 mm)
- VFBGA7H-161 package
  (7 mm × 7 mm × 1.0 mm, ball pitch: 0.5 mm)
- VFBGA10H-144 package
  (10 mm × 10 mm × 1.0 mm, ball pitch: 0.8 mm)
- Chip

(Correct)

Shipping form

- TQFP24-144pin plastic package
  (16 mm × 16 mm × 1.0 mm, lead pitch: 0.4 mm)
- PFBGA6U96 package* ＃1
  (6 mm × 6 mm × 1.0 mm, ball pitch: 0.5 mm)
- VFBGA7H-161 package
  (7 mm × 7 mm × 1.0 mm, ball pitch: 0.5 mm)
- VFBGA10H-144 package
  (10 mm × 10 mm × 1.0 mm, ball pitch: 0.8 mm)
- Chip

＃1：PFBGA6U96 is discontinued.

Mar/27/2015

errata_c17704_13

S1C17 Family Technical Manual Errata

ITEM **LCD drive voltage**

Object manual	Document code	Object item	Page
S1C17701Technical Manual	411089905	26.4 Analog Circuit Characteristics	26-3
S1C17702Technical Manual	411581702	27.4 Analog Circuit Characteristics	27-3
S1C17704Technical Manual	411511903	26.4 Analog Circuit Characteristics	26-3
S1C17705/703Technical Manual	411706602	25.9 LCD Driver Characteristics	25-10
S1C17706Technical Manual	412026401	27.9 LCD Driver Characteristics	27-7

(Error)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1µF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1}		0.18V_{C5}		0.22V_{C5}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		0.39V_{C5}		0.43V_{C5}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		0.59V_{C5}		0.63V_{C5}	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		0.79V_{C5}		0.83V_{C5}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

(Correct)

Unless otherwise specified: V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = 25°C, C_1–C_{11} = 0.1µF, Checker pattern displayed, No panel load

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1}		0.18V_{C5}		0.22V_{C5}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2}		0.39V_{C5}		0.43V_{C5}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3}		0.59V_{C5}		0.63V_{C5}	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4}		0.79V_{C5}		0.83V_{C5}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5}	LC[3:0] = 0x0		4.20		V
			LC[3:0] = 0x1		4.30		V
			LC[3:0] = 0x2		4.40		V

V_{C5} and V_{C1}

Aug/28/2013

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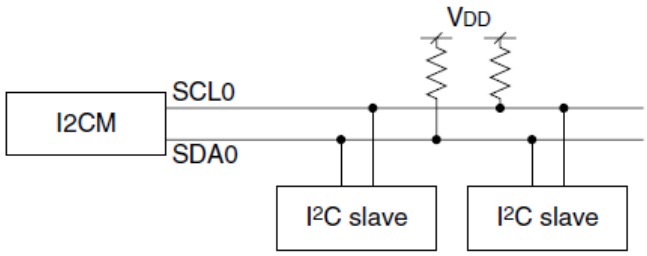
S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412301	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Nov/09/2012

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S1C17 Family Technical Manual Errata

ITEM About the Fine mode setting of T16E.			
Object manual	Document code	Object item	Page
S1C17001 Technical Manual	411412303	13.6 Clock Output Control	150
S1C17003 Technical Manual	411635102	13.6 Clock Output Control	13-8
S1C17624/604/622/621 Technical Manual	411914902	12.7 Clock Output Control	12-6
S1C17701 Technical Manual	411089905	13.6 Controlling Clock Output	13-8
S1C17702 Technical Manual	411581702	13.6 Clock Output Control	13-8
S1C17704 Technical Manual	411511903	13.6 Controlling Clock Output	13-8

Page 150 S1C17001 Technical Manual

Page 13-8 S1C17003 Technical Manual

Page 13-8 S1C17701 Technical Manual

Page 13-8 S1C17702 Technical Manual

Page 13-8 S1C17704 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(3) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Page 12-6 S1C17623/604/622/621 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(4) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Dec/27/2011

errata_c17704_10

S1C17 Series Technical Manual Errata

Item Wakeup from HALT by T8OSC1 interrupt			
Object manual	Document code	Object Item	Page
S1C17701 Technical Manual S1C17704 Technical Manual	411089704 411511804	14 8-bit OSC1 Timer Appendix C Power Saving	14-7 AP-31 AP-32

(Error)

Note: To avoid occurrence of unnecessary interrupts, be sure to reset the T8OIF flag before the compare match interrupt is enabled using T8OIE.

(Correct)

Note: - To avoid occurrence of unnecessary interrupts, be sure to reset the T8OIF flag before the compare match interrupt is enabled using T8OIE.

- Interrupt will not be occurred when PCLK is OFF, because T8OIF will not be set by matching counter value to conpare data register value. Use T8OSC1 interrupt with PCLK ON.

(Error) Peripheral modules that operate with PCLK - Prescaler (PWM & capture timer, remote controller, P port) - UART - 8-bit timer - 16-bit timer Ch.0–2 - Interrupt controller - SPI - I2C - SVD circuit - Power control circuit - P port & port MUX (control registers and chattering filters) - PWM & capture timer - MISC register - Remote controller
(Correct) Peripheral modules that operate with PCLK - Prescaler (PWM & capture timer, remote controller, P port) - UART - 8-bit timer - 16-bit timer Ch.0–2 - Interrupt controller - SPI - I2C - SVD circuit - Power control circuit - P port & port MUX (control registers and chattering filters) - PWM & capture timer - MISC register - Remote controller - 8-bit OSC1 Timer

(Error) The peripheral modules listed below operate with a clock other than PCLK except for accessing their control registers. Therefore, PCLK is not required after the control registers are set once and the module starts operating. - Clock timer - Stopwatch timer - Watchdog timer - 8-bit OSC1 timer - LCD driver
(Correct) The peripheral modules listed below operate with a clock other than PCLK except for accessing their control registers. Therefore, PCLK is not required after the control registers are set once and the module starts operating. - Clock timer - Stopwatch timer - Watchdog timer ~~- 8-bit OSC1 timer~~ - LCD driver

Dev/27/2011

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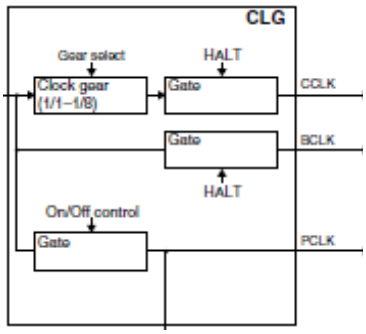
S1C17 Series Technical Manual Errata

Item Clock gear			
Object manual	Document code	Object Item	Page
S1C17701 Technical Manual S1C17704 Technical Manual	411089704 411511804	8 Clock Generator	8-1 8-2 8-4 8-6

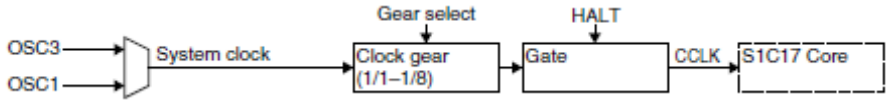
(Error)



(Correct)

[Delete clock gear block]

(Error)



(Correct)

[Delete clock gear block]

(Error)

Selecting a clock gear

Use CCLKGR[1:0] (D[1:0]/CLG_CCLK register) to select a gear for reducing the system clock speed.

* **CCLKGR[1:0]**: CCLK Clock Gear Ratio Select Bits in the CCLK Control (CLG_CCLK) Register (D[1:0]/0x5081)

Table 8.2.1 Selecting a CCLK Gear

CCLKGR[1:0]	Gear ratio
0x3	1/8
0x2	1/4
0x1	1/2
0x0	1/1

(Default: 0x0)

(Correct)

[Delete]

(Error)

Table 8.4.1 List of CLG Registers

Address	Register name		Function
0x5080	CLG_PCLK	PCLK Control Register	Controls the PCLK output.
0x5081	CLG_CCLK	CCLK Control Register	Configures the CCLK division ratio.

(Correct)

[Delete register in 0x5081]

(Error)

0x5081: CCLK Control Register (CLG_CCLK)

Register name	Address	Bit	Name	Function	Setting		Init.	R/W	Remarks
CCLK Control Register (CLG_CCLK)	0x5081 (8 bits)	D7–2	–	reserved	–		–	–	0 when being read.
		D1–0	CCLKGR[1:0]	CCLK clock gear ratio select	CCLKGR[1:0]	Gear ratio	0x0	R/W	
					0x3	1/8			
					0x2	1/4			
					0x1	1/2			
					0x0	1/1			

D[7:2] Reserved

D[1:0] CCLKGR[1:0]: CCLK Clock Gear Ratio Select Bits

Selects a gear ratio to decelerate the system clock. This determines the rate of the CCLK clock for driving the S1C17 Core. Drive the S1C17 Core with the slowest clock possible to reduce current consumption.

Table 8.4.3 Selecting CCLK Gear Ratio

CCLKGR[1:0]	Gear ratio
0x3	1/8
0x2	1/4
0x1	1/2
0x0	1/1

(Default: 0x0)

(Correct)

[Delete]

Dev/27/2011

errata_c17704_8

S1C17 Series Technical Manual Errata

Item Interrupt enable bits in 8-bit OSC1 Timer / Clock Timer / Stopwatch Timer

Object manual	Document code	Object Item	Page
S1C17701 Technical Manual	411089905	8-bit OSC1 Timer	14-13
S1C17704 Technical Manual	411511804	Clock Timer	15-10
		Stopwatch Timer	16-11

(Error)

D0 **T8OIE: 8-bit OSC1 Timer Interrupt Enable Bit**

Enables/disables the compare match interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)

Setting T8OIE to 1 enables the 8-bit OSC1 timer to request interrupts to the ITC; setting to 0 disables the interrupt.
In addition, it is necessary to set the 8-bit OSC1 timer interrupt enable bits in the ITC to interrupt enabled to actually generate an interrupt.

(Correct)

D0 **T8OIE: 8-bit OSC1 Timer Interrupt Enable Bit**

Enables/disables the interrupt flag set by compare match ~~interrupt~~.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)

Setting T8OIE to 1 enables ~~the 8-bit OSC1 timer to request interrupts to the ITC~~ interrupt flag set by compare match; setting to 0 disables the interrupt flag set.
In addition, it is necessary to set the 8-bit OSC1 timer interrupt enable bits in the ITC to interrupt enabled to actually generate an interrupt.

Note: Even if you set this bit to 0 when the T8OIF (D0/T8OSC1_IFLG register) is 1, interrupt request to CPU will not be disabled.If you want to disable interrupt request, use interrupt mask function in Interrupt Controller (ITC).

(Error)

This register enables or disables the interrupt requests by the clock timer 32 Hz, 8 Hz, 2 Hz, and 1 Hz signals, individually. Setting CTIE* bit to 1 enables the clock timer interrupt request by the falling edge of the corresponding signal; setting it to 0 disables the interrupt.
In addition, it is necessary to set the clock timer interrupt enable bit in the ITC to interrupt enabled to actually generate an interrupt.

D[7:4] **Reserved**
D3 **CTIE32: 32 Hz Interrupt Enable Bit**
Enables/disables the 32 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)
D2 **CTIE8: 8 Hz Interrupt Enable Bit**
Enables/disables the 8 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)
D1 **CTIE2: 2 Hz Interrupt Enable Bit**
Enables/disables the 2 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)
D0 **CTIE1: 1 Hz Interrupt Enable Bit**
Enables/disables the 1 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)

(Correct)

This register enables or disables the interrupt flag set ~~requests~~ by the clock timer 32 Hz, 8 Hz, 2 Hz, and 1 Hz signals, individually. Setting CTIE* bit to 1 enables the clock timer interrupt flag set ~~request~~ by the falling edge of the corresponding signal; setting it to 0 disables the interrupt flag set.
In addition, it is necessary to set the clock timer interrupt enable bit in the ITC to interrupt enabled to actually generate an interrupt.

D[7:4] **Reserved**
D3 **CTIE32: 32 Hz Interrupt Enable Bit**
Enables/disables the 32 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)
D2 **CTIE8: 8 Hz Interrupt Enable Bit**
Enables/disables the 8 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)
D1 **CTIE2: 2 Hz Interrupt Enable Bit**
Enables/disables the 2 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)
D0 **CTIE1: 1 Hz Interrupt Enable Bit**
Enables/disables the 1 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)

Note: Even if you set this bit to 0 when the CTIF32, CTIF8, CTIF2, CTIF1 (D[3:0]/CT_IFLG register) is 1, interrupt request to CPU will not be disabled.If you want to disable interrupt request, use interrupt mask function in Interrupt Controller (ITC).

(Error)

This register enables or disables the interrupt requests by the stopwatch timer 100 Hz, 10 Hz, and 1 Hz signals, individually. Setting SIE* bit to 1 enables the stopwatch timer interrupt request by the falling edge of the corresponding signal; setting it to 0 disables the interrupt.
In addition, it is necessary to set the stopwatch timer interrupt enable bit in the ITC to interrupt enabled to actually generate an interrupt.

D[7:3] Reserved

D2 SIE1: 1 Hz Interrupt Enable Bit
Enables/disables the 1 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)

D1 SIE10: 10 Hz Interrupt Enable Bit
Enables/disables the 10 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)

D0 SIE100: 100 Hz Interrupt Enable Bit
Enables/disables the 100 Hz interrupt.
1 (R/W): Enable interrupt
0 (R/W): Disable interrupt (default)

(Correct)

This register enables or disables the interrupt flag set ~~requests~~ by the stopwatch timer 100 Hz, 10 Hz, and 1 Hz signals, individually. Setting SIE* bit to 1 enables the stopwatch timer interrupt flag set ~~request~~ by the falling edge of the corresponding signal; setting it to 0 disables the interrupt.
In addition, it is necessary to set the stopwatch timer interrupt enable bit in the ITC to interrupt enabled to actually generate an interrupt.

D[7:3] Reserved

D2 SIE1: 1 Hz Interrupt Enable Bit
Enables/disables the 1 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)

D1 SIE10: 10 Hz Interrupt Enable Bit
Enables/disables the 10 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)

D0 SIE100: 100 Hz Interrupt Enable Bit
Enables/disables the 100 Hz interrupt flag set.
1 (R/W): Enable interrupt flag set
0 (R/W): Disable interrupt flag set (default)

Note: Even if you set this bit to 0 when the SIF1, SIF10, SIF100, (D[2:0]/SWT_IFLG register) is 1, interrupt request to CPU will not be disabled.If you want to disable interrupt request, use interrupt mask function in Interrupt Controller (ITC).