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S1C17 Series Technical Manual Errata

ITEM Countermeasure in case of display the LCD ghost			
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(Add)

17.6.1 Display On/Off

In the case of display the LCD ghost(LCD On mode)

In the case of display the LCD ghost, it may be improved by the following sequences

At the All off;

1. select reference voltage :VC1 (VCSEL/LCD_VREG register=0x0)
2. select All off (static) (DSPC[1:0]/LCD_DCTL register=0x3)
3. LCD Booster clock :Off (LCDBCLKE/LCD_BCLK register=0x0)
4. LCDCLK :Off (LCDTCLKE/LCD_TCLK register=0x0)

At the All on;

1. LCDCLK :On (LCDTCLKE/LCD_TCLK register=0x1)
2. LCD Booster clock :On (LCDBCLKE/LCD_BCLK register=0x1)
3. select reference voltage (VCSEL/LCD_VREG register=0x*)
4. select display mode (DSPC[1:0]/LCD_DCTL register=0x*)

Notes): In the All off (static) state, an electric current of about 1uA is added.

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ITEM About the CBUFEN register of T16A/T16A2

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(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.

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(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.