Apr/17/2017

errata_c17601_12

S1C17 Family Technical Manual Errata

ITEM **A part of shipping form is discontinued**			
Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	Configuration as shipped	1-2

1.1 Features

(Error)

●Configuration as shipped

- TQFP13-64 10 mm x 10 mm body, 0.5 mm pitch
- VFBGA8H-81 8 mm x 8 mm, body, 0.8 mm pitch
- Bare chip 100 µm pitch

(Correct)

●Configuration as shipped

- TQFP13-64 10 mm x 10 mm body, 0.5 mm pitch
- VFBGA8H-81 8 mm x 8 mm, body, 0.8 mm pitch #1
- Bare chip 100 µm pitch

#1 : VFBGA8H-81 is discontinued.

Aug/28/2013

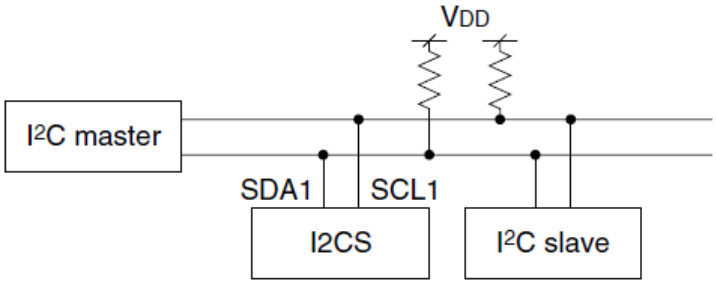
errata_c17601_11

S1C17 Family Technical Manual Errata

ITEM **I2C Slave Input/Output Pins**			
Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	21.2 I2C Slave Input/Output Pins	21-2
S1C17611 Technical Manual	411882301	21.2 I2C Slave Input/Output Pins	21-2
S1C17706 Technical Manual	412026401	18.2 I2CS Input/Output Pins	18-1
S1C17002 Technical Manual	411554402	V.3.2 I2C Slave I/O Pins	V-3-2
S1C17003 Technical Manual	411635102	21.2 I2C Slave Input/Output Pins	21-2
S1C17803 Technical Manual	411820401	21.2 I2CS Input/Output Pins	21-2

(Addition)

Note: The pins go to high impedance status when the port function is switched. The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDDwith an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Aug/28/2013

errata_c17601_10

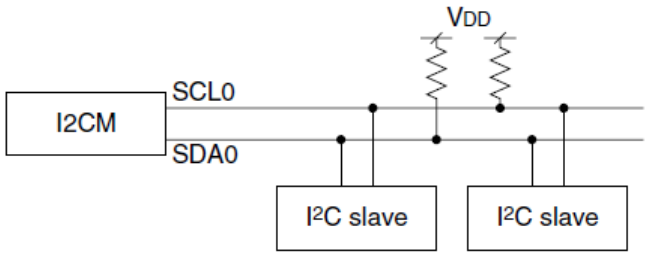
S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412301	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554402	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Aug/20/2010

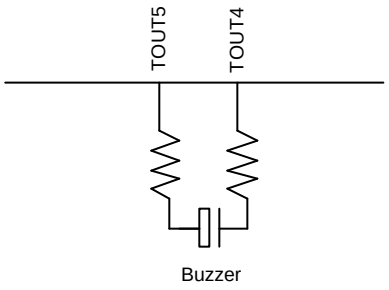
errata_c17601_9

S1C17 Manual errata

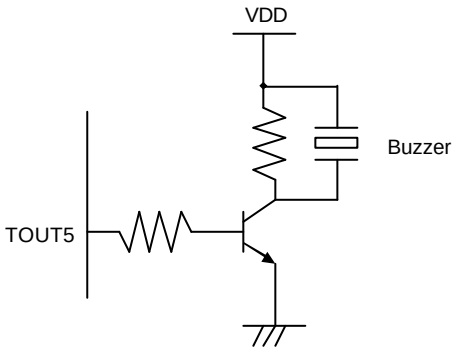
ITEM: Basic External Connection Diagram		
Object manuals	Document code	Object number
S1C17705	411706600	P26-1
S1C17711	411905600	P26-1
S1C17121	411723700	P29-1
S1C17601	411805700	P29-1
S1C17611	411882300	P29-1
S1C17621/602/622/604/624	411914900	P30-1

P26-1(S1C17705)

(Error)

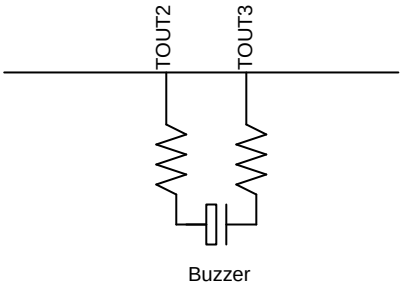


(Correct)

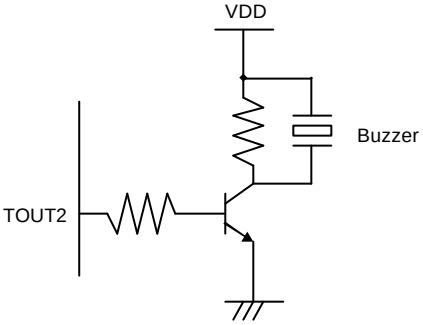


P26-1(S1C17711)

(Error)



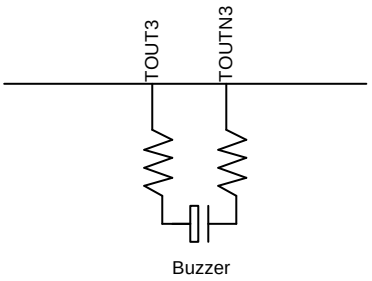
(Correct)



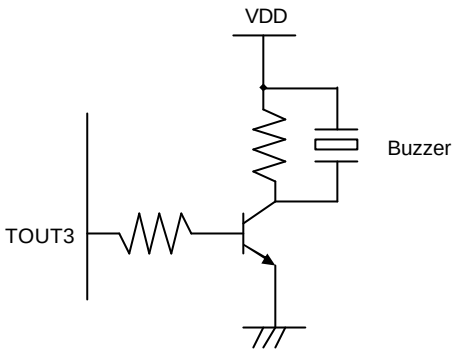
P29-1(S1C17121, S1C17601, S1C17611)

P30-1(S1C17621/602/622/604/624)

(Error)



(Correct)



Aug/10/2010

errata_c17601_8

S1C17 Manual errata

ITEM: SPI Clock		
Object manuals	Document code	Object number
S1C17121	411723700	P19-3
S1C17702	411581700	P19-3
S1C17003	411635100	P19-3
S1C17601	411805700	P19-3
S1C17611	411882300	P19-3
S1C17705	411706600	P15-2
S1C17621/S1C17602/S1C17622/ S1C17604/S1C17624	411914900	P19-3

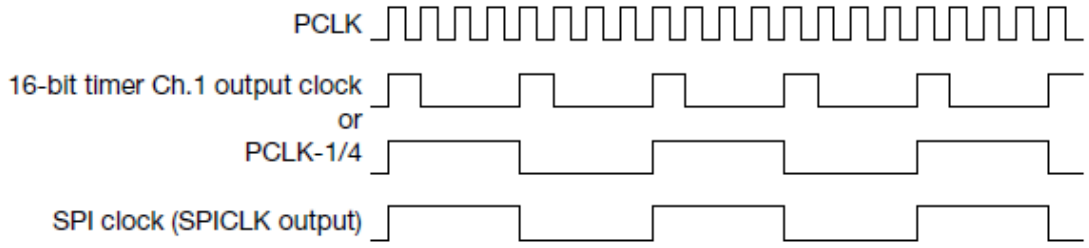
P19-3(S1C17602,S1C17121,S1C17702,S1C17003,S1C17601,S1C17611)

(Error)

The Master mode SPI uses the internal clock output by the 16-bit timer Ch.1 as SPI clock. This clock is output from the SPICLK pin to slave device while also driving the shift register. Use the MCLK(D9/SPI_CTL register) to select to use the 16-bit timer ch.1 output clock or PCLK-1/4 clock. Setting MCLK to 1 selects the 16-bit timer Ch.1 output clock; setting to 0 selects to 0 selects the PCLK-1/4 clock.

*MCLK: SPI Clock Source Select Bit in the SPI Control(SPI_CTL)Register(D9/0x4326)

Using the 16-bit timer Ch.1 output clock enables programmable transfer rates. For more information on 16-bit timer control, see ”11 16-bit Timer(T16).”

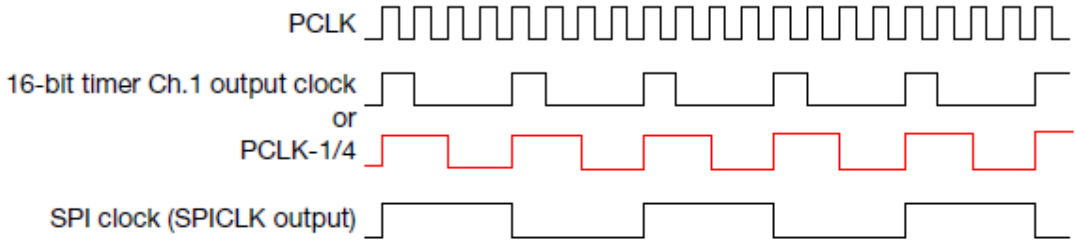


(Correct)

The Master mode SPI uses the internal clock output by the 16-bit timer Ch.1 as SPI clock. This clock is output from the SPICLK pin to slave device while also driving the shift register. Use the MCLK(D9/SPI_CTL register) to select to use the 16-bit timer ch.1 output clock or PCLK-1/4 clock is used. Setting MCLK to 1 selects the 16-bit timer Ch.1 output clock; setting to 0 selects to 0 selects the PCLK-1/4 clock.

*MCLK: SPI Clock Source Select Bit in the SPI Control(SPI_CTL)Register(D9/0x4326)

Using the 16-bit timer Ch.1 output clock enables programmable transfer rates. For more information on 16-bit timer control, see ”11 16-bit Timer(T16).”



P15-2(S1C17705)

(Error)

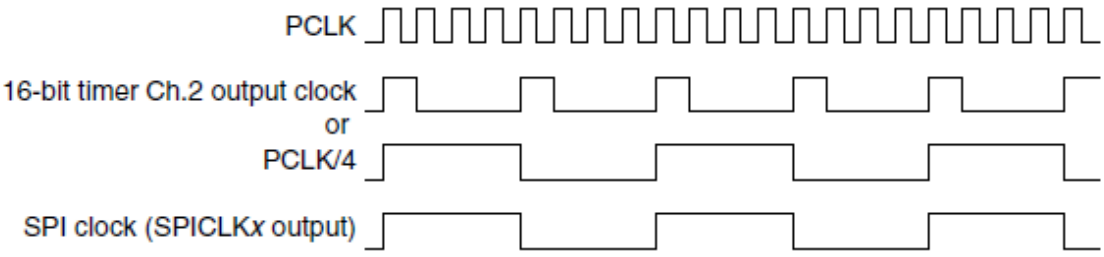


Figure 15.3.1 Master Mode SPI Clock

(Correct)

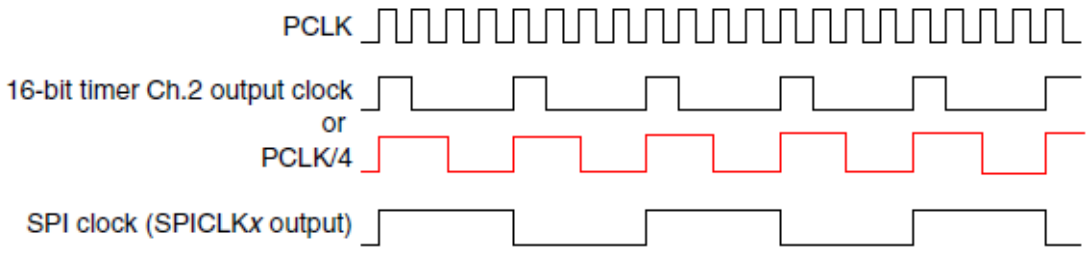


Figure 15.3.1 Master Mode SPI Clock

P19-3(S1C17621/S1C17602/S1C17622/S1C17604/S1C17624)

(Error)

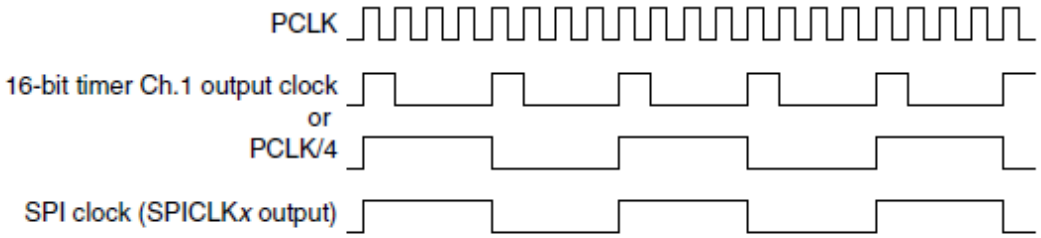


Figure 19.3.1 Master Mode SPI Clock

(Correct)

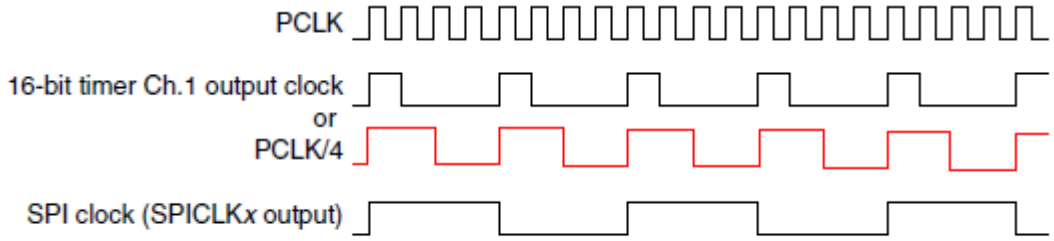


Figure 19.3.1 Master Mode SPI Clock

Jun/10/2010

errata_c17601_7

S1C17 Manual errata

ITEM: Input/Output Port Chattering Filter Function (P)			
Object manuals	Document codes	Items	Pages
S1C17121	411723701	10.6 P0 and P1 Port Chattering Filter Function 10.8 Control Register Details 10.9 Precautions	10-7 10-20 10-32
S1C17554/564	411914400	8.5 P0-P3 Port Chattering Filter Function 8.8 Control Register Details	8-4 8-10
S1C17601	411805700	10.6 P0 and P1 Port Chattering Filter Function 10.8 Control Register Details 10.9 Precautions	10-7 10-20 10-29
S1C17611	411882300	10.6 P0 and P1 Port Chattering Filter Function 10.8 Control Register Details 10.9 Precautions	10-7 10-20 10-28
S1C17624/604/622/602/621	411914900	9.6 P0 and P1 Port Chattering Filter Function 9.9 Control Register Details	9-4 9-11
S1C17705	411706600	8.6 P0-P3 Port Chattering Filter Function 8.9 Control Register Details	8-4 8-10
S1C17711	411905600	8.6 P0-P3 Port Chattering Filter Function 8.9 Control Register Details	8-4 8-10

Jun/10/2010

errata_c17601_7

(Correct)

(1) Add following description to the note of "Chattering Filter Function".

(2) Add following description to the note of “Control Register Details /Px_CHAT register".

(3) Add following description to "P0/P1 Port chattering filter circuit" of “Precautions”. (S1C17121/601/611)

• An unexpected interrupt may occur after SLEEP status is canceled if the slp instruction is executed while the chattering filter function is enabled. The chattering filter must be disabled before placing the CPU into SLEEP status.

Jun/10/2010

errata_c17601_6

S1C17 Manual errata

ITEM: Data Transmit Control (I2CS)			
Object manuals	Document codes	Items	Pages
S1C17002	411554401	V.3.5 Data Transmit/Receive Control	V-3-7
S1C17003	411645101	21.5 Data Transmit/Receive Control	21-7
S1C17121	411723701	21.5 Data Transmit/Receive Control	21-7
S1C17554/564	411914400	18.5 Data Transmit/Receive Control	18-4
S1C17601	411805700	21.5 Data Transmit/Receive Control	21-7
S1C17611	411882300	21.5 Data Transmit/Receive Control	21-7
S1C17624/604/622/602/621	411914900	21.5 Data Transmit/Receive Control	21-4
S1C17705	411706600	17.5 Data Transmit/Receive Control	17-4
S1C17711	411905600	17.5 Data Transmit/Receive Control	17-4

(Error)

Data transmission

When the clock stretch function is disabled (default)

Transmit data must be written to SDATA[7:0] within 1 cycle of the I2C clock (SCL* input clock) after TXEMP has been set to 1. This time is not enough for data preparation, so write transmit data before TXEMP has been set to 1. If the previous transmit data is still stored in SDATA[7:0], it is overwritten with the new data to be transferred. Therefore, the clear operation (see below) using TBUF_CLR is unnecessary.

When the clock stretch function is enabled

The master device is placed into wait status by the clock stretch function, so transmit data can be written after TXEMP is set. However, if the previous transmit data is still stored in SDATA[7:0], it will be sent immediately after TXEMP has been set. In order to avoid this problem, clear the I2CS_TRNS register using TBUF_CLR/I2CS_CTL register before this module is selected as the slave device. The I2CS_TRNS register is cleared by writing 1 to TBUF_CLR then writing 0 to it.

It is not necessary to clear the I2CS_TRNS register if the first transmit data is written before TXEMP has been set.

(Correct)

Data transmission

When the clock stretch function is disabled (default)

Transmit data must be written to SDATA[7:0] within 1 cycle of the I2C clock (SCL* input clock) after TXEMP has been set to 1. This time is not enough for data preparation, so write transmit data before TXEMP has been set to 1. If the previous transmit data is still stored in SDATA[7:0], it is overwritten with the new data to be transferred. Therefore, the clear operation (see below) using TBUF_CLR is unnecessary.

When the asynchronous address detection function is used, the data written before ASDET_EN is reset in 0 becomes invalid. Therefore, the transmission data must be written, after TXEMP has been set to 1.

When the clock stretch function is enabled

The master device is placed into wait status by the clock stretch function, so transmit data can be written after TXEMP is set. However, if the previous transmit data is still stored in SDATA[7:0], it will be sent immediately after TXEMP has been set. In order to avoid this problem, clear the I2CS_TRNS register using TBUF_CLR/I2CS_CTL register before this module is selected as the slave device. The I2CS_TRNS register is cleared by writing 1 to TBUF_CLR then writing 0 to it.

It is not necessary to clear the I2CS_TRNS register if the first transmit data is written before TXEMP has been set.

When the asynchronous address detection function is used, the data written before ASDET_EN is reset in 0 becomes invalid. Therefore, the transmission data must be written, after TXEMP has been set to 1.

May/11/2010

errata_c17601_5

S1C17 Manual errata

ITEM:

Object manuals	Document codes	Items	Pages
S1C17704 technical manual	411511902	18.10 Precautions	18-21
S1C17702 technical manual	411581701	18.10 Precautions	18-21
S1C17705 technical manual	411706600	14.9 Control Register Details	14-10
S1C17601 technical manual	411805700	18.10 Precautions	18-21
S1C17602 technical manual	411620100	18.10 Precautions	18-21
S1C17611 technical manual	411882300	18.10 Precautions	18-21
S1C17121 technical manual	411723701	18.10 Precautions	18-21
S1C17003 technical manual	411635101	18.10 Precautions	18-21

(Error)

For S1C17705

The following UART bits should be set with transfers disabled (RXEN = 0).

.....

All UART_CTLx register bits other than RXEN (RBFI, TIEN, RIEN, REIEN, TEIEN)

.....

For S1C17704

• Before setting the bits listed below, make sure the transmit and receive operations are disabled (RXEN = 0).

.....

- All bits (RBFI, TIEN, RIEN, and REIEN except RXEN) of the UART_CTL register

.....

For Others

• The following UART bits should be set with transfers blocked (RXEN = 0).

.....

- All UART_CTL register (0x4104) bits other than RXEN (RBFI, TIEN, RIEN, REIEN)

.....

(Correct)

• The following UART bits should be set with transfers disabled (RXEN = 0).

.....

- RBFI bit in the UART_CTL*x* register

.....

Mar/03/2010

errata_c17601_4

S1C17 Manual errata

ITEM: I2CM Interrupts

Object manuals	Document codes	Items	Pages
S1C17701 technical manual	411089903	20.6 I2C Interrupt	20-11
S1C17704 technical manual	411511902	20.6 I2C Interrupt	20-11
S1C17702 technical manual	411581701	20.6 I2C Interrupt	20-10
S1C17705 technical manual	411706600	16.6 I2CM Interrupts	16-6
S1C17601 technical manual	411805700	20.6 I2C Master Interrupts	20-10
S1C17602 technical manual	411620100	20.6 I2C Master Interrupts	20-10
S1C17611 technical manual	411882300	20.6 I2C Master Interrupts	20-10
S1C17121 technical manual	411723701	20.6 I2C Master Interrupts	20-10
S1C17001 technical manual	411412301	20.6 I2C Interrupt	250
S1C17003 technical manual	411635101	20.6 I2C Master Interrupts	20-10

(Error)

Transmit buffer empty interrupt

To use this interrupt, set TINTE/I2CM_ICTL register to 1. If TINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If transmit buffer empty interrupts are enabled (TINTE = 1), an interrupt request is output to the ITC as soon as the transmit data set in RTDT[7:0]/I2CM_DAT register is transferred to the shift register.

An interrupt occurs if other interrupt conditions are satisfied.

Receive buffer full interrupt

To use this interrupt, set RINTE/I2CM_ICTL register to 1. If RINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If receive buffer full interrupts are enabled (RINTE = 1), an interrupt request is output to the ITC as soon as the data received in the shift register is loaded to RTDT[7:0].

An interrupt occurs if other interrupt conditions are met.

For more information on interrupt processing, see the “Interrupt Controller (ITC)” chapter.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set TINTE/I2CM_ICTL register to 1. If TINTE is set to 0 (default),

interrupt requests for this cause will not be sent to the ITC.
If transmit buffer empty interrupts are enabled (TINTE = 1), an interrupt request is output to the ITC as soon as the transmit data set in RTDT[7:0]/I2CM_DAT register is transferred to the shift register.
An interrupt occurs if other interrupt conditions are satisfied.
Transmit buffer empty interrupt occurs when the data was only sent.

- The clear method of transmit buffer empty flag

  Write the data to RTDT/I2CM_DAT.

  When TXE/I2CM_DAT is 0, the data doesn't send and the flag is only cleared.

Receive buffer full interrupt

To use this interrupt, set RINTE/I2CM_ICTL register to 1. If RINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.
If receive buffer full interrupts are enabled (RINTE = 1), an interrupt request is output to the ITC as soon as the data received in the shift register is loaded to RTDT[7:0].
An interrupt occurs if other interrupt conditions are met.
Receive buffer full interrupt occurs when the data was only received.

- The clear method of receive buffer full flag

  Read the data from RTDT/I2CM_DAT.

NOTE: When I2CM interrupt occurs, decide the transmit buffer empty interrupt or the receive buffer full interrupt by the program sequence of the I2C master. There're not registers to decide which interrupt occurred.

For more information on interrupt processing, see the "Interrupt Controller (ITC)" chapter.

Mar/03/2010

errata_c17601_3

S1C17 Manual errata

ITEM: Heavy Load Protection Function

Object manuals	Document codes	Items	Pages
S1C17702 technical manual	411581701	4.4 Heavy Load Protection Function	4-5
S1C17705 technical manual	411706600	4.5 Heavy Load Protection Function	4-4
S1C17601 technical manual	411805700	4.4 Heavy Load Protection Function	4-4
S1C17602 technical manual	411620100	4.4 Heavy Load Protection Function	4-4
S1C17611 technical manual	411882300	4.4 Heavy Load Protection Function	4-4

(Error)

The internal logic voltage regulator enters heavy load protection mode by writing 1 to the HVLD/VD1_CTL register and it ensures stable VD1 output. Use the heavy load protection function when a heavy load such as a lamp or buzzer is driven with a port output.

(Correct)

The internal logic voltage regulator enters heavy load protection mode by writing 1 to the HVLD/VD1_CTL register and it ensures stable VD1 output. ~~Use the heavy load protection function when a heavy load such as a lamp or buzzer is driven with a port output~~. If the unstable operation occurs by programming operations as the below, Use the heavy load protection function.

- The case of driving the high current consumption such as diode, buzzer and so on by the port outputs; set the heavy load protection function to enable during driving the diode or buzzer.
- The case of having the high current consumption difference between high clock and low clock using by system clock; set the heavy load protection function to enable during several ten micro seconds from in front of the change to end of the change.
- The case of having the high current consumption difference between HALT/SLEEP mode and those releases, and of changing frequently them; set the heavy load protection function to enable during repeating their process.

NOTE: Release the heavy load protection function after the unstable operations finished. In addition, If the unstable operations occur frequently, set the heavy load protection function to enable during these operations.

Dec/28/2009

errata_c17601_2

S1C17 Manual errata

ITEM: Mistakes of a method to clear receive data buffer.			
Object manuals	Document codes	Items	Pages
S17C17601 Technical Manual	411805700	18 UART	18-7, 18-19, 18-21

P18-7(S1C17601)

(Error)

Setting the RXEN bit to 0 empties the transmission and receive data buffers, clearing any remaining data. The data being transferred cannot be guaranteed if RXEN is set to 0 while data is being sent or received.

(Correct)

Setting the RXEN bit to 0 empties the transmission ~~and receive~~ data buffers, clearing any remaining data. The data being transferred cannot be guaranteed if RXEN is set to 0 while data is being sent or received.

P18-19(S1C17601)

(Error) **D0 RXEN: UART Enable Bit**

Permits data transfer by the UART.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Set RXEN to 1 before starting UART transfers. Setting RXEN to 0 will stop data transfers. Set the transfer conditions while RXEN is 0.

Preventing transfers by writing 0 to RXEN also clears transfer data buffers.

(Correct) **D0 RXEN: UART Enable Bit**

Permits data transfer by the UART.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Set RXEN to 1 before starting UART transfers. Setting RXEN to 0 will stop data transfers. Set the transfer conditions while RXEN is 0.

Preventing transfers by writing 0 to RXEN also clears ~~transfer~~ transmit data buffer~~s~~.

P18-21(S1C17601)

(Error)

Preventing transfer by setting RXEN to 0 clears (initializes) transfer data buffers. Before writing 0 to RXEN, confirm the absence of data in the buffers awaiting transmission or reading.

(Correct)

Preventing transfer by setting RXEN to 0 clears (initializes) transfer data buffers. Before writing 0 to RXEN, confirm the absence of data in the buffers awaiting transmission ~~or reading~~.

Dec/28/2009

errata_c17601_1

S1C17 Manual errata

ITEM: Mistakes of a method to reset of receive err flags.			
Object manuals	Document codes	Items	Pages
S17C17601 Technical Manual	411805700	18 UART	18-14

P18-14(S1C17601

(Error) **D6 FER: Framing Error Flag Bit**

Indicates whether a framing error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

FER is set to 1 when a framing error occurs. Framing errors occur when data is received with the stop bit set to 0. FER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

D5 PER: Parity Error Flag Bit

Indicates whether a parity error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

PER is set to 1 when a parity error occurs. Parity checking is enabled only when PREN/ UART_MOD*x* register is set to 1 and is performed when received data is transferred from the shift register to the receive data buffer. PER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

D4 OER: Overrun Error Flag Bit

Indicates whether an overrun error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

OER is set to 1 when an overrun error occurs. Overrun errors occur when data is received in the shift register when the receive data buffer is already full and additional data is sent. The receive data buffer is not overwritten even if this error occurs. The shift register is overwritten as soon as the error occurs.

OER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

(Correct) **D6 FER: Framing Error Flag Bit**

Indicates whether a framing error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

FER is set to 1 when a framing error occurs. Framing errors occur when data is received with the stop bit set to 0. FER is reset by writing 1 ~~or by setting RXEN/UART_CTL*x* register to 0~~.

D5 PER: Parity Error Flag Bit

Indicates whether a parity error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

PER is set to 1 when a parity error occurs. Parity checking is enabled only when PREN/ UART_MOD*x* register is set to 1 and is performed when received data is transferred from the shift register to the receive data buffer. PER is reset by writing 1 ~~or by setting RXEN/UART_CTL*x* register to 0~~.

D4 OER: Overrun Error Flag Bit

Indicates whether an overrun error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

OER is set to 1 when an overrun error occurs. Overrun errors occur when data is received in the shift register when the receive data buffer is already full and additional data is sent. The receive data buffer is not overwritten even if this error occurs. The shift register is overwritten as soon as the error occurs.

OER is reset by writing 1 ~~or by setting RXEN/UART_CTL*x* register to 0~~.