Jul/4/2014

errata_c17554/564_6

S1C17 Series Technical Manual Errata

ITEM Add shipping form (VFBGA5H-81)

Object manual	Document code	Object Item	Page
S1C17554/564 Technical Manual	411914403	1.1 Features	1-2
		1.3.2 S1C17564 Pin Configuration Diagram	1-9
		1.3.3 Pin Descriptions	1-12
		26 Package	26-1

1.1 Features (P.1-2)

(Error)

Shipping form

-

(Correct)

Shipping form

VFBGA5H-81 (5mm x 5mm x 1.0mm, ball pitch：0.5mm)

1.3.2 S1C17564 Pin Configuration Diagram (P.1-9)

(Error)

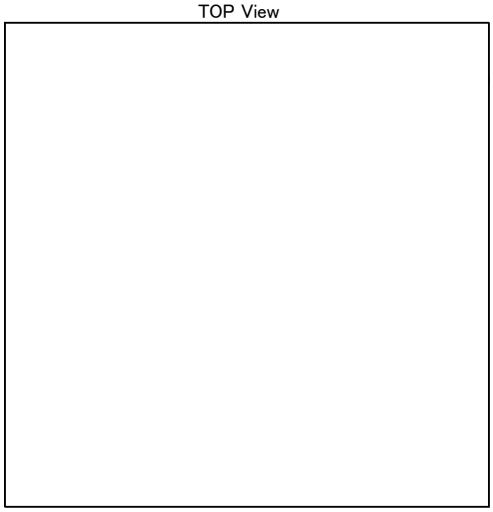
-

(Correct)

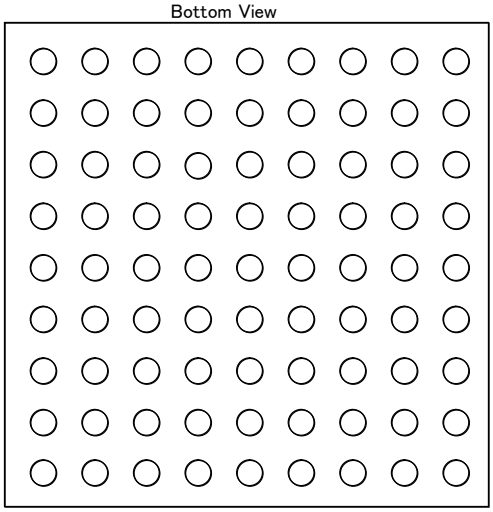
Add

S1C17564 Pin Configuration Diagram(VFBGA5H-81)

TOP View



Bottom View



TOP View

	1	2	3	4	5	6	7	8	9
A	NC	P00 AIN0	P02 AIN2 US_SSI0	AVDD	VSS	P42 SCLK0 TOUT1 CAP1	P40 SIN0 TOUT6 CAP6	#RESET	NC
B	P10 SDI0	P01 AIN1	P03 AIN3 US_SSI1	P32 TOUT4 CAP4 FOUTA	HVDD	P41 SOUT0 TOUT7 CAP7	LVDD	REGEN	VSS
C	P12 SPICLK0	P50 US_SDI0	P11 SDO0	VSS	P17 SCL0	P45 (EXCL0) SDA0	VIN	VOUT	P23 (EXCL2) SDI2
D	LVDD	P13 #SPISS0 TOUT5 CAP5	HVDD	VSS	VSS	VSS	P22 (EXCL1) FOUTB	P21 TOUT3 CAP3	P20 TOUT2 CAP2
E	P51 US_SDO0	P14 SIN1 SDI1	P15 SOUT1 SDO1	VSS	VSS	VSS	HVDD	VSS	OSC4
F	P16 SCLK1 SPICLK1	P43 SDA1 REMI	P44 SCL1 REMO	VSS	VSS	VSS	P54 US_SDO1	VSS	OSC3
G	HVDD	P24 (EXCL3) SDO2	VSS	LVDD	DST2 P37	TEST	P34 REMO #SPISS1	VPP	OSC2
H	VSS	P25 #BFR #SPISS2	P26 SDA1	HVDD	P53 US_SDI1	LVDD	P33 REMI SPICLK2	VSS	OSC1
J	NC	P52 US_SCK0	P27 SCL1	P30 TOUT0 CAP0	P31 #BFR ADTRG	DSIO P36	DCLK P35	P55 US_SCK1	NC

1.3.3 Pin Descriptions (P.1-12)

(Error)

-

(Correct)

Name	I/O	Default status	Function	S1C17564 VFBGA
HVDD	–	–	I/O power supply pins (1.65 to 5.5 V)	B5, D3, E7, G1, H4
LVDD	–	–	Core power supply pins (1.65 to 1.95 V)	D1, G4, H6, B7
VSS	–	–	GND pins	A5, B9, C4, D4, D5, D6, E4, E5, E6, E8, F4, F5, F6, F8, G3, H1, H8
VPP	–	–	Flash programming/erasing power supply pin (7/7.5 V)	G8
AVDD	–	–	Analog power supply pin (2.7 to 5.5 V)	A4
VIN	–	–	Regulator input pin (2.0 to 5.5 V)	C7
VOUT	–	–	Regulator output pin (1.8 V)	C8
REGEN	I	I	Regulator enable input pin	B8
OSC3	I	I	OSC3 oscillator input or external clock (LVDD level) input pin	F9
OSC4	O	O	OSC3 oscillator output pin	E9
OSC1	I	I	OSC1 oscillator input or external clock (LVDD level) input pin	H9
OSC2	O	O	OSC1 oscillator output pin	G9
#RESET	I	I(Pull-up)	Initial reset input pin	A8
TEST	I	I(Pull-down)	Test input pin (Connect to VSS for normal operation.)	G6
P00	I/O	I(Pull-up)	I/O port pin	A2
AIN0	I		A/D converter Ch.0 analog signal input pin	
P01	I/O	I(Pull-up)	I/O port pin	B2
AIN1	I		A/D converter Ch.1 analog signal input pin	
P02	I/O	I(Pull-up)	I/O port pin	A3
AIN2	I		A/D converter Ch.2 analog signal input pin	
US_SSI0	I/O		USI Ch.0 data input/output pin (S1C17564)	
P03	I/O	I(Pull-up)	I/O port pin	B3
AIN3	I		A/D converter Ch.3 analog signal input pin	
US_SSI1	I/O		USI Ch.1 data input/output pin (S1C17564)	
P10	I/O	I(Pull-up)	I/O port pin	B1
SDI0	I		SPI Ch.0 data input pin	
P11	I/O	I(Pull-up)	I/O port pin	C3
SDO0	O		SPI Ch.0 data output pin	
P12	I/O	I(Pull-up)	I/O port pin	C1
SPICLK0	I/O		SPI Ch.0 clock input/output pin	
P13	I/O	I(Pull-up)	I/O port pin	D2
#SPISS0	I		SPI Ch.0 slave select signal input pin	
TOUT5	O		T16A Ch.2 TOUT B signal output pin	
CAP5	I		T16A Ch.2 capture B trigger signal input pin	
P14	I/O	I(Pull-up)	I/O port pin	E2
SIN1	I		UART Ch.1 data input pin	
SDI1	I		SPI Ch.1 data input pin	
P15	I/O	I(Pull-up)	I/O port pin	E3
SOUT1	O		UART Ch.1 data output pin	
SDO1	O		SPI Ch.1 data output pin	
P16	I/O	I(Pull-up)	I/O port pin	F1
SCLK1	I		UART Ch.1 external clock input pin	
SPICLK1	I/O		SPI Ch.1 clock input/output pin	
P17	I/O	I(Pull-up)	I/O port pin	C5
SCL0	I/O		I2C master SCL input/output pin	
P20	I/O	I(Pull-up)	I/O port pin	D9
TOUT2	O		T16A Ch.1 TOUT A signal output pin	
CAP2	I		T16A Ch.1 capture A trigger signal input pin	
P21	I/O	I(Pull-up)	I/O port pin	D8
TOUT3	O		T16A Ch.1 TOUT B signal output pin	
CAP3	I		T16A Ch.1 capture B trigger signal input pin	
P22 (EXCL1)	I/O	I(Pull-up)	I/O port pin (T16A Ch.1 external clock input pin)	D7
FOUTB	O		Clock output pin	
P23 (EXCL2)	I/O	I(Pull-up)	I/O port pin (T16A Ch.2 external clock input pin)	C9
SDI2	I		SPI Ch.2 data input pin	
P24 (EXCL3)	I/O	I(Pull-up)	I/O port pin (T16A Ch.3 external clock input pin)	G2
SDO2	O		SPI Ch.2 data output pin	
P25	I/O	I(Pull-up)	I/O port pin	H2
#BFR	I		I2C slave bus free request input pin	
#SPISS2	I		SPI Ch.2 slave select signal input pin	
P26	I/O	I(Pull-up)	I/O port pin	H3
SDA1	I/O		I2C slave data input/output pin	
P27	I/O	I(Pull-up)	I/O port pin	J3
SCL1	I/O		I2C slave SCL input/output pin	
P30	I/O	I(Pull-up)	I/O port pin	J4
TOUT0	O		T16A Ch.0 TOUT A signal output pin	
CAP0	I		T16A Ch.0 capture A trigger signal input pin	
P31	I/O	I(Pull-up)	I/O port pin	J5

#BFR	I		I2C slave bus free request input pin	
#ADTRG	I		A/D converter external trigger input pin	
P32	I/O	I(Pull-up)	I/O port pin	B4
TOUT4	O		T16A Ch.2 TOUT A signal output pin	
CAP4	I		T16A Ch.2 capture A trigger signal input pin	
FOUTA	O		Clock output pin	
P33	I/O	I(Pull-up)	I/O port pin	H7
REMI	I		REMC input pin	
SPICLK2	I/O		SPI Ch.2 clock input/output pin	
P34	I/O	I(Pull-up)	I/O port pin	G7
REMO	O		REMC output pin	
#SPISS1	I		SPI Ch.1 slave select signal input pin	
DCLK	O	O(H)	On-chip debugger clock output pin	J7
P35	I/O		I/O port pin	
DSIO	I/O	I(Pull-up)	On-chip debugger data input/output pin	J6
P36	I/O		I/O port pin	
DST2	O	O(L)	On-chip debugger status output pin	G5
P37	I/O		I/O port pin	
P40	I/O	I(Pull-up)	I/O port pin	A7
SIN0	I		UART Ch.0 data input pin	
TOUT6	O		T16A Ch.3 TOUT A signal output pin	
CAP6	I		T16A Ch.3 capture A trigger signal input pin	
P41	I/O	I(Pull-up)	I/O port pin	B6
SOUT0	O		UART Ch.0 data output pin	
TOUT7	O		T16A Ch.3 TOUT B signal output pin	
CAP7	I		T16A Ch.3 capture B trigger signal input pin	
P42	I/O	I(Pull-up)	I/O port pin	A6
SCLK0	I		UART Ch.0 external clock input pin	
TOUT1	O		T16A Ch.0 TOUT B signal output pin	
CAP1	I		T16A Ch.0 capture B trigger signal input pin	
P43	I/O	I(Pull-up)	I/O port pin	F2
SDA1	I/O		I2C slave data input/output pin	
REMI	I		REMC input pin	
P44	I/O	I(Pull-up)	I/O port pin	F3
SCL1	I/O		I2C slave SCL input/output pin	
REMO	O		REMC output pin	
P45 (EXCL0)	I/O	I(Pull-up)	I/O port pin (T16A Ch.0 external clock input pin)	C6
SDA0	I/O		I2C master data input/output pin	
P50	I/O	I(Pull-up)	I/O port pin	C2
US_SDI0	I/O		USI Ch.0 data input/output pin (S1C17564)	
P51	I/O	I(Pull-up)	I/O port pin	E1
US_SDO0	O		USI Ch.0 data output pin (S1C17564)	
P52	I/O	I(Pull-up)	I/O port pin	J2
US_SCK0	I/O		USI Ch.0 clock input/output pin (S1C17564)	
P53	I/O	I(Pull-up)	I/O port pin	H5
US_SDI1	I/O		USI Ch.1 data input/output pin (S1C17564)	
P54	I/O	I(Pull-up)	I/O port pin	F7
US_SDO1	O		USI Ch.1 data output pin (S1C17564)	
P55	I/O	I(Pull-up)	I/O port pin	J8
US_SCK1	I/O		USI Ch.1 clock input/output pin (S1C17564)	
N.C.			Unused terminal*	A1, A9, J1, J9

26 Package (P.26-1)

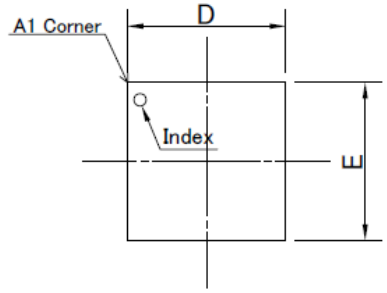
(Error)

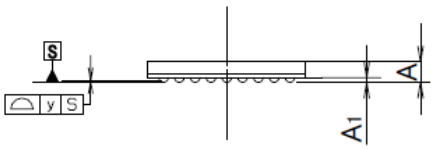
-

(Correct)

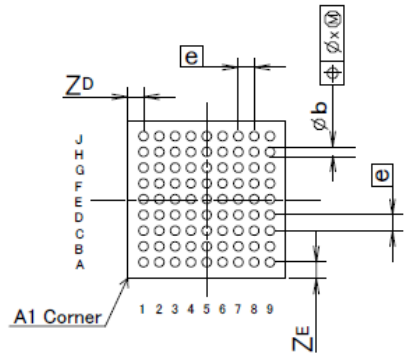
Add

Top View





Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	–	5	–
E	–	5	–
A	–	–	1.0
A_1	–	0.23	–
e	–	0.5	–
b	0.26	–	0.36
x	–	–	0.08
y	–	–	0.1
Z_D	–	0.5	–
Z_E	–	0.5	–

1 = 1mm

Jan/29/2014

errata_c17554/564_5

S1C17 Technical Manual Errata

ITEM: USI/USIL AC Characteristics			
Object manual	Document code	Object ITEM	Page
S1C17554/564 Technical Manual	411914403	24.11 USI Characteristics (S1C17564)	24-8

24-8

(Error)

SPI master mode (8 or 9 bits, normal mode)

Unless otherwise specified: HVDD = 1.65 to 5.5V, VSS = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85 + tPCLK	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

SPI master mode (8 or 9 bits, fast mode)

Unless otherwise specified: HVDD = 1.65 to 5.5V, VSS = 0V, Ta = -40 to 85°C

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	85	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

(Correct)

SPI master mode (8 or 9 bits, normal mode)

Unless otherwise specified: HVDD = 1.65 to 5.5V, VSS = 0V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	**(85 + tPCLK) x 2**	-	-	ns
spi_sdi setup time	tSDS	85 + tPCLK	-	-	ns

SPI master mode (8 or 9 bits, fast mode)

Unless otherwise specified: HVDD = 1.65 to 5.5V, VSS = 0V, Ta = -40 to 85°C

Item	記号	Min.	Typ.	Max.	Unit
spi_sck cycle time	tSPCK	**85 x 2**	-	-	ns
spi_sdi setup time	tSDS	85	-	-	ns

Dec/27/2011

errata_c17554/564_4

S1C17 Series Technical Manual Errata

ITEM About the CBUFEN register of T16A/T16A2

Object manual	Document code	Object Item	Page
S1C17624/604/622/602/621 Technical Manual	411914902	13.8 Control Register Details	13-14 13-15
S1C17705/703 Technical Manual	411706602	10.8 Control Register Details	10-19
S1C17706 Technical Manual	412026401	10.8 Control Register Details	10-17
S1C17711 Technical Manual	411905602	10.8 Control Register Details	10-14
S1C17554/564 Technical Manual	411914402	11.8 Control Register Details	11-14
S1C17651 Technical Manual	412120600	12.8 Control Register Details	12-13

Page 13-14 13-15 S1C624/604/622/602/621 Technical Manual

Page 10-17 S1C17706 Technical Manual

Page 12-13 S1C17651 Technical Manual

(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.

Page 13-14 13-15 S1C17705/703 Technical Manual

Page 10-14 S1C17711 Technical Manual

Page 11-14 S1C17554/564 Technical Manual

(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (CLKEN = 0) before setting CBUFEN.