Aug/28/2013

errata_c17001_9

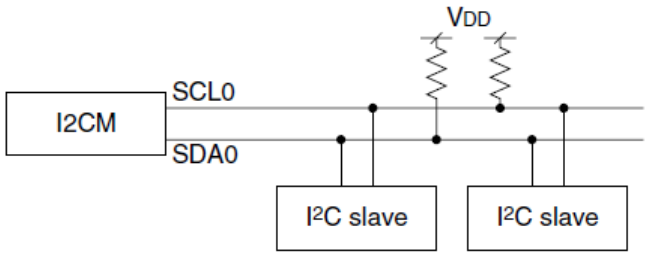
S1C17 Family Technical Manual Errata

ITEM **I2C Master Input/Output Pins**

Object manual	Document code	Object item	Page
S1C17601 Technical Manual	411805701	20.2 I2C Master Input/Output Pins	20-2
S1C17611 Technical Manual	411882301	20.2 I2C Master Input/Output Pins	20-2
S1C17701 Technical Manual	411089904	20.2 I2C I/O Pins	20-2
S1C17704 Technical Manual	411511903	20.2 I2C I/O Pins	20-2
S1C17706 Technical Manual	412026401	17.2 I2CM Input/Output Pins	17-1
S1C17001 Technical Manual	411412303	20.2 I2C Input/Output Pins	252
S1C17002 Technical Manual	411554403	V.2.2 I2C Master I/O Pins	V-2-2
S1C17003 Technical Manual	411635102	20.2 I2C Master Input/Output Pins	20-2
S1C17501 Technical Manual	411525602	VI.2.2 I2C I/O Pins	VI-2-2
S1C17801 Technical Manual	411390802	VI.2.2 I2C I/O Pins	VI-2-2
S1C17803 Technical Manual	411820401	20.2 I2CM Input/Output Pins	20-2

(Addition)

Note: The pins go to high impedance status when the port function is switched.
The SCL and SDA pins do not output a high level, so these lines should be pulled up to VDD with an external pull-up resistor. Be sure to avoid pulling these pins up to a voltage that exceeds the VDD level.



Nov/09/2012

errata_c17001_8

S1C17 Family Technical Manual Errata

ITEM About the Fine mode setting of T16E.			
Object manual	Document code	Object item	Page
S1C17001 Technical Manual	411412303	13.6 Clock Output Control	150
S1C17003 Technical Manual	411635102	13.6 Clock Output Control	13-8
S1C17624/604/622/621 Technical Manual	411914902	12.7 Clock Output Control	12-6
S1C17701 Technical Manual	411089905	13.6 Controlling Clock Output	13-8
S1C17702 Technical Manual	411581702	13.6 Clock Output Control	13-8
S1C17704 Technical Manual	411511903	13.6 Controlling Clock Output	13-8

Page 150 S1C17001 Technical Manual

Page 13-8 S1C17003 Technical Manual

Page 13-8 S1C17701 Technical Manual

Page 13-8 S1C17702 Technical Manual

Page 13-8 S1C17704 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(3) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Page 12-6 S1C17623/604/622/621 Technical Manual

Add following comment at Precautions of “Setting fine mode for clock output”.

(4) Use the Fine mode only for T16EDF = 0x0 (PCLK-1/1).

Mar/03/2010

errata_c17001_7

S1C17 Manual errata

ITEM: I2CM Interrupts

Object manuals	Document codes	Items	Pages
S1C17701 technical manual	411089903	20.6 I2C Interrupt	20-11
S1C17704 technical manual	411511902	20.6 I2C Interrupt	20-11
S1C17702 technical manual	411581701	20.6 I2C Interrupt	20-10
S1C17705 technical manual	411706600	16.6 I2CM Interrupts	16-6
S1C17601 technical manual	411805700	20.6 I2C Master Interrupts	20-10
S1C17602 technical manual	411620100	20.6 I2C Master Interrupts	20-10
S1C17611 technical manual	411882300	20.6 I2C Master Interrupts	20-10
S1C17121 technical manual	411723701	20.6 I2C Master Interrupts	20-10
S1C17001 technical manual	411412301	20.6 I2C Interrupt	250
S1C17003 technical manual	411635101	20.6 I2C Master Interrupts	20-10

(Error)

Transmit buffer empty interrupt

To use this interrupt, set TINTE/I2CM_ICTL register to 1. If TINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If transmit buffer empty interrupts are enabled (TINTE = 1), an interrupt request is output to the ITC as soon as the transmit data set in RTDT[7:0]/I2CM_DAT register is transferred to the shift register.

An interrupt occurs if other interrupt conditions are satisfied.

Receive buffer full interrupt

To use this interrupt, set RINTE/I2CM_ICTL register to 1. If RINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.

If receive buffer full interrupts are enabled (RINTE = 1), an interrupt request is output to the ITC as soon as the data received in the shift register is loaded to RTDT[7:0].

An interrupt occurs if other interrupt conditions are met.

For more information on interrupt processing, see the “Interrupt Controller (ITC)” chapter.

(Correct)

Transmit buffer empty interrupt

To use this interrupt, set TINTE/I2CM_ICTL register to 1. If TINTE is set to 0 (default),

interrupt requests for this cause will not be sent to the ITC.
If transmit buffer empty interrupts are enabled (TINTE = 1), an interrupt request is output to the ITC as soon as the transmit data set in RTDT[7:0]/I2CM_DAT register is transferred to the shift register.
An interrupt occurs if other interrupt conditions are satisfied.
Transmit buffer empty interrupt occurs when the data was only sent.

- The clear method of transmit buffer empty flag

  Write the data to RTDT/I2CM_DAT.

  When TXE/I2CM_DAT is 0, the data doesn't send and the flag is only cleared.

Receive buffer full interrupt

To use this interrupt, set RINTE/I2CM_ICTL register to 1. If RINTE is set to 0 (default), interrupt requests for this cause will not be sent to the ITC.
If receive buffer full interrupts are enabled (RINTE = 1), an interrupt request is output to the ITC as soon as the data received in the shift register is loaded to RTDT[7:0].
An interrupt occurs if other interrupt conditions are met.
Receive buffer full interrupt occurs when the data was only received.

- The clear method of receive buffer full flag

  Read the data from RTDT/I2CM_DAT.

NOTE: When I2CM interrupt occurs, decide the transmit buffer empty interrupt or the receive buffer full interrupt by the program sequence of the I2C master. There're not registers to decide which interrupt occurred.

For more information on interrupt processing, see the "Interrupt Controller (ITC)" chapter.

Dec/28/2009

errata_c17001_6

S1C17001 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C17001	411412300	1.3.1	12

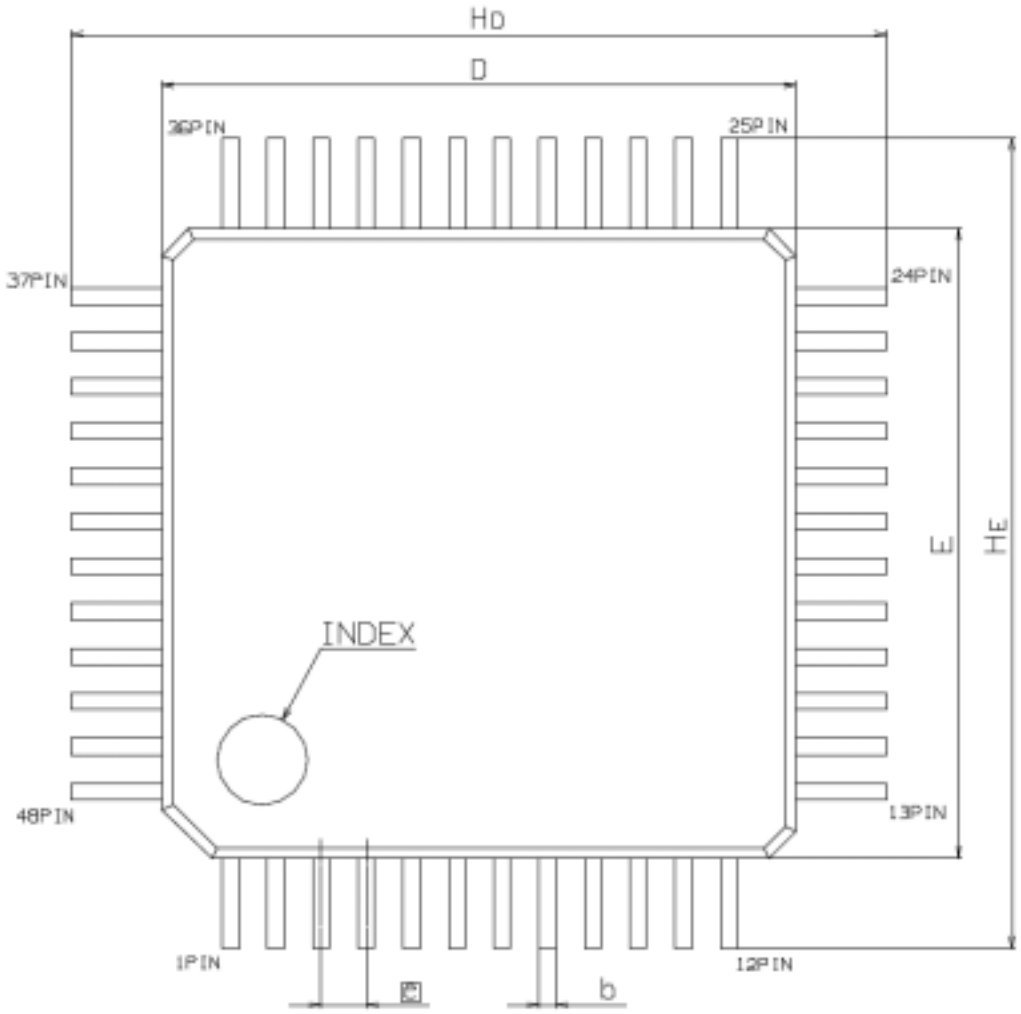
(Error)

1.3.1 There was not Chip and Package information after pin assignment (WCSP).

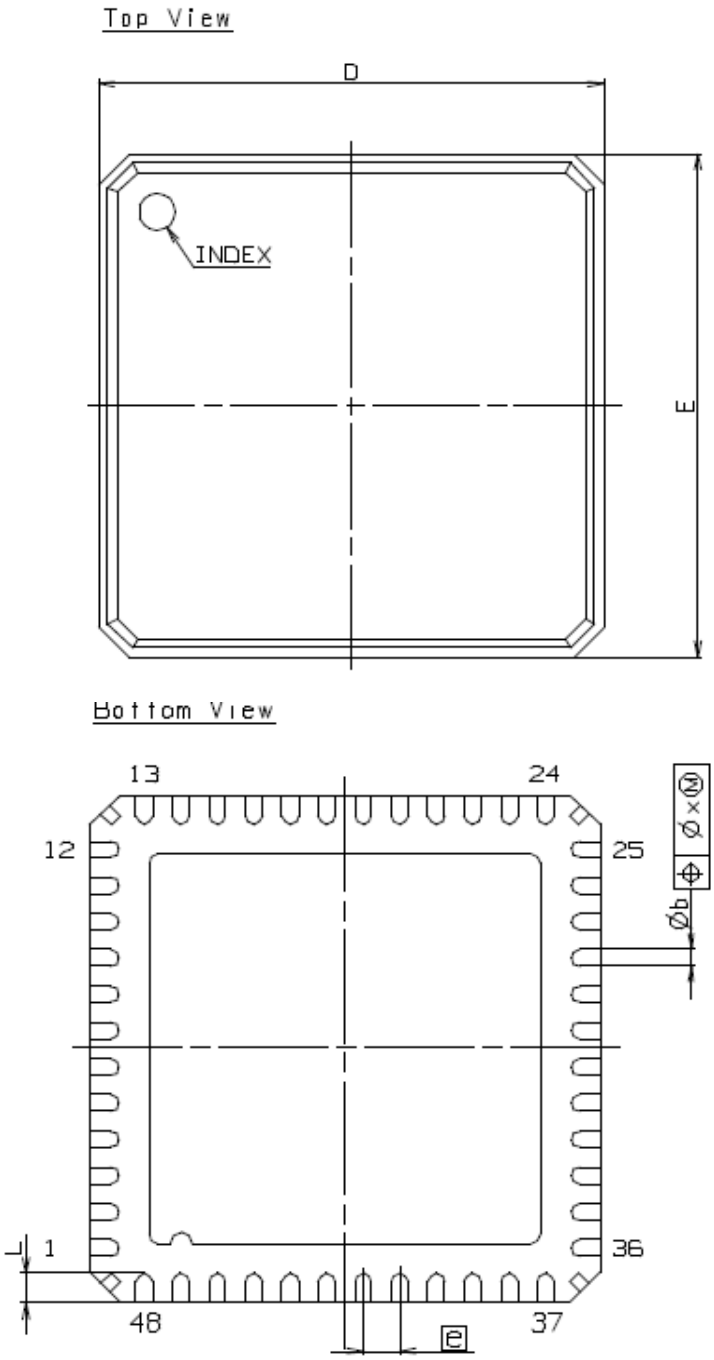
(Correct)

1.3.1 Chip and Package information are added after pin assignment (WCSP).

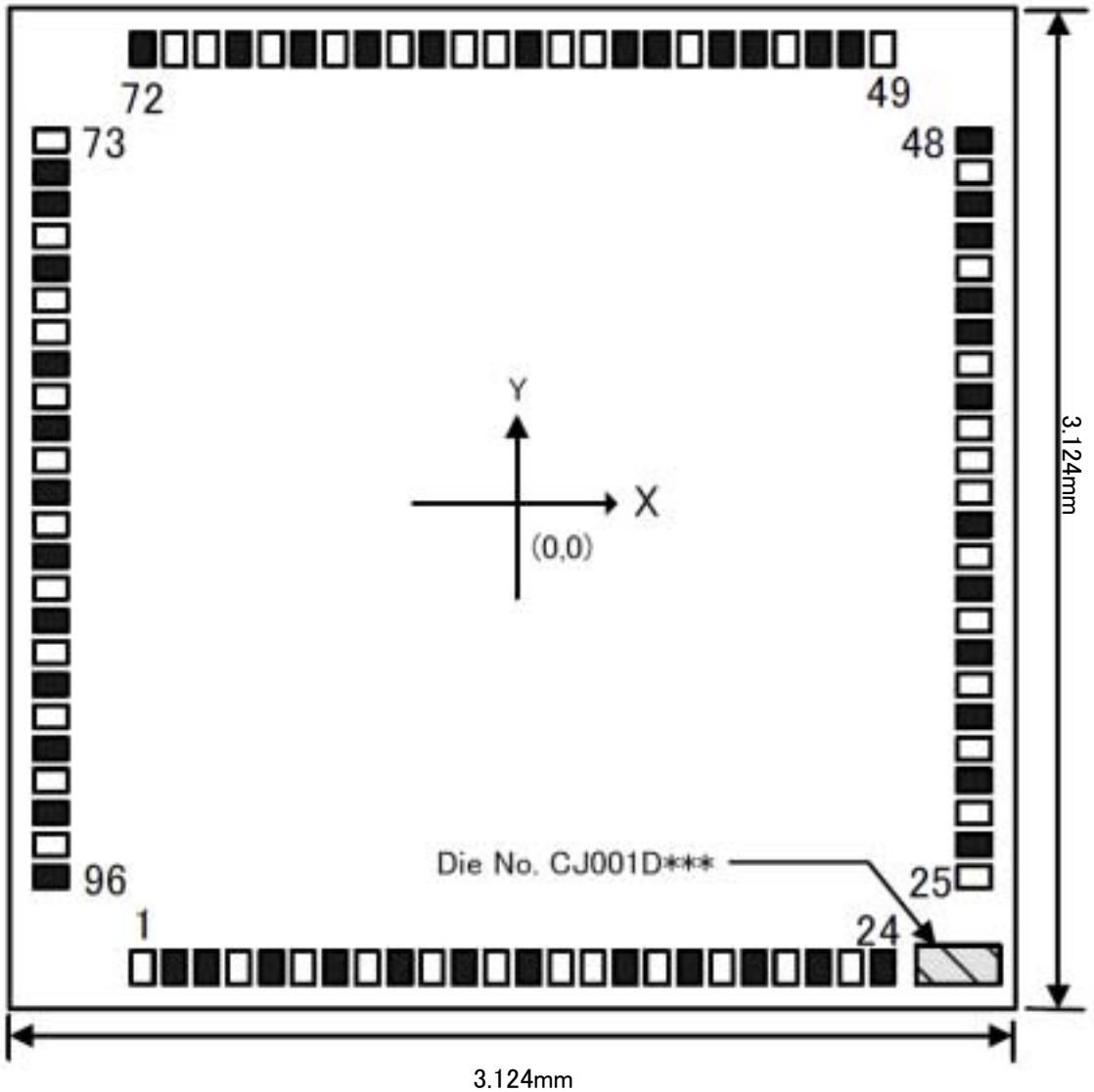
QFP12-48


HD
D
36PIN
25PIN
37PIN
24PIN
INDEX
48PIN
13PIN
1PIN
12PIN
e
b
E
HE

QFN7-48



CHIP



Note: *** are any three characters

is NC pad

is a DieNo.

Chip thickness 400um

Opening of Pad

No.1～24 , 49～72 90um x 86um

No.25～48 , 73～96 86um×90um

Dec/28/2009

errata_c17001_6

PAD Coordinates

PAD No.	X(mm)	Y(mm)	Assignment	PAD No.	X(mm)	Y(mm)	Assignment
1	-1.15	-1.434	#TEST2	49	1.15	1.434	#TEST5
2	-1.05	-1.434	NC	50	1.05	1.434	NC
3	-0.95	-1.434	NC	51	0.95	1.434	NC
4	-0.85	-1.434	P05/REMO	52	0.85	1.434	OSC3
5	-0.75	-1.434	NC	53	0.75	1.434	NC
6	-0.65	-1.434	P04/REMI	54	0.65	1.434	NC
7	-0.55	-1.434	NC	55	0.55	1.434	OSC4
8	-0.45	-1.434	VSS	56	0.45	1.434	NC
9	-0.35	-1.434	NC	57	0.35	1.434	NC
10	-0.25	-1.434	P03	58	0.25	1.434	VSS
11	-0.15	-1.434	NC	59	0.15	1.434	P25/SCLK
12	-0.05	-1.434	P02	60	0.05	1.434	NC
13	0.05	-1.434	NC	61	-0.05	1.434	P24/SOUT
14	0.15	-1.434	P01	62	-0.15	1.434	P23/SIN
15	0.25	-1.434	P00	63	-0.25	1.434	NC
16	0.35	-1.434	NC	64	-0.35	1.434	HVDD
17	0.45	-1.434	HVDD	65	-0.45	1.434	NC
18	0.55	-1.434	NC	66	-0.55	1.434	P22/SPICLK
19	0.65	-1.434	P12	67	-0.65	1.434	NC
20	0.75	-1.434	NC	68	-0.75	1.434	P21/SDO
21	0.85	-1.434	P11	69	-0.85	1.434	NC
22	0.95	-1.434	NC	70	-0.95	1.434	P20/SDI
23	1.05	-1.434	P10	71	-1.05	1.434	P17/#SPISS
24	1.15	-1.434	NC	72	-1.15	1.434	NC
25	1.434	-1.15	#TEST3	73	-1.434	1.15	#TEST1
26	1.434	-1.05	NC	74	-1.434	1.05	NC
27	1.434	-0.95	#RESET	75	-1.434	0.95	NC
28	1.434	-0.85	NC	76	-1.434	0.85	TEST0
29	1.434	-0.75	VSS	77	-1.434	0.75	NC
30	1.434	-0.65	NC	78	-1.434	0.65	DCLK/P31
31	1.434	-0.55	P27/EXCL3	79	-1.434	0.55	DST2/P32
32	1.434	-0.45	NC	80	-1.434	0.45	NC
33	1.434	-0.35	P26/TOUT	81	-1.434	0.35	DSI0/P33
34	1.434	-0.25	NC	82	-1.434	0.25	NC
35	1.434	-0.15	P13/FOUT1	83	-1.434	0.15	VSS
36	1.434	-0.05	NC	84	-1.434	0.05	NC
37	1.434	0.05	P30/FOUT3	85	-1.434	-0.05	LVDD
38	1.434	0.15	LVDD	86	-1.434	-0.15	NC
39	1.434	0.25	VSS	87	-1.434	-0.25	P14/SDA
40	1.434	0.35	NC	88	-1.434	-0.35	NC
41	1.434	0.45	OSC1	89	-1.434	-0.45	P15/SCL
42	1.434	0.55	NC	90	-1.434	-0.55	NC
43	1.434	0.65	NC	91	-1.434	-0.65	P16/EXCL0
44	1.434	0.75	OSC2	92	-1.434	-0.75	NC
45	1.434	0.85	NC	93	-1.434	-0.85	P07/EXCL1
46	1.434	0.95	NC	94	-1.434	-0.95	NC
47	1.434	1.05	#TEST4	95	-1.434	-1.05	P06/EXCL2
48	1.434	1.15	NC	96	-1.434	-1.15	NC

PAD/Pin/Ball No.				Name	I/O	Default status	Function
CHIP	QFN7 -48PIN	QFP12 -48PIN	WCSP				
1	37	37	A1	**#TEST2**	I	I（Pull-Up）	Test pin (fixed at High during normal operations)
4	38	38	A2	**P05**/REMO	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ Remote output pin
6	39	39	B3	**P04**/REMI	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ Remote input pin
8	40	40	A3	**VSS**	-	-	Power supply pin (GND)
10	41	41	B4	**P03**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
12	42	42	A4	**P02**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
14	43	43	C4	**P01**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
15	44	44	D4	**P00**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
17	45	45	A5	**HVDD**	-	-	Power supply pin (HVDD+)
19	46	46	B5	**P12**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
21	47	47	A6	**P11**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
23	48	48	C5	**P10**	I/O	I(Pull-Up）	Input/output port pin (with interrupt)
25	1	1	A7	**#TEST3**	I	I（Pull-Up）	Test pin (fixed at High during normal operations)
27	2	2	B6	**#RESET**	I	I（Pull-Up）	Initial set input pin
29	3	3	B7	**VSS**	-	-	Power supply pin (GND)
31	4	4	C6	**P27**/EXCL3	I/O	I(Pull-Up）	Input/output port pin*/ T16E external clock input pin
33	5	5	C7	**P26**/TOUT	I/O	I(Pull-Up）	Input/output port pin*/ T16E PWM signal output pin
35	6	6	D5	**P13**/FOUT1	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ OSC1 clock output pin
37	7	7	D7	**P30**/FOUT3	I/O	I(Pull-Up）	Input/output port pin*/ OSC3 division clock output pin

38	8	8	D6	**LVDD**	-	-	Power supply pin (LVDD+)
39	9	9	E6	**VSS**	-	-	Power supply pin (GND)
41	10	10	E7	**OSC1**	I	I	OSC1 oscillator input pin (permits external clock input)
44	11	11	F7	**OSC2**	O	O	OSC1 oscillator output pin
47	12	12	F6	**#TEST4**	I	I（Pull-Up）	Test pin (fixed at High during normal operations)
49	13	13	G7	**#TEST5**	I	I（Pull-Up）	Test pin (fixed at High during normal operations)
52	14	14	G6	**OSC3**	I	I	OSC3 oscillator input pin (permits external clock input)
55	15	15	G5	**OSC4**	O	O	OSC3 oscillator output pin
58	16	16	F5	**VSS**	-	-	Power supply pin (GND)
59	17	17	E5	**P25**/SCLK	I/O	I(Pull-Up）	Input/output port pin*/ UART clock input pin
61	18	18	G4	**P24**/SOUT	I/O	I(Pull-Up）	Input/output port pin*/ UART data output pin
62	19	19	F4	**P23**/SIN	I/O	I(Pull-Up）	Input/output port pin*/ UART data input pin
64	20	20	G3	**HVDD**	-	-	Power supply pin (HVDD+)
66	21	21	E4	**P22**/SPICLK	I/O	I(Pull-Up）	Input/output port pin*/ SPI clock input/output pin
68	22	22	G2	**P21**/SDO	I/O	I(Pull-Up）	Input/output port pin*/ SPI data output pin
70	23	23	F3	**P20**/SDI	I/O	I(Pull-Up）	Input/output port pin*/ SPI data input pin
71	24	24	F2	**P17**/#SPISS	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ SPI slave select input pin
73	25	25	G1	**#TEST1**	I	I（Pull-Up）	Test pin (fixed at High during normal operations)
76	26	26	F1	**TEST0**	I	I（Pull-Down）	Test pin (fixed at Low during normal operations)
78	27	27	E3	**DCLK**/P31	I/O	O（H）	On-chip debugger clock output pin* / input/output port pin
79	28	28	E2	**DST2**/P32	I/O	O（L）	On-chip debugger status output pin* / input/output port pin
81	29	29	E1	**DSIO**/P33	I/O	I(Pull-Up）	On-chip debugger data input/output pin*/ input/output port pin

83	30	30	D2	**VSS**	-	-	Power supply pin (GND)
85	31	31	D1	**LVDD**	-	-	Power supply pin (LVDD+)
87	32	32	D3	**P14**/SDA	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ I2C data input/output pin
89	33	33	C1	**P15**/SCL	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ I2C clock output pin
91	34	34	C2	**P16**/EXCL0	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ T16 Ch.0 external clock input pin
93	35	35	B1	**P07**/EXCL1	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ T16 Ch.1 external clock input pin
95	36	36	B2	**P06**/EXCL2	I/O	I(Pull-Up）	Input/output port pin (with interrupt)*/ T16 Ch.2 external clock input pin

Note: Pins appearing in bold and functions indicated by “*” are default settings.

Dec/28/2009

errata_c17001_5

S1C17 Manual errata

ITEM: Mistakes of a method to clear receive data buffer.			
Object manuals	Document codes	Items	Pages
S17C17001 Technical Manual	411412300	18 UART	217, 229, 231

P217 (S1C17001)

(Error)

Setting the RXEN bit to 0 empties the transmission and receive data buffers, clearing any remaining data. The data being transferred cannot be guaranteed if RXEN is set to 0 while data is being sent or received.

(Correct)

Setting the RXEN bit to 0 empties the transmission ~~and receive~~ data buffers, clearing any remaining data. The data being transferred cannot be guaranteed if RXEN is set to 0 while data is being sent or received.

P229 (S1C17001)

(Error) **D0 RXEN: UART Enable Bit**

Permits data transfer by the UART.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Set RXEN to 1 before starting UART transfers. Setting RXEN to 0 will stop data transfers. Set the transfer conditions while RXEN is 0.

Preventing transfers by writing 0 to RXEN also clears transfer data buffers.

(Correct) **D0 RXEN: UART Enable Bit**

Permits data transfer by the UART.

1 (R/W): Permitted

0 (R/W): Prohibited (default)

Set RXEN to 1 before starting UART transfers. Setting RXEN to 0 will stop data transfers. Set the transfer conditions while RXEN is 0.

Preventing transfers by writing 0 to RXEN also clears ~~transfer~~ transmit data buffer~~s~~.

P231 (S1C17001)

(Error)

Preventing transfer by setting RXEN to 0 clears (initializes) transfer data buffers. Before writing 0 to RXEN, confirm the absence of data in the buffers awaiting transmission or reading.

(Correct)

Preventing transfer by setting RXEN to 0 clears (initializes) transfer data buffers. Before writing 0 to RXEN, confirm the absence of data in the buffers awaiting transmission ~~or reading~~.

Dec/28/2009

errata_c17001_4

S1C17 Manual errata

ITEM: Mistakes of a method to reset of receive err flags.			
Object manuals	Document codes	Items	Pages
S17C17001 Technical Manual	411412300	18 UART	224

P224(S1C17001)

(Error) **D6 FER: Framing Error Flag Bit**

Indicates whether a framing error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

FER is set to 1 when a framing error occurs. Framing errors occur when data is received with the stop bit set to 0. FER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

D5 PER: Parity Error Flag Bit

Indicates whether a parity error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

PER is set to 1 when a parity error occurs. Parity checking is enabled only when PREN/ UART_MOD*x* register is set to 1 and is performed when received data is transferred from the shift register to the receive data buffer. PER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

D4 OER: Overrun Error Flag Bit

Indicates whether an overrun error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

OER is set to 1 when an overrun error occurs. Overrun errors occur when data is received in the shift register when the receive data buffer is already full and additional data is sent. The receive data buffer is not overwritten even if this error occurs. The shift register is overwritten as soon as the error occurs.

OER is reset by writing 1 or by setting RXEN/UART_CTL*x* register to 0.

(Correct) **D6 FER: Framing Error Flag Bit**

Indicates whether a framing error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

FER is set to 1 when a framing error occurs. Framing errors occur when data is received with the stop bit set to 0. FER is reset by writing 1 ~~or by setting RXEN/UART_CTL*x* register to 0~~.

D5 PER: Parity Error Flag Bit

Indicates whether a parity error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

PER is set to 1 when a parity error occurs. Parity checking is enabled only when PREN/ UART_MOD*x* register is set to 1 and is performed when received data is transferred from the shift register to the receive data buffer. PER is reset by writing 1 ~~or by setting RXEN/UART_CTL*x* register to 0~~.

D4 OER: Overrun Error Flag Bit

Indicates whether an overrun error has occurred or not.

1 (R): Error occurred

0 (R): No error (default)

1 (W): Reset to 0

0 (W): Ignored

OER is set to 1 when an overrun error occurs. Overrun errors occur when data is received in the shift register when the receive data buffer is already full and additional data is sent. The receive data buffer is not overwritten even if this error occurs. The shift register is overwritten as soon as the error occurs.

OER is reset by writing 1 ~~or by setting RXEN/UART_CTL*x* register to 0~~.

Jun/10/2009

errata_c17001_3

S1C17 Series Manual errata

ITEM: Error in list of instructions

Object manuals	Document code	Object number
S1C17701 Technical Manual	411089902	2-5
S1C17704 Technical Manual	411511901	2-5
S1C17702 Technical Manual	411581700	2-5
S1C17602 Technical Manual	411620100	2-5
S1C17001 Technical Manual	411412300	2-5
S1C17003 Technical Manual	411635100	2-5
S1C17002 Technical Manual	411554401	I-5-5
S1C17501 Technical Manual	411525601	I-5-5
S1C17801 Technical Manual	411390801	I-5-5

2-5 (S1C17701, S1C17704, S1C17702, S1C17602, S1C17001, S1C17003) /

I-5-5 (S1C17501, S1C17801, S1C17002)

(Error)

Branch	jpa	imm7	Absolute jump
	ipa.d	%rb	Delayed branching possible

(Correct)

Branch	jpa	imm7	Absolute jump
	jpa.d	%rb	Delayed branching possible

S1C17 Series Manual errata

ITEM: SPICLK frequency limitation in SPI slave mode		
Object manuals	Document code	Object number
S1C17001 Technical Manual	411412300	235
S1C17701 Technical Manual	411089902	19-3
S1C17602 Technical Manual	411620100	19-3
S1C17702 Technical Manual	411581700	19-3
S1C17002 Technical Manual	411554401	V-4-3, V-5-3
S1C17501 Technical Manual	411525601	VI-3-3, VI-4-3
S1C17801 Technical Manual	411390801	VI-3-3, VI-4-3

1-2

(Error)

Note: The frequency of the clock input via the SPICLK pin must be less than 1/3 of the PCLK and have a clock duty ratio of 50%.

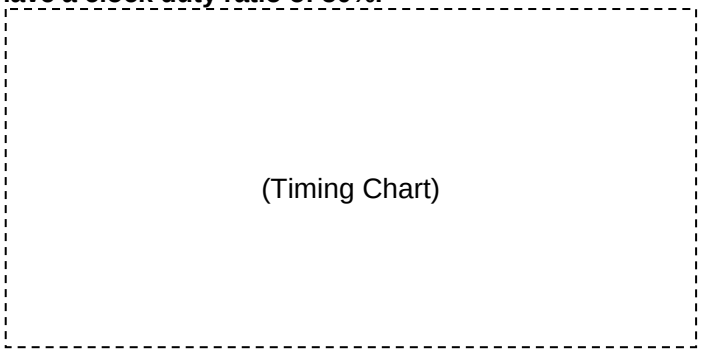
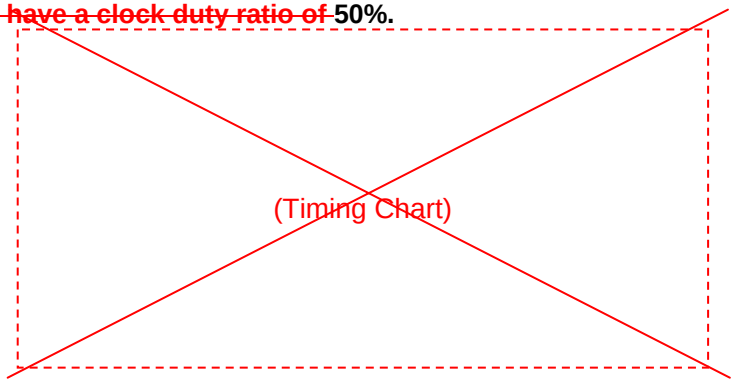


Figure 19.3.2 Slave mode SPI clock

(Correct)

Note: The duty ratio of the clock input via the SPICLK pin must be ~~less than 1/3 of the PCLK and have a clock duty ratio of~~ 50%.



~~Figure 19.3.2 Slave mode SPI clock~~

2008/7/22

errata_c17001_1

S1C17001 Manual errata

ITEM: External Clock Input AC Characteristics		
Object manuals	Document code	Object number
S1C17001 technical manual	411412300	301

(Error)

EXCLx input High pulse width Min=1/fSYS

EXCLx input Low pulse width Min=1/fSYS

(Correct)

EXCLx input High pulse width Min=2/fSYS

EXCLx input Low pulse width Min=2/fSYS