S1L60000 series

Core	I/O
1.8V	1.8V
	3.3V
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V

Series		S1L60000 Series									
Features		● 0.25μm CMOS, using 3-, 4-layer interconnect process ● 107 ps internal gate delay at 2.5V, 2-input NAND Typ. ● Low power consumption (Internal cell: 2.5V 0.18μW/MHz/BC) ● Drive capacity (I_{OL}=0.1, 1, 3, 6, 12, 24mA at 3.3V, I_{OL}=0.1, 1, 3, 6, 9, 18mA at 2.5V, I_{OL}=0.05, 0.3, 1, 2, 3, 6mA at 2.0V, I_{OL}=0.045, 0.27, 0.9, 1.8, 2.7, 5.4mA at 1.8V) ● RAM (synchronous type, asynchronous type), PLL, and various types of macro cells can be implemented.									
Model Name	3-layer Metallization	S1L60093	S1L60173	S1L60283	S1L60403	S1L60593	S1L60833	S1L61233	S1L61583	S1L61903	S1L62513
	4-layer Metallization	S1L60094	S1L60174	S1L60284	S1L60404	S1L60594	S1L60834	S1L61234	S1L61584	S1L61904	S1L62514
Total BC (Raw Gates)		99.2K	171.8K	284.4K	400.3K	595.4K	831.6K	1,234.9K	1,587.8K	1,903.0K	2,519.6K
Usable Gates	3-layer Metallization	59.6K	103.1K	142.2K	200.2K	297.7K	332.7K	494.0K	635.1K	761.2K	1,007.9K
	4-layer Metallization	69.5K	120.2K	184.9K	260.2K	387.0K	415.8K	617.5K	793.9K	951.5K	1,259.8K
Total Lead Count Micro Lead Pitch	80μm	—	—	—	—	—	284	344	388	424	488
	70μm	112	148	188	224	272	—	—	—	—	—
Delay Time	Internal Gates	tpd=107ps (2.5V operation, F/O=1, typical wiring load)									
	Input Buffer	tpd=270ps (2.5V operation, F/O=2, typical wiring load)									
	Output Buffer	tpd=1600ps (2.5V operation, C_L=15pF)									
I/O Levels		CMOS, LVTTL, PCI-3.3V									
Input Modes		LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail safe, Gated									
Output Modes		Normal, Open-drain, 3-state, Bidirectional, Fail safe, Gated									

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.