Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V
3.3V	3.3V
	5.0V

S1L50000 series

Series		S1L50000 Series													
Features		● 0.35μm CMOS, using 2-, 3- or 4-layer interconnect process ● 0.14 ns internal gate delay at 3.3V, 2-input power NAND Typ. ● Low power consumption (Internal cell: 3.3V 0.7μW/MHz/BC) ● Drive capacity (I_{OL}=0.1, 1, 3, 8, 12, 24mA at 5.0V, I_{OL}=0.1, 1, 2, 6, 12mA at 3.3V, I_{OL}=0.1, 0.5, 1, 3, 6mA at 2.5V, I_{OL}=0.05, 0.3, 0.6, 2, 4mA at 2.0V) ● RAM (asynchronous type), PLL, and various types of macro cells can be implemented.													
Model Name	2-layer Metallization	S1L50062	S1L50122	S1L50282	S1L50552	S1L50752	S1L50992	S1L51252	S1L51772	S1L52502	S1L53352	S1L54422	S1L55062	S1L56682	S1L58152
	3-layer Metallization	S1L50063	S1L50123	S1L50283	S1L50553	S1L50753	S1L50993	S1L51253	S1L51773	S1L52503	S1L53353	S1L54423	S1L55063	S1L56683	S1L58153
	4-layer Metallization	S1L50064	S1L50124	S1L50284	S1L50554	S1L50754	S1L50994	S1L51254	S1L51774	S1L52504	S1L53354	S1L54424	S1L55064	S1L56684	S1L58154
Total BC (Raw Gates)		5.8K	12.0K	28.8K	55.5K	75.8K	99.2K	125.8K	177.1K	250.2K	335.9K	442.2K	506.7K	668.6K	815.5K
Usable Gates	2-layer Metallization	2.9K	6.0K	14.4K	26.1K	35.7K	46.7K	56.6K	79.7K	112.6K	144.5K	176.9K	202.7K	267.5K	326.2K
	3-layer Metallization	5.1K	10.6K	25.3K	47.2K	64.4K	84.4K	100.7K	132.8K	187.7K	251.9K	309.5K	354.7K	468.0K	570.9K
	4-layer Metallization	5.5K	11.4K	27.3K	52.8K	72.0K	94.3K	119.5K	168.2K	237.7K	319.1K	397.9K	456.1K	601.7K	734.0K
Total Lead Count Micro Lead Pitch	80μm	—	56	88	124	144	168	188	224	264	308	352	376	432	480
	70μm	48	64	104	144	168	192	216	—	—	—	—	—	—	—
Delay Time	Internal Gates	t_{pd}=0.14ns (3.3V operation, F/O=2, typical wiring load), 0.21ns (2.0V operation, F/O=2, typical wiring load)													
	Input Buffer	t_{pd}=0.38ns (5.0V operation, F/O=2, typical wiring load), 0.4ns (3.3V operation, F/O=2, typical wiring load), 1.3ns (2.0V operation, F/O=2, typical wiring load)													
	Output Buffer	t_{pd}=2.12ns (5.0V operation, C_L=15pF), 2.02ns (3.3V operation, C_L=15pF), 3.9ns (2.0V operation, C_L=15pF)													
I/O Levels		CMOS, LVTTL, PCI-5V, PCI-3.3V													
Input Modes		LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail safe, Gated													
Output Modes		Normal, Open-drain, 3-state, Bidirectional, Fail safe, Gated													