EPSON
EXCEED YOUR VISION

CMOS 16-BIT SINGLE CHIP MICROCONTROLLER

S1C17589
Technical Manual

SEIKO EPSON CORPORATION

Rev. 1.1

Evaluation board/kit and Development tool important notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson dose not assume any responsibility or liability of any kind of damage and/or fire coursed by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. When exporting the products or technology described in this material, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You are requested not to use, to resell, to export and/or to otherwise dispose of the products (and any technical information furnished, if any) for the development and/or manufacture of weapon of mass destruction or for other military purposes.

All brands or product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

Preface

This is a technical manual for designers and programmers who develop a product using the S1C17589. This document describes the functions of the IC, embedded peripheral circuit operations, and their control methods.

For the CPU functions and instructions, refer to the "S1C17 Family S1C17 Core Manual." For the functions and operations of the debugging tools, refer to the respective tool manuals. (Our "Products: Document Downloads" website provides the downloadable manuals.)

Notational conventions and symbols in this manual

Register address

Peripheral circuit chapters do not provide control register addresses. Refer to "Peripheral Circuit Area" in the "Memory and Bus" chapter or "List of Peripheral Circuit Control Registers" in the Appendix.

Register and control bit names

In this manual, the register and control bit names are described as shown below to distinguish from signal and pin names.

XXX register: Represents a register including its all bits.
XXX.YYY bit: Represents the one control bit YYY in the XXX register.
XXX.ZZZ[1:0] bits: Represents the two control bits ZZZ1 and ZZZ0 in the XXX register.

Register table contents and symbols

Initial: Value set at initialization

Reset: Initialization condition. The initialization condition depends on the reset group (H0, H1, or S0). For more information on the reset groups, refer to "Initialization Conditions (Reset Groups)" in the "Power Supply, Reset, and Clocks" chapter.

R/W: R = Read only bit
W = Write only bit
WP = Write only bit with a write protection using the MSCPROT.PROT[15:0] bits
R/W = Read/write bit
R/WP = Read/write bit with a write protection using the MSCPROT.PROT[15:0] bits

Control bit read/write values

This manual describes control bit values in a hexadecimal notation except for one-bit values (and except when decimal or binary notation is required in terms of explanation). The values are described as shown below according to the control bit width.

1 bit: 0 or 1
2 to 4 bits: 0x0 to 0xf
5 to 8 bits: 0x00 to 0xff
9 to 12 bits: 0x000 to 0xfff
13 to 16 bits: 0x0000 to 0xffff

Decimal: 0 to 9999...
Binary: 0b0000... to 0b1111...

Channel number

Multiple channels may be implemented in some peripheral circuits (e.g., 16-bit timer, etc.). The peripheral circuit chapters use '*n*' as the value that represents the channel number in the register and pin names regardless of the number of channel actually implemented. Normally, the descriptions are applied to all channels. If there is a channel that has different functions from others, the channel number is specified clearly.

Example) T16_*n*CTL register of the 16-bit timer
If one channel is implemented (Ch.0 only): T16_*n*CTL = T16_0CTL only
If two channels are implemented (Ch.0 and Ch.1): T16_*n*CTL = T16_0CTL and T16_1CTL

For the number of channels implemented in the peripheral circuits of this IC, refer to "Features" in the "Overview" chapter.

– Contents –

1 Overview

The S1C17589 is a 16-bit embedded Flash MCU that features wide operating voltage range from 1.8 V to 5.5 V. It includes a lot of general-purpose I/O ports and A/D converter input ports and is suitable for various kinds of sensing applications from battery-driven equipment to home electrical products.

1.1 Features

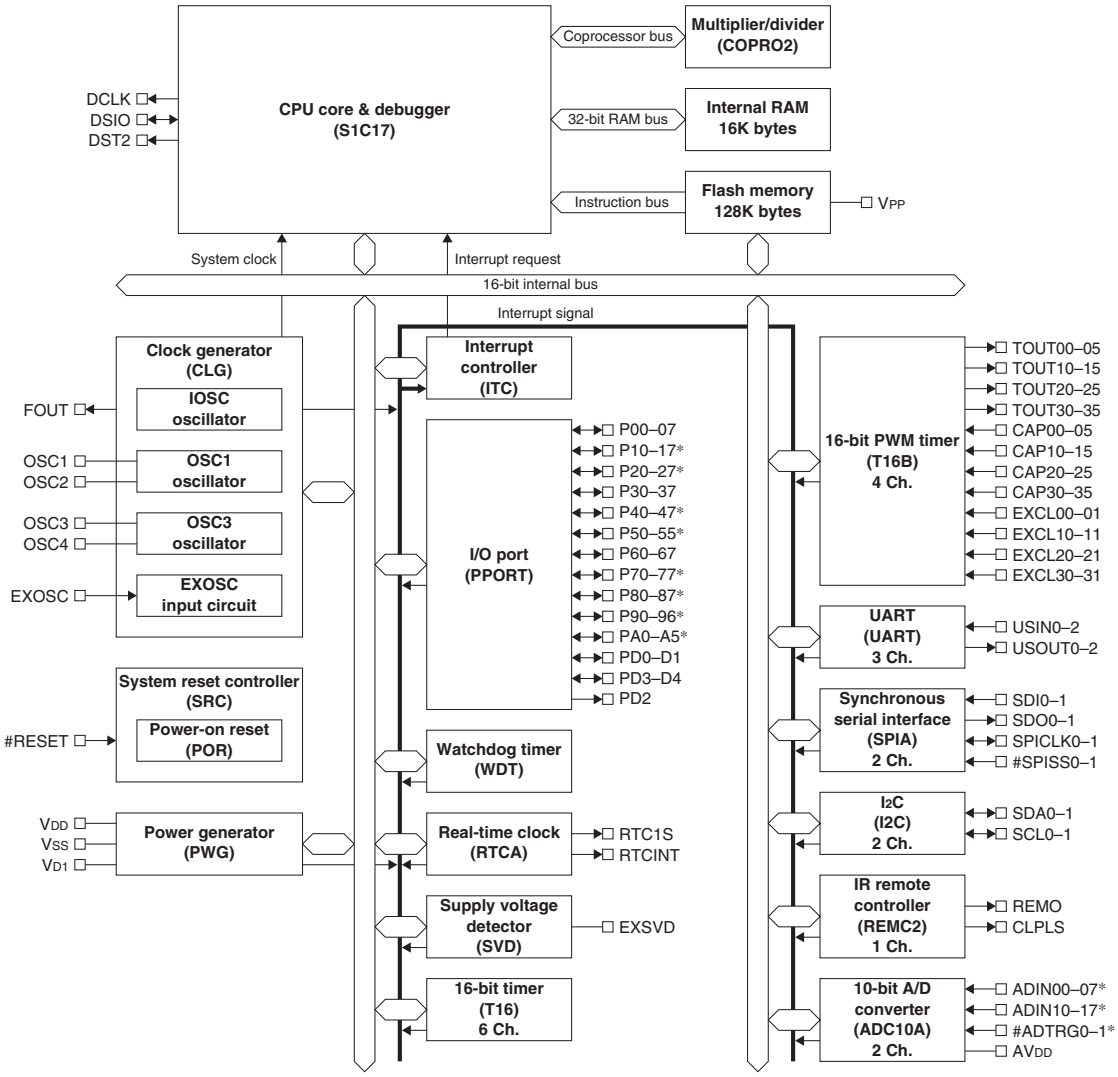
Table 1.1.1 Features

Model	S1C17589
CPU	
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17
Other	On-chip debugger
Embedded Flash memory	
Capacity	128K bytes (for both instructions and data)
Erase/program count	50 times (min.) * Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini
	On-board programming function using ICDmini
Embedded RAM	
Capacity	16K bytes
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	16.8 MHz (max.)
IOSC oscillator circuit	16/12/8 (boot clock source)/4 MHz (typ.) selectable via software
	10 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator
	Oscillation stop detection circuit included
OSC3 oscillator circuit	16.8 MHz (max.) crystal/ceramic oscillator
EXOSC clock input	16.8 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	Input/output port: 87 bits (max.) (Chip, QFP15-100PIN) 67 bits (max.) (QFP14-80PIN) 51 bits (max.) (QFP13-64PIN)
	Output port: 1 bit (max.)
	Pins are shared with the peripheral I/O.
Number of input interrupt ports	83 bits (max.) (Chip, QFP15-100PIN) 63 bits (max.) (QFP14-80PIN) 47 bits (max.) (QFP13-64PIN)
Number of ports that support universal port multiplexer (UPMUX)	32 bits (Chip, QFP15-100PIN, QFP14-80PIN) 31 bits (QFP13-64PIN)
	A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	
Watchdog timer (WDT)	Generates NMI or watchdog timer reset.
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	6 channels
	Generates the SPIA master clocks and the ADC10A trigger signals.
16-bit PWM timer (T16B)	4 channels
	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 6 ports/channel
Supply voltage detector (SVD)	
Detection level	20 levels (1.8 to 3.7 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.

Serial interfaces	
UART (UART)	3 channels
	Baud-rate generator included, IrDA1.0 supported
Synchronous serial interface (SPIA)	2 channels
	2 to 16-bit variable data length
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I^2C (I2C)	2 channels
	Baud-rate generator included
IR remote controller (REMC2)	
Number of transmitter channels	1 channel
Other	EL lamp drive waveform can be generated (by the hardware) for an application example.
10-bit A/D converter (ADC10A)	
Conversion method	Successive approximation type
Resolution	10 bits
Number of conversion channels	2 channels (Chip, QFP15-100PIN, QFP14-80PIN) 1 channel (QFP13-64PIN)
Number of analog signal inputs	Ch.0: 8 ports, Ch.1: 8 ports (Chip, QFP15-100PIN) Ch.0: 8 ports, Ch.1: 3 ports (QFP14-80PIN) Ch.0: 7 ports, Ch.1: none (QFP13-64PIN)
Multiplier/divider (COPRO2)	
Arithmetic functions	16-bit × 16-bit multiplier
	16-bit × 16-bit + 32-bit multiply and accumulation unit
	32-bit ÷ 32-bit divider
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels)
	Internal interrupt: 23 systems (8 levels)
Power supply voltage	
V_{DD} operating voltage	1.8 to 5.5 V
V_{DD} operating voltage for Flash programming	1.8 to 5.5 V (V_{PP} = 7.5 V external power supply is required.)
AV_{DD} operating voltage	2.7 to 5.5 V
Operating temperature	
Operating temperature range	-40 to 85 °C
Current consumption (Typ. value)	
SLEEP mode	0.2 µA IOSC = OFF, OSC1 = OFF, OSC3 = OFF
HALT mode	0.6 µA OSC1 = 32 kHz, RTC = ON
RUN mode	9 µA OSC1 = 32 kHz, RTC = ON, CPU = OSC1
	280 µA OSC3 = 1 MHz (ceramic osillator), OSC1 = 32 kHz, RTC = ON, CPU = OSC3
Shipping form	
1 *1	QFP15-100PIN (P-LQFP100-1414-0.50, 14 × 14 mm, t = 1.7 mm, 0.5 mm pitch)
2 *1	QFP14-80PIN (P-LQFP080-1212-0.50, 12 × 12 mm, t = 1.7 mm, 0.5 mm pitch)
3 *1	QFP13-64PIN (P-LQFP064-1010-0.50, 10 × 10 mm, t = 1.7 mm, 0.5 mm pitch)
4	Die form (Pad pitch: 80 µm (min.))

*1 Shown in parentheses are JEITA package names.

1.2 Block Diagram



* The pin configuration depends on the package type.

Figure 1.2.1 S1C17589 Block Diagram

1.3 Pins

1.3.1 Pin Configuration Diagram (QFP Packages)

QFP15-100PIN

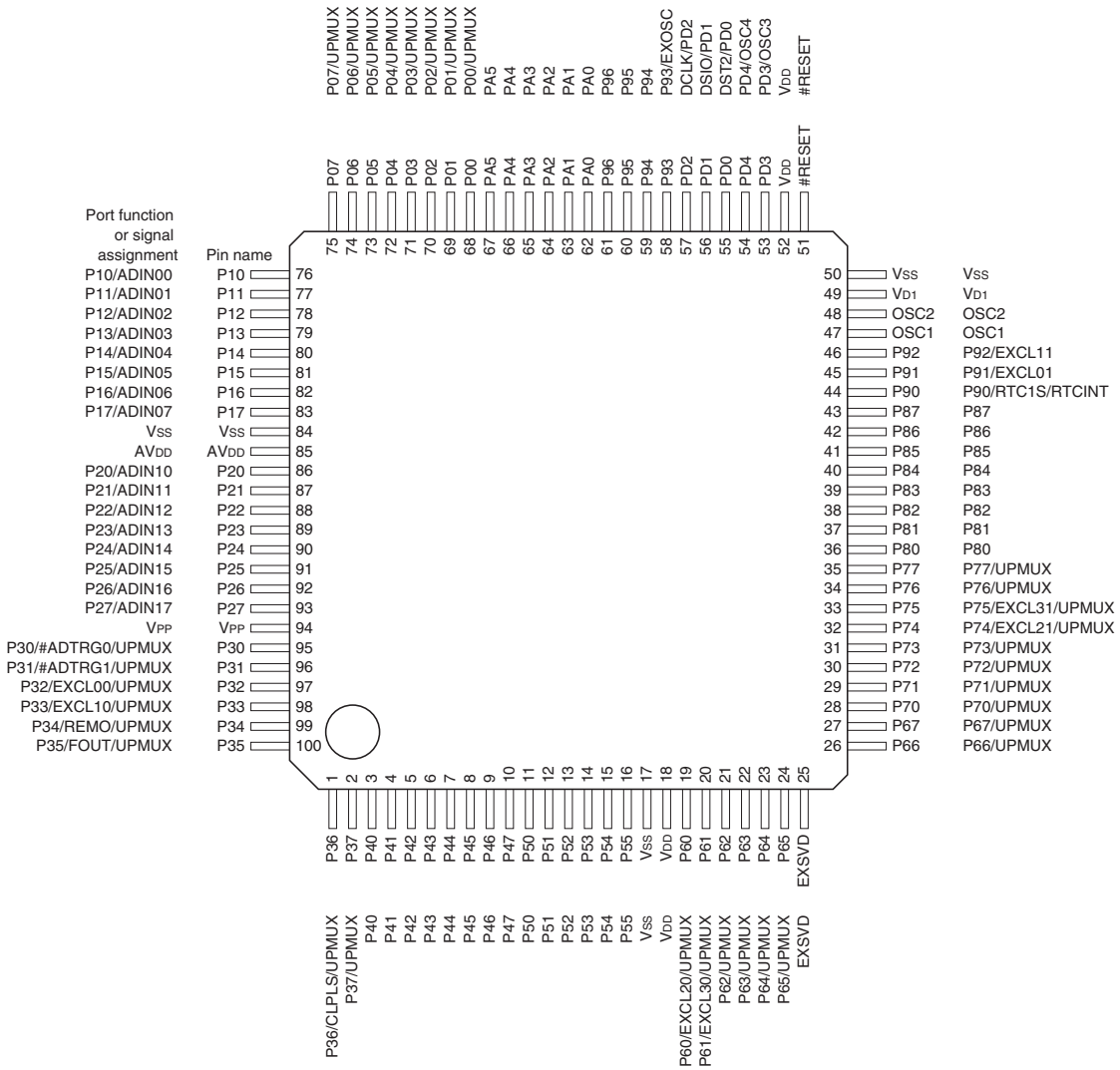


Figure 1.3.1.1 S1C17589 Pin Configuration Diagram (QFP15-100PIN)

QFP14-80PIN

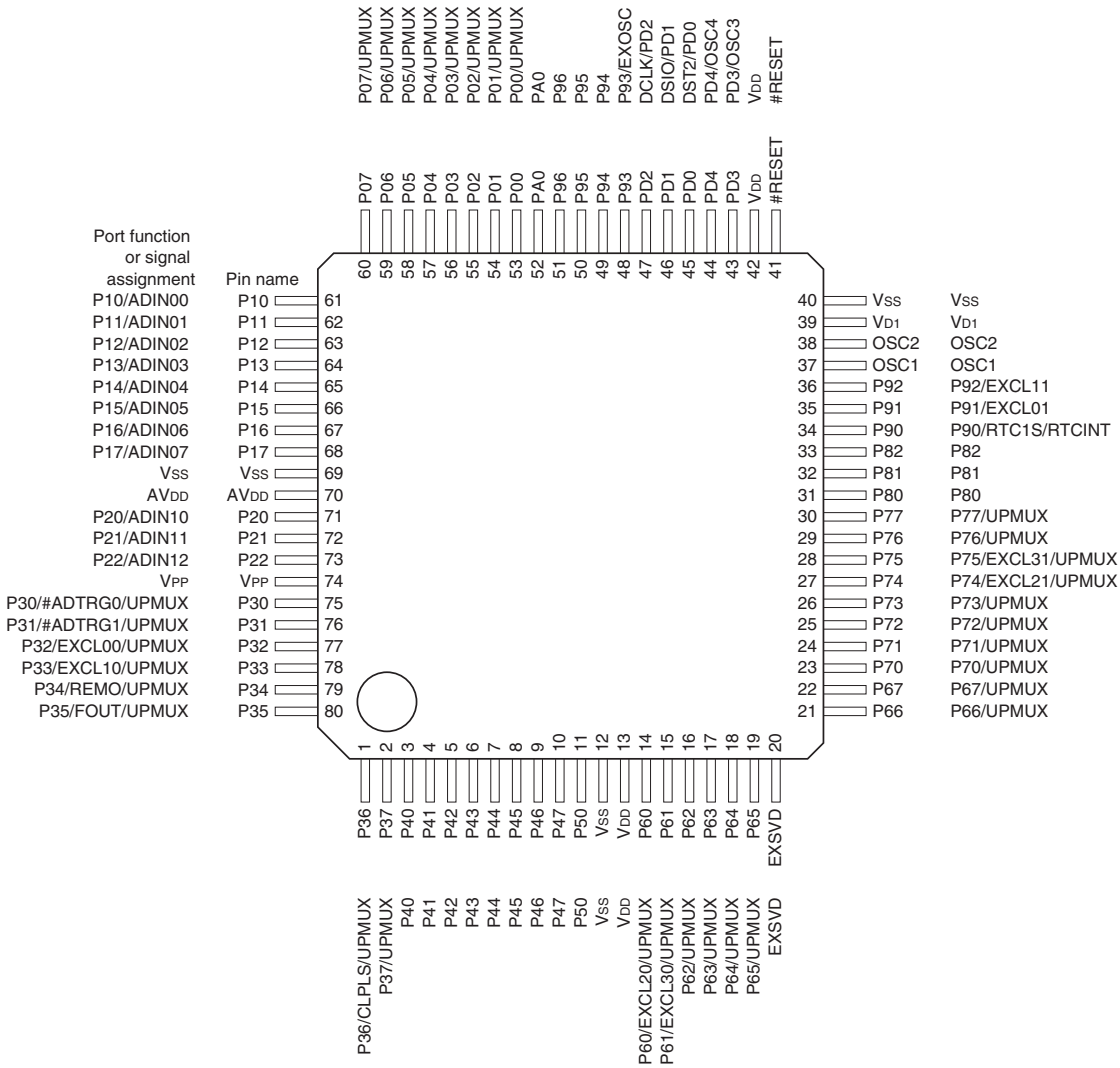


Figure 1.3.1.2 S1C17589 Pin Configuration Diagram (QFP14-80PIN)

QFP13-64PIN

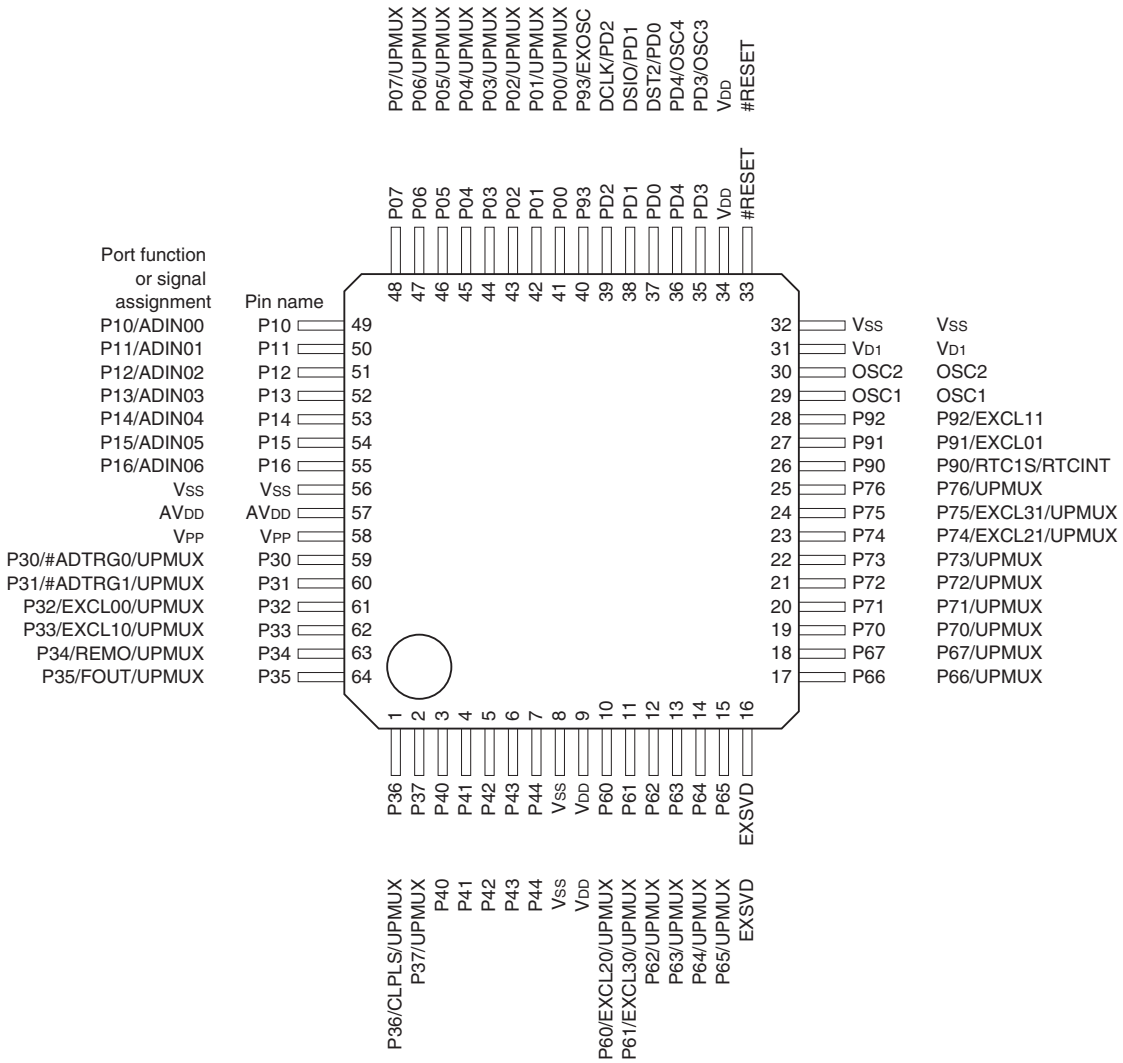


Figure 1.3.1.3 S1C17589 Pin Configuration Diagram (QFP13-64PIN)

1.3.2 Pad Configuration Diagram (Chip)

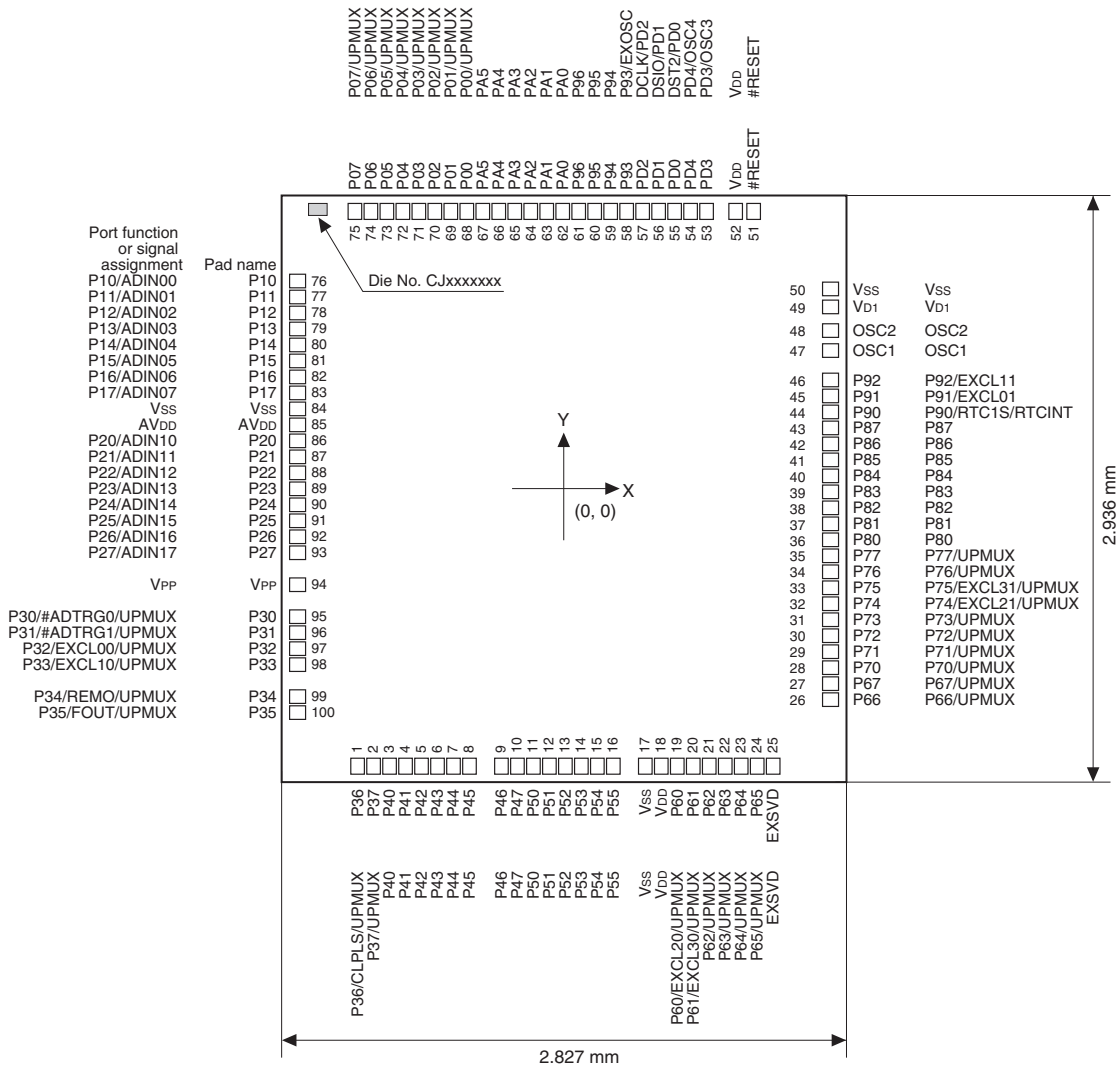


Figure 1.3.2.1 S1C17589 Pad Configuration Diagram (Chip)

Pad opening No. 1–25, 51–75: X = 68 µm, Y = 80 µm
No. 26–50, 76–100: X = 80 µm, Y = 68 µm
Chip thickness 400 µm

Table 1.3.2.1 Pad Coordinates

No.	X µm	Y µm	No.	X µm	Y µm	No.	X µm	Y µm	No.	X µm	Y µm
1	-1,033.4	-1,388.3	26	1,333.7	-1,055.2	51	948.8	1,388.3	76	-1,333.7	1,040.0
2	-953.4	-1,388.3	27	1,333.7	-975.2	52	858.8	1,388.3	77	-1,333.7	960.0
3	-873.4	-1,388.3	28	1,333.7	-895.2	53	713.2	1,388.3	78	-1,333.7	880.0
4	-793.4	-1,388.3	29	1,333.7	-815.2	54	633.2	1,388.3	79	-1,333.7	800.0
5	-713.4	-1,388.3	30	1,333.7	-735.2	55	553.2	1,388.3	80	-1,333.7	720.0
6	-633.4	-1,388.3	31	1,333.7	-655.2	56	473.2	1,388.3	81	-1,333.7	640.0
7	-553.4	-1,388.3	32	1,333.7	-575.2	57	393.2	1,388.3	82	-1,333.7	560.0
8	-473.4	-1,388.3	33	1,333.7	-495.2	58	313.2	1,388.3	83	-1,333.7	480.0
9	-313.4	-1,388.3	34	1,333.7	-415.2	59	233.2	1,388.3	84	-1,333.7	400.0
10	-233.4	-1,388.3	35	1,333.7	-335.2	60	153.2	1,388.3	85	-1,333.7	320.0
11	-153.4	-1,388.3	36	1,333.7	-255.2	61	73.2	1,388.3	86	-1,333.7	240.0
12	-73.4	-1,388.3	37	1,333.7	-175.2	62	-6.8	1,388.3	87	-1,333.7	160.0
13	6.6	-1,388.3	38	1,333.7	-95.2	63	-86.8	1,388.3	88	-1,333.7	80.0
14	86.6	-1,388.3	39	1,333.7	-15.2	64	-166.8	1,388.3	89	-1,333.7	0.0
15	166.6	-1,388.3	40	1,333.7	64.8	65	-246.8	1,388.3	90	-1,333.7	-80.0
16	246.6	-1,388.3	41	1,333.7	144.8	66	-326.8	1,388.3	91	-1,333.7	-160.0
17	406.6	-1,388.3	42	1,333.7	224.8	67	-406.8	1,388.3	92	-1,333.7	-240.0
18	486.6	-1,388.3	43	1,333.7	304.8	68	-486.8	1,388.3	93	-1,333.7	-320.0
19	566.6	-1,388.3	44	1,333.7	384.8	69	-566.8	1,388.3	94	-1,333.7	-480.0
20	646.6	-1,388.3	45	1,333.7	464.8	70	-646.8	1,388.3	95	-1,333.7	-640.0
21	726.6	-1,388.3	46	1,333.7	544.8	71	-726.8	1,388.3	96	-1,333.7	-720.0
22	806.6	-1,388.3	47	1,333.7	692.0	72	-806.8	1,388.3	97	-1,333.7	-800.0
23	886.6	-1,388.3	48	1,333.7	792.0	73	-886.8	1,388.3	98	-1,333.7	-880.0
24	966.6	-1,388.3	49	1,333.7	910.4	74	-966.8	1,388.3	99	-1,333.7	-1,040.0
25	1,046.6	-1,388.3	50	1,333.7	1,000.4	75	-1,046.8	1,388.3	100	-1,333.7	-1,120.0

1.3.3 Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Table 1.3.3.1 Pin description

Chip	QFP15-100PIN	QFP14-80PIN	QFP13-64PIN	Pin/pad name	Assigned signal	I/O	Initial state	Function
✓	✓	✓	✓	V_{DD}	V_{DD}	P	–	Power supply (+)
✓	✓	✓	✓	AV_{DD}	AV_{DD}	P	–	Analog power supply (+)
✓	✓	✓	✓	V_{SS}	V_{SS}	P	–	GND
✓	✓	✓	✓	V_{PP}	V_{PP}	P	–	Power supply for Flash programming
✓	✓	✓	✓	V_{D1}	V_{D1}	A	–	Internal voltage regulator output
✓	✓	✓	✓	EXSVD	EXSVD	A	–	Supply voltage detector input
✓	✓	✓	✓	OSC1	OSC1	A	-	OSC1 oscillator circuit input
✓	✓	✓	✓	OSC2	OSC2	A	-	OSC1 oscillator circuit output
✓	✓	✓	✓	#RESET	#RESET	I	I (Pull-up)	Reset input

Chip	QFP15-100PIN	QFP14-80PIN	QFP13-64PIN	Pin/pad name	Assigned signal	I/O	Initial state	Function
✓	✓	✓	✓	P00	P00	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P01	P01	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P02	P02	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P03	P03	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P04	P04	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P05	P05	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P06	P06	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P07	P07	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P10	P10	I/O	Hi-Z	I/O port
					ADIN00	A		10-bit A/D converter Ch.0 analog signal input 0
✓	✓	✓	✓	P11	P11	I/O	Hi-Z	I/O port
					ADIN01	A		10-bit A/D converter Ch.0 analog signal input 1
✓	✓	✓	✓	P12	P12	I/O	Hi-Z	I/O port
					ADIN02	A		10-bit A/D converter Ch.0 analog signal input 2
✓	✓	✓	✓	P13	P13	I/O	Hi-Z	I/O port
					ADIN03	A		10-bit A/D converter Ch.0 analog signal input 3
✓	✓	✓	✓	P14	P14	I/O	Hi-Z	I/O port
					ADIN04	A		10-bit A/D converter Ch.0 analog signal input 4
✓	✓	✓	✓	P15	P15	I/O	Hi-Z	I/O port
					ADIN05	A		10-bit A/D converter Ch.0 analog signal input 5
✓	✓	✓	✓	P16	P16	I/O	Hi-Z	I/O port
					ADIN06	A		10-bit A/D converter Ch.0 analog signal input 6
✓	✓	✓	–	P17	P17	I/O	Hi-Z	I/O port
					ADIN07	A		10-bit A/D converter Ch.0 analog signal input 7
✓	✓	✓	–	P20	P20	I/O	Hi-Z	I/O port
					ADIN10	A		10-bit A/D converter Ch.1 analog signal input 0
✓	✓	✓	–	P21	P21	I/O	Hi-Z	I/O port
					ADIN11	A		10-bit A/D converter Ch.1 analog signal input 1
✓	✓	✓	–	P22	P22	I/O	Hi-Z	I/O port
					ADIN12	A		10-bit A/D converter Ch.1 analog signal input 2
✓	✓	–	–	P23	P23	I/O	Hi-Z	I/O port
					ADIN13	A		10-bit A/D converter Ch.1 analog signal input 3
✓	✓	–	–	P24	P24	I/O	Hi-Z	I/O port
					ADIN14	A		10-bit A/D converter Ch.1 analog signal input 4
✓	✓	–	–	P25	P25	I/O	Hi-Z	I/O port
					ADIN15	A		10-bit A/D converter Ch.1 analog signal input 5
✓	✓	–	–	P26	P26	I/O	Hi-Z	I/O port
					ADIN16	A		10-bit A/D converter Ch.1 analog signal input 6
✓	✓	–	–	P27	P27	I/O	Hi-Z	I/O port
					ADIN17	A		10-bit A/D converter Ch.1 analog signal input 7
✓	✓	✓	✓	P30	P30	I/O	Hi-Z	I/O port
					#ADTRG0	I		10-bit A/D converter Ch.0 trigger input
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P31	P31	I/O	Hi-Z	I/O port
					#ADTRG1	I		10-bit A/D converter Ch.1 trigger input
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P32	P32	I/O	Hi-Z	I/O port
					EXCL00	I		16-bit PWM timer Ch.0 event counter input 0
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P33	P33	I/O	Hi-Z	I/O port
					EXCL10	I		16-bit PWM timer Ch.1 event counter input 0
					UPMUX	I/O		User-selected I/O (universal port multiplexer)

Chip	QFP15-100PIN	QFP14-80PIN	QFP13-64PIN	Pin/pad name	Assigned signal	I/O	Initial state	Function
✓	✓	✓	✓	P34	P34	I/O	Hi-Z	I/O port
					REMO	O		IR remote controller transmit data output
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P35	P35	I/O	Hi-Z	I/O port
					FOUT	O		Clock external output
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P36	P36	I/O	Hi-Z	I/O port
					CLPLS	O		IR remote controller clear pulse output
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P37	P37	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P40	P40	I/O	Hi-Z	I/O port
✓	✓	✓	✓	P41	P41	I/O	Hi-Z	I/O port
✓	✓	✓	✓	P42	P42	I/O	Hi-Z	I/O port
✓	✓	✓	✓	P43	P43	I/O	Hi-Z	I/O port
✓	✓	✓	✓	P44	P44	I/O	Hi-Z	I/O port
✓	✓	✓	–	P45	P45	I/O	Hi-Z	I/O port
✓	✓	✓	–	P46	P46	I/O	Hi-Z	I/O port
✓	✓	✓	–	P47	P47	I/O	Hi-Z	I/O port
✓	✓	✓	–	P50	P50	I/O	Hi-Z	I/O port
✓	✓	–	–	P51	P51	I/O	Hi-Z	I/O port
✓	✓	–	–	P52	P52	I/O	Hi-Z	I/O port
✓	✓	–	–	P53	P53	I/O	Hi-Z	I/O port
✓	✓	–	–	P54	P54	I/O	Hi-Z	I/O port
✓	✓	–	–	P55	P55	I/O	Hi-Z	I/O port
✓	✓	✓	✓	P60	P60	I/O	Hi-Z	I/O port
					EXCL20	I		16-bit PWM timer Ch.2 event counter input 0
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P61	P61	I/O	Hi-Z	I/O port
					EXCL30	I		16-bit PWM timer Ch.3 event counter input 0
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P62	P62	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P63	P63	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P64	P64	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P65	P65	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P66	P66	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P67	P67	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P70	P70	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P71	P71	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P72	P72	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P73	P73	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P74	P74	I/O	Hi-Z	I/O port
					EXCL21	I		16-bit PWM timer Ch.2 event counter input 1
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P75	P75	I/O	Hi-Z	I/O port
					EXCL31	I		16-bit PWM timer Ch.3 event counter input 1
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	✓	P76	P76	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)

Chip	QFP15-100PIN	QFP14-80PIN	QFP13-64PIN	Pin/pad name	Assigned signal	I/O	Initial state	Function
✓	✓	✓	–	P77	P77	I/O	Hi-Z	I/O port
					UPMUX	I/O		User-selected I/O (universal port multiplexer)
✓	✓	✓	–	P80	P80	I/O	Hi-Z	I/O port
✓	✓	✓	–	P81	P81	I/O	Hi-Z	I/O port
✓	✓	✓	–	P82	P82	I/O	Hi-Z	I/O port
✓	✓	–	–	P83	P83	I/O	Hi-Z	I/O port
✓	✓	–	–	P84	P84	I/O	Hi-Z	I/O port
✓	✓	–	–	P85	P85	I/O	Hi-Z	I/O port
✓	✓	–	–	P86	P86	I/O	Hi-Z	I/O port
✓	✓	–	–	P87	P87	I/O	Hi-Z	I/O port
✓	✓	✓	✓	P90	P90	I/O	Hi-Z	I/O port
					RTC1S	O		Real-time clock 1-second cycle pulse output
					RTCINT	O		Real-time clock interrupt signal output
✓	✓	✓	✓	P91	P91	I/O	Hi-Z	I/O port
					EXCL01	I		16-bit PWM timer Ch.0 event counter input 1
✓	✓	✓	✓	P92	P92	I/O	Hi-Z	I/O port
					EXCL11	I		16-bit PWM timer Ch.1 event counter input 1
✓	✓	✓	✓	P93	P93	I/O	Hi-Z	I/O port
					EXOSC	I		Clock generator external clock input
✓	✓	✓	–	P94	P94	I/O	Hi-Z	I/O port
✓	✓	✓	–	P95	P95	I/O	Hi-Z	I/O port
✓	✓	✓	–	P96	P96	I/O	Hi-Z	I/O port
✓	✓	✓	–	PA0	PA0	I/O	Hi-Z	I/O port
✓	✓	–	–	PA1	PA1	I/O	Hi-Z	I/O port
✓	✓	–	–	PA2	PA2	I/O	Hi-Z	I/O port
✓	✓	–	–	PA3	PA3	I/O	Hi-Z	I/O port
✓	✓	–	–	PA4	PA4	I/O	Hi-Z	I/O port
✓	✓	–	–	PA5	PA5	I/O	Hi-Z	I/O port
✓	✓	✓	✓	PD0	DST2	O	O (L)	On-chip debugger status output
					PD0	I/O		I/O port
✓	✓	✓	✓	PD1	DSIO	I/O	I (Pull-up)	On-chip debugger data input/output
					PD1	I/O		I/O port
✓	✓	✓	✓	PD2	DCLK	O	O (H)	On-chip debugger clock output
					PD2	O		Output port
✓	✓	✓	✓	PD3	PD3	I/O	Hi-Z	I/O port
					OSC3	A		OSC3 oscillator circuit input
✓	✓	✓	✓	PD4	PD4	I/O	Hi-Z	I/O port
					OSC4	A		OSC3 oscillator circuit output

Note: In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Table 1.3.3.2 Peripheral Circuit Input/output Function Selectable by UPMUX

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0, 1	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I2C (I2C)	SCL*n*	I/O	*n* = 0, 1	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART)	USIN*n*	I	*n* = 0, 1, 2	UART Ch.*n* data input
	USOUT*n*	O		UART Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0, 1, 2, 3	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1
	TOUT*n*2/CAP*n*2	I/O		T16B Ch.*n* PWM output/capture input 2
	TOUT*n*3/CAP*n*3	I/O		T16B Ch.*n* PWM output/capture input 3
	TOUT*n*4/CAP*n*4	I/O		T16B Ch.*n* PWM output/capture input 4
	TOUT*n*5/CAP*n*5	I/O		T16B Ch.*n* PWM output/capture input 5

Note: Do not assign a function to two or more pins simultaneously.

2 Power Supply, Reset, and Clocks

The power supply, reset, and clocks in this IC are managed by the embedded power generator, system reset controller, and clock generator, respectively.

2.1 Power Generator (PWG)

2.1.1 Overview

PWG is the power generator that controls the internal power supply system to drive this IC with stability and low power. The main features of PWG are outlined below.

- Embedded V_{D1} regulator
  - The V_{D1} regulator generates the V_{D1} voltage to drive internal circuits, this makes it possible to keep current consumption constant independent of the V_{DD} voltage level.
  - The V_{D1} regulator supports two operation modes, normal mode and economy mode, and setting the V_{D1} regulator into economy mode at light loads helps achieve low-power operations.

Figure 2.1.1.1 shows the PWG configuration.

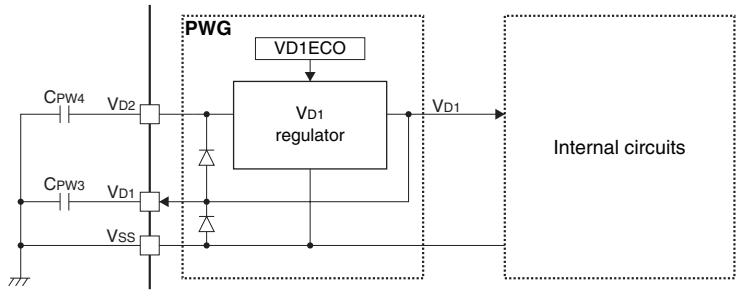


Figure 2.1.1.1 PWG Configuration

2.1.2 Pins

Table 2.1.2.1 lists the PWG pins.

Table 2.1.2.1 List of PWG Pins

Pin name	I/O	Initial status	Function
V_{DD}	P	–	Power supply (+)
V_{SS}	P	–	GND
V_{D1}	A	–	Embedded regulator output pin

For the V_{DD} operating voltage range and recommended external parts, refer to "Recommended Operating Conditions, Power supply voltage V_{DD}" in the "Electrical Characteristics" chapter and the "Basic External Connection Diagram" chapter, respectively.

2.1.3 V_{D1} Regulator Operation Mode

The V_{D1} regulator supports two operation modes, normal mode and economy mode. Setting the V_{D1} regulator into economy mode at light loads helps achieve low-power operations. Table 2.1.3.1 lists examples of light load conditions in which economy mode can be set.

Table 2.1.3.1 Examples of Light Load Conditions in which Economy Mode Can be Set

Light load condition	Exceptions
SLEEP mode (when all oscillators are stopped, or OSC1 only is active)	When a clock source except for OSC1 is active
HALT mode (when OSC1 only is active)	
RUN mode (when OSC1 only is active)	

The V_{D1} regulator also supports automatic mode in which the hardware detects a light load condition and automatically switches between normal mode and economy mode. Use the V_{D1} regulator in automatic mode when no special control is required.

2.2 System Reset Controller (SRC)

2.2.1 Overview

SRC is the system reset controller that resets the internal circuits according to the requests from the reset sources to archive steady IC operations. The main features of SRC are outlined below.

- Embedded reset hold circuit maintains reset state to boot the system safely while the internal power supply is unstable after power on or the oscillation frequency is unstable after the clock source is initiated.
- Supports reset requests from multiple reset sources.
  - #RESET pin
  - POR
  - Key-entry reset
  - Watchdog timer reset
  - Supply voltage detector reset
  - Peripheral circuit software reset (supports some peripheral circuits only)
- The CPU registers and peripheral circuit control bits will be reset with an appropriate initialization condition according to changes in status.

Figure 2.2.1.1 shows the SRC configuration.

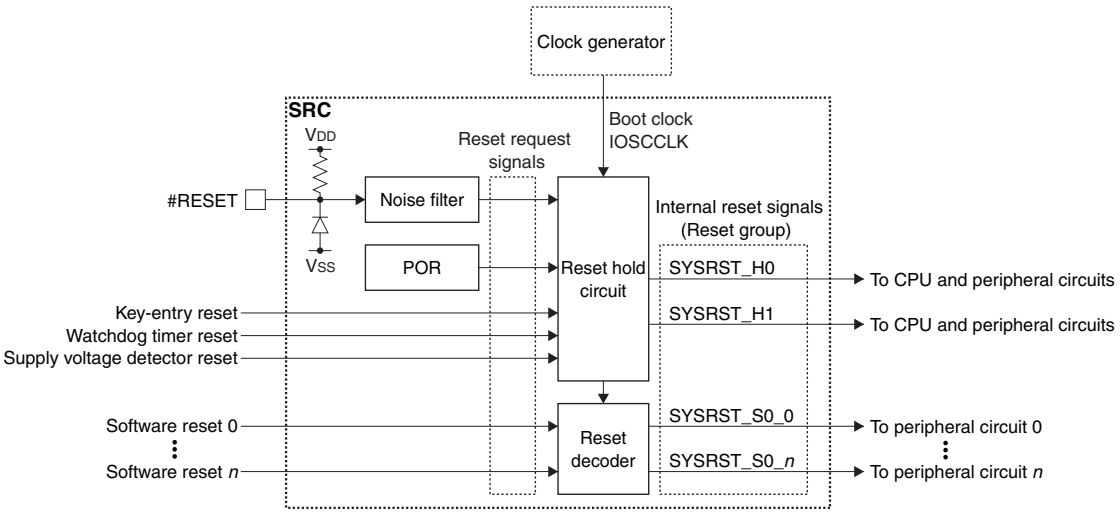


Figure 2.2.1.1 SRC Configuration

2.2.2 Input Pin

Table 2.2.2.1 shows the SRC pin.

Table 2.2.2.1 SRC Pin

Pin name	I/O	Initial status	Function
#RESET	I	I (Pull-up)	Reset input

The #RESET pin is connected to the noise filter that removes pulses not conforming to the requirements. An internal pull-up resistor is connected to the #RESET pin, so the pin can be left open. For the #RESET pin characteristics, refer to "#RESET pin characteristics" in the "Electrical Characteristics" chapter.

2.2.3 Reset Sources

The reset source refers to causes that request system initialization. The following shows the reset sources.

#RESET pin

Inputting a reset signal with a certain low level period to the #RESET pin issues a reset request.

POR

POR (Power On Reset) issues a reset request when the rise of VDD is detected. Reset requests from this circuit ensure that the system will be reset properly when the power is turned on. Figure 2.2.3.1 shows an example of POR internal reset operation according to variations in VDD.

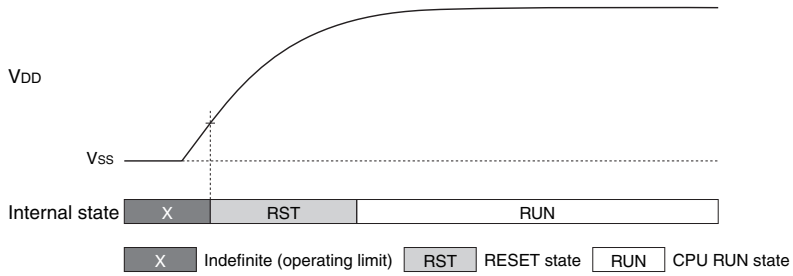


Figure 2.2.3.1 Example of Internal Reset by POR

For the POR electrical specifications, refer to "POR characteristics" in the "Electrical Characteristics" chapter.

Key-entry reset

Inputting a low level signal of a certain period to the I/O port pins configured to a reset input issues a reset request. This function must be enabled using an I/O port register. For more information, refer to the "I/O Ports" chapter.

Watchdog timer reset

Setting the watchdog timer into reset mode will issue a reset request when the counter overflows. This helps return the runaway CPU to a normal operating state. For more information, refer to the "Watchdog timer" chapter.

Supply voltage detector reset

By enabling the low power supply voltage detection reset function, the supply voltage detector will issue a reset request when a drop in the power supply voltage is detected. This makes it possible to put the system into reset state if the IC must be stopped under a low voltage condition. For more information, refer to the "Supply Voltage Detector" chapter.

Peripheral circuit software reset

Some peripheral circuits provide a control bit for software reset (MODEN or SFTRST). Setting this bit initializes the peripheral circuit control bits. Note, however, that the software reset operations depend on the peripheral circuit. For more information, refer to "Control Registers" in each peripheral circuit chapter.

Note: The MODEN bit of some peripheral circuits does not issue software reset.

2.2.4 Initialization Conditions (Reset Groups)

A different initialization condition is set for the CPU registers and peripheral circuit control bits, individually. The reset group refers to an initialization condition. Initialization is performed when a reset source included in a reset group issues a reset request. Table 2.2.4.1 lists the reset groups. For the reset group to initialize the registers and control bits, refer to the "CPU and Debugger" chapter or "Control Registers" in each peripheral circuit chapter.

Table 2.2.4.1 List of Reset Groups

Reset group	Reset source	Reset cancelation timing
H0	#RESET pin POR Key-entry reset Supply voltage detector reset Watchdog timer reset	Reset state is maintained for the reset hold time tRSTR after the reset request is canceled.
H1	#RESET pin POR	
S0	Peripheral circuit software reset (MODEN and SFTRST bits. The software reset operations depend on the peripheral circuit.	Reset state is canceled immediately after the reset request is canceled.

2.3 Clock Generator (CLG)

2.3.1 Overview

CLG is the clock generator that controls the clock sources and manages clock supply to the CPU and the peripheral circuits. The main features of CLG are outlined below.

- Supports multiple clock sources.
  - IOSC oscillator circuit that oscillates with a fast startup and no external parts required
  - High-precision and low-power OSC1 oscillator circuit that uses a 32.768 kHz crystal resonator
  - OSC3 oscillator circuit that supports up to 16.8 MHz crystal/ceramic resonators
  - EXOSC clock input circuit that allows input of square wave and sine wave clock signals
- The system clock (SYSCLK), which is used as the operating clock for the CPU and bus, and the peripheral circuit operating clocks can be configured individually by selecting the suitable clock source and division ratio.
- The 8 MHz clock output from the IOSC oscillator circuit is used as the boot clock for fast booting.
- Controls the oscillator and clock input circuits to enable/disable according to the operating mode, RUN or SLEEP mode.
- Provides a flexible system clock switching function at SLEEP mode cancelation.
  - The clock sources to be stopped in SLEEP mode can be selected.
  - SYSCLK to be used at SLEEP mode cancelation can be selected from all clock sources.
  - The oscillator and clock input circuit on/off state can be maintained or changed at SLEEP mode cancelation.
- Provides the FOUT function to output an internal clock for driving external ICs or for monitoring the internal state.

Figure 2.3.1.1 shows the CLG configuration.

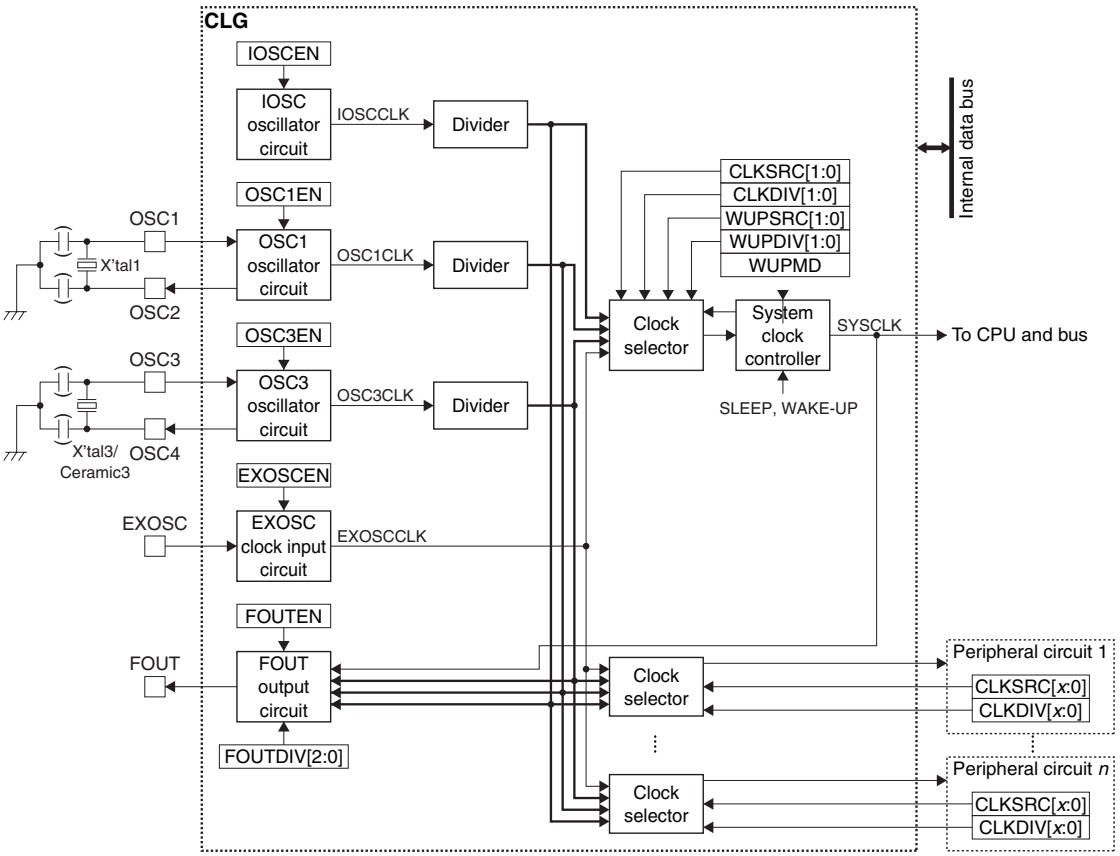


Figure 2.3.1.1 CLG Configuration

2.3.2 Input/Output Pins

Table 2.3.2.1 lists the CLG pins.

Table 2.3.2.1 List of CLG Pins

Pin name	I/O*	Initial status*	Function
OSC1	A	–	OSC1 oscillator circuit input
OSC2	A	–	OSC1 oscillator circuit output
OSC3	A	–	OSC3 oscillator circuit input
OSC4	A	–	OSC3 oscillator circuit output
EXOSC	I	I	EXOSC clock input
FOUT	O	O (L)	FOUT clock output

* Indicates the status when the pin is configured for CLG.

If the port is shared with the CLG input/output function and other functions, the CLG function must be assigned to the port. For more information, refer to the "I/O Ports" chapter.

2.3.3 Clock Sources

IOSC oscillator circuit

The IOSC oscillator circuit features a fast startup and no external parts are required for oscillating. Figure 2.3.3.1 shows the configuration of the IOSC oscillator circuit.

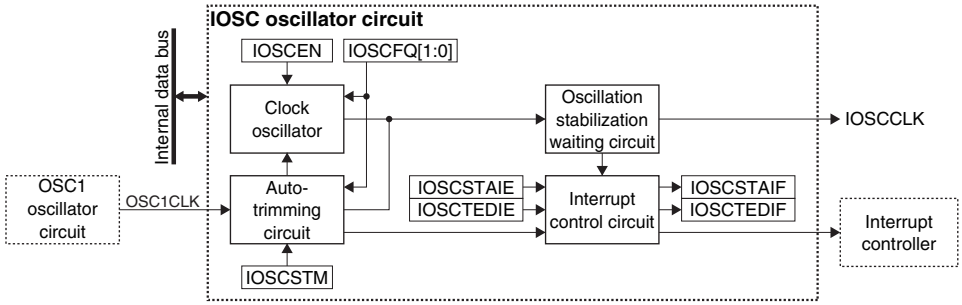


Figure 2.3.3.1 IOSC Oscillator Circuit Configuration

The IOSC oscillator circuit output clock IOSCCLK is used as SYSCLK at booting. The IOSCCLK frequency can be selected using the CLGIOSC.IOSCFQ[1:0] bits. The IOSC oscillator circuit is equipped with an auto-trimming function that automatically adjusts the frequency. This helps reduce frequency deviation due to unevenness in manufacturing quality, temperature, and changes in voltage. For more information on the auto-trimming function and the oscillation characteristics, refer to "IOSC oscillation auto-trimming function" in this chapter and "IOSC oscillator circuit characteristics" in the "Electrical Characteristics" chapter, respectively.

OSC1 oscillator circuit

The OSC1 oscillator circuit is a high-precision and low-power oscillator circuit that uses a 32.768 kHz crystal resonator. Figure 2.3.3.2 shows the configuration of the OSC1 oscillator circuit.

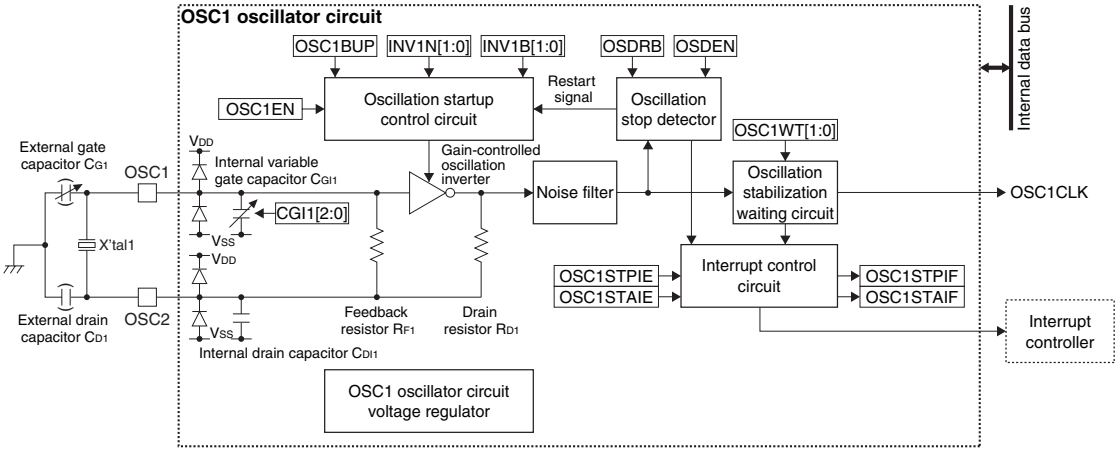


Figure 2.3.3.2 OSC1 Oscillator Circuit Configuration

This oscillator circuit includes a gain-controlled oscillation inverter and a variable gate capacitor allowing use of various crystal resonators with ranges from cylinder type through surface-mount type.

The oscillator circuit also includes a feedback resistor and a drain resistor, so no external parts are required except for a crystal resonator. The embedded oscillation stop detector, which detects oscillation stop and restarts the oscillator, allows the system to operate in safety under adverse environments that may stop the oscillation. The oscillation startup control circuit operates for a set period of time after the oscillation is enabled to assist the oscillator in initiating, this makes it possible to use a low-power resonator that is difficult to start up. For the recommended parts and the oscillation characteristics, refer to the "Basic External Connection Diagram" chapter and "OSC1 oscillator circuit characteristics" in the "Electrical Characteristics" chapter, respectively.

Note: Depending on the circuit board or the crystal resonator type used, an external gate capacitor C_{G1} and a drain capacitor C_{D1} may be required.

OSC3 oscillator circuit

The OSC3 oscillator circuit is a crystal/ceramic oscillator that generates a high-speed clock. Figure 2.3.3.3 shows the configuration of the OSC3 oscillator circuit.

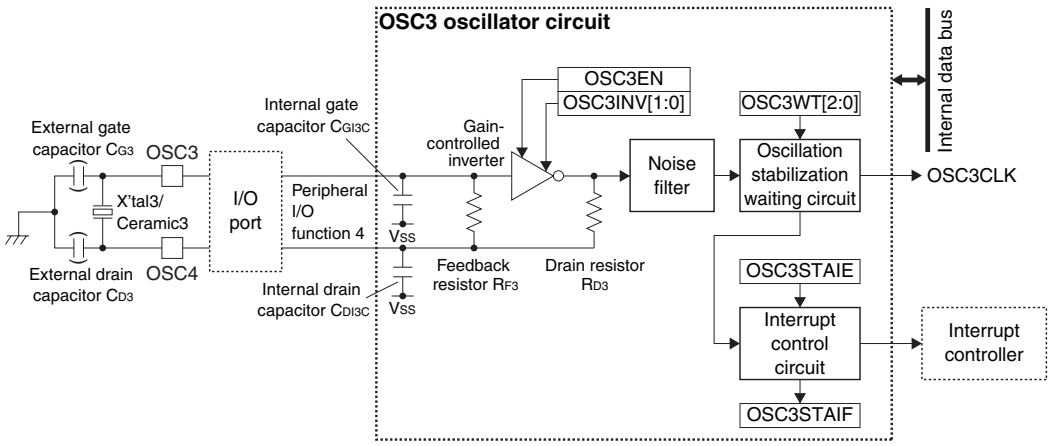


Figure 2.3.3.3 OSC3 Oscillator Circuit Configuration

This oscillator circuit includes a feedback resistor and a drain resistor, so no external part is required except for a crystal/ceramic resonator. The embedded gain-controlled inverter allows selection of the resonator from a wide frequency range.

For the recommended parts and the oscillation characteristics, refer to the "Basic External Connection Diagram" chapter and the "Electrical Characteristics" chapter, respectively.

EXOSC clock input

EXOSC is an external clock input circuit that supports square wave and sine wave clocks. Figure 2.3.3.4 shows the configuration of the EXOSC clock input circuit.

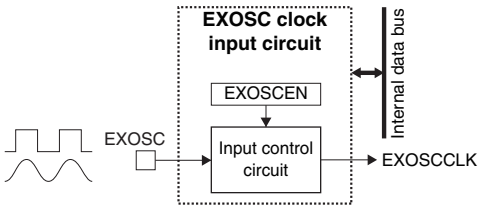


Figure 2.3.3.4 EXOSC Clock Input Circuit

EXOSC has no oscillation stabilization waiting circuit included, therefore, it must be enabled when a stabilized clock is being supplied. For the input clock characteristics, refer to "EXOSC external clock input characteristics" in the "Electrical Characteristics" chapter.

2.3.4 Operations

Oscillation start time and oscillation stabilization waiting time

The oscillation start time refers to the time after the oscillator circuit is enabled until the oscillation signal is actually sent to the internal circuits. The oscillation stabilization waiting time refers to the time it takes the clock to stabilize after the oscillation starts. To avoid malfunctions of the internal circuits due to an unstable clock during this period, the oscillator circuit includes an oscillation stabilization waiting circuit that can disable supplying the clock to the system until the designated time has elapsed. Figure 2.3.4.1 shows the relationship between the oscillation start time and the oscillation stabilization waiting time.

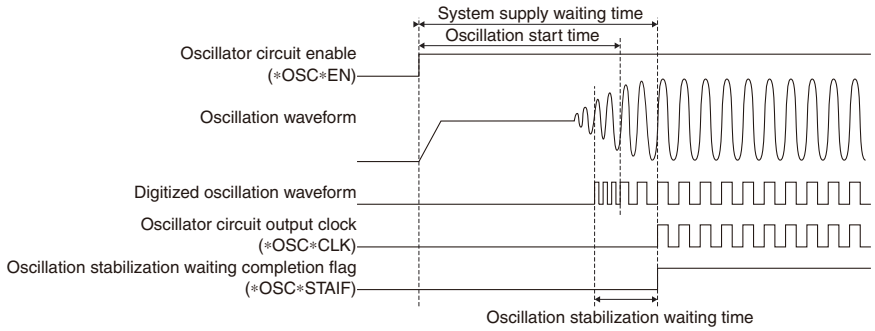


Figure 2.3.4.1 Oscillation Start Time and Oscillation Stabilization Waiting Time

The oscillation stabilization waiting times for the OSC1 and OSC3 oscillator circuits can be set using the CLGOSC1.OSC1WT[1:0] bits and CLGOSC3.OSC3WT[2:0] bits, respectively. To check whether the oscillation stabilization waiting time is set properly and the clock is stabilized immediately after the oscillation starts or not, monitor the oscillation clock using the FOUT output function. The oscillation stabilization waiting time for the IOSC oscillator circuit is fixed at 16 IOSCCLK clocks. The oscillation stabilization waiting time for the OSC1 oscillator circuit should be set to 16,384 OSC1CLK clocks or more. The oscillation stabilization waiting time for the OSC3 oscillator circuit should be set to 1,024 OSC3CLK clocks or more.
When the oscillation stabilization waiting operation has completed, the oscillator circuit sets the oscillation stabilization waiting completion flag and starts clock supply to the internal circuits.

Note: The oscillation stabilization waiting time is always expended at start of oscillation even if the oscillation stabilization waiting completion flag has not be cleared to 0.

When the oscillation startup control circuit in the OSC1 oscillator circuit is enabled by setting the CLGOSC1.OSC1BUP bit to 1, it uses the high-gain oscillation inverter for a set period of time (startup boosting operation) after the oscillator circuit is enabled (by setting the CLGOSC.OSC1EN bit to 1) to reduce oscillation start time. Note, however, that the oscillation operation may become unstable if there is a large gain differential between normal operation and startup boosting operation. Furthermore, the oscillation start time being actually reduced depends on the characteristics of the resonator used. Figure 2.3.4.2 shows an operation example when the oscillation startup control circuit is used.

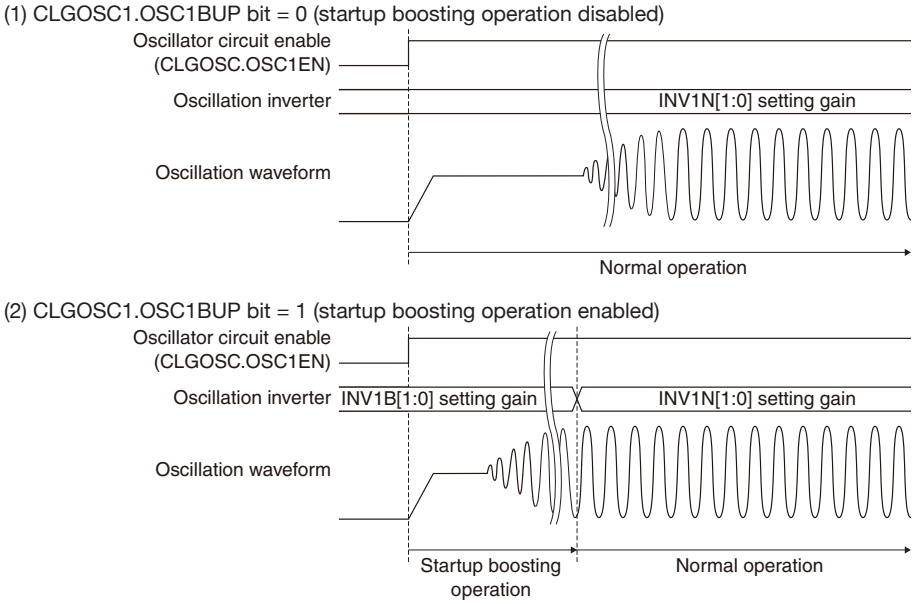


Figure 2.3.4.2 Operation Example when the Oscillation Startup Control Circuit is Used

Oscillation start procedure for the IOSC oscillator circuit

Follow the procedure shown below to start oscillation of the IOSC oscillator circuit.

1. Write 1 to the CLGINTF.IOSCSTAIF bit. (Clear interrupt flag)
2. Write 1 to the CLGINTE.IOSCSTAIE bit. (Enable interrupt)
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. Configure the CLGIOSC.IOSCFQ[1:0] bits. (Select frequency)
5. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
6. Write 1 to the CLGOSC.IOSCEN bit. (Start oscillation)
7. IOSCCLK can be used if the CLGINTF.IOSCSTAIF bit = 1 after an interrupt occurs.

Note: Make sure that the CLGOSC.IOSCEN bit is set to 0 (oscillation stopped) before selecting the frequency using the CLGIOSC.IOSCFQ[1:0] bits.

Oscillation start procedure for the OSC1 oscillator circuit

Follow the procedure shown below to start oscillation of the OSC1 oscillator circuit.

1. Write 1 to the CLGINTF.OSC1STAIF bit. (Clear interrupt flag)
2. Write 1 to the CLGINTE.OSC1STAIE bit. (Enable interrupt)
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. Configure the following CLGOSC1 register bits according to the resonator used:
   - CLGOSC1.INV1N[1:0] bits (Set oscillation inverter gain)
   - CLGOSC1.CGI1[2:0] bits (Set internal gate capacitor)
   - CLGOSC1.OSC1WT[1:0] bits (Set oscillation stabilization waiting time)

   In addition to the above, configure the following bits when using the oscillation startup control circuit (see Figure 2.3.4.2):
   - CLGOSC1.INV1B[1:0] bits (Set oscillation inverter gain for startup boosting period)
   - Set the CLGOSC1.OSC1BUP bit to 1. (Enable oscillation startup control circuit)
5. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits.(Set system protection)
6. Write 1 to the CLGOSC.OSC1EN bit. (Start oscillation)
7. OSC1CLK can be used if the CLGINTF.OSC1STAIF bit = 1 after an interrupt occurs.

The setting values of the CLGOSC1.INV1N[1:0], CLGOSC1.CGI1[2:0], CLGOSC1.OSC1WT[1:0], and CLGOSC1.INV1B[1:0] bits should be determined after performing evaluation using the populated circuit board.

Oscillation start procedure for the OSC3 oscillator circuit

Follow the procedure shown below to start oscillation of the OSC3 oscillator circuit.

1. Write 1 to the CLGINTF.OSC3STAIF bit. (Clear interrupt flag)
2. Write 1 to the CLGINTE.OSC3STAIE bit. (Enable interrupt)
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. Configure the following CLGOSC3 register bits.
   - CLGOSC3.OSC3WT[2:0] bits (Set oscillation stabilization waiting time)
   - CLGOSC3.OSC3INV[1:0] bits (Set oscillation inverter gain)
5. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
6. Assign the OSC3 oscillator input/output functions to the ports. (Refer to the "I/O Ports" chapter.)
7. Write 1 to the CLGOSC.OSC3EN bit. (Start oscillation)
8. OSC3CLK can be used if the CLGINTF.OSC3STAIF bit = 1 after an interrupt occurs.

The setting values of the CLGOSC3.OSC3INV[1:0] and CLGOSC3.OSC3WT[2:0] bits should be determined after performing evaluation using the populated circuit board.

System clock switching

The CPU boots using IOSCCLK as SYSCLK. After booting, the clock source of SYSCLK can be switched according to the processing speed required. The SYSCLK frequency can also be set by selecting the clock source division ratio, this makes it possible to run the CPU at the most suitable performance for the process to be executed. The CLGSCLK.CLKSRC[1:0] and CLGSCLK.CLKDIV[1:0] bits are used for this control.
The CLGSCLK register bits are protected against writings by the system protect function, therefore, the system protection must be removed by writing 0x0096 to the MSCPROT.PROT[15:0] bits before the register setting can be altered. For the transition between the operating modes including the system clock switching, refer to "Operating Mode."

Note: When selecting a clock source with a frequency of 12.6 MHz or higher, the setting of the FLASHCWAIT.RDWAIT[1:0] bits must be altered. For detailed information on the FLASHCWAIT.RDWAIT[1:0] bits, refer to "Control Registers (FLASHC Flash Read Cycle Register)" in the "Memory and Bus" chapter.

Clock control in SLEEP mode

The CPU enters SLEEP mode when it executes the slp instruction. Whether the clock sources being operated are stopped or not at this point can be selected in each source individually. This allows the CPU to fast switch between SLEEP mode and RUN mode, and the peripheral circuits to continue operating without disabling the clock in SLEEP mode. The CLGOSC.IOSCSLPC, CLGOSC.OSC1SLPC, CLGOSC.OSC3SLPC, and CLGOSC.EXOSCSLPC bits are used for this control. Figure 2.3.4.3 shows a control example.

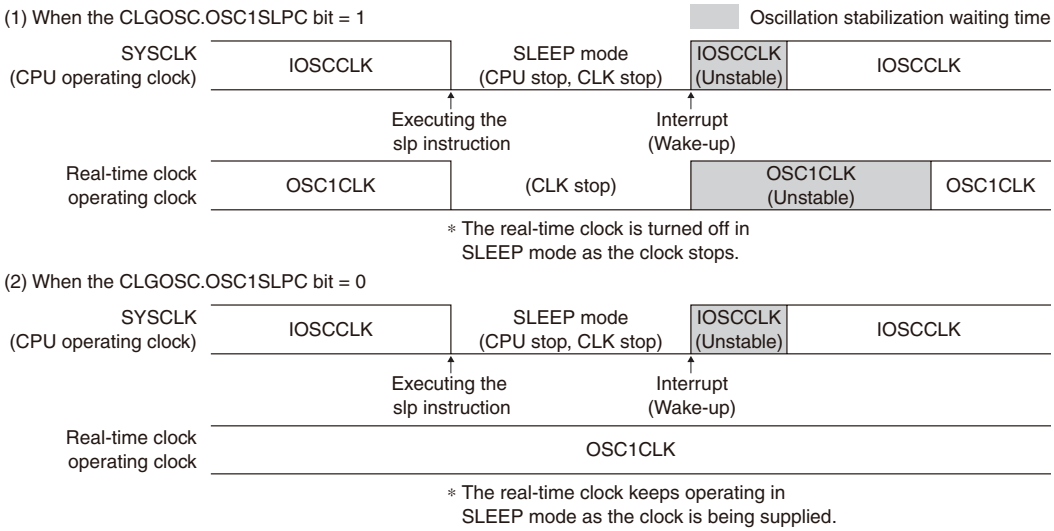


Figure 2.3.4.3 Clock Control Example in SLEEP Mode

The SYSCLK condition (clock source and division ratio) at wake-up from SLEEP mode to RUN mode can also be configured. This allows flexible clock control according to the wake-up process. Configure the clock using the CLGSCLK.WUPSRC[1:0] and CLGSCLK.WUPDIV[1:0] bits, and write 1 to the CLGSCLK.WUPMD bit to enable this function.

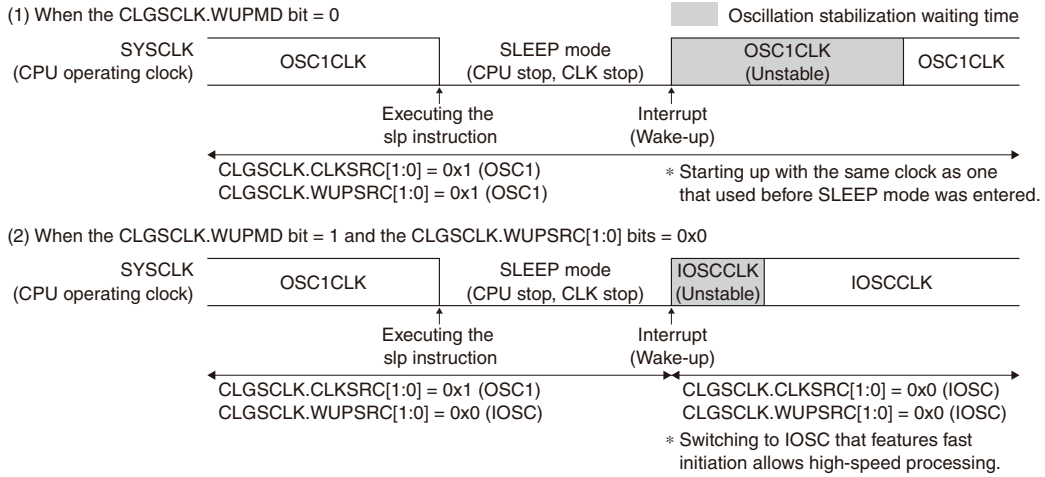


Figure 2.3.4.4 Clock Control Example at SLEEP Cancelation

Clock external output (FOUT)

The FOUT pin can output the clock generated by a clock source or its divided clock to outside the IC. This allows monitoring the oscillation frequency of the oscillator circuit or supplying an operating clock to external ICs. Follow the procedure shown below to start clock external output.

1. Assign the FOUT function to the port. (Refer to the "I/O Ports" chapter.)
2. Configure the following CLGFOUT register bits:
   - CLGFOUT.FOUTSRC[1:0] bits (Select clock source)
   - CLGFOUT.FOUTDIV[2:0] bits (Set clock division ratio)
   - Set the CLGFOUT.FOUTEN bit to 1. (Enable clock external output)

IOSC oscillation auto-trimming function

The auto-trimming function adjusts the IOSCCLK clock frequency selected using the CLGIOSC.IOSCFQ[1:0] bits by trimming the clock with reference to the high precision OSC1CLK clock generated by the OSC1 oscillator circuit. Follow the procedure shown below to enable the auto-trimming function.

1. After enabling the OSC1 oscillation, check if the stabilized clock is supplied (CLGINTF.OSC1STAIF bit = 1).
2. After enabling the IOSC oscillation, check if the stabilized clock is supplied (CLGINTF.IOSCSTAIF bit = 1).
3. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
4. If the SYSCLK clock source is IOSC, set the CLGSCLK.CLKSRC[1:0] bits to a value other than 0x0 (IOSC).
5. Write 1 to the CLGINTF.IOSCTEDIF bit. (Clear interrupt flag)
6. Write 1 to the CLGINTE.IOSCTEDIE bit. (Enable interrupt)
7. Write 1 to the CLGIOSC.IOSCSTM bit. (Enable IOSC oscillation auto-trimming)
8. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
9. The trimmed IOSCCLK can be used if the CLGINTF.IOSCTEDIF bit = 1 after an interrupt occurs.

After the trimming operation has completed, the CLGIOSC.IOSCSTM bit automatically reverts to 0. Although the trimming time depends on the temperature, an average of several 10 ms is required. When IOSCCLK is being used as the system clock or a peripheral circuit clock, do not use the auto-trimming function.

OSC1 oscillation stop detection function

The oscillation stop detection function restarts the OSC1 oscillator circuit when it detects oscillation stop under adverse environments that may stop the oscillation. Follow the procedure shown below to enable the oscillation stop detection function.

1. After enabling the OSC1 oscillation, check if the stabilized clock is supplied (CLGINTF.OSC1STAIF bit = 1).
2. Write 1 to the CLGINTF.OSC1STPIF bit. (Clear interrupt flag)
3. Write 1 to the CLGINTE.OSC1STPIE bit. (Enable interrupt)
4. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
5. Set the following CLGOSC1 register bits:
   - Set the CLGOSC1.OSDRB bit to 1. (Enable OSC1 restart function)
   - Set the CLGOSC1.OSDEN bit to 1. (Enable oscillation stop detection function)
6. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)
7. The OSC1 oscillation stops if the CLGINTF.OSC1STPIF bit = 1 after an interrupt occurs. If the CLGOSC1.OSDRB bit = 1, the hardware restarts the OSC1 oscillator circuit.

Note: Enabling the oscillation stop detection function increase the oscillation stop detector current (I_{OSD1}).

2.4 Operating Mode

2.4.1 Initial Boot Sequence

Figure 2.4.1.1 shows the initial boot sequence after power is turned on.

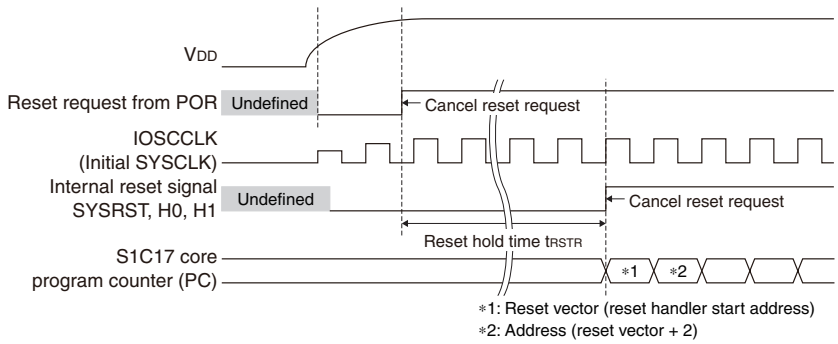


Figure 2.4.1.1 Initial Boot Sequence

Note: The reset cancelation time at power-on varies according to the power rise time and reset request cancelation time.

For the reset hold time t_{RSTR}, refer to "Reset hold circuit characteristics" in the "Electrical Characteristics" chapter.

2.4.2 Transition between Operating Modes

State transitions between operating modes shown in Figure 2.4.2.1 take place in this IC.

RUN mode

RUN mode refers to the state in which the CPU is executing the program. A transition to this mode takes place when the system reset request from the system reset controller is canceled. RUN mode is classified into "IOSC RUN," "OSC1 RUN," "OSC3 RUN," and "EXOSC RUN" by the SYSCLK clock source.

HALT mode

When the CPU executes the halt instruction, it suspends program execution and stops operating. This state is HALT mode. In this mode, the clock sources and peripheral circuits keep operating. This mode can be set while no software processing is required and it reduces power consumption as compared with RUN mode. HALT mode is classified into "IOSC HALT," "OSC1 HALT," "OSC3 HALT," and "EXOSC HALT" by the SYSCLK clock source.

SLEEP mode

When the CPU executes the slp instruction, it suspends program execution and stops operating. This state is SLEEP mode. In this mode, the clock sources stop operating as well.

However, the clock source in which the CLGOSC.IOSCSLPC/OSC1SLPC/OSC3SLPC/EXOSCSLPC bit is set to 0 keeps operating, so the peripheral circuits with the clock being supplied can also operate. By setting this mode when no software processing and peripheral circuit operations are required, power consumption can be less than HALT mode.

Note: The current consumption when a clock source is active in SLEEP mode by setting the CLGOSC.IOSCSLPC/OSC1SLPC/OSC3SLPC/EXOSCSLPC bit to 0 is equivalent to the value in HALT mode with the same clock source condition (refer to "Current Consumption, Current consumption in HALT mode I_{HALT1}, I_{HALT2}, and I_{HALT3}" in the "Electrical Characteristics" chapter).

DEBUG mode

When a debug interrupt occurs, the CPU enters DEBUG mode. DEBUG mode is canceled when the retd instruction is executed. For more information on DEBUG mode, refer to "Debugger" in the "CPU and Debugger" chapter.

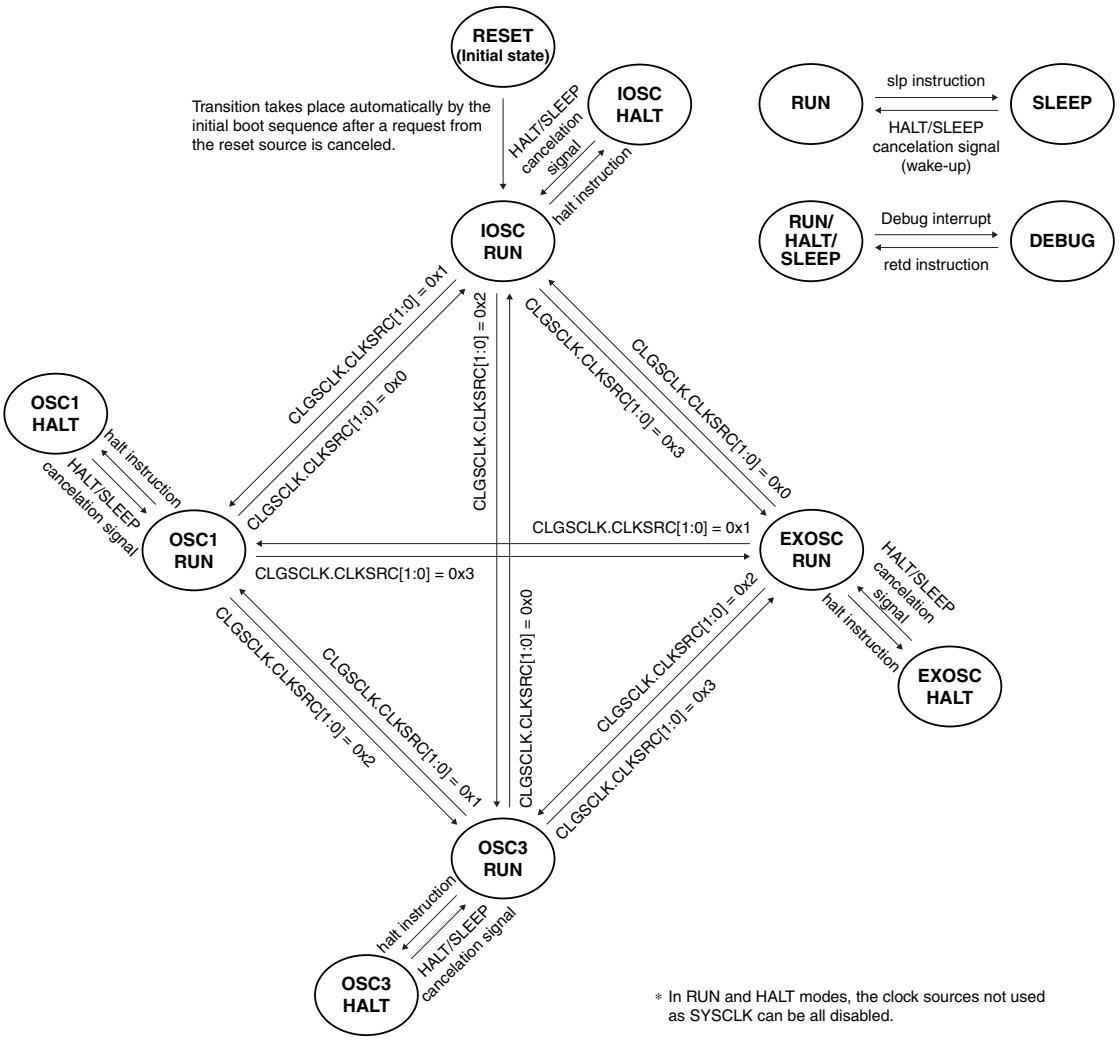


Figure 2.4.2.1 Operating Mode-to-Mode State Transition Diagram

Canceling HALT or SLEEP mode

The conditions listed below generate the HALT/SLEEP cancelation signal to cancel HALT or SLEEP mode and put the CPU into RUN mode. This transition is executed even if the CPU does not accept the interrupt request.

- Interrupt request from a peripheral circuit
- NMI from the watchdog timer
- Debug interrupt
- Reset request

2.5 Interrupts

CLG has a function to generate the interrupts shown in Table 2.5.1.

Table 2.5.1 CLG Interrupt Functions

Interrupt	Interrupt flag	Set condition	Clear condition
IOSC oscillation stabilization waiting completion	CLGINTF.IOSCSTAIF	When the IOSC oscillation stabilization waiting operation has completed after the oscillation starts	Writing 1
OSC1 oscillation stabilization waiting completion	CLGINTF.OSC1STAIF	When the OSC1 oscillation stabilization waiting operation has completed after the oscillation starts	Writing 1
OSC3 oscillation stabilization waiting completion	CLGINTF.OSC3STAIF	When the OSC3 oscillation stabilization waiting operation has completed after the oscillation starts	Writing 1
OSC1 oscillation stop	CLGINTF.OSC1STPIF	When OSC1CLK is stopped, or when the CLGOSC.OSC1EN or CLGOSC1.OSDEN bit setting is altered from 1 to 0.	Writing 1
IOSC oscillation auto-trimming completion	CLGINTF.IOSCTEDIF	When the IOSC oscillation auto-trimming operation has completed	Writing 1

CLG provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

2.6 Control Registers

PWG V_{D1} Regulator Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PWGVD1CTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1–0	REGMODE[1:0]	0x0	H0	R/WP	

Bits 15–2 Reserved

Bits 1–0 REGMODE[1:0]

These bits control the internal regulator operating mode.

Table 2.6.1 Internal Regulator Operating Mode

PWGVD1CTL.REGMODE[1:0] bits	Operating mode
0x3	Economy mode
0x2	Normal mode
0x1	Reserved
0x0	Automatic mode

CLG System Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGSCLK	15	WUPMD	0	H0	R/WP	–
	14	–	0	–	R	
	13–12	WUPDIV[1:0]	0x0	H0	R/WP	
	11–10	–	0x0	–	R	
	9–8	WUPSRC[1:0]	0x0	H0	R/WP	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bit 15 WUPMD

This bit enables the SYSCLK switching function at wake-up.
1 (R/WP): Enable
0 (R/WP): Disable

When the CLGSCLK.WUPMD bit = 1, setting values of the CLGSCLK.WUPSRC[1:0] bits and the CLGSCLK.WUPDIV[1:0] bits are loaded to the CLGSCLK.CLKSRC[1:0] bits and the CLGSCLK.CLKDIV[1:0] bits, respectively, at wake-up from SLEEP mode to switch SYSCLK. When the CLGSCLK.WUPMD bit = 0, the CLGSCLK.CLKSRC[1:0] and CLGSCLK.CLKDIV[1:0] bits are not altered at wake-up.

Note: Do not set the CLGSCLK.WUPMD bit to 1 when placing the IC into SLEEP mode with the CLGOSC.****SLPC bit set to 0.

Bit 14 Reserved

Bits 13–12 WUPDIV[1:0]

These bits select the SYSCLK division ratio for resetting the CLGSCLK.CLKDIV[1:0] bits at wake-up. This setting is ineffective when the CLGSCLK.WUPMD bit = 0.

Bits 11–10 Reserved

Bits 9–8 WUPSRC[1:0]

These bits select the SYSCLK clock source for resetting the CLGSCLK.CLKSRC[1:0] bits at wake-up. When a currently stopped clock source is selected, it will automatically start oscillating or clock input at wake-up. However, this setting is ineffective when the CLGSCLK.WUPMD bit = 0.

Table 2.6.2 SYSCLK Clock Source and Division Ratio Settings at Wake-up

CLGSCLK. WUPDIV[1:0] bits	CLGSCLK.WUPSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSCCLK	OSC1CLK	OSC3CLK	EXOSCCLK
0x3	1/8	Reserved	1/16	Reserved
0x2	1/4	Reserved	1/8	Reserved
0x1	1/2	1/2	1/2	Reserved
0x0	1/1	1/1	1/1	1/1

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits set the division ratio of the clock source to determine the SYSCLK frequency.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the SYSCLK clock source.
When a currently stopped clock source is selected, it will automatically start oscillating or clock input.

Table 2.6.3 SYSCLK Clock Source and Division Ratio Settings

CLGSCLK. CLKDIV[1:0] bits	CLGSCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSCCLK	OSC1CLK	OSC3CLK	EXOSCCLK
0x3	1/8	Reserved	1/16	Reserved
0x2	1/4	Reserved	1/8	Reserved
0x1	1/2	1/2	1/2	Reserved
0x0	1/1	1/1	1/1	1/1

CLG Oscillation Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGOSC	15–12	–	0x0	–	R	–
	11	EXOSCSLPC	1	H0	R/W	
	10	OSC3SLPC	1	H0	R/W	
	9	OSC1SLPC	1	H0	R/W	
	8	IOSCSLPC	1	H0	R/W	
	7–4	–	0x0	–	R	
	3	EXOSCEN	0	H0	R/W	
	2	OSC3EN	0	H0	R/W	
	1	OSC1EN	0	H0	R/W	
	0	IOSCEN	1	H0	R/W	

Bits 15–12 Reserved

Bit 11 EXOSCSLPC
Bit 10 OSC3SLPC
Bit 9 OSC1SLPC
Bit 8 IOSCSLPC

These bits control the clock source operations in SLEEP mode.
1 (R/W): Stop clock source in SLEEP mode
0 (R/W): Continue operation state before SLEEP

Each bit corresponds to the clock source as follows:
CLGOSC.EXOSCSLPC bit: EXOSC clock input
CLGOSC.OSC3SLPC bit: OSC3 oscillator circuit
CLGOSC.OSC1SLPC bit: OSC1 oscillator circuit
CLGOSC.IOSCSLPC bit: IOSC oscillator circuit

Bits 7–4 Reserved

Bit 3 EXOSCEN
Bit 2 OSC3EN
Bit 1 OSC1EN
Bit 0 IOSCEN

These bits control the clock source operation.
1(R/W): Start oscillating or clock input
0(R/W): Stop oscillating or clock input

Each bit corresponds to the clock source as follows:
CLGOSC.EXOSCEN bit: EXOSC clock input
CLGOSC.OSC3EN bit: OSC3 oscillator circuit
CLGOSC.OSC1EN bit: OSC1 oscillator circuit
CLGOSC.IOSCEN bit: IOSC oscillator circuit

CLG IOSC Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGIOSC	15–8	–	0x00	–	R	–
	7–5	–	0x0	–	R	
	4	IOSCSTM	0	H0	R/WP	
	3–2	–	0x0	–	R	
	1-0	IOSCFQ[1:0]	0x1	H0	R/WP	

Bits 15–5 Reserved

Bit 4 IOSCSTM

This bit controls the IOSCCLK auto-trimming function.

1 (WP): Start trimming

0 (WP): Stop trimming

1 (R): Trimming is executing.

0 (R): Trimming has finished. (Trimming operation inactivated.)

This bit is automatically cleared to 0 when trimming has finished.

Notes: • Do not use IOSCCLK as the system clock or peripheral circuit clocks while the CLGIOSC. IOSCSTM bit = 1.

• The auto-trimming function does not work if the OSC1 oscillator circuit is stopped. Make sure the CLGINTF.OSC1STAIF bit is set to 1 before starting the trimming operation.

• Be sure to avoid altering the CLGIOSC.IOSCFQ[1:0] bits while the auto-trimming is being executed.

Bits 3–2 Reserved

Bits 1–0 IOSCFQ[1:0]

These bits select the IOSCCLK frequency.

Table 2.6.4 IOSCCLK Frequency Selection

CLGIOSC.IOSCFQ[1:0] bits	IOSCCLK frequency
0x3	16 MHz
0x2	12 MHz
0x1	8 MHz
0x0	4 MHz

CLG OSC1 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGOSC1	15	–	0	–	R	–
	14	OSDRB	1	H0	R/WP	
	13	OSDEN	0	H0	R/WP	
	12	OSC1BUP	1	H0	R/WP	
	11	–	0	–	R	
	10–8	CGI1[2:0]	0x0	H0	R/WP	
	7–6	INV1B[1:0]	0x2	H0	R/WP	
	5–4	INV1N[1:0]	0x1	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	OSC1WT[1:0]	0x2	H0	R/WP	

Bit 15 Reserved

Bit 14 OSDRB

This bit enables the OSC1 oscillator circuit restart function by the oscillation stop detector when OSC1 oscillation stop is detected.

1 (R/WP): Enable (Restart the OSC1 oscillator circuit when oscillation stop is detected.)

0 (R/WP): Disable

Bit 13 OSDEN

This bit controls the oscillation stop detector in the OSC1 oscillator circuit.
1 (R/WP): OSC1 oscillation stop detector on
0 (R/WP): OSC1 oscillation stop detector off

Note: Do not write 1 to the CLGOSC1.OSDEN bit before stabilized OSC1CLK is supplied. Furthermore, the CLGOSC1.OSDEN bit should be set to 0 when the CLGOSC.OSC1EN bit is set to 0.

Bit 12 OSC1BUP

This bit enables the oscillation startup control circuit in the OSC1 oscillator circuit.
1 (R/WP): Enable (Activate booster operation at startup.)
0 (R/WP): Disable

Bit 11 Reserved

Bits 10–8 CGI1[2:0]

These bits set the internal gate capacitance in the OSC1 oscillator circuit.

Table 2.6.5 OSC1 Internal Gate Capacitance Setting

CLGOSC1.CGI1[2:0] bits	Capacitance
0x7	Max.
0x6	↑
0x5	
0x4	
0x3	
0x2	
0x1	↓
0x0	Min.

For more information, refer to "OSC1 oscillator circuit characteristics, Internal gate capacitance C_{GI1}" in the "Electrical Characteristics" chapter.

Bits 7–6 INV1B[1:0]

These bits set the oscillation inverter gain that will be applied at boost startup of the OSC1 oscillator circuit.

Table 2.6.6 Setting Oscillation Inverter Gain at OSC1 Boost Startup

CLGOSC1.INV1B[1:0] bits	Inverter gain
0x3	Max.
0x2	↑
0x1	↓
0x0	Min.

Note: The CLGOSC1.INV1B[1:0] bits must be set to a value equal to or larger than the CLGOSC1. INV1N[1:0] bits.

Bits 5–4 INV1N[1:0]

These bits set the oscillation inverter gain applied at normal operation of the OSC1 oscillator circuit.

Table 2.6.7 Setting Oscillation Inverter Gain at OSC1 Normal Operation

CLGOSC1.INV1N[1:0] bits	Inverter gain
0x3	Max.
0x2	↑
0x1	↓
0x0	Min.

Bits 3–2 Reserved

Bits 1–0 OSC1WT[1:0]

These bits set the oscillation stabilization waiting time for the OSC1 oscillator circuit.

Table 2.6.8 OSC1 Oscillation Stabilization Waiting Time Setting

CLGOSC1.OSC1WT[1:0] bits	Oscillation stabilization waiting time
0x3	65,536 clocks
0x2	16,384 clocks
0x1	4,096 clocks
0x0	Reserved

CLG OSC3 Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGOSC3	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–4	OSC3INV[1:0]	0x3	H0	R/WP	
	3	–	0	–	R	
	2–0	OSC3WT[2:0]	0x6	H0	R/WP	

Bits 15–6 Reserved

Bits 5–4 OSC3INV[1:0]

These bits set the oscillation inverter gain when crystal/ceramic oscillator is selected as the OSC3 oscillator type.

Table 2.6.9 OSC3 Oscillation Inverter Gain Setting

CLGOSC3.OSC3INV[1:0] bits	Inverter gain
0x3	Max.
0x2	↑
0x1	↓
0x0	Min.

Bit 3 Reserved

Bits 2–0 OSC3WT[2:0]

These bits set the oscillation stabilization waiting time for the OSC3 oscillator circuit.

Table 2.6.10 OSC3 Oscillation Stabilization Waiting Time Setting

CLGOSC3.OSC3WT[2:0] bits	Oscillation stabilization waiting time
0x7	65,536 clocks
0x6	16,384 clocks
0x5	4,096 clocks
0x4	1,024 clocks
0x3	256 clocks
0x2	64 clocks
0x1	16 clocks
0x0	4 clocks

CLG Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGINTF	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6	(reserved)	0	H0	R	
	5	OSC1STPIF	0	H0	R/W	Cleared by writing 1.
	4	IOSCTEDIF	0	H0	R/W	
	3	–	0	–	R	–
	2	OSC3STAIF	0	H0	R/W	Cleared by writing 1.
	1	OSC1STAIF	0	H0	R/W	
	0	IOSCSTAIF	0	H0	R/W	

Bits 15–6 Reserved

Bit 5 OSC1STPIF
Bit 4 IOSCTEDIF

These bits indicate the OSC1 oscillation stop and IOSC oscillation auto-trimming completion interrupt cause occurrence statuses.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

Each bit corresponds to the interrupt as follows:
CLGINTF.OSC1STPIF bit: OSC1 oscillation stop interrupt
CLGINTF.IOSCTEDIF bit: IOSC oscillation auto-trimming completion interrupt

Bit 3 Reserved

Bit 2 OSC3STAIF
Bit 1 OSC1STAIF
Bit 0 IOSCSTAIF

These bits indicate the oscillation stabilization waiting completion interrupt cause occurrence status in each clock source.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

Each bit corresponds to the clock source as follows:
CLGINTF.OSC3STAIF bit: OSC3 oscillator circuit
CLGINTF.OSC1STAIF bit: OSC1 oscillator circuit
CLGINTF.IOSCSTAIF bit: IOSC oscillator circuit

Note: The CLGINTF.IOSCSTAIF bit is 0 after system reset is canceled, but IOSCCLK has already been stabilized.

CLG Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGINTE	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6	(reserved)	0	H0	R	
	5	OSC1STPIE	0	H0	R/W	
	4	IOSCTEDIE	0	H0	R/W	
	3	–	0	–	R	
	2	OSC3STAIE	0	H0	R/W	
	1	OSC1STAIE	0	H0	R/W	
	0	IOSCSTAIE	0	H0	R/W	

Bits 15–6 Reserved

Bit 5 OSC1STPIE
Bit 4 IOSCTEDIE

These bits enable the OSC1 oscillation stop and IOSC oscillation auto-trimming completion interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Each bit corresponds to the interrupt as follows:
CLGINTE.OSC1STPIE bit: OSC1 oscillation stop interrupt
CLGINTE.IOSCTEDIE bit: IOSC oscillation auto-trimming completion interrupt

Bit 3 Reserved

Bit 2 OSC3STAIE
Bit 1 OSC1STAIE
Bit 0 IOSCSTAIE

These bits enable the oscillation stabilization waiting completion interrupt of each clock source.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Each bit corresponds to the clock source as follows:
CLGINTE.OSC3STAIE bit: OSC3 oscillator circuit
CLGINTE.OSC1STAIE bit: OSC1 oscillator circuit
CLGINTE.IOSCSTAIE bit: IOSC oscillator circuit

CLG FOUT Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
CLGFOUT	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–4	FOUTDIV[2:0]	0x0	H0	R/W	
	3–2	FOUTSRC[1:0]	0x0	H0	R/W	
	1	–	0	–	R	
	0	FOUTEN	0	H0	R/W	

Bits 15–7 Reserved

Bits 6–4 FOUTDIV[2:0]

These bits set the FOUT clock division ratio.

Bits 3–2 FOUTSRC[1:0]

These bits select the FOUT clock source.

Table 2.6.11 FOUT Clock Source and Division Ratio Settings

CLGFOUT. FOUTDIV[2:0] bits	CLGFOUT.FOUTSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSCCLK	OSC1CLK	OSC3CLK	SYSCLK
0x7	1/128	1/32,768	1/128	Reserved
0x6	1/64	1/4,096	1/64	Reserved
0x5	1/32	1/1,024	1/32	Reserved
0x4	1/16	1/256	1/16	Reserved
0x3	1/8	1/8	1/8	Reserved
0x2	1/4	1/4	1/4	Reserved
0x1	1/2	1/2	1/2	Reserved
0x0	1/1	1/1	1/1	1/1

Note: When the CLGFOUT.FOUTSRC[1:0] bits are set to 0x3, the FOUT output will be stopped in SLEEP/HALT mode as SYSCLK is stopped.

Bit 1 Reserved

Bit 0 FOUTEN

This bit controls the FOUT clock external output.
1 (R/W): Enable external output
0 (R/W): Disable external output

Note: Since the FOUT signal generated is out of sync with writings to the CLGFOUT.FOUTEN bit, a glitch may occur when the FOUT output is enabled or disabled.

3 CPU and Debugger

3.1 Overview

This IC incorporates the Seiko Epson original 16-bit CPU core (S1C17) with a debugger. The main features of the CPU core are listed below.

- Seiko Epson original 16-bit RISC processor
  - 24-bit general-purpose registers: 8
  - 24-bit special registers: 2
  - 8-bit special register: 1
  - Up to 16M bytes of memory space (24-bit address)
  - Harvard architecture using separated instruction bus and data bus
- Compact and fast instruction set optimized for development in C language
  - Code length: 16-bit fixed length
  - Number of instructions: 111 basic instructions (184 including variations)
  - Execution cycle: Main instructions are executed in one cycle.
  - Extended immediate instructions: Immediate data can be extended up to 24 bits.
- Supports reset, NMI, address misaligned, debug, and external interrupts.
  - Reads a vector from the vector table and branches to the interrupt handler routine directly.
  - Can generate software interrupts with a vector number specified (all vector numbers specifiable).
- HALT mode (halt instruction) and SLEEP mode (slp instruction) are provided as the standby function.
- Incorporates a debugger with three-wire communication interface to assist in software development.

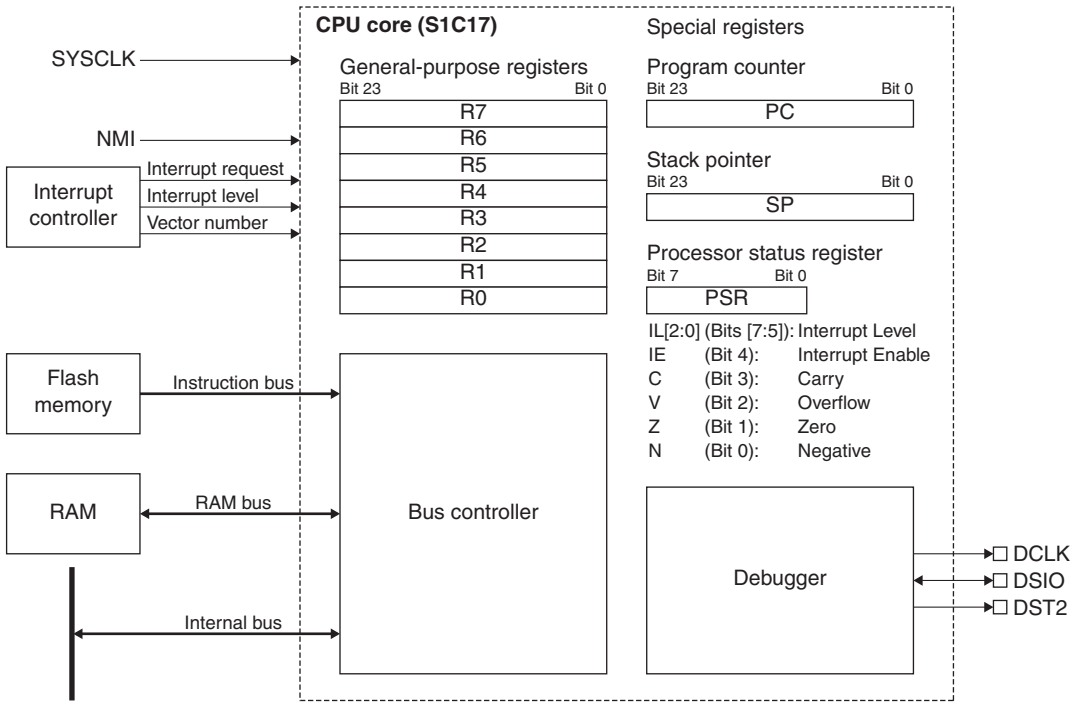


Figure 3.1.1 S1C17 Configuration

3.2 CPU Core

3.2.1 CPU Registers

The CPU includes eight general-purpose registers and three special registers (Table 3.2.1.1).

Table 3.2.1.1 Initialization of CPU Registers

CPU register name			Initial	Reset
General-purpose registers		R0 to R7	0x000000	H0
Special registers	Program counter	PC	The reset vector is automatically loaded.	H0
	Stack pointer	SP	0x000000	H0
	Processor status register	PSR	0x00	H0

For details on the CPU registers, refer to the "S1C17 Family S1C17 Core Manual." For more information on the reset vector, refer to the "Interrupt Controller" chapter.

3.2.2 Instruction Set

The CPU instruction codes are all fixed to 16 bits in length which, combined with pipelined processing, allows the most important instructions to be executed in one cycle. For details on the instructions, refer to the "S1C17 Family S1C17 Core Manual."

3.2.3 Reading PSR

The PSR contents can be read through the MSCPSR register. Note, however, that data cannot be written to PSR through the MSCPSR register.

3.2.4 I/O Area Reserved for the S1C17 Core

The address range from 0xfffc00 to 0xffffff is the I/O area reserved for the S1C17 core. Do not access this area except when it is required.

3.3 Debugger

3.3.1 Debugging Functions

The debugger provides the following functions:

- Instruction break: A debug interrupt is generated immediately before the set instruction address is executed. An instruction break can be set at up to four addresses.
- Single step: A debug interrupt is generated after each instruction has been executed.
- Forcible break: A debug interrupt is generated using an external input signal.
- Software break: A debug interrupt is generated when the brk instruction is executed.

When a debug interrupt occurs, the CPU enters DEBUG mode. The peripheral circuit operations in DEBUG mode depend on the setting of the DBRUN bit provided in the clock control register of each peripheral circuit. For more information on the DBRUN bit, refer to "Clock Supply in DEBUG Mode" in each peripheral circuit chapter. DEBUG mode continues until a cancel command is sent from the personal computer or the CPU executes the retd instruction. Neither hardware interrupts nor NMI are accepted during DEBUG mode.

3.3.2 Resource Requirements and Debugging Tools

Debugging work area

Debugging requires a 64-byte debugging work area. For more information on the work area location, refer to the "Memory and Bus" chapter. The start address of this debugging work area can be read from the DBRAM register.

Debugging tools

To perform debugging, connect ICDmini (S5U1C17001H) to the input/output pin for the debugger embedded in this IC and control it from the personal computer. This requires the tools shown below.

- S1C17 Family In-Circuit Debugger ICDmini (S5U1C17001H)
- S1C17 Family C Compiler Package (e.g., S5U1C17001C)

3.3.3 List of Debugger Input/Output Pins

Table 3.3.3.1 lists the debug pins.

Table 3.3.3.1 List of Debug Pins

Pin name	I/O	Initial state	Function
DCLK	O	O	On-chip debugger clock output pin Outputs a clock to the ICDmini (S5U1C17001H).
DSIO	I/O	I	On-chip debugger data input/output pin Used to input/output debugging data and input the break signal.
DST2	O	O	On-chip debugger status output pin Outputs the processor status during debugging.

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Notes: • Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on.

• Do not drive the DSIO pin with a low level from outside, as it generates a debug interrupt that puts the CPU into DEBUG mode.

3.3.4 External Connection

Figure 3.3.4.1 shows a connection example between this IC and ICDmini when performing debugging.

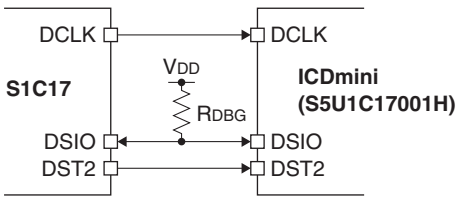


Figure 3.3.4.1 External Connection

For the recommended pull-up resistor value, refer to "Recommended Operating Conditions, DSIO pull-up resistor RDBG" in the "Electrical Characteristics" chapter. RDBG is not required when using the DSIO pin as a general-purpose I/O port pin.

3.3.5 Flash Security Function

This IC provides a security function to protect the internal Flash memory from unauthorized reading and tampering by using the debugger through ICDmini. Figure 3.3.5.1 shows a Flash security function setting flow.

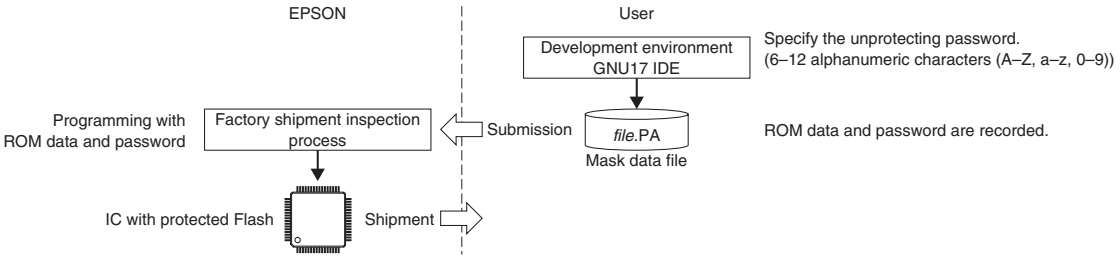


Figure 3.3.5.1 Shipment of IC with ROM Data Programmed and Flash Security Function Setting Flow

The following shows the status of the IC with protected Flash:

- The Flash memory data is undefined if it is read from the debugger.
- An error occurs if an attempt is made to program the Flash memory through ICDmini.

However, the Flash security function can be disabled by entering the unprotecting password predefined to GNU17 IDE (the security function will take effect again after a reset). For setting the password, refer to the "(S1C17 Family C Compiler Package) S5U1C17001C Manual."

Note: Disable the Flash security function before debugging an IC with protected Flash via ICDmini. The debugging functions may not run normally if the Flash security function is enabled.

3.4 Control Register

MISC PSR Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCPSR	15–8	–	0x00	–	R	–
	7–5	PSRIL[2:0]	0x0	H0	R	
	4	PSRIE	0	H0	R	
	3	PSRC	0	H0	R	
	2	PSRV	0	H0	R	
	1	PSRZ	0	H0	R	
	0	PSRN	0	H0	R	

Bits 15–8 Reserved

Bits 7–5 PSRIL[2:0]

The value (0 to 7) of the PSR IL[2:0] (interrupt level) bits can be read out with these bits.

Bit 4 PSRIE

The value (0 or 1) of the PSR IE (interrupt enable) bit can be read out with this bit.

Bit 3 PSRC

The value (0 or 1) of the PSR C (carry) flag can be read out with this bit.

Bit 2 PSRV

The value (0 or 1) of the PSR V (overflow) flag can be read out with this bit.

Bit 1 PSRZ

The value (0 or 1) of the PSR Z (zero) flag can be read out with this bit.

Bit 0 PSRN

The value (0 or 1) of the PSR N (negative) flag can be read out with this bit.

Debug RAM Base Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
DBRAM	31–24	–	0x00	–	R	–
	23–0	DBRAM[23:0]	*1	H0	R	

*1 Debugging work area start address

Bits 31–24 Reserved

Bits 23–0 DBRAM[23:0]

The start address of the debugging work area (64 bytes) can be read out with these bits.

4 Memory and Bus

4.1 Overview

This IC supports up to 16M bytes of accessible memory space for both instructions and data.
The features are listed below.

- Embedded Flash memory that supports on-board programming
- All memory and control registers are accessible in 16-bit width and one cycle.
- Write-protect function to protect system control registers

Figure 4.1.1 shows the memory map.

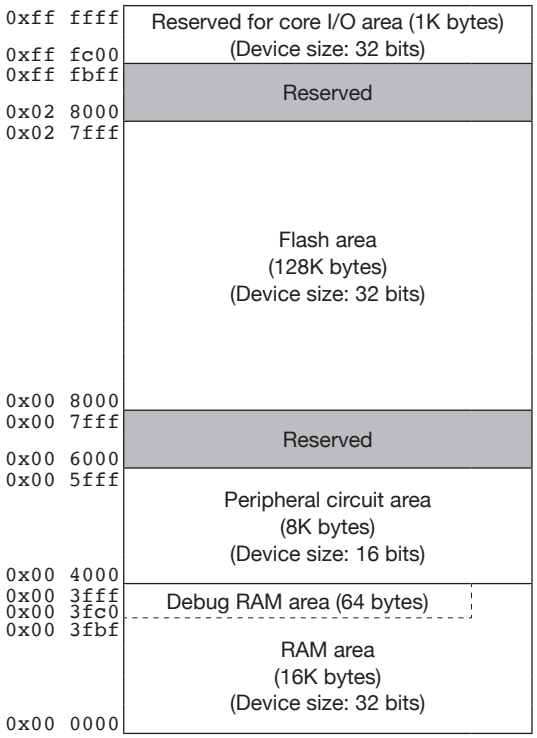


Figure 4.1.1 Memory Map

4.2 Bus Access Cycle

The CPU uses the system clock for bus access operations. First, "Bus access cycle," "Device size," and "Access size" are defined as follows:

- Bus access cycle: One system clock period = 1 cycle
- Device size: Bit width of the memory and peripheral circuits that can be accessed in one cycle
- Access size: Access size designated by the CPU instructions (e.g., ld %rd, [%rb] → 16-bit data transfer)

Table 4.2.1 lists numbers of bus access cycles by different device size and access size. The peripheral circuits can be accessed with an 8-bit, 16-bit, or 32-bit instruction.

Table 4.2.1 Number of Bus Access Cycles

Device size	Access size	Number of bus access cycles
8 bits	8 bits	1
	16 bits	2
	32 bits	4
16 bits	8 bits	1
	16 bits	1
	32 bits	2
32 bits	8 bits	1
	16 bits	1
	32 bits	1

Note: When data is transferred to a memory in 32-bit access, the eight high-order bits are written to the memory as 0x00 since the bit width of the S1C17 core general-purpose registers is 24 bits. Conversely when sending from a memory to a register, the eight high-order bits are ignored.
The CPU performs 32-bit access for stack operations in an interrupt handling. In this case, the CPU read/write 32-bit data that consists of the PSR value as the eight high-order bits and the return address as the 24 low-order bits. For more information, refer to the "S1C17 Family S1C17 Core Manual."

The CPU adopts Harvard architecture that allows simultaneous processing of an instruction fetch and a data access. However, they are not performed simultaneously under one of the conditions listed below. This prolongs the instruction fetch cycle for the number of data area bus cycles.

- When the CPU executes an instruction stored in the Flash area and accesses data in the Flash area
- When the CPU executes an instruction stored in the internal RAM area and accesses data in the internal RAM area

4.3 Flash Memory

The Flash memory is used to store application programs and data. Address 0x8000 in the Flash area is defined as the vector table base address by default, therefore a vector table must be located beginning from this address. For more information on the vector table, refer to "Vector Table" in the "Interrupt Controller" chapter.

4.3.1 Flash Memory Pin

Table 4.3.1.1 shows the Flash memory pin.

Table 4.3.1.1 Flash Memory Pin

Pin name	I/O	Initial status	Function
VPP	P	–	Flash programming power supply

For the VPP voltage, refer to "Recommended Operating Conditions, Flash programming voltage VPP" in the "Electrical Characteristics" chapter.

Note: Always leave the VPP pin open except when programming the Flash memory.

4.3.2 Flash Bus Access Cycle Setting

There is a limit of frequency to access the Flash memory with no wait cycle, therefore, the number of bus access cycles for reading must be changed according to the system clock frequency. The number of bus access cycles for reading can be configured using the FLASHCWAIT.RDWAIT[1:0] bits. Select a setting for higher frequency than the system clock.

4.3.3 Flash Programming

The Flash memory supports on-board programming, so it can be programmed with the ROM data by using the debugger through an ICDmini. Figure 4.3.3.1 shows a connection diagram for on-board programming.

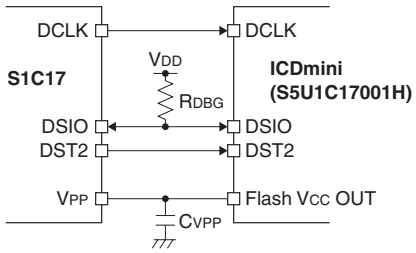


Figure 4.3.3.1 External Connection

The VPP pin must be left open except when programming the Flash memory. However, it is not necessary to disconnect the wire when using ICDmini to supply the VPP power source, as ICDmini controls the power supply so that it will be supplied during Flash programming only. When supplying the VPP power source, be sure to connect CVPP for stabilizing the VPP voltage.
For detailed information on ROM data programming method, refer to the "(S1C17 Family C Compiler Package) S5U1C17001C Manual." The IC can also be shipped after being programmed in the factory with the ROM data developed. Should you desire to ship the IC with ROM data programmed from the factory, please contact our customer support.

4.4 RAM

The RAM can be used to execute the instruction codes copied from another memory as well as storing variables or other data. This allows higher speed processing and lower power consumption than Flash memory.

Note: The 64 bytes at the end of the RAM is reserved as the debug RAM area. When using the debug functions under application development, do not access this area from the application program. This area can be used for applications of mass-produced devices that do not need debugging.

The RAM size used by the application can be configured to equal or less than the implemented size using the MSCIRAMSZ.IRAMSZ[2:0] bits. For example, this function can be used to prevent creating programs that seek to access areas outside the RAM area of the target model when developing an application for a model in which the RAM size is smaller than this IC. After the limitation is applied, accessing an address outside the RAM area results in the same operation (undefined value is read out) as when a reserved area is accessed.

4.5 Peripheral Circuit Control Registers

The control registers for the peripheral circuits are located in the 8K-byte area beginning with address 0x4000. Table 4.5.1 shows the control register map. For details of each control register, refer to "List of Peripheral Circuit Registers" in the appendix or "Control Registers" in each peripheral circuit chapter.

Table 4.5.1 Peripheral Circuit Control Register Map

Peripheral circuit	Address	Register name	
MISC registers (MISC)	0x4000	MSCPROT	MISC System Protect Register
	0x4002	MSCIRAMSZ	MISC IRAM Size Register
	0x4004	MSCTTBRL	MISC Vector Table Address Low Register
	0x4006	MSCTTBRH	MISC Vector Table Address High Register
	0x4008	MSCPSR	MISC PSR Register
Power generator (PWG)	0x4020	PWGVD1CTL	PWG VD1 Regulator Control Register
Clock generator (CLG)	0x4040	CLGSCLK	CLG System Clock Control Register
	0x4042	CLGOSC	CLG Oscillation Control Register
	0x4044	CLGIOSC	CLG IOSC Control Register
	0x4046	CLGOSC1	CLG OSC1 Control Register
	0x4048	CLGOSC3	CLG OSC3 Control Register
	0x404c	CLGINTF	CLG Interrupt Flag Register
	0x404e	CLGINTE	CLG Interrupt Enable Register
	0x4050	CLGFOUT	CLG FOUT Control Register
Interrupt controller (ITC)	0x4080	ITCLV0	ITC Interrupt Level Setup Register 0
	0x4082	ITCLV1	ITC Interrupt Level Setup Register 1
	0x4084	ITCLV2	ITC Interrupt Level Setup Register 2

Peripheral circuit	Address	Register name	
Interrupt controller (ITC)	0x4086	ITCLV3	ITC Interrupt Level Setup Register 3
	0x4088	ITCLV4	ITC Interrupt Level Setup Register 4
	0x408a	ITCLV5	ITC Interrupt Level Setup Register 5
	0x408c	ITCLV6	ITC Interrupt Level Setup Register 6
	0x408e	ITCLV7	ITC Interrupt Level Setup Register 7
	0x4090	ITCLV8	ITC Interrupt Level Setup Register 8
	0x4092	ITCLV9	ITC Interrupt Level Setup Register 9
	0x4094	ITCLV10	ITC Interrupt Level Setup Register 10
	0x4096	ITCLV11	ITC Interrupt Level Setup Register 11
Watchdog timer (WDT)	0x40a0	WDTCLK	WDT Clock Control Register
	0x40a2	WDTCTL	WDT Control Register
Real-time clock (RTCA)	0x40c0	RTCCTL	RTC Control Register
	0x40c2	RTCALM1	RTC Second Alarm Register
	0x40c4	RTCALM2	RTC Hour/Minute Alarm Register
	0x40c6	RTCSWCTL	RTC Stopwatch Control Register
	0x40c8	RTCSEC	RTC Second/1Hz Register
	0x40ca	RTCHUR	RTC Hour/Minute Register
	0x40cc	RTCMON	RTC Month/Day Register
	0x40ce	RTCYAR	RTC Year/Week Register
	0x40d0	RTCINTF	RTC Interrupt Flag Register
	0x40d2	RTCINTE	RTC Interrupt Enable Register
Supply voltage detector (SVD)	0x4100	SVDCLK	SVD Clock Control Register
	0x4102	SVDCTL	SVD Control Register
	0x4104	SVDINTF	SVD Status and Interrupt Flag Register
	0x4106	SVDINTE	SVD Interrupt Enable Register
16-bit timer (T16) Ch.0	0x4160	T16_0CLK	T16 Ch.0 Clock Control Register
	0x4162	T16_0MOD	T16 Ch.0 Mode Register
	0x4164	T16_0CTL	T16 Ch.0 Control Register
	0x4166	T16_0TR	T16 Ch.0 Reload Data Register
	0x4168	T16_0TC	T16 Ch.0 Counter Data Register
	0x416a	T16_0INTF	T16 Ch.0 Interrupt Flag Register
	0x416c	T16_0INTE	T16 Ch.0 Interrupt Enable Register
Flash controller (FLASHC)	0x41b0	FLASHCWAIT	FLASHC Flash Read Cycle Register
I/O ports (PPORT)	0x4200	P0DAT	P0 Port Data Register
	0x4202	P0IOEN	P0 Port Enable Register
	0x4204	P0RCTL	P0 Port Pull-up/down Control Register
	0x4206	P0INTF	P0 Port Interrupt Flag Register
	0x4208	P0INTCTL	P0 Port Interrupt Control Register
	0x420a	P0CHATEN	P0 Port Chattering Filter Enable Register
	0x420c	P0MODSEL	P0 Port Mode Select Register
	0x420e	P0FNCSEL	P0 Port Function Select Register
	0x4210	P1DAT	P1 Port Data Register
	0x4212	P1IOEN	P1 Port Enable Register
	0x4214	P1RCTL	P1 Port Pull-up/down Control Register
	0x4216	P1INTF	P1 Port Interrupt Flag Register
	0x4218	P1INTCTL	P1 Port Interrupt Control Register
	0x421a	P1CHATEN	P1 Port Chattering Filter Enable Register
	0x421c	P1MODSEL	P1 Port Mode Select Register
	0x421e	P1FNCSEL	P1 Port Function Select Register
	0x4220	P2DAT	P2 Port Data Register
	0x4222	P2IOEN	P2 Port Enable Register
	0x4224	P2RCTL	P2 Port Pull-up/down Control Register
	0x4226	P2INTF	P2 Port Interrupt Flag Register
	0x4228	P2INTCTL	P2 Port Interrupt Control Register
	0x422a	P2CHATEN	P2 Port Chattering Filter Enable Register
	0x422c	P2MODSEL	P2 Port Mode Select Register
	0x422e	P2FNCSEL	P2 Port Function Select Register
	0x4230	P3DAT	P3 Port Data Register
	0x4232	P3IOEN	P3 Port Enable Register
	0x4234	P3RCTL	P3 Port Pull-up/down Control Register

Peripheral circuit	Address	Register name	
I/O ports (PPORT)	0x4236	P3INTF	P3 Port Interrupt Flag Register
	0x4238	P3INTCTL	P3 Port Interrupt Control Register
	0x423a	P3CHATEN	P3 Port Chattering Filter Enable Register
	0x423c	P3MODSEL	P3 Port Mode Select Register
	0x423e	P3FNCSEL	P3 Port Function Select Register
	0x4240	P4DAT	P4 Port Data Register
	0x4242	P4IOEN	P4 Port Enable Register
	0x4244	P4RCTL	P4 Port Pull-up/down Control Register
	0x4246	P4INTF	P4 Port Interrupt Flag Register
	0x4248	P4INTCTL	P4 Port Interrupt Control Register
	0x424a	P4CHATEN	P4 Port Chattering Filter Enable Register
	0x424c	P4MODSEL	P4 Port Mode Select Register
	0x424e	P4FNCSEL	P4 Port Function Select Register
	0x4250	P5DAT	P5 Port Data Register
	0x4252	P5IOEN	P5 Port Enable Register
	0x4254	P5RCTL	P5 Port Pull-up/down Control Register
	0x4256	P5INTF	P5 Port Interrupt Flag Register
	0x4258	P5INTCTL	P5 Port Interrupt Control Register
	0x425a	P5CHATEN	P5 Port Chattering Filter Enable Register
	0x425c	P5MODSEL	P5 Port Mode Select Register
	0x425e	P5FNCSEL	P5 Port Function Select Register
	0x4260	P6DAT	P6 Port Data Register
	0x4262	P6IOEN	P6 Port Enable Register
	0x4264	P6RCTL	P6 Port Pull-up/down Control Register
	0x4266	P6INTF	P6 Port Interrupt Flag Register
	0x4268	P6INTCTL	P6 Port Interrupt Control Register
	0x426a	P6CHATEN	P6 Port Chattering Filter Enable Register
	0x426c	P6MODSEL	P6 Port Mode Select Register
	0x426e	P6FNCSEL	P6 Port Function Select Register
	0x4270	P7DAT	P7 Port Data Register
	0x4272	P7IOEN	P7 Port Enable Register
	0x4274	P7RCTL	P7 Port Pull-up/down Control Register
	0x4276	P7INTF	P7 Port Interrupt Flag Register
	0x4278	P7INTCTL	P7 Port Interrupt Control Register
	0x427a	P7CHATEN	P7 Port Chattering Filter Enable Register
	0x427c	P7MODSEL	P7 Port Mode Select Register
	0x427e	P7FNCSEL	P7 Port Function Select Register
	0x4280	P8DAT	P8 Port Data Register
	0x4282	P8IOEN	P8 Port Enable Register
	0x4284	P8RCTL	P8 Port Pull-up/down Control Register
	0x4286	P8INTF	P8 Port Interrupt Flag Register
	0x4288	P8INTCTL	P8 Port Interrupt Control Register
	0x428a	P8CHATEN	P8 Port Chattering Filter Enable Register
	0x428c	P8MODSEL	P8 Port Mode Select Register
	0x428e	P8FNCSEL	P8 Port Function Select Register
	0x4290	P9DAT	P9 Port Data Register
	0x4292	P9IOEN	P9 Port Enable Register
	0x4294	P9RCTL	P9 Port Pull-up/down Control Register
	0x4296	P9INTF	P9 Port Interrupt Flag Register
	0x4298	P9INTCTL	P9 Port Interrupt Control Register
	0x429a	P9CHATEN	P9 Port Chattering Filter Enable Register
	0x429c	P9MODSEL	P9 Port Mode Select Register
	0x429e	P9FNCSEL	P9 Port Function Select Register
	0x42a0	PADAT	PA Port Data Register
	0x42a2	PAIOEN	PA Port Enable Register
	0x42a4	PARCTL	PA Port Pull-up/down Control Register
	0x42a6	PAINTF	PA Port Interrupt Flag Register
	0x42a8	PAINTCTL	PA Port Interrupt Control Register
	0x42aa	PACHATEN	PA Port Chattering Filter Enable Register
	0x42ac	PAMODSEL	PA Port Mode Select Register

Peripheral circuit	Address	Register name	
I/O ports (PPORT)	0x42ae	PAFNCSEL	PA Port Function Select Register
	0x42d0	PDDAT	Pd Port Data Register
	0x42d2	PDIOEN	Pd Port Enable Register
	0x42d4	PDRCTL	Pd Port Pull-up/down Control Register
	0x42dc	PDMODSEL	Pd Port Mode Select Register
	0x42de	PDFNCSEL	Pd Port Function Select Register
	0x42e0	PCLK	P Port Clock Control Register
	0x42e2	PINTFGRP	P Port Interrupt Flag Group Register
Universal port multiplexer (UPMUX)	0x4300	P0UPMUX0	P00–01 Universal Port Multiplexer Setting Register
	0x4302	P0UPMUX1	P02–03 Universal Port Multiplexer Setting Register
	0x4304	P0UPMUX2	P04–05 Universal Port Multiplexer Setting Register
	0x4306	P0UPMUX3	P06–07 Universal Port Multiplexer Setting Register
	0x4308	P3UPMUX0	P30–31 Universal Port Multiplexer Setting Register
	0x430a	P3UPMUX1	P32–33 Universal Port Multiplexer Setting Register
	0x430c	P3UPMUX2	P34–35 Universal Port Multiplexer Setting Register
	0x430e	P3UPMUX3	P36–37 Universal Port Multiplexer Setting Register
	0x4310	P6UPMUX0	P60–61 Universal Port Multiplexer Setting Register
	0x4312	P6UPMUX1	P62–63 Universal Port Multiplexer Setting Register
	0x4314	P6UPMUX2	P64–65 Universal Port Multiplexer Setting Register
	0x4316	P6UPMUX3	P66–67 Universal Port Multiplexer Setting Register
	0x4318	P7UPMUX0	P70–71 Universal Port Multiplexer Setting Register
	0x431a	P7UPMUX1	P72–73 Universal Port Multiplexer Setting Register
	0x431c	P7UPMUX2	P74–75 Universal Port Multiplexer Setting Register
	0x431e	P7UPMUX3	P76–77 Universal Port Multiplexer Setting Register
UART (UART) Ch.0	0x4380	UA0CLK	UART Ch.0 Clock Control Register
	0x4382	UA0MOD	UART Ch.0 Mode Register
	0x4384	UA0BR	UART Ch.0 Baud-Rate Register
	0x4386	UA0CTL	UART Ch.0 Control Register
	0x4388	UA0TXD	UART Ch.0 Transmit Data Register
	0x438a	UA0RXD	UART Ch.0 Receive Data Register
	0x438c	UA0INTF	UART Ch.0 Status and Interrupt Flag Register
	0x438e	UA0INTE	UART Ch.0 Interrupt Enable Register
16-bit timer (T16) Ch.1	0x43a0	T16_1CLK	T16 Ch.1 Clock Control Register
	0x43a2	T16_1MOD	T16 Ch.1 Mode Register
	0x43a4	T16_1CTL	T16 Ch.1 Control Register
	0x43a6	T16_1TR	T16 Ch.1 Reload Data Register
	0x43a8	T16_1TC	T16 Ch.1 Counter Data Register
	0x43aa	T16_1INTF	T16 Ch.1 Interrupt Flag Register
	0x43ac	T16_1INTE	T16 Ch.1 Interrupt Enable Register
Synchronous serial interface (SPIA) Ch.0	0x43b0	SPI0MOD	SPIA Ch.0 Mode Register
	0x43b2	SPI0CTL	SPIA Ch.0 Control Register
	0x43b4	SPI0TXD	SPIA Ch.0 Transmit Data Register
	0x43b6	SPI0RXD	SPIA Ch.0 Receive Data Register
	0x43b8	SPI0INTF	SPIA Ch.0 Interrupt Flag Register
	0x43ba	SPI0INTE	SPIA Ch.0 Interrupt Enable Register
I²C (I2C) Ch.0	0x43c0	I2C0CLK	I2C Ch.0 Clock Control Register
	0x43c2	I2C0MOD	I2C Ch.0 Mode Register
	0x43c4	I2C0BR	I2C Ch.0 Baud-Rate Register
	0x43c8	I2C0OADR	I2C Ch.0 Own Address Register
	0x43ca	I2C0CTL	I2C Ch.0 Control Register
	0x43cc	I2C0TXD	I2C Ch.0 Transmit Data Register
	0x43ce	I2C0RXD	I2C Ch.0 Receive Data Register
	0x43d0	I2C0INTF	I2C Ch.0 Status and Interrupt Flag Register
	0x43d2	I2C0INTE	I2C Ch.0 Interrupt Enable Register
16-bit PWM timer (T16B) Ch.0	0x5000	T16B0CLK	T16B Ch.0 Clock Control Register
	0x5002	T16B0CTL	T16B Ch.0 Counter Control Register
	0x5004	T16B0MC	T16B Ch.0 Max Counter Data Register
	0x5006	T16B0TC	T16B Ch.0 Timer Counter Data Register
	0x5008	T16B0CS	T16B Ch.0 Counter Status Register
	0x500a	T16B0INTF	T16B Ch.0 Interrupt Flag Register

Peripheral circuit	Address	Register name	
16-bit PWM timer (T16B) Ch.0	0x500c	T16B0INTE	T16B Ch.0 Interrupt Enable Register
	0x5010	T16B0CCCTL0	T16B Ch.0 Compare/Capture 0 Control Register
	0x5012	T16B0CCR0	T16B Ch.0 Compare/Capture 0 Data Register
	0x5018	T16B0CCCTL1	T16B Ch.0 Compare/Capture 1 Control Register
	0x501a	T16B0CCR1	T16B Ch.0 Compare/Capture 1 Data Register
	0x5020	T16B0CCCTL2	T16B Ch.0 Compare/Capture 2 Control Register
	0x5022	T16B0CCR2	T16B Ch.0 Compare/Capture 2 Data Register
	0x5028	T16B0CCCTL3	T16B Ch.0 Compare/Capture 3 Control Register
	0x502a	T16B0CCR3	T16B Ch.0 Compare/Capture 3 Data Register
	0x5030	T16B0CCCTL4	T16B Ch.0 Compare/Capture 4 Control Register
	0x5032	T16B0CCR4	T16B Ch.0 Compare/Capture 4 Data Register
	0x5038	T16B0CCCTL5	T16B Ch.0 Compare/Capture 5 Control Register
	0x503a	T16B0CCR5	T16B Ch.0 Compare/Capture 5 Data Register
16-bit PWM timer (T16B) Ch.1	0x5040	T16B1CLK	T16B Ch.1 Clock Control Register
	0x5042	T16B1CTL	T16B Ch.1 Counter Control Register
	0x5044	T16B1MC	T16B Ch.1 Max Counter Data Register
	0x5046	T16B1TC	T16B Ch.1 Timer Counter Data Register
	0x5048	T16B1CS	T16B Ch.1 Counter Status Register
	0x504a	T16B1INTF	T16B Ch.1 Interrupt Flag Register
	0x504c	T16B1INTE	T16B Ch.1 Interrupt Enable Register
	0x5050	T16B1CCCTL0	T16B Ch.1 Compare/Capture 0 Control Register
	0x5052	T16B1CCR0	T16B Ch.1 Compare/Capture 0 Data Register
	0x5058	T16B1CCCTL1	T16B Ch.1 Compare/Capture 1 Control Register
	0x505a	T16B1CCR1	T16B Ch.1 Compare/Capture 1 Data Register
	0x5060	T16B1CCCTL2	T16B Ch.1 Compare/Capture 2 Control Register
	0x5062	T16B1CCR2	T16B Ch.1 Compare/Capture 2 Data Register
	0x5068	T16B1CCCTL3	T16B Ch.1 Compare/Capture 3 Control Register
	0x506a	T16B1CCR3	T16B Ch.1 Compare/Capture 3 Data Register
	0x5070	T16B1CCCTL4	T16B Ch.1 Compare/Capture 4 Control Register
	0x5072	T16B1CCR4	T16B Ch.1 Compare/Capture 4 Data Register
	0x5078	T16B1CCCTL5	T16B Ch.1 Compare/Capture 5 Control Register
	0x507a	T16B1CCR5	T16B Ch.1 Compare/Capture 5 Data Register
16-bit PWM timer (T16B) Ch.2	0x5080	T16B2CLK	T16B Ch.2 Clock Control Register
	0x5082	T16B2CTL	T16B Ch.2 Counter Control Register
	0x5084	T16B2MC	T16B Ch.2 Max Counter Data Register
	0x5086	T16B2TC	T16B Ch.2 Timer Counter Data Register
	0x5088	T16B2CS	T16B Ch.2 Counter Status Register
	0x508a	T16B2INTF	T16B Ch.2 Interrupt Flag Register
	0x508c	T16B2INTE	T16B Ch.2 Interrupt Enable Register
	0x5090	T16B2CCCTL0	T16B Ch.2 Compare/Capture 0 Control Register
	0x5092	T16B2CCR0	T16B Ch.2 Compare/Capture 0 Data Register
	0x5098	T16B2CCCTL1	T16B Ch.2 Compare/Capture 1 Control Register
	0x509a	T16B2CCR1	T16B Ch.2 Compare/Capture 1 Data Register
	0x50a0	T16B2CCCTL2	T16B Ch.2 Compare/Capture 2 Control Register
	0x50a2	T16B2CCR2	T16B Ch.2 Compare/Capture 2 Data Register
	0x50a8	T16B2CCCTL3	T16B Ch.2 Compare/Capture 3 Control Register
	0x50aa	T16B2CCR3	T16B Ch.2 Compare/Capture 3 Data Register
	0x50b0	T16B2CCCTL4	T16B Ch.2 Compare/Capture 4 Control Register
	0x50b2	T16B2CCR4	T16B Ch.2 Compare/Capture 4 Data Register
	0x50b8	T16B2CCCTL5	T16B Ch.2 Compare/Capture 5 Control Register
	0x50ba	T16B2CCR5	T16B Ch.2 Compare/Capture 5 Data Register
16-bit PWM timer (T16B) Ch.3	0x50c0	T16B3CLK	T16B Ch.3 Clock Control Register
	0x50c2	T16B3CTL	T16B Ch.3 Counter Control Register
	0x50c4	T16B3MC	T16B Ch.3 Max Counter Data Register
	0x50c6	T16B3TC	T16B Ch.3 Timer Counter Data Register
	0x50c8	T16B3CS	T16B Ch.3 Counter Status Register
	0x50ca	T16B3INTF	T16B Ch.3 Interrupt Flag Register
	0x50cc	T16B3INTE	T16B Ch.3 Interrupt Enable Register
	0x50d0	T16B3CCCTL0	T16B Ch.3 Compare/Capture 0 Control Register
	0x50d2	T16B3CCR0	T16B Ch.3 Compare/Capture 0 Data Register

Peripheral circuit	Address	Register name	
16-bit PWM timer (T16B) Ch.3	0x50d8	T16B3CCCTL1	T16B Ch.3 Compare/Capture 1 Control Register
	0x50da	T16B3CCR1	T16B Ch.3 Compare/Capture 1 Data Register
	0x50e0	T16B3CCCTL2	T16B Ch.3 Compare/Capture 2 Control Register
	0x50e2	T16B3CCR2	T16B Ch.3 Compare/Capture 2 Data Register
	0x50e8	T16B3CCCTL3	T16B Ch.3 Compare/Capture 3 Control Register
	0x50ea	T16B3CCR3	T16B Ch.3 Compare/Capture 3 Data Register
	0x50f0	T16B3CCCTL4	T16B Ch.3 Compare/Capture 4 Control Register
	0x50f2	T16B3CCR4	T16B Ch.3 Compare/Capture 4 Data Register
	0x50f8	T16B3CCCTL5	T16B Ch.3 Compare/Capture 5 Control Register
	0x50fa	T16B3CCR5	T16B Ch.3 Compare/Capture 5 Data Register
16-bit timer (T16) Ch.5	0x5140	T16_5CLK	T16 Ch.5 Clock Control Register
	0x5142	T16_5MOD	T16 Ch.5 Mode Register
	0x5144	T16_5CTL	T16 Ch.5 Control Register
	0x5146	T16_5TR	T16 Ch.5 Reload Data Register
	0x5148	T16_5TC	T16 Ch.5 Counter Data Register
	0x514a	T16_5INTF	T16 Ch.5 Interrupt Flag Register
	0x514c	T16_5INTE	T16 Ch.5 Interrupt Enable Register
UART (UART) Ch.1	0x5200	UA1CLK	UART Ch.1 Clock Control Register
	0x5202	UA1MOD	UART Ch.1 Mode Register
	0x5204	UA1BR	UART Ch.1 Baud-Rate Register
	0x5206	UA1CTL	UART Ch.1 Control Register
	0x5208	UA1TXD	UART Ch.1 Transmit Data Register
	0x520a	UA1RXD	UART Ch.1 Receive Data Register
	0x520c	UA1INTF	UART Ch.1 Status and Interrupt Flag Register
	0x520e	UA1INTE	UART Ch.1 Interrupt Enable Register
UART (UART) Ch.2	0x5220	UA2CLK	UART Ch.2 Clock Control Register
	0x5222	UA2MOD	UART Ch.2 Mode Register
	0x5224	UA2BR	UART Ch.2 Baud-Rate Register
	0x5226	UA2CTL	UART Ch.2 Control Register
	0x5228	UA2TXD	UART Ch.2 Transmit Data Register
	0x522a	UA2RXD	UART Ch.2 Receive Data Register
	0x522c	UA2INTF	UART Ch.2 Status and Interrupt Flag Register
	0x522e	UA2INTE	UART Ch.2 Interrupt Enable Register
16-bit timer (T16) Ch.2	0x5260	T16_2CLK	T16 Ch.2 Clock Control Register
	0x5262	T16_2MOD	T16 Ch.2 Mode Register
	0x5264	T16_2CTL	T16 Ch.2 Control Register
	0x5266	T16_2TR	T16 Ch.2 Reload Data Register
	0x5268	T16_2TC	T16 Ch.2 Counter Data Register
	0x526a	T16_2INTF	T16 Ch.2 Interrupt Flag Register
	0x526c	T16_2INTE	T16 Ch.2 Interrupt Enable Register
Synchronous serial interface (SPIA) Ch.1	0x5270	SPI1MOD	SPIA Ch.1 Mode Register
	0x5272	SPI1CTL	SPIA Ch.1 Control Register
	0x5274	SPI1TXD	SPIA Ch.1 Transmit Data Register
	0x5276	SPI1RXD	SPIA Ch.1 Receive Data Register
	0x5278	SPI1INTF	SPIA Ch.1 Interrupt Flag Register
	0x527a	SPI1INTE	SPIA Ch.1 Interrupt Enable Register
I²C (I2C) Ch.1	0x52c0	I2C1CLK	I2C Ch.1 Clock Control Register
	0x52c2	I2C1MOD	I2C Ch.1 Mode Register
	0x52c4	I2C1BR	I2C Ch.1 Baud-Rate Register
	0x52c8	I2C1OADR	I2C Ch.1 Own Address Register
	0x52ca	I2C1CTL	I2C Ch.1 Control Register
	0x52cc	I2C1TXD	I2C Ch.1 Transmit Data Register
	0x52ce	I2C1RXD	I2C Ch.1 Receive Data Register
	0x52d0	I2C1INTF	I2C Ch.1 Status and Interrupt Flag Register
	0x52d2	I2C1INTE	I2C Ch.1 Interrupt Enable Register
IR remote controller (REMC2)	0x5320	REMCLK	REMC2 Clock Control Register
	0x5322	REMDBCTL	REMC2 Data Bit Counter Control Register
	0x5324	REMDBCNT	REMC2 Data Bit Counter Register
	0x5326	REMAPLEN	REMC2 Data Bit Active Pulse Length Register
	0x5328	REMDBLEN	REMC2 Data Bit Length Register

Peripheral circuit	Address	Register name	
IR remote controller (REMC2)	0x532a	REMINTF	REMC2 Status and Interrupt Flag Register
	0x532c	REMINTE	REMC2 Interrupt Enable Register
	0x5330	REMCARR	REMC2 Carrier Waveform Register
	0x5332	REMCCTL	REMC2 Carrier Modulation Control Register
16-bit timer (T16) Ch.3	0x5480	T16_3CLK	T16 Ch.3 Clock Control Register
	0x5482	T16_3MOD	T16 Ch.3 Mode Register
	0x5484	T16_3CTL	T16 Ch.3 Control Register
	0x5486	T16_3TR	T16 Ch.3 Reload Data Register
	0x5488	T16_3TC	T16 Ch.3 Counter Data Register
	0x548a	T16_3INTF	T16 Ch.3 Interrupt Flag Register
	0x548c	T16_3INTE	T16 Ch.3 Interrupt Enable Register
10-bit A/D converter (ADC10A) Ch.0	0x54a2	ADC10_0CTL	ADC10A Ch.0 Control Register
	0x54a4	ADC10_0TRG	ADC10A Ch.0 Trigger/Analog Input Select Register
	0x54a6	ADC10_0CFG	ADC10A Ch.0 Configuration Register
	0x54a8	ADC10_0INTF	ADC10A Ch.0 Interrupt Flag Register
	0x54aa	ADC10_0INTE	ADC10A Ch.0 Interrupt Enable Register
	0x54ac	ADC10_0AD0D	ADC10A Ch.0 Result Register 0
	0x54ae	ADC10_0AD1D	ADC10A Ch.0 Result Register 1
	0x54b0	ADC10_0AD2D	ADC10A Ch.0 Result Register 2
	0x54b2	ADC10_0AD3D	ADC10A Ch.0 Result Register 3
	0x54b4	ADC10_0AD4D	ADC10A Ch.0 Result Register 4
	0x54b6	ADC10_0AD5D	ADC10A Ch.0 Result Register 5
	0x54b8	ADC10_0AD6D	ADC10A Ch.0 Result Register 6
	0x54ba	ADC10_0AD7D	ADC10A Ch.0 Result Register 7
16-bit timer (T16) Ch.4	0x54c0	T16_4CLK	T16 Ch.4 Clock Control Register
	0x54c2	T16_4MOD	T16 Ch.4 Mode Register
	0x54c4	T16_4CTL	T16 Ch.4 Control Register
	0x54c6	T16_4TR	T16 Ch.4 Reload Data Register
	0x54c8	T16_4TC	T16 Ch.4 Counter Data Register
	0x54ca	T16_4INTF	T16 Ch.4 Interrupt Flag Register
	0x54cc	T16_4INTE	T16 Ch.4 Interrupt Enable Register
10-bit A/D converter (ADC10A) Ch.1	0x54e2	ADC10_1CTL	ADC10A Ch.1 Control Register
	0x54e4	ADC10_1TRG	ADC10A Ch.1 Trigger/Analog Input Select Register
	0x54e6	ADC10_1CFG	ADC10A Ch.1 Configuration Register
	0x54e8	ADC10_1INTF	ADC10A Ch.1 Interrupt Flag Register
	0x54ea	ADC10_1INTE	ADC10A Ch.1 Interrupt Enable Register
	0x54ec	ADC10_1AD0D	ADC10A Ch.1 Result Register 0
	0x54ee	ADC10_1AD1D	ADC10A Ch.1 Result Register 1
	0x54f0	ADC10_1AD2D	ADC10A Ch.1 Result Register 2
	0x54f2	ADC10_1AD3D	ADC10A Ch.1 Result Register 3
	0x54f4	ADC10_1AD4D	ADC10A Ch.1 Result Register 4
	0x54f6	ADC10_1AD5D	ADC10A Ch.1 Result Register 5
	0x54f8	ADC10_1AD6D	ADC10A Ch.1 Result Register 6
	0x54fa	ADC10_1AD7D	ADC10A Ch.1 Result Register 7

4.5.1 System-Protect Function

The system-protect function protects control registers and bits from writings. They cannot be rewritten unless write protection is removed by writing 0x0096 to the MSCPROT.PROT[15:0] bits. This function is provided to prevent deadlock that may occur when a system-related register is altered by a runaway CPU. See "Control Registers" in each peripheral circuit to identify the registers and bits with write protection.

Note: Once write protection is removed using the MSCPROT.PROT[15:0] bits, write enabled status is maintained until write protection is applied again. After the registers/bits required have been altered, apply write protection.

4.6 Control Registers

MISC System Protect Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCPROT	15–0	PROT[15:0]	0x0000	H0	R/W	–

Bits 15–0 PROT[15:0]

These bits protect the control registers related to the system against writings.
0x0096 (R/W): Disable system protection
Other than 0x0096 (R/W): Enable system protection

While the system protection is enabled, any data will not be written to the affected control bits (bits with "WP" or "R/WP" appearing in the R/W column).

MISC IRAM Size Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCIRAMSZ	15–9	–	0x00	–	R	–
	8	(reserved)	0	H0	R/WP	Always set to 0.
	7–3	–	0x0c	–	R	–
	2–0	IRAMSZ[2:0]	0x6	H0	R/WP	

Bits 15–3 Reserved

Bits 2–0 IRAMSZ[2:0]

These bits set the internal RAM size that can be used.

Table 4.6.1 Internal RAM Size Selections

MSCIRAMSZ.IRAMSZ[2:0] bits	Internal RAM size
0x7–0x5	Reserved
0x6	16KB
0x5	12KB
0x4	8KB
0x3	4KB
0x2	2KB
0x1	1KB
0x0	512B

FLASHC Flash Read Cycle Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
FLASHCWAIT	15–8	–	0x00	–	R	–
	7	XBUSY	0	H0	R	
	6–2	–	0x00	–	R	
	1–0	RDWAIT[1:0]	0x1	H0	R/WP	

Bits 15–8 Reserved

Bit 7 XBUSY

This bit indicates whether the Flash memory can be accessed or not.
1 (R): Flash memory ready to access
0 (R): Flash access prohibited

The Flash memory can always be accessed during normal operation.

Bits 6–2 Reserved

Bits 1–0 RDWAIT[1:0]

These bits set the number of bus access cycles for reading from the Flash memory.

Table 4.6.2 Setting Number of Bus Access Cycles for Flash Read

FLASHCWAIT.RDWAIT[1:0] bits	Number of bus Access cycles	System clock frequency
0x3	4	16.8 MHz (max.)
0x2	3	16.8 MHz (max.)
0x1	2	12.6 MHz (max.)
0x0	1	6.3 MHz (max.)

Note: Be sure to set the FLASHCWAIT.RDWAIT[1:0] bits before the system clock is configured.

5 Interrupt Controller (ITC)

5.1 Overview

The features of the ITC are listed below.

- Honors interrupt requests from the peripheral circuits and outputs the interrupt request, interrupt level and vector number signals to the CPU.
- The interrupt level of each interrupt source is selectable from among eight levels.
- Priorities of the simultaneously generated interrupts are established from the interrupt level.
- Handles the simultaneously generated interrupts with the same interrupt level as smaller vector number has higher priority.

Figure 5.1.1 shows the configuration of the ITC.

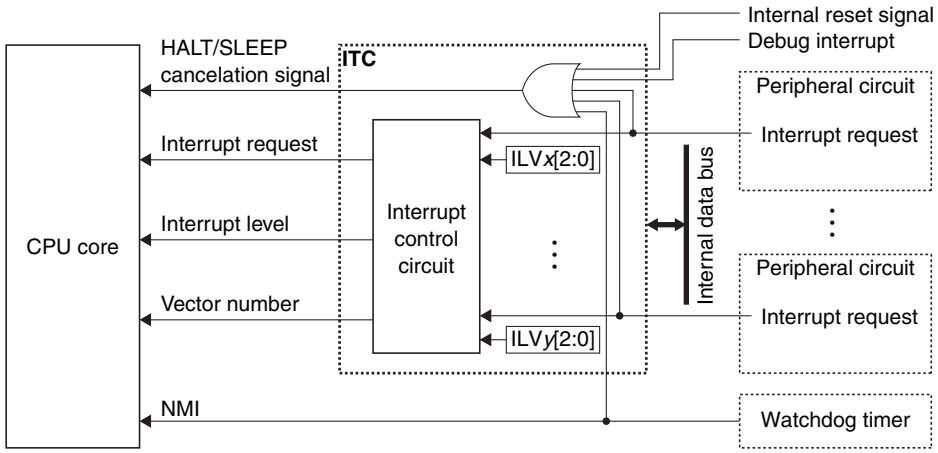


Figure 5.1.1 ITC Configuration

5.2 Vector Table

The vector table contains the vectors to the interrupt handler routines (handler routine start address) that will be read by the CPU to execute the handler when an interrupt occurs.
Table 5.2.1 shows the vector table.

Table 5.2.1 Vector Table

TTBR initial value = 0x8000

Vector number/ Software interrupt number	Vector address	Hardware interrupt name	Cause of hardware interrupt	Priority
0 (0x00)	TTBR + 0x00	Reset	• Low input to the #RESET pin • Power-on reset • Key reset • Watchdog timer overflow *2 • Supply voltage detector reset	1
1 (0x01)	TTBR + 0x04	Address misaligned interrupt	Memory access instruction	2
–	(0xfffc00)	Debugging interrupt	brk instruction, etc.	3
2 (0x02)	TTBR + 0x08	NMI	Watchdog timer overflow *2	4
3 (0x03)	TTBR + 0x0c	Reserved for C compiler	–	–

Vector number/ Software interrupt number	Vector address	Hardware interrupt name	Hardware interrupt flag	Priority
4 (0x04)	TTBR + 0x10	Supply voltage detector interrupt	Low power supply voltage detection	High *1 ↑
5 (0x05)	TTBR + 0x14	Port interrupt	Port input	
6 (0x06)	TTBR + 0x18	reserved	–	
7 (0x07)	TTBR + 0x1c	Clock generator interrupt	• IOSC oscillation stabilization waiting completion • OSC1 oscillation stabilization waiting completion • OSC3 oscillation stabilization waiting completion • OSC1 oscillation stop • IOSC oscillation auto-trimming completion	
8 (0x08)	TTBR + 0x20	Real-time clock interrupt	• 1-day, 1-hour, 1-minute, and 1-second • 1/32-second, 1/8-second, 1/4-second, and 1/2-second • Stopwatch 1 Hz, 10 Hz, and 100 Hz • Alarm • Theoretical regulation completion	
9 (0x09)	TTBR + 0x24	16-bit timer Ch.0 interrupt	Underflow	
10 (0x0a)	TTBR + 0x28	UART Ch.0 interrupt	• End of transmission • Framing error • Parity error • Overrun error • Receive buffer two bytes full • Receive buffer one byte full • Transmit buffer empty	
11 (0x0b)	TTBR + 0x2c	16-bit timer Ch.1 interrupt	Underflow	
12 (0x0c)	TTBR + 0x30	Synchronous serial interface Ch.0 interrupt	• End of transmission • Receive buffer full • Transmit buffer empty • Overrun error	
13 (0x0d)	TTBR + 0x34	I^2C Ch.0 interrupt	• End of data transfer • General call address reception • NACK reception • STOP condition • START condition • Error detection • Receive buffer full • Transmit buffer empty	
14 (0x0e)	TTBR + 0x38	16-bit PWM timer Ch.0 interrupt	• Capture overwrite • Compare/capture • Counter MAX • Counter zero	
15 (0x0f)	TTBR + 0x3c	16-bit PWM timer Ch.1 interrupt	• Capture overwrite • Compare/capture • Counter MAX • Counter zero	
16 (0x10)	TTBR + 0x40	16-bit PWM timer Ch.2 interrupt	• Capture overwrite • Compare/capture • Counter MAX • Counter zero	
17 (0x11)	TTBR + 0x44	16-bit PWM timer Ch.3 interrupt	• Capture overwrite • Compare/capture • Counter MAX • Counter zero	
18 (0x12)	TTBR + 0x48	16-bit timer Ch.5 interrupt	Underflow	
19 (0x13)	TTBR + 0x4c	UART Ch.1 interrupt	• End of transmission • Framing error • Parity error • Overrun error • Receive buffer two bytes full • Receive buffer one byte full • Transmit buffer empty	
20 (0x14)	TTBR + 0x50	16-bit timer Ch.2 interrupt	Underflow	
21 (0x15)	TTBR + 0x54	Synchronous serial interface Ch.1 interrupt	• End of transmission • Receive buffer full • Transmit buffer empty • Overrun error	

Vector number/ Software interrupt number	Vector address	Hardware interrupt name	Hardware interrupt flag	Priority
22 (0x16)	TTBR + 0x58	I^2C Ch.1 interrupt	• End of data transfer • General call address reception • NACK reception • STOP condition • START condition • Error detection • Receive buffer full • Transmit buffer empty	
23 (0x17)	TTBR + 0x5c	IR remote controller interrupt	• Compare AP • Compare DB	
24 (0x18)	TTBR + 0x60	16-bit timer Ch.3 interrupt	Underflow	
25 (0x19)	TTBR + 0x64	10-bit A/D converter Ch.0 interrupt	• Analog input signal *m* A/D conversion completion • Analog input signal *m* A/D conversion result overwrite error	
26 (0x1a)	TTBR + 0x68	16-bit timer Ch.4 interrupt	Underflow	
27 (0x1b)	TTBR + 0x6c	10-bit A/D converter Ch.1 interrupt	• Analog input signal *m* A/D conversion completion • Analog input signal *m* A/D conversion result overwrite error	
28 (0x1c)	TTBR + 0x70	UART Ch.2 interrupt	• End of transmission • Framing error • Parity error • Overrun error • Receive buffer two bytes full • Receive buffer one byte full • Transmit buffer empty	
29 (0x1d) : 31 (0x1f)	TTBR + 0x74 : TTBR + 0x7c	reserved : reserved	– : –	↓ Low *1

*1 When the same interrupt level is set
*2 Either reset or NMI can be selected as the watchdog timer interrupt with software.

5.2.1 Vector Table Base Address (TTBR)

The MSCTTBRL and MSCTTBRH registers are provided to set the base (start) address of the vector table in which interrupt vectors are programmed. "TTBR" described in Table 5.2.1 means the value set to these registers. After an initial reset, the MSCTTBRL and MSCTTBRH registers are set to address 0x8000. Therefore, even when the vector table location is changed, it is necessary that at least the reset vector be written to the above address. Bits 7 to 0 in the MSCTTBRL register are fixed at 0, so the vector table always begins from a 256-byte boundary address.

5.3 Initialization

The following shows an example of the initial setting procedure related to interrupts:

1. Execute the di instruction to set the CPU into interrupt disabled state.
2. If the vector table start address is different from the default address, set it to the MSCTTBRL and MSCTTBRH registers after removing system protection by writing 0x0096 to the MSCPROT.PROT[15:0] bits. Then, write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits to set system protection.
3. Set the interrupt enable bit of the peripheral circuit to 0 (interrupt disabled).
4. Set the interrupt level for the peripheral circuit using the ITCLV*x*.ILV*x*[2:0] bits in the ITC.
5. Configure the peripheral circuit and start its operation.
6. Clear the interrupt factor flag of the peripheral circuit.
7. Set the interrupt enable bit of the peripheral circuit to 1 (interrupt enabled).
8. Execute the ei instruction to set the CPU into interrupt enabled state.

5.4 Maskable Interrupt Control and Operations

5.4.1 Peripheral Circuit Interrupt Control

The peripheral circuit that generates interrupts includes an interrupt enable bit and an interrupt flag for each interrupt cause.

Interrupt flag: The flag is set to 1 when the interrupt cause occurs. The clear condition depends on the peripheral circuit.

Interrupt enable bit: By setting this bit to 1 (interrupt enabled), an interrupt request will be sent to the ITC when the interrupt flag is set to 1. When this bit is set to 0 (interrupt disabled), no interrupt request will be sent to the ITC even if the interrupt flag is set to 1. An interrupt request is also sent to the ITC if the status is changed to interrupt enabled when the interrupt flag is 1.

For specific information on causes of interrupts, interrupt flags, and interrupt enable bits, refer to the respective peripheral circuit descriptions.

Note: To prevent occurrence of unnecessary interrupts, the corresponding interrupt flag should be cleared before setting the interrupt enable bit to 1 (interrupt enabled) and before terminating the interrupt handler routine.

5.4.2 ITC Interrupt Request Processing

On receiving an interrupt signal from a peripheral circuit, the ITC sends an interrupt request, the interrupt level, and the vector number to the CPU. Vector numbers are determined by the ITC internal hardware for each interrupt cause, as shown in Table 5.2.1. The interrupt level is a value to configure the priority, and it can be set to between 0 (low) and 7 (high) using the ITCLV*x*.ILV*x*[2:0] bits provided for each interrupt source. The default ITC settings are level 0 for all maskable interrupts. Interrupt requests are not accepted by the CPU if the level is 0.

The ITC outputs the interrupt request with the highest priority to the CPU in accordance with the following conditions if interrupt requests are input to the ITC simultaneously from two or more peripheral circuits.

- The interrupt with the highest interrupt level takes precedence.
- If multiple interrupt requests are input with the same interrupt level, the interrupt with the lowest vector number takes precedence.

The other interrupts occurring at the same time are held until all interrupts with higher priority levels have been accepted by the CPU.
If an interrupt cause with higher priority occurs while the ITC is outputting an interrupt request signal to the CPU (before being accepted by the CPU), the ITC alters the vector number and interrupt level signals to the setting information on the more recent interrupt. The previously occurring interrupt is held. The held interrupt is canceled and no interrupt is generated if the interrupt flag in the peripheral circuit is cleared via software.

Note: Before changing the interrupt level, make sure that no interrupt of which the level is changed can be generated (the interrupt enable bit of the peripheral circuit is set to 0 or the peripheral circuit is deactivated).

5.4.3 Conditions to Accept Interrupt Requests by the CPU

The CPU accepts an interrupt request sent from the ITC when all of the following conditions are met:

- The IE (Interrupt Enable) bit of the PSR has been set to 1.
- The interrupt request that has occurred has a higher interrupt level than the value set in the IL[2:0] (Interrupt Level) bits of the PSR.
- No other interrupt request having higher priority, such as NMI, has occurred.

5.5 NMI

The watchdog timer embedded in this IC can generate a non-maskable interrupt (NMI). This interrupt takes precedence over other interrupts and is unconditionally accepted by the CPU.
For detailed information on generating NMI, refer to the "Watchdog Timer" chapter.

5.6 Software Interrupts

The CPU provides the "int *imm5*" and "intl *imm5*, *imm3*" instructions allowing the software to generate any interrupts. The operand *imm5* specifies a vector number (0–31) in the vector table. In addition to this, the intl instruction has the operand *imm3* to specify the interrupt level (0–7) to be set to the IL[2:0] bits in the PSR. The software interrupt cannot be disabled (non-maskable interrupt). The processor performs the same interrupt processing operation as that of the hardware interrupt.

5.7 Interrupt Processing by the CPU

The CPU samples interrupt requests for each cycle. On accepting an interrupt request, the CPU switches to interrupt processing immediately after execution of the current instruction has been completed.
Interrupt processing involves the following steps:

1. The PSR and current program counter (PC) values are saved to the stack.
2. The PSR IE bit is cleared to 0 (disabling subsequent maskable interrupts).
3. The PSR IL[2:0] bits are set to the received interrupt level. (The NMI does not affect the IL bits.)
4. The vector for the interrupt occurred is loaded to the PC to execute the interrupt handler routine.

When an interrupt is accepted, Step 2 prevents subsequent maskable interrupts. Setting the IE bit to 1 in the interrupt handler routine allows handling of multiple interrupts. In this case, since the IL[2:0] bits are changed by Step 3, only an interrupt with a higher level than that of the currently processed interrupt will be accepted.
Ending interrupt handler routines using the reti instruction returns the PSR to the state before the interrupt occurred. The program resumes processing following the instruction being executed at the time the interrupt occurred.

Note: When HALT or SLEEP mode is canceled, the CPU jumps to the interrupt handler routine after executing one instruction. To execute the interrupt handler routine immediately after HALT or SLEEP mode is canceled, place the nop instruction at just behind the halt/slp instruction.

5.8 Control Registers

MISC Vector Table Address Low Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCTTBRL	15–8	TTBR[15:8]	0x80	H0	R/WP	–
	7–0	TTBR[7:0]	0x00	H0	R	

Bits 15–0 TTBR[15:0]

These bits set the vector table base address (16 low-order bits).

MISC Vector Table Address High Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
MSCTTBRH	15–8	–	0x00	–	R	–
	7–0	TTBR[23:16]	0x00	H0	R/WP	

Bits 15–8 Reserved

Bits 7–0 TTBR[23:16]

These bits set the vector table base address (eight high-order bits).

ITC Interrupt Level Setup Register *x*

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ITCLV*x*	15–11	–	0x00	–	R	–
	10–8	ILVy_1[2:0]	0x0	H0	R/W	
	7–3	–	0x00	–	R	
	2–0	ILVy_0[2:0]	0x0	H0	R/W	

Bits 15–11 Reserved

Bits 7–3 Reserved

Bits 10–8 ILVy_1[2:0] ($y_1 = 2x + 1$)

Bits 2–0 ILVy_0[2:0] ($y_0 = 2x$)

These bits set the interrupt level of each interrupt.

Table 5.8.1 Interrupt Level and Priority Settings

ITCLV*x*.ILV*y*[2:0] bits	Interrupt level	Priority
0x7	7	High
0x6	6	↑
. . .	. . .	
0x1	1	↓
0x0	0	Low

The following shows the ITCLV*x* register configuration in this IC.

Table 5.8.2 List of ITCLV*x* Registers

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ITCLV0 (ITC Interrupt Level Setup Register 0)	15–11	–	0x00	–	R	–
	10–8	ILV1[2:0]	0x0	H0	R/W	Port interrupt (ILVPPORT)
	7–3	–	0x00	–	R	–
	2–0	ILV0[2:0]	0x0	H0	R/W	Supply voltage detector interrupt (ILVSVD)
ITCLV1 (ITC Interrupt Level Setup Register 1)	15–11	–	0x00	–	R	–
	10–8	ILV3[2:0]	0x0	H0	R/W	Clock generator interrupt (ILVCLG)
	7–3	–	0x00	–	R	–
	2–0	ILV2[2:0]	0x0	H0	R/W	(reserved)
ITCLV2 (ITC Interrupt Level Setup Register 2)	15–11	–	0x00	–	R	–
	10–8	ILV5[2:0]	0x0	H0	R/W	16-bit timer Ch.0 interrupt (ILVT16_0)
	7–3	–	0x00	–	R	–
	2–0	ILV4[2:0]	0x0	H0	R/W	Real-time clock interrupt (ILVRTCA_0)
ITCLV3 (ITC Interrupt Level Setup Register 3)	15–11	–	0x00	–	R	–
	10–8	ILV7[2:0]	0x0	H0	R/W	16-bit timer Ch.1 interrupt (ILVT16_1)
	7–3	–	0x00	–	R	–
	2–0	ILV6[2:0]	0x0	H0	R/W	UART Ch.0 interrupt (ILVUART_0)
ITCLV4 (ITC Interrupt Level Setup Register 4)	15–11	–	0x00	–	R	–
	10–8	ILV9[2:0]	0x0	H0	R/W	I²C Ch.0 interrupt (ILVI2C_0)
	7–3	–	0x00	–	R	–
	2–0	ILV8[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.0 interrupt (ILVSPIA_0)
ITCLV5 (ITC Interrupt Level Setup Register 5)	15–11	–	0x00	–	R	–
	10–8	ILV11[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.1 interrupt (ILVT16B_1)
	7–3	–	0x00	–	R	–
	2–0	ILV10[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.0 interrupt (ILVT16B_0)
ITCLV6 (ITC Interrupt Level Setup Register 6)	15–11	–	0x00	–	R	–
	10–8	ILV13[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.3 interrupt (ILVT16B_3)
	7–3	–	0x00	–	R	–
	2–0	ILV12[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.2 interrupt (ILVT16B_2)

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ITCLV7 (ITC Interrupt Level Setup Register 7)	15–11	–	0x00	–	R	–
	10–8	ILV15[2:0]	0x0	H0	R/W	UART Ch.1 interrupt (ILVUART_1)
	7–3	–	0x00	–	R	–
	2–0	ILV14[2:0]	0x0	H0	R/W	16-bit timer Ch.5 interrupt (ILVT16_5)
ITCLV8 (ITC Interrupt Level Setup Register 8)	15–11	–	0x00	–	R	–
	10–8	ILV17[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.1 interrupt (ILVSPIA_1)
	7–3	–	0x00	–	R	–
	2–0	ILV16[2:0]	0x0	H0	R/W	16-bit timer Ch.2 interrupt (ILVT16_2)
ITCLV9 (ITC Interrupt Level Setup Register 9)	15–11	–	0x00	–	R	–
	10–8	ILV19[2:0]	0x0	H0	R/W	IR remote controller interrupt (ILVREMC2_0)
	7–3	–	0x00	–	R	–
	2–0	ILV18[2:0]	0x0	H0	R/W	I^2C Ch.1 interrupt (ILVI2C_1)
ITCLV10 (ITC Interrupt Level Setup Register 10)	15–11	–	0x00	–	R	–
	10–8	ILV21[2:0]	0x0	H0	R/W	10-bit A/D converter Ch.0 interrupt (ILVADC10_0)
	7–3	–	0x00	–	R	–
	2–0	ILV20[2:0]	0x0	H0	R/W	16-bit timer Ch.3 interrupt (ILVT16_3)
ITCLV11 (ITC Interrupt Level Setup Register 11)	15–11	–	0x00	–	R	–
	10–8	ILV23[2:0]	0x0	H0	R/W	10-bit A/D converter Ch.1 interrupt (ILVADC10_1)
	7–3	–	0x00	–	R	–
	2–0	ILV22[2:0]	0x0	H0	R/W	16-bit timer Ch.4 interrupt (ILVT16_4)
ITCLV12 (ITC Interrupt Level Setup Register 12)	15–11	–	0x00	–	R	–
	10–8	ILV25[2:0]	0x0	H0	R/W	(reserved)
	7–3	–	0x00	–	R	–
	2–0	ILV24[2:0]	0x0	H0	R/W	UART Ch.2 interrupt (ILVUART_2)

6 I/O Ports (PPORT)

6.1 Overview

PPORT controls the I/O ports. The main features are outlined below.

- Allows port-by-port function configurations.
  - Each port can be configured with or without a pull-up or pull-down resistor.
  - Each port can be configured with or without a chattering filter.
  - Allows selection of the function (general-purpose I/O port (GPIO) function, up to four peripheral I/O functions) to be assigned to each port.
- Ports, except for those shared with debug pins, are initially placed into Hi-Z state.
  (No current passes through the pin during this Hi-Z state.)

Note: '*x*', which is used in the port names P*xy*, register names, and bit names, refers to a port group (*x* = 0, 1, 2, ··· , d) and '*y*' refers to a port number (*y* = 0, 1, 2, ··· , 7).

Figure 6.1.1 shows the configuration of PPORT.

Table 6.1.1 Port Configuration of S1C17589

Item	S1C17589	S1C17589
Port groups included	P0[7:0], P1[7:0], P2[7:0], P3[7:0], P4[7:0], P5[5:0], P6[7:0], P7[7:0], P8[7:0], P9[6:0], Pa[5:0], Pd[4:0]	
Ports with general-purpose I/O function (GPIO)	P0[7:0], P1[7:0], P2[7:0], P3[7:0], P4[7:0], P5[5:0], P6[7:0], P7[7:0], P8[7:0], P9[6:0], Pa[5:0], Pd[4:0] (Pd2: output only)	
Ports with interrupt function	P0[7:0], P1[7:0], P2[7:0], P3[7:0], P4[7:0], P5[5:0], P6[7:0], P7[7:0], P8[7:0], P9[6:0], Pa[5:0]	
Ports for debug function	Pd[2:0]	
Key-entry reset function	Supported (P0[3:0])	

Note: Depending on the package type, some ports are not available. Refer to "Pin Descriptions" in the "Overview" chapter for the ports that can be used.

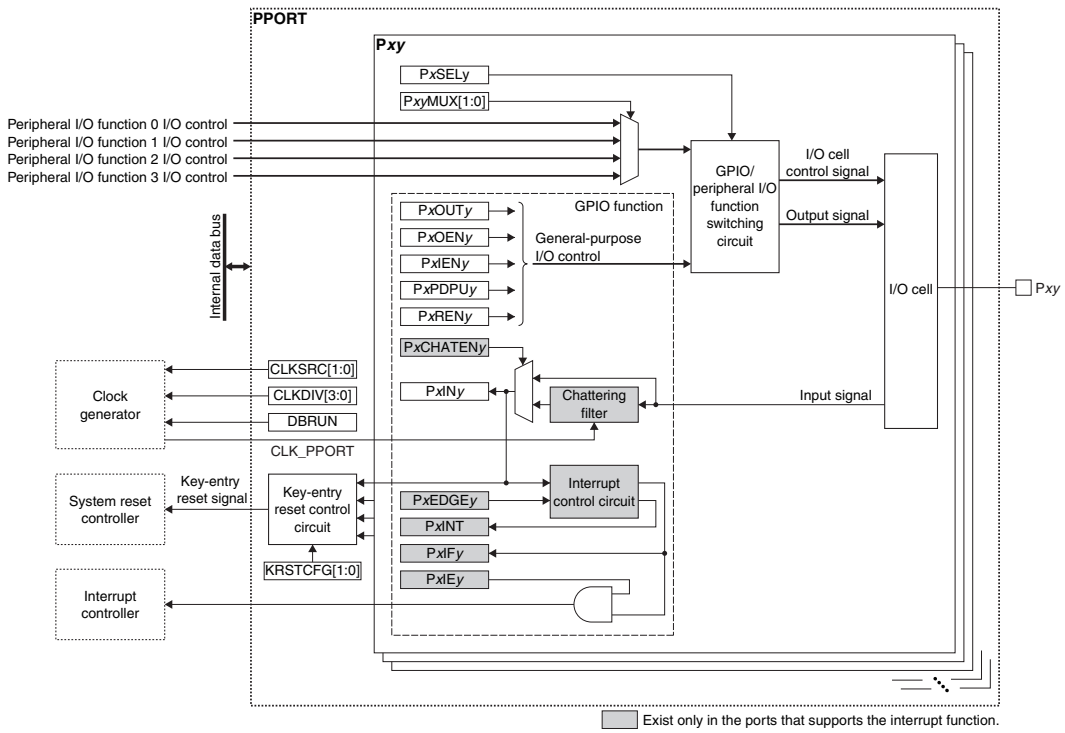


Figure 6.1.1 PPORT Configuration

6.2 I/O Cell Structure and Functions

Figure 6.2.1 shows the I/O cell Configuration.

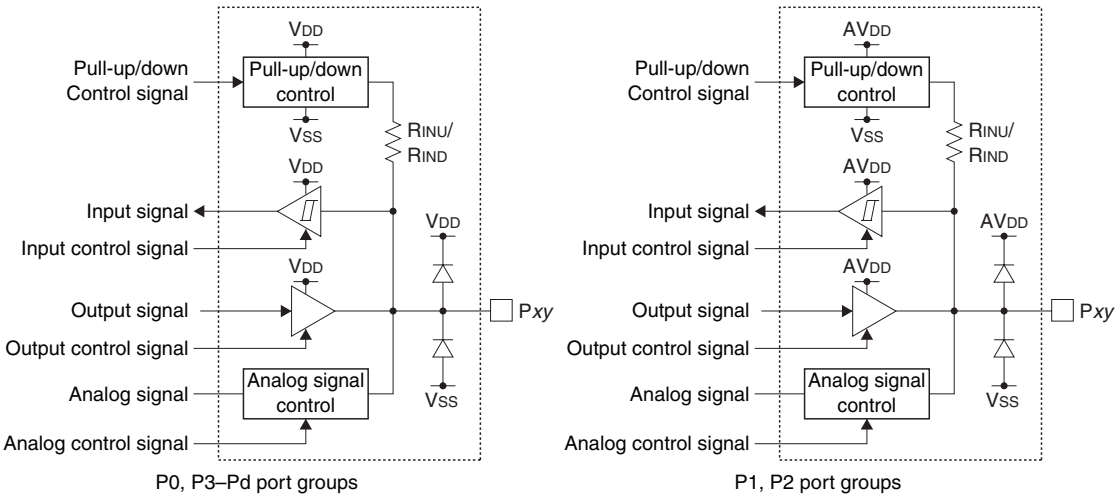


Figure 6.2.1 I/O Cell Configuration

6.2.1 Schmitt Input

The input functions are all configured with the Schmitt interface level. When a port is set to input disable status (P*x*IOEN.P*x*IEN*y* bit = 0), unnecessary current is not consumed if the P*xy* pin is placed into floating status.

6.2.2 Pull-Up/Pull-Down

The GPIO port has a pull-up/pull-down function. Either pull-up or pull-down may be selected for each port individually. This function may also be disabled for the port that does not require pulling up/down.
When the port level is switched from low to high through the pull-up resistor included in the I/O cell or from high to low through the pull-down resistor, a delay will occur in the waveform rising/falling edge depending on the time constant by the pull-up/pull-down resistance and the pin load capacitance. The rising/falling time is commonly determined by the following equation:

$$t_{PR} = -R_{INU} \times (C_{IN} + C_{BOARD}) \times \ln(1 - V_{T+}/V_{**}) \quad \text{(Eq. 6.1)}$$
$$t_{PF} = -R_{IND} \times (C_{IN} + C_{BOARD}) \times \ln(1 - V_{T-}/V_{**})$$

Where

- t_{PR}: Rising time (port level = low → high) [second]
- t_{PF}: Falling time (port level = high → low) [second]
- V_{**}: Power supply voltage V_{DD} [V] (P0, P3–Pd port groups)
  Analog power supply voltage AV_{DD} [V] (P1, P2 port groups)
- V_{T+}: High level Schmitt input threshold voltage [V]
- V_{T-}: Low level Schmitt input threshold voltage [V]
- R_{INU}/R_{IND}: Pull-up/pull-down resistance [Ω]
- C_{IN}: Pin capacitance [F]
- C_{BOARD}: Parasitic capacitance on the board [F]

6.2.3 CMOS Output and High Impedance State

The I/O cells except for analog output can output signals in the V_{DD} (AV_{DD}) and V_{SS} levels. Also the GPIO ports may be put into high-impedance (Hi-Z) state.

6.3 Clock Settings

6.3.1 PPORT Operating Clock

When using the chattering filter for entering external signals to PPORT, the PPORT operating clock CLK_PPORT must be supplied to PPORT from the clock generator.
The CLK_PPORT supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
3. Set the following PCLK register bits:
   - PCLK.CLKSRC[1:0] bits (Clock source selection)
   - PCLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)
4. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Settings in Step 3 determine the input sampling time of the chattering filter.

6.3.2 Clock Supply in SLEEP Mode

When using the chattering filter function during SLEEP mode, the PPORT operating clock CLK_PPORT must be configured so that it will keep suppling by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_PPORT clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_PPORT clock source is 1, the CLK_PPORT clock source is deactivated during SLEEP mode and it disables the chattering filter function regardless of the P*x*CHATEN.P*x*CHATEN*y* bit setting (chattering filter enabled/disabled).

6.3.3 Clock Supply in DEBUG Mode

The CLK_PPORT supply during DEBUG mode should be controlled using the PCLK.DBRUN bit.
The CLK_PPORT supply to PPORT is suspended when the CPU enters DEBUG mode if the PCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_PPORT supply resumes. The PPORT chattering filter stops operating when the CLK_PPORT supply is suspended. If the chattering filter is enabled in PPORT, the input port function is also deactivated. However, the control registers can be altered. If the PCLK.DBRUN bit = 1, the CLK_PPORT supply is not suspended and the chattering filter will keep operating in DEBUG mode.

6.4 Operations

6.4.1 Initialization

After a reset, the ports except for the debugging function are configured as shown below.

- Port input: Disabled
- Port output: Disabled
- Pull-up: Off
- Pull-down: Off
- Port pins: High impedance state
- Port function: Configured to GPIO

This status continues until the ports are configured via software. The debugging function ports are configured for debug signal input/output.

Initial settings when using a port for a peripheral I/O function

When using the P*xy* port for a peripheral I/O function, perform the following software initial settings:

1. Set the following P*x*IOEN register bits:
   - Set the P*x*IOEN.P*x*IEN*y* bit to 0. (Disable input)
   - Set the P*x*IOEN.P*x*OEN*y* bit to 0. (Disable output)
2. Set the P*x*MODSEL.P*x*SEL*y* bit to 0. (Disable peripheral I/O function)
3. Initialize the peripheral circuit that uses the pin.
4. Set the P*x*FNCSEL.P*xy*MUX[1:0] bits. (Select peripheral I/O function)
5. Set the P*x*MODSEL.P*x*SEL*y* bit to 1. (Enable peripheral I/O function)

For the list of the peripheral I/O functions that can be assigned to each port of this IC, refer to "Control Register and Port Function Configuration of this IC." For the specific information on the peripheral I/O functions, refer to the respective peripheral circuit chapter.

Initial settings when using a port as a general-purpose output port (only for the ports with GPIO function)

When using the P*xy* port pin as a general-purpose output pin, perform the following software initial settings:

1. Set the P*x*IOEN.P*x*OEN*y* bit to 1. (Enable output)
2. Set the P*x*MODSEL.P*x*SEL*y* bit to 0. (Enable GPIO function)

Initial settings when using a port as a general-purpose input port (only for the ports with GPIO function)

When using the P*xy* port pin as a general-purpose input pin, perform the following software initial settings:

1. Write 0 to the P*x*INTCTL.P*x*IE*y* bit. * (Disable interrupt)
2. When using the chattering filter, configure the PPORT operating clock (see "PPORT Operating Clock") and set the P*x*CHATEN.P*x*CHATEN*y* bit to 1. *

   When the chattering filter is not used, set the P*x*CHATEN.P*x*CHATEN*y* bit to 0 (supply of the PPORT operating clock is not required).
3. Configure the following P*x*RCTL register bits when pulling up/down the port using the internal pull-up or down resistor:
   - P*x*RCTL.P*x*PDPU*y* bit (Select pull-up or pull-down resistor)
   - Set the P*x*RCTL.P*x*REN*y* bit to 1. (Enable pull-up/down)

   Set the P*x*RCTL.P*x*REN*y* bit to 0 if the internal pull-up/down resistors are not used.
4. Set the P*x*MODSEL.P*x*SEL*y* bit to 0. (Enable GPIO function)
5. Configure the following bits when using the port input interrupt: *
   - Write 1 to the P*x*INTF.P*x*IF*y* bit. (Clear interrupt flag)
   - P*x*INTCTL.P*x*EDGE*y* bit (Select interrupt edge (input rising edge/falling edge))
   - Set the P*x*INTCTL.P*x*IE*y* bit to 1. (Enable interrupt)
6. Set the following P*x*IOEN register bits:
   - Set the P*x*IOEN.P*x*OEN*y* bit to 0. (Disable output)
   - Set the P*x*IOEN.P*x*IEN*y* bit to 1. (Enable input)

∗ Steps 1 and 5 are required for the ports with an interrupt function. Step 2 is required for the ports with a chattering filter function.

Table 6.4.1.1 lists the port status according to the combination of data input/output control and pull-up/down control.

Table 6.4.1.1 GPIO Port Control List

PxIOEN. PxIENy bit	PxIOEN. PxOENy bit	PxRCTL. PxRENy bit	PxRCTL. PxPDPUy bit	Input	Output	Pull-up/pull-down condition
0	0	0	×	Disabled		Off (Hi-Z) *1
0	0	1	0	Disabled		Pulled down
0	0	1	1	Disabled		Pulled up
1	0	0	×	Enabled	Disabled	Off (Hi-Z) *2
1	0	1	0	Enabled	Disabled	Pulled down
1	0	1	1	Enabled	Disabled	Pulled up
0	1	0	×	Disabled	Enabled	Off
0	1	1	0	Disabled	Enabled	Off
0	1	1	1	Disabled	Enabled	Off
1	1	1	0	Enabled	Enabled	Off
1	1	1	1	Enabled	Enabled	Off

*1: Initial status. Current does not flow if the pin is placed into floating status.
*2: Use of the pull-up or pull-down function is recommended, as undesired current will flow if the port input is set to floating status.

Note: If the PxMODSEL.PxSELy bit for the port without a GPIO function is set to 0, the port goes into initial status (refer to "Initial Settings"). The GPIO control bits are configured to a read-only bit always read out as 0.

6.4.2 Port Input/Output Control

Peripheral I/O function control

The port for which a peripheral I/O function is selected is controlled by the peripheral circuit. For more information, refer to the respective peripheral circuit chapter.

Setting output data to a GPIO port

Write data (1 = high output, 0 = low output) to be output from the P*xy* pin to the PxDAT.P*x*OUT*y* bit.

Reading input data from a GPIO port

The data (1 = high input, 0 = low input) input from the P*xy* pin can be read out from the PxDAT.P*x*IN*y* bit.

Note: The PxDAT.P*x*IN*y* bit retains the input port status at 1 clock before being read from the CPU.

Chattering filter function

Some ports have a chattering filter function and it can be controlled in each port. This function is enabled by setting the PxCHATEN.P*x*CHATEN*y* bit to 1. The input sampling time to remove chattering is determined by the CLK_PPORT frequency configured using the PCLK register in common to all ports. The chattering filter removes pulses with a shorter width than the input sampling time.

$$\text{Input sampling time} = \frac{2 \text{ to } 3}{\text{CLK\_PPORT frequency [Hz]}} \text{ [second]} \qquad \text{(Eq.6.2)}$$

Make sure the P*xy* port interrupt is disabled before altering the PCLK register and PxCHATEN.P*x*CHATEN*y* bit settings. A P*xy* port interrupt may erroneously occur if these settings are altered in an interrupt enabled status. Furthermore, enable the interrupt after a lapse of four or more CLK_PPORT cycles from enabling the chattering filter function.
If the clock generator is configured so that it will supply CLK_PPORT to PPORT in SLEEP mode, the chattering filter of the port will function even in SLEEP mode. If CLK_PPORT is configured to stop in SLEEP mode, PPORT inactivates the chattering filter during SLEEP mode to input pin status transitions directly to itself.

Key-entry reset function

This function issues a reset request when low-level pulses are input to all the specified ports simultaneously. Make the following settings when using this function:

1. Configure the ports to be used for key-entry reset as general-purpose input ports (refer to "Initial settings when using a port as a general-purpose input port (only for the ports with GPIO function)").
2. Configure the input pin combination for key-entry reset using the PCLK.KRSTCFG[1:0] bits.

Note: When enabling the key-entry reset function, be sure to configure the port pins to be used for it as general-purpose input pins before setting the PCLK.KRSTCFG[1:0] bits.

PPORT issues a reset request immediately after all the input pins specified by the PCLK.KRSTCFG[1:0] are set to a low level if the chattering filter function is disabled (initial status). To issue a reset request only when low-level signals longer than the time configured are input, enable the chattering filter function for all the ports used for key-entry reset.
The pins configured for key-entry reset can also be used as general-purpose input pins.

6.5 Interrupts

When the GPIO function is selected for the port with an interrupt function, the port input interrupt function can be used.

Table 6.5.1 Port Input Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Port input interrupt	P*x*INTF.P*x*IF*y*	Rising or falling edge of the input signal	Writing 1
	PINTFGRP.P*x*INT	Setting an interrupt flag in the port group	Clearing P*x*INTF.P*x*IF*y*

Interrupt edge selection

Port input interrupts will occur at the falling edge of the input signal when setting the P*x*INTCTL.P*x*EDGE*y* bit to 1, or the rising edge when setting to 0.

Interrupt enable

PPORT provides interrupt enable bits (P*x*INTCTL.P*x*IE*y* bit) corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

Interrupt check in port group unit

When interrupts are enabled in two or more port groups, check the PINTFGRP.P*x*INT bit in the interrupt handler first. It helps minimize the handler codes for finding the port that has generated an interrupt. If this bit is set to 1, an interrupt has occurred in the port group. Next, check the P*x*INTF.P*x*IF*y* bit set to 1 in the port group to determine the port that has generated an interrupt. Clearing the P*x*INTF.P*x*IF*y* bit also clears the PINTFGRP.P*x*INT bit. If the port is set to interrupt disabled status by the P*x*INTCTL.P*x*IE*y* bit, the PINTFGRP.P*x*INT bit will not be set even if the P*x*INTF.P*x*IF*y* bit is set to 1.

6.6 Control Registers

This section describes the same control registers of all port groups as a single register. For the register and bit configurations in each port group and their initial values, refer to "Control Register and Port Function Configuration of this IC."

P*x* Port Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*DAT	15–8	P*x*OUT[7:0]	0x00	H0	R/W	–
	7–0	P*x*IN[7:0]	0x00	H0	R	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.
∗3: The initial value may be changed by the port.

Bits 15–8 P*x*OUT[7:0]

These bits are used to set data to be output from the GPIO port pins.
1 (R/W): Output high level from the port pin
0 (R/W): Output low level from the port pin

When output is enabled (P*x*IOEN.P*x*OEN*y* bit = 1), the port pin outputs the data set here. Although data can be written when output is disabled (P*x*IOEN.P*x*OEN*y* bit = 0), it does not affect the pin status.
These bits do not affect the outputs when the port is used as a peripheral I/O function.

Bits 7–0 P*x*IN[7:0]

The GPIO port pin status can be read out from these bits.
1 (R): Port pin = High level
0 (R): Port pin = Low level

The port pin status can be read out when input is enabled (P*x*IOEN.P*x*IEN*y* bit = 1). When input is disabled (P*x*IOEN.P*x*IEN*y* bit = 0), these bits are always read as 0.
When the port is used for a peripheral I/O function, the input value cannot be read out from these bits.

P*x* Port Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PxIOEN	15–8	PxIEN[7:0]	0x00	H0	R/W	–
	7–0	PxOEN[7:0]	0x00	H0	R/W	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 P*x*IEN[7:0]

These bits enable/disable the GPIO port input.
1 (R/W): Enable (The port pin status is input.)
0 (R/W): Disable (Input data is fixed at 0.)

When both data output and data input are enabled, the pin output status controlled by this IC can be read.
These bits do not affect the input control when the port is used as a peripheral I/O function.

Bits 7–0 P*x*OEN[7:0]

These bits enable/disable the GPIO port output.
1 (R/W): Enable (Data is output from the port pin.)
0 (R/W): Disable (The port is placed into Hi-Z.)

These bits do not affect the output control when the port is used as a peripheral I/O function.

P*x* Port Pull-up/down Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PxRCTL	15–8	PxPDPU[7:0]	0x00	H0	R/W	–
	7–0	PxREN[7:0]	0x00	H0	R/W	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 P*x*PDPU[7:0]

These bits select either the pull-up resistor or the pull-down resistor when using a resistor built into the port.
1 (R/W): Pull-up resistor
0 (R/W): Pull-down resistor

The selected pull-up/down resistor is enabled when the P*x*RCTL.P*x*REN*y* bit = 1.

Bits 7–0 P*x*REN[7:0]

These bits enable/disable the port pull-up/down control.
1 (R/W): Enable (The built-in pull-up/down resistor is used.)
0 (R/W): Disable (No pull-up/down control is performed.)

Enabling this function pulls up or down the port when output is disabled (P*x*IOEN.P*x*OEN*y* bit = 0). When output is enabled (P*x*IOEN.P*x*OEN*y* bit = 1), the P*x*RCTL.P*x*REN*y* bit setting is ineffective regardless of how the P*x*IOEN.P*x*IEN*y* bit is set and the port is not pulled up/down.
These bits do not affect the pull-up/down control when the port is used as a peripheral I/O function.

Px Port Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PxINTF	15–8	–	0x00	–	R	–
	7–0	PxIF[7:0]	0x00	H0	R/W	Cleared by writing 1.

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 Reserved

Bits 7–0 PxIF[7:0]

These bits indicate the port input interrupt cause occurrence status.

1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

Px Port Interrupt Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PxINTCTL	15–8	PxEDGE[7:0]	0x00	H0	R/W	–
	7–0	PxIE[7:0]	0x00	H0	R/W	

∗1: This register is effective when the GPIO function is selected.
∗2: The bit configuration differs depending on the port group.

Bits 15–8 PxEDGE[7:0]

These bits select the input signal edge to generate a port input interrupt.

1 (R/W): An interrupt will occur at a falling edge.
0 (R/W): An interrupt will occur at a rising edge.

Bits 7–0 PxIE[7:0]

These bits enable port input interrupts.

1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

Note: To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

Px Port Chattering Filter Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PxCHATEN	15–8	–	0x00	–	R	–
	7–0	PxCHATEN[7:0]	0x00	H0	R/W	

∗1: The bit configuration differs depending on the port group.

Bits 15–8 Reserved

Bits 7–0 PxCHATEN[7:0]

These bits enable/disable the chattering filter function.

1 (R/W): Enable (The chattering filter is used.)
0 (R/W): Disable (The chattering filter is bypassed.)

Px Port Mode Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PxMODSEL	15–8	–	0x00	–	R	–
	7–0	PxSEL[7:0]	0x00	H0	R/W	

∗1: The bit configuration differs depending on the port group.
∗2: The initial value may be changed by the port.

Bits 15–8 Reserved

Bits 7–0 P*x*SEL[7:0]

These bits select whether each port is used for the GPIO function or a peripheral I/O function.
1 (R/W): Use peripheral I/O function
0 (R/W): Use GPIO function

P*x* Port Function Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*FNCSEL	15–14	P*x*7MUX[1:0]	0x0	H0	R/W	–
	13–12	P*x*6MUX[1:0]	0x0	H0	R/W	
	11–10	P*x*5MUX[1:0]	0x0	H0	R/W	
	9–8	P*x*4MUX[1:0]	0x0	H0	R/W	
	7–6	P*x*3MUX[1:0]	0x0	H0	R/W	
	5–4	P*x*2MUX[1:0]	0x0	H0	R/W	
	3–2	P*x*1MUX[1:0]	0x0	H0	R/W	
	1–0	P*x*0MUX[1:0]	0x0	H0	R/W	

∗1: The bit configuration differs depending on the port group.
∗2: The initial value may be changed by the port.

Bits 15–14 P*x*7MUX[1:0]

: :

Bits 1–0 P*x*0MUX[1:0]

These bits select the peripheral I/O function to be assigned to each port pin.

Table 6.6.1 Selecting Peripheral I/O Function

P*x*FNCSEL.P*xy*MUX[1:0] bits	Peripheral I/O function
0x3	Function 3
0x2	Function 2
0x1	Function 1
0x0	Function 0

This selection takes effect when the P*x*MODSEL.P*x*SEL*y* bit = 1.

P Port Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PCLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/WP	
	7–4	CLKDIV[3:0]	0x0	H0	R/WP	
	3–2	KRSTCFG[1:0]	0x0	H0	R/WP	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the PPORT operating clock is supplied in DEBUG mode or not.
1 (R/WP): Clock supplied in DEBUG mode
0 (R/WP): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the PPORT operating clock (chattering filter clock).

Bits 3–2 KRSTCFG[1:0]

These bits configure the key-entry reset function.

Table 6.6.2 Key-Entry Reset Function Settings

PCLK.KRSTCFG[1:0] bits	key-entry reset
0x3	Reset when P0[3:0] inputs = all low
0x2	Reset when P0[2:0] inputs = all low
0x1	Reset when P0[1:0] inputs = all low
0x0	Disable

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of PPORT (chattering filter).
The PPORT operating clock should be configured by selecting the clock source using the PCLK.CLKSRC[1:0] bits and the clock division ratio using the PCLK.CLKDIV[3:0] bits as shown in Table 6.6.3. These settings determine the input sampling time of the chattering filter.

Table 6.6.3 Clock Source and Division Ratio Settings

PCLK.CLKDIV[3:0] bits	PCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0xf	1/32,768			1/1
0xe	1/16,384			
0xd	1/8,192			
0xc	1/4,096			
0xb	1/2,048			
0xa	1/1,024			
0x9	1/512			
0x8	1/256			
0x7	1/128			
0x6	1/64			
0x5	1/32			
0x4	1/16			
0x3	1/8			
0x2	1/4			
0x1	1/2			
0x0	1/1			

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

P Port Interrupt Flag Group Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PINTFGRP	15–13	–	0x0	–	R	–
	12	PcINT	0	H0	R	
	11	PbINT	0	H0	R	
	10	PaINT	0	H0	R	
	9	P9INT	0	H0	R	
	8	P8INT	0	H0	R	
	7	P7INT	0	H0	R	
	6	P6INT	0	H0	R	
	5	P5INT	0	H0	R	
	4	P4INT	0	H0	R	
	3	P3INT	0	H0	R	
	2	P2INT	0	H0	R	
	1	P1INT	0	H0	R	
	0	P0INT	0	H0	R	

∗1: Only the bits corresponding to the port groups that support interrupts are provided.

Bits 15–13 Reserved

Bits 12–0 PxINT

These bits indicate that P*x* port group includes a port that has generated an interrupt.

1 (R): A port generated an interrupt

0 (R): No port generated an interrupt

The PINTFGRP.P*x*INT bit is cleared when the interrupt flag for the port that has generated an interrupt is cleared.

6.7 Control Register and Port Function Configuration of this IC

This section shows the PPORT control register/bit configuration in this IC and the list of peripheral I/O functions selectable for each port.

6.7.1 P0 Port Group

The P0 port group supports the GPIO and interrupt functions.

Table 6.7.1.1 Control Registers for P0 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P0DAT (P0 Port Data Register)	15–8	P0OUT[7:0]	0x00	H0	R/W	–
	7–0	P0IN[7:0]	0x00	H0	R	
P0IOEN (P0 Port Enable Register)	15–8	P0IEN[7:0]	0x00	H0	R/W	–
	7–0	P0OEN[7:0]	0x00	H0	R/W	
P0RCTL (P0 Port Pull-up/ down Control Register)	15–8	P0PDPU[7:0]	0x00	H0	R/W	–
	7–0	P0REN[7:0]	0x00	H0	R/W	
P0INTF (P0 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P0IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P0INTCTL (P0 Port Interrupt Control Register)	15–8	P0EDGE[7:0]	0x00	H0	R/W	–
	7–0	P0IE[7:0]	0x00	H0	R/W	
P0CHATEN (P0 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P0CHATEN[7:0]	0x00	H0	R/W	
P0MODSEL (P0 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P0SEL[7:0]	0x00	H0	R/W	
P0FNCSEL (P0 Port Function Select Register)	15–14	P07MUX[1:0]	0x0	H0	R/W	–
	13–12	P06MUX[1:0]	0x0	H0	R/W	
	11–10	P05MUX[1:0]	0x0	H0	R/W	
	9–8	P04MUX[1:0]	0x0	H0	R/W	
	7–6	P03MUX[1:0]	0x0	H0	R/W	
	5–4	P02MUX[1:0]	0x0	H0	R/W	
	3–2	P01MUX[1:0]	0x0	H0	R/W	
	1–0	P00MUX[1:0]	0x0	H0	R/W	

Table 6.7.1.2 P0 Port Group Function Assignment

Port name	P0SEL*y* = 0	P0SEL*y* = 1							
	GPIO	P0*y*MUX = 0x0 (Function 0)		P0*y*MUX = 0x1 (Function 1)		P0*y*MUX = 0x2 (Function 2)		P0*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P00	P00	–	–	UPMUX	∗1	–	–	–	–
P01	P01	–	–	UPMUX	∗1	–	–	–	–
P02	P02	–	–	UPMUX	∗1	–	–	–	–
P03	P03	–	–	UPMUX	∗1	–	–	–	–
P04	P04	–	–	UPMUX	∗1	–	–	–	–
P05	P05	–	–	UPMUX	∗1	–	–	–	–
P06	P06	–	–	UPMUX	∗1	–	–	–	–
P07	P07	–	–	UPMUX	∗1	–	–	–	–

∗1: Refer to the “Universal Port Multiplexer” chapter.

6.7.2 P1 Port Group

The P1 port group supports the GPIO and interrupt functions.

Table 6.7.2.1 Control Registers for P1 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P1DAT (P1 Port Data Register)	15–8	P1OUT[7:0]	0x00	H0	R/W	–
	7–0	P1IN[7:0]	0x00	H0	R	
P1IOEN (P1 Port Enable Register)	15–8	P1IEN[7:0]	0x00	H0	R/W	–
	7–0	P1OEN[7:0]	0x00	H0	R/W	
P1RCTL (P1 Port Pull-up/down Control Register)	15–8	P1PDPU[7:0]	0x00	H0	R/W	–
	7–0	P1REN[7:0]	0x00	H0	R/W	
P1INTF (P1 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P1IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P1INTCTL (P1 Port Interrupt Control Register)	15–8	P1EDGE[7:0]	0x00	H0	R/W	–
	7–0	P1IE[7:0]	0x00	H0	R/W	
P1CHATEN (P1 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P1CHATEN[7:0]	0x00	H0	R/W	
P1MODSEL (P1 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P1SEL[7:0]	0x00	H0	R/W	
P1FNCSEL (P1 Port Function Select Register)	15–14	P17MUX[1:0]	0x2	H0	R	–
	13–12	P16MUX[1:0]	0x2	H0	R	
	11–10	P15MUX[1:0]	0x2	H0	R	
	9–8	P14MUX[1:0]	0x2	H0	R	
	7–6	P13MUX[1:0]	0x2	H0	R	
	5–4	P12MUX[1:0]	0x2	H0	R	
	3–2	P11MUX[1:0]	0x2	H0	R	
	1–0	P10MUX[1:0]	0x2	H0	R	

Table 6.7.2.2 P1 Port Group Function Assignment

Port name	P1SEL*y* = 0	P1SEL*y* = 1							
	GPIO	P1*y*MUX = 0x0 (Function 0)		P1*y*MUX = 0x1 (Function 1)		P1*y*MUX = 0x2 (Function 2)		P1*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P10	P10	–	–	–	–	ADC10A	ADIN00	–	–
P11	P11	–	–	–	–	ADC10A	ADIN01	–	–
P12	P12	–	–	–	–	ADC10A	ADIN02	–	–
P13	P13	–	–	–	–	ADC10A	ADIN03	–	–
P14	P14	–	–	–	–	ADC10A	ADIN04	–	–
P15	P15	–	–	–	–	ADC10A	ADIN05	–	–
P16	P16	–	–	–	–	ADC10A	ADIN06	–	–
P17	P17	–	–	–	–	ADC10A	ADIN07	–	–

6.7.3 P2 Port Group

The P2 port group supports the GPIO and interrupt functions.

Table 6.7.3.1 Control Registers for P2 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P2DAT (P2 Port Data Register)	15–8	P2OUT[7:0]	0x00	H0	R/W	–
	7–0	P2IN[7:0]	0x00	H0	R	
P2IOEN (P2 Port Enable Register)	15–8	P2IEN[7:0]	0x00	H0	R/W	–
	7–0	P2OEN[7:0]	0x00	H0	R/W	
P2RCTL (P2 Port Pull-up/down Control Register)	15–8	P2PDPU[7:0]	0x00	H0	R/W	–
	7–0	P2REN[7:0]	0x00	H0	R/W	
P2INTF (P2 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P2IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P2INTCTL (P2 Port Interrupt Control Register)	15–8	P2EDGE[7:0]	0x00	H0	R/W	–
	7–0	P2IE[7:0]	0x00	H0	R/W	
P2CHATEN (P2 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P2CHATEN[7:0]	0x00	H0	R/W	
P2MODSEL (P2 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P2SEL[7:0]	0x00	H0	R/W	
P2FNCSEL (P2 Port Function Select Register)	15–14	P27MUX[1:0]	0x2	H0	R	–
	13–12	P26MUX[1:0]	0x2	H0	R	
	11–10	P25MUX[1:0]	0x2	H0	R	
	9–8	P24MUX[1:0]	0x2	H0	R	
	7–6	P23MUX[1:0]	0x2	H0	R	
	5–4	P22MUX[1:0]	0x2	H0	R	
	3–2	P21MUX[1:0]	0x2	H0	R	
	1–0	P20MUX[1:0]	0x2	H0	R	

Table 6.7.3.2 P2 Port Group Function Assignment

Port name	P2SEL*y* = 0	P2SEL*y* = 1							
	GPIO	P2*y*MUX = 0x0 (Function 0)		P2*y*MUX = 0x1 (Function 1)		P2*y*MUX = 0x2 (Function 2)		P2*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P20	P20	–	–	–	–	ADC10A	ADIN10	–	–
P21	P21	–	–	–	–	ADC10A	ADIN11	–	–
P22	P22	–	–	–	–	ADC10A	ADIN12	–	–
P23	P23	–	–	–	–	ADC10A	ADIN13	–	–
P24	P24	–	–	–	–	ADC10A	ADIN14	–	–
P25	P25	–	–	–	–	ADC10A	ADIN15	–	–
P26	P26	–	–	–	–	ADC10A	ADIN16	–	–
P27	P27	–	–	–	–	ADC10A	ADIN17	–	–

6.7.4 P3 Port Group

The P3 port group supports the GPIO and interrupt functions.

Table 6.7.4.1 Control Registers for P3 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P3DAT (P3 Port Data Register)	15–8	P3OUT[7:0]	0x00	H0	R/W	–
	7–0	P3IN[7:0]	0x00	H0	R	
P3IOEN (P3 Port Enable Register)	15–8	P3IEN[7:0]	0x00	H0	R/W	–
	7–0	P3OEN[7:0]	0x00	H0	R/W	
P3RCTL (P3 Port Pull-up/down Control Register)	15–8	P3PDPU[7:0]	0x00	H0	R/W	–
	7–0	P3REN[7:0]	0x00	H0	R/W	
P3INTF (P3 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P3IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P3INTCTL (P3 Port Interrupt Control Register)	15–8	P3EDGE[7:0]	0x00	H0	R/W	–
	7–0	P3IE[7:0]	0x00	H0	R/W	
P3CHATEN (P3 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P3CHATEN[7:0]	0x00	H0	R/W	
P3MODSEL (P3 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P3SEL[7:0]	0x00	H0	R/W	
P3FNCSEL (P3 Port Function Select Register)	15–14	P37MUX[1:0]	0x0	H0	R/W	–
	13–12	P36MUX[1:0]	0x0	H0	R/W	
	11–10	P35MUX[1:0]	0x0	H0	R/W	
	9–8	P34MUX[1:0]	0x0	H0	R/W	
	7–6	P33MUX[1:0]	0x0	H0	R/W	
	5–4	P32MUX[1:0]	0x0	H0	R/W	
	3–2	P31MUX[1:0]	0x0	H0	R/W	
	1–0	P30MUX[1:0]	0x0	H0	R/W	

Table 6.7.4.2 P3 Port Group Function Assignment

Port name	P3SEL*y* = 0	P3SEL*y* = 1							
	GPIO	P3*y*MUX = 0x0 (Function 0)		P3*y*MUX = 0x1 (Function 1)		P3*y*MUX = 0x2 (Function 2)		P3*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P30	P30	ADC10A	#ADTRG0	UPMUX	∗1	–	–	–	–
P31	P31	ADC10A	#ADTRG1	UPMUX	∗1	–	–	–	–
P32	P32	T16B Ch.0	EXCL00	UPMUX	∗1	–	–	–	–
P33	P33	T16B Ch.1	EXCL10	UPMUX	∗1	–	–	–	–
P34	P34	REMC2	REMO	UPMUX	∗1	–	–	–	–
P35	P35	CLG	FOUT	UPMUX	∗1	–	–	–	–
P36	P36	REMC2	CLPLS	UPMUX	∗1	–	–	–	–
P37	P37	–	–	UPMUX	∗1	–	–	–	–

∗1: Refer to the “Universal Port Multiplexer” chapter.

6.7.5 P4 Port Group

The P4 port group supports the GPIO and interrupt functions.

Table 6.7.5.1 Control Registers for P4 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P4DAT (P4 Port Data Register)	15–8	P4OUT[7:0]	0x00	H0	R/W	–
	7–0	P4IN[7:0]	0x00	H0	R	
P4IOEN (P4 Port Enable Register)	15–8	P4IEN[7:0]	0x00	H0	R/W	–
	7–0	P4OEN[7:0]	0x00	H0	R/W	
P4RCTL (P4 Port Pull-up/down Control Register)	15–8	P4PDPU[7:0]	0x00	H0	R/W	–
	7–0	P4REN[7:0]	0x00	H0	R/W	
P4INTF (P4 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P4IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P4INTCTL (P4 Port Interrupt Control Register)	15–8	P4EDGE[7:0]	0x00	H0	R/W	–
	7–0	P4IE[7:0]	0x00	H0	R/W	
P4CHATEN (P4 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P4CHATEN[7:0]	0x00	H0	R/W	
P4MODSEL (P4 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P4SEL[7:0]	0x00	H0	R/W	
P4FNCSEL (P4 Port Function Select Register)	15–14	P47MUX[1:0]	0x2	H0	R	–
	13–12	P46MUX[1:0]	0x2	H0	R	
	11–10	P45MUX[1:0]	0x2	H0	R	
	9–8	P44MUX[1:0]	0x2	H0	R	
	7–6	P43MUX[1:0]	0x2	H0	R	
	5–4	P42MUX[1:0]	0x2	H0	R	
	3–2	P41MUX[1:0]	0x2	H0	R	
	1–0	P40MUX[1:0]	0x2	H0	R	

Table 6.7.5.2 P4 Port Group Function Assignment

Port name	P4SEL*y* = 0	P4SEL*y* = 1							
	GPIO	P4*y*MUX = 0x0 (Function 0)		P4*y*MUX = 0x1 (Function 1)		P4*y*MUX = 0x2 (Function 2)		P4*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P40	P40	–	–	–	–	–	–	–	–
P41	P41	–	–	–	–	–	–	–	–
P42	P42	–	–	–	–	–	–	–	–
P43	P43	–	–	–	–	–	–	–	–
P44	P44	–	–	–	–	–	–	–	–
P45	P45	–	–	–	–	–	–	–	–
P46	P46	–	–	–	–	–	–	–	–
P47	P47	–	–	–	–	–	–	–	–

6.7.6 P5 Port Group

The P5 port group consists of six ports P50–P55 and they support the GPIO and interrupt functions.

Table 6.7.6.1 Control Registers for P5 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P5DAT (P5 Port Data Register)	15–14	–	0x0	–	R	–
	13–8	P5OUT[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P5IN[5:0]	0x00	H0	R	
P5IOEN (P5 Port Enable Register)	15–14	–	0x0	–	R	–
	13–8	P5IEN[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P5OEN[5:0]	0x00	H0	R/W	
P5RCTL (P5 Port Pull-up/down Control Register)	15–14	–	0x0	–	R	–
	13–8	P5PDPU[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P5REN[5:0]	0x00	H0	R/W	
P5INTF (P5 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	P5IF[5:0]	0x00	H0	R/W	Cleared by writing 1.
P5INTCTL (P5 Port Interrupt Control Register)	15–14	–	0x0	–	R	–
	13–8	P5EDGE[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	P5IEN[5:0]	0x00	H0	R/W	
P5CHATEN (P5 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	P5CHATEN[5:0]	0x00	H0	R/W	
P5MODSEL (P5 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	P5SEL[5:0]	0x00	H0	R/W	
P5FNCSEL (P5 Port Function Select Register)	15–12	–	0x0	–	R	–
	11–10	P55MUX[1:0]	0x2	H0	R	
	9–8	P54MUX[1:0]	0x2	H0	R	
	7–6	P53MUX[1:0]	0x2	H0	R	
	5–4	P52MUX[1:0]	0x2	H0	R	
	3–2	P51MUX[1:0]	0x2	H0	R	
	1–0	P50MUX[1:0]	0x2	H0	R	

Table 6.7.6.2 P5 Port Group Function Assignment

Port name	P5SEL*y* = 0	P5SEL*y* = 1							
	GPIO	P5*y*MUX = 0x0 (Function 0)		P5*y*MUX = 0x1 (Function 1)		P5*y*MUX = 0x2 (Function 2)		P5*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P50	P50	–	–	–	–	–	–	–	–
P51	P51	–	–	–	–	–	–	–	–
P52	P52	–	–	–	–	–	–	–	–
P53	P53	–	–	–	–	–	–	–	–
P54	P54	–	–	–	–	–	–	–	–
P55	P55	–	–	–	–	–	–	–	–

6.7.7 P6 Port Group

The P6 port group supports the GPIO and interrupt functions.

Table 6.7.7.1 Control Registers for P6 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P6DAT (P6 Port Data Register)	15–8	P6OUT[7:0]	0x00	H0	R/W	–
	7–0	P6IN[7:0]	0x00	H0	R	
P6IOEN (P6 Port Enable Register)	15–8	P6IEN[7:0]	0x00	H0	R/W	–
	7–0	P6OEN[7:0]	0x00	H0	R/W	
P6RCTL (P6 Port Pull-up/down Control Register)	15–8	P6PDPU[7:0]	0x00	H0	R/W	–
	7–0	P6REN[7:0]	0x00	H0	R/W	
P6INTF (P6 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P6IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P6INTCTL (P6 Port Interrupt Control Register)	15–8	P6EDGE[7:0]	0x00	H0	R/W	–
	7–0	P6IE[7:0]	0x00	H0	R/W	
P6CHATEN (P6 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P6CHATEN[7:0]	0x00	H0	R/W	
P6MODSEL (P6 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P6SEL[7:0]	0x00	H0	R/W	
P6FNCSEL (P6 Port Function Select Register)	15–14	P67MUX[1:0]	0x0	H0	R/W	–
	13–12	P66MUX[1:0]	0x0	H0	R/W	
	11–10	P65MUX[1:0]	0x0	H0	R/W	
	9–8	P64MUX[1:0]	0x0	H0	R/W	
	7–6	P63MUX[1:0]	0x0	H0	R/W	
	5–4	P62MUX[1:0]	0x0	H0	R/W	
	3–2	P61MUX[1:0]	0x0	H0	R/W	
	1–0	P60MUX[1:0]	0x0	H0	R/W	

Table 6.7.7.2 P6 Port Group Function Assignment

Port name	P6SEL*y* = 0	P6SEL*y* = 1							
	GPIO	P6*y*MUX = 0x0 (Function 0)		P6*y*MUX = 0x1 (Function 1)		P6*y*MUX = 0x2 (Function 2)		P6*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P60	P60	T16B Ch.2	EXCL20	UPMUX	*1	–	–	–	–
P61	P61	T16B Ch.3	EXCL30	UPMUX	*1	–	–	–	–
P62	P62	–	–	UPMUX	*1	–	–	–	–
P63	P63	–	–	UPMUX	*1	–	–	–	–
P64	P64	–	–	UPMUX	*1	–	–	–	–
P65	P65	–	–	UPMUX	*1	–	–	–	–
P66	P66	–	–	UPMUX	*1	–	–	–	–
P67	P67	–	–	UPMUX	*1	–	–	–	–

*1: Refer to the “Universal Port Multiplexer” chapter.

6.7.8 P7 Port Group

The P7 port group supports the GPIO and interrupt functions.

Table 6.7.8.1 Control Registers for P7 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P7DAT (P7 Port Data Register)	15–8	P7OUT[7:0]	0x00	H0	R/W	–
	7–0	P7IN[7:0]	0x00	H0	R	
P7IOEN (P7 Port Enable Register)	15–8	P7IEN[7:0]	0x00	H0	R/W	–
	7–0	P7OEN[7:0]	0x00	H0	R/W	
P7RCTL (P7 Port Pull-up/down Control Register)	15–8	P7PDPU[7:0]	0x00	H0	R/W	–
	7–0	P7REN[7:0]	0x00	H0	R/W	
P7INTF (P7 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P7IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P7INTCTL (P7 Port Interrupt Control Register)	15–8	P7EDGE[7:0]	0x00	H0	R/W	–
	7–0	P7IE[7:0]	0x00	H0	R/W	
P7CHATEN (P7 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P7CHATEN[7:0]	0x00	H0	R/W	
P7MODSEL (P7 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P7SEL[7:0]	0x00	H0	R/W	
P7FNCSEL (P7 Port Function Select Register)	15–14	P77MUX[1:0]	0x0	H0	R/W	–
	13–12	P76MUX[1:0]	0x0	H0	R/W	
	11–10	P75MUX[1:0]	0x0	H0	R/W	
	9–8	P74MUX[1:0]	0x0	H0	R/W	
	7–6	P73MUX[1:0]	0x0	H0	R/W	
	5–4	P72MUX[1:0]	0x0	H0	R/W	
	3–2	P71MUX[1:0]	0x0	H0	R/W	
	1–0	P70MUX[1:0]	0x0	H0	R/W	

Table 6.7.8.2 P7 Port Group Function Assignment

Port name	P7SEL*y* = 0	P7SEL*y* = 1							
	GPIO	P7*y*MUX = 0x0 (Function 0)		P7*y*MUX = 0x1 (Function 1)		P7*y*MUX = 0x2 (Function 2)		P7*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P70	P70	–	–	UPMUX	*1	–	–	–	–
P71	P71	–	–	UPMUX	*1	–	–	–	–
P72	P72	–	–	UPMUX	*1	–	–	–	–
P73	P73	–	–	UPMUX	*1	–	–	–	–
P74	P74	T16B Ch.2	EXCL21	UPMUX	*1	–	–	–	–
P75	P75	T16B Ch.3	EXCL31	UPMUX	*1	–	–	–	–
P76	P76	–	–	UPMUX	*1	–	–	–	–
P77	P77	–	–	UPMUX	*1	–	–	–	–

*1: Refer to the “Universal Port Multiplexer” chapter.

6.7.9 P8 Port Group

The P8 port group supports the GPIO and interrupt functions.

Table 6.7.9.1 Control Registers for P8 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P8DAT (P8 Port Data Register)	15–8	P8OUT[7:0]	0x00	H0	R/W	–
	7–0	P8IN[7:0]	0x00	H0	R	
P8IOEN (P8 Port Enable Register)	15–8	P8IEN[7:0]	0x00	H0	R/W	–
	7–0	P8OEN[7:0]	0x00	H0	R/W	
P8RCTL (P8 Port Pull-up/down Control Register)	15–8	P8PDPU[7:0]	0x00	H0	R/W	–
	7–0	P8REN[7:0]	0x00	H0	R/W	
P8INTF (P8 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–0	P8IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
P8INTCTL (P8 Port Interrupt Control Register)	15–8	P8EDGE[7:0]	0x00	H0	R/W	–
	7–0	P8IE[7:0]	0x00	H0	R/W	
P8CHATEN (P8 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–0	P8CHATEN[7:0]	0x00	H0	R/W	
P8MODSEL (P8 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–0	P8SEL[7:0]	0x00	H0	R/W	
P8FNCSEL (P8 Port Function Select Register)	15–14	P87MUX[1:0]	0x2	H0	R	–
	13–12	P86MUX[1:0]	0x2	H0	R	
	11–10	P85MUX[1:0]	0x2	H0	R	
	9–8	P84MUX[1:0]	0x2	H0	R	
	7–6	P83MUX[1:0]	0x2	H0	R	
	5–4	P82MUX[1:0]	0x2	H0	R	
	3–2	P81MUX[1:0]	0x2	H0	R	
	1–0	P80MUX[1:0]	0x2	H0	R	

Table 6.7.9.2 P8 Port Group Function Assignment

Port name	P8SEL*y* = 0	P8SEL*y* = 1							
	GPIO	P8*y*MUX = 0x0 (Function 0)		P8*y*MUX = 0x1 (Function 1)		P8*y*MUX = 0x2 (Function 2)		P8*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P80	P80	–	–	–	–	–	–	–	–
P81	P81	–	–	–	–	–	–	–	–
P82	P82	–	–	–	–	–	–	–	–
P83	P83	–	–	–	–	–	–	–	–
P84	P84	–	–	–	–	–	–	–	–
P85	P85	–	–	–	–	–	–	–	–
P86	P86	–	–	–	–	–	–	–	–
P87	P87	–	–	–	–	–	–	–	–

6.7.10 P9 Port Group

The P9 port group consists of seven ports P90–P96 and they support the GPIO and interrupt functions.

Table 6.7.10.1 Control Registers for P9 Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P9DAT (P9 Port Data Register)	15	–	0	–	R	–
	14–8	P9OUT[6:0]	0x00	H0	R/W	
	7	–	0	–	R	
	6–0	P9IN[6:0]	0x00	H0	R	
P9IOEN (P9 Port Enable Register)	15	–	0	–	R	–
	14–8	P9IEN[6:0]	0x00	H0	R/W	
	7	–	0	–	R	
	6–0	P9OEN[6:0]	0x00	H0	R/W	
P9RCTL (P9 Port Pull-up/down Control Register)	15	–	0	–	R	–
	14–8	P9PDPU[6:0]	0x00	H0	R/W	
	7	–	0	–	R	
	6–0	P9REN[6:0]	0x00	H0	R/W	
P9INTF (P9 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–0	P9IF[6:0]	0x00	H0	R/W	Cleared by writing 1.
P9INTCTL (P9 Port Interrupt Control Register)	15	–	0	–	R	–
	14–8	P9EDGE[6:0]	0x00	H0	R/W	
	7	–	0	–	R	
	6–0	P9IEN[6:0]	0x00	H0	R/W	
P9CHATEN (P9 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–0	P9CHATEN[6:0]	0x00	H0	R/W	
P9MODSEL (P9 Port Mode Select Register)	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–0	P9SEL[6:0]	0x00	H0	R/W	
P9FNCSEL (P9 Port Function Select Register)	15–14	–	0x0	–	R	–
	13–12	P96MUX[1:0]	0x2	H0	R	
	11–10	P95MUX[1:0]	0x2	H0	R	
	9–8	P94MUX[1:0]	0x2	H0	R	
	7–6	P93MUX[1:0]	0x0	H0	R/W	
	5–4	P92MUX[1:0]	0x0	H0	R/W	
	3–2	P91MUX[1:0]	0x0	H0	R/W	
	1–0	P90MUX[1:0]	0x0	H0	R/W	

Table 6.7.10.2 P9 Port Group Function Assignment

Port name	P9SEL*y* = 0	P9SEL*y* = 1							
	GPIO	P9*y*MUX = 0x0 (Function 0)		P9*y*MUX = 0x1 (Function 1)		P9*y*MUX = 0x2 (Function 2)		P9*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
P90	P90	RTC	RTC1S	RTC	RTCINT	–	–	–	–
P91	P91	T16B Ch.0	EXCL01	–	–	–	–	–	–
P92	P92	T16B Ch.1	EXCL11	–	–	–	–	–	–
P93	P93	CLG	EXOSC	–	–	–	–	–	–
P94	P94	–	–	–	–	–	–	–	–
P95	P95	–	–	–	–	–	–	–	–
P96	P96	–	–	–	–	–	–	–	–

6.7.11 Pa Port Group

The Pa port group consists of six ports Pa0–Pa5 and they support the GPIO and interrupt functions.

Table 6.7.11.1 Control Registers for Pa Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PADAT (Pa Port Data Register)	15–14	–	0x0	–	R	–
	13–8	PAOUT[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	PAIN[5:0]	0x00	H0	R	
PAIOEN (Pa Port Enable Register)	15–14	–	0x0	–	R	–
	13–8	PAIEN[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	PAOEN[5:0]	0x00	H0	R/W	
PARCTL (Pa Port Pull-up/down Control Register)	15–14	–	0x0	–	R	–
	13–8	PAPDPU[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	PAREN[5:0]	0x00	H0	R/W	
PAINTF (Pa Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	PAIF[5:0]	0x00	H0	R/W	Cleared by writing 1.
PAINTCTL (Pa Port Interrupt Control Register)	15–14	–	0x0	–	R	–
	13–8	PAEDGE[5:0]	0x00	H0	R/W	
	7–6	–	0x0	–	R	
	5–0	PAIEN[5:0]	0x00	H0	R/W	
PACHATEN (Pa Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	PACHATEN[5:0]	0x00	H0	R/W	
PAMODSEL (Pa Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5–0	PASEL[5:0]	0x00	H0	R/W	
PAFNCSEL (Pa Port Function Select Register)	15–12	–	0x0	–	R	–
	11–10	PA5MUX[1:0]	0x2	H0	R	
	9–8	PA4MUX[1:0]	0x2	H0	R	
	7–6	PA3MUX[1:0]	0x2	H0	R	
	5–4	PA2MUX[1:0]	0x2	H0	R	
	3–2	PA1MUX[1:0]	0x2	H0	R	
	1–0	PA0MUX[1:0]	0x2	H0	R	

Table 6.7.11.2 Pa Port Group Function Assignment

Port name	PASEL*y* = 0	PASEL*y* = 1							
	GPIO	PA*y*MUX = 0x0 (Function 0)		PA*y*MUX = 0x1 (Function 1)		PA*y*MUX = 0x2 (Function 2)		PA*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
Pa0	Pa0	–	–	–	–	–	–	–	–
Pa1	Pa1	–	–	–	–	–	–	–	–
Pa2	Pa2	–	–	–	–	–	–	–	–
Pa3	Pa3	–	–	–	–	–	–	–	–
Pa4	Pa4	–	–	–	–	–	–	–	–
Pa5	Pa5	–	–	–	–	–	–	–	–

6.7.12 Pd Port Group

The Pd port group consists of five ports Pd0–Pd4 and three ports Pd0–Pd2 are configured as a debugging function port at initialization. These five ports support the GPIO function. The GPIO function of the Pd2 port supports output only, therefore, the pull-up/down function cannot be used.

Table 6.7.12.1 Control Registers for Pd Port Group

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PDDAT (Pd Port Data Register)	15–13	–	0x0	–	R	–
	12–8	PDOUT[4:0]	0x00	H0	R/W	
	7–5	–	0x0	–	R	
	4–3	PDIN[4:3]	x	H0	R	
	2	–	0	–	R	
	1–0	PDIN[1:0]	x	H0	R	
PDIOEN (Pd Port Enable Register)	15–13	–	0x0	–	R	–
	12–11	PDIEN[4:3]	0x0	H0	R/W	
	10	(reserved)	0	H0	R/W	
	9–8	PDIEN[1:0]	0x0	H0	R/W	
	7–5	–	0x0	–	R	
	4–0	PDOEN[4:0]	0x00	H0	R/W	
PDRCTL (Pd Port Pull-up/down Control Register)	15–13	–	0x0	–	R	–
	12–11	PDPDPU[4:3]	0x0	H0	R/W	
	10	(reserved)	0	H0	R/W	
	9–8	PDPDPU[1:0]	0x0	H0	R/W	
	7–5	–	0x0	–	R	
	4–3	PDREN[4:3]	0x0	H0	R/W	
	2	(reserved)	0	H0	R/W	
	1–0	PDREN[1:0]	0x0	H0	R/W	
PDINTF PDINTCTL PDCHATEN	15–0	–	0x0000	–	R	–
PDMODSEL (Pd Port Mode Select Register)	15–8	–	0x00	–	R	–
	7–5	–	0x0	–	R	
	4–0	PDSEL[4:0]	0x07	H0	R/W	
PDFNCSEL (Pd Port Function Select Register)	15–10	–	0x00	–	R	–
	9–8	PD4MUX[1:0]	0x0	H0	R/W	
	7–6	PD3MUX[1:0]	0x0	H0	R/W	
	5–4	PD2MUX[1:0]	0x0	H0	R/W	
	3–2	PD1MUX[1:0]	0x0	H0	R/W	
	1–0	PD0MUX[1:0]	0x0	H0	R/W	

Table 6.7.12.2 Pd Port Group Function Assignment

Port name	PdSEL*y* = 0	PdSEL*y* = 1							
	GPIO	Pd*y*MUX = 0x0 (Function 0)		Pd*y*MUX = 0x1 (Function 1)		Pd*y*MUX = 0x2 (Function 2)		Pd*y*MUX = 0x3 (Function 3)	
		Peripheral	Pin	Peripheral	Pin	Peripheral	Pin	Peripheral	Pin
Pd0	Pd0	DBG	DST2	–	–	–	–	–	–
Pd1	Pd1	DBG	DSIO	–	–	–	–	–	–
Pd2	Pd2	DBG	DCLK	–	–	–	–	–	–
Pd3	Pd3	–	–	–	–	CLG	OSC3	–	–
Pd4	Pd4	–	–	–	–	CLG	OSC4	–	–

6.7.13 Common Registers between Port Groups

Table 6.7.13.1 Control Registers for Common Use with Port Groups

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
PCLK (P Port Clock Control Register)	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/WP	
	7–4	CLKDIV[3:0]	0x0	H0	R/WP	
	3–2	KRSTCFG[1:0]	0x0	H0	R/WP	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	
PINTFGRP (P Port Interrupt Flag Group Register)	15–11	–	0x00	–	R	–
	10	PAINT	0	H0	R	
	9	P9INT	0	H0	R	
	8	P8INT	0	H0	R	
	7	P7INT	0	H0	R	
	6	P6INT	0	H0	R	
	5	P5INT	0	H0	R	
	4	P4INT	0	H0	R	
	3	P3INT	0	H0	R	
	2	P2INT	0	H0	R	
	1	P1INT	0	H0	R	
	0	P0INT	0	H0	R	

7 Universal Port Multiplexer (UPMUX)

7.1 Overview

UPMUX is a multiplexer that allows software to assign the desired peripheral I/O function to an I/O port. The main features are outlined below.

- Allows programmable assignment of the synchronous serial interface, I²C, UART, and 16-bit PWM timer peripheral I/O functions to the P0[7:0], P3[7:0], P6[7:0], and P7[7:0] ports.
- The peripheral I/O function assigned via UPMUX is enabled by setting the P*x*FNCSEL.P*xy*MUX[1:0] bits to 0x1.

Note: '*x*', which is used in the port names P*xy*, register names, and bit names, refers to a port group (*x* = 0, 3, 6, 7) and '*y*' refers to a port number (*y* = 0, 1, 2, ··· , 7).

Figure 7.1.1 shows the configuration of UPMUX.

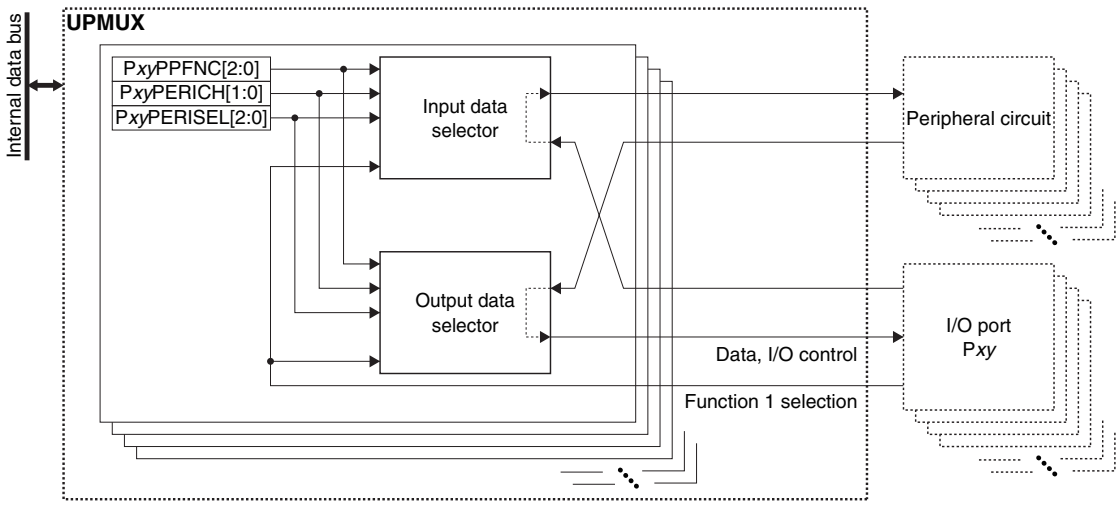


Figure 7.1.1 UPMUX Configuration

7.2 Peripheral Circuit I/O Function Assignment

An I/O function of a peripheral circuit supported may be assigned to peripheral I/O function 1 of an I/O port listed above. The following shows the procedure to assign a peripheral I/O function and enable it in the I/O port:

1. Configure the P*x*IOEN register of the I/O port.
   - Set the P*x*IOEN.P*x*IEN*y* bit to 0. (Disable input)
   - Set the P*x*IOEN.P*x*OEN*y* bit to 0. (Disable output)
2. Set the P*x*MODSEL.P*x*SEL*y* bit of the I/O port to 0. (Disable peripheral I/O function)
3. Set the following P*x*UPMUX*n* register bits (*n* = 0 to 3).
   - P*x*UPMUX*n*.P*xy*PERISEL[2:0] bits (Select peripheral circuit)
   - P*x*UPMUX*n*.P*xy*PERICH[1:0] bits (Select peripheral circuit channel)
   - P*x*UPMUX*n*.P*xy*PPFNC[2:0] bits (Select function to assign)
4. Initialize the peripheral circuit.
5. Set the P*x*FNCSEL.P*xy*MUX[1:0] bits of the I/O port to 0x1. (Select peripheral I/O function 1)
6. Set the P*x*MODSEL.P*x*SEL*y* bit of the I/O port to 1. (Enable peripheral I/O function)

7.3 Control Registers

P*xy–xz* Universal Port Multiplexer Setting Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
P*x*UPMUX*n*	15–13	P*xz*PPFNC[2:0]	0x0	H0	R/W	–
	12–11	P*xz*PERICH[1:0]	0x0	H0	R/W	
	10–8	P*xz*PERISEL[2:0]	0x0	H0	R/W	
	7–5	P*xy*PPFNC[2:0]	0x0	H0	R/W	
	4–3	P*xy*PERICH[1:0]	0x0	H0	R/W	
	2–0	P*xy*PERISEL[2:0]	0x0	H0	R/W	

∗1: '*x*' in the register name refers to a port group number and '*n*' refers to a register number (0–3).
∗2: '*x*' in the bit name refers to a port group number, '*y*' refers to an even port number (0, 2, 4, 6), and '*z*' refers to an odd port number (*z* = *y* + 1).

Bits 15–13 P*xz*PPFNC[2:0]
Bits 7–5 P*xy*PPFNC[2:0]

These bits specify the peripheral I/O function to be assigned to the port. (See Table 7.3.1.)

Bits 12–11 P*xz*PERICH[1:0]
Bits 4–3 P*xy*PERICH[1:0]

These bits specify a peripheral circuit channel number. (See Table 7.3.1.)

Bits 10–8 P*xz*PERISEL[2:0]
Bits 2–0 P*xy*PERISEL[2:0]

These bits specify a peripheral circuit. (See Table 7.3.1.)

Table 7.3.1 Peripheral I/O Function Selections

P*x*UPMUX*n*.P*xy*PPFNC[2:0] bits (Peripheral I/O function)	P*x*UPMUX*n*.P*xy*PERISEL[2:0] bits (Peripheral circuit)							
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
	None ∗	I2C	SPIA	UART	T16B	Reserved	Reserved	Reserved
	P*x*UPMUX*n*.P*xy*PERICH[1:0] bits (Peripheral circuit channel)							
	–	0x0–0x1	0x0–0x1	0x0–0x2	0x0–0x3	–	–	–
	–	Ch.0–1	Ch.0–1	Ch.0–2	Ch.0–3	–	–	–
0x0	None ∗	None ∗	None ∗	None ∗	None ∗	None ∗	None ∗	None ∗
0x1	Reserved	SCL*n*	SDI*n*	USIN*n*	TOUT*n*0/ CAP*n*0	Reserved	Reserved	Reserved
0x2		SDA*n*	SDO*n*	USOUT*n*	TOUT*n*1/ CAP*n*1			
0x3		Reserved	SPICLK*n*	Reserved	TOUT*n*2/ CAP*n*2			
0x4			#SPISS*n*		TOUT*n*3/ CAP*n*3			
0x5			Reserved		TOUT*n*4/ CAP*n*4			
0x6					TOUT*n*5/ CAP*n*5			
0x7					Reserved			

∗ "None" means no assignment. Selecting this will put the P*xy* pin into Hi-Z status when peripheral I/O function 1 is selected and enabled in the I/O port.

Note: Do not assign a peripheral input function to two or more I/O ports. Although the I/O ports output the same waveforms when an output function is assigned to two or more I/O port, a skew occurs due to the internal delay.

8 Watchdog Timer (WDT)

8.1 Overview

WDT restarts the system if a problem occurs, such as when the program cannot be executed normally.
The features of WDT are listed below.

- Includes a 10-bit up counter to count NMI/reset generation cycle.
- A counter clock source and clock division ratio are selectable.
- Counter overflow generates a reset or NMI.

Figure 8.1.1 shows the configuration of WDT.

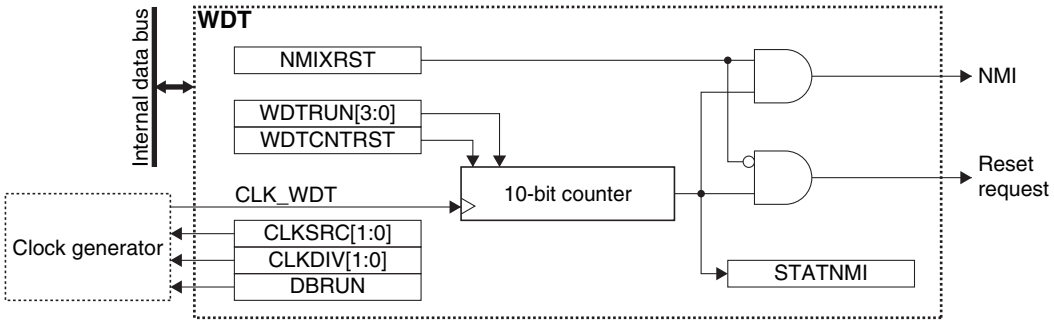


Figure 8.1.1 WDT Configuration

8.2 Clock Settings

8.2.1 WDT Operating Clock

When using WDT, the WDT operating clock CLK_WDT must be supplied to WDT from the clock generator.
The CLK_WDT supply should be controlled as in the procedure shown below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
3. Set the following WDTCLK register bits:
   WDTCLK.CLKSRC[1:0] bits (Clock source selection)
   WDTCLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)
4. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Use the following equation to calculate the WDT counter overflow cycle (NMI/reset generation cycle).

$$t_{WDT} = \frac{1{,}024}{CLK\_WDT} \qquad \text{(Eq. 8.1)}$$

Where

t_{WDT}: Counter overflow cycle [second]
CLK_WDT: WDT operating clock frequency [Hz]

Example) t_{WDT} = 4 seconds when CLK_WDT = 256 Hz

8.2.2 Clock Supply in DEBUG Mode

The CLK_WDT supply during DEBUG mode should be controlled using the WDTCLK.DBRUN bit.
The CLK_WDT supply to WDT is suspended when the CPU enters DEBUG mode if the WDTCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_WDT supply resumes. Although WDT stops operating when the CLK_WDT supply is suspended, the register retains the status before DEBUG mode was entered.
If the WDTCLK.DBRUN bit = 1, the CLK_WDT supply is not suspended and WDT will keep operating in DEBUG mode.

8.3 Operations

8.3.1 WDT Control

Starting up WDT

WDT should be initialized and started up with the procedure listed below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Configure the WDT operating clock.
3. Configure the WDTCTL.NMIXRST bit. (Select NMI or reset mode)
4. Write 1 to the WDTCTL.WDTCNTRST bit. (Reset WDT counter)
5. Write a value other than 0xa to the WDTCTL.WDTRUN[3:0] bits. (Start up WDT)
6. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Resetting WDT

WDT generates a system reset (WDTCTL.NMIXRST bit = 0) or NMI (WDTCTL.NMIXRST bit = 1) when the counter overflows. To avert system restart by WDT, its embedded counter must be reset periodically via software while WDT is running.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Write 1 to the WDTCTL.WDTCNTRST bit. (Reset WDT counter)
3. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

A location should be provided for periodically processing this routine. Process this routine within the t_{WDT} cycle. After resetting, WDT starts counting with a new NMI/reset generation cycle.
If WDT is not reset within the t_{WDT} cycle for any reason, the CPU is switched to interrupt processing by NMI or reset, the interrupt vector is read out, and the interrupt handler routine is executed.
If the counter overflows and generates an NMI without WDT being reset, the WDTCTL.STATNMI bit is set to 1.

8.3.2 Operations in HALT and SLEEP Modes

During HALT mode

WDT operates in HALT mode. HALT mode is therefore cleared by an NMI or reset if it continues for more than the NMI/reset generation cycle and the NMI or reset handler is executed. To disable WDT in HALT mode, stop WDT by writing 0xa to the WDTCTL.WDTRUN[3:0] bits before executing the halt instruction. Reset WDT before resuming operations after HALT mode is cleared.

During SLEEP mode

WDT operates in SLEEP mode if the selected clock source is running. In this case SLEEP mode is cleared by an NMI or reset if it continues for more than the NMI/reset generation cycle and the NMI or reset handler is executed. Therefore, stop WDT by setting the WDTCTL.WDTRUN[3:0] bits before executing the slp instruction.
If the clock source stops in SLEEP mode, WDT stops. To prevent generation of an unnecessary NMI or reset after clearing SLEEP mode, reset WDT before executing the slp instruction. WDT should also be stopped as required using the WDTCTL.WDTRUN[3:0] bits.

8.4 Control Registers

WDT Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
WDTCLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/WP	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the WDT operating clock is supplied in DEBUG mode or not.
1 (R/WP): Clock supplied in DEBUG mode
0 (R/WP): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the WDT operating clock (counter clock). The clock frequency should be set to around 256 Hz.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of WDT.

Table 8.4.1 Clock Source and Division Ratio Settings

WDTCLK. CLKDIV[1:0] bits	WDTCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/65,536	1/128	1/65,536	1/1
0x2	1/32,768		1/32,768	
0x1	1/16,384		1/16,384	
0x0	1/8,192		1/8,192	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

WDT Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
WDTCTL	15–10	–	0x00	–	R	–
	9	NMIXRST	0	H0	R/WP	
	8	STATNMI	0	H0	R	
	7–5	–	0x0	–	R	
	4	WDTCNTRST	0	H0	WP	Always read as 0.
	3–0	WDTRUN[3:0]	0xa	H0	R/WP	–

Bits 15–10 Reserved

Bit 9 NMIXRST

This bit sets the WDT operating mode.
1 (R/WP): NMI mode
0 (R/WP): Reset mode

This bit is used to select whether an NMI signal or a reset signal is output when WDT has not been reset within the NMI/reset generation cycle.

Bit 8 STATNMI

This bit indicates that a counter overflow and NMI have occurred.

1 (R): NMI (counter overflow) occurred
0 (R): NMI not occurred

When the NMI generation function of WDT is used, read this bit in the NMI handler routine to confirm that WDT was the source of the NMI.
The STATNMI set to 1 is cleared to 0 by resetting WDT.

Bits 7–5 Reserved

Bit 4 WDTCNTRST

This bit resets WDT.

1 (WP): Reset
0 (WP): Ignored
0 (R): Always 0 when being read

Bits 3–0 WDTRUN[3:0]

These bits control WDT to run and stop.

0xa (WP): Stop
Values other than 0xa (WP): Run
0xa (R): Idle
0x0 (R): Running

Always 0x0 is read if a value other than 0xa is written.
Since an NMI or reset may be generated immediately after running depending on the counter value, WDT should also be reset concurrently when running WDT.

9 Real-Time Clock (RTCA)

9.1 Overview

RTCA is a real-time clock with a perpetual calendar function. The main features of RTCA are outlined below.

- Includes a BCD real-time clock counter to implement a time-of-day clock (second, minute, and hour) and calendar (day, day of the week, month, and year with leap year supported).
- Provides a hold function for reading correct counter values by suspending the real-time clock counter operation.
- 24-hour or 12-hour mode is selectable.
- Capable of controlling the starting and stopping of the time-of-day clock.
- Provides a 30-second correction function to adjust time using a time signal.
- Includes a 1 Hz counter to count 128 to 1 Hz.
- Includes a BCD stopwatch counter with 1/100-second counting supported.
- Provides a theoretical regulation function to correct clock error due to frequency tolerance with no external parts required.

Figure 9.1.1 shows the configuration of RTCA.

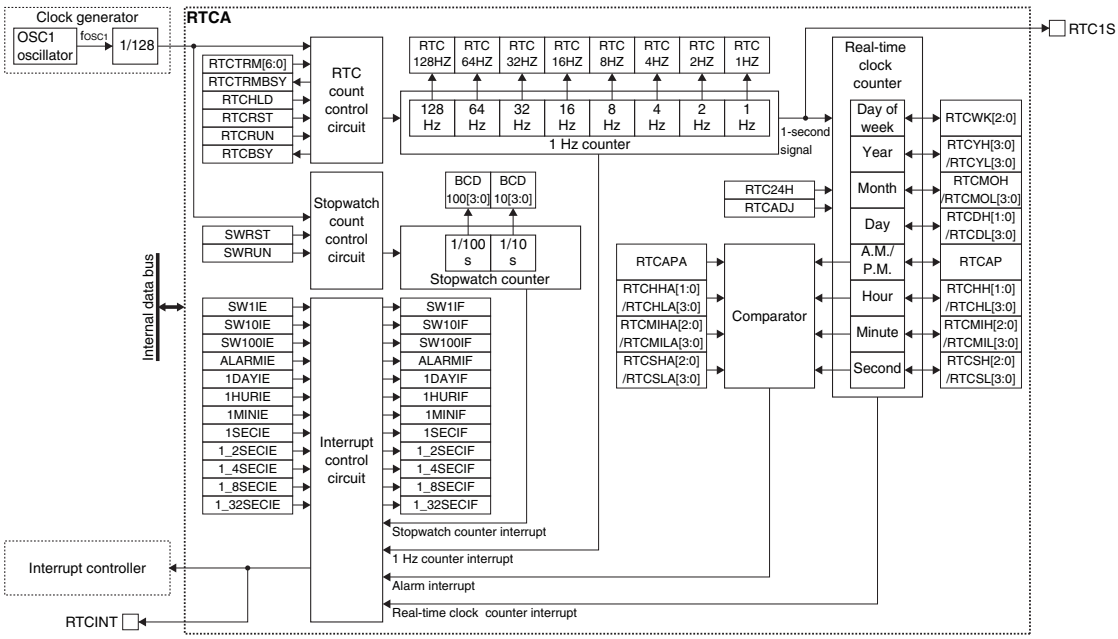


Figure 9.1.1 RTCA Configuration

9.2 Output Pin and External Connection

9.2.1 Output Pin

Table 9.2.1.1 shows the RTCA pin.

Table 9.2.1.1 RTCA Pin

Pin name	I/O*	Initial status*	Function
RTC1S	O	O (L)	1-second signal monitor output pin
RTCINT	O	O (L)	RTCA interrupt signal output pin

* Indicates the status when the pin is configured for RTCA.

If the port is shared with the RTCA output function and other functions, the RTCA function must be assigned to the port. For more information, refer to the "I/O Ports" chapter.

9.3 Clock Settings

9.3.1 RTCA Operating Clock

RTCA uses CLK_RTCA, which is generated by the clock generator from OSC1 as the clock source, as its operating clock. RTCA is operable when OSC1 is enabled.
To continue the RTCA operation during SLEEP mode with OSC1 being activated, the CLGOSC.OSC1SLPC bit must be set to 0.

9.3.2 Theoretical Regulation Function

The time-of-day clock loses accuracy if the OSC1 frequency f_{OSC1} has a frequency tolerance from 32.768 kHz. To correct this error without changing any external part, RTCA provides a theoretical regulation function. Follow the procedure below to perform theoretical regulation.

1. Measure f_{OSC1} and calculate the frequency tolerance correction value
   "m [ppm] = -{(f_{OSC1} - 32,768 [Hz]) / 32,768 [Hz]} × 10^6."
2. Determine the theoretical regulation execution cycle time "n seconds."
3. Determine the value to be written to the RTCCTL.RTCTRM[6:0] bits from the results in Steps 1 and 2.
4. Write the value determined in Step 3 to the RTCCTL.RTCTRM[6:0] bits periodically in n-second cycles using an RTCA alarm or second interrupt.
5. Monitor the RTC1S signal to check that every n-second cycle has no error included.

The correction value for theoretical regulation can be specified within the range from -64 to +63 and it should be written to the RTCCTL.RTCTRM[6:0] bits as a two's-complement number. Use Eq. 9.1 to calculate the correction value.

$$\text{RTCTRM[6:0]} = \frac{m}{10^6} \times 256 \times n \quad \text{(However, RTCTRM[6:0] is an integer after rounding off to -64 to +63.)} \quad \text{(Eq. 9.1)}$$

Where

- n: Theoretical regulation execution cycle time [second] (time interval to write the correct value to the RTCCTL.RTCTRM[6:0] bits periodically via software)
- m: OSC1 frequency tolerance correction value [ppm]

Figure 9.3.2.1 shows the RTC1S signal waveform.

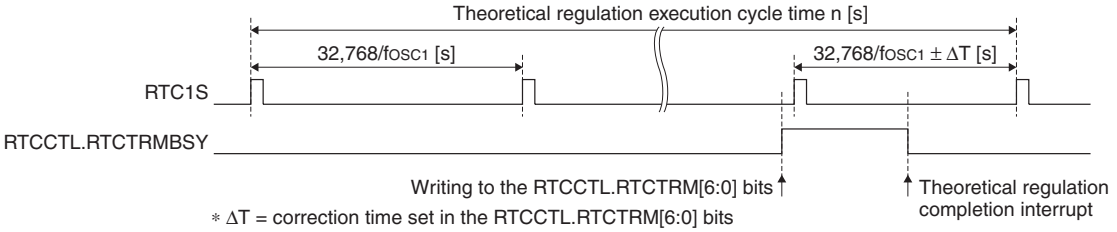


Figure 9.3.2.1 RTC1S Signal Waveform

Table 9.3.2.1 lists the frequency tolerance correction rates when the theoretical regulation execution cycle time n is 4,096 seconds as an example.

Table 9.3.2.1 Correction Rates when Theoretical Regulation Execution Cycle Time n = 4,096 Seconds

RTCCTL.RTCTRM[6:0] bits (two's-complement)	Correction value (decimal)	Correction rate [ppm]	RTCCTL.RTCTRM[6:0] bits (two's-complement)	Correction value (decimal)	Correction rate [ppm]
0x00	0	0.0	0x40	-64	-61.0
0x01	1	1.0	0x41	-63	-60.1
0x02	2	1.9	0x42	-62	-59.1
0x03	3	2.9	0x43	-61	-58.2
. . .	. . .	. . .	. . .	. . .	. . .
0x3e	62	59.1	0x7e	-2	-1.9
0x3f	63	60.1	0x7f	-1	-1.0

Minimum resolution: 1 ppm, Correction rate range: -61.0 to 60.1 ppm

Notes: • The theoretical regulation affects only the real-time clock counter and 1 Hz counter. It does not affect the stopwatch counter.

• After a value is written to the RTCCTL.RTCTRM[6:0] bits, the theoretical regulation correction takes effect on the 1 Hz counter value at the same timing as when the 1 Hz counter changes to 0x7f. Also an interrupt occurs depending on the counter value at this time.

9.4 Operations

9.4.1 RTCA Control

Follow the sequences shown below to set time to RTCA, to read the current time and to set alarm.

Time setting

1. Set RTCA to 12H or 24H mode using the RTCCTL.RTC24H bit.
2. Write 1 to the RTCCTL.RTCRUN bit to enable for the real-time clock counter to start counting up.
3. Check to see if the RTCCTL.RTCBSY bit = 0 that indicates the counter is ready to rewrite. If the RTCCTL.RTCBSY bit = 1, wait until it is set to 0.
4. Write the current date and time in BCD code to the control bits listed below.
   RTCSEC.RTCSH[2:0]/RTCSL[3:0] bits (second)
   RTCHUR.RTCMIH[2:0]/RTCMIL[3:0] bits (minute)
   RTCHUR.RTCHH[1:0]/RTCHL[3:0] bits (hour)
   RTCHUR.RTCAP bit (AM/PM) (effective when RTCCTL.RTC24H bit = 0)
   RTCMON.RTCDH[1:0]/RTCDL[3:0] bits (day)
   RTCMON.RTCMOH/RTCMOL[3:0] bits (month)
   RTCYAR.RTCYH[3:0]/RTCYL[3:0] bits (year)
   RTCYAR.RTCWK[2:0] bits (day of the week)
5 Write 1 to the RTCCTL.RTCADJ bit (execute 30-second correction) using a time signal to adjust the time. (For more information on the 30-second correction, refer to "Real-Time Clock Counter Operations.")
6. Write 1 to the real-time clock counter interrupt flags in the RTCINTF register to clear them.
7. Write 1 to the interrupt enable bits in the RTCINTE register to enable real-time clock counter interrupts.

Time read

1. Check to see if the RTCCTL.RTCBSY bit = 0. If the RTCCTL.RTCBSY bit = 1, wait until it is set to 0.
2. Write 1 to the RTCCTL.RTCHLD bit to suspend count-up operation of the real-time clock counter.
3. Read the date and time from the control bits listed in "Time setting, Step 4" above.
4. Write 0 to the RTCCTL.RTCHLD bit to resume count-up operation of the real-time clock counter. If a second count-up timing has occurred in the count hold state, the hardware corrects the second counter for +1 second (for more information on the +1 second correction, refer to "Real-Time Clock Counter Operations").

Alarm setting

1. Write 0 to the RTCINTE.ALARMIE bit to disable alarm interrupts.
2. Write the alarm time in BCD code to the control bits listed below (a time within 24 hours from the current time can be specified).
   RTCALM1.RTCSHA[2:0]/RTCSLA[3:0] bits (second)
   RTCALM2.RTCMIHA[2:0]/RTCMILA[3:0] bits (minute)
   RTCALM2.RTCHHA[1:0]/RTCHLA[3:0] bits (hour)
   RTCALM2.RTCAPA bit (AM/PM) (effective when RTCCTL.RTC24H bit = 0)
3. Write 1 to the RTCINTF.ALARMIF bit to clear the alarm interrupt flag.
4. Write 1 to the RTCINTE.ALARMIE bit to enable alarm interrupts.
   When the real-time clock counter reaches the alarm time set in Step 2, an alarm interrupt occurs.

9.4.2 Real-Time Clock Counter Operations

The real-time clock counter consists of second, minute, hour, AM/PM, day, month, year, and day of the week counters and it performs counting up using the RTC1S signal. It has the following functions as well.

Recognizing leap years

The leap year recognizing algorithm used in RTCA is effective only for Christian Era years. Years within 0 to 99 that can be divided by four without a remainder are recognized as leap years. If the year counter = 0x00, RTCA assumes it as a common year. If a leap year is recognized, the count range of the day counter changes when the month counter is set to February.

Corrective operation when a value out of the effective range is set

When a value out of the effective range is set to the year, day of the week, or hour (in 24H mode) counter, the counter will be cleared to 0 at the next count-up timing. When a such value is set to the month, day, or hour (in 12H mode) counter, the counter will be set to 1 at the next count-up timing.

Note: Do not set the RTCMON.RTCMOL[3:0] bits to 0x0 if the RTCMON.RTCMOH bit = 0.

30-second correction

This function is provided to set the time-of-day clock by the time signal. Writing 1 to the RTCCTL.RTCADJ bit clears the second counter and adds 1 to the minute counter if the second counter represents 30 to 59 seconds, or clears the second counter with the minute counter left unchanged if the second counter represents 0 to 29 seconds.

+1 second correction

If a second count-up timing occurred while the RTCCTL.RTCHLD bit = 1 (count hold state), the real-time clock counter counts up by +1 second (performs +1 second correction) after the counting has resumed by writing 0 to the RTCCTL.RTCHLD bit.

Note: If two or more second count-up timings occurred while the RTCCTL.RTCHLD bit = 1, the counter is always corrected for +1 second only.

9.4.3 Stopwatch Control

Follow the sequences shown below to start counting of the stopwatch and to read the counter.

Count start

1. Write 1 to the RTCSWCTL.SWRST bit to reset the stopwatch counter.
2. Write 1 to the stopwatch interrupt flags in the RTCINTF register to clear them.
3. Write 1 to the interrupt enable bits in the RTCINTE register to enable stopwatch interrupts.
4. Write 1 to the RTCSWCTL.SWRUN bit to start stopwatch count up operation.

Counter read

1. Read the count value from the RTCSWCTL.BCD10[3:0] and BCD100[3:0] bits.
2. Read again.
   i. If the two read values are the same, assume that the count values are read correctly.
   ii. If different values are read, perform reading once more and compare the read value with the previous one.

9.4.4 Stopwatch Count-up Pattern

The stopwatch consists of 1/100-second and 1/10-second counters and these counters perform counting up in increments of approximate 1/100 and 1/10 seconds with the count-up patterns shown in Figure 9.4.4.1.

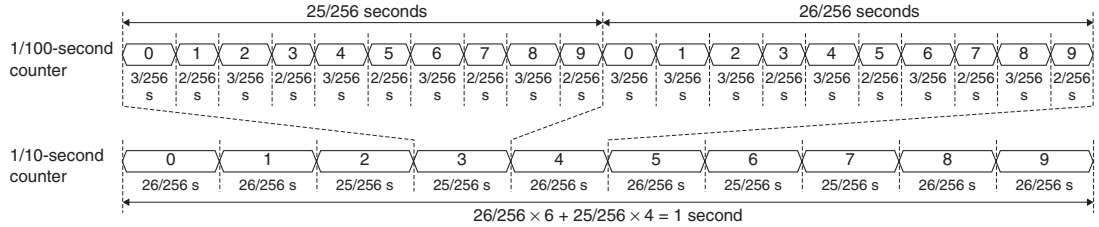


Figure 9.4.4.1 Stopwatch Count-Up Patterns

9.5 Interrupts

RTCA has a function to generate the interrupts shown in Table 9.5.1.

Table 9.5.1 RTCA Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Alarm	RTCINTF.ALARMIF	Matching between the RTCALM1–2 register contents and the real-time clock counter contents	Writing 1
1-day	RTCINTF.1DAYIF	Day counter count up	Writing 1
1-hour	RTCINTF.1HURIF	Hour counter count up	Writing 1
1-minute	RTCINTF.1MINIF	Minute counter count up	Writing 1
1-second	RTCINTF.1SECIF	Second counter count up	Writing 1
1/2-second	RTCINTF.1_2SECIF	See Figure 9.5.1.	Writing 1
1/4-second	RTCINTF.1_4SECIF	See Figure 9.5.1.	Writing 1
1/8-second	RTCINTF.1_8SECIF	See Figure 9.5.1.	Writing 1
1/32-second	RTCINTF.1_32SECIF	See Figure 9.5.1.	Writing 1
Stopwatch 1 Hz	RTCINTF.SW1IF	1/10-second counter overflow	Writing 1
Stopwatch 10 Hz	RTCINTF.SW10IF	1/10-second counter count up	Writing 1
Stopwatch 100 Hz	RTCINTF.SW100IF	1/100-second counter count up	Writing 1
Theoretical regulation completion	RTCINTF.RTCTRMIF	At the end of theoretical regulation operation	Writing 1

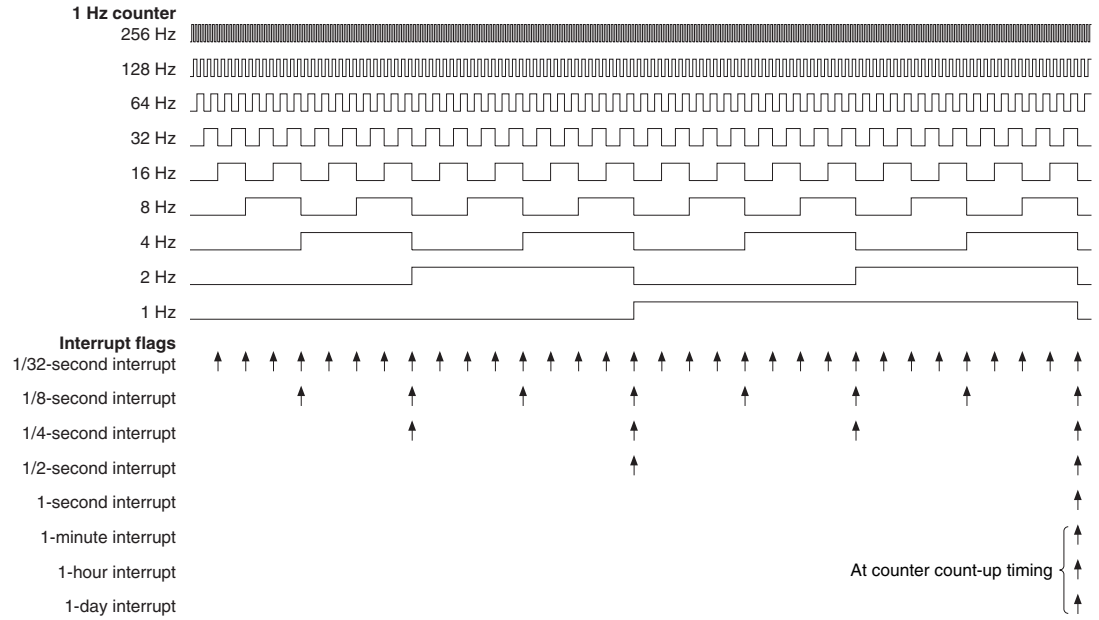


Figure 9.5.1 RTCA Interrupt Timings

Notes: • 1-second to 1/32-second interrupts occur after a lapse of 1/256 second from change of the 1 Hz counter value.

• An alarm interrupt occurs after a lapse of 1/256 second from matching between the AM/PM (in 12H mode), hour, minute, and second counter value and the alarm setting value.

RTCA provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.
The interrupt request signal is output from the RTCINT pin, so it can be used for starting external devices or other purposes.

9.6 Control Registers

RTC Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCCTL	15	RTCTRMBSY	0	H0	R	–
	14–8	RTCTRM[6:0]	0x00	H0	W	Read as 0x00.
	7	–	0	–	R	–
	6	RTCBSY	0	H0	R	
	5	RTCHLD	0	H0	R/W	Cleared by setting the RTCCTL.RTCRST bit to 1.
	4	RTC24H	0	H0	R/W	–
	3	–	0	–	R	
	2	RTCADJ	0	H0	R/W	Cleared by setting the RTCCTL.RTCRST bit to 1.
	1	RTCRST	0	H0	R/W	–
	0	RTCRUN	0	H0	R/W	

Bit 15 RTCTRMBSY

This bit indicates whether the theoretical regulation is currently executed or not.
1 (R): Theoretical regulation is executing.
0 (R): Theoretical regulation has finished (or not executed).

This bit goes 1 when a value is written to the RTCCTL.RTCTRM[6:0] bits. The theoretical regulation takes up to 1 second for execution. This bit reverts to 0 automatically after the theoretical regulation has finished execution.

Bits 14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation. For a calculation method of correction value, refer to "Theoretical Regulation Function."

Notes:
- When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.
- Writing 0x00 to the RTCCTL.RTCTRM[6:0] bits sets the RTCCTL.RTCTRMBSY bit to 1 as well. However, no correcting operation is performed.

Bit 7 Reserved

Bit 6 RTCBSY

This bit indicates whether the counter is performing count-up operation or not.
1 (R): In count-up operation
0 (R): Idle (ready to rewrite real-time clock counter)

This bit goes 1 when performing 1-second count-up, +1 second correction, or 30-second correction. It retains 1 for 1/256 second and then reverts to 0.

Bit 5 RTCHLD

This bit halts the count-up operation of the real-time clock counter.
1 (R/W): Halt real-time clock counter count-up operation
0 (R/W): Normal operation

Writing 1 to this bit halts the count-up operation of the real-time clock counter, this makes it possible to read the counter value correctly without changing the counter. Write 0 to this bit to resume count-up operation immediately after the counter has been read. Depending on these operation timings, the +1 second correction may be executed after the count-up operation resumes. For more information on the +1 second correction, refer to "Real-Time Clock Counter Operations."

Note: When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCHLD bit cannot be rewritten to 1 (as fixed at 0).

Bit 4 RTC24H

This bit sets the hour counter to 24H mode or 12H mode.
1 (R/W): 24H mode
0 (R/W): 12H mode

This selection changes the count range of the hour counter. Note, however, that the counter value is not updated automatically, therefore, it must be programmed again.

Note: Be sure to avoid writing to this bit when the RTCCTL.RTCRUN bit = 1.

Bit 3 Reserved

Bit 2 RTCADJ

This bit executes the 30-second correction time adjustment function.
1 (W): Execute 30-second correction
0 (W): Ineffective
1 (R): 30-second correction is executing.
0 (R): 30-second correction has finished. (Normal operation)

Writing 1 to this bit executes 30-second correction and an enabled interrupt occurs even if the RTCCTL.RTCRUN bit = 0. The correction takes up to 2/256 seconds. The RTCCTL.RTCADJ bit is automatically cleared to 0 when the correction has finished. For more information on the 30-second correction, refer to "Real-Time Clock Counter Operations."

Notes: • Be sure to avoid writing to this bit when the RTCCTL.RTCBSY bit = 1.
• Do not write 1 to this bit again while the RTCCTL.RTCADJ bit = 1.

Bit 1 RTCRST

This bit resets the 1 Hz counter, the RTCCTL.RTCADJ bit, and the RTCCTL.RTCHLD bit.
1 (W): Reset
0 (W): Ineffective
1 (R): Reset is being executed.
0 (R): Reset has finished. (Normal operation)

This bit is automatically cleared to 0 after reset has finished.

Bit 0 RTCRUN

This bit starts/stops the real-time clock counter.
1 (R/W): Running/start control
0 (R/W): Idle/stop control

When the real-time clock counter stops counting by writing 0 to this bit, the counter retains the value when it stopped. Writing 1 to this bit again resumes counting from the value retained.

RTC Second Alarm Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCALM1	15	–	0	–	R	–
	14–12	RTCSHA[2:0]	0x0	H0	R/W	
	11–8	RTCSLA[3:0]	0x0	H0	R/W	
	7–0	–	0x00	–	R	

Bit 15 Reserved

Bits 14–12 RTCSHA[2:0]
Bits 11–8 RTCSLA[3:0]

The RTCALM1.RTCSHA[2:0] bits and the RTCALM1.RTCSLA[3:0] bits set the 10-second digit and 1-second digit of the alarm time, respectively. A value within 0 to 59 seconds can be set in BCD code as shown in Table 9.6.1.

Table 9.6.1 Setting Examples in BCD Code

Setting value in BCD code		Alarm (second) setting
RTCALM1.RTCSHA[2:0] bits	RTCALM1.RTCSLA[3:0] bits	
0x0	0x0	00 seconds
0x0	0x1	01 second
. . .	. . .	. . .
0x0	0x9	09 seconds
0x1	0x0	10 seconds
. . .	. . .	. . .
0x5	0x9	59 seconds

Bits 7–0 Reserved

RTC Hour/Minute Alarm Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCALM2	15	–	0	–	R	–
	14	RTCAPA	0	H0	R/W	
	13–12	RTCHHA[1:0]	0x0	H0	R/W	
	11–8	RTCHLA[3:0]	0x0	H0	R/W	
	7	–	0	–	R	
	6–4	RTCMIHA[2:0]	0x0	H0	R/W	
	3–0	RTCMILA[3:0]	0x0	H0	R/W	

Bit 15 Reserved

Bit 14 RTCAPA

This bit sets A.M. or P.M. of the alarm time in 12H mode (RTCCTL.RTC24H bit = 0).
1 (R/W): P.M.
0 (R/W): A.M.

This setting is ineffective in 24H mode (RTCCTL.RTC24H bit = 1).

Bits 13–12 RTCHHA[1:0]
Bits 11–8 RTCHLA[3:0]

The RTCALM2.RTCHHA[1:0] bits and the RTCALM2.RTCHLA[3:0] bits set the 10-hour digit and 1-hour digit of the alarm time, respectively. A value within 1 to 12 o'clock in 12H mode or 0 to 23 in 24H mode can be set in BCD code.

Bit 7 Reserved

Bits 6–4 RTCMIHA[2:0]
Bits 3–0 RTCMILA[3:0]

The RTCALM2.RTCMIHA[2:0] bits and the RTCALM2.RTCMILA[3:0] bits set the 10-minute digit and 1-minute digit of the alarm time, respectively. A value within 0 to 59 minutes can be set in BCD code.

RTC Stopwatch Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCSWCTL	15–12	BCD10[3:0]	0x0	H0	R	–
	11–8	BCD100[3:0]	0x0	H0	R	
	7–5	–	0x0	–	R	
	4	SWRST	0	H0	W	Read as 0.
	3–1	–	0x0	–	R	–
	0	SWRUN	0	H0	R/W	

Bits 15–12 BCD10[3:0]
Bits 11–8 BCD100[3:0]

The 1/10-second and 1/100-second digits of the stopwatch counter can be read as a BCD code from the RTCSWCTL.BCD10[3:0] bits and the RTCSWCTL.BCD100[3:0] bits, respectively.

Note: The counter value may not be read correctly while the stopwatch counter is running. The RTCSWCTL.BCD10[3:0]/BCD100[3:0] bits must be read twice and assume the counter value was read successfully if the two read results are the same.

Bits 7–5 Reserved

Bit 4 SWRST

This bit resets the stopwatch counter to 0x00.

1 (W): Reset
0 (W): Ineffective
0 (R): Always 0 when being read

When the stopwatch counter in running status is reset, it continues counting from count 0x00. The stopwatch counter retains 0x00 if it is reset in idle status.

Bits 3–1 Reserved

Bit 0 SWRUN

This bit starts/stops the stopwatch counter.

1 (R/W): Running/start control
0 (R/W): Idle/stop control

When the stopwatch counter stops counting by writing 0 to this bit, the counter retains the value when it stopped. Writing 1 to this bit again resumes counting from the value retained.

Note: The stopwatch counter stops in sync with the stopwatch clock after 0 is written to the RTCSWCTL.SWRUN bit. Therefore, the counter value may be incremented (+1) from the value at writing 0.

RTC Second/1Hz Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCSEC	15	–	0	–	R	–
	14–12	RTCSH[2:0]	0x0	H0	R/W	
	11–8	RTCSL[3:0]	0x0	H0	R/W	
	7	RTC1HZ	0	H0	R	Cleared by setting the RTCCTL.RTCRST bit to 1.
	6	RTC2HZ	0	H0	R	
	5	RTC4HZ	0	H0	R	
	4	RTC8HZ	0	H0	R	
	3	RTC16HZ	0	H0	R	
	2	RTC32HZ	0	H0	R	
	1	RTC64HZ	0	H0	R	
	0	RTC128HZ	0	H0	R	

Bit 15 Reserved

Bits 14–12 RTCSH[2:0]
Bits 11–8 RTCSL[3:0]

The RTCSEC.RTCSH[2:0] bits and the RTCSEC.RTCSL[3:0] bits are used to set and read the 10-second digit and the 1-second digit of the second counter, respectively. The setting/read values are a BCD code within the range from 0 to 59.

Note: Be sure to avoid writing to the RTCSEC.RTCSH[2:0]/RTCSL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

Bit 7 RTC1HZ
Bit 6 RTC2HZ
Bit 5 RTC4HZ
Bit 4 RTC8HZ
Bit 3 RTC16HZ
Bit 2 RTC32HZ
Bit 1 RTC64HZ
Bit 0 RTC128HZ

1 Hz counter data can be read from these bits.
The following shows the correspondence between the bit and frequency:
RTCSEC.RTC1HZ bit: 1 Hz
RTCSEC.RTC2HZ bit: 2 Hz
RTCSEC.RTC4HZ bit: 4 Hz
RTCSEC.RTC8HZ bit: 8 Hz
RTCSEC.RTC16HZ bit: 16 Hz
RTCSEC.RTC32HZ bit: 32 Hz
RTCSEC.RTC64HZ bit: 64 Hz
RTCSEC.RTC128HZ bit: 128 Hz

Note: The counter value may not be read correctly while the 1 Hz counter is running. These bits must be read twice and assume the counter value was read successfully if the two read results are the same.

RTC Hour/Minute Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCHUR	15	–	0	–	R	–
	14	RTCAP	0	H0	R/W	
	13–12	RTCHH[1:0]	0x1	H0	R/W	
	11–8	RTCHL[3:0]	0x2	H0	R/W	
	7	–	0	–	R	
	6–4	RTCMIH[2:0]	0x0	H0	R/W	
	3–0	RTCMIL[3:0]	0x0	H0	R/W	

Bit 15 Reserved

Bit 14 RTCAP

This bit is used to set and read A.M. or P.M. data in 12H mode (RTCCTL.RTC24H bit = 0).
1 (R/W): P.M.
0 (R/W): A.M.

In 24H mode (RTCCTL.RTC24H bit = 1), this bit is fixed at 0 and writing 1 is ignored. However, if the RTCHUR.RTCAP bit = 1 when changed to 24H mode, it goes 0 at the next count-up timing of the hour counter.

Bits 13–12 RTCHH[1:0]
Bits 11–8 RTCHL[3:0]

The RTCHUR.RTCHH[1:0] bits and the RTCHUR.RTCHL[3:0] bits are used to set and read the 10-hour digit and the 1-hour digit of the hour counter, respectively. The setting/read values are a BCD code within the range from 1 to 12 in 12H mode or 0 to 23 in 24H mode.

Note: Be sure to avoid writing to the RTCHUR.RTCHH[1:0]/RTCHL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

Bit 7 Reserved

Bits 6–4 RTCMIH[2:0]
Bits 3–0 RTCMIL[3:0]

The RTCHUR.RTCMIH[2:0] bits and the RTCHUR.RTCMIL[3:0] bits are used to set and read the 10-minute digit and the 1-minute digit of the minute counter, respectively. The setting/read values are a BCD code within the range from 0 to 59.

Note: Be sure to avoid writing to the RTCHUR.RTCMIH[2:0]/RTCMIL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Month/Day Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCMON	15–13	–	0x0	–	R	–
	12	RTCMOH	0	H0	R/W	
	11–8	RTCMOL[3:0]	0x1	H0	R/W	
	7–6	–	0x0	–	R	
	5–4	RTCDH[1:0]	0x0	H0	R/W	
	3–0	RTCDL[3:0]	0x1	H0	R/W	

Bits 15–13 Reserved

Bit 12 RTCMOH
Bits 11–8 RTCMOL[3:0]

The RTCMON.RTCMOH bit and the RTCMON.RTCMOL[3:0] bits are used to set and read the 10-month digit and the 1-month digit of the month counter, respectively. The setting/read values are a BCD code within the range from 1 to 12.

Notes:
- Be sure to avoid writing to the RTCMON.RTCMOH/RTCMOL[3:0] bits while the RTCCTL.RTCBSY bit = 1.
- Be sure to avoid setting the RTCMON.RTCMOH/RTCMOL[3:0] bits to 0x00.

Bits 7–6 Reserved

Bits 5–4 RTCDH[1:0]
Bits 3–0 RTCDL[3:0]

The RTCMON.RTCDH[1:0] bits and the RTCMON.RTCDL[3:0] bits are used to set and read the 10-day digit and the 1-day digit of the day counter, respectively. The setting/read values are a BCD code within the range from 1 to 31 (to 28 for February in a common year, to 29 for February in a leap year, or to 30 for April/June/September/November).

Note: Be sure to avoid writing to the RTCMON.RTCDH[1:0]/RTCDL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Year/Week Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCYAR	15–11	–	0x00	–	R	–
	10–8	RTCWK[2:0]	0x0	H0	R/W	
	7–4	RTCYH[3:0]	0x0	H0	R/W	
	3–0	RTCYL[3:0]	0x0	H0	R/W	

Bits 15–11 Reserved

Bits 10–8 RTCWK[2:0]

These bits are used to set and read day of the week.
The day of the week counter is a base-7 counter and the setting/read values are 0x0 to 0x6. Table 9.6.2 lists the correspondence between the count value and day of the week.

Table 9.6.2 Correspondence between the count value and day of the week

RTCYAR.RTCWK[2:0] bits	Day of the week
0x6	Saturday
0x5	Friday
0x4	Thursday
0x3	Wednesday
0x2	Tuesday
0x1	Monday
0x0	Sunday

Note: Be sure to avoid writing to the RTCYAR.RTCWK[2:0] bits while the RTCCTL.RTCBSY bit = 1.

Bits 7–4 RTCYH[3:0]
Bits 3–0 RTCYL[3:0]

The RTCYAR.RTCYH[3:0] bits and the RTCYAR.RTCYL[3:0] bits are used to set and read the 10-year digit and the 1-year digit of the year counter, respectively. The setting/read values are a BCD code within the range from 0 to 99.

Note: Be sure to avoid writing to the RTCYAR.RTCYH[3:0]/RTCYL[3:0] bits while the RTCCTL.RTCBSY bit = 1.

RTC Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCINTF	15	RTCTRMIF	0	H0	R/W	Cleared by writing 1.
	14	SW1IF	0	H0	R/W	
	13	SW10IF	0	H0	R/W	
	12	SW100IF	0	H0	R/W	
	11–9	–	0x0	–	R	–
	8	ALARMIF	0	H0	R/W	Cleared by writing 1.
	7	1DAYIF	0	H0	R/W	
	6	1HURIF	0	H0	R/W	
	5	1MINIF	0	H0	R/W	
	4	1SECIF	0	H0	R/W	
	3	1_2SECIF	0	H0	R/W	
	2	1_4SECIF	0	H0	R/W	
	1	1_8SECIF	0	H0	R/W	
	0	1_32SECIF	0	H0	R/W	

Bit 15 RTCTRMIF
Bit 14 SW1IF
Bit 13 SW10IF
Bit 12 SW100IF

These bits indicate the real-time clock interrupt cause occurrence status.

1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
RTCINTF.RTCTRMIF bit: Theoretical regulation completion interrupt
RTCINTF.SW1IF bit: Stopwatch 1 Hz interrupt
RTCINTF.SW10IF bit: Stopwatch 10 Hz interrupt
RTCINTF.SW100IF bit: Stopwatch 100 Hz interrupt

Bits 11–9 Reserved

Bit 8 ALARMIF
Bit 7 1DAYIF
Bit 6 1HURIF
Bit 5 1MINIF
Bit 4 1SECIF
Bit 3 1_2SECIF
Bit 2 1_4SECIF
Bit 1 1_8SECIF
Bit 0 1_32SECIF

These bits indicate the real-time clock interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
RTCINTF. ALARMIF bit: Alarm interrupt
RTCINTF.1DAYIF bit: 1-day interrupt
RTCINTF.1HURIF bit: 1-hour interrupt
RTCINTF.1MINIF bit: 1-minute interrupt
RTCINTF.1SECIF bit: 1-second interrupt
RTCINTF.1_2SECIF bit: 1/2-second interrupt
RTCINTF.1_4SECIF bit: 1/4-second interrupt
RTCINTF.1_8SECIF bit: 1/8-second interrupt
RTCINTF.1_32SECIF bit: 1/32-second interrupt

RTC Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
RTCINTE	15	RTCTRMIE	0	H0	R/W	–
	14	SW1IE	0	H0	R/W	
	13	SW10IE	0	H0	R/W	
	12	SW100IE	0	H0	R/W	
	11–9	–	0x0	–	R	
	8	ALARMIE	0	H0	R/W	
	7	1DAYIE	0	H0	R/W	
	6	1HURIE	0	H0	R/W	
	5	1MINIE	0	H0	R/W	
	4	1SECIE	0	H0	R/W	
	3	1_2SECIE	0	H0	R/W	
	2	1_4SECIE	0	H0	R/W	
	1	1_8SECIE	0	H0	R/W	
	0	1_32SECIE	0	H0	R/W	

Bit 15 RTCTRMIE
Bit 14 SW1IE
Bit 13 SW10IE
Bit 12 SW100IE

These bits enable real-time clock interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
RTCINTE.RTCTRMIE bit: Theoretical regulation completion interrupt
RTCINTE.SW1IE bit: Stopwatch 1 Hz interrupt
RTCINTE.SW10IE bit: Stopwatch 10 Hz interrupt
RTCINTE.SW100IE bit: Stopwatch 100 Hz interrupt

Bits 11–9 Reserved

Bit 8 ALARMIE
Bit 7 1DAYIE
Bit 6 1HURIE
Bit 5 1MINIE
Bit 4 1SECIE
Bit 3 1_2SECIE
Bit 2 1_4SECIE
Bit 1 1_8SECIE
Bit 0 1_32SECIE

These bits enable real-time clock interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
RTCINTE.ALARMIE bit: Alarm interrupt
RTCINTE.1DAYIE bit: 1-day interrupt
RTCINTE.1HURIE bit: 1-hour interrupt
RTCINTE.1MINIE bit: 1-minute interrupt
RTCINTE.1SECIE bit: 1-second interrupt
RTCINTE.1_2SECIE bit: 1/2-second interrupt
RTCINTE.1_4SECIE bit: 1/4-second interrupt
RTCINTE.1_8SECIE bit: 1/8-second interrupt
RTCINTE.1_32SECIE bit: 1/32-second interrupt

10 Supply Voltage Detector (SVD)

10.1 Overview

SVD is a supply voltage detector to monitor the power supply voltage applied to an external pin. The main features are listed below.

- Power supply voltage to be detected: External power supply (EXSVD)
- Detectable voltage level: Selectable from among 20 levels (1.8 to 3.7 V)
- Detection results:
  - Can be read whether the power supply voltage is lower than the detection voltage level or not.
  - Can generate an interrupt or a reset when low power supply voltage is detected.
- Interrupt: 1 system (Low power supply voltage detection interrupt)
- Supports intermittent operations:
  - Three detection cycles are selectable.
  - Low power supply voltage detection count function to generate an interrupt/reset when low power supply voltage is successively detected the number of times specified.
  - Continuous operation is also possible.

Figure 10.1.1 shows the configuration of SVD.

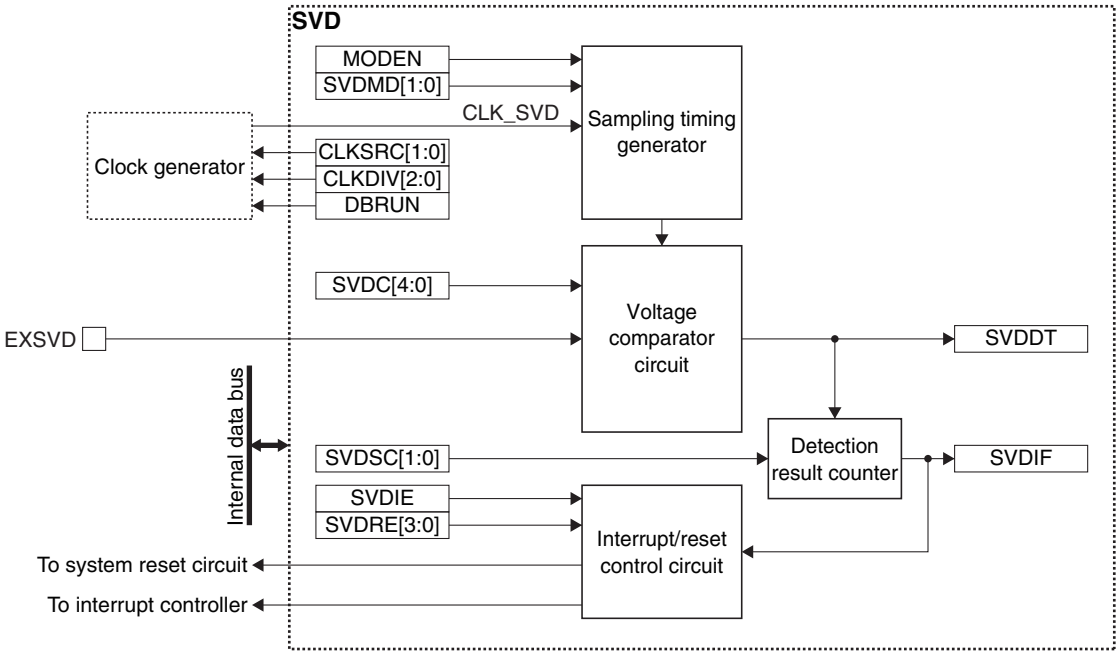


Figure 10.1.1 SVD Configuration

10.2 Input Pin and External Connection

10.2.1 Input Pin

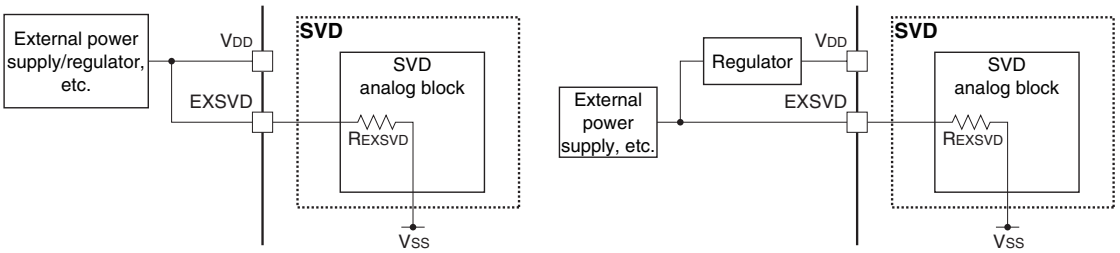
Table 10.2.1.1 shows the SVD input pin.

Table 10.2.1.1 SVD Input Pin

Pin name	I/O	Initial status	Function
EXSVD	A	I	External power supply voltage detection pin

Note: Do not leave the EXSVD pin open even if SVD is not used.

10.2.2 External Connection



(1) When detecting the voltage supplied to the VDD pin (2) When detecting an external power supply voltage

Figure 10.2.2.1 Connection between EXSVD Pin and External Power Supply

For the EXSVD pin input voltage range and the EXSVD input impedance, refer to "Supply Voltage Detector Characteristics" in the "Electrical Characteristics" chapter.

10.3 Clock Settings

10.3.1 SVD Operating Clock

When using SVD, the SVD operating clock CLK_SVD must be supplied to SVD from the clock generator.
The CLK_SVD supply should be controlled as in the procedure shown below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
3. Set the following SVDCLK register bits:
   - SVDCLK.CLKSRC[1:0] bits (Clock source selection)
   - SVDCLK.CLKDIV[2:0] bits (Clock division ratio selection = Clock frequency setting)
4. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

The CLK_SVD frequency should be set to around 32 kHz.

10.3.2 Clock Supply in SLEEP Mode

When using SVD during SLEEP mode, the SVD operating clock CLK_SVD must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_SVD clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_SVD clock source is 1, the CLK_SVD clock source is deactivated during SLEEP mode and SVD stops with the register settings maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_SVD is supplied and the SVD operation resumes.

10.3.3 Clock Supply in DEBUG Mode

The CLK_SVD supply during DEBUG mode should be controlled using the SVDCLK.DBRUN bit.
The CLK_SVD supply to SVD is suspended when the CPU enters DEBUG mode if the SVDCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_SVD supply resumes. Although SVD stops operating when the CLK_SVD supply is suspended, the registers retain the status before DEBUG mode was entered.
If the SVDCLK.DBRUN bit = 1, the CLK_SVD supply is not suspended and SVD will keep operating in DEBUG mode.

10.4 Operations

10.4.1 SVD Control

Starting detection

SVD should be initialized and activated with the procedure listed below.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Configure the operating clock using the SVDCLK.CLKSRC[1:0] and SVDCLK.CLKDIV[2:0] bits.
3. Set the following SVDCTL register bits:
   - SVDCTL.SVDSC[1:0] bits (Set low power supply voltage detection counter)
   - SVDCTL.SVDC[4:0] bits (Set SVD detection voltage V_{SVD})
   - SVDCTL.SVDRE[3:0] bits (Select reset/interrupt mode)
   - SVDCTL.SVDMD[1:0] bits (Set intermittent operation mode)
4. Set the following bits when using the interrupt:
   - Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
   - Set the SVDINTE.SVDIE bit to 1. (Enable SVD interrupt)
5. Set the SVDCTL.MODEN bit to 1. (Enable SVD detection)
6. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Terminating detection

Follow the procedure shown below to stop SVD operation.

1. Write 0x0096 to the MSCPROT.PROT[15:0] bits. (Remove system protection)
2. Write 0 to the SVDCTL.MODEN bit. (Disable SVD detection)
3. Write a value other than 0x0096 to the MSCPROT.PROT[15:0] bits. (Set system protection)

Reading detection results

The following two detection results can be obtained by reading the SVDINTF.SVDDT bit:

- Power supply voltage (EXSVD) ≥ SVD detection voltage V_{SVD} when SVDINTF.SVDDT bit = 0
- Power supply voltage (EXSVD) < SVD detection voltage V_{SVD} when SVDINTF.SVDDT bit = 1

Before reading the SVDINTF.SVDDT bit, wait for at least SVD circuit enable response time after 1 is written to the SVDCTL.MODEN bit (refer to "Supply Voltage Detector Characteristics, SVD circuit enable response time t_{SVDEN}" in the "Electrical Characteristics" chapter).
After the SVDCTL.SVDC[4:0] bits setting value is altered to change the SVD detection voltage V_{SVD} when the SVDCTL.MODEN bit = 1, wait for at least SVD circuit response time before reading the SVDINTF.SVDDT bit (refer to "Supply Voltage Detector Characteristics, SVD circuit response time t_{SVD}" in the "Electrical Characteristics" chapter).

10.4.2 SVD Operations

Continuous operation mode

SVD operates in continuous operation mode by default (SVDCTL.SVDMD[1:0] bits = 0x0). In this mode, SVD operates continuously while the SVDCTL.MODEN bit is set to 1 and it keeps loading the detection results to the SVDINTF.SVDDT bit. During this period, the current detection results can be obtained by reading the SVDINTF.SVDDT bit as necessary. Furthermore, an interrupt (if the SVDCTL.SVDRE[3:0] bits ≠ 0xa) or a reset (if the SVDCTL.SVDRE[3:0] bits = 0xa) can be generated when the SVDINTF.SVDDT bit is set to 1 (low power supply voltage is detected). This mode can keep detecting power supply voltage drop after the voltage detection masking time has elapsed even if the IC is placed into SLEEP status or accidental clock stoppage has occurred.

Intermittent operation mode

SVD operates in intermittent operation mode when the SVDCTL.SVDMD[1:0] bits are set to 0x1 to 0x3. In this mode, SVD turns on at an interval set using the SVDCTL.SVDMD[1:0] bits to perform detection operation and then it turns off while the SVDCTL.MODEN bit is set to 1. During this period, the latest detection results can be obtained by reading the SVDINTF.SVDDT bit as necessary. Furthermore, an interrupt or a reset can be generated when SVD has successively detected low power supply voltage the number of times specified by the SVDCTL.SVDSC[1:0] bits.

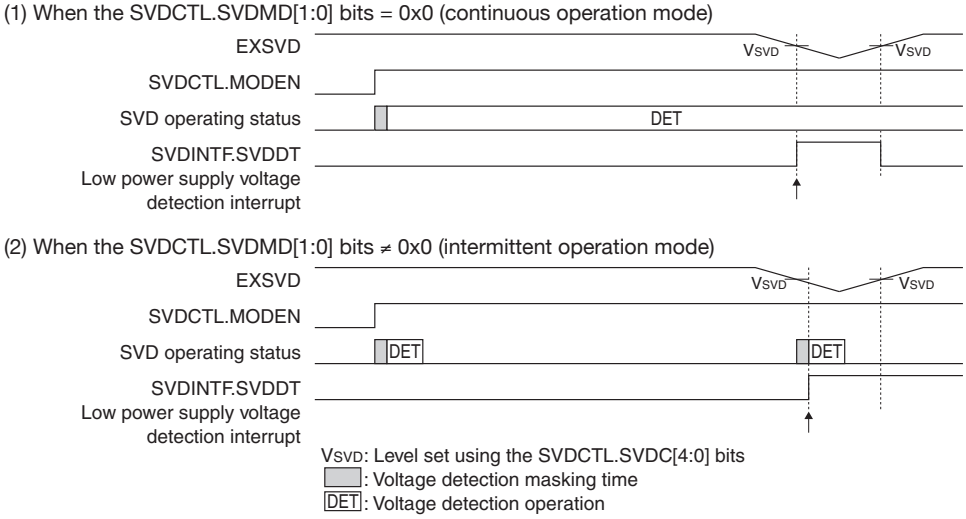


Figure 10.4.2.1 SVD Operations

10.5 SVD Interrupt and Reset

10.5.1 SVD Interrupt

Setting the SVDCTL.SVDRE[3:0] bits to a value other than 0xa allows use of the low power supply voltage detection interrupt function.

Table 10.5.1.1 Low Power Supply Voltage Detection Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Low power supply voltage detection	SVDINTF.SVDIF	In continuous operation mode When the SVDINTF.SVDDT bit is 1 In intermittent operation mode When low power supply voltage is successively detected the specified number of times	Writing 1

SVD provides the interrupt enable bit (SVDINTE.SVDIE bit) corresponding to the interrupt flag (SVDINTF.SVDIF bit). An interrupt request is sent to the interrupt controller only when the SVDINTF.SVDIF bit is set while the interrupt is enabled by the SVDINTE.SVDIE bit. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

Once the SVDINTF.SVDIF bit is set, it will not be cleared even if the power supply voltage subsequently returns to a value exceeding the SVD detection voltage VSVD. An interrupt may occur due to a temporary power supply voltage drop, check the power supply voltage status by reading the SVDINTF.SVDDT bit in the interrupt handler routine.

10.5.2 SVD Reset

Setting the SVDCTL.SVDRE[3:0] bits to 0xa allows use of the SVD reset issuance function.
The reset issuing timing is the same as that of the SVDINTF.SVDIF bit being set when a low voltage is detected.
After a reset has been issued, SVD enters continuous operation mode even if it was operating in intermittent operation mode, and continues operating.
If the power supply voltage reverts to the normal level, the SVDINTF.SVDDT bit goes 0 and the reset state is canceled. After that, SVD resumes operating in the operation mode set previously via the initialization routine.
During reset state, the SVD control bits are set as shown in Table 10.5.2.1.

Table 10.5.2.1 SVD Control Bits During Reset State

Control register	Control bit	Setting
SVDCLK	DBRUN	Reset to the initial values.
	CLKDIV[2:0]	
	CLKSRC[1:0]	
SVDCTL	SVDSC[1:0]	Cleared to 0. (The set value becomes invalid as SVD enters continuous operation mode.)
	SVDC[4:0]	The set value is retained.
	SVDRE[3:0]	The set value (0xa) is retained.
	SVDMD[1:0]	Cleared to 0 to set continuous operation mode.
	MODEN	The set value (1) is retained.
SVDINTF	SVDIF	The status (1) before being reset is retained.
SVDINTE	SVDIE	Cleared to 0.

10.6 Control Registers

SVD Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDCLK	15–9	–	0x00	–	R	–
	8	DBRUN	1	H0	R/WP	
	7	–	0	–	R	
	6–4	CLKDIV[2:0]	0x0	H0	R/WP	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/WP	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the SVD operating clock is supplied in DEBUG mode or not.
1 (R/WP): Clock supplied in DEBUG mode
0 (R/WP): No clock supplied in DEBUG mode

Bit 7 Reserved

Bits 6–4 CLKDIV[2:0]

These bits select the division ratio of the SVD operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of SVD.

Table 10.6.1 Clock Source and Division Ratio Settings

SVDCLK.CLKDIV[2:0] bits	SVDCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x6, 0x7	Reserved	1/1	Reserved	1/1
0x5	1/512		1/512	
0x4	1/256		1/256	
0x3	1/128		1/128	
0x2	1/64		1/64	
0x1	1/32		1/32	
0x0	1/16		1/16	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The clock frequency should be set to around 32 kHz.

SVD Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDCTL	15	–	0	–	R	–
	14–13	SVDSC[1:0]	0x0	H0	R/WP	Writing takes effect when the SVDCTL.SVDMD[1:0] bits are not 0x0.
	12–8	SVDC[4:0]	0x1e	H1	R/WP	–
	7–4	SVDRE[3:0]	0x0	H1	R/WP	
	3	–	0	–	R	
	2–1	SVDMD[1:0]	0x0	H0	R/WP	
	0	MODEN	0	H1	R/WP	

Bit 15 Reserved

Bits 14–13 SVDSC[1:0]

These bits set the condition to generate an interrupt/reset (number of successive low voltage detections) in intermittent operation mode (SVDCTL.SVDMD[1:0] bits = 0x1 to 0x3).

Table 10.6.2 Interrupt/Reset Generating Condition in Intermittent Operation Mode

SVDCTL.SVDSC[1:0] bits	Interrupt/reset generating condition
0x3	Low power supply voltage is successively detected eight times.
0x2	Low power supply voltage is successively detected four times.
0x1	Low power supply voltage is successively detected twice.
0x0	Low power supply voltage is successively detected once.

This setting is ineffective in continuous operation mode (SVDCTL.SVDMD[1:0] bits = 0x0).

Bits 12–8 SVDC[4:0]

These bits select an SVD detection voltage V_{SVD} for detecting low voltage from among 30 levels.

Table 10.6.3 Setting of SVD Detection Voltage V_{SVD}

SVDCTL.SVDC[4:0] bits	SVD detection voltage V_{SVD} [V]
0x1f	High
0x1e	↑
0x1d	
:	
0x0d	↓
0x0c	Low
0x0b–0x00	Use prohibited

For more information, refer to “Supply Voltage Detector Characteristics, SVD detection voltage V_{SVD}” in the “Electrical Characteristics” chapter.

Bits 7–4 SVDRE[3:0]

These bits enable/disable the reset issuance function when a low power supply voltage is detected.
0xa (R/WP): Enable (Issue reset)
Other than 0xa (R/WP): Disable (Generate interrupt)

For more information on the SVD reset issuance function, refer to "SVD Reset."

Bit 3 Reserved

Bits 2–1 SVDMD[1:0]

These bits select intermittent operation mode and its detection cycle.

Table 10.6.4 Intermittent Operation Mode Detection Cycle Selection

SVDCTL.SVDMD[1:0] bits	Operation mode (detection cycle)
0x3	Intermittent operation mode (CLK_SVD/512)
0x2	Intermittent operation mode (CLK_SVD/256)
0x1	Intermittent operation mode (CLK_SVD/128)
0x0	Continuous operation mode

For more information on intermittent and continuous operation modes, refer to "SVD Operations."

Bit 0 MODEN

This bit enables/disables for the SVD circuit to operate.
1 (R/WP): Enable (Start detection operations)
0 (R/WP): Disable (Stop detection operations)

After this bit has been altered, wait until the value written is read out from this bit without subsequent operations being performed.

Notes: • Writing 0 to the SVDCTL.MODEN bit resets the SVD hardware. However, the register values set and the interrupt flag are not cleared. The SVDCTL.MODEN bit is actually set to 0 after this processing has finished. If 1 is written to the SVDCTL.MODEN bit continuously without waiting for the bit being read as 0 at this time, writing 0 may be ignored and a malfunction may occur as the hardware restarts without resetting.

• The SVD internal circuit is initialized if the SVDCTL.SVDSC[1:0] bits, SVDCTL.SVDRE[3:0] bits, or SVDCTL.SVDMD[1:0] bits are altered while SVD is in operation after 1 is written to the SVDCTL.MODEN bit.

SVD Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDINTF	15–9	–	0x00	–	R	–
	8	SVDDT	x	–	R	
	7–1	–	0x00	–	R	
	0	SVDIF	0	H1	R/W	Cleared by writing 1.

Bits 15–9 Reserved

Bit 8 SVDDT

The power supply voltage detection results can be read out from this bit.
1 (R): Power supply voltage (EXSVD) < SVD detection voltage V_{SVD}
0 (R): Power supply voltage (EXSVD) ≥ SVD detection voltage V_{SVD}

Bits 7–1 Reserved

Bit 0 SVDIF

This bit indicates the low power supply voltage detection interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

Note: The SVD internal circuit is initialized if the interrupt flag is cleared while SVD is in operation after 1 is written to the SVDCTL.MODEN bit.

SVD Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SVDINTE	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	SVDIE	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 SVDIE

This bit enables low power supply voltage detection interrupts.

1 (R/W): Enable interrupts

0 (R/W): Disable interrupts

Notes: • If the SVDCTL.SVDRE[3:0] bits are set to 0xa, no low power supply voltage detection interrupt will occur, as a reset is issued at the same timing as an interrupt.

• To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

11 16-bit Timers (T16)

11.1 Overview

T16 is a 16-bit timer. The features of T16 are listed below.

- 16-bit presettable down counter
- Provides a reload data register for setting the preset value.
- A clock source and clock division ratio for generating the count clock are selectable.
- Repeat mode or one-shot mode is selectable.
- Can generate counter underflow interrupts.

Figure 11.1.1 shows the configuration of a T16 channel.

Table 11.1.1 T16 Channel Configuration of S1C17589

Item	S1C17589
Number of channels	6 channels (Ch.0–Ch.5)
Event counter function	Not supported (No EXCL*m* pins are provided.)
Peripheral clock output (Outputs the counter underflow signal.)	Ch.1 → Synchronous serial interface Ch.0 master clock Ch.2 → Synchronous serial interface Ch.1 master clock Ch.3 → 10-bit A/D converter Ch.0 trigger signal Ch.4 → 10-bit A/D converter Ch.1 trigger signal

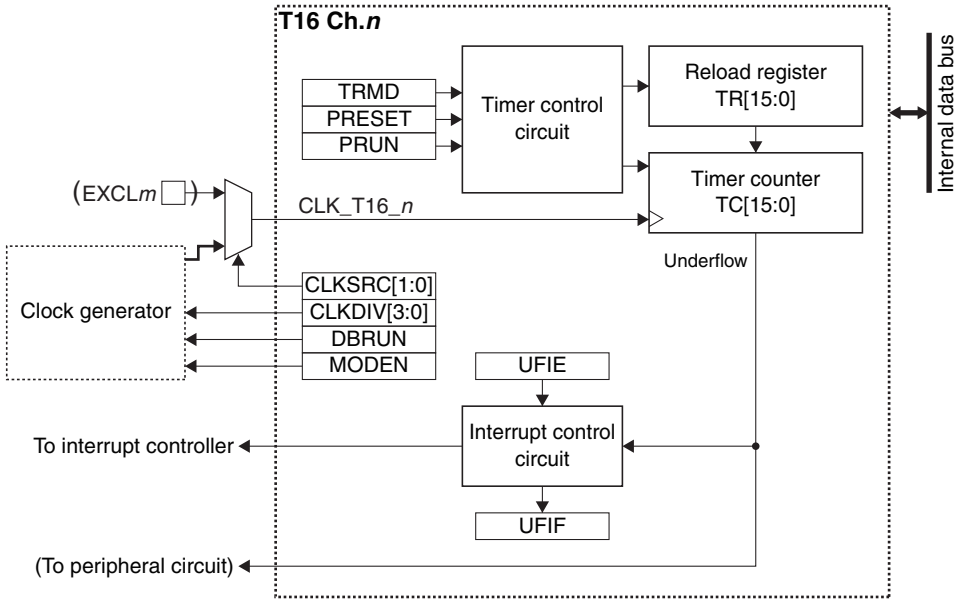


Figure 11.1.1 Configuration of a T16 Channel

11.2 Input Pin

Table 11.2.1 shows the T16 input pin.

Table 11.2.1 T16 Input Pin

Pin name	I/O*	Initial status*	Function
EXCL*m*	I	I (Hi-Z)	External event signal input pin

* Indicates the status when the pin is configured for T16.

If the port is shared with the EXCL*m* pin and other functions, the EXCL*m* input function must be assigned to the port before using the event counter function. The EXCL*m* signal can be input through the chattering filter. For more information, refer to the "I/O Ports" chapter.

11.3 Clock Settings

11.3.1 T16 Operating Clock

When using T16 Ch.*n*, the T16 Ch.*n* operating clock CLK_T16_*n* must be supplied to T16 Ch.*n* from the clock generator. The CLK_T16_*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following T16_*n*CLK register bits:
   - T16_*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - T16_*n*CLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)

11.3.2 Clock Supply in SLEEP Mode

When using T16 during SLEEP mode, the T16 operating clock CLK_T16_*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_T16_*n* clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_T16_*n* clock source is 1, the CLK_T16_*n* clock source is deactivated during SLEEP mode and T16 stops with the register settings and counter value maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_T16_*n* is supplied and the T16 operation resumes.

11.3.3 Clock Supply in DEBUG Mode

The CLK_T16_*n* supply during DEBUG mode should be controlled using the T16_*n*CLK.DBRUN bit.
The CLK_T16_*n* supply to T16 Ch.*n* is suspended when the CPU enters DEBUG mode if the T16_*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_T16_*n* supply resumes. Although T16 Ch.*n* stops operating when the CLK_T16_*n* supply is suspended, the counter and registers retain the status before DEBUG mode was entered. If the T16_*n*CLK.DBRUN bit = 1, the CLK_T16_*n* supply is not suspended and T16 Ch.*n* will keep operating in DEBUG mode.

11.3.4 Event Counter Clock

The channel that supports the event counter function counts down at the rising edge of the EXCL*m* pin input signal when the T16_*n*CLK.CLKSRC[1:0] bits are set to 0x3.

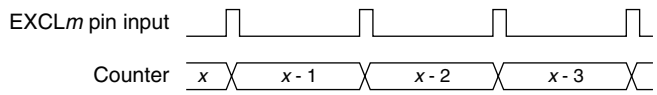


Figure 11.3.4.1 Count Down Timing

Note that the EXOSC clock is selected for the channel that does not support the event counter function.

11.4 Operations

11.4.1 Initialization

T16 Ch.*n* should be initialized and started counting with the procedure shown below.

1. Configure the T16 Ch.*n* operating clock (see "T16 Operating Clock").
2. Set the T16_*n*CTL.MODEN bit to 1. (Enable count operation clock)
3. Set the T16_*n*MOD.TRMD bit. (Select operation mode (Repeat mode or One-shot mode))
4. Set the T16_*n*TR register. (Set reload data (counter preset data))
5. Set the following bits when using the interrupt:
   - Write 1 to the T16_*n*INTF.UFIF bit. (Clear interrupt flag)
   - Set the T16_*n*INTE.UFIE bit to 1. (Enable underflow interrupt)

6. Set the following T16_*n*CTL register bits:
   - Set the T16_*n*CTL.PRESET bit to 1. (Preset reload data to counter)
   - Set the T16_*n*CTL.PRUN bit to 1. (Start counting)

11.4.2 Counter Underflow

Normally, the T16 counter starts counting down from the reload data value preset and generates an underflow signal when an underflow occurs. This signal is used to generate an interrupt and may be output to a specific peripheral circuit as a clock (T16 Ch.*n* must be set to repeat mode to generate a clock). The underflow cycle is determined by the T16 Ch.*n* operating clock setting and reload data (counter initial value) set in the T16_*n*TR register.
The following shows the equations to calculate the underflow cycle and frequency:

$$T = \frac{TR + 1}{f_{CLK\_T16\_n}} \qquad fr = \frac{f_{CLK\_T16\_n}}{TR + 1} \qquad \text{(Eq. 11.1)}$$

Where

T: Underflow cycle [s]
fr: Underflow frequency [Hz]
TR: T16_*n*TR register setting
$f_{CLK\_T16\_n}$: T16 Ch.*n* operating clock frequency [Hz]

11.4.3 Operations in Repeat Mode

T16 Ch.*n* enters repeat mode by setting the T16_*n*MOD.TRMD bit to 0.
In repeat mode, the count operation starts by writing 1 to the T16_*n*CTL.PRUN bit and continues until 0 is written. A counter underflow presets the T16_*n*TR register value to the counter, so underflow occurs periodically. Select this mode to generate periodic underflow interrupts or when using the timer to output a trigger/clock to the peripheral circuit.

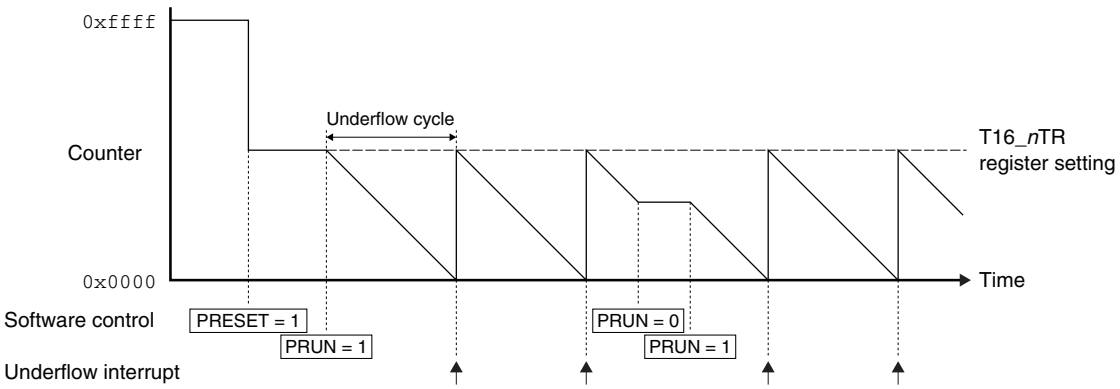


Figure 11.4.3.1 Count Operations in Repeat Mode

11.4.4 Operations in One-shot Mode

T16 Ch.*n* enters one-shot mode by setting the T16_*n*MOD.TRMD bit to 1.
In one-shot mode, the count operation starts by writing 1 to the T16_*n*CTL.PRUN bit and stops after the T16_*n*TR register value is preset to the counter when an underflow has occurred. At the same time the counter stops, the T16_*n*CTL.PRUN bit is cleared automatically. Select this mode to stop the counter after an interrupt has occurred once, such as for checking a specific lapse of time.

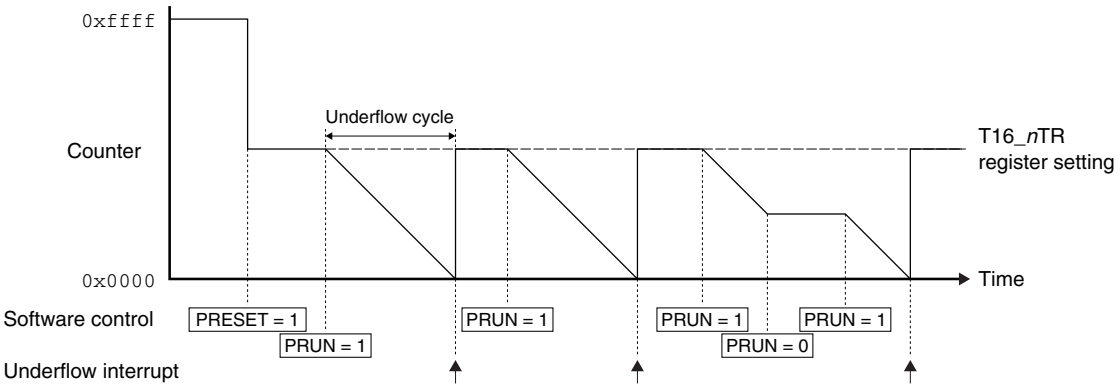


Figure 11.4.4.1 Count Operations in One-shot Mode

11.4.5 Counter Value Read

The counter value can be read out from the T16_*n*TC.TC[15:0] bits. However, since T16 operates on CLK_T16_*n*, one of the operations shown below is required to read correctly by the CPU.

- Read the counter value twice or more and check to see if the same value is read.
- Stop the timer and then read the counter value.

11.5 Interrupt

Each T16 channel has a function to generate the interrupt shown in Table 11.5.1.

Table 11.5.1 T16 Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Underflow	T16_*n*INTF.UFIF	When the counter underflows	Writing 1

T16 provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

11.6 Control Registers

T16 Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–4	CLKDIV[3:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the T16 Ch.*n* operating clock is supplied in DEBUG mode or not.
1 (R/W): Clock supplied in DEBUG mode
0 (R/W): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the T16 Ch.*n* operating clock (counter clock).

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of T16 Ch.*n*.

Table 11.6.1 Clock Source and Division Ratio Settings

T16_*n*CLK.CLKDIV[3:0] bits	T16_*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC/EXCL*m*
0xf	1/32,768	1/1	1/32,768	1/1
0xe	1/16,384		1/16,384	
0xd	1/8,192		1/8,192	
0xc	1/4,096		1/4,096	
0xb	1/2,048		1/2,048	
0xa	1/1,024		1/1,024	
0x9	1/512		1/512	
0x8	1/256	1/256	1/256	
0x7	1/128	1/128	1/128	
0x6	1/64	1/64	1/64	
0x5	1/32	1/32	1/32	
0x4	1/16	1/16	1/16	
0x3	1/8	1/8	1/8	
0x2	1/4	1/4	1/4	
0x1	1/2	1/2	1/2	
0x0	1/1	1/1	1/1	

(Note 1) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.
(Note 2) When the T16_*n*CLK.CLKSRC[1:0] bits are set to 0x3, EXCL*m* is selected for the channel with an event counter function or EXOSC is selected for other channels.

T16 Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*MOD	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	TRMD	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 TRMD

This bit selects the T16 operation mode.
1 (R/W): One-shot mode
0 (R/W): Repeat mode

For detailed information on the operation mode, refer to "Operations in One-shot Mode" and "Operations in Repeat Mode."

T16 Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*CTL	15–9	–	0x00	–	R	–
	8	PRUN	0	H0	R/W	
	7–2	–	0x00	–	R	
	1	PRESET	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–9 Reserved

Bit 8 PRUN

This bit starts/stops the timer.
1 (W): Start timer
0 (W): Stop timer
1 (R): Timer is running
0 (R): Timer is idle

By writing 1 to this bit, the timer starts count operations. However, the T16_*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance. While the timer is running, writing 0 to this bit stops count operations. When the counter stops due to a counter underflow in one-shot mode, this bit is automatically cleared to 0.

Bits 7–2 Reserved

Bit 1 PRESET

This bit presets the reload data stored in the T16_*n*TR register to the counter.

1 (W): Preset
0 (W): Ineffective
1 (R): Presetting in progress
0 (R): Presetting finished or normal operation

By writing 1 to this bit, the timer presets the T16_*n*TR register value to the counter. However, the T16_*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance. This bit retains 1 during presetting and is automatically cleared to 0 after presetting has finished.

Bit 0 MODEN

This bit enables the T16 Ch.*n* operations.

1 (R/W): Enable (Start supplying operating clock)
0 (R/W): Disable (Stop supplying operating clock)

T16 Ch.*n* Reload Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*TR	15–0	TR[15:0]	0xffff	H0	R/W	–

Bits 15–0 TR[15:0]

These bits are used to set the initial value to be preset to the counter.
The value set to this register will be preset to the counter when 1 is written to the T16_*n*CTL.PRESET bit or when the counter underflows.

Notes:
- The T16_*n*TR register cannot be altered while the timer is running (T16_*n*CTL.PRUN bit = 1), as an incorrect initial value may be preset to the counter.
- When one-shot mode is set, the T16_*n*TR.TR[15:0] bits should be set to a value equal to or greater than 0x0001.

T16 Ch.*n* Counter Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*TC	15–0	TC[15:0]	0xffff	H0	R	–

Bits 15–0 TC[15:0]

The current counter value can be read out from these bits.

T16 Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*INTF	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	UFIF	0	H0	R/W	Cleared by writing 1.

Bits 15–1 Reserved

Bit 0 UFIF

This bit indicates the T16 Ch.*n* underflow interrupt cause occurrence status.

1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

T16 Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16_*n*INTE	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	UFIE	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 UFIE

This bit enables T16 Ch.*n* underflow interrupts.

1 (R/W): Enable interrupts

0 (R/W): Disable interrupts

Note: To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

12 UART (UART)

12.1 Overview

The UART is an asynchronous serial interface. The features of the UART are listed below.

- Includes a baud rate generator for generating the transfer clock.
- Supports 7- and 8-bit data length (LSB first).
- Odd parity, even parity, or non-parity mode is selectable.
- The start bit length is fixed at 1 bit.
- The stop bit length is selectable from 1 bit and 2 bits.
- Supports full-duplex communications.
- Includes a 2-byte receive data buffer and a 1-byte transmit data buffer.
- Includes an RZI modulator/demodulator circuit to support IrDA 1.0-compatible infrared communications.
- Can detect parity error, framing error, and overrun error.
- Can generate receive buffer full (1 byte/2 bytes), transmit buffer empty, end of transmission, parity error, framing error, and overrun error interrupts.
- Input pin can be pulled up with an internal resistor.
- The output pin is configurable as an open-drain output.

Figure 12.1.1 shows the UART configuration.

Table 12.1.1 UART Channel Configuration of S1C17589

Item	S1C17589
Number of channels	3 channels (Ch.0 to Ch.2)

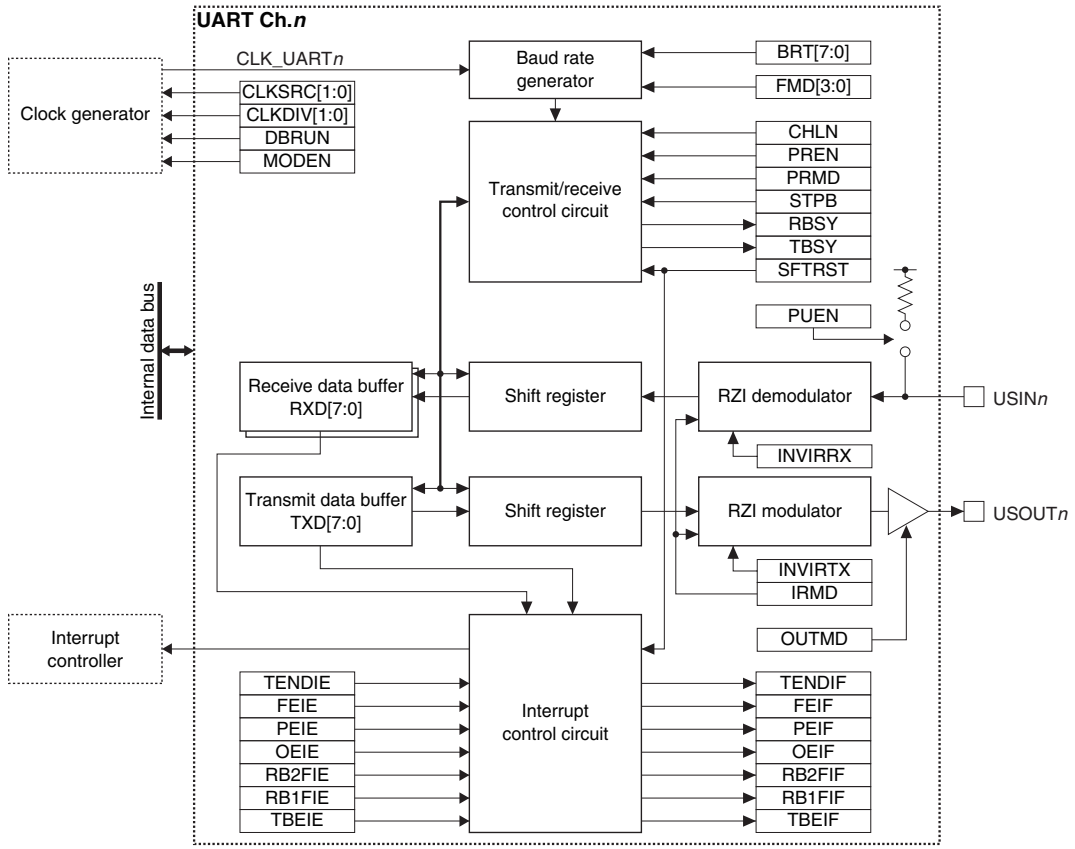


Figure 12.1.1 UART Configuration

12.2 Input/Output Pins and External Connections

12.2.1 List of Input/Output Pins

Table 12.2.1.1 lists the UART pins.

Table 12.2.1.1 List of UART Pins

Pin name	I/O*	Initial status*	Function
USIN*n*	I	I (Hi-Z)	UART Ch.*n* data input pin
USOUT*n*	O	O (High)	UART Ch.*n* data output pin

* Indicates the status when the pin is configured for the UART.

If the port is shared with the UART pin and other functions, the UART input/output function must be assigned to the port before activating the UART. For more information, refer to the "I/O Ports" chapter.

12.2.2 External Connections

Figure 12.2.2.1 shows a connection diagram between the UART in this IC and an external UART device.

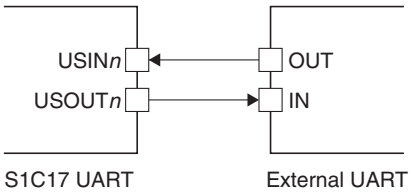


Figure 12.2.2.1 Connections between UART and an External UART Device

12.2.3 Input Pin Pull-Up Function

The UART includes a pull-up resistor for the USIN*n* pin. Setting the UA*n*MOD.PUEN bit to 1 enables the resistor to pull up the USIN*n* pin.

12.2.4 Output Pin Open-Drain Output Function

The USOUT*n* pin supports the open-drain output function. Default configuration is a push-pull output and it is switched to an open-drain output by setting the UA*n*MOD.OUTMD bit to 1.

12.3 Clock Settings

12.3.1 UART Operating Clock

When using the UART Ch.*n*, the UART Ch.*n* operating clock CLK_UART*n* must be supplied to the UART Ch.*n* from the clock generator. The CLK_UART*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following UA*n*CLK register bits:
   - UA*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - UA*n*CLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)

   The UART operating clock should be selected so that the baud rate generator will be configured easily.

12.3.2 Clock Supply in SLEEP Mode

When using the UART during SLEEP mode, the UART operating clock CLK_UART*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_UART*n* clock source.

12.3.3 Clock Supply in DEBUG Mode

The CLK_UART*n* supply during DEBUG mode should be controlled using the UA*n*CLK.DBRUN bit.
The CLK_UART*n* supply to the UART Ch.*n* is suspended when the CPU enters DEBUG mode if the UA*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_UART*n* supply resumes. Although the UART Ch.*n* stops operating when the CLK_UART*n* supply is suspended, the output pin and registers retain the status before DEBUG mode was entered. If the UA*n*CLK.DBRUN bit = 1, the CLK_UART*n* supply is not suspended and the UART Ch.*n* will keep operating in DEBUG mode.

12.3.4 Baud Rate Generator

The UART includes a baud rate generator to generate the transfer (sampling) clock. The transfer rate is determined by the UA*n*BR.BRT[7:0] and UA*n*BR.FMD[3:0] bit settings. Use the following equations to calculate the setting values for obtaining the desired transfer rate.

$$bps = \frac{CLK\_UART}{\{(BRT + 1) \times 16 + FMD\}} \qquad BRT = \left(\frac{CLK\_UART}{bps} - FMD - 16\right) \div 16 \qquad \text{(Eq. 12.1)}$$

Where

CLK_UART: UART operating clock frequency [Hz]
bps: Transfer rate [bit/s]
BRT: UA*n*BR.BRT[7:0] setting value (0 to 255)
FMD: UA*n*BR.FMD[3:0] setting value (0 to 15)

For the transfer rate range configurable in the UART, refer to "UART Characteristics, Transfer baud rates U_{BRT1} and U_{BRT2}" in the "Electrical Characteristics" chapter.

12.4 Data Format

The UART allows setting of the data length, stop bit length, and parity function. The start bit length is fixed at one bit.

Data length

With the UA*n*MOD.CHLN bit, the data length can be set to seven bits (UA*n*MOD.CHLN bit = 0) or eight bits (UA*n*MOD.CHLN bit = 1).

Stop bit length

With the UA*n*MOD.STPB bit, the stop bit length can be set to one bit (UA*n*MOD.STPB bit = 0) or two bits (UA*n*MOD.STPB bit = 1).

Parity function

The parity function is configured using the UA*n*MOD.PREN and UA*n*MOD.PRMD bits.

Table 12.4.1 Parity Function Setting

UA*n*MOD.PREN bit	UA*n*MOD.PRMD bit	Parity function
1	1	Odd parity
1	0	Even parity
0	*	Non parity

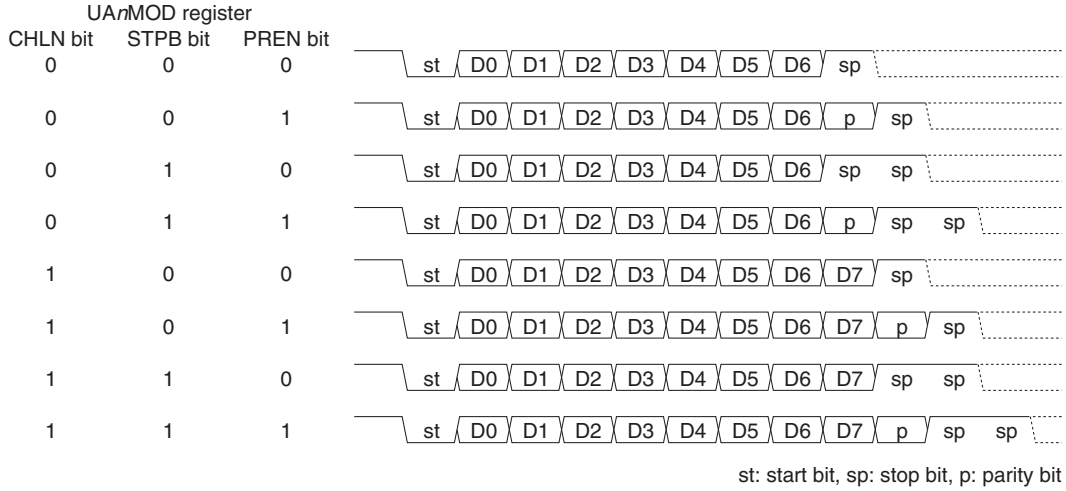


Figure 12.4.1 Data Format

12.5 Operations

12.5.1 Initialization

The UART Ch.*n* should be initialized with the procedure shown below.

1. Assign the UART Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
2. Set the UA*n*CLK.CLKSRC[1:0] and UA*n*CLK.CLKDIV[1:0] bits. (Configure operating clock)
3. Configure the following UA*n*MOD register bits:
   - UA*n*MOD.PUEN bit (Enable/disable USIN*n* pin pull-up)
   - UA*n*MOD.OUTMD bit (Enable/disable USOUT*n* pin open-drain output)
   - UA*n*MOD.IRMD bit (Enable/disable IrDA interface)
   - UA*n*MOD.CHLN bit (Set 7/8-bit data length)
   - UA*n*MOD.PREN bit (Enable/disable parity function)
   - UA*n*MOD.PRMD bit (Even/odd parity selection)
   - UA*n*MOD.STPB bit (Set 1/2-bit stop bit length)
4. Set the UA*n*BR.BRT[7:0] and UA*n*BR.FMD[3:0] bits. (Set transfer rate)
5. Set the following UA*n*CTL register bits:
   - Set the UA*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the UA*n*CTL.MODEN bit to 1. (Enable UART Ch.*n* operations)
6. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the UA*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the UA*n*INTE register to 1. * (Enable interrupts)

   * The initial value of the UA*n*INTF.TBEIF bit is 1, therefore, an interrupt will occur immediately after the UA*n*INTE.TBEIE bit is set to 1.

12.5.2 Data Transmission

A data sending procedure and the UART Ch.*n* operations are shown below. Figures 12.5.2.1 and 12.5.2.2 show a timing chart and a flowchart, respectively.

Data sending procedure

1. Check to see if the UA*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
2. Write transmit data to the UA*n*TXD register.
3. Wait for a UART interrupt when using the interrupt.
4. Repeat Steps 1 to 3 (or 1 and 2) until the end of transmit data.

UART data sending operations

The UART Ch.*n* starts data sending operations when transmit data is written to the UA*n*TXD register.
The transmit data in the UA*n*TXD register is automatically transferred to the shift register and the UA*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
The USOUT*n* pin outputs a start bit and the UA*n*INTF.TBSY bit is set to 1 (transmit busy). The shift register data bits are then output successively from the LSB. Following output of MSB, the parity bit (if parity is enabled) and the stop bit are output.

Even if transmit data is being output from the USOUT*n* pin, the next transmit data can be written to the UA*n*TXD register after making sure the UA*n*INTF.TBEIF bit is set to 1.

If no transmit data remains in the UA*n*TXD register after the stop bit has been output from the USOUT*n* pin, the UA*n*INTF.TBSY bit is cleared to 0 and the UA*n*INTF.TENDIF bit is set to 1 (transmission completed).

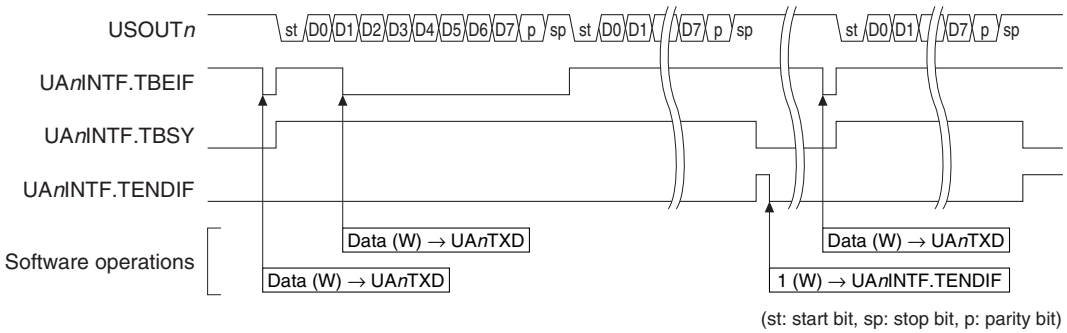


Figure 12.5.2.1 Example of Data Sending Operations

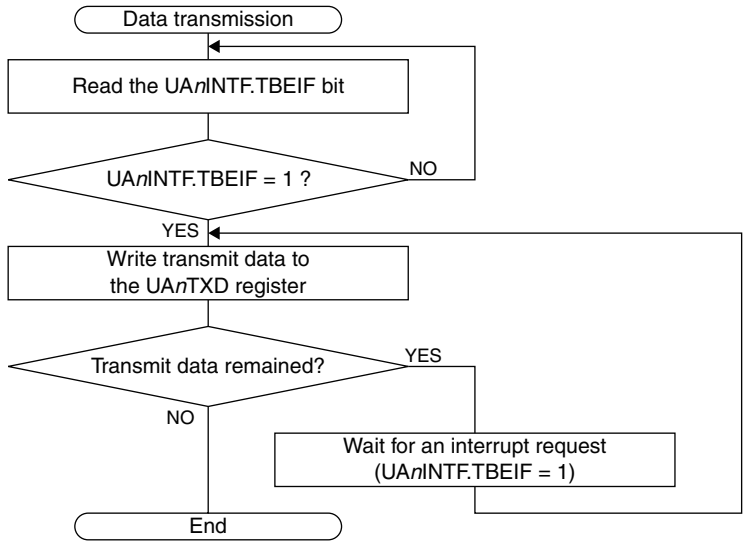


Figure 12.5.2.2 Data Transmission Flowchart

12.5.3 Data Reception

A data receiving procedure and the UART Ch.*n* operations are shown below. Figures 12.5.3.1 and 12.5.3.2 show a timing chart and flowcharts, respectively.

Data receiving procedure (read by one byte)

1. Wait for a UART interrupt when using the interrupt.
2. Check to see if the UA*n*INTF.RB1FIF bit is set to 1 (receive buffer one byte full).
3. Read the received data from the UA*n*RXD register.
4. Repeat Steps 1 to 3 (or 2 and 3) until the end of data reception.

Data receiving procedure (read by two bytes)

1. Wait for a UART interrupt when using the interrupt.
2. Check to see if the UA*n*INTF.RB2FIF bit is set to 1 (receive buffer two bytes full).
3. Read the received data from the UA*n*RXD register twice.
4. Repeat Steps 1 to 3 (or 2 and 3) until the end of data reception.

UART data receiving operations

The UART Ch.*n* starts data receiving operations when a start bit is input to the USIN*n* pin.
After the receive circuit has detected a low level as a start bit, it starts sampling the following data bits and loads the received data into the receive shift register. The UA*n*INTF.RBSY bit is set to 1 when the start bit is detected.
The UA*n*INTF.RBSY bit is cleared to 0 and the receive shift register data is transferred to the receive data buffer at the stop bit receive timing.
The receive data buffer consists of a 2-byte FIFO and receives data until it becomes full. When the receive data buffer receives the first data, it sets the UA*n*INTF.RB1FIF bit to 1 (receive buffer one byte full). If the second data is received without reading the first data, the UA*n*INTF.RB2FIF bit is set to 1 (receive buffer two bytes full).

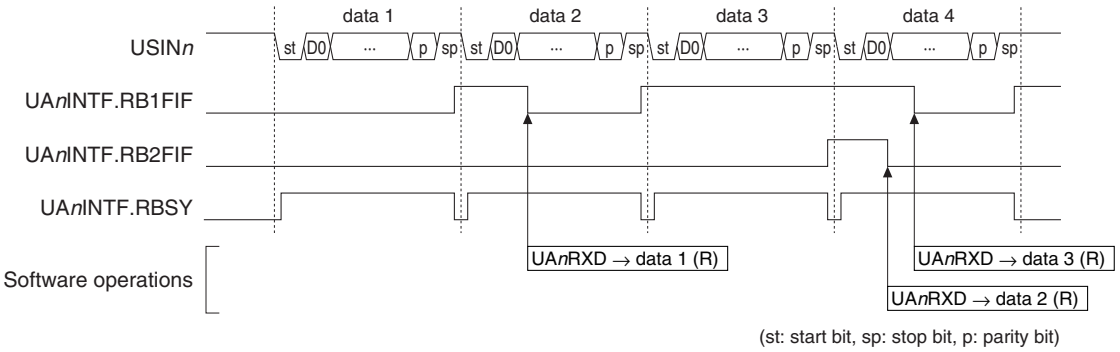


Figure 12.5.3.1 Example of Data Receiving Operations

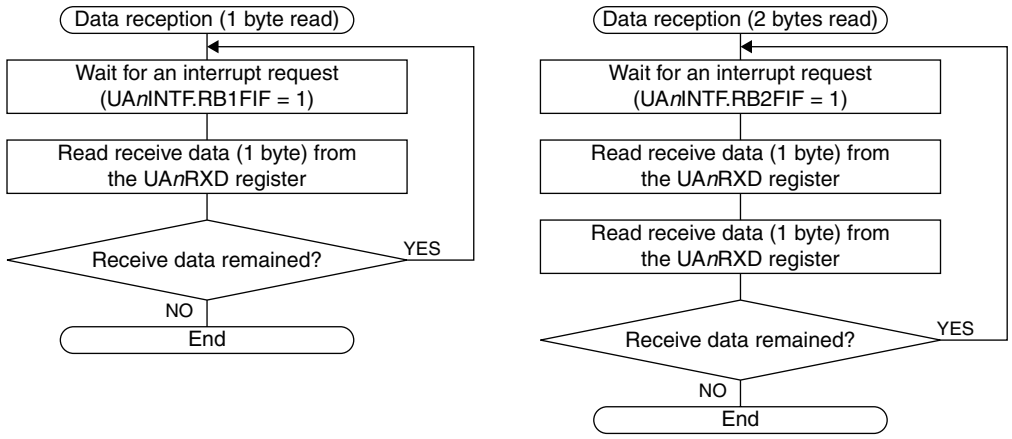


Figure 12.5.3.2 Data Reception Flowcharts

12.5.4 IrDA Interface

This UART includes an RZI modulator/demodulator circuit enabling implementation of IrDA 1.0-compatible infrared communication function simply by adding simple external circuits.
Set the UA*n*MOD.IRMD bit to 1 to use the IrDA interface.
Data transfer control is identical to that for normal interface even if the IrDA interface function is enabled.

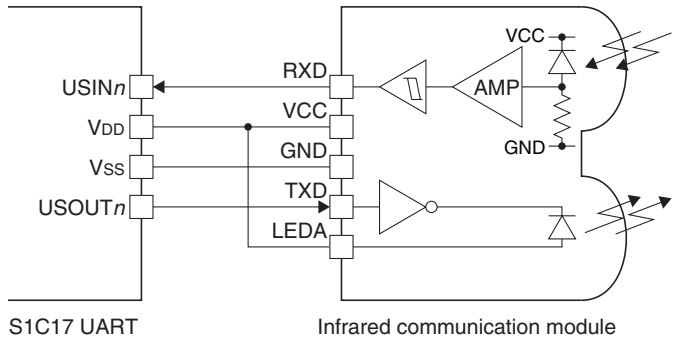


Figure 12.5.4.1 Example of Connections with an Infrared Communication Module

The transmit data output from the UART Ch.*n* transmit shift register is output from the USOUT*n* pin after the low pulse width is converted into 3/16 by the RZI modulator in SIR method and inverted. The USOUT*n* pin output signal can be inverted by setting the UA*n*MOD.INVIRTX bit to 1.

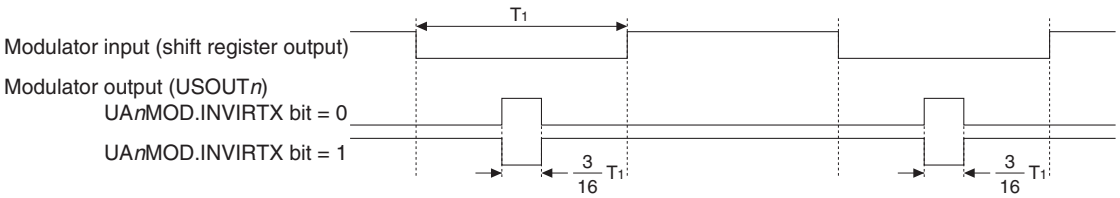


Figure 12.5.4.2 IrDA Transmission Signal Waveform

The received IrDA signal is input to the RZI demodulator and the low pulse width is converted into the normal width before input to the receive shift register. The USIN*n* pin input signal can be inverted prior to being demodulated by setting the UA*n*MOD.INVIRRX bit to 1.

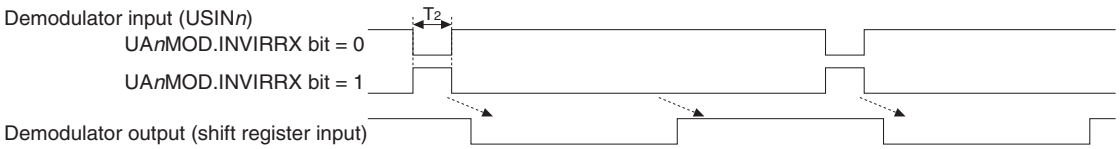


Figure 12.5.4.3 IrDA Receive Signal Waveform

Note: The low pulse width (T_2) of the IrDA signal input must be CLK_UART × 3 cycles or longer.

12.6 Receive Errors

Three different receive errors, framing error, parity error, and overrun error, may be detected while receiving data. Since receive errors are interrupt causes, they can be processed by generating interrupts.

12.6.1 Framing Error

The UART determines loss of sync if a stop bit is not detected (when the stop bit is received as 0) and assumes that a framing error has occurred. The received data that encountered an error is still transferred to the receive data buffer and the UA*n*INTF.FEIF bit (framing error interrupt flag) is set to 1 when the data becomes ready to read from the UA*n*RXD register.

Note: Framing error/parity error interrupt flag set timings
These interrupt flags will be set after the data that encountered an error is transferred to the receive data buffer. Note, however, that the set timing depends on the buffer status at that point.

- When the receive data buffer is empty
  The interrupt flag will be set when the data that encountered an error is transferred to the receive data buffer.

- When the receive data buffer has a one-byte free space
  The interrupt flag will be set when the first data byte already loaded is read out after the data that encountered an error is transferred to the second byte entry of the receive data buffer.

12.6.2 Parity Error

If the parity function is enabled, a parity check is performed when data is received. The UART checks matching between the data received in the shift register and its parity bit, and issues a parity error if the result is a non-match. The received data that encountered an error is still transferred to the receive data buffer and the UA*n*INTF.PEIF bit (parity error interrupt flag) is set to 1 when the data becomes ready to read from the UA*n*RXD register (see the Note on framing error).

12.6.3 Overrun Error

If the receive data buffer is still full (two bytes of received data have not been read) when a data reception to the shift register has completed, an overrun error occurs as the data cannot be transferred to the receive data buffer. When an overrun error occurs, the UA*n*INTF.OEIF bit (overrun error interrupt flag) is set to 1.

12.7 Interrupts

The UART has a function to generate the interrupts shown in Table 12.7.1.

Table 12.7.1 UART Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
End of transmission	UA*n*INTF.TENDIF	When the UA*n*INTF.TBEIF bit = 1 after the stop bit has been sent	Writing 1 or software reset
Framing error	UA*n*INTF.FEIF	Refer to the “Receive Errors.”	Writing 1, reading received data that encountered an error, or software reset
Parity error	UA*n*INTF.PEIF	Refer to the “Receive Errors.”	Writing 1, reading received data that encountered an error, or software reset
Overrun error	UA*n*INTF.OEIF	Refer to the “Receive Errors.”	Writing 1 or software reset
Receive buffer two bytes full	UA*n*INTF.RB2FIF	When the second received data byte is loaded to the receive data buffer in which the first byte is already received	Reading received data or software reset
Receive buffer one byte full	UA*n*INTF.RB1FIF	When the first received data byte is loaded to the emptied receive data buffer	Reading data to empty the receive data buffer or software reset
Transmit buffer empty	UA*n*INTF.TBEIF	When transmit data written to the transmit data buffer is transferred to the shift register	Writing transmit data

The UART provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the “Interrupt Controller” chapter.

12.8 Control Registers

UART Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the UART operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the UART operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the UART.

Table 12.8.1 Clock Source and Division Ratio Settings

UA*n*CLK.CLKDIV[1:0] bits	UA*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/8	1/1	1/8	1/1
0x2	1/4		1/4	
0x1	1/2		1/2	
0x0	1/1		1/1	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The UA*n*CLK register settings can be altered only when the UA*n*CTL.MODEN bit = 0.

UART Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*MOD	15–10	–	0x00	–	R	–
	9	INVIRRX	0	H0	R/W	
	8	INVIRTX	0	H0	R/W	
	7	–	0	–	R	
	6	PUEN	0	H0	R/W	
	5	OUTMD	0	H0	R/W	
	4	IRMD	0	H0	R/W	
	3	CHLN	0	H0	R/W	
	2	PREN	0	H0	R/W	
	1	PRMD	0	H0	R/W	
	0	STPB	0	H0	R/W	

Bits 15–10 Reserved

Bit 9 INVIRRX

This bit enables the USIN*n* input inverting function when the IrDA interface function is enabled.

1 (R/W): Enable input inverting function

0 (R/W): Disable input inverting function

Bit 8 INVIRTX

This bit enables the USOUT*n* output inverting function when the IrDA interface function is enabled.

1 (R/W): Enable output inverting function

0 (R/W): Disable output inverting function

Bit 7 Reserved

Bit 6 PUEN

This bit enables pull-up of the USIN*n* pin.

1 (R/W): Enable pull-up

0 (R/W): Disable pull-up

Bit 5 OUTMD

This bit sets the USOUT*n* pin output mode.
1 (R/W): Open-drain output
0 (R/W): Push-pull output

Bit 4 IRMD

This bit enables the IrDA interface function.
1 (R/W): Enable IrDA interface function
0 (R/W): Disable IrDA interface function

Bit 3 CHLN

This bit sets the data length.
1 (R/W): 8 bits
0 (R/W): 7 bits

Bit 2 PREN

This bit enables the parity function.
1 (R/W): Enable parity function
0 (R/W): Disable parity function

Bit 1 PRMD

This bit selects either odd parity or even parity when using the parity function.
1 (R/W): Odd parity
0 (R/W): Even parity

Bit 0 STPB

This bit sets the stop bit length.
1 (R/W): 2 bits
0 (R/W): 1 bit

Note: The UA*n*MOD register settings can be altered only when the UA*n*CTL.MODEN bit = 0.

UART Ch.*n* Baud–Rate Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*BR	15–12	–	0x0	–	R	–
	11–8	FMD[3:0]	0x0	H0	R/W	
	7–0	BRT[7:0]	0x00	H0	R/W	

Bits 15–12 Reserved

Bits 11–8 FMD[3:0]
Bits 7–0 BRT[7:0]

These bits set the UART transfer rate. For more information, refer to "Baud Rate Generator."

Note: The UA*n*BR register settings can be altered only when the UA*n*CTL.MODEN bit = 0.

UART Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*CTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 SFTRST

This bit issues software reset to the UART.

1 (W): Issue software reset
0 (W): Ineffective
1 (R): Software reset is executing.
0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the UART transmit/receive control circuit and interrupt flags. This bit is automatically cleared after the reset processing has finished.

Bit 0 MODEN

This bit enables the UART operations.

1 (R/W): Enable UART operations (The operating clock is supplied.)
0 (R/W): Disable UART operations (The operating clock is stopped.)

Note: If the UA*n*CTL.MODEN bit is altered from 1 to 0 while sending/receiving data, the data being sent/received cannot be guaranteed. When setting the UA*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the UA*n*CTL.SFTRST bit as well.

UART Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*TXD	15–8	–	0x00	–	R	–
	7–0	TXD[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 TXD[7:0]

Data can be written to the transmit data buffer through these bits. Make sure the UA*n*INTF.TBEIF bit is set to 1 before writing data.

UART Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*RXD	15–8	–	0x00	–	R	–
	7–0	RXD[7:0]	0x00	H0	R	

Bits 15–8 Reserved

Bits 7–0 RXD[7:0]

The receive data buffer can be read through these bits. The receive data buffer consists of a 2-byte FIFO, and older received data is read first.

UART Ch.*n* Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*INTF	15–10	–	0x00	–	R	–
	9	RBSY	0	H0/S0	R	
	8	TBSY	0	H0/S0	R	
	7	–	0	–	R	
	6	TENDIF	0	H0/S0	R/W	Cleared by writing 1.
	5	FEIF	0	H0/S0	R/W	Cleared by writing 1 or reading the UA*n*RXD register.
	4	PEIF	0	H0/S0	R/W	
	3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
	2	RB2FIF	0	H0/S0	R	Cleared by reading the UA*n*RXD register.
	1	RB1FIF	0	H0/S0	R	
	0	TBEIF	1	H0/S0	R	Cleared by writing to the UA*n*TXD register.

Bits 15–10 Reserved

Bit 9 RBSY

This bit indicates the receiving status. (See Figure 12.5.3.1.)

1 (R): During receiving

0 (R): Idle

Bit 8 TBSY

This bit indicates the sending status. (See Figure 12.5.2.1.)

1 (R): During sending

0 (R): Idle

Bit 7 Reserved

Bit 6 TENDIF
Bit 5 FEIF
Bit 4 PEIF
Bit 3 OEIF
Bit 2 RB2FIF
Bit 1 RB1FIF
Bit 0 TBEIF

These bits indicate the UART interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

UA*n*INTF.TENDIF bit: End-of-transmission interrupt

UA*n*INTF.FEIF bit: Framing error interrupt

UA*n*INTF.PEIF bit: Parity error interrupt

UA*n*INTF.OEIF bit: Overrun error interrupt

UA*n*INTF.RB2FIF bit: Receive buffer two bytes full interrupt

UA*n*INTF.RB1FIF bit: Receive buffer one byte full interrupt

UA*n*INTF.TBEIF bit: Transmit buffer empty interrupt

UART Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
UA*n*INTE	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6	TENDIE	0	H0	R/W	
	5	FEIE	0	H0	R/W	
	4	PEIE	0	H0	R/W	
	3	OEIE	0	H0	R/W	
	2	RB2FIE	0	H0	R/W	
	1	RB1FIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–7 Reserved

Bit 6 TENDIE
Bit 5 FEIE
Bit 4 PEIE
Bit 3 OEIE
Bit 2 RB2FIE
Bit 1 RB1FIE
Bit 0 TBEIE

These bits enable UART interrupts.

1 (R/W): Enable interrupts

0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
UA*n*INTE.TENDIE bit: End-of-transmission interrupt
UA*n*INTE.FEIE bit: Framing error interrupt
UA*n*INTE.PEIE bit: Parity error interrupt
UA*n*INTE.OEIE bit: Overrun error interrupt
UA*n*INTE.RB2FIE bit: Receive buffer two bytes full interrupt
UA*n*INTE.RB1FIE bit: Receive buffer one byte full interrupt
UA*n*INTE.TBEIE bit: Transmit buffer empty interrupt

13 Synchronous Serial Interface (SPIA)

13.1 Overview

SPIA is a synchronous serial interface. The features of SPIA are listed below.

- Supports both master and slave modes.
- Data length: 2 to 16 bits programmable
- Either MSB first or LSB first can be selected for the data format.
- Clock phase and polarity are configurable.
- Supports full-duplex communications.
- Includes separated transmit data buffer and receive data buffer registers.
- Can generate receive buffer full, transmit buffer empty, end of transmission, and overrun interrupts.
- Master mode allows use of a 16-bit timer to set baud rate.
- Slave mode is capable of being operated with the external input clock SPICLK*n* only.
- Slave mode is capable of being operated in SLEEP mode allowing wake-up by an SPIA interrupt.
- Input pins can be pulled up/down with an internal resistor.

Figure 13.1.1 shows the SPIA configuration.

Table 13.1.1 SPIA Channel Configuration of S1C17589

Item	S1C17589
Number of channels	2 channels (Ch.0 and Ch.1)
Internal clock input	Ch.0 ← 16-bit timer Ch.1 Ch.1 ← 16-bit timer Ch.2

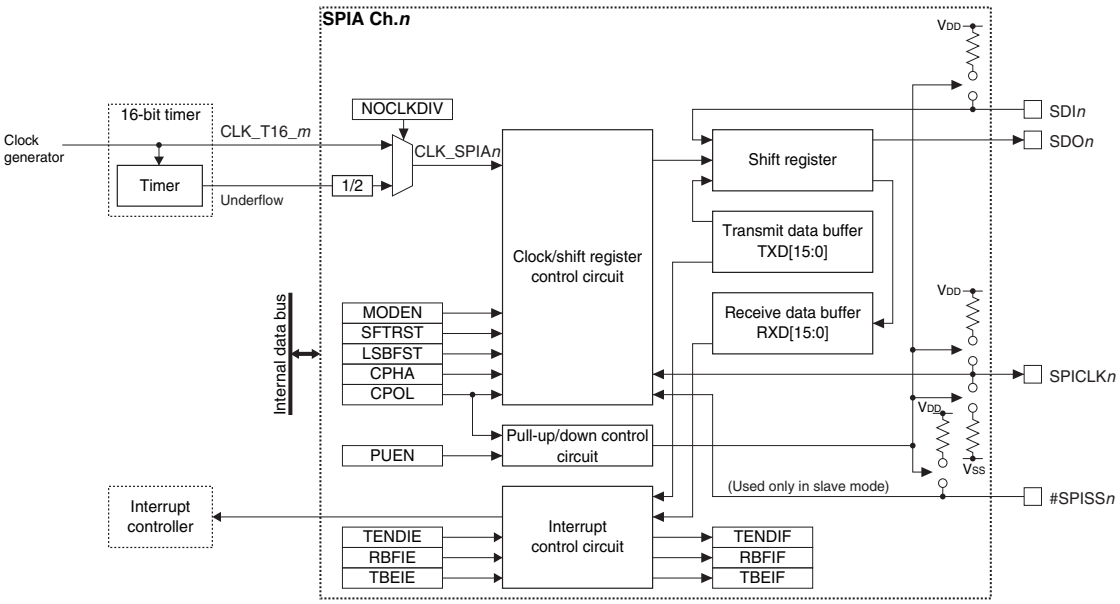


Figure 13.1.1 SPIA Configuration

13.2 Input/Output Pins and External Connections

13.2.1 List of Input/Output Pins

Table 13.2.1.1 lists the SPIA pins.

Table 13.2.1.1 List of SPIA Pins

Pin name	I/O*	Initial status*	Function
SDI*n*	I	I (Hi-Z)	SPIA Ch.*n* data input pin
SDO*n*	O or Hi-Z	Hi-Z	SPIA Ch.*n* data output pin
SPICLK*n*	I or O	I (Hi-Z)	SPIA Ch.*n* external clock input/output pin
#SPISS*n*	I	I (Hi-Z)	SPIA Ch.*n* slave select signal input pin

* Indicates the status when the pin is configured for SPIA.

If the port is shared with the SPIA pin and other functions, the SPIA input/output function must be assigned to the port before activating SPIA. For more information, refer to the "I/O Ports" chapter.

13.2.2 External Connections

SPIA operates in master mode or slave mode. Figures 13.2.2.1 and 13.2.2.2 show connection diagrams between SPIA in each mode and external SPI devices.

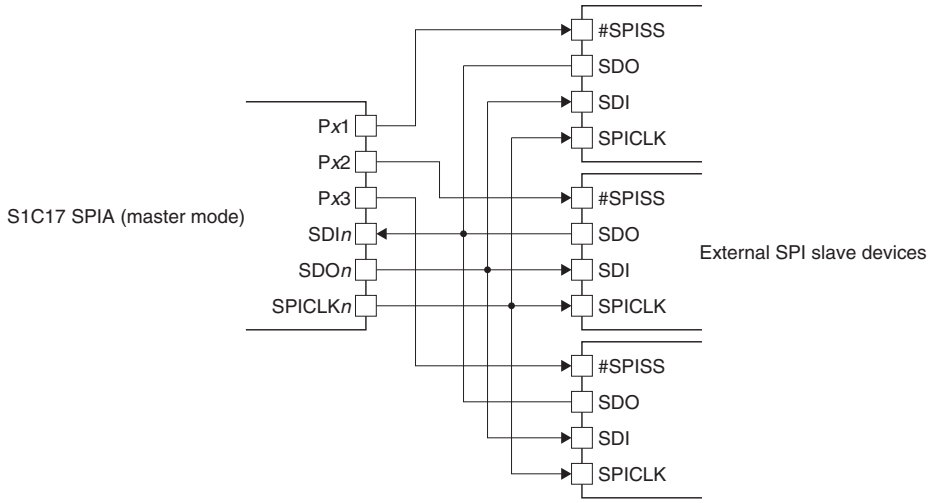


Figure 13.2.2.1 Connections between SPIA in Master Mode and External SPI Slave Devices

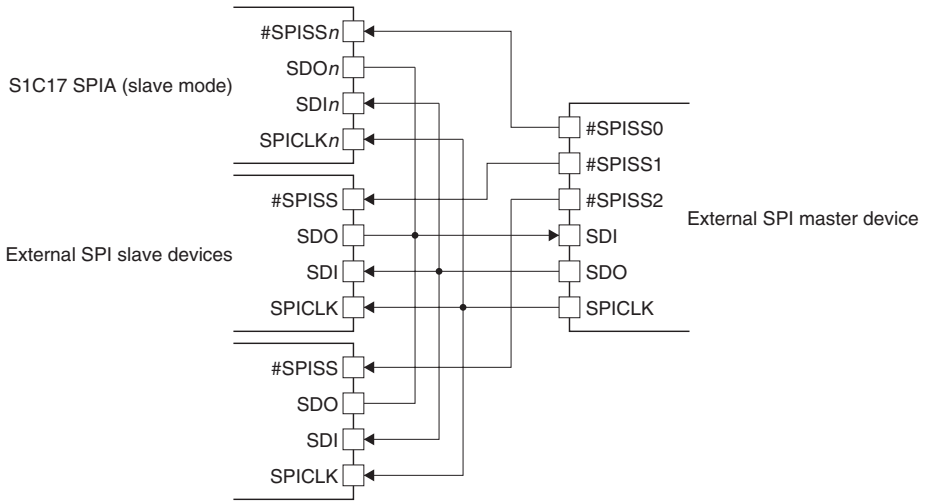


Figure 13.2.2.2 Connections between SPIA in Slave Mode and External SPI Master Device

13.2.3 Pin Functions in Master Mode and Slave Mode

The pin functions are changed according to the master or slave mode selection. The differences in pin functions between the modes are shown in Table 13.2.3.1.

Table 13.2.3.1 Pin Function Differences between Modes

Pin	Function in master mode	Function in slave mode
SDI*n*	Always placed into input state.	
SDO*n*	Always placed into output state.	This pin is placed into output state while a low level is applied to the #SPISS*n* pin or placed into Hi-Z state while a high level is applied to the #SPISS*n* pin.
SPICLK*n*	Outputs the SPI clock to external devices. Output clock polarity and phase can be configured if necessary.	Inputs an external SPI clock. Clock polarity and phase can be designated according to the input clock.
#SPISS*n*	Not used. This input function is not required to be assigned to the port. To output the slave select signal in master mode, use a general-purpose I/O port function.	Applying a low level to the #SPISS*n* pin enables SPIA to transmit/receive data. While a high level is applied to this pin, SPIA is not selected as a slave device. Data input to the SDI*n* pin and the clock input to the SPICLK*n* pin are ignored. When a high level is applied, the transmit/receive bit count is cleared to 0 and the already received bits are discarded.

13.2.4 Input Pin Pull-Up/Pull-Down Function

The SPIA input pins (SDI*n* in master mode or SDI*n*, SPICLK*n*, and #SPISS*n* pins in slave mode) have a pull-up or pull-down function as shown in Table 13.2.4.1. This function is enabled by setting the SPI*n*MOD.PUEN bit to 1.

Table 13.2.4.1 Pull-Up or Pull-Down of Input Pins

Pin	Master mode	Slave mode
SDI*n*	Pull-up	Pull-up
SPICLK*n*	–	SPI*n*MOD.CPOL bit = 1: Pull-up SPI*n*MOD.CPOL bit = 0: Pull-down
#SPISS*n*	–	Pull-up

13.3 Clock Settings

13.3.1 SPIA Operating Clock

Operating clock in master mode

In master mode, the SPIA operating clock is supplied from the 16-bit timer. The following two options are provided for the clock configuration.

Use the 16-bit timer operating clock without dividing

By setting the SPI*n*MOD.NOCLKDIV bit to 1, the operating clock CLK_T16_*m*, which is configured by selecting a clock source and a division ratio, for the 16-bit timer channel corresponding to the SPIA channel is input to SPIA as CLK_SPIA*n*. Since this clock is also used as the SPI clock SPICLK*n* without changing, the CLK_SPIA*n* frequency becomes the baud rate.

To supply CLK_SPIA*n* to SPIA, the 16-bit timer clock source must be enabled in the clock generator. It does not matter how the T16_*m*CTL.MODEN and T16_*m*CTL.PRUN bits of the corresponding 16-bit timer channel are set (1 or 0).

When setting this mode, the timer function of the corresponding 16-bit timer channel may be used for another purpose.

Use the 16-bit timer as a baud rate generator

By setting the SPI*n*MOD.NOCLKDIV bit to 0, SPIA inputs the underflow signal generated by the corresponding 16-bit timer channel and converts it to the SPICLK*n*. The 16-bit timer must be run with an appropriate reload data set. The SPICLK*n* frequency (baud rate) and the 16-bit timer reload data are calculated by the equations shown below.

$$f_{SPICLK} = \frac{f_{CLK\_SPIA}}{2 \times (RLD + 1)} \qquad RLD = \frac{f_{CLK\_SPIA}}{f_{SPICLK} \times 2} - 1 \qquad \text{(Eq. 13.1)}$$

Where

f_{SPICLK}: SPICLK*n* frequency [Hz] (= baud rate [bps])
f_{CLK_SPIA}: SPIA operating clock frequency [Hz]
RLD: 16-bit timer reload data value

For controlling the 16-bit timer, refer to the "16-bit Timers" chapter.

Operating clock in slave mode

SPIA set in slave mode operates with the clock supplied from the external SPI master to the SPICLK*n* pin. The 16-bit timer channel (including the clock source selector and the divider) corresponding to the SPIA channel is not used. Furthermore, the SPI*n*MOD.NOCLKDIV bit setting becomes ineffective.
SPIA keeps operating using the clock supplied from the external SPI master even if all the internal clocks halt during SLEEP mode, so SPIA can receive data and can generate receive buffer full interrupts.

13.3.2 Clock Supply in DEBUG Mode

In master mode, the operating clock supply during DEBUG mode should be controlled using the T16_*m*CLK.DBRUN bit.
The CLK_T16_*m* supply to SPIA Ch.*n* is suspended when the CPU enters DEBUG mode if the T16_*m*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_T16_*m* supply resumes. Although SPIA Ch.*n* stops operating when the CLK_T16_*m* supply is suspended, the output pins and registers retain the status before DEBUG mode was entered. If the T16_*m*CLK.DBRUN bit = 1, the CLK_T16_*m* supply is not suspended and SPIA Ch.*n* will keep operating in DEBUG mode.
SPIA in slave mode operates with the external SPI master clock input from the SPICLK*n* pin regardless of whether the CPU is placed into DEBUG mode or normal mode.

13.3.3 SPI Clock (SPICLK*n*) Phase and Polarity

The SPICLK*n* phase and polarity can be configured separately using the SPI*n*MOD.CPHA bit and the SPI*n*MOD.CPOL bit, respectively. Figure 13.3.3.1 shows the clock waveform and data input/output timing in each setting.

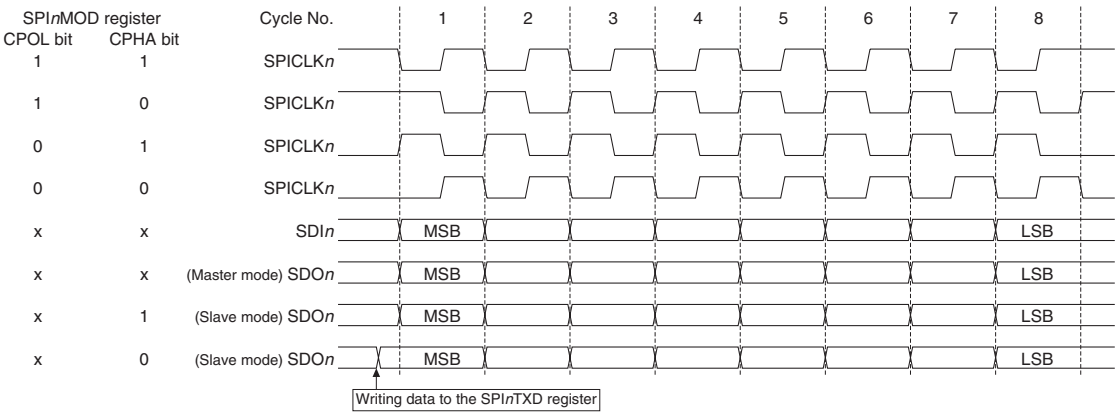


Figure 13.3.3.1 SPI Clock Phase and Polarity (SPI*n*MOD.LSBFST bit = 0, SPI*n*MOD.CHLN[3:0] bits = 0x7)

13.4 Data Format

The SPIA data length can be selected from 2 bits to 16 bits by setting the SPI*n*MOD.CHLN[3:0] bits. The input/output permutation is configurable to MSB first or LSB first using the SPI*n*MOD.LSBFST bit. Figure 13.4.1 shows a data format example when the SPI*n*MOD.CHLN[3:0] bits = 0x7, the SPI*n*MOD.CPOL bit = 0 and the SPI*n*MOD.CPHA bit = 0.

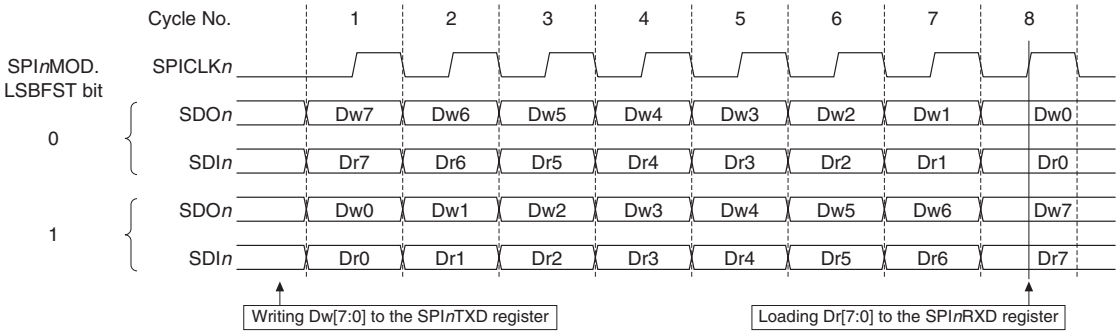


Figure 13.4.1 Data Format Selection Using the SPI*n*MOD.LSBFST Bit
(SPI*n*MOD.CHLN[3:0] bits = 0x7, SPI*n*MOD.CPOL bit = 0, SPI*n*MOD.CPHA bit = 0)

13.5 Operations

13.5.1 Initialization

SPIA Ch.*n* should be initialized with the procedure shown below.

1. <Master mode only> Generate a clock by controlling the 16-bit timer and supply it to SPIA Ch.*n*.
2. Configure the following SPI*n*MOD register bits:
   - SPI*n*MOD.PUEN bit (Enable input pin pull-up/down)
   - SPI*n*MOD.NOCLKDIV bit (Select master mode operating clock)
   - SPI*n*MOD.LSBFST bit (Select MSB first/LSB first)
   - SPI*n*MOD.CPHA bit (Select clock phase)
   - SPI*n*MOD.CPOL bit (Select clock polarity)
   - SPI*n*MOD.MST bit (Select master/slave mode)
3. Assign the SPIA Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
4. Set the following SPI*n*CTL register bits:
   - Set the SPI*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the SPI*n*CTL.MODEN bit to 1. (Enable SPIA Ch.*n* operations)
5. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the SPI*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the SPI*n*INTE register to 1. * (Enable interrupts)

   * The initial value of the SPI*n*INTF.TBEIF bit is 1, therefore, an interrupt will occur immediately after the SPI*n*INTE.TBEIE bit is set to 1.

13.5.2 Data Transmission in Master Mode

A data sending procedure and operations in master mode are shown below. Figures 13.5.2.1 and 13.5.2.2 show a timing chart and a flowchart, respectively.

Data sending procedure

1. Assert the slave select signal by controlling the general-purpose output port (if necessary).
2. Check to see if the SPI*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
3. Write transmit data to the SPI*n*TXD register.

4. Wait for an SPIA interrupt when using the interrupt.
5. Repeat Steps 2 to 4 (or 2 and 3) until the end of transmit data.
6. Negate the slave select signal by controlling the general-purpose output port (if necessary).

Data sending operations

SPIA Ch.*n* starts data sending operations when transmit data is written to the SPI*n*TXD register.
The transmit data in the SPI*n*TXD register is automatically transferred to the shift register and the SPI*n*INTF.TBEIF bit is set to 1. If the SPI*n*INTE.TBEIE bit = 1 (transmit buffer empty interrupt enabled), a transmit buffer empty interrupt occurs at the same time.
The SPICLK*n* pin outputs clocks of the number of the bits specified by the SPI*n*MOD.CHLN[3:0] bits and the transmit data bits are output in sequence from the SDO*n* pin in sync with these clocks.

Even if the clock is being output from the SPICLK*n* pin, the next transmit data can be written to the SPI*n*TXD register after making sure the SPI*n*INTF.TBEIF bit is set to 1.

If transmit data has not been written to the SPI*n*TXD register after the last clock is output from the SPICLK*n* pin, the clock output halts and the SPI*n*INTF.TENDIF bit is set to 1. At the same time SPIA issues an end-of-transmission interrupt request if the SPI*n*INTE.TENDIE bit = 1.

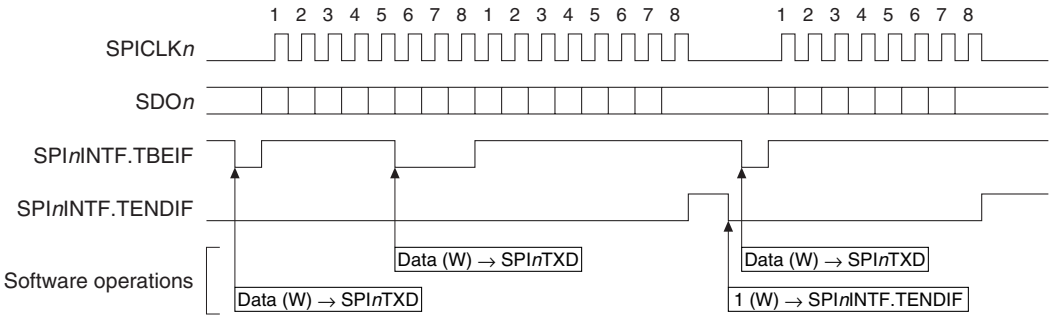


Figure 13.5.2.1 Example of Data Sending Operations in Master Mode (SPI*n*MOD.CHLN[3:0] bits = 0x7)

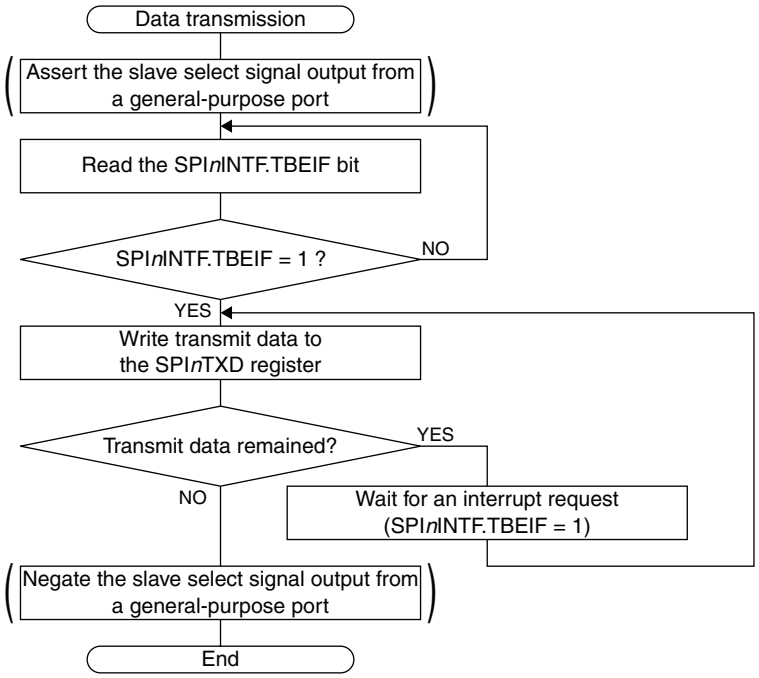


Figure 13.5.2.2 Data Transmission Flowchart in Master Mode

13.5.3 Data Reception in Master Mode

A data receiving procedure and operations in master mode are shown below. Figures 13.5.3.1 and 13.5.3.2 show a timing chart and flowcharts, respectively.

Data receiving procedure

1. Assert the slave select signal by controlling the general-purpose output port (if necessary).
2. Check to see if the SPI*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
3. Write dummy data (or transmit data) to the SPI*n*TXD register.
4. Wait for a transmit buffer empty interrupt (SPI*n*INTF.TBEIF bit = 1).
5. Write dummy data (or transmit data) to the SPI*n*TXD register.
6. Wait for a receive buffer full interrupt (SPI*n*INTF.RBFIF bit = 1).
7. Read the received data from the SPI*n*RXD register.
8. Repeat Steps 5 to 7 until the end of data reception.
9. Negate the slave select signal by controlling the general-purpose output port (if necessary).

Note: To perform continuous data reception without stopping SPICLK*n*, Steps 7 and 5 operations must be completed within the SPICLK*n* cycles equivalent to "Data bit length - 1" after Step 6.

Data receiving operations

SPIA Ch.*n* starts data receiving operations simultaneously with data sending operations when transmit data (may be dummy data if data transmission is not required) is written to the SPI*n*TXD register.
The SPICLK*n* pin outputs clocks of the number of the bits specified by the SPI*n*MOD.CHLN[3:0] bits. The transmit data bits are output in sequence from the SDO*n* pin in sync with these clocks and the receive data bits input from the SDI*n* pin are shifted into the shift register.
When the last clock is output from the SPICLK*n* pin and receive data bits are all shifted into the shift register, the received data is transferred to the receive data buffer and the SPI*n*INTF.RBFIF bit is set to 1. At the same time SPIA issues a receive buffer full interrupt request if the SPI*n*INTE.RBFIE bit = 1. After that, the received data in the receive data buffer can be read through the SPI*n*RXD register.

Note: If data of the number of the bits specified by the SPI*n*MOD.CHLN[3:0] bits is received when the SPI*n*INTF.RBFIF bit is set to 1, the SPI*n*RXD register is overwritten with the newly received data and the previously received data is lost. In this case, the SPI*n*INTF.OEIF bit is set.

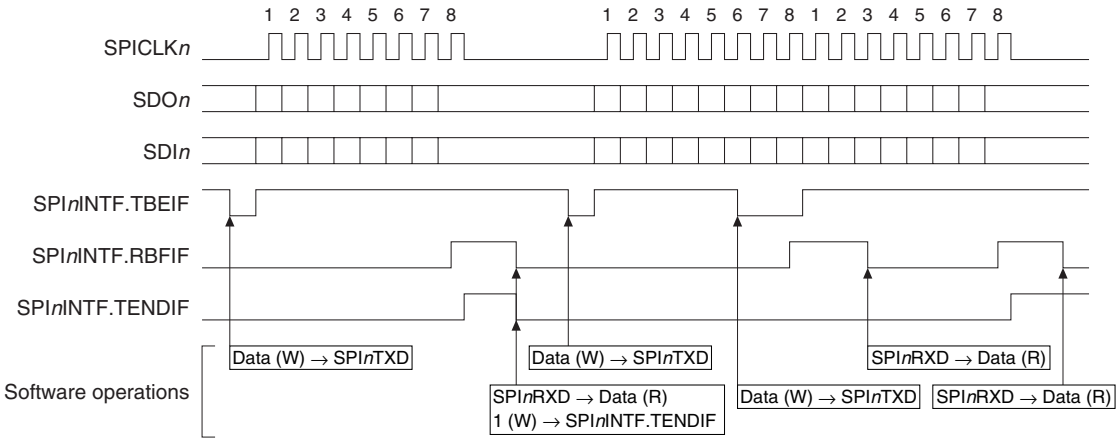


Figure 13.5.3.1 Example of Data Receiving Operations in Master Mode (SPI*n*MOD.CHLN[3:0] bits = 0x7)

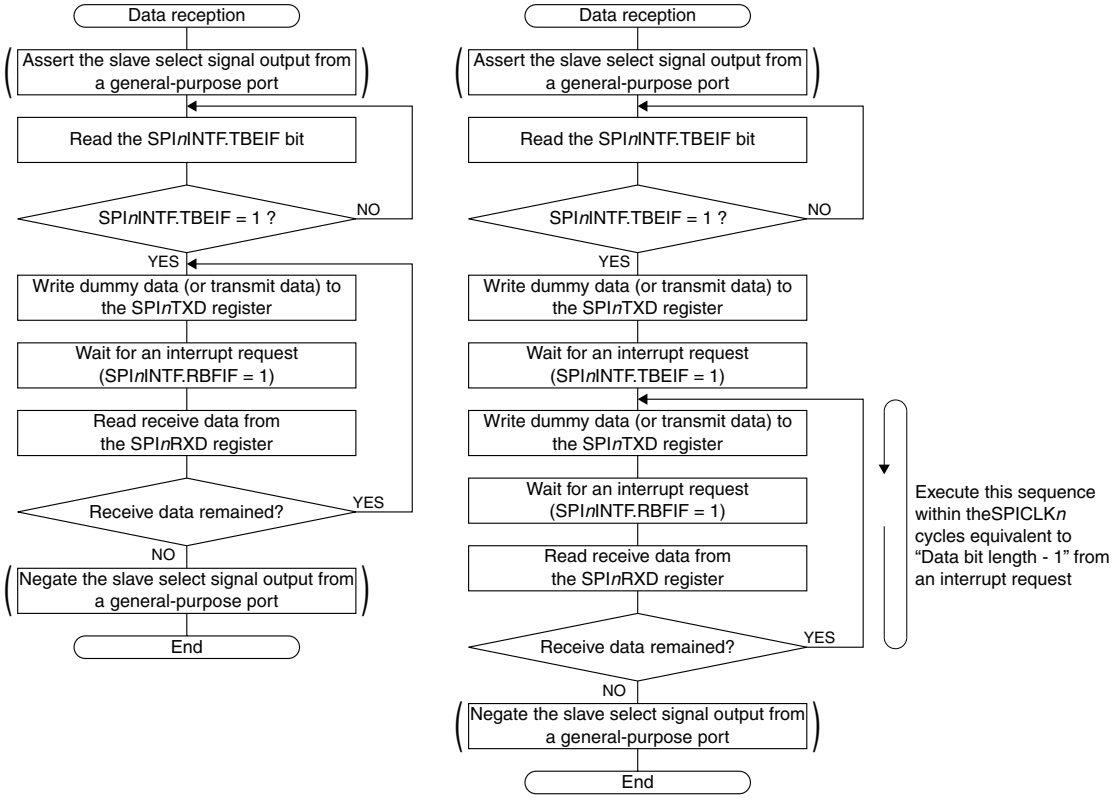


Figure 13.5.3.2 Data Reception Flowcharts in Master Mode

13.5.4 Terminating Data Transfer in Master Mode

A procedure to terminate data transfer in master mode is shown below.

1. Wait for an end-of-transmission interrupt (SPI*n*INTF.TENDIF bit = 1).
2. Set the SPI*n*CTL.MODEN bit to 0 to disable the SPIA Ch.*n* operations.
3. Stop the 16-bit timer to disable the clock supply to SPIA Ch.*n*.

13.5.5 Data Transfer in Slave Mode

A data sending/receiving procedure and operations in slave mode are shown below. Figures 13.5.5.1 and 13.5.5.2 show a timing chart and flowcharts, respectively.

Data sending procedure

1. Check to see if the SPI*n*INTF.TBEIF bit is set to 1 (transmit buffer empty).
2. Write transmit data to the SPI*n*TXD register.
3. Wait for a transmit buffer empty interrupt (SPI*n*INTF.TBEIF bit = 1).
4. Repeat Steps 2 and 3 until the end of transmit data.

Note: Transmit data must be written to the SPI*n*TXD register after the SPI*n*INTF.TBEIF bit is set to 1 by the time the sending SPI*n*TXD register data written is completed. If no transmit data is written during this period, the data bits input from the SDI*n* pin are shifted and output from the SDO*n* pin without being modified.

Data receiving procedure

1. Wait for a receive buffer full interrupt (SPI*n*INTF.RBFIF bit = 1).
2. Read the received data from the SPI*n*RXD register.
3. Repeat Steps 1 and 2 until the end of data reception.

Data transfer operations

The following shows the slave mode operations different from master mode:

- Slave mode operates with the SPI clock supplied from the external SPI master to the SPICLK*n* pin.
  The data transfer rate is determined by the SPICLK*n* frequency. It is not necessary to control the 16-bit timer.
- SPIA can operate as a slave device only when the slave select signal input from the external SPI master to the #SPISS*n* pin is set to the active (low) level.
  If #SPISS*n* = high, the software transfer control, the SPICLK*n* pin input, and the SDI*n* pin input are all ineffective. If the #SPISS*n* signal goes high during data transfer, the transfer bit counter is cleared and data in the shift register is discarded.
- Slave mode starts data transfer when SPICLK*n* is input from the external SPI master after the #SPISS*n* signal is asserted. Writing transmit data is not a trigger to start data transfer. Therefore, it is not necessary to write dummy data to the transmit data buffer when performing data reception only.
- Data transmission/reception can be performed even in SLEEP mode, it makes it possible to wake the CPU up using an SPIA interrupt.

Other operations are the same as master mode.

Notes: • If data of the number of bits specified by the SPI*n*MOD.CHLN[3:0] bits is received when the SPI*n*INTF.RBFIF bit is set to 1, the SPI*n*RXD register is overwritten with the newly received data and the previously received data is lost. In this case, the SPI*n*INTF.OEIF bit is set.

• When the clock for the first bit is input from the SPICLK*n* pin, SPIA starts sending the data currently stored in the shift register even if the SPI*n*INTF.TBEIF bit is set to 1.

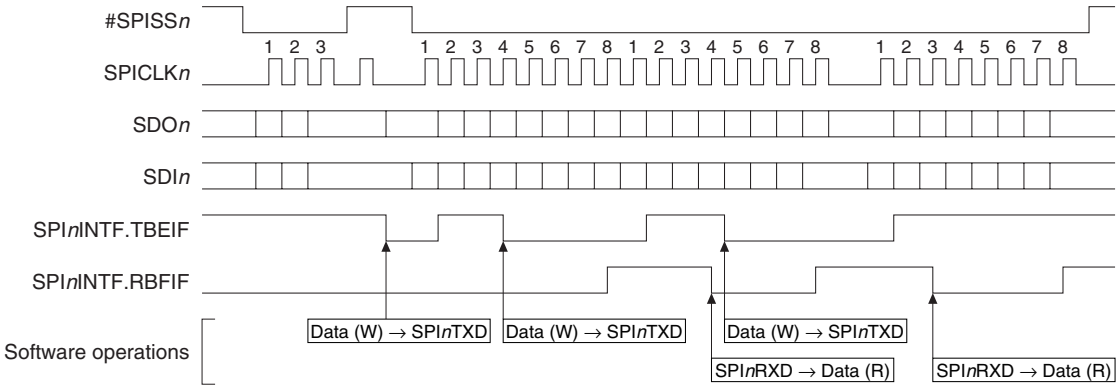


Figure 13.5.5.1 Example of Data Transfer Operations in Slave Mode (SPI*n*MOD.CHLN[3:0] bits = 0x7)

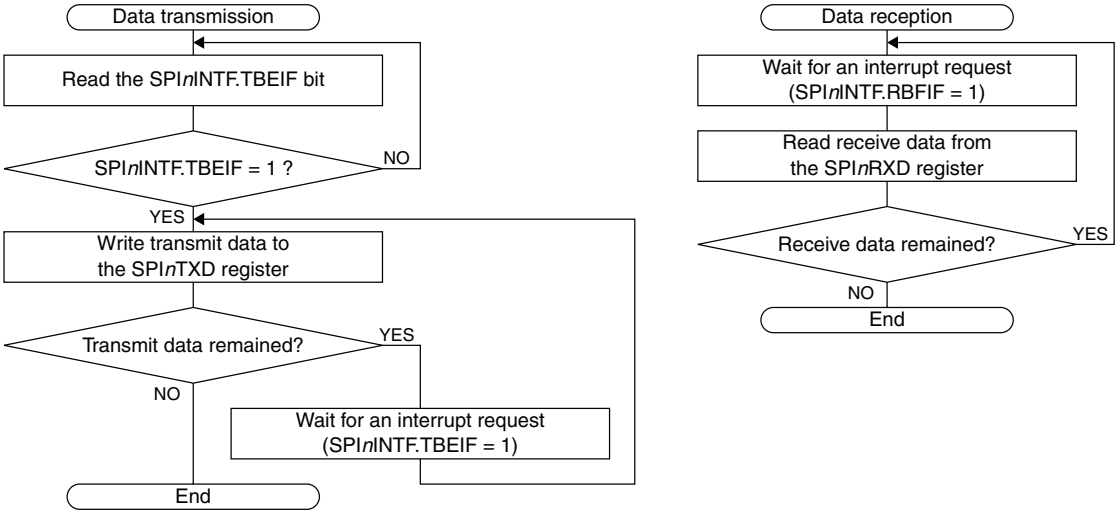


Figure 13.5.5.2 Data Transfer Flowcharts in Slave Mode

13.5.6 Terminating Data Transfer in Slave Mode

A procedure to terminate data transfer in slave mode is shown below.

1. Wait for an end-of-transmission interrupt (SPI*n*INTF.TENDIF bit = 1). Or determine end of transfer via the received data.
2. Set the SPI*n*CTL.MODEN bit to 0 to disable the SPIA Ch.*n* operations.

13.6 Interrupts

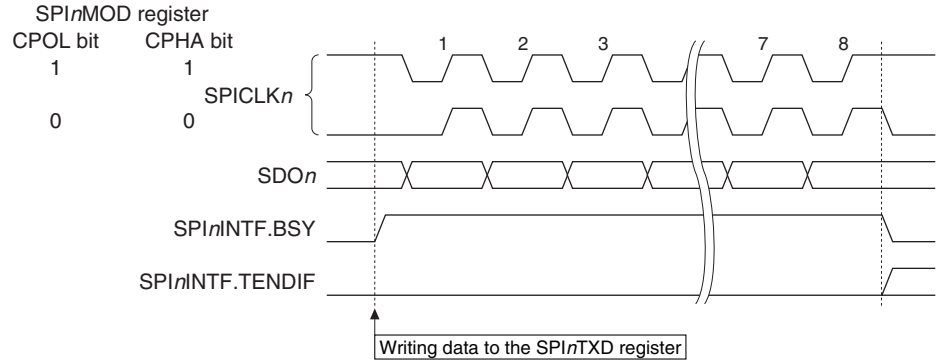
SPIA has a function to generate the interrupts shown in Table 13.6.1.

Table 13.6.1 SPIA Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
End of transmission	SPI*n*INTF.TENDIF	When the SPI*n*INTF.TBEIF bit = 1 after data of the specified bit length (defined by the SPI*n*MOD.CHLN[3:0] bits) has been sent	Writing 1
Receive buffer full	SPI*n*INTF.RBFIF	When data of the specified bit length is received and the received data is transferred from the shift register to the received data buffer	Reading the SPI*n*RXD register
Transmit buffer empty	SPI*n*INTF.TBEIF	When transmit data written to the transmit data buffer is transferred to the shift register	Writing to the SPI*n*TXD register
Overrun error	SPI*n*INTF.OEIF	When the receive data buffer is full (when the received data has not been read) at the point that receiving data to the shift register has completed	Writing 1

SPIA provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.
The SPI*n*INTF register also contains the BSY bit that indicates the SPIA operating status.
Figure 13.6.1 shows the SPI*n*INTF.BSY and SPI*n*INTF.TENDIF bit set timings.

Master mode



Slave mode

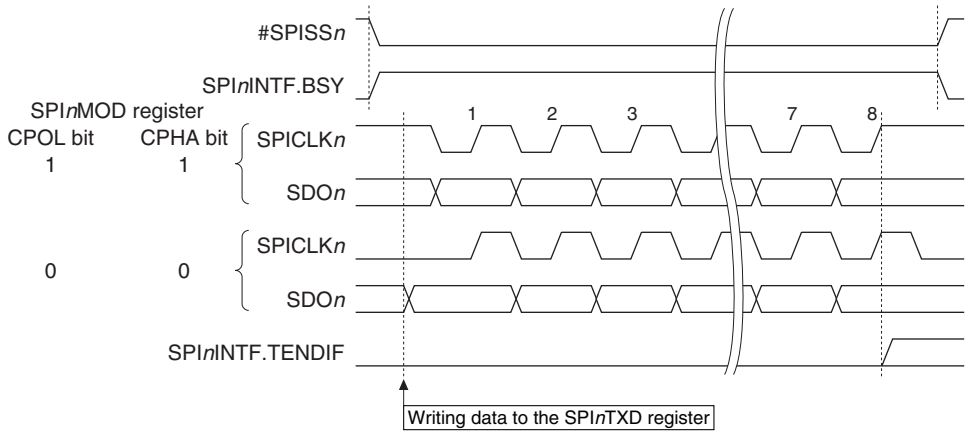


Figure 13.6.1 SPI*n*INTF.BSY and SPI*n*INTF.TENDIF Bit Set Timings (when SPI*n*MOD.CHLN[3:0] bits = 0x7)

13.7 Control Registers

SPIA Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*MOD	15–12	–	0x0	–	R	–
	11–8	CHLN[3:0]	0x7	H0	R/W	
	7–6	–	0x0	–	R	
	5	PUEN	0	H0	R/W	
	4	NOCLKDIV	0	H0	R/W	
	3	LSBFST	0	H0	R/W	
	2	CPHA	0	H0	R/W	
	1	CPOL	0	H0	R/W	
	0	MST	0	H0	R/W	

Bits 15–12 Reserved

Bits 11–8 CHLN[3:0]

These bits set the bit length of transfer data.

Table 13.7.1 Data Bit Length Settings

SPI*n*MOD.CHLN[3:0] bits	Data bit length
0xf	16 bits
0xe	15 bits
0xd	14 bits
0xc	13 bits
0xb	12 bits
0xa	11 bits
0x9	10 bits
0x8	9 bits
0x7	8 bits
0x6	7 bits
0x5	6 bits
0x4	5 bits
0x3	4 bits
0x2	3 bits
0x1	2 bits
0x0	Setting prohibited

Bits 7–6 Reserved

Bit 5 PUEN

This bit enables pull-up/down of the input pins.
1 (R/W): Enable pull-up/down
0 (R/W): Disable pull-up/down

For more information, refer to "Input Pin Pull-Up/Pull-Down Function."

Bit 4 NOCLKDIV

This bit selects SPICLK*n* in master mode. This setting is ineffective in slave mode.
1 (R/W): SPICLK*n* frequency = CLK_SPIA*n* frequency (= 16-bit timer operating clock frequency)
0 (R/W): SPICLK*n* frequency = 16-bit timer output frequency / 2

For more information, refer to "SPIA Operating Clock."

Bit 3 LSBFST

This bit configures the data format (input/output permutation).
1 (R/W): LSB first
0 (R/W): MSB first

Bit 2 CPHA
Bit 1 CPOL

These bits set the SPI clock phase and polarity. For more information, refer to "SPI Clock (SPICLK*n*) Phase and Polarity."

Bit 0 MST

This bit sets the SPIA operating mode (master mode or slave mode).
1 (R/W): Master mode
0 (R/W): Slave mode

Note: The SPI*n*MOD register settings can be altered only when the SPI*n*CTL.MODEN bit = 0.

SPIA Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*CTL	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 SFTRST

This bit issues software reset to SPIA.

1 (W): Issue software reset
0 (W): Ineffective
1 (R): Software reset is executing.
0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the SPIA shift register and transfer bit counter. This bit is automatically cleared after the reset processing has finished.

Bit 0 MODEN

This bit enables the SPIA operations.

1 (R/W): Enable SPIA operations (In master mode, the operating clock is supplied.)
0 (R/W): Disable SPIA operations (In master mode, the operating clock is stopped.)

Note: If the SPI*n*CTL.MODEN bit is altered from 1 to 0 while sending/receiving data, the data being sent/received cannot be guaranteed. When setting the SPI*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the SPI*n*CTL.SFTRST bit as well.

SPIA Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*TXD	15–0	TXD[15:0]	0x0000	H0	R/W	–

Bits 15–0 TXD[15:0]

Data can be written to the transmit data buffer through these bits.
In master mode, writing to these bits starts data transfer.
Transmit data can be written when the SPI*n*INTF.TBEIF bit = 1 regardless of whether data is being output from the SDO*n* pin or not.
Note that the upper data bits that exceed the data bit length configured by the SPI*n*MOD.CHLN[3:0] bits will not be output from the SDO*n* pin.

Note: Be sure to avoid writing to the SPI*n*TXD register when the SPI*n*INTF.TBEIF bit = 0. Otherwise, transfer data cannot be guaranteed.

SPIA Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*RXD	15–0	RXD[15:0]	0x0000	H0	R	–

Bits 15–0 RXD[15:0]

The receive data buffer can be read through these bits. Received data can be read when the SPI*n*INTF.RBFIF bit = 1 regardless of whether data is being input from the SDI*n* pin or not. Note that the upper bits that exceed the data bit length configured by the SPI*n*MOD.CHLN[3:0] bits become 0.

Note: The SPI*n*RXD.RXD[15:0] bits are cleared to 0x0000 when 1 is written to the SPI*n*CTL.MODEN bit or the SPI*n*CTL.SFTRST bit.

SPIA Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*INTF	15–8	–	0x00	–	R	–
	7	BSY	0	H0	R	
	6–4	–	0x0	–	R	
	3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
	2	TENDIF	0	H0/S0	R/W	
	1	RBFIF	0	H0/S0	R	Cleared by reading the SPI*n*RXD register.
	0	TBEIF	1	H0/S0	R	Cleared by writing to the SPI*n*TXD register.

Bits 15–8 Reserved

Bit 7 BSY

This bit indicates the SPIA operating status.

1 (R): Transmit/receive busy (master mode), #SPISS*n* = Low level (slave mode)

0 (R): Idle

Bits 6–4 Reserved

Bit 3 OEIF

Bit 2 TENDIF

Bit 1 RBFIF

Bit 0 TBEIF

These bits indicate the SPIA interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag (OEIF, TENDIF)

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

SPI*n*INTF.OEIF bit: Overrun error interrupt

SPI*n*INTF.TENDIF bit: End-of-transmission interrupt

SPI*n*INTF.RBFIF bit: Receive buffer full interrupt

SPI*n*INTF.TBEIF bit: Transmit buffer empty interrupt

SPIA Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
SPI*n*INTE	15–8	–	0x00	–	R	–
	7–4	–	0x0	–	R	
	3	OEIE	0	H0	R/W	
	2	TENDIE	0	H0	R/W	
	1	RBFIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–4 Reserved

Bit 3 OEIE

Bit 2 TENDIE

Bit 1 RBFIE

Bit 0 TBEIE

These bits enable SPIA interrupts.

1 (R/W): Enable interrupts

0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:

SPI*n*INTE.OEIE bit: Overrun error interrupt

SPI*n*INTE.TENDIE bit: End-of-transmission interrupt

SPI*n*INTE.RBFIE bit: Receive buffer full interrupt

SPI*n*INTE.TBEIE bit: Transmit buffer empty interrupt

14 I²C (I2C)

14.1 Overview

The I2C is a subset of the I²C bus interface. The features of the I2C are listed below.

- Functions as an I²C bus master (single master) or a slave device.
- Supports standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s).
- Supports 7-bit and 10-bit address modes.
- Supports clock stretching.
- Includes a baud rate generator for generating the clock in master mode.
- No clock source is required to run the I2C in slave mode, as it can run with the I²C bus signals only.
- Slave mode is capable of being operated in SLEEP mode allowing wake-up by an interrupt when an address match is detected.
- Master mode supports automatic bus clear sending function.
- Can generate receive buffer full, transmit buffer empty, and other interrupts.

Figure 14.1.1 shows the I2C configuration.

Table 14.1.1 I2C Channel Configuration of S1C17589

Item	S1C17589
Number of channels	2 channels (Ch.0 and Ch.1)

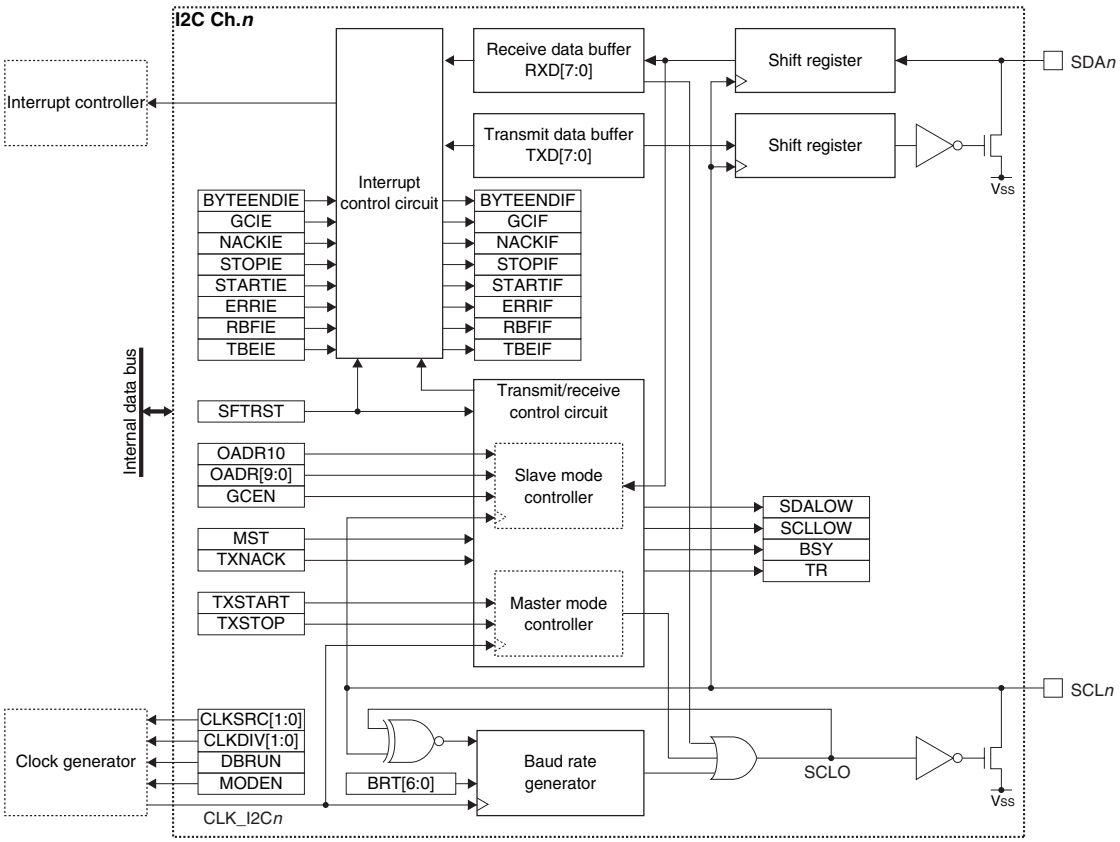


Figure 14.1.1 I2C Configuration

14.2 Input/Output Pins and External Connections

14.2.1 List of Input/Output Pins

Table 14.2.1.1 lists the I2C pins.

Table 14.2.1.1 List of I2C Pins

Pin name	I/O*	Initial status*	Function
SDA*n*	I/O	I	I2C bus serial data input/output pin
SCL*n*	I/O	I	I2C bus clock input/output pin

* Indicates the status when the pin is configured for the I2C.

If the port is shared with the I2C pin and other functions, the I2C input/output function must be assigned to the port before activating the I2C. For more information, refer to the "I/O Ports" chapter.

14.2.2 External Connections

Figure 14.2.2.1 shows a connection diagram between the I2C in this IC and external I2C devices.
The serial data (SDA) and serial clock (SCL) lines must be pulled up with an external resistor.
When the I2C is set into master mode, one or more slave devices that have a unique address may be connected to the I2C bus. When the I2C is set into slave mode, one or more master and slave devices that have a unique address may be connected to the I2C bus.

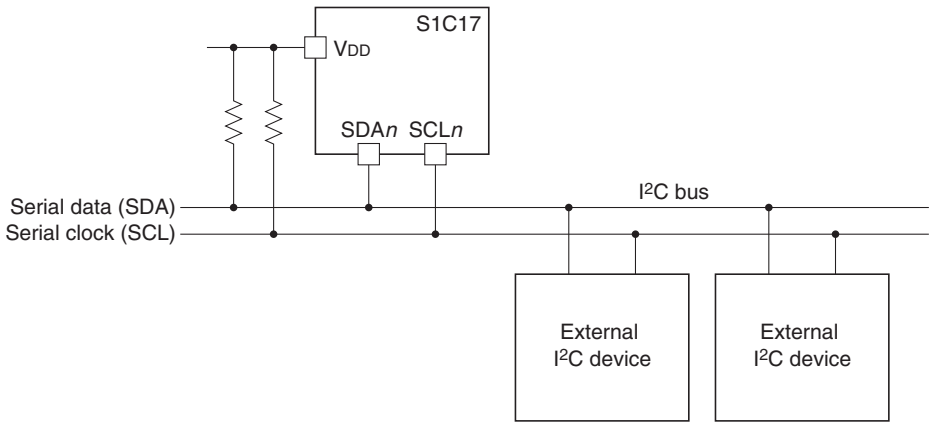


Figure 14.2.2.1 Connections between I2C and External I2C Devices

Notes: • The SDA and SCL lines must be pulled up to a VDD of this IC or lower voltage. However, if the I2C input/output ports are configured with the over voltage tolerant fail-safe type I/O, these lines can be pulled up to a voltage exceeding the VDD of this IC but within the recommended operating voltage range of this IC.

• The internal pull-up resistors for the I/O ports cannot be used for pulling up SDA and SCL.

• When the I2C is set into master mode, no other master device can be connected to the I2C bus.

14.3 Clock Settings

14.3.1 I2C Operating Clock

Master mode operating clock

When using the I2C Ch.*n* in master mode, the I2C Ch.*n* operating clock CLK_I2C*n* must be supplied to the I2C Ch.*n* from the clock generator. The CLK_I2C*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following I2C*n*CLK register bits:
   - I2C*n*CLK.CLKSRC[1:0] bits (Clock source selection)
   - I2C*n*CLK.CLKDIV[1:0] bits (Clock division ratio selection = Clock frequency setting)

   When using the I2C in master mode during SLEEP mode, the I2C Ch.*n* operating clock CLK_I2C*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_I2C*n* clock source.
   The I2C operating clock should be selected so that the baud rate generator will be configured easily.

Slave mode operating clock

The I2C set to slave mode uses the SCL supplied from the I²C master as its operating clock. The clock setting by the I2C*n*CLK register is ineffective.
The I2C keeps operating using the clock supplied from the external I²C master even if all the internal clocks halt during SLEEP mode, so the I2C can receive data and can generate receive buffer full interrupts.

14.3.2 Clock Supply in DEBUG Mode

In master mode, the CLK_I2C*n* supply during DEBUG mode should be controlled using the I2C*n*CLK.DBRUN bit. The CLK_I2C*n* supply to the I2C Ch.*n* is suspended when the CPU enters DEBUG mode if the I2C*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_I2C*n* supply resumes. Although the I2C Ch.*n* stops operating when the CLK_I2C*n* supply is suspended, the output pin and registers retain the status before DEBUG mode was entered. If the I2C*n*CLK.DBRUN bit = 1, the CLK_I2C*n* supply is not suspended and the I2C Ch.*n* will keep operating in DEBUG mode.
In slave mode, the I2C Ch.*n* operates with the external I²C master clock input from the SCL*n* pin regardless of whether the CPU is placed into DEBUG mode or normal mode.

14.3.3 Baud Rate Generator

The I2C includes a baud rate generator to generate the serial clock SCL used in master mode. The I2C set to slave mode does not use the baud rate generator, as it operates with the serial clock input from the SCL*n* pin.

Setting data transfer rate (for master mode)

The transfer rate is determined by the I2C*n*BR.BRT[6:0] bit settings. Use the following equations to calculate the setting values for obtaining the desired transfer rate.

$$bps = \frac{f_{CLK\_I2Cn}}{(BRT + 3) \times 2} \qquad BRT = \frac{f_{CLK\_I2Cn}}{bps \times 2} - 3 \qquad \text{(Eq. 14.1)}$$

Where
- bps: Data transfer rate [bit/s]
- f_{CLK_I2Cn}: I2C operating clock frequency [Hz]
- BRT: I2C*n*BR.BRT[6:0] bits setting value (1 to 127)

∗ The equations above do not include SCL rising/falling time and delay time by clock stretching (see Figure 14.3.3.1).

Note: The I²C bus transfer rate is limited to 100 kbit/s in standard mode or 400 kbit/s in fast mode. Do not set a transfer rate exceeding the limit.

Baud rate generator clock output and operations for supporting clock stretching

Figure 14.3.3.1 shows the clock generated by the baud rate generator and the clock waveform on the I²C bus.

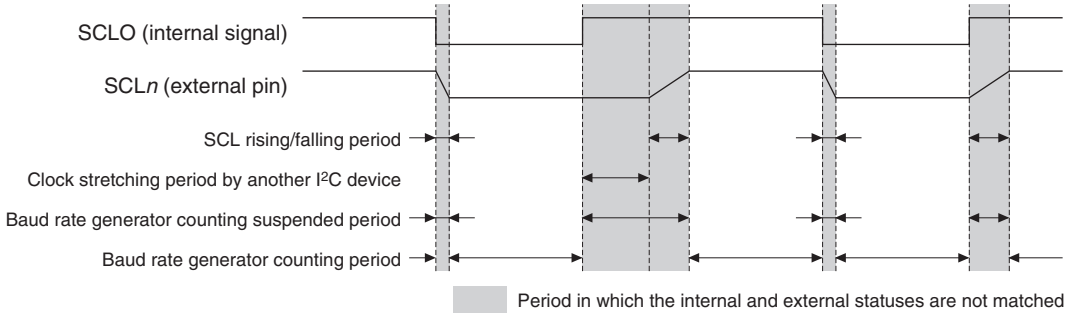


Figure 14.3.3.1 Baud Rate Generator Output Clock and SCL*n* Output Waveform

The baud rate generator output clock SCLO is compared with the SCL*n* pin status and the results are returned to the baud rate generator. If a mismatch has occurred between SCLO and SCL*n* pin levels, the baud rate generator suspends counting. This extends the clock to control data transfer during the SCL signal rising/falling period and clock stretching period in which SCL is fixed at low by a slave device.

14.4 Operations

14.4.1 Initialization

The I2C Ch.*n* should be initialized with the procedure shown below.

When using the I2C in master mode

1. Configure the operating clock and the baud rate generator using the I2C*n*CLK and I2C*n*BR registers.
2. Assign the I2C Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
3. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the I2C*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the I2C*n*INTE register to 1. (Enable interrupts)
4. Set the following I2C*n*CTL register bits:
   - Set the I2C*n*CTL.MST bit to 1. (Set master mode)
   - Set the I2C*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the I2C*n*CTL.MODEN bit to 1. (Enable I2C Ch.*n* operations)

When using the I2C in slave mode

1. Set the following I2C*n*MOD register bits:
   - I2C*n*MOD.OADR10 bit (Set 10/7-bit address mode)
   - I2C*n*MOD.GCEN bit (Enable response to general call address)
2. Set its own address to the I2C*n*OADR.OADR[9:0] (or OADR[6:0]) bits.
3. Assign the I2C Ch.*n* input/output function to the ports. (Refer to the "I/O Ports" chapter.)
4. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the I2C*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the I2C*n*INTE register to 1. (Enable interrupts)
5. Set the following I2C*n*CTL register bits:
   - Set the I2C*n*CTL.MST bit to 0. (Set slave mode)
   - Set the I2C*n*CTL.SFTRST bit to 1. (Execute software reset)
   - Set the I2C*n*CTL.MODEN bit to 1. (Enable I2C Ch.*n* operations)

14.4.2 Data Transmission in Master Mode

A data sending procedure in master mode and the I2C Ch.*n* operations are shown below. Figures 14.4.2.1 and 14.4.2.2 show an operation example and a flowchart, respectively.

Data sending procedure

1. Issue a START condition by setting the I2C*n*CTL.TXSTART bit to 1.
2. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
3. Write the 7-bit slave address to the I2C*n*TXD.TXD[7:1] bits and 0 that represents WRITE as the data transfer direction to the I2C*n*TXD.TXD0 bit.
4. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) generated when an ACK is received or a NACK reception interrupt (I2C*n*INTF.NACKIF bit = 1) generated when a NACK is received.
   i. Go to Step 5 if transmit data remains when a transmit buffer empty interrupt has occurred.
   ii. Go to Step 7 or 1 after clearing the I2C*n*INTF.NACKIF bit when a NACK reception interrupt has occurred.
5. Write transmit data to the I2C*n*TXD register.
6. Repeat Steps 4 and 5 until the end of transmit data.
7. Issue a STOP condition by setting the I2C*n*CTL.TXSTOP bit to 1.
8. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1).
   Clear the I2C*n*INTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data sending operations

Generating a START condition

The I2C Ch.*n* starts generating a START condition when the I2C*n*CTL.TXSTART bit is set to 1. When the generating operation has completed, the I2C Ch.*n* clears the I2C*n*CTL.TXSTART bit to 0 and sets both the I2C*n*INTF.STARTIF and I2C*n*INTF.TBEIF bits to 1.

Sending slave address and data

If the I2C*n*INTF.TBEIF bit = 1, a slave address or data can be written to the I2C*n*TXD register. The I2C Ch.*n* pulls down SCL to low and enters standby state until data is written to the I2C*n*TXD register. The writing operation triggers the I2C Ch.*n* to send the data to the shift register automatically and to output eight clock pulses and data bits to the I²C bus.

When the slave device returns an ACK as the response, the I2C*n*INTF.TBEIF bit is set to 1. After this interrupt occurs, the subsequent data may be sent or a STOP/repeated START condition may be issued to terminate transmission. If the slave device returns NACK, the I2C*n*INTF.NACKIF bit is set to 1 without setting the I2C*n*INTF.TBEIF bit.

Generating a STOP/repeated START condition

After the I2C*n*INTF.TBEIF bit is set to 1 (transmit buffer empty) or the I2C*n*INTF.NACKIF bit is set to 1 (NACK received), setting the I2C*n*CTL.TXSTOP bit to 1 generates a STOP condition. When the bus free time (t_{BUF} defined in the I²C Specifications) has elapsed after the STOP condition has been generated, the I2C*n*CTL.TXSTOP bit is cleared to 0 and the I2C*n*INTF.STOPIF bit is set to 1.

When setting the I2C*n*CTL.TXSTART bit to 1 while the I2C*n*INTF.TBEIF bit = 1 (transmit buffer empty) or the I2C*n*INTF.NACKIF bit = 1 (NACK received), the I2C Ch.*n* generates a repeated START condition. When the repeated START condition has been generated, the I2C*n*INTF.STARTIF and I2C*n*INTF.TBEIF bits are both set to 1 same as when a START condition has been generated.

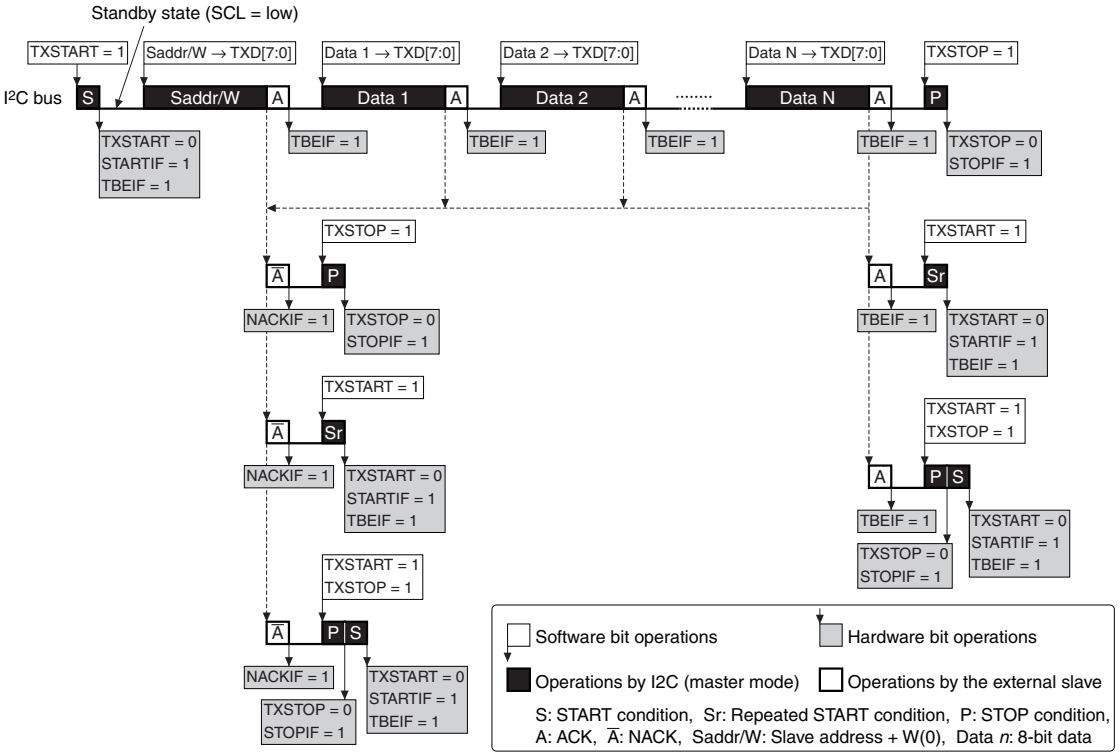


Figure 14.4.2.1 Example of Data Sending Operations in Master Mode

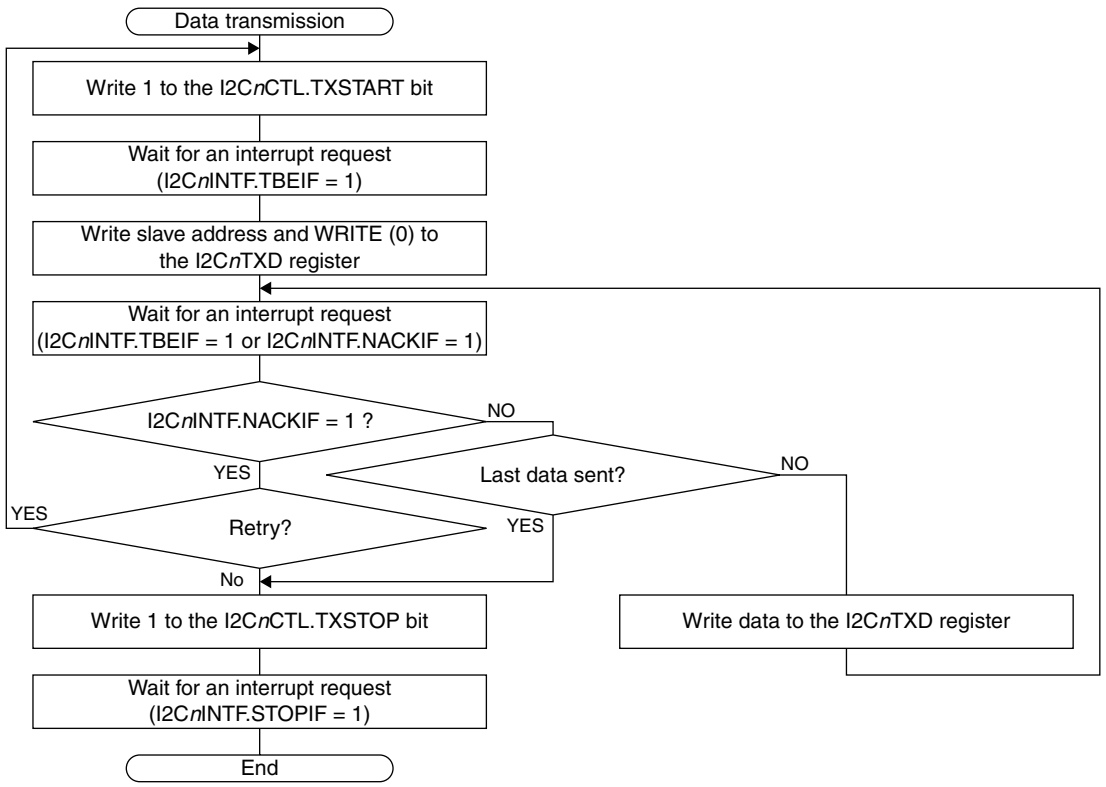


Figure 14.4.2.2 Master Mode Data Transmission Flowchart

14.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.*n* operations are shown below. Figures 14.4.3.1 and 14.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. When receiving one-byte data, write 1 to the I2C*n*CTL.TXNACK bit.
2. Issue a START condition by setting the I2C*n*CTL.TXSTART bit to 1.
3. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
4. Write the 7-bit slave address to the I2C*n*TXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2C*n*TXD.TXD0 bit.
5. Wait for a receive buffer full interrupt (I2C*n*INTF.RBFIF bit = 1) generated when a one-byte reception has completed or a NACK reception interrupt (I2C*n*INTF.NACKIF bit = 1) generated when a NACK is received.
   i. Go to Step 6 when a receive buffer full interrupt has occurred.
   ii. Clear the I2C*n*INTF.NACKIF bit and issue a STOP condition by setting the I2C*n*CTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 9 or Step 2 if making a retry.
6. Perform one of the operations below when the last or next-to-last data is received.
   i. When the next-to-last data is received, write 1 to the I2C*n*CTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 7.
   ii. When the last data is received, read the received data from the I2C*n*RXD register and set the I2C*n*CTL.TXSTOP to 1 to generate a STOP condition. Then go to Step 9.
7. Read the received data from the I2C*n*RXD register.
8. Repeat Steps 5 to 7 until the end of data reception.
9. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1).
   Clear the I2C*n*INTF.STOPIF bit by writing 1 after the interrupt has occurred.

Data receiving operations

Generating a START condition

It is the same as the data transmission in master mode.

Sending slave address

It is the same as the data transmission in master mode. Note, however, that the I2C*n*TXD.TXD0 bit must be set to 1 that represents READ as the data transfer direction to issue a request to the slave to send data.

Receiving data

After the slave address has been sent, the slave device sends an ACK and the first data. The I2C Ch.*n* sets the I2C*n*INTF.RBFIF bit to 1 after the data reception has completed. Furthermore, the I2C Ch.*n* returns an ACK. To return a NACK, such as for a response after the last data has been received, write 1 to the I2C*n*CTL.TXNACK bit before the I2C*n*INTF.RBFIF bit is set to 1.

The received data can be read out from the I2C*n*RXD register after a receive buffer full interrupt has occurred. The I2C Ch.*n* pulls down SCL to low and enters standby state until data is read out from the I2C*n*RXD register.

This reading triggers the I2C Ch.*n* to start subsequent data reception.

Generating a STOP or repeated START condition

It is the same as the data transmission in master mode.

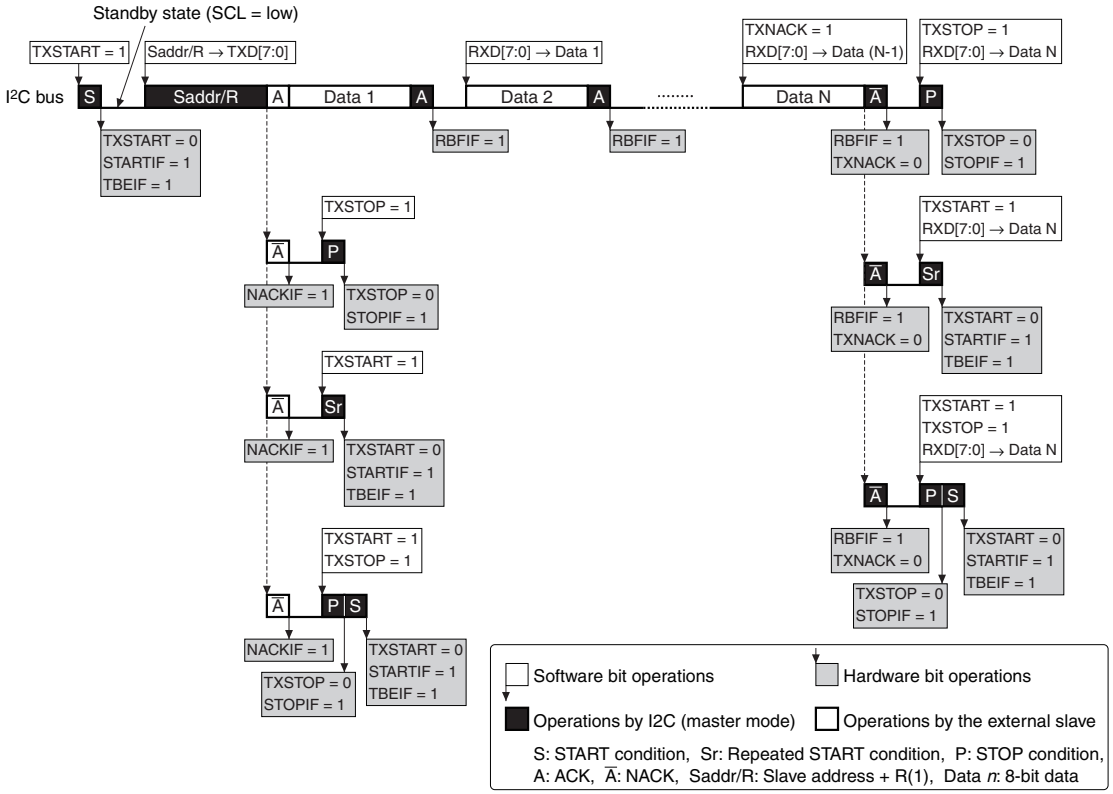


Figure 14.4.3.1 Example of Data Receiving Operations in Master Mode

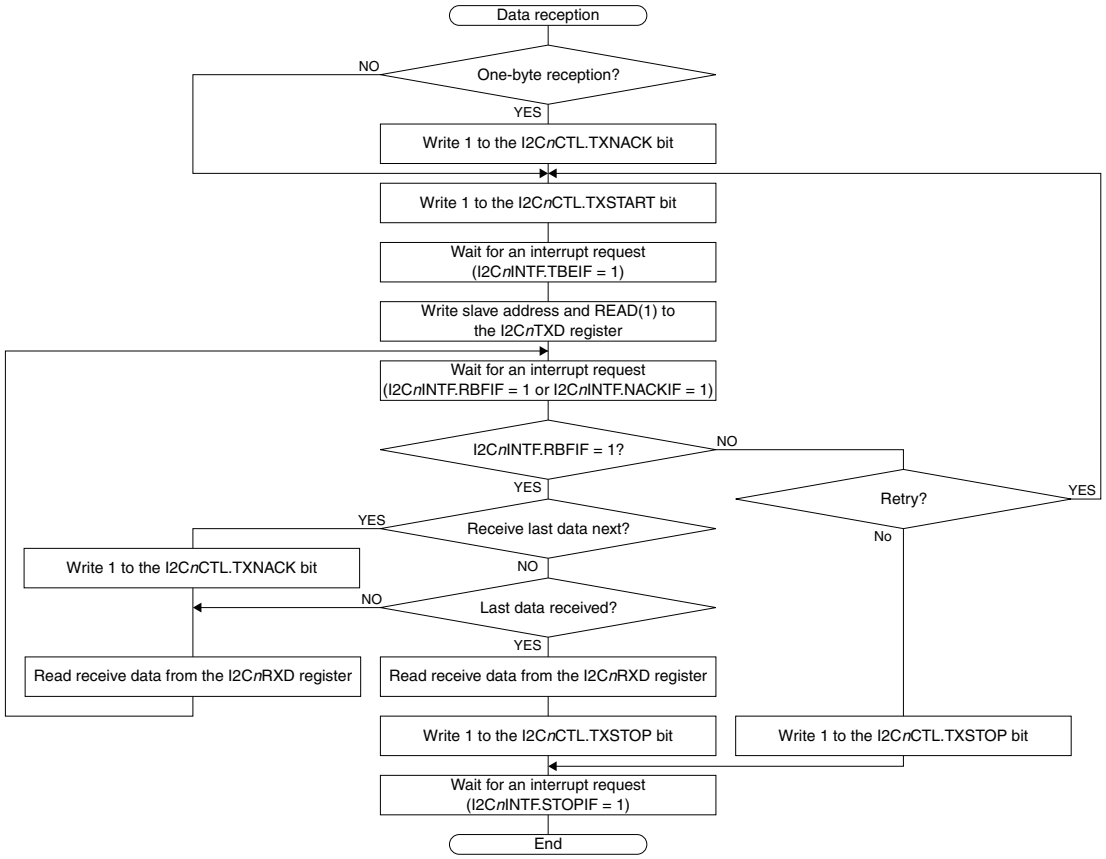


Figure 14.4.3.2 Master Mode Data Reception Flowchart

14.4.4 10-bit Addressing in Master Mode

A 10-bit address consists of the first address that contains two high-order bits and the second address that contains eight low-order bits.

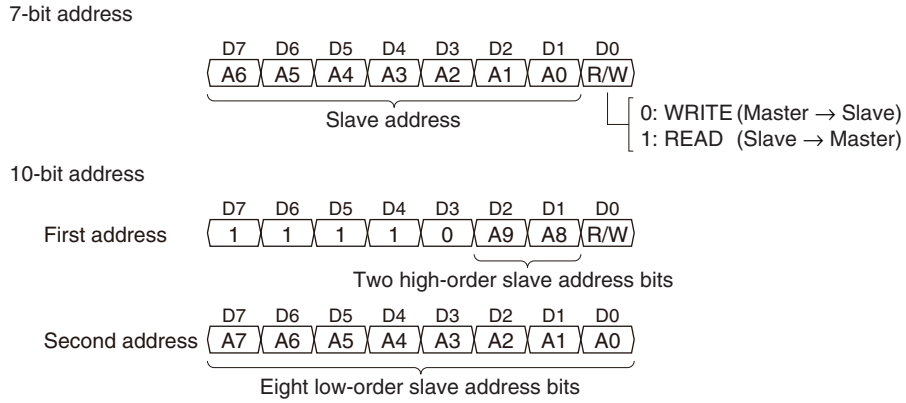


Figure 14.4.4.1 10-bit Address Configuration

The following shows a procedure to start data transfer in 10-bit address mode when the I2C Ch.*n* is placed into master mode (see the 7-bit mode descriptions above for control procedures when a NACK is received or sending/receiving data). Figure 14.4.4.2 shows an operation example.

Starting data transmission in 10-bit address mode

1. Issue a START condition by setting the I2C*n*CTL.TXSTART bit to 1.
2. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
3. Write the first address to the I2C*n*TXD.TXD[7:1] bits and 0 that represents WRITE as the data transfer direction to the I2C*n*TXD.TXD0 bit.
4. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1).
5. Write the second address to the I2C*n*TXD.TXD[7:0] bits.
6. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1).
7. Perform data transmission.

Starting data reception in 10-bit address mode

1 to 6. These steps are the same as the data transmission starting procedure described above.

7. Issue a repeated START condition by setting the I2C*n*CTL.TXSTART bit to 1.
8. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
9. Write the first address to the I2C*n*TXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2C*n*TXD.TXD0 bit.
10. Perform data reception.

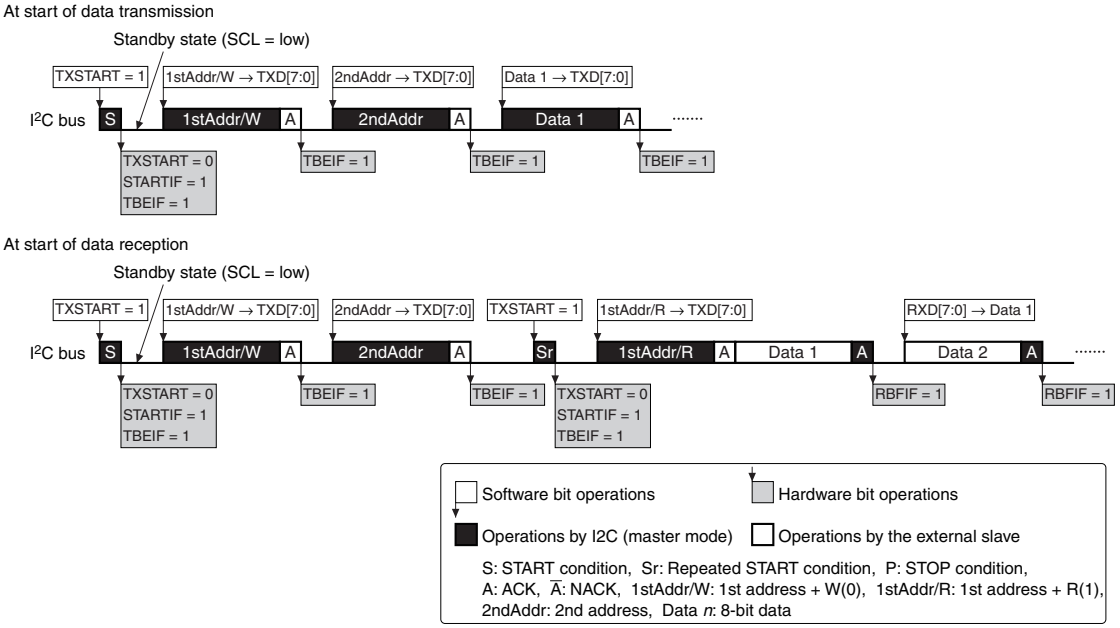


Figure 14.4.4.2 Example of Data Transfer Starting Operations in 10-bit Address Mode (Master Mode)

14.4.5 Data Transmission in Slave Mode

A data sending procedure in slave mode and the I2C Ch.*n* operations are shown below. Figures 14.4.5.1 and 14.4.5.2 show an operation example and a flowchart, respectively.

Data sending procedure

1. Wait for a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   Clear the I2C*n*INTF.STARTIF bit by writing 1 after the interrupt has occurred.
2. Check to see if the I2C*n*INTF.TR bit = 1 (transmission mode).
   (Start a data receiving procedure if the I2C*n*INTF.TR bit = 0.)
3. Write transmit data to the I2C*n*TXD register.
4. Wait for a transmit buffer empty interrupt (I2C*n*INTF.TBEIF bit = 1), a NACK reception interrupt (I2C*n*INTF.NACKIF bit = 1), or a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1).
   i. Go to Step 3 when a transmit buffer empty interrupt has occurred.
   ii. Go to Step 5 after clearing the I2C*n*INTF.NACKIF bit when a NACK reception interrupt has occurred.
   iii. Go to Step 6 when a STOP condition interrupt has occurred.
5. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   i. Go to Step 6 when a STOP condition interrupt has occurred.
   ii. Go to Step 2 when a START condition interrupt has occurred.
6. Clear the I2C*n*INTF.STOPIF bit and then terminate data sending operations.

Data sending operations

START condition detection and slave address check

While the I2C*n*CTL.MODEN bit = 1 and the I2C*n*CTL.MST bit = 0 (slave mode), the I2C Ch.*n* monitors the I²C bus. When the I2C Ch.*n* detects a START condition, it starts receiving of the slave address sent from the master. If the received address is matched with the own address set to the I2C*n*OADR.OADR[6:0] bits (when the I2C*n*MOD.OADR10 bit = 0 (7-bit address mode)) or the I2C*n*OADR.OADR[9:0] bits (when the I2C*n*MOD.OADR10 bit = 1 (10-bit address mode)), the I2C*n*INTF.STARTIF bit and the I2C*n*INTF.BSY bit are both set to 1. The I2C Ch.*n* sets the I2C*n*INTF.TR bit to the R/W bit value in the received address. If this value is 1, the I2C Ch.*n* sets the I2C*n*INTF.TBEIF bit to 1 and starts data sending operations.

Sending the first data byte

After the valid slave address has been received, the I2C Ch.*n* pulls down SCL to low and enters standby state until data is written to the I2C*n*TXD register. This puts the I²C bus into clock stretching state and the external master into standby state. When transmit data is written to the I2C*n*TXD register, the I2C Ch.*n* clears the I2C*n*INTF.TBEIF bit and sends an ACK to the master. The transmit data written in the I2C*n*TXD register is automatically transferred to the shift register and the I2C*n*INTF.TBEIF bit is set to 1. The data bits in the shift register are output in sequence to the I²C bus.

Sending subsequent data

If the I2C*n*INTF.TBEIF bit = 1, subsequent transmit data can be written during data transmission. If the I2C*n*INTF.TBEIF bit is still set to 1 when the data transmission from the shift register has completed, the I2C Ch.*n* pulls down SCL to low (sets the I²C bus into clock stretching state) until transmit data is written to the I2C*n*TXD register.

If the next transmit data already exists in the I2C*n*TXD register or data has been written after the above, the I2C Ch.*n* sends the subsequent eight-bit data when an ACK from the external master is received. At the same time, the I2C*n*INTF.BYTEENDIF bit is set to 1. If a NACK is received, the I2C*n*INTF.NACKIF bit is set to 1 without sending data.

STOP/repeated START condition detection

While the I2C*n*CTL.MST bit = 0 (slave mode) and the I2C*n*INTF.BSY = 1, the I2C Ch.*n* monitors the I²C bus. When the I2C Ch.*n* detects a STOP condition, it terminates data sending operations. At this time, the I2C*n*INTF.BSY bit is cleared to 0 and the I2C*n*INTF.STOPIF bit is set to 1. Also when the I2C Ch.*n* detects a repeated START condition, it terminates data sending operations. In this case, the I2C*n*INTF.STARTIF bit is set to 1.

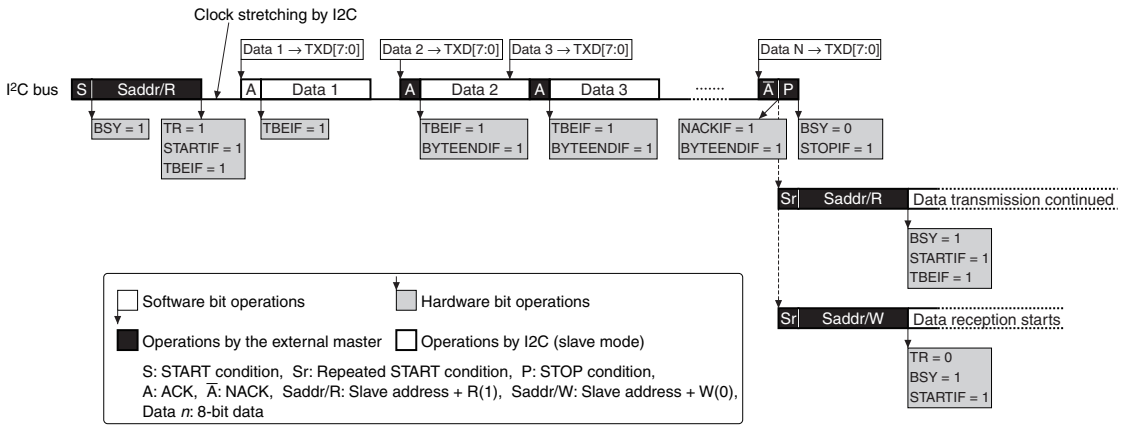


Figure 14.4.5.1 Example of Data Sending Operations in Slave Mode

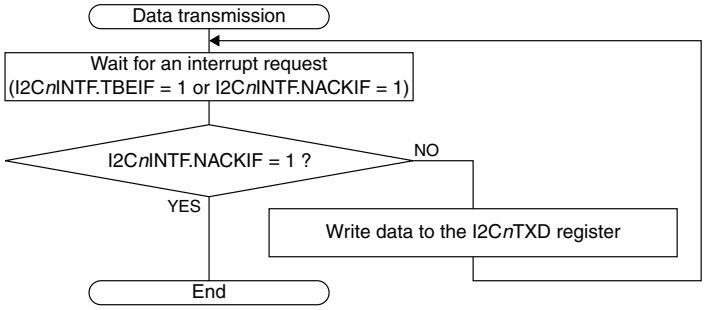


Figure 14.4.5.2 Slave Mode Data Transmission Flowchart

14.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.*n* operations are shown below. Figures 14.4.6.1 and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1. When receiving one-byte data, write 1 to the I2C*n*CTL.TXNACK bit.
2. Wait for a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
3. Check to see if the I2C*n*INTF.TR bit = 0 (reception mode).
   (Start a data sending procedure if I2C*n*INTF.TR bit = 1.)
4. Clear the I2C*n*INTF.STARTIF bit by writing 1.
5. Wait for a receive buffer full interrupt (I2C*n*INTF.RBFIF bit = 1) generated when a one-byte reception has completed or an end of transfer interrupt (I2C*n*INTF.BYTEENDIF bit = 1).
   Clear the I2C*n*INTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.
6. If the next receive data is the last one, write 1 to the I2C*n*CTL.TXNACK bit to send a NACK after it is received.
7. Read the received data from the I2C*n*RXD register.
8. Repeat Steps 5 to 7 until the end of data reception.
9. Wait for a STOP condition interrupt (I2C*n*INTF.STOPIF bit = 1) or a START condition interrupt (I2C*n*INTF.STARTIF bit = 1).
   i. Go to Step 10 when a STOP condition interrupt has occurred.
   ii. Go to Step 3 when a START condition interrupt has occurred.
10. Clear the I2C*n*INTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

START condition detection and slave address check

It is the same as the data transmission in slave mode.
However, the I2C*n*INTF.TR bit is cleared to 0 and the I2C*n*INTF.TBEIF bit is not set.
If the I2C*n*MOD.GCEN bit is set to 1 (general call address response enabled), the I2C Ch.*n* starts data receiving operations when the general call address is received.
Slave mode can be operated even in SLEEP mode, it makes it possible to wake the CPU up using an interrupt when an address match is detected.

Receiving the first data byte

After the valid slave address has been received, the I2C Ch.*n* sends an ACK and pulls down SCL to low until 1 is written to the I2C*n*INTF.STARTIF bit. This puts the I²C bus into clock stretching state and the external master into standby state. When 1 is written to the I2C*n*INTF.STARTIF bit, the I2C Ch.*n* releases SCL and receives data sent from the external master into the shift register. After eight-bit data has been received, the I2C Ch.*n* sends an ACK and pulls down SCL to low. The received data in the shift register is transferred to the receive data buffer and the I2C*n*INTF.RBFIF and I2C*n*INTF.BYTEENDIF bits are both set to 1. After that, the received data can be read out from the I2C*n*RXD register.

Receiving subsequent data

When the received data is read out from the I2C*n*RXD register after the I2C*n*INTF.RBFIF bit has been set to 1, the I2C Ch.*n* clears the I2C*n*INTF.RBFIF bit to 0, releases SCL, and receives subsequent data sent from the external master. After eight-bit data has been received, the I2C Ch.*n* sends an ACK and pulls down SCL to low. The received data in the shift register is transferred to the receive data buffer and the I2C*n*INTF.RBFIF and I2C*n*INTF.BYTEENDIF bits are both set to 1.

To return a NACK after eight-bit data is received, such as when terminating data reception, write 1 to the I2C*n*CTL.TXNACK bit before the data reception is completed. The I2C*n*CTL.TXNACK bit is automatically cleared to 0 after a NACK has been sent.

STOP/repeated START condition detection

It is the same as the data transmission in slave mode.

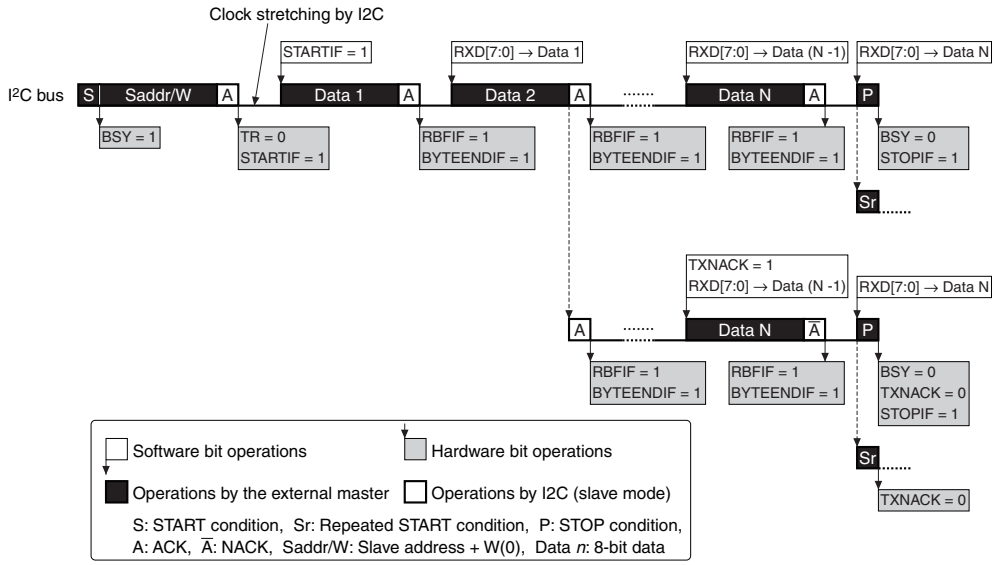


Figure 14.4.6.1 Example of Data Receiving Operations in Slave Mode

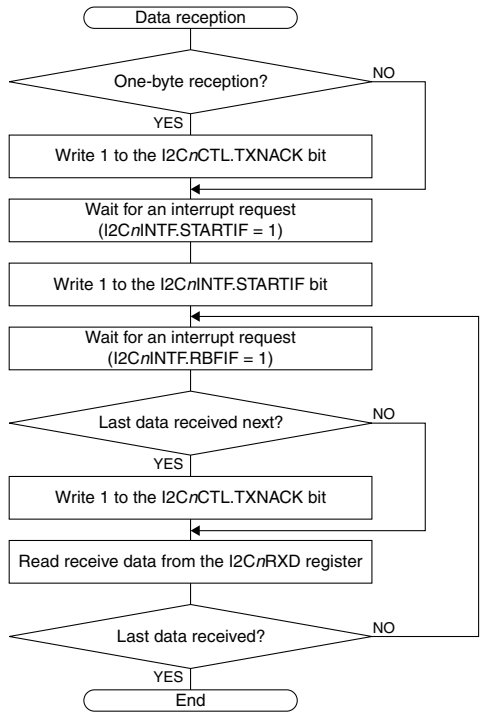


Figure 14.4.6.2 Slave Mode Data Reception Flowchart

14.4.7 Slave Operations in 10-bit Address Mode

The I2C Ch.*n* functions as a slave device in 10-bit address mode when the I2C*n*CTL.MST bit = 0 and the I2C*n*MOD.OADR10 bit = 1.

The following shows the address receiving operations in 10-bit address mode. Figure 14.4.7.1 shows an operation example. See Figure 14.4.4.1 for the 10-bit address configuration.

10-bit address receiving operations

After a START condition is issued, the master sends the first address that includes the two high-order slave address bits and the R/W bit (= 0). If the received two high-order slave address bits are matched with the I2C*n*OADR.OADR[9:8] bits, the I2C Ch.*n* returns an ACK. At this time, other slaves may returns an ACK as the two high-order bits may be matched.

Then the master sends the eight low-order slave address bits as the second address. If this address is matched with the I2C*n*OADR.OADR[7:0] bits, the I2C Ch.*n* returns an ACK and starts data receiving operations.

If the master issues a request to the slave to send data (data reception in the master), the master generates a repeated START condition and sends the first address with the R/W bit set to 1. This reception switches the I2C Ch.*n* to data sending mode.

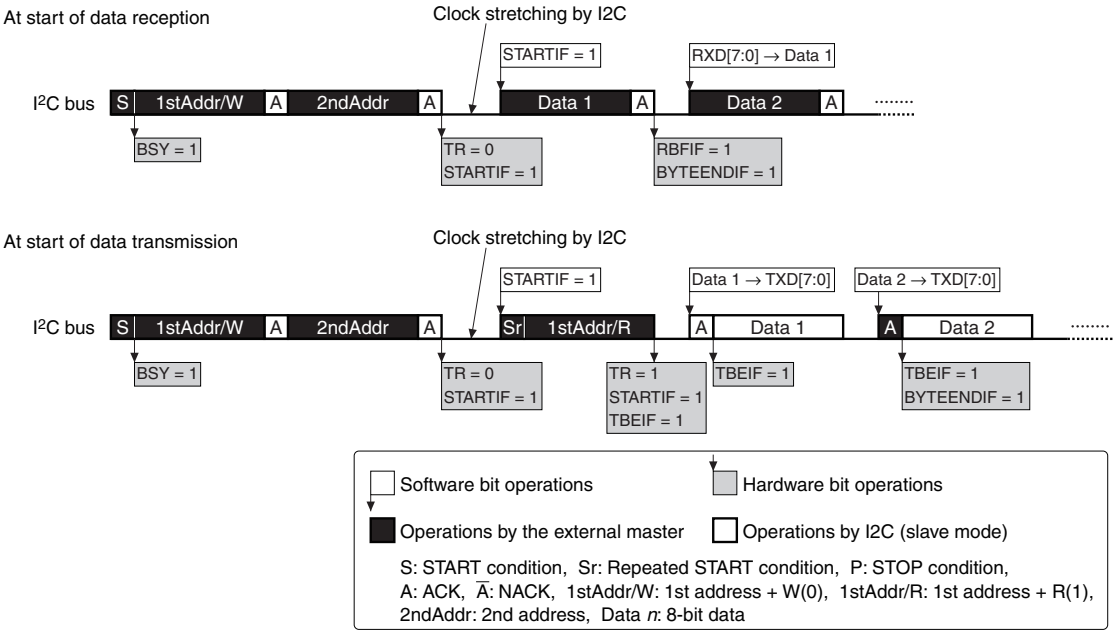


Figure 14.4.7.1 Example of Data Transfer Starting Operations in 10-bit Address Mode (Slave Mode)

14.4.8 Automatic Bus Clearing Operation

The I2C Ch.*n* set into master mode checks the SDA state immediately before generating a START condition. If SDA is set to a low level at this time, the I2C Ch.*n* automatically executes bus clearing operations that output up to ten clocks from the SCL*n* pin with SDA left free state.

When SDA goes high from low within nine clocks, the I2C Ch.*n* issues a START condition and starts normal operations. If SDA does not change from low when the I2C Ch.*n* outputs the ninth clock, it is regarded as an automatic bus clearing failure. In this case, the I2C Ch.*n* clears the I2C*n*CTL.TXSTART bit to 0 and sets both the I2C*n*INTF.ERRIF and I2C*n*INTF.STARTIF bits to 1.

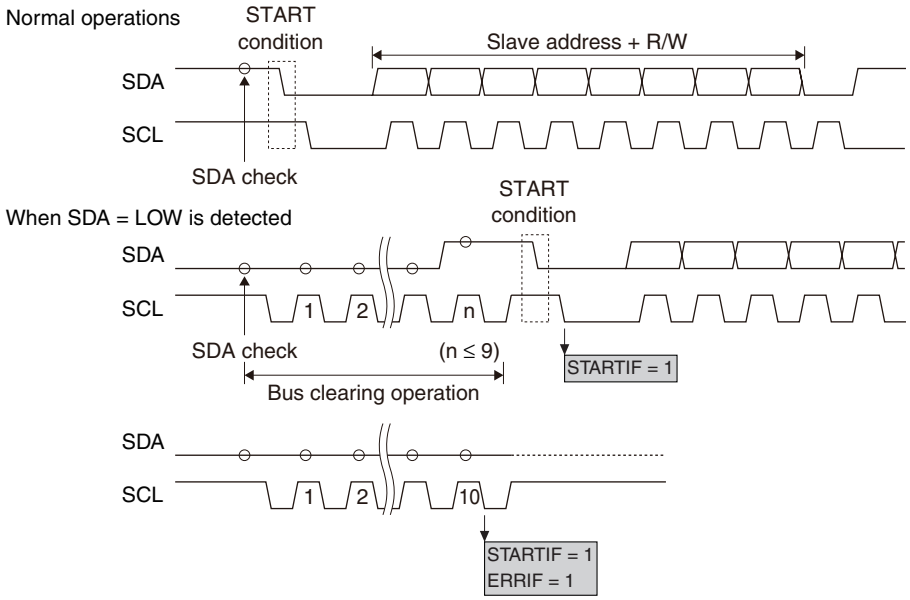


Figure 14.4.8.1 Automatic Bus Clearing Operation

14.4.9 Error Detection

The I2C includes a hardware error detection function.
Furthermore, the I2C*n*INTF.SDALOW and I2C*n*INTF.SCLLOW bits are provided to allow software to check whether the SDA and SCL lines are fixed at low. If unintended low level is detected on SDA or SCL, a software recovery processing, such as I2C Ch.*n* software reset, can be performed.

The table below lists the hardware error detection conditions and the notification method.

Table 14.4.9.1 Hardware Error Detection Function

No.	Error detecting period/timing	I²C bus line monitored and error condition	Notification method
1	While the I2C Ch.*n* controls SDA to high for sending address, data, or a NACK	SDA = low	I2C*n*INTF.ERRIF = 1
2	<Master mode only> When 1 is written to the I2C*n*CTL.TXSTART bit while the I2C*n*INTF.BSY bit = 0	SCL = low	I2C*n*INTF.ERRIF = 1 I2C*n*CTL.TXSTART = 0 I2C*n*INTF.STARTIF = 1
3	<Master mode only> When 1 is written to the I2C*n*CTL.TXSTOP bit while the I2C*n*INTF.BSY bit = 0	SCL = low	I2C*n*INTF.ERRIF = 1 I2C*n*CTL.TXSTOP = 0 I2C*n*INTF.STOPIF = 1
4	<Master mode only> When 1 is written to the I2C*n*CTL.TXSTART bit while the I2C*n*INTF.BSY bit = 0 (Refer to "Automatic Bus Clearing Operation.")	SDA Automatic bus clearing failure	I2C*n*INTF.ERRIF = 1 I2C*n*CTL.TXSTART = 0 I2C*n*INTF.STARTIF = 1

14.5 Interrupts

The I2C has a function to generate the interrupts shown in Table 14.5.1.

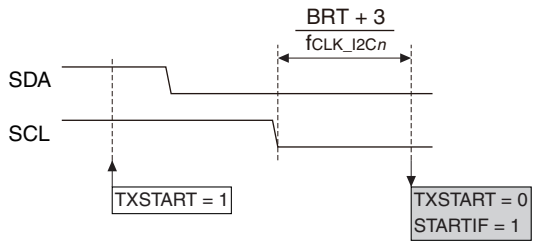
Table 14.5.1 I2C Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
End of data transfer	I2C*n*INTF.BYTEENDIF	When eight-bit data transfer and the following ACK/NACK transfer are completed	Writing 1, software reset
General call address reception	I2C*n*INTF.GCIF	Slave mode only: When the general call address is received	Writing 1, software reset
NACK reception	I2C*n*INTF.NACKIF	When a NACK is received	Writing 1, software reset
STOP condition	I2C*n*INTF. STOPIF	Master mode: When a STOP condition is generated and the bus free time (t_{BUF}) between STOP and START conditions has elapsed Slave mode: When a STOP condition is detected while the I2C Ch.*n* is selected as the slave currently accessed	Writing 1, software reset
START condition	I2C*n*INTF. STARTIF	Master mode: When a START condition is issued Slave mode: When an address match is detected (including general call)	Writing 1, software reset
Error detection	I2C*n*INTF. ERRIF	Refer to "Error Detection."	Writing 1, software reset
Receive buffer full	I2C*n*INTF. RBFIF	When received data is loaded to the receive data buffer	Reading received data (to empty the receive data buffer), software reset
Transmit buffer empty	I2C*n*INTF. TBEIF	Master mode: When a START condition is issued or when an ACK is received from the slave Slave mode: When transmit data written to the transmit data buffer is transferred to the shift register or when an address match is detected with R/W bit set to 1	Writing transmit data

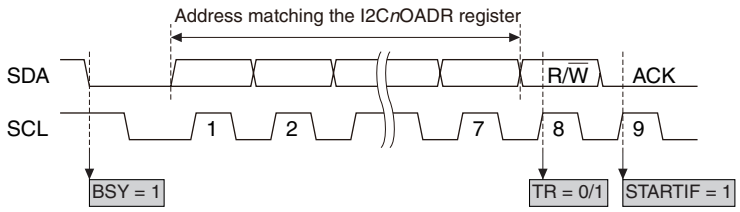
The I2C provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

(1) START condition interrupt

Master mode

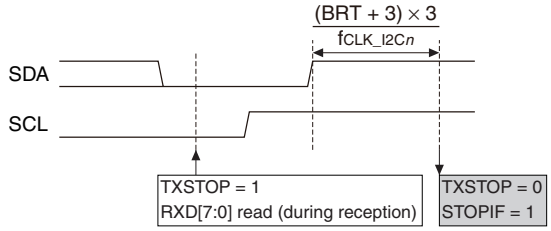


Slave mode

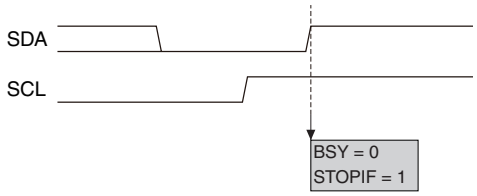


(2) STOP condition interrupt

Master mode



Slave mode



(f_{CLK_I2Cn}: I2C operating clock frequency [Hz], BRT: I2C*n*BR.BRT[6:0] bits setting value (1 to 127))

Figure 14.5.1 START/STOP Condition Interrupt Timings

14.6 Control Registers

I2C Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–6	–	0x0	–	R	
	5–4	CLKDIV[1:0]	0x0	H0	R/W	
	3–2	–	0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the I2C operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–6 Reserved

Bits 5–4 CLKDIV[1:0]

These bits select the division ratio of the I2C operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the I2C.

Table 14.6.1 Clock Source and Division Ratio Settings

I2C*n*CLK.CLKDIV[1:0] bits	I2C*n*CLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0x3	1/8	1/1	1/8	1/1
0x2	1/4		1/4	
0x1	1/2		1/2	
0x0	1/1		1/1	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The I2C*n*CLK register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

I2C Ch.*n* Mode Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*MOD	15–8	–	0x00	–	R	–
	7–3	–	0x00	–	R	
	2	OADR10	0	H0	R/W	
	1	GCEN	0	H0	R/W	
	0	–	0	–	R	

Bits 15–3 Reserved

Bit 2 OADR10

This bit sets the number of own address bits for slave mode.
1 (R/W): 10-bit address
0 (R/W): 7-bit address

Bit 1 GCEN

This bit sets whether to respond to master general calls in slave mode or not.
1 (R/W): Respond to general calls.
0 (R/W): Do not respond to general calls.

Bit 0 Reserved

Note: The I2C*n*MOD register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

I2C Ch.*n* Baud-Rate Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*BR	15–8	–	0x00	–	R	–
	7	–	0	–	R	
	6–0	BRT[6:0]	0x7f	H0	R/W	

Bits 15–7 Reserved

Bits 6–0 BRT[6:0]

These bits set the I2C Ch.*n* transfer rate for master mode. For more information, refer to "Baud Rate Generator."

Notes: • The I2C*n*BR register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

• Be sure to avoid setting the I2C*n*BR register to 0.

I2C Ch.*n* Own Address Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*OADR	15–10	–	0x00	–	R	–
	9–0	OADR[9:0]	0x000	H0	R/W	

Bits 15–10 Reserved

Bits 9–0 OADR[9:0]

These bits set the own address for slave mode.
The I2C*n*OADR.OADR[9:0] bits are effective in 10-bit address mode (I2C*n*MOD.OADR10 bit = 1), or the I2C*n*OADR.OADR[6:0] bits are effective in 7-bit address mode (I2C*n*MOD.OADR10 bit = 0).

Note: The I2C*n*OADR register settings can be altered only when the I2C*n*CTL.MODEN bit = 0.

I2C Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*CTL	15–8	–	0x00	–	R	–
	7–6	–	0x0	–	R	
	5	MST	0	H0	R/W	
	4	TXNACK	0	H0/S0	R/W	
	3	TXSTOP	0	H0/S0	R/W	
	2	TXSTART	0	H0/S0	R/W	
	1	SFTRST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–6 Reserved

Bit 5 MST

This bit selects the I2C Ch.*n* operating mode.

1 (R/W): Master mode

0 (R/W): Slave mode

Bit 4 TXNACK

This bit issues a request for sending a NACK at the next responding.

1 (W): Issue a NACK.

0 (W): Ineffective

1 (R): On standby or during sending a NACK

0 (R): NACK has been sent.

This bit is automatically cleared after a NACK has been sent.

Bit 3 TXSTOP

This bit issues a STOP condition in master mode. This bit is ineffective in slave mode.

1 (W): Issue a STOP condition.

0 (W): Ineffective

1 (R): On standby or during generating a STOP condition

0 (R): STOP condition has been generated.

This bit is automatically cleared when the bus free time (t_{BUF} defined in the I²C Specifications) has elapsed after the STOP condition has been generated.

Bit 2 TXSTART

This bit issues a START condition in master mode. This bit is ineffective in slave mode.

1 (W): Issue a START condition.

0 (W): Ineffective

1 (R): On standby or during generating a START condition

0 (R): START condition has been generated.

This bit is automatically cleared when a START condition has been generated.

Bit 1 SFTRST

This bit issues software reset to the I2C.

1 (W): Issue software reset

0 (W): Ineffective

1 (R): Software reset is executing.

0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the I2C transmit/receive control circuit and interrupt flags. This bit is automatically cleared after the reset processing has finished.

Bit 0 MODEN

This bit enables the I2C operations.

1 (R/W): Enable I2C operations (The operating clock is supplied.)

0 (R/W): Disable I2C operations (The operating clock is stopped.)

Note: If the I2C*n*CTL.MODEN bit is altered from 1 to 0 while sending/receiving data, the data being sent/received cannot be guaranteed. When setting the I2C*n*CTL.MODEN bit to 1 again after that, be sure to write 1 to the I2C*n*CTL.SFTRST bit as well.

I2C Ch.*n* Transmit Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*TXD	15–8	–	0x00	–	R	–
	7–0	TXD[7:0]	0x00	H0	R/W	

Bits 15–8 Reserved

Bits 7–0 TXD[7:0]

Data can be written to the transmit data buffer through these bits. Make sure the I2C*n*INTF.TBEIF bit is set to 1 before writing data.

Note: Be sure to avoid writing to the I2C*n*TXD register when the I2C*n*INTF.TBEIF bit = 0, otherwise transmit data cannot be guaranteed.

I2C Ch.*n* Receive Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*RXD	15–8	–	0x00	–	R	–
	7–0	RXD[7:0]	0x00	H0	R	

Bits 15–8 Reserved

Bits 7–0 RXD[7:0]

The receive data buffer can be read through these bits.

I2C Ch.*n* Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*INTF	15–13	–	0x0	–	R	–
	12	SDALOW	0	H0	R	
	11	SCLLOW	0	H0	R	
	10	BSY	0	H0/S0	R	
	9	TR	0	H0	R	
	8	–	0	–	R	
	7	BYTEENDIF	0	H0/S0	R/W	Cleared by writing 1.
	6	GCIF	0	H0/S0	R/W	
	5	NACKIF	0	H0/S0	R/W	
	4	STOPIF	0	H0/S0	R/W	
	3	STARTIF	0	H0/S0	R/W	
	2	ERRIF	0	H0/S0	R/W	
	1	RBFIF	0	H0/S0	R	Cleared by reading the I2C*n*RXD register.
	0	TBEIF	0	H0/S0	R	Cleared by writing to the I2C*n*TXD register.

Bits 15–13 Reserved

Bit 12 SDALOW

This bit indicates that SDA is set to low level.

1 (R): SDA = Low level

0 (R): SDA = High level

Bit 11 SCLLOW

This bit indicates that SCL is set to low level.

1 (R): SCL = Low level

0 (R): SCL = High level

Bit 10 BSY

This bit indicates that the I²C bus is placed into busy status.

1 (R): I²C bus busy

0 (R): I²C bus free

Bit 9 TR

This bit indicates whether the I2C is set in transmission mode or not.

1 (R): Transmission mode

0 (R): Reception mode

Bit 8 Reserved

Bit 7 BYTEENDIF
Bit 6 GCIF
Bit 5 NACKIF
Bit 4 STOPIF
Bit 3 STARTIF
Bit 2 ERRIF
Bit 1 RBFIF
Bit 0 TBEIF

These bits indicate the I2C interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

I2C*n*INTF.BYTEENDIF bit: End of transfer interrupt
I2C*n*INTF.GCIF bit: General call address reception interrupt
I2C*n*INTF.NACKIF bit: NACK reception interrupt
I2C*n*INTF.STOPIF bit: STOP condition interrupt
I2C*n*INTF.STARTIF bit: START condition interrupt
I2C*n*INTF.ERRIF bit: Error detection interrupt
I2C*n*INTF.RBFIF bit: Receive buffer full interrupt
I2C*n*INTF.TBEIF bit: Transmit buffer empty interrupt

I2C Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
I2C*n*INTE	15–8	–	0x00	–	R	–
	7	BYTEENDIE	0	H0	R/W	
	6	GCIE	0	H0	R/W	
	5	NACKIE	0	H0	R/W	
	4	STOPIE	0	H0	R/W	
	3	STARTIE	0	H0	R/W	
	2	ERRIE	0	H0	R/W	
	1	RBFIE	0	H0	R/W	
	0	TBEIE	0	H0	R/W	

Bits 15–8 Reserved

Bit 7 BYTEENDIE
Bit 6 GCIE
Bit 5 NACKIE
Bit 4 STOPIE
Bit 3 STARTIE
Bit 2 ERRIE
Bit 1 RBFIE
Bit 0 TBEIE

These bits enable I2C interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
I2C*n*INTE.BYTEENDIE bit: End of transfer interrupt
I2C*n*INTE.GCIE bit: General call address reception interrupt
I2C*n*INTE.NACKIE bit: NACK reception interrupt
I2C*n*INTE.STOPIE bit: STOP condition interrupt
I2C*n*INTE.STARTIE bit: START condition interrupt
I2C*n*INTE.ERRIE bit: Error detection interrupt
I2C*n*INTE.RBFIE bit: Receive buffer full interrupt
I2C*n*INTE.TBEIE bit: Transmit buffer empty interrupt

15 16-bit PWM Timers (T16B)

15.1 Overview

T16B is a 16-bit PWM timer with comparator/capture functions. The features of T16B are listed below.

- Counter block
  - 16-bit up/down counter
  - A clock source and a clock division ratio for generating the count clock are selectable in each channel.
  - The count mode is configurable from combinations of up, down, or up/down count operations, and one-shot operations (counting for one cycle configured) or repeat operations (counting continuously until stopped via software).
  - Supports an event counter function using an external clock.
- Comparator/capture block
  - Supports up to six comparator/capture circuits to be included per one channel.
  - The comparator compares the counter value with the values specified via software to generate interrupt signals and a PWM waveform. (Can be used as an interval timer, PWM waveform generator, and external event counter.)
  - The capture circuit captures counter values using external/software trigger signals and generates interrupts. (Can be used to measure external event periods/cycles.)

Figure 15.1.1 shows the T16B configuration.

Table 15.1.1 T16B Channel Configuration of S1C17589

Item	S1C17589
Number of channels	4 channels (Ch.0–Ch.3)
Event counter function	Ch.0: EXCL00 or EXCL01 pin input Ch.1: EXCL10 or EXCL11 pin input Ch.2: EXCL20 or EXCL21 pin input Ch.3: EXCL30 or EXCL31 pin input
Number of comparator/ capture circuits per channel	6 systems (0 to 5)
Timer generating signal output	Ch.0: TOUT00 to TOUT05 pin outputs (6 systems) Ch.1: TOUT10 to TOUT15 pin outputs (6 systems) Ch.2: TOUT20 to TOUT25 pin outputs (6 systems) Ch.3: TOUT30 to TOUT35 pin outputs (6 systems)
Capture signal input	Ch.0: CAP00 to CAP05 pin inputs (6 systems) Ch.1: CAP10 to CAP15 pin inputs (6 systems) Ch.2: CAP20 to CAP25 pin inputs (6 systems) Ch.3: CAP30 to CAP35 pin inputs (6 systems)

Note: In this chapter, '*n*' refers to a channel number, and '*m*' refers to an input/output pin number or a comparator/capture circuit number in a channel.

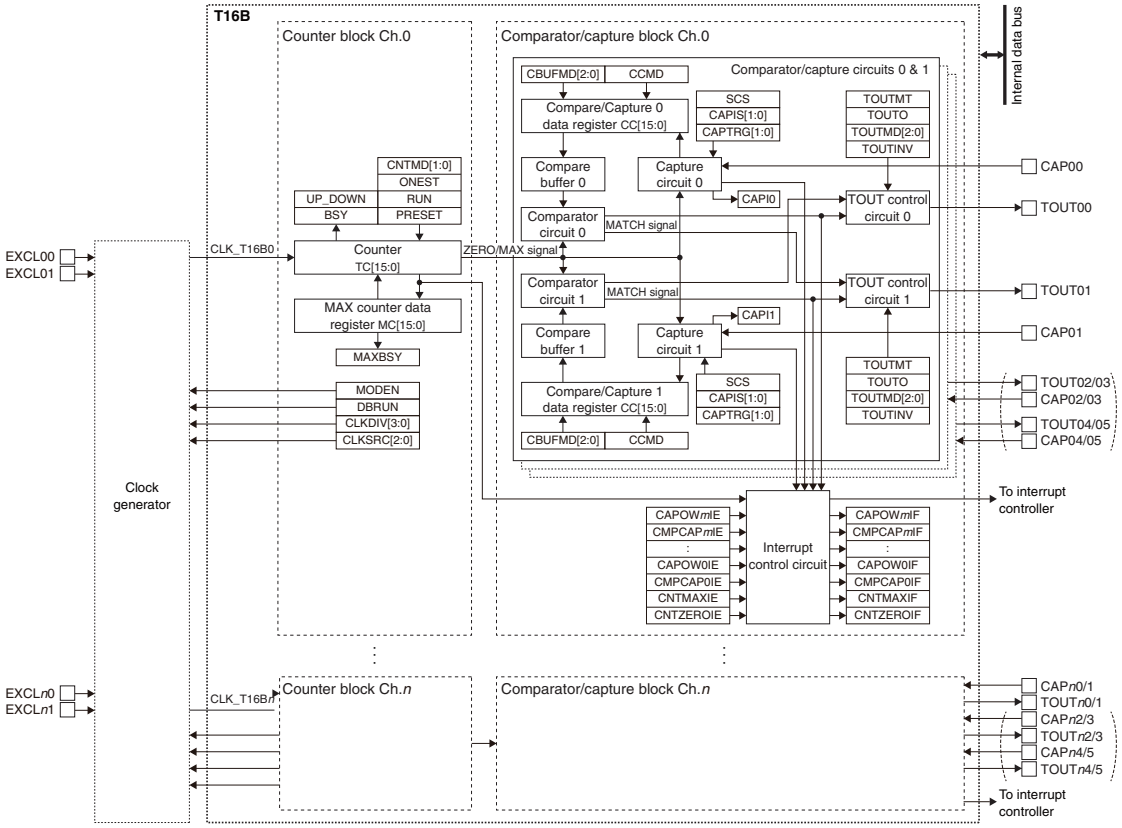


Figure 15.1.1 T16B Configuration

15.2 Input/Output Pins

Table 15.2.1 lists the T16B pins.

Table 15.2.1 List of T16B Pins

Pin name	I/O*	Initial status*	Function
EXCL*nm*	I	I (Hi-Z)	External clock input
TOUT*nm*/CAP*nm*	O or I	O (L)	TOUT signal output (in comparator mode) or capture trigger signal input (in capture mode)

* Indicates the status when the pin is configured for T16B.

If the port is shared with the T16B pin and other functions, the T16B input/output function must be assigned to the port before activating T16B. For more information, refer to the "I/O Ports" chapter.

15.3 Clock Settings

15.3.1 T16B Operating Clock

When using T16B Ch.*n*, the T16B Ch.*n* operating clock CLK_T16B*n* must be supplied to T16B Ch.*n* from the clock generator. The CLK_T16B*n* supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).

   When an external clock is used, select the EXCL*nm* pin function (refer to the "I/O Ports" chapter).
2. Set the following T16B*n*CLK register bits:
   - T16B*n*CLK.CLKSRC[2:0] bits (Clock source selection)
   - T16B*n*CLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)

15.3.2 Clock Supply in SLEEP Mode

When using T16B during SLEEP mode, the T16B operating clock CLK_T16B*n* must be configured so that it will keep supplying by writing 0 to the CLGOSC.*xxxx*SLPC bit for the CLK_T16B*n* clock source.
If the CLGOSC.*xxxx*SLPC bit for the CLK_T16B*n* clock source is 1, the CLK_T16B*n* clock source is deactivated during SLEEP mode and T16B stops with the register settings and counter value maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_T16B*n* is supplied and the T16B operation resumes.

15.3.3 Clock Supply in DEBUG Mode

The CLK_T16B*n* supply during DEBUG mode should be controlled using the T16B*n*CLK.DBRUN bit.
The CLK_T16B*n* supply to T16B Ch.*n* is suspended when the CPU enters DEBUG mode if the T16B*n*CLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_T16B*n* supply resumes. Although T16B Ch.*n* stops operating when the CLK_T16B*n* supply is suspended, the counter and registers retain the status before DEBUG mode was entered. If the T16B*n*CLK.DBRUN bit = 1, the CLK_T16B*n* supply is not suspended and T16B Ch.*n* will keep operating in DEBUG mode.

15.3.4 Event Counter Clock

When EXCL*nm* is selected as the clock source using the T16B*n*CLK.CLKSRC[2:0] bits, the channel functions as a timer or event counter that counts the EXCL*nm* pin input clocks.
The counter counts rising edges of the input signal. This can be changed so that the counter will count falling edges of the original signal by selecting EXCL*nm* inverted input as the clock source.

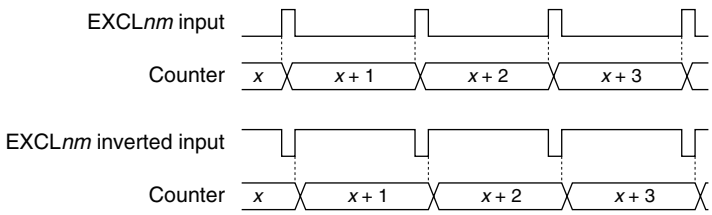


Figure 15.3.4.1 Count Timing (During Count Up Operation)

Note: When running the counter using the event counter clock, two dummy clocks must be input before the first counting up/down can be performed.

15.4 Operations

15.4.1 Initialization

T16B Ch.*n* should be initialized and started counting with the procedure shown below. Perform initial settings for comparator mode when using T16B as an interval timer, PWM waveform generator, or external event counter. Perform initial settings for capture mode when using T16B to measure external event periods/cycles.

Initial settings for comparator mode

1. Configure the T16B Ch.*n* operating clock.
2. Set the T16B*n*CTL.MODEN bit to 1. (Enable T16B operations)
3. Set the following T16B*n*CCCTL0 and T16B*n*CCCTL1 register bits:
   - Set the T16B*n*CCCTL*m*.CCMD bit to 0. * (Set comparator mode)
   - T16B*n*CCCTL*m*.CBUFMD[2:0] bits (Configure compare buffer)

   * Another circuit in the comparator/capture circuit pair (circuits 0 and 1, 2 and 3, 4 and 5) can be set to capture mode.

   Set the following bits when the TOUT*nm* output is used.
   - T16B*n*CCCTL*m*.TOUTMT bit (Select waveform generation signal)
   - T16B*n*CCCTL*m*.TOUTMD[2:0] bits (Select TOUT signal generation mode)
   - T16B*n*CCCTL*m*.TOUTINV bit (Select TOUT signal polarity)
4. Set the T16B*n*MC register. (Set MAX counter data)
5. Set the T16B*n*CCR0 and T16B*n*CCR1 registers. (Set the counter comparison value)
6. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the T16B*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the T16B*n*INTE register to 1. (Enable interrupts)
7. Set the following T16B*n*CTL register bits:
   - T16B*n*CTL.CNTMD[1:0] bits (Select count up/down operation)
   - T16B*n*CTL.ONEST bit (Select one-shot/repeat operation)
   - Set the T16B*n*CTL.PRESET bit to 1. (Reset counter)
   - Set the T16B*n*CTL.RUN bit to 1. (Start counting)

Initial settings for capture mode

1. Configure the T16B Ch.*n* operating clock.
2. Set the T16B*n*CTL.MODEN bit to 1. (Enable T16B operations)
3. Set the following T16B*n*CCCTL0 and T16B*n*CCCTL1 register bits:
   - Set the T16B*n*CCCTL*m*.CCMD bit to 1. * (Set capture mode)
   - T16B*n*CCCTL*m*.SCS bit (Set synchronous/asynchronous mode)
   - T16B*n*CCCTL*m*.CAPIS[1:0] bits (Set trigger signal)
   - T16B*n*CCCTL*m*.CAPTRG[1:0] bits (Select trigger edge)

   * Another circuit in the comparator/capture circuit pair (circuits 0 and 1, 2 and 3, 4 and 5) can be set to comparator mode.
4. Set the T16B*n*MC register. (Set MAX counter data)
5. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the T16B*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the T16B*n*INTE register to 1. (Enable interrupts)
6. Set the following T16B*n*CTL register bits:
   - T16B*n*CTL.CNTMD[1:0] bits (Select count up/down operation)
   - T16B*n*CTL.ONEST bit (Select one-shot/repeat operation)
   - Set the T16B*n*CTL.PRESET bit to 1. (Reset counter)
   - Set the T16B*n*CTL.RUN bit to 1. (Start counting)

15.4.2 Counter Block Operations

The counter in each counter block channel is a 16-bit up/down counter that counts the selected operating clock (count clock).

Count mode

The T16B*n*CTL.CNTMD[1:0] bits allow selection of up, down, and up/down mode. The T16B*n*CTL.ONEST bit allows selection of repeat and one-shot mode. The counter operates in six counter modes specified with a combination of these modes.

Repeat mode enables the counter to continue counting until stopped via software. Select this mode to generate periodic interrupts at desired intervals or to generate timer output waveforms.

One-shot mode enables the counter to stop automatically. Select this mode to stop the counter after an interrupt has occurred once, such as for measuring pulse width or external event intervals and checking a specific lapse of time.

Up, down, and up/down mode configures the counter as an up counter, down counter and up/down counter, respectively.

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

1. Check to see if the T16B*n*CTL.MAXBSY bit is set to 0.
2. Write the MAX value to the T16B*n*MC.MC[15:0] bits.

Note: When rewriting the MAX value, the new MAX value should be written after the counter has been reset to the previously set MAX value.

Counter reset

Setting the T16B*n*CTL.PRESET bit to 1 resets the counter. This clears the counter to 0x0000 in up or up/down mode, or presets the MAX value to the counter in down mode. The counter is also cleared to 0x0000 when the counter value exceeds the MAX value during count up operation.

Counting start

To start counting, set the T16B*n*CTL.RUN bit to 1. The counting stop control depends on the count mode set.

Counter value read

The counter value can be read out from the T16B*n*TC.TC[15:0] bits. However, since T16B operates on CLK_T16B*n*, one of the operations shown below is required to read correctly by the CPU.

- Read the counter value twice or more and check to see if the same value is read.
- Stop the timer and then read the counter value.

Counter status check

The counter operating status can be checked using the T16B*n*CS.BSY bit. The T16B*n*CS.BSY bit is set to 1 while the counter is running or 0 while the counter is idle.

The current count direction can also be checked using the T16B*n*CS.UP_DOWN bit. The T16B*n*CS.UP_DOWN bit is set to 1 during count up operation or 0 during count down operation.

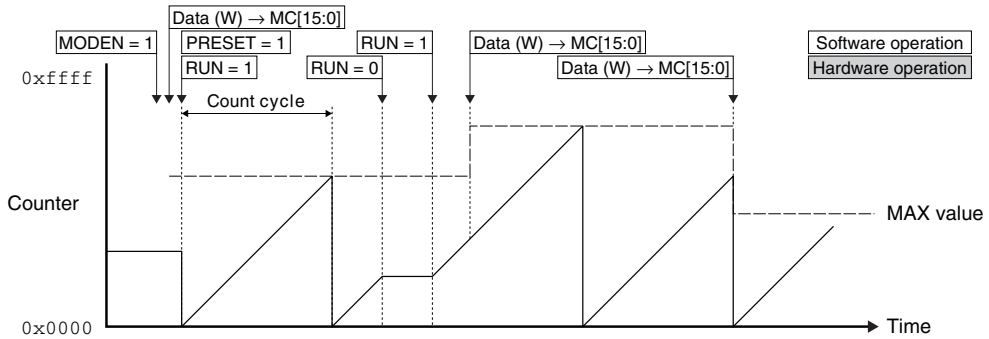
Operations in repeat up count and one-shot up count modes

In these modes, the counter operates as an up counter and counts from 0x0000 (or current value) to the MAX value.

In repeat up count mode, the counter returns to 0x0000 if it exceeds the MAX value and continues counting until the T16B*n*CTL.RUN bit is set to 0. If the MAX value is altered to a value larger than the current counter value during counting, the counter keeps counting up to the new MAX value. If the MAX value is altered to a value smaller than the current counter value, the counter is cleared to 0x0000 and continues counting up to the new MAX value.

In one-shot up count mode, the counter returns to 0x0000 if it exceeds the MAX value and stops automatically at that point.

(1) Repeat up count mode



(2) One-shot up count mode

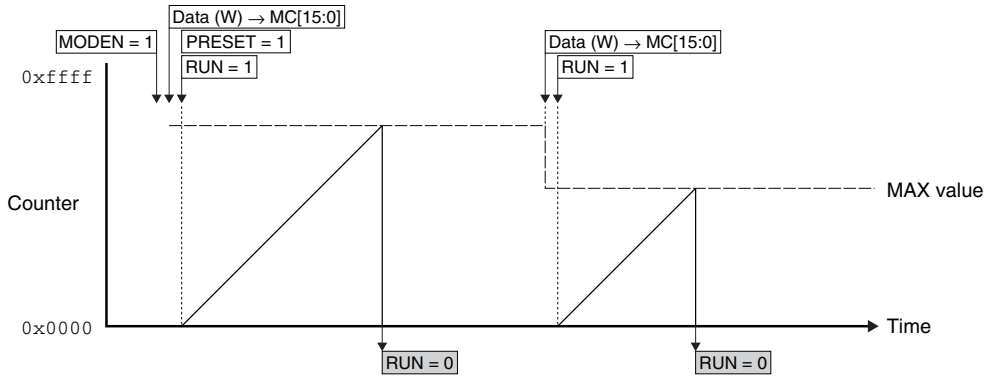


Figure 15.4.2.1 Operations in Repeat Up Count and One-shot Up Count Modes

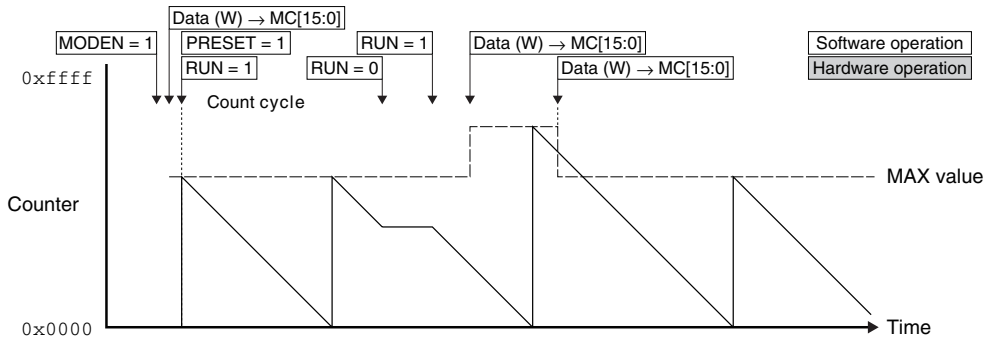
Operations in repeat down count and one-shot down count modes

In these modes, the counter operates as a down counter and counts from the MAX value (or current value) to 0x0000.

In repeat down count mode, the counter returns to the MAX value if a counter underflow occurs and continues counting until the T16B*n*CTL.RUN bit is set to 0. If the MAX value is altered during counting, the counter keeps counting down to 0x0000 and continues counting down from the new MAX value after a counter underflow occurs.

In one-shot down count mode, the counter returns to the MAX value if a counter underflow occurs and stops automatically at that point.

(1) Repeat down count mode



(2) One-shot down count mode

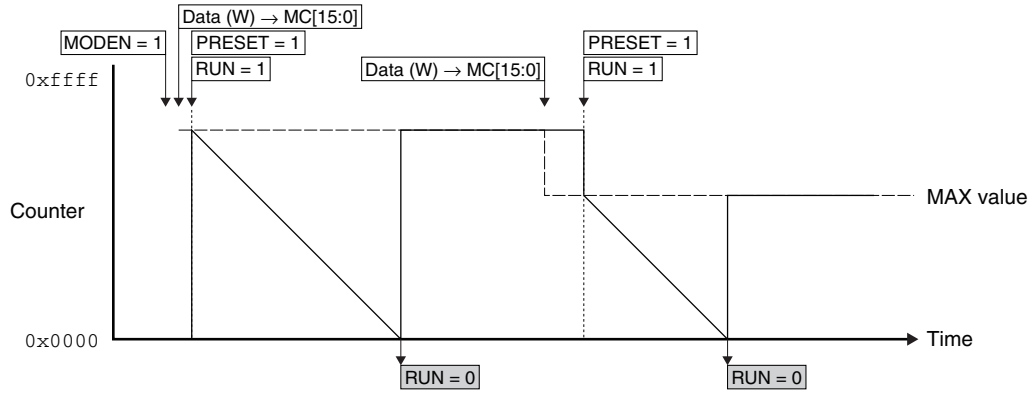


Figure 15.4.2.2 Operations in Repeat Down Count and One-shot Down Count Modes

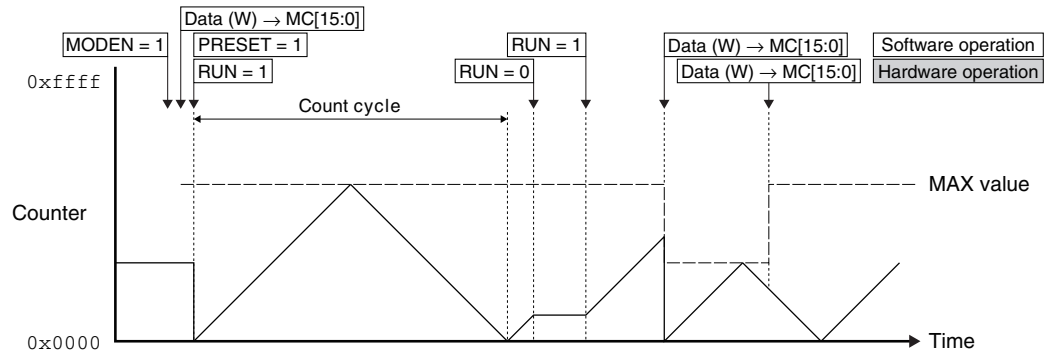
Operations in repeat up/down count and one-shot up/down count modes

In these modes, the counter operates as an up/down counter and counts as 0x0000 (or current value) → the MAX value → 0x0000.

In repeat up/down count mode, the counter repeats counting up from 0x0000 to the MAX value and counting down from the MAX value to 0x0000 until the T16B*n*CTL.RUN bit is set to 0. If the MAX value is altered to a value larger than the current counter value during count up operation, the counter keeps counting up to the new MAX value. If the MAX value is altered to a value smaller than the current counter value, the counter is cleared to 0x0000 and continues counting up to the new MAX value. If the MAX value is altered during count down operation, the counter keeps counting down to 0x0000 and then starts counting up to the new MAX value.

In one-shot up/down count mode, the counter stops automatically when it reaches 0x0000 during count down operation.

(1) Repeat up/down count mode



(2) One-shot up/down count mode

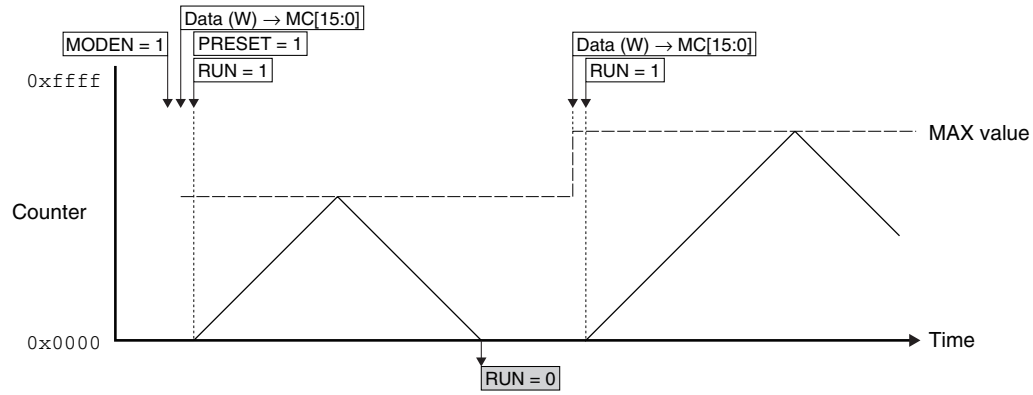


Figure 15.4.2.3 Operations in Repeat Up/Down Count and One-shot Up/Down Count Modes

15.4.3 Comparator/Capture Block Operations

The comparator/capture block functions as a comparator to compare the counter value with the register value set or a capture circuit to capture counter values using the external/software trigger signals.

Comparator/capture block operating mode

The comparator/capture block includes two systems (four or six systems) of comparator/capture circuits and each system can be set to comparator mode or capture mode, individually.

Set the T16B*n*CCCTL*m*.CCMD bit to 0 to set the comparator/capture circuit *m* to comparator mode or 1 to set it to capture mode.

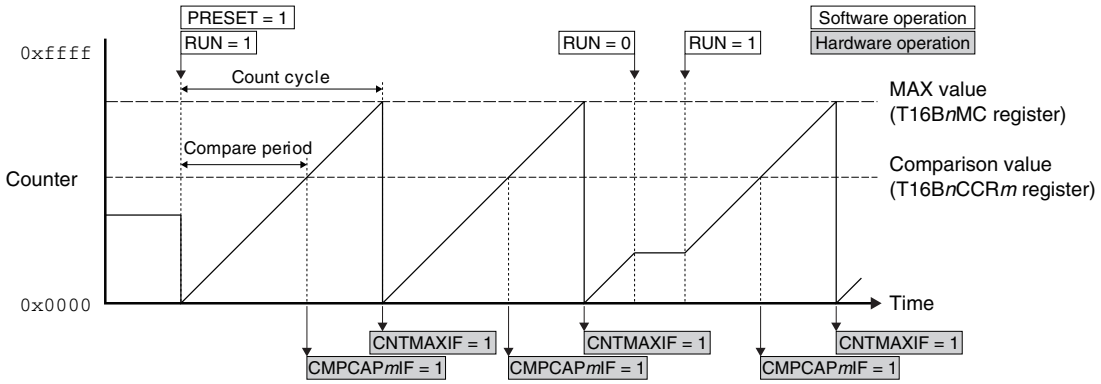
Operations in comparator mode

The comparator mode compares the counter value and the value set via software. It generates an interrupt and toggles the timer output signal level when the values are matched. The T16B*n*CCR*m* register functions as the compare data register used for setting a comparison value in this mode. The TOUT*nm*/CAP*nm* pin is configured to the TOUT*nm* pin.

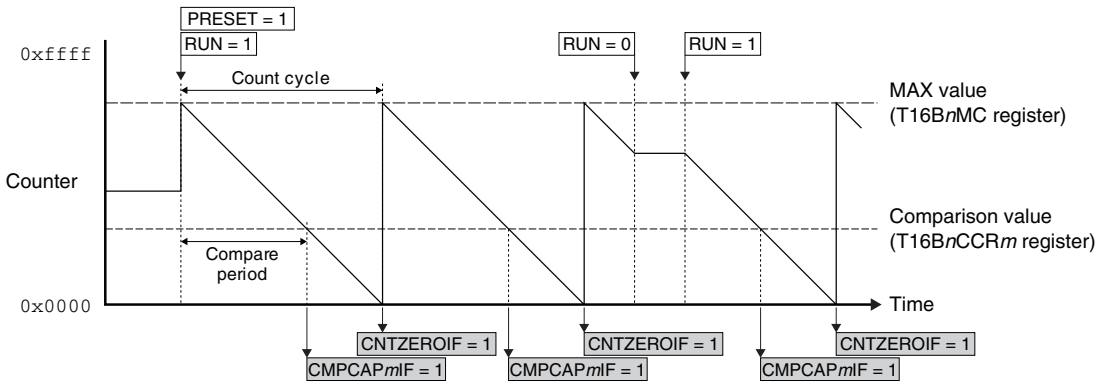
When the counter reaches the value set in the T16B*n*CCR*m* register during counting, the comparator asserts the MATCH signal and sets the T16B*n*INTF.COMPCAP*m*IF bit (compare interrupt flag) to 1.

When the counter reaches the MAX value in comparator mode, the T16B*n*INTF.CNTMAXIF bit (counter MAX interrupt flag) is set to 1. When the counter reaches 0x0000, the T16B*n*INTF.CNTZEROIF bit (counter zero interrupt flag) is set to 1.

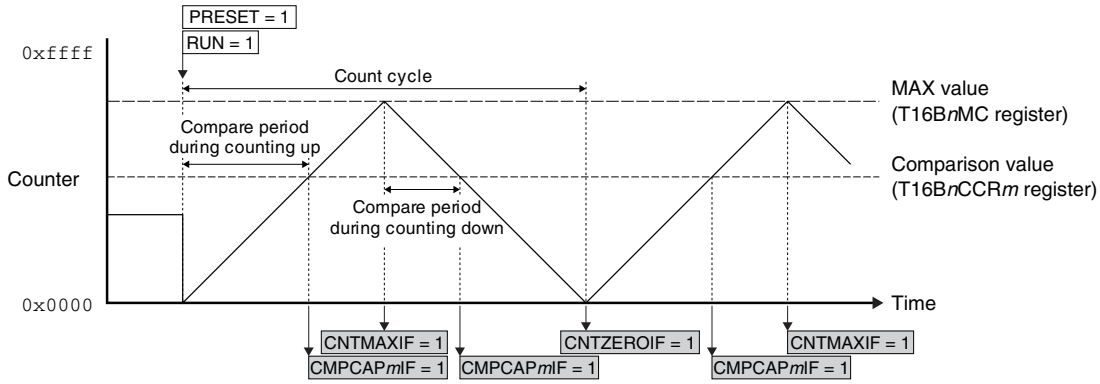
(1) Repeat up count mode



(2) Repeat down count mode



(3) Repeat up/down count mode



(Note that the T16B*n*INTF.CMPCAP*m*IF/CNTMAXIF/CNTZEROIF bit clearing operations via software are omitted from the figure.)

Figure 15.4.3.1 Operation Examples in Comparator Mode

The time from counter = 0x0000 or MAX value to occurrence of a compare interrupt (compare period) and the time to occurrence of a counter MAX or counter zero interrupt (count cycle) can be calculated as follows:

During counting up

$$\text{Compare period} = \frac{(CC + 1)}{f_{CLK\_T16B}} [s] \qquad \text{Count cycle} = \frac{(MAX + 1)}{f_{CLK\_T16B}} [s] \qquad \text{(Eq. 15.1)}$$

During counting down

$$\text{Compare period} = \frac{(MAX - CC + 1)}{f_{CLK\_T16B}} [s] \qquad \text{Count cycle} = \frac{(MAX + 1)}{f_{CLK\_T16B}} [s] \qquad \text{(Eq. 15.2)}$$

Where

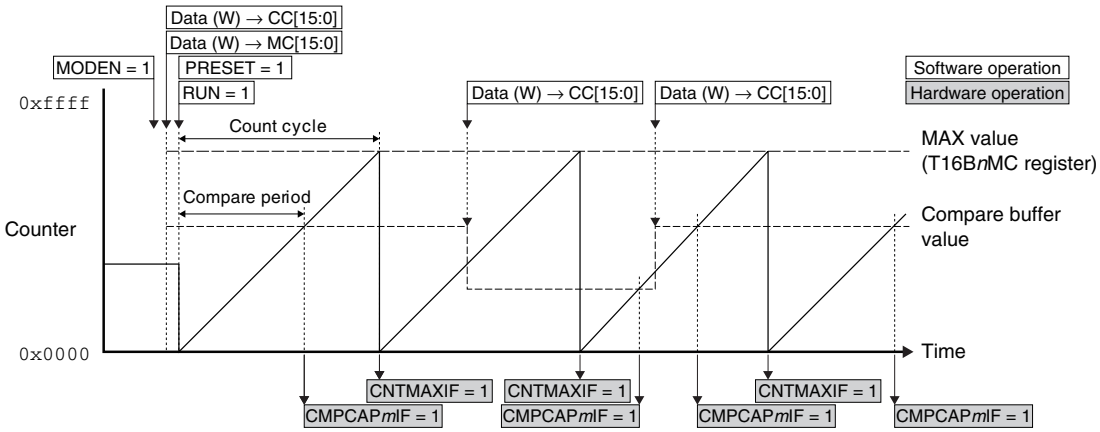
CC: T16B*n*CCR*m* register setting value (0 to 65,535)
MAX: T16B*n*MC register setting value (0 to 65,535)
f_{CLK_T16B}: Count clock frequency [Hz]

The comparator MATCH signal and counter MAX/ZERO signals are also used to generate a timer output waveform (TOUT). Refer to "TOUT Output Control" for more information.

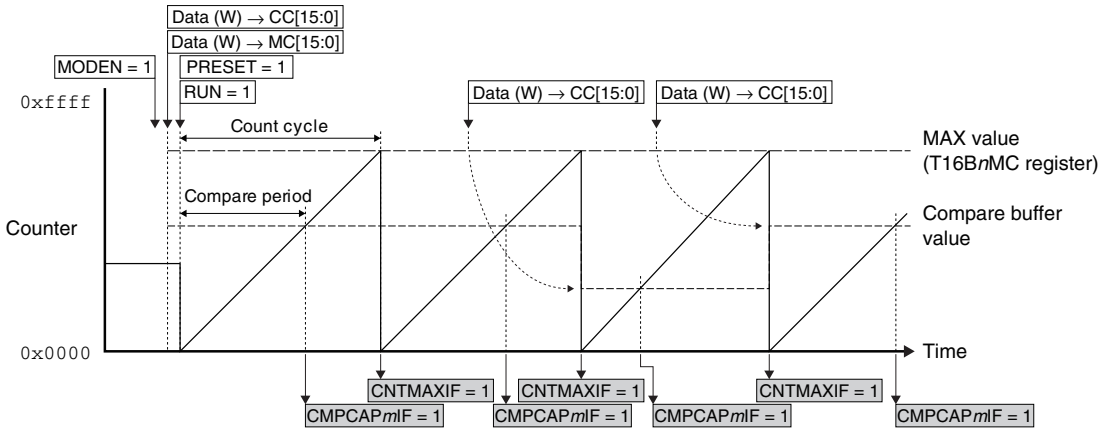
Compare buffer

The comparator loads the comparison value, which has been written to the T16B*n*CCR*m* register, to the compare buffer before comparing it with the counter value. For example, when generating a PWM waveform, the waveform with the desired duty ratio may not be generated if the comparison value is altered asynchronous to the count operation. To avoid this problem, the timing to load the comparison value to the compare buffer can be configured using the T16B*n*CCCTL*m*.CBUFMD[2:0] bits for synchronization with the count operation.

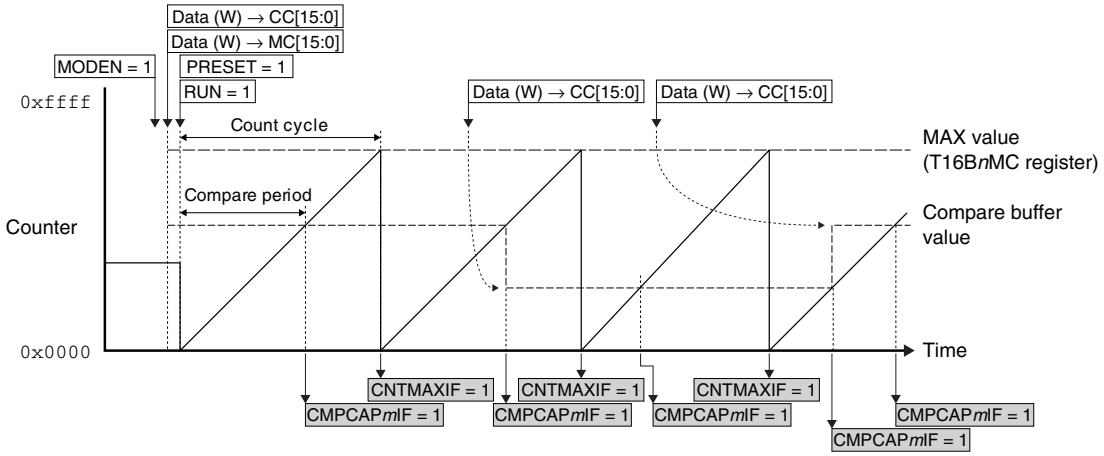
(1) Repeat up count mode
(1.1) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x0



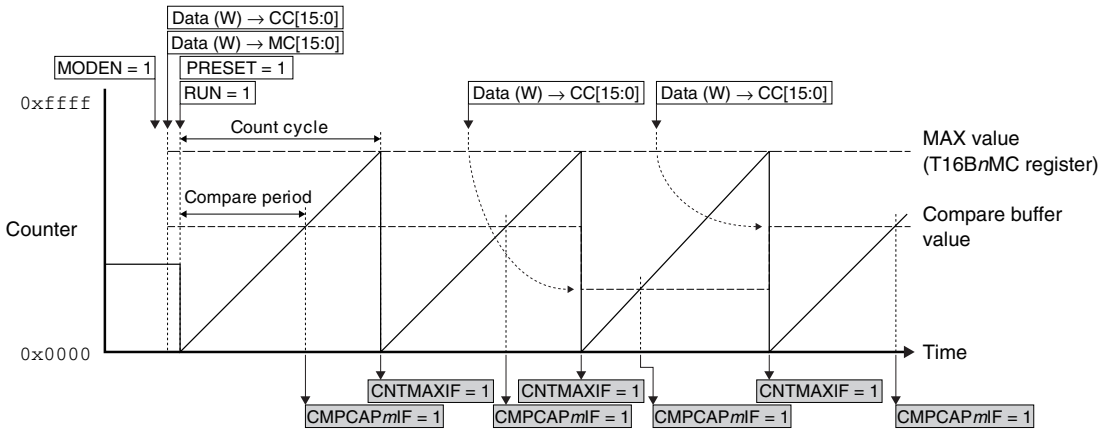
(1.2) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x1



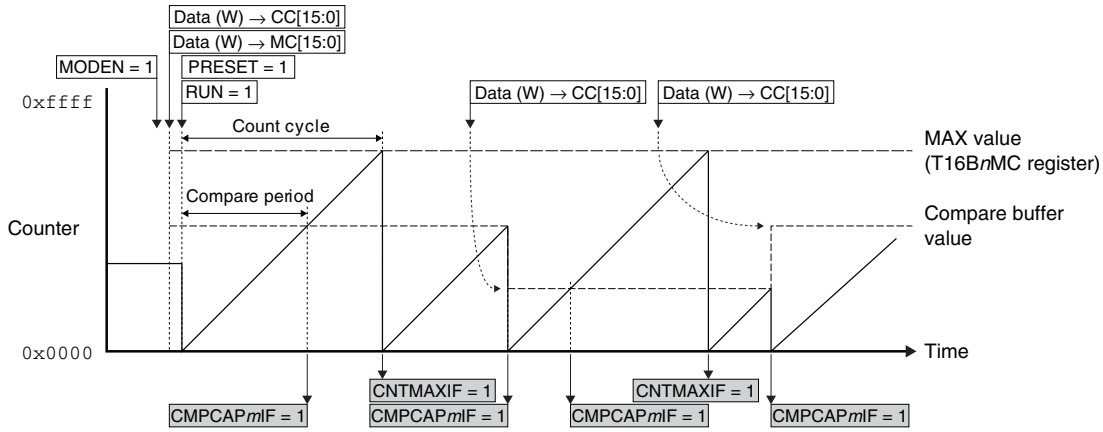
(1.3) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x2



(1.4) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x3

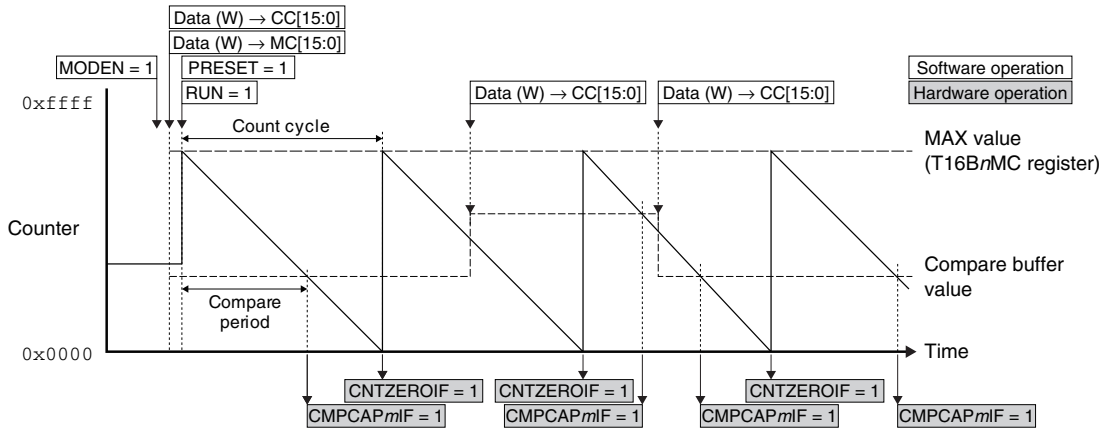


(1.5) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x4

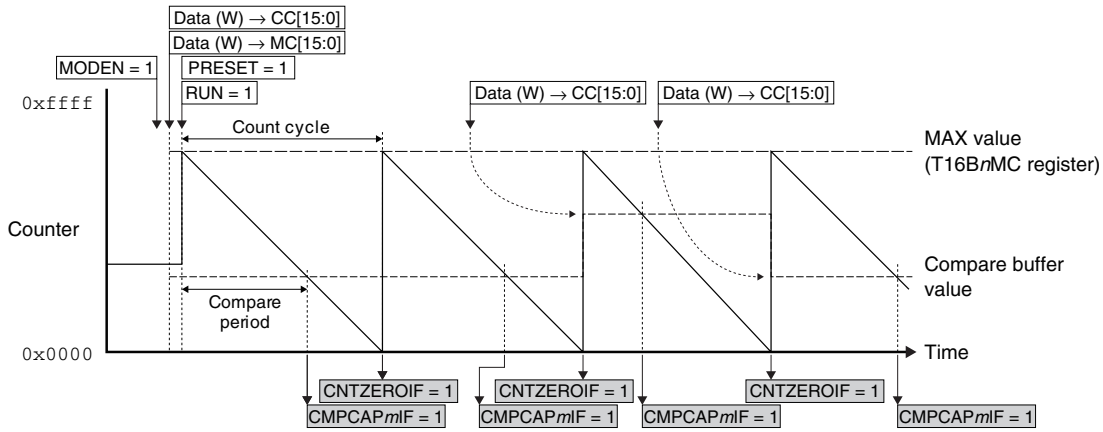


(2) Repeat down count mode

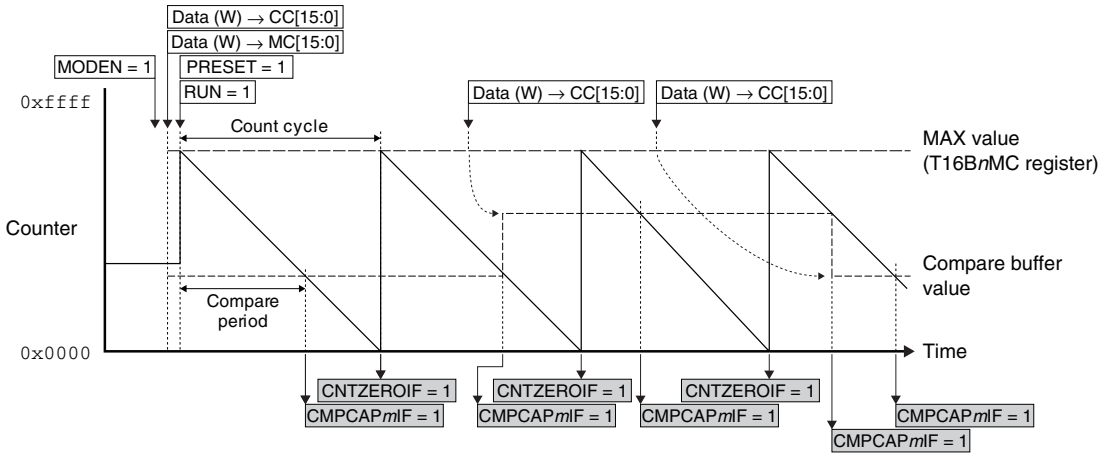
(2.1) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x0



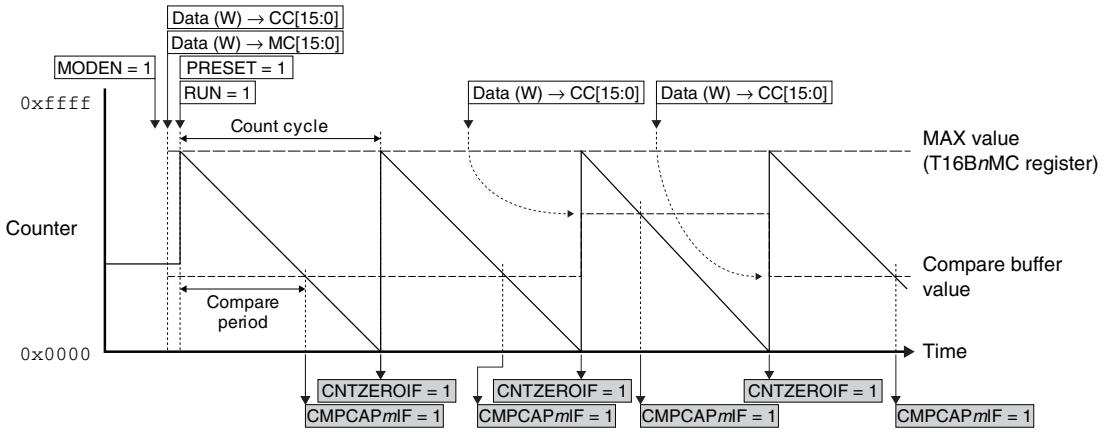
(2.2) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x1



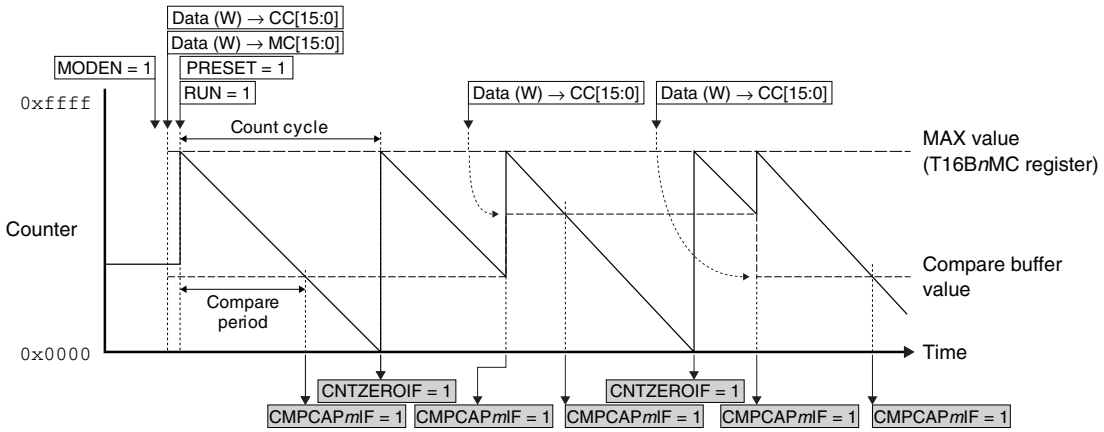
(2.3) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x2



(2.4) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x3

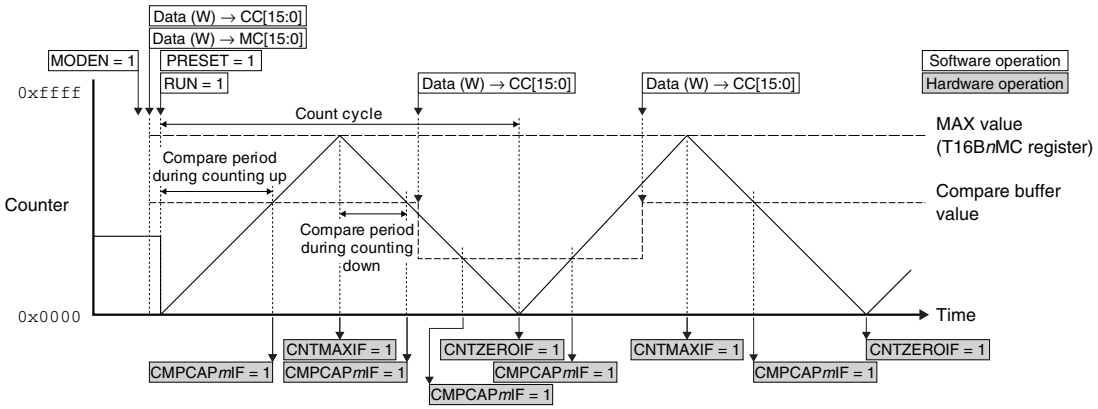


(2.5) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x4

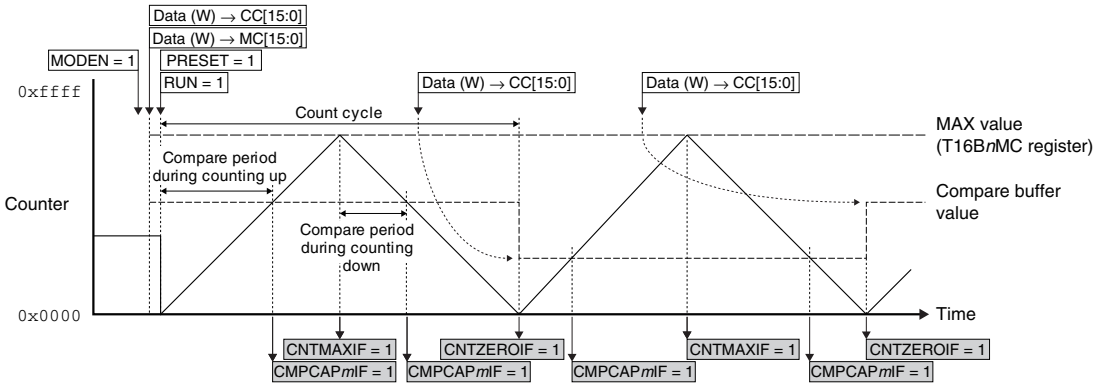


(3) Repeat up/down count mode

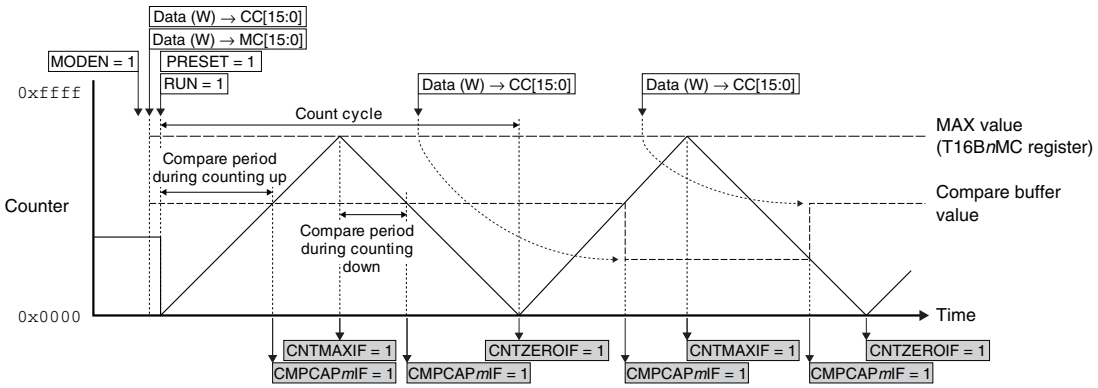
(3.1) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x0

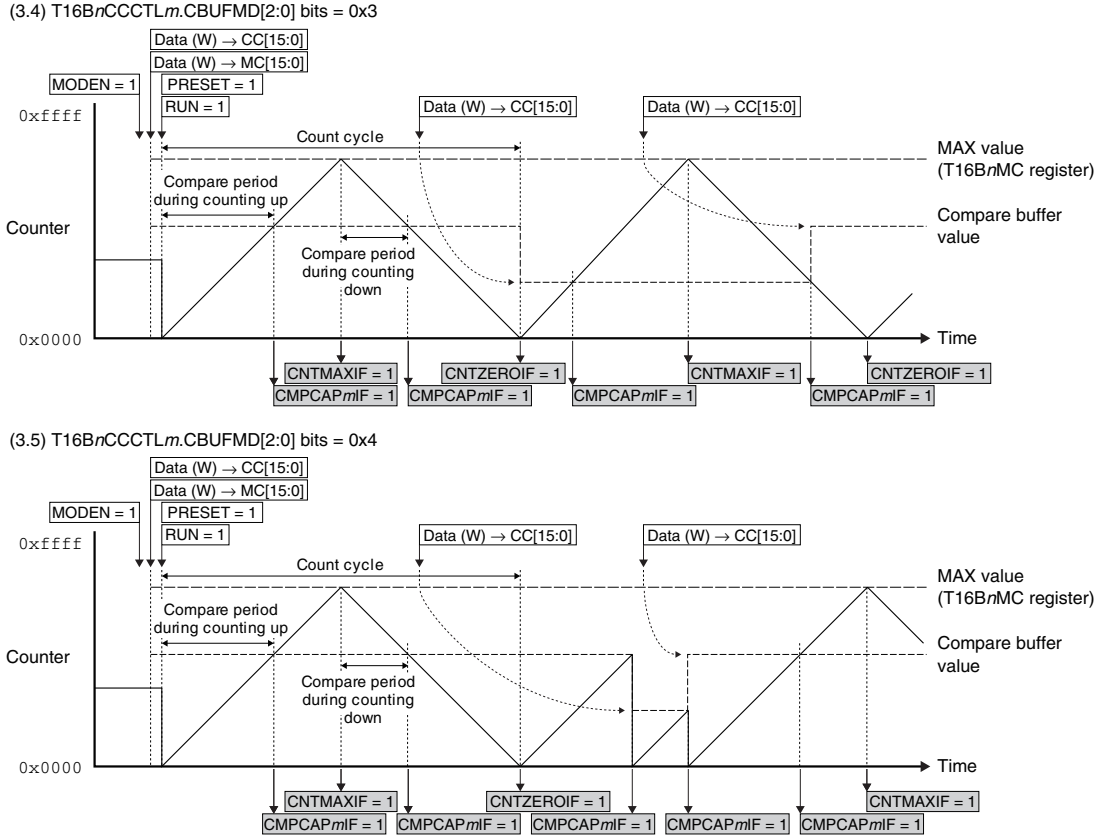


(3.2) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x1



(3.3) T16B*n*CCCTL*m*.CBUFMD[2:0] bits = 0x2





(Note that the T16B*n*INTF.CMPCAP*m*IF/CNTMAXIF/CNTZEROIF bit clearing operations via software are omitted from the figure.)

Figure 15.4.3.2 Compare Buffer Operations

Operations in capture mode

The capture mode captures the counter value when an external event, such as a key entry, occurs (at the specified edge of the external input/software trigger signal). In this mode, the T16B*n*CCR*m* register functions as the capture register from which the captured data is read. Furthermore, the TOUT*nm*/CAP*nm* pin is configured to the CAP*nm* pin.

The trigger signal and the trigger edge to capture the counter value are selected using the T16B*n*CCCTL*m*.CAPIS[1:0] bits and the T16B*n*CCCTL*m*.CAPTRG[1:0] bits, respectively.

When a specified trigger edge is input during counting, the current counter value is loaded to the T16B*n*CCR*m* register. At the same time the T16B*n*INTF.CMPCAP*m*IF bit is set. The interrupt occurred by this bit can be used to read the captured data from the T16B*n*CCR*m* register. For example, external event cycles and pulse widths can be measured from the difference between two captured counter values read.

If the captured data stored in the T16B*n*CCR*m* register is overwritten by the next trigger when the T16B*n*INTF.CMPCAP*m*IF bit is still set, an overwrite error occurs (the T16B*n*INTF.CAPOW*m*IF bit is set).

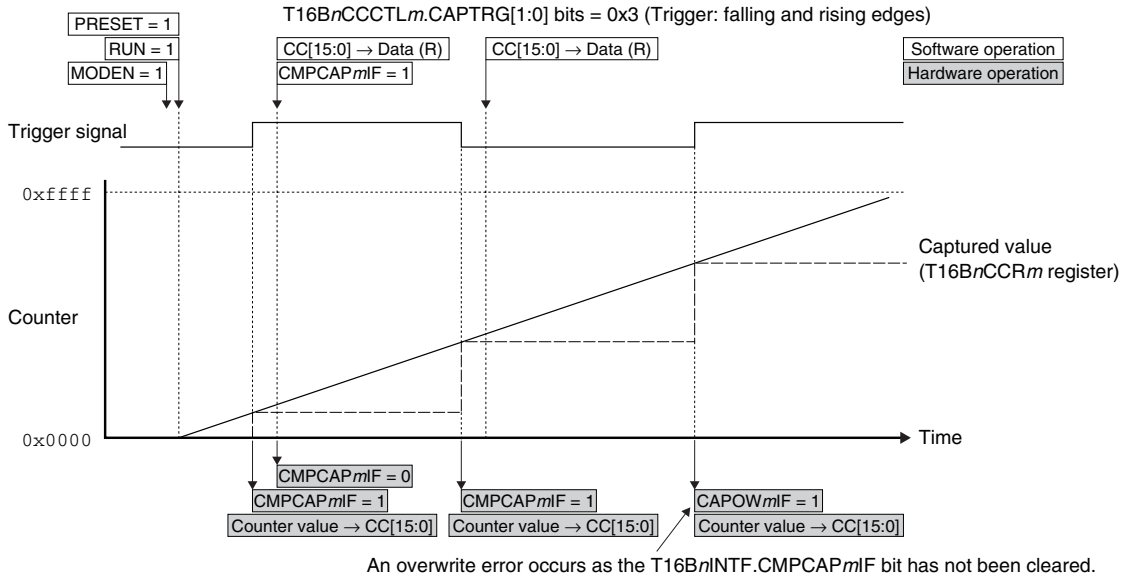


Figure 15.4.3.3 Operations in Capture Mode (Example in One-shot Up Count Mode)

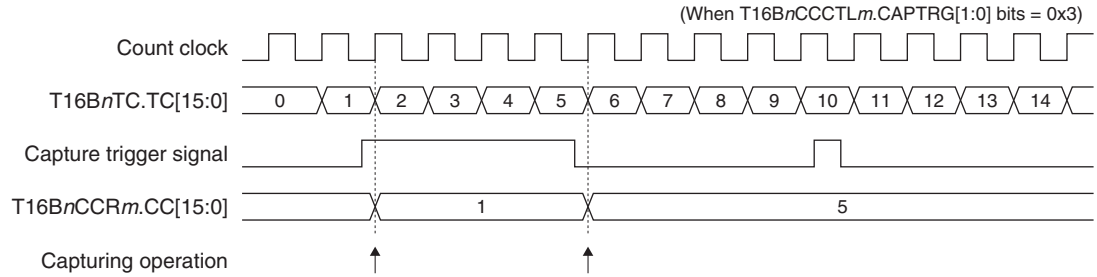
Synchronous capture mode/asynchronous capture mode

The capture circuit can operate in two operating modes: synchronous capture mode and asynchronous capture mode.

Synchronous capture mode is provided to avoid the possibility of invalid data reading by capturing counter data simultaneously with the counter being counted up/down. Set the T16B*n*CCCTL*m*.SCS bit to 1 to set the capture circuit to synchronous capture mode. This mode captures counter data by synchronizing the capture signal with the counter clock.

On the other hand, asynchronous capture mode can capture counter data by detecting a trigger pulse even if the pulse is shorter than the counter clock cycle that becomes invalid in synchronous capture mode. Set the T16B*n*CCCTL*m*.SCS bit to 0 to set the capture circuit to asynchronous capture mode.

(1) Synchronous capture mode



(2) Asynchronous capture mode

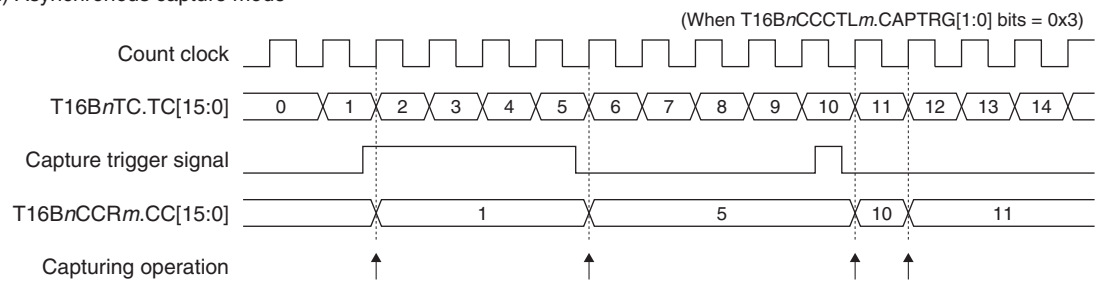


Figure 15.4.3.4 Synchronous Capture Mode/Asynchronous Capture Mode

15.4.4 TOUT Output Control

Comparator mode can generate TOUT signals using the comparator MATCH and counter MAX/ZERO signals. The generated signals can be output to outside the IC. Figure 15.4.4.1 shows the TOUT output circuits (circuits 0 and 1).

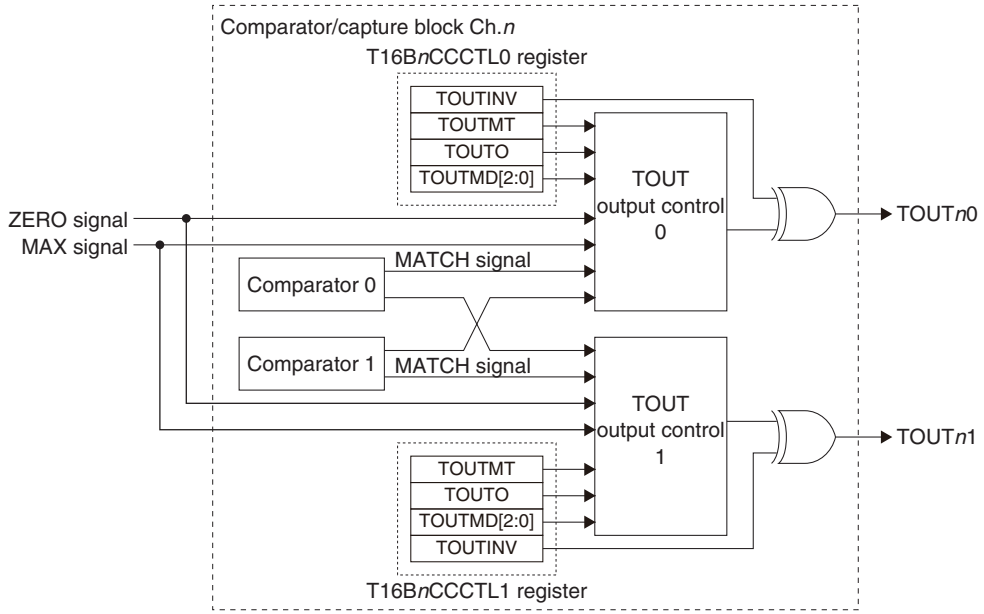


Figure 15.4.4.1 TOUT Output Circuits (Circuits 0 and 1)

Each timer channel includes two (four, or six) TOUT output circuits and their signal generation and output can be controlled individually.

TOUT generation mode

The T16B*n*CCCTL*m*.TOUTMD[2:0] bits are used to set how the TOUT signal waveform is changed by the MATCH and MAX/ZERO signals.

Furthermore, when the T16B*n*CCCTL*m*.TOUTMT bit is set to 1, the TOUT circuit uses the MATCH signal output from another system in the circuit pair (0 and 1, 2 and 3, 4 and 5). This makes it possible to change the signal twice within a counter cycle.

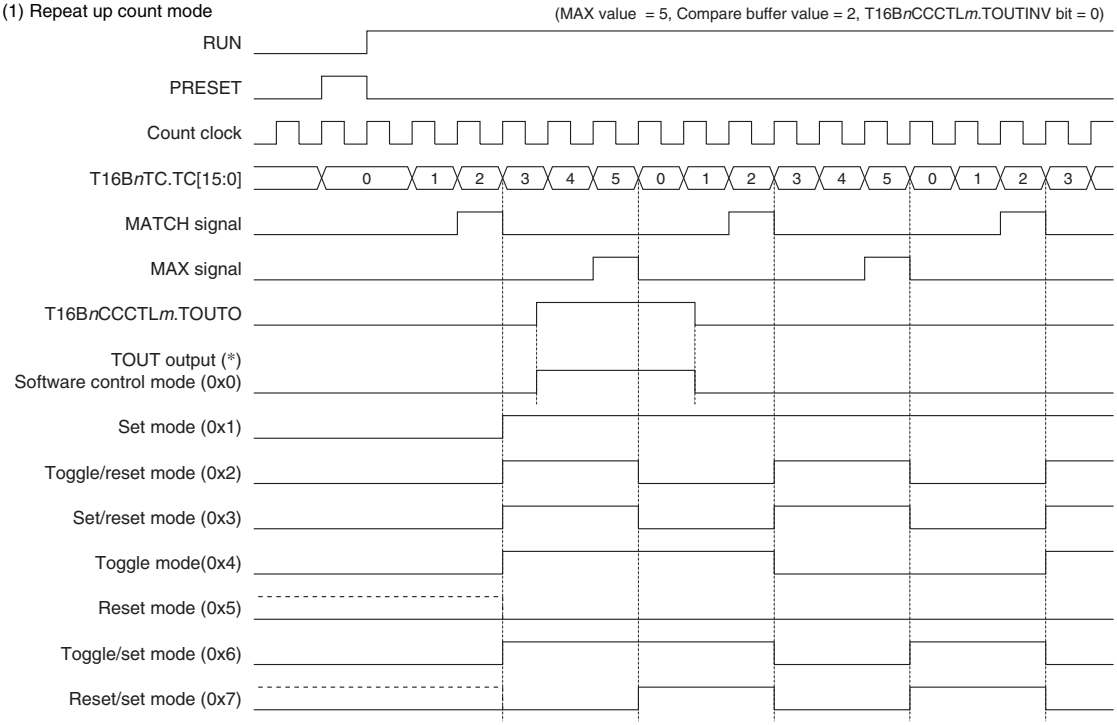
TOUT signal polarity

The TOUT signal polarity (active level) can be set using the T16B*n*CCCTL*m*.TOUTINV bit. It is set to active high by setting the T16B*n*CCCTL*m*.TOUTINV bit to 0 and active low by setting to 1.

Figures 15.4.4.2 and 15.4.4.3 show the TOUT output waveforms.

(1) Repeat up count mode

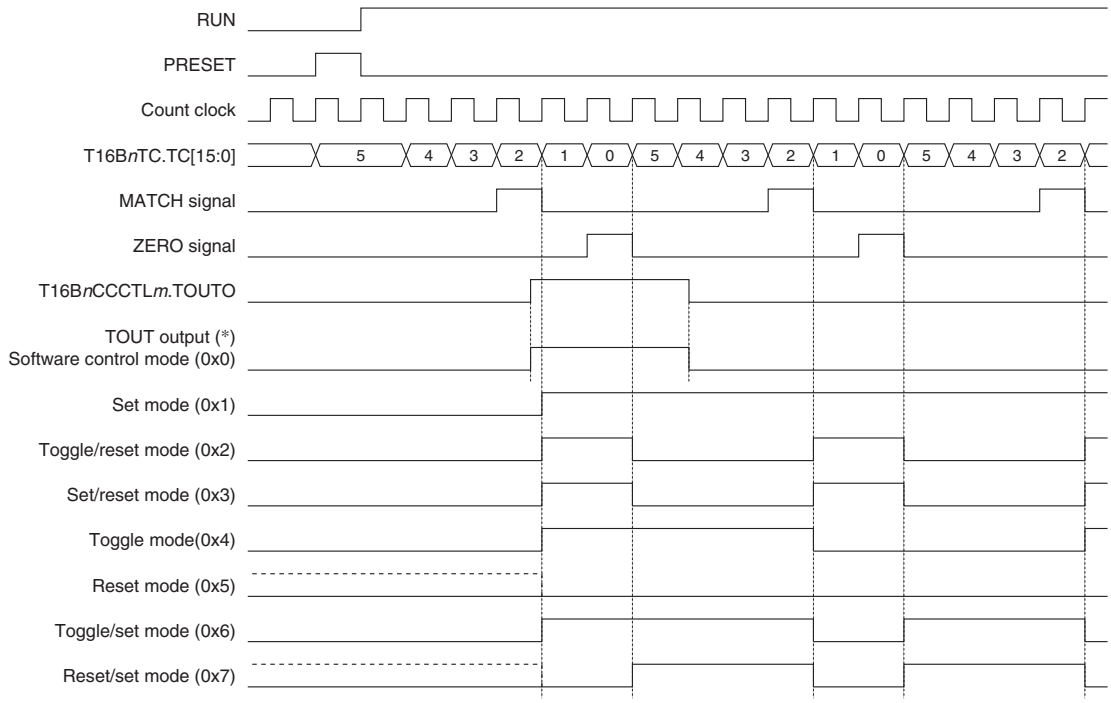
(MAX value = 5, Compare buffer value = 2, T16B*n*CCCTL*m*.TOUTINV bit = 0)



∗ ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

(2) Repeat down count mode

(MAX value = 5, Compare buffer value = 2, T16B*n*CCCTL*m*.TOUTINV bit = 0)



∗ ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

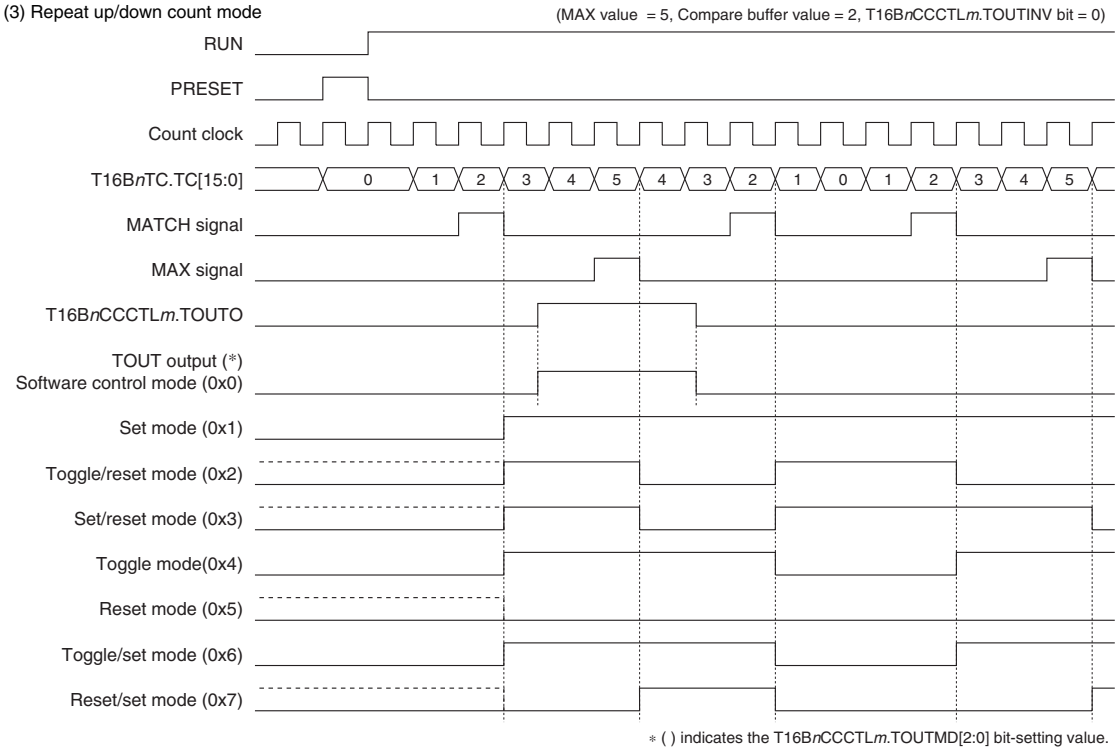
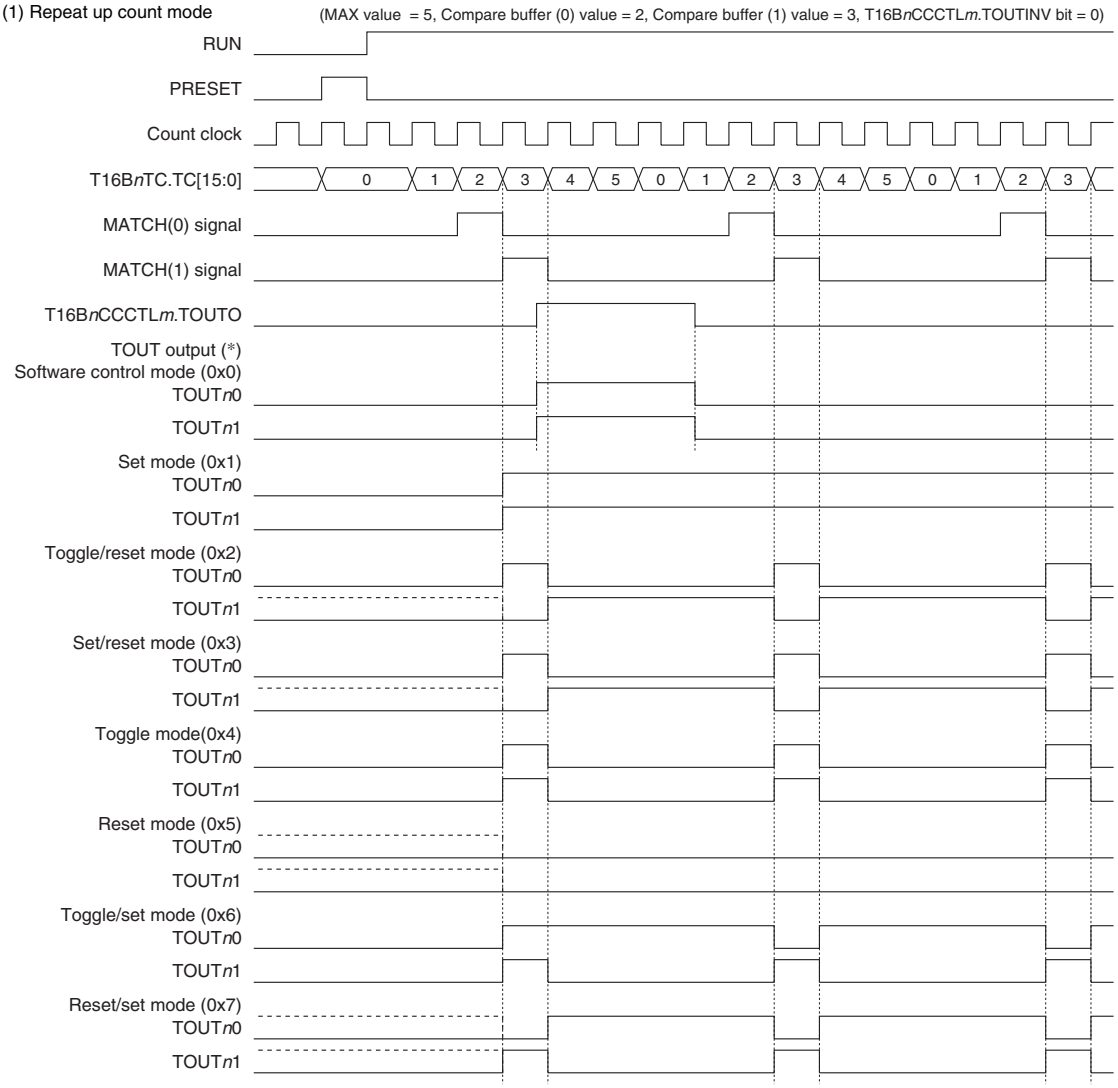


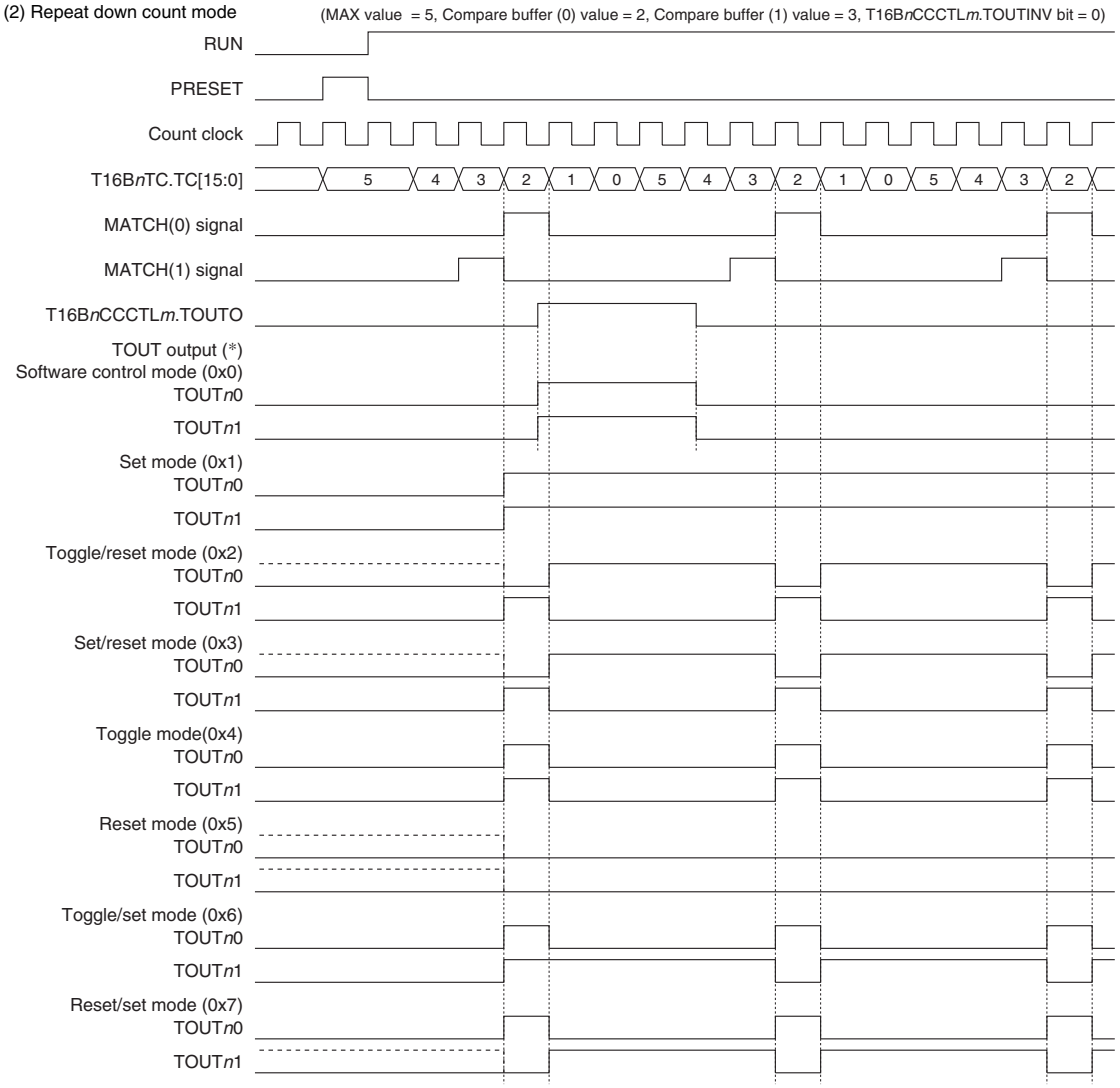
Figure 15.4.4.2 TOUT Output Waveform (T16B*n*CCCTL*m*.TOUTMT bit = 0)

(1) Repeat up count mode



* ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

(2) Repeat down count mode



* ( ) indicates the T16B*n*CCCTL*m*.TOUTMD[2:0] bit-setting value.

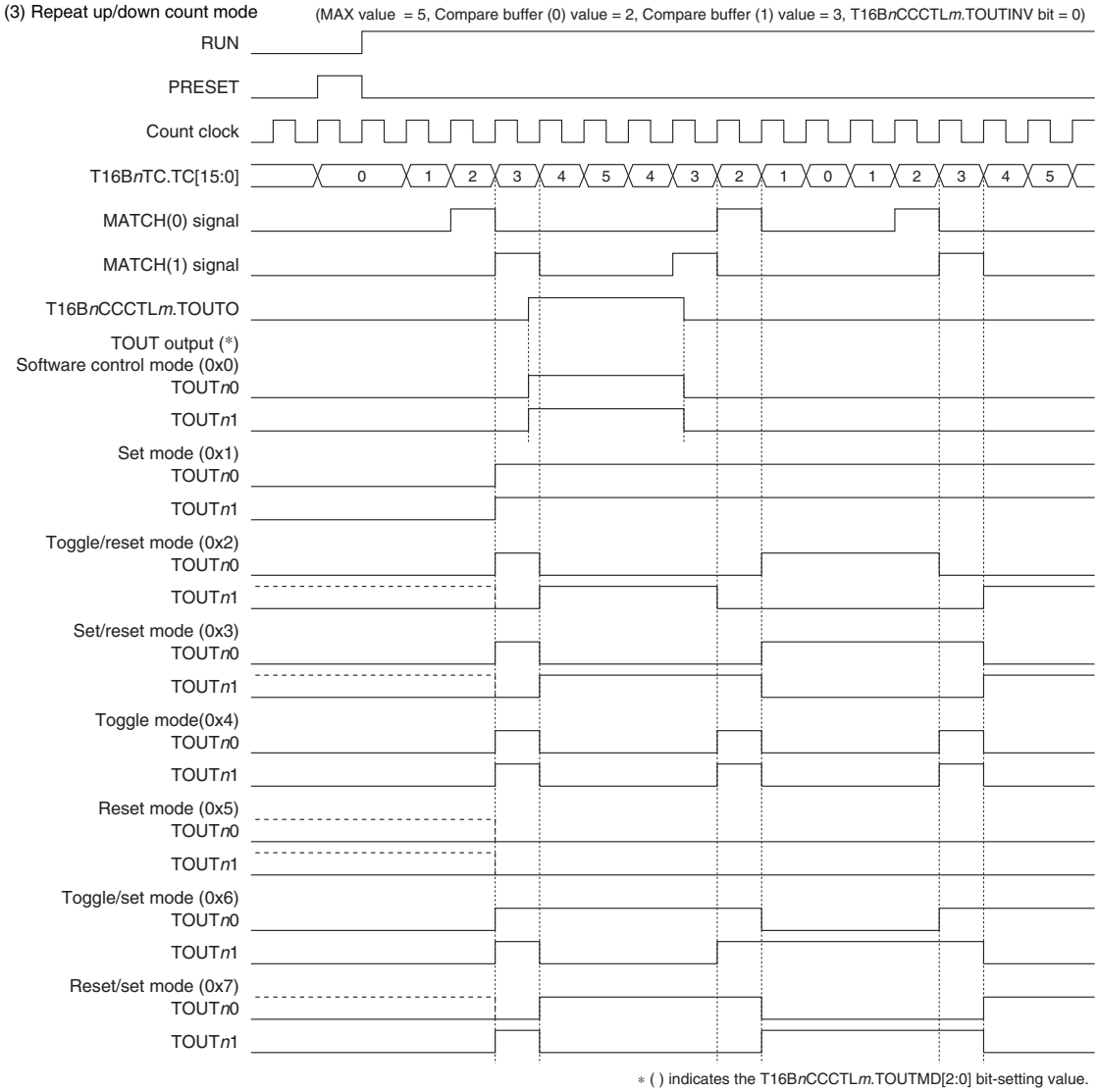


Figure 15.4.4.3 TOUT Output Waveform (T16B*n*CCCTL0.TOUTMT bit = 1, T16B*n*CCCTL1.TOUTMT bit = 0)

15.5 Interrupt

Each T16B channel has a function to generate the interrupt shown in Table 15.5.1.

Table 15.5.1 T16B Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Capture overwrite	T16B*n*INTF.CAPOW*m*IF	When the T16B*n*INTF.CMPCAP*m*IF bit =1 and the T16B*n* CCR*m* register is overwritten with new captured data in capture mode	Writing 1
Compare/ capture	T16B*n*INTF.CMPCAP*m*IF	When the counter value becomes equal to the compare buffer value in comparator mode When the counter value is loaded to the T16B*n*CCR*m* register by a capture trigger input in capture mode	Writing 1
Counter MAX	T16B*n*INTF.CNTMAXIF	When the counter reaches the MAX value	Writing 1
Counter zero	T16B*n*INTF.CNTZEROIF	When the counter reaches 0x0000	Writing 1

T16B provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

15.6 Control Registers

T16B Ch.*n* Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–4	CLKDIV[3:0]	0x0	H0	R/W	
	3	–	0	–	R	
	2–0	CLKSRC[2:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the T16B Ch.*n* operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the T16B Ch.*n* operating clock (counter clock).

Bit 3 Reserved

Bits 2–0 CLKSRC[2:0]

These bits select the clock source of T16B Ch.*n*.

Table 15.6.1 Clock Source and Division Ratio Settings

T16B*n*CLK.CLKDIV[3:0] bits	T16B*n*CLK.CLKSRC[2:0] bits							
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
	IOSC	OSC1	OSC3	EXOSC	EXCL*n*0	EXCL*n*1	EXCL*n*0 inverted input	EXCL*n*1 inverted input
0xf	1/32,768	1/1	1/32,768	1/1	1/1	1/1	1/1	1/1
0xe	1/16,384		1/16,384					
0xd	1/8,192		1/8,192					
0xc	1/4,096		1/4,096					
0xb	1/2,048		1/2,048					
0xa	1/1,024		1/1,024					
0x9	1/512		1/512					
0x8	1/256	1/256	1/256					
0x7	1/128	1/128	1/128					
0x6	1/64	1/64	1/64					
0x5	1/32	1/32	1/32					
0x4	1/16	1/16	1/16					
0x3	1/8	1/8	1/8					
0x2	1/4	1/4	1/4					
0x1	1/2	1/2	1/2					
0x0	1/1	1/1	1/1					

(Note) The oscillator circuits/external inputs that are not supported in this IC cannot be selected as the clock source.

T16B Ch.*n* Counter Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CTL	15–9	–	0x00	–	R	–
	8	MAXBSY	0	H0	R	
	7–6	–	0x0	–	R	
	5–4	CNTMD[1:0]	0x0	H0	R/W	
	3	ONEST	0	H0	R/W	
	2	RUN	0	H0	R/W	
	1	PRESET	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bits 15–9 Reserved

Bit 8 MAXBSY

This bit indicates whether data can be written to the T16B*n*MC register or not.

1 (R): Busy status (cannot be written)

0 (R): Idle (can be written)

While this bit is 1, the T16B*n*MC register is loading the MAX value. Data writing is prohibited during this period.

Bits 7–6 Reserved

Bits 5–4 CNTMD[1:0]

These bits select the counter up/down mode. The count mode is configured with this selection and the T16B*n*CTL.ONEST bit setting (see Table 15.6.2).

Bit 3 ONEST

This bit selects the counter repeat/one-shot mode. The count mode is configured with this selection and the T16B*n*CTL.CNTMD[1:0] bit settings (see Table 15.6.2).

Table 15.6.2 Count Mode

T16B*n*CTL.CNTMD[1:0] bits	Count mode	
	T16B*n*CTL.ONEST bit = 1	T16B*n*CTL.ONEST bit = 0
0x3	Reserved	
0x2	One-shot up/down count mode	Repeat up/down count mode
0x1	One-shot down count mode	Repeat down count mode
0x0	One-shot up count mode	Repeat up count mode

Bit 2 RUN

This bit starts/stops counting.

1 (W): Start counting
0 (W): Stop counting
1 (R): Counting
0 (R): Idle

By writing 1 to this bit, the counter block starts count operations. However, the T16B*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance. While the timer is running, writing 0 to the T16B*n*CTL.RUN bit stops count operations. When the counter stops by the counter MAX/ZERO signal in one-shot mode, this bit is automatically cleared to 0.

Bit 1 PRESET

This bit resets the counter.

1 (W): Reset
0 (W): Ineffective
1 (R): Resetting in progress
0 (R): Resetting finished or normal operation

In up mode or up/down mode, the counter is cleared to 0x0000 by writing 1 to this bit. In down mode, the MAX value, which has been set to the T16B*n*MC register, is preset to the counter. However, the T16B*n*CTL.MODEN bit must be set to 1 in conjunction with this bit or it must be set in advance.

Bit 0 MODEN

This bit enables the T16B Ch.*n* operations.

1 (R/W): Enable (Start supplying operating clock)
0 (R/W): Disable (Stop supplying operating clock)

Note: The counter reset operation using the T16B*n*CTL.PRESET bit and the counting start operation using the T16B*n*CTL.RUN bit take effect only when the T16B*n*CTL.MODEN bit = 1.

T16B Ch.*n* Max Counter Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*MC	15–0	MC[15:0]	0xffff	H0	R/W	–

Bits 15–0 MC[15:0]

These bits are used to set the MAX value to preset to the counter. For more information, refer to "Counter Block Operations - MAX counter data register."

Notes:
- When one-shot mode is selected, do not alter the T16B*n*MC.MC[15:0] bits (MAX value) during counting.
- Make sure the T16B*n*CTL.MODEN bit is set to 1 before writing data to the T16B*n*MC.MC[15:0] bits. If the T16B*n*CTL.MODEN bit = 0 when writing to the T16B*n*MC.MC[15:0] bits, set the T16B*n*CTL.MODEN bit to 1 until the T16B*n*CS.BSY bit is set to 0 from 1.
- Do not set the T16B*n*MC.MC[15:0] bits to 0x0000.

T16B Ch.*n* Timer Counter Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*TC	15–0	TC[15:0]	0x0000	H0	R	–

Bits 15–0 TC[15:0]

The current counter value can be read out through these bits.

T16B Ch.*n* Counter Status Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CS	15–8	–	0x00	–	R	–
	7	CAPI5	0	H0	R	
	6	CAPI4	0	H0	R	
	5	CAPI3	0	H0	R	
	4	CAPI2	0	H0	R	
	3	CAPI1	0	H0	R	
	2	CAPI0	0	H0	R	
	1	UP_DOWN	1	H0	R	
	0	BSY	0	H0	R	

Bits 15–8 Reserved

Bit 7 CAPI5
Bit 6 CAPI4
Bit 5 CAPI3
Bit 4 CAPI2
Bit 3 CAPI1
Bit 2 CAPI0

These bits indicate the signal level currently input to the CAP*nm* pin.
1 (R): Input signal = High level
0 (R): Input signal = Low level

The following shows the correspondence between the bit and the CAP*nm* pin:
T16B*n*CS.CAPI5 bit: CAP*n*5 pin
T16B*n*CS.CAPI4 bit: CAP*n*4 pin
T16B*n*CS.CAPI3 bit: CAP*n*3 pin
T16B*n*CS.CAPI2 bit: CAP*n*2 pin
T16B*n*CS.CAPI1 bit: CAP*n*1 pin
T16B*n*CS.CAPI0 bit: CAP*n*0 pin

Note: The configuration of the T16B*n*CS.CAPI*m* bits depends on the model. The bits corresponding to the CAP*nm* pins that do not exist are read-only bits and are always fixed at 0.

Bit 1 UP_DOWN

This bit indicates the currently set count direction.
1 (R): Count up
0 (R): Count down

Bit 0 BSY

This bit indicates the counter operating status.
1 (R): Running
0 (R): Idle

T16B Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*INTF	15–14	–	0x0	–	R	–
	13	CAPOW5IF	0	H0	R/W	Cleared by writing 1.
	12	CMPCAP5IF	0	H0	R/W	
	11	CAPOW4IF	0	H0	R/W	
	10	CMPCAP4IF	0	H0	R/W	
	9	CAPOW3IF	0	H0	R/W	
	8	CMPCAP3IF	0	H0	R/W	
	7	CAPOW2IF	0	H0	R/W	
	6	CMPCAP2IF	0	H0	R/W	
	5	CAPOW1IF	0	H0	R/W	
	4	CMPCAP1IF	0	H0	R/W	
	3	CAPOW0IF	0	H0	R/W	
	2	CMPCAP0IF	0	H0	R/W	
	1	CNTMAXIF	0	H0	R/W	
	0	CNTZEROIF	0	H0	R/W	

Bits 15–14 Reserved

Bit 13 CAPOW5IF
Bit 12 CMPCAP5IF
Bit 11 CAPOW4IF
Bit 10 CMPCAP4IF
Bit 9 CAPOW3IF
Bit 8 CMPCAP3IF
Bit 7 CAPOW2IF
Bit 6 CMPCAP2IF
Bit 5 CAPOW1IF
Bit 4 CMPCAP1IF
Bit 3 CAPOW0IF
Bit 2 CMPCAP0IF
Bit 1 CNTMAXIF
Bit 0 CNTZEROIF

These bits indicate the T16B Ch.*n* interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
T16B*n*INTF.CAPOW5IF bit: Capture 5 overwrite interrupt
T16B*n*INTF.CMPCAP5IF bit: Compare/capture 5 interrupt
T16B*n*INTF.CAPOW4IF bit: Capture 4 overwrite interrupt
T16B*n*INTF.CMPCAP4IF bit: Compare/capture 4 interrupt
T16B*n*INTF.CAPOW3IF bit: Capture 3 overwrite interrupt
T16B*n*INTF.CMPCAP3IF bit: Compare/capture 3 interrupt
T16B*n*INTF.CAPOW2IF bit: Capture 2 overwrite interrupt
T16B*n*INTF.CMPCAP2IF bit: Compare/capture 2 interrupt
T16B*n*INTF.CAPOW1IF bit: Capture 1 overwrite interrupt
T16B*n*INTF.CMPCAP1IF bit: Compare/capture 1 interrupt
T16B*n*INTF.CAPOW0IF bit: Capture 0 overwrite interrupt
T16B*n*INTF.CMPCAP0IF bit: Compare/capture 0 interrupt
T16B*n*INTF.CNTMAXIF bit: Counter MAX interrupt
T16B*n*INTF.CNTZEROIF bit: Counter zero interrupt

Note: The configuration of the T16B*n*INTF.CAPOW*m*IF and T16B*n*INTF.CMPCAP*m*IF bits depends on the model. The bits corresponding to the comparator/capture circuits that do not exist are read-only bits and are always fixed at 0.

T16B Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*INTE	15–14	–	0x0	–	R	–
	13	CAPOW5IE	0	H0	R/W	
	12	CMPCAP5IE	0	H0	R/W	
	11	CAPOW4IE	0	H0	R/W	
	10	CMPCAP4IE	0	H0	R/W	
	9	CAPOW3IE	0	H0	R/W	
	8	CMPCAP3IE	0	H0	R/W	
	7	CAPOW2IE	0	H0	R/W	
	6	CMPCAP2IE	0	H0	R/W	
	5	CAPOW1IE	0	H0	R/W	
	4	CMPCAP1IE	0	H0	R/W	
	3	CAPOW0IE	0	H0	R/W	
	2	CMPCAP0IE	0	H0	R/W	
	1	CNTMAXIE	0	H0	R/W	
	0	CNTZEROIE	0	H0	R/W	

Bits 15–14 Reserved

Bit 13 CAPOW5IE
Bit 12 CMPCAP5IE
Bit 11 CAPOW4IE
Bit 10 CMPCAP4IE
Bit 9 CAPOW3IE
Bit 8 CMPCAP3IE
Bit 7 CAPOW2IE
Bit 6 CMPCAP2IE
Bit 5 CAPOW1IE
Bit 4 CMPCAP1IE
Bit 3 CAPOW0IE
Bit 2 CMPCAP0IE
Bit 1 CNTMAXIE
Bit 0 CNTZEROIE

These bits enable T16B Ch.*n* interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
T16B*n*INTE.CAPOW5IE bit: Capture 5 overwrite interrupt
T16B*n*INTE.CMPCAP5IE bit: Compare/capture 5 interrupt
T16B*n*INTE.CAPOW4IE bit: Capture 4 overwrite interrupt
T16B*n*INTE.CMPCAP4IE bit: Compare/capture 4 interrupt
T16B*n*INTE.CAPOW3IE bit: Capture 3 overwrite interrupt
T16B*n*INTE.CMPCAP3IE bit: Compare/capture 3 interrupt
T16B*n*INTE.CAPOW2IE bit: Capture 2 overwrite interrupt
T16B*n*INTE.CMPCAP2IE bit: Compare/capture 2 interrupt
T16B*n*INTE.CAPOW1IE bit: Capture 1 overwrite interrupt
T16B*n*INTE.CMPCAP1IE bit: Compare/capture 1 interrupt
T16B*n*INTE.CAPOW0IE bit: Capture 0 overwrite interrupt
T16B*n*INTE.CMPCAP0IE bit: Compare/capture 0 interrupt
T16B*n*INTE.CNTMAXIE bit: Counter MAX interrupt
T16B*n*INTE.CNTZEROIE bit: Counter zero interrupt

Notes:
- The configuration of the T16B*n*INTE.CAPOW*m*IE and T16B*n*INTE.CMPCAP*m*IE bits depends on the model. The bits corresponding to the comparator/capture circuits that do not exist are read-only bits and are always fixed at 0.
- To prevent generating unnecessary interrupts, the corresponding interrupt flag should be cleared before enabling interrupts.

T16B Ch.*n* Comparator/Capture *m* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CCCTL*m*	15	SCS	0	H0	R/W	–
	14–12	CBUFMD[2:0]	0x0	H0	R/W	
	11–10	CAPIS[1:0]	0x0	H0	R/W	
	9–8	CAPTRG[1:0]	0x0	H0	R/W	
	7	–	0	–	R	
	6	TOUTMT	0	H0	R/W	
	5	TOUTO	0	H0	R/W	
	4–2	TOUTMD[2:0]	0x0	H0	R/W	
	1	TOUTINV	0	H0	R/W	
	0	CCMD	0	H0	R/W	

Bit 15 SCS

This bit selects either synchronous capture mode or asynchronous capture mode.
1 (R/W): Synchronous capture mode
0 (R/W): Asynchronous capture mode

For more information, refer to "Comparator/Capture Block Operations - Synchronous capture mode/ asynchronous capture mode." The T16B*n*CCCTL*m*.SCS bit is control bit for capture mode and is ineffective in comparator mode.

Bits 14–12 CBUFMD[2:0]

These bits select the timing to load the comparison value written in the T16B*n*CCR*m* register to the compare buffer. The T16B*n*CCCTL*m*.CBUFMD[2:0] bits are control bits for comparator mode and are ineffective in capture mode.

Table 15.6.3 Timings to Load Comparison Value to Compare Buffer

T16B*n*CCCTL*m*. CBUFMD[2:0] bits	Count mode	Comparison Value load timing
0x7–0x5	Reserved	
0x4	Up mode	When the counter becomes equal to the comparison value set previously Also the counter is reset to 0x0000 simultaneously.
	Down mode	When the counter becomes equal to the comparison value set previously Also the counter is reset to the MAX value simultaneously.
	Up/down mode	When the counter becomes equal to the comparison value set previously Also the counter is reset to 0x0000 simultaneously.
0x3	Up mode	When the counter reverts to 0x0000
	Down mode	When the counter reverts to the MAX value
	Up/down mode	When the counter becomes equal to the comparison value set previously or when the counter reverts to 0x0000
0x2	Up mode	When the counter becomes equal to the comparison value set previously
	Down mode	
	Up/down mode	
0x1	Up mode	When the counter reaches the MAX value
	Down mode	When the counter reaches 0x0000
	Up/down mode	When the counter reaches 0x0000 or the MAX value
0x0	Up mode	At the CLK_16B*n* rising edge after writing to the T16B*n*CCR*m* register
	Down mode	
	Up/down mode	

Bits 11–10 CAPIS[1:0]

These bits select the trigger signal for capturing (see Table 15.6.4). The T16B*n*CCCTL*m*.CAPIS[1:0] bits are control bits for capture mode and are ineffective in comparator mode.

Bits 9–8 CAPTRG[1:0]

These bits select the trigger edge(s) of the trigger signal at which the counter value is captured in the T16B*n*CCR*m* register in capture mode (see Table 15.6.4). The T16B*n*CCCTL*m*.CAPTRG[1:0] bits are control bits for capture mode and are ineffective in comparator mode.

Table 15.6.4 Trigger Signal/Edge for Capturing Counter Value

T16B*n*CCCTL*m*. CAPTRG[1:0] bits (Trigger edge)	Trigger condition	
	T16B*n*CCCTL*m*.CAPIS[1:0] bits (Trigger signal)	
	0x0 (External trigger signal)	0x2 (Software trigger signal = L) 0x3 (Software trigger signal = H)
0x3 (↑ & ↓)	Rising or falling edge of the CAP*nm* pin input signal	Altering the T16B*n*CCCTL*m*.CAPIS[1:0] bits from 0x2 to 0x3, or from 0x3 to 0x2
0x2 (↓)	Falling edge of the CAP*nm* pin input signal	Altering the T16B*n*CCCTL*m*.CAPIS[1:0] bits from 0x3 to 0x2
0x1 (↑)	Rising edge of the CAP*nm* pin input signal	Altering the T16B*n*CCCTL*m*.CAPIS[1:0] bits from 0x2 to 0x3
0x0	Not triggered (disable capture function)	

Bit 7 Reserved

Bit 6 TOUTMT

This bit selects whether the comparator MATCH signal of another system is used for generating the TOUT*nm* signal or not.

1 (R/W): Generate TOUT using two comparator MATCH signals of the comparator circuit pair (0 and 1, 2 and 3, 4 and 5)

0 (R/W): Generate TOUT using one comparator MATCH signal of comparator *m* and the counter MAX or ZERO signals

The T16B*n*CCCTL*m*.TOUTMT bit is control bit for comparator mode and is ineffective in capture mode.

Bit 5 TOUTO

This bit sets the TOUT*nm* signal output level when software control mode (T16B*n*CCCTL*m*.TOUTMD[2:0] = 0x0) is selected for the TOUT*nm* output.

1 (R/W): High level output

0 (R/W): Low level output

The T16B*n*CCCTL*m*.TOUTO bit is control bit for comparator mode and is ineffective in capture mode.

Bits 4–2 TOUTMD[2:0]

These bits configure how the TOUT*nm* signal waveform is changed by the comparator MATCH and counter MAX/ZERO signals.

The T16B*n*CCCTL*m*.TOUTMD[2:0] bits are control bits for comparator mode and are ineffective in capture mode.

Table 15.6.5 TOUT Generation Mode

T16B*n*CCCTL*m*. TOUTMD[2:0] bits	TOUT generation mode and operations			
	T16B*n*CCCTL*m*. TOUTMT bit	Count mode	Output signal	Change in the signal
0x7	**Reset/set mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal becomes inactive by the MATCH signal and it becomes active by the MAX signal.
		Down count mode	TOUT*nm*	The signal becomes inactive by the MATCH signal and it becomes active by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal becomes inactive by the MATCH*m* signal and it becomes active by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes inactive by the MATCH*m*+1 signal and it becomes active by the MATCH*m* signal.
0x6	**Toggle/set mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes active by the MAX signal.
		Down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes active by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal is inverted by the MATCH*m* signal and it becomes active by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal is inverted by the MATCH*m*+1 signal and it becomes active by the MATCH*m* signal.
0x5	**Reset mode**			
	0	All count modes	TOUT*nm*	The signal becomes inactive by the MATCH signal.
	1	All count modes	TOUT*nm*	The signal becomes inactive by the MATCH*m* or MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes inactive by the MATCH*m*+1 or MATCH*m* signal.

T16B*n*CCCTL*m*. TOUTMD[2:0] bits	TOUT generation mode and operations			
	T16B*n*CCCTL*m*. TOUTMT bit	Count mode	Output signal	Change in the signal
0x4	**Toggle mode**			
	0	All count modes	TOUT*nm*	The signal is inverted by the MATCH signal.
	1	All count modes	TOUT*nm*	The signal is inverted by the MATCH*m* or MATCH*m*+1 signal.
			TOUT*nm*+1	The signal is inverted by the MATCH*m*+1 or MATCH*m* signal.
0x3	**Set/reset mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal becomes active by the MATCH signal and it becomes inactive by the MAX signal.
		Down count mode	TOUT*nm*	The signal becomes active by the MATCH signal and it becomes inactive by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal becomes active by the MATCH*m* signal and it becomes inactive by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes active by the MATCH*m*+1 signal and it becomes inactive by the MATCH*m* signal.
0x2	**Toggle/reset mode**			
	0	Up count mode Up/down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes inactive by the MAX signal.
		Down count mode	TOUT*nm*	The signal is inverted by the MATCH signal and it becomes inactive by the ZERO signal.
	1	All count modes	TOUT*nm*	The signal is inverted by the MATCH*m* signal and it becomes inactive by the MATCH*m*+1 signal.
			TOUT*nm*+1	The signal is inverted by the MATCH*m*+1 signal and it becomes inactive by the MATCH*m* signal.
0x1	**Set mode**			
	0	All count modes	TOUT*nm*	The signal becomes active by the MATCH signal.
	1	All count modes	TOUT*nm*	The signal becomes active by the MATCH*m* or MATCH*m*+1 signal.
			TOUT*nm*+1	The signal becomes active by the MATCH*m*+1 or MATCH*m* signal.
0x0	**Software control mode**			
	*	All count modes	TOUT*nm*	The signal becomes active by setting the T16B*n*CCCTL*m*. TOUTO bit to 1 and it becomes inactive by setting to 0.

Bit 1 TOUTINV

This bit selects the TOUT*nm* signal polarity.

1 (R/W): Inverted (active low)

0 (R/W): Normal (active high)

The T16B*n*CCCTL*m*.TOUTINV bit is control bit for comparator mode and is ineffective in capture mode.

Bit 0 CCMD

This bit selects the operating mode of the comparator/capture circuit *m*.

1 (R/W): Capture mode (T16*n*CCR*m* register = capture register)

0 (R/W): Comparator mode (T16*n*CCR*m* register = compare data register)

T16B Ch.*n* Compare/Capture *m* Data Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
T16B*n*CCR*m*	15–0	CC[15:0]	0x0000	H0	R/W	–

Bits 15–0 CC[15:0]

In comparator mode, this register is configured as the compare data register and used to set the comparison value to be compared with the counter value.

In capture mode, this register is configured as the capture register and the counter value captured by the capture trigger signal is loaded.

16 IR Remote Controller (REMC2)

16.1 Overview

The REMC2 circuit generates infrared remote control output signals. This circuit can also be applicable to an EL lamp drive circuit by adding a simple external circuit.
The features of the REMC2 are listed below.

- Outputs an infrared remote control signal.
- Includes a carrier generator.
- Flexible carrier signal generation and data pulse width modulation.
- Automatic data setting function for continuous data transmission.
- Output signal inverting function supporting various formats.
- EL lamp drive waveform can be generated for an application example.

Figure 16.1.1 shows the REMC2 configuration.

Table 16.1.1 REMC2 Channel Configuration of S1C17589

Item	S1C17589
Number of channels	1 transmitter channel

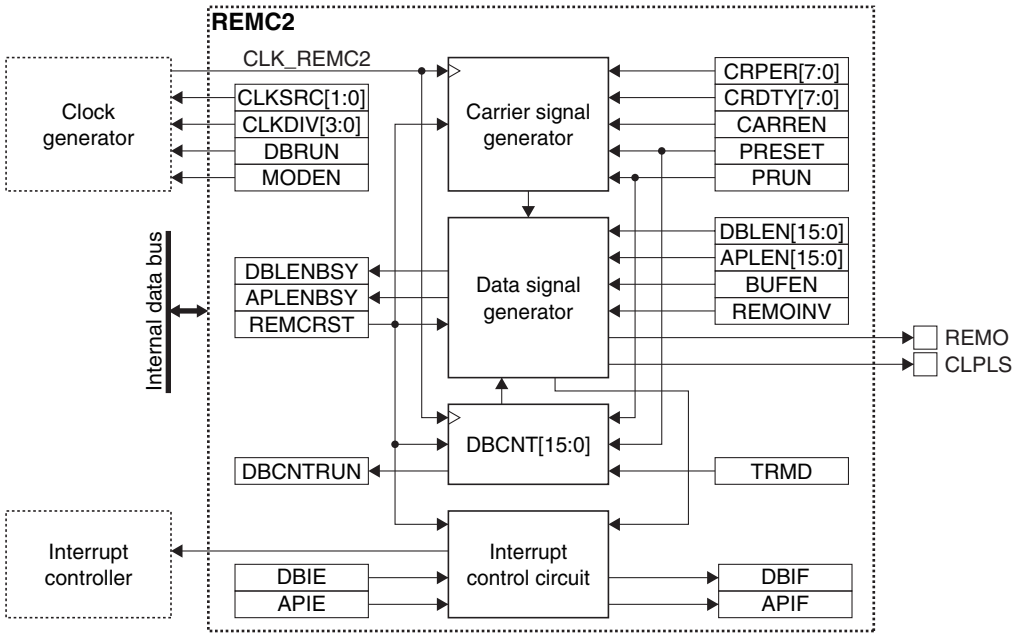


Figure 16.1.1 REMC2 Configuration

16.2 Input/Output Pins and External Connections

16.2.1 Output Pin

Table 16.2.1.1 shows the REMC2 pin.

Table 16.2.1.1 REMC2 Pin

Pin name	I/O*	Initial status*	Function
REMO	O	O (L)	IR remote controller transmit data output
CLPLS	O	O (L)	IR remote controller clear pulse output

* Indicates the status when the pin is configured for the REMC2.

If the port is shared with the REMC2 pin and other functions, the REMC2 output function must be assigned to the port before activating the REMC2. For more information, refer to the "I/O Ports" chapter.

16.2.2 External Connections

Figure 16.2.2.1 shows a connection example between the REMC2 and an external infrared module.

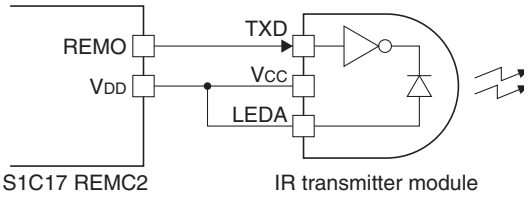


Figure 16.2.2.1 Connection Example Between REMC2 and External Infrared Module

16.3 Clock Settings

16.3.1 REMC2 Operating Clock

When using the REMC2, the REMC2 operating clock CLK_REMC2 must be supplied to the REMC2 from the clock generator. The CLK_REMC2 supply should be controlled as in the procedure shown below.

1. Enable the clock source in the clock generator if it is stopped (refer to "Clock Generator" in the "Power Supply, Reset, and Clocks" chapter).
2. Set the following REMCLK register bits:
   - REMCLK.CLKSRC[1:0] bits (Clock source selection)
   - REMCLK.CLKDIV[3:0] bits (Clock division ratio selection = Clock frequency setting)

16.3.2 Clock Supply in SLEEP Mode

When using REMC2 during SLEEP mode, the REMC2 operating clock CLK_REMC2 must be configured so that it will keep supplying by writing 0 to the CLGOSC*xxxx*SLPC bit for the CLK_REMC2 clock source.
If the CLGOSC*xxxx*SLPC bit for the CLK_REMC2 clock source is 1, the CLK_REMC2 clock source is deactivated during SLEEP mode and REMC2 stops with the register settings maintained at those before entering SLEEP mode. After the CPU returns to normal mode, CLK_REMC2 is supplied and the REMC2 operation resumes.

16.3.3 Clock Supply in DEBUG Mode

The CLK_REMC2 supply during DEBUG mode should be controlled using the REMCLK.DBRUN bit.
The CLK_REMC2 supply to the REMC2 is suspended when the CPU enters DEBUG mode if the REMCLK.DBRUN bit = 0. After the CPU returns to normal mode, the CLK_REMC2 supply resumes. Although the REMC2 stops operating when the CLK_REMC2 supply is suspended, the output pin and registers retain the status before DEBUG mode was entered. If the REMCLK.DBRUN bit = 1, the CLK_REMC2 supply is not suspended and the REMC2 will keep operating in DEBUG mode.

16.4 Operations

16.4.1 Initialization

The REMC2 should be initialized with the procedure shown below.

1. Write 1 to the REMDBCTL.REMCRST bit. (Reset REMC2)
2. Configure the REMCLK.CLKSRC[1:0] and REMCLK.CLKDIV[3:0] bits. (Configure operating clock)
3. Assign the REMC2 output function to the port. (Refer to the "I/O Ports" chapter.)

4. Configure the following REMDBCTL register bits:
   - Set the REMDBCTL.MODEN bit to 1. (Enable count operation clock)
   - REMDBCTL.TRMD bit (Select repeat mode/one-shot mode)
   - Set the REMDBCTL.BUFEN bit to 1. (Enable compare buffer)
   - REMDBCTL.REMOINV bit (Configure inverse logic output signal)
5. Configure the following REMCARR register bits:
   - REMCARR.CRPER[7:0] bit (Set carrier signal cycle)
   - REMCARR.CRDTY[7:0] bit (Set carrier signal duty)
6. Set the REMCCTL.CARREN bit. (Enable/disable carrier modulation)
7. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the REMINTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the REMINTE register to 1. (Enable interrupts)

16.4.2 Data Transmission Procedures

Starting data transmission

The following shows a procedure to start data transmission.

1. Set the REMAPLEN.APLEN[15:0] bits. (Set data signal duty)
2. Set the REMDBLEN.DBLEN[15:0] bits. (Set data signal cycle)
3. Set the following REMDBCTL register bits:
   - Set the REMDBCTL.PRESET bit to 1. (Reset internal counters)
   - Set the REMDBCTL.PRUN bit to 1. (Start counting)

Continuous data transmission control

The following shows a procedure to send data continuously after starting data transmission (after Step 3 above).

1. Set the duty and cycle for the subsequent data to the REMAPLEN.APLEN[15:0] and REMDBLEN.DBLEN[15:0] bits, respectively, before a compare DB interrupt (REMINTF.DBIF bit = 1) occurs. (It is not necessary to rewrite settings when sending the same data with the current settings.)
2. Wait for a compare DB interrupt (REMINTF.DBIF bit = 1).
3. Repeat Steps 1 and 2 until the end of data.

Terminating data transmission

The following shows a procedure to terminate data transmission.

1. Wait for a compare DB interrupt (REMINTF.DBIF bit = 1).
2. Set the REMDBCTL.PRUN bit to 0. (Stop counting)
3. Set the REMDBCTL.MODEN bit to 0. (Disable count operation clock)

16.4.3 REMO Output Waveform

Carrier refers to infrared frequency in infrared remote control communication. Note, however, that carrier in this manual refers to sub-carrier used in infrared remote control communication, as REMC2 does not control infrared rays directly.
The REMC2 outputs the logical AND between the carrier signal output from the carrier generator and the data signal output from the data signal generator. Figure 16.4.3.1 shows an example of the output waveform.

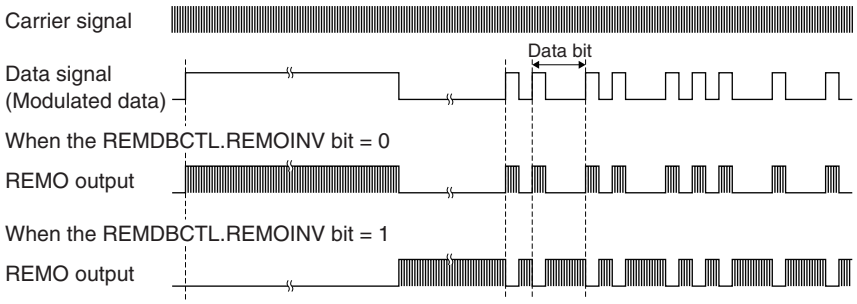
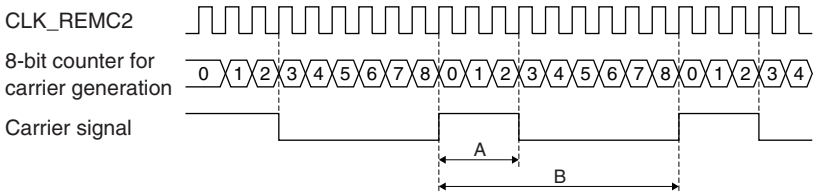


Figure 16.4.3.1 REMO Output Waveform Example

Carrier signal

The carrier signal is generated by comparing the values of the 8-bit counter for carrier generation that runs with CLK_REMC2 and the setting values of the REMCARR.CRDTY[7:0] and REMCARR.CRPER[7:0] bits. Figure 16.4.3.2 shows an example of the carrier signal generated.

Example) REMCARR.CRDTY[7:0] bits = 2, REMCARR.CRPER[7:0] bits = 8



A: REMCARR.CRDTY[7:0] bits + 1 [clock]
B: REMCARR.CRPER[7:0] bits + 1 [clock]

Figure 16.4.3.2 Example of Carrier Signal Generated

The carrier signal frequency and duty ratio can be calculated by the equations shown below.

$$\text{Carrier frequency} = \frac{f_{CLK\_REMC2}}{CRPER + 1} \qquad \text{Duty ratio} = \frac{CRDTY + 1}{CRPER + 1} \qquad \text{(Eq. 16.1)}$$

Where

f_{CLK_REMC2}: CLK_REMC2 frequency [Hz]
CRPER: REMCARR.CRPER[7:0] bit-setting value (1–255)
CRDTY: REMCARR.CRDTY[7:0] bit-setting value (0–254)
∗ REMCARR.CRDTY[7:0] bits < REMCARR.CRPER[7:0] bits

The 8-bit counter for carrier generation is reset by the REMDBCTL.PRESET bit and is started/stopped by the REMDBCTL.PRUN bit in conjunction with the 16-bit counter for data signal generation. When the counter value is matched with the REMCARR.CRDTY[7:0] bits, the carrier signal waveform is inverted. When the counter value is matched with the REMCARR.CRPER[7:0] bits, the carrier signal waveform is inverted and the counter is reset to 0x00.

Data signal

The data signal is generated by comparing the values of the 16-bit counter for data signal generation (REMDBCNT.DBCNT[15:0] bits) that runs with CLK_REMC2 and the setting values of the REMAPLEN.APLEN[15:0] and REMDBLEN.DBLEN[15:0] bits. Figure 16.4.3.3 shows an example of the data signal generated.

Example) REMAPLEN.APLEN[15:0] bits = 0x0bd0, REMDBLEN.DBLEN[15:0] bits = 0x11b8,
REMDBCTL.TRMD bit = 0 (repeat mode), REMDBCTL.REMOINV bit = 0 (signal logic non-inverted)

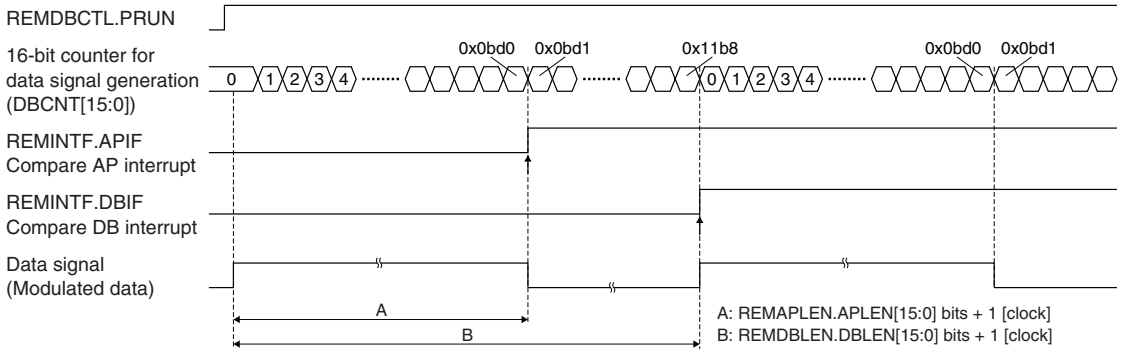


Figure 16.4.3.3 Example of Data Signal Generated

The data length and duty ratio of the pulse-width-modulated data signal can be calculated with the equations shown below.

$$\text{Data length} = \frac{\text{DBLEN} + 1}{f_{CLK\_REMC2}} \qquad \text{Duty ratio} = \frac{\text{APLEN} + 1}{\text{DBLEN} + 1} \qquad \text{(Eq. 16.2)}$$

Where

f_{CLK_REMC2}: CLK_REMC2 frequency [Hz]
DBLEN: REMDBLEN.DBLEN[15:0] bit-setting value (1–65,535)
APLEN: REMAPLEN.APLEN[15:0] bit-setting value (0–65,534)
∗ REMAPLEN.APLEN[15:0] bits < REMDBLEN.DBLEN[15:0] bits

The 16-bit counter for data signal generation is reset by the REMDBCTL.PRESET bit and is started/stopped by the REMDBCTL.PRUN bit. When the counter value is matched with the REMAPLEN.APLEN[15:0] bits (compare AP), the data signal waveform is inverted. When the counter value is matched with the REMDBLEN.DBLEN[15:0] bits (compare DB), the data signal waveform is inverted and the counter is reset to 0x0000.
A different interrupt can be generated when the counter value is matched with the REMDBLEN.DBLEN[15:0] and REMAPLEN.APLEN[15:0] bits, respectively.

Repeat mode and one-shot mode

When the 16-bit counter for data signal generation is set to repeat mode (REMDBCTL.TRMD bit = 0), the counter keeps operating until it is stopped using the REMDBCTL.PRUN bit. When the counter is set to one-shot mode (REMDBCTL.TRMD bit = 1), the counter stops automatically when the counter value is matched with the REMDBLEN.DBLEN[15:0] bit-setting value.

16.4.4 Continuous Data Transmission and Compare Buffers

Figure 16.4.4.1 shows an operation example of continuous data transmission with the compare buffer enabled.

Example) REMDBCTL.TRMD bit = 0 (repeat mode), REMDBCTL.BUFEN bit = 1 (compare buffer enabled), REMDBCTL.REMOINV bit = 0 (signal logic non-inverted)

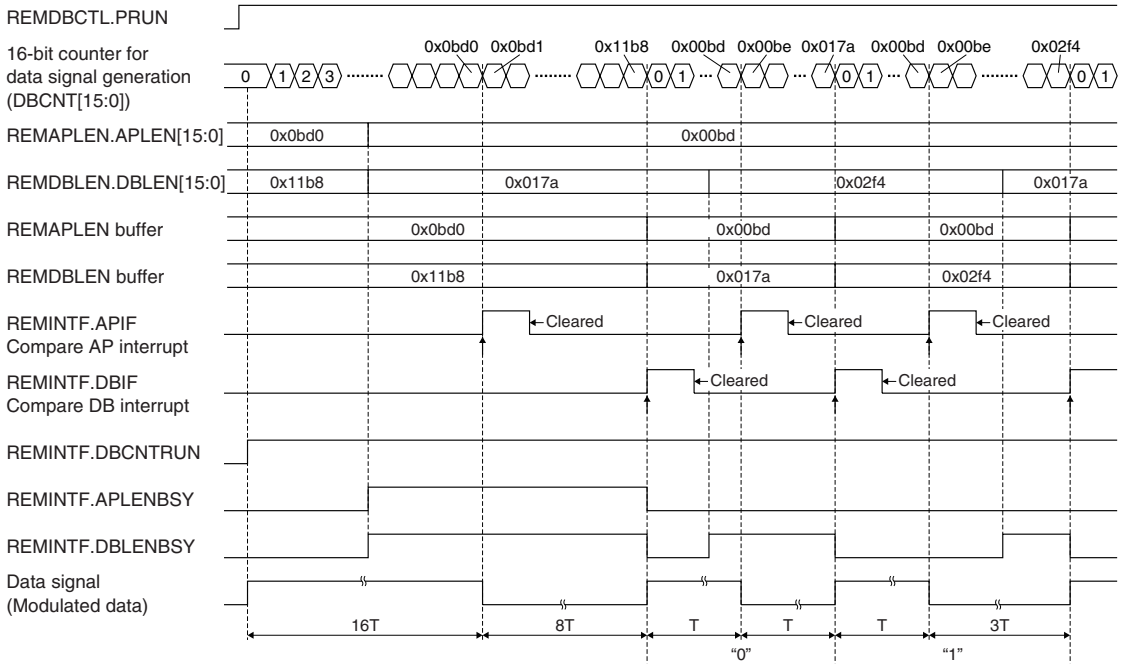


Figure 16.4.4.1 Continuous Data Transmission Example

When the compare buffer is disabled (REMDBCTL.BUFEN bit = 0), the 16-bit counter value is directly compared with the REMAPLEN.APLEN[15:0] and REMDBLEN.DBLEN[15:0] bit values. The comparison value is altered immediately after the REMAPLEN.APLEN[15:0] or REMDBLEN.DBLEN[15:0] bits are rewritten.
When the compare buffer is enabled (REMDBCTL.BUFEN bit = 1), the REMAPLEN.APLEN[15:0] and REMDBLEN.DBLEN[15:0] bit values are loaded into the compare buffers provided respectively (REMAPLEN buffer and REMDBLEN buffer) and the 16-bit counter value is compared with the compare buffers.
The comparison values are loaded into the compare buffers when the 16-bit counter is matched with the REMDBLEN buffer (when the count for the data length has completed). Therefore, the next transmit data can be set during the current data transmission. When the compare buffers are enabled, the buffer status flags (REMINTF.APLENBSY bit and REMINTF.DBLENBSY bit) become effective. The flag is set to 1 when the setting value is written to the register and cleared to 0 when the written value is transferred to the buffer.

16.5 Interrupts

The REMC2 has a function to generate the interrupts shown in Table 16.5.1.

Table 16.5.1 REMC2 Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Compare AP	REMINTF.APIF	When the REMAPLEN register (or REMAPLEN buffer) value and the 16-bit counter for data signal generation are matched	Writing 1 to the interrupt flag or the REMDBCTL.REMCRST bit
Compare DB	REMINTF.DBIF	When the REMDBLEN register (or REMDBLEN buffer) value and the 16-bit counter for data signal generation are matched	Writing 1 to the interrupt flag or the REMDBCTL.REMCRST bit

The REMC2 provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

16.6 Application Example: Driving EL Lamp

The REMC2 can be used to simply drive an EL lamp as an application example. Figures 16.6.1 and 16.6.2 show an example of an EL lamp drive circuit and an example of the drive waveform generated, respectively. For details of settings and an example of components, refer to the Application Note provided separately.

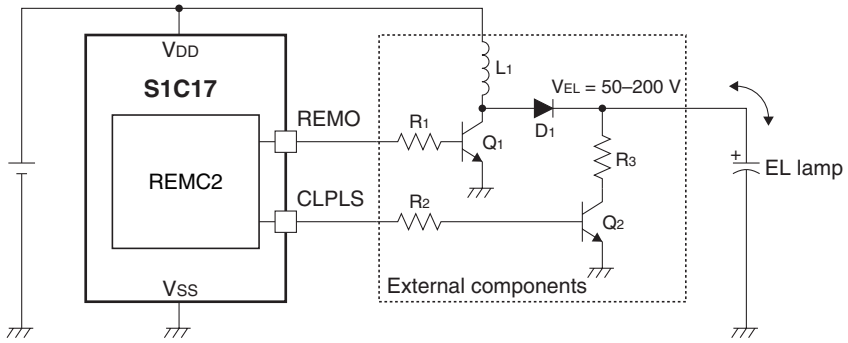


Figure 16.6.1 Example of EL Lamp Drive Circuit

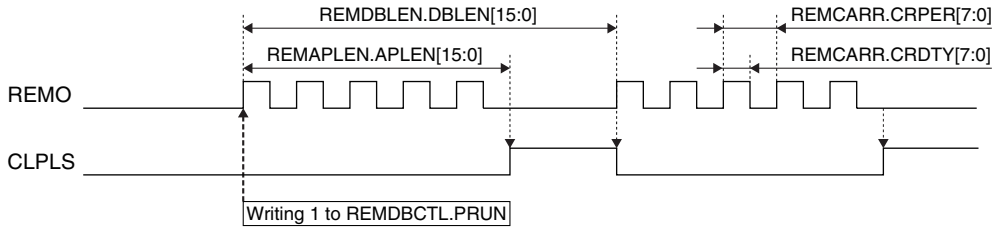


Figure 16.6.2 Example of Generated Drive Waveform

The REMO and CLPLS signals are output from the respective pins while the REMDBCTL.PRUN bit = 1. The difference between the setting values of the REMDBLEN.DBLEN[15:0] bits and REMAPLEN.APLEN[15:0] bits becomes the CLPLS pulse width (high period).

16.7 Control Registers

REMC2 Clock Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMCLK	15–9	–	0x00	–	R	–
	8	DBRUN	0	H0	R/W	
	7–4	CLKDIV[3:0]	0x0	H0	R/W	
	3–2	–	0x0	–	R	
	1–0	CLKSRC[1:0]	0x0	H0	R/W	

Bits 15–9 Reserved

Bit 8 DBRUN

This bit sets whether the REMC2 operating clock is supplied in DEBUG mode or not.

1 (R/W): Clock supplied in DEBUG mode

0 (R/W): No clock supplied in DEBUG mode

Bits 7–4 CLKDIV[3:0]

These bits select the division ratio of the REMC2 operating clock.

Bits 3–2 Reserved

Bits 1–0 CLKSRC[1:0]

These bits select the clock source of the REMC2.

Table 16.7.1 Clock Source and Division Ratio Settings

REMCLK. CLKDIV[3:0] bits	REMCLK.CLKSRC[1:0] bits			
	0x0	0x1	0x2	0x3
	IOSC	OSC1	OSC3	EXOSC
0xf	1/32,768	1/1	1/32,768	1/1
0xe	1/16,384		1/16,384	
0xd	1/8,192		1/8,192	
0xc	1/4,096		1/4,096	
0xb	1/2,048		1/2,048	
0xa	1/1,024		1/1,024	
0x9	1/512		1/512	
0x8	1/256	1/256	1/256	
0x7	1/128	1/128	1/128	
0x6	1/64	1/64	1/64	
0x5	1/32	1/32	1/32	
0x4	1/16	1/16	1/16	
0x3	1/8	1/8	1/8	
0x2	1/4	1/4	1/4	
0x1	1/2	1/2	1/2	
0x0	1/1	1/1	1/1	

(Note) The oscillation circuits/external input that are not supported in this IC cannot be selected as the clock source.

Note: The REMCLK register settings can be altered only when the REMDBCTL.MODEN bit = 0.

REMC2 Data Bit Counter Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMDBCTL	15–10	–	0x00	–	R	–
	9	PRESET	0	H0/S0	R/W	Cleared by writing 1 to the
	8	PRUN	0	H0/S0	R/W	REMDBCTL.REMCRST bit.
	7–5	–	0x0	–	R	–
	4	REMOINV	0	H0	R/W	
	3	BUFEN	0	H0	R/W	
	2	TRMD	0	H0	R/W	
	1	REMCRST	0	H0	W	
	0	MODEN	0	H0	R/W	

Bits 15–10 Reserved

Bit 9 PRESET

This bit resets the internal counters (16-bit counter for data signal generation and 8-bit counter for carrier generation).

1 (W): Reset
0 (W): Ineffective
1 (R): Resetting in progress
0 (R): Resetting finished or normal operation

Before the counter can be reset using this bit, the REMDBCTL.MODEN bit must be set to 1.
This bit is cleared to 0 after the counter reset operation has finished or when 1 is written to the REMDBCTL.REMCRST bit.

Bit 8 PRUN

This bit starts/stops counting by the internal counters (16-bit counter for data signal generation and 8-bit counter for carrier generation).

1 (W): Start counting
0 (W): Stop counting
1 (R): Counting
0 (R): Idle

Before the counter can start counting by this bit, the REMDBCTL.MODEN bit must be set to 1.
While the counter is running, writing 0 to the REMDBCTL.PRUN bit stops count operations. When the counter stops by occurrence of a compare DB in one-shot mode, this bit is automatically cleared to 0.

Bits 7–5 Reserved

Bit 4 REMOINV

This bit inverts the REMO output signal.
1 (R/W): Inverted
0 (R/W): Non-inverted

For more information, see Figure 16.4.3.1.

Bit 3 BUFEN

This bit enables or disables the compare buffers.
1 (R/W): Enable
0 (R/W): Disable

For more information, refer to "Continuous Data Transmission and Compare Buffers."

Note: The REMDBCTL.BUFEN bit must be set to 0 when setting the data signal duty and cycle for the first time.

Bit 2 TRMD

This bit selects the operation mode of the 16-bit counter for data signal generation.
1 (R/W): One-shot mode
0 (R/W): Repeat mode

For more information, refer to "REMO Output Waveform, Data signal."

Bit 1 REMCRST

This bit issues software reset to the REMC2.
1 (W): Issue software reset
0 (W): Ineffective
1 (R): Software reset is executing.
0 (R): Software reset has finished. (During normal operation)

Setting this bit resets the REMC2 internal counters and interrupt flags. This bit is automatically cleared after the reset processing has finished.

Note: After the data signal is output in one-shot mode, set the REMDBCTL.REMCRST bit to 1.

Bit 0 MODEN

This bit enables the REMC2 operations.
1 (R/W): Enable REMC2 operations (The operating clock is supplied.)
0 (R/W): Disable REMC2 operations (The operating clock is stopped.)

Note: If the REMDBCTL.MODEN bit is altered from 1 to 0 while sending data, the data being sent cannot be guaranteed. When setting the REMDBCTL.MODEN bit to 1 again after that, be sure to write 1 to the REMDBCTL.REMCRST bit as well.

REMC2 Data Bit Counter Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMDBCNT	15–0	DBCNT[15:0]	0x0000	H0/S0	R	Cleared by writing 1 to the REMDBCTL.REMCRST bit.

Bits 15–0 DBCNT[15:0]

The current value of the 16-bit counter for data signal generation can be read out through these bits.

REMC2 Data Bit Active Pulse Length Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMAPLEN	15–0	APLEN[15:0]	0x0000	H0	R/W	Writing enabled when REMDBCTL.MODEN bit = 1.

Bits 15–0 APLEN[15:0]

These bits set the active pulse length of the data signal (high period when the REMDBCTL.REMOINV bit = 0 or low period when the REMDBCTL.REMOINV bit = 1).
The REMO pin output is set to the active level from the 16-bit counter for data signal generation = 0x0000 and it is inverted to the inactive level when the counter exceeds the REMAPLEN.APLEN[15:0] bit-setting value. The data signal duty ratio is determined by this setting and the REMDBLEN.DBLEN[15:0] bit-setting. (See Figure 16.4.3.3.)
Before this register can be rewritten, the REMDBCTL.MODEN bit must be set to 1.

REMC2 Data Bit Length Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMDBLEN	15–0	DBLEN[15:0]	0x0000	H0	R/W	Writing enabled when REMDBCTL.MODEN bit = 1.

Bits 15–0 DBLEN[15:0]

These bits set the data length of the data signal (length of one cycle).
A data signal cycle begins with the 16-bit counter for data signal generation = 0x0000 and ends when the counter exceeds the REMDBLEN.DBLEN[15:0] bit-setting value. (See Figure 16.4.3.3.)
Before this register can be rewritten, the REMDBCTL.MODEN bit must be set to 1.

REMC2 Status and Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMINTF	15–11	–	0x00	–	R	–
	10	DBCNTRUN	0	H0/S0	R	Cleared by writing 1 to the REMDBCTL.REMCRST bit.
	9	DBLENBSY	0	H0	R	Effective when the REMDBCTL.BUFEN bit = 1.
	8	APLENBSY	0	H0	R	
	7–2	–	0x00	–	R	–
	1	DBIF	0	H0/S0	R/W	Cleared by writing 1 to this bit or the REMDBCTL.REMCRST bit.
	0	APIF	0	H0/S0	R/W	

Bits 15–11 Reserved

Bit 10 DBCNTRUN

This bit indicates whether the 16-bit counter for data signal generation is running or not. (See Figure 16.4.4.1.)
1 (R): Running (Counting)
0 (R): Idle

Bit 9 DBLENBSY

This bit indicates whether the value written to the REMDBLEN.DBLEN[15:0] bits is transferred to the REMDBLEN buffer or not. (See Figure 16.4.4.1.)
1 (R): Transfer to the REMDBLEN buffer has not completed.
0 (R): Transfer to the REMDBLEN buffer has completed.

While this bit is set to 1, writing to the REMDBLEN.DBLEN[15:0] bits is ineffective.

Bit 8 APLENBSY

This bit indicates whether the value written to the REMAPLEN.APLEN[15:0] bits is transferred to the REMAPLEN buffer or not. (See Figure 16.4.4.1.)
1 (R): Transfer to the REMAPLEN buffer has not completed.
0 (R): Transfer to the REMAPLEN buffer has completed.

While this bit is set to 1, writing to the REMAPLEN.APLEN[15:0] bits is ineffective.

Bits 7–2 Reserved

Bit 1 DBIF
Bit 0 APIF

These bits indicate the REMC2 interrupt cause occurrence status.
1 (R): Cause of interrupt occurred
0 (R): No cause of interrupt occurred
1 (W): Clear flag
0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:
REMINTF.DBIF bit: Compare DB interrupt
REMINTF.APIF bit: Compare AP interrupt

These interrupt flags are also cleared to 0 when 1 is written to the REMDBCTL.REMCRST bit.

REMC2 Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMINTE	15–8	–	0x00	–	R	–
	7–2	–	0x00	–	R	
	1	DBIE	0	H0	R/W	
	0	APIE	0	H0	R/W	

Bits 15–2 Reserved

Bit 1 DBIE
Bit 0 APIE

These bits enable REMC2 interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
REMINTE.DBIE bit: Compare DB interrupt
REMINTE.APIE bit: Compare AP interrupt

REMC2 Carrier Waveform Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMCARR	15–8	CRDTY[7:0]	0x00	H0	R/W	–
	7–0	CRPER[7:0]	0x00	H0	R/W	

Bits 15–8 CRDTY[7:0]

These bits set the high level period of the carrier signal.
The carrier signal is set to high level from the 8-bit counter for carrier generation = 0x00 and it is inverted to low level when the counter exceeds the REMCARR.CRDTY[7:0] bit-setting value. The carrier signal duty ratio is determined by this setting and the REMCARR.CRPER[7:0] bit-setting. (See Figure 16.4.3.2.)

Bits 7–0 CRPER[7:0]

These bits set the carrier signal cycle.
A carrier signal cycle begins with the 8-bit counter for carrier generation = 0x00 and ends when the counter exceeds the REMCARR.CRPER[7:0] bit-setting value. (See Figure 16.4.3.2.)

REMC2 Carrier Modulation Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
REMCCTL	15–8	–	0x00	–	R	–
	7–1	–	0x00	–	R	
	0	CARREN	0	H0	R/W	

Bits 15–1 Reserved

Bit 0 CARREN

This bit enables carrier modulation.

1 (R/W): Enable carrier modulation

0 (R/W): Disable carrier modulation (output data signal only)

Note: When carrier modulation is disabled, the REMDBCTL.REMOINV bit should be set to 0.

17 10-bit A/D Converter (ADC10A)

17.1 Overview

The ADC10A is a successive approximation type 10-bit A/D converter.
The features of the ADC10A are listed below.

- Conversion method: Successive approximation type
- Resolution: 10 bits
- Analog input voltage range: AVDD to VSS
- Supports two conversion modes: 1. One-time conversion mode
  2. Continuous conversion mode
- Supports three conversion triggers: 1. Software trigger
  2. 16-bit timer underflow trigger
  3. External trigger
- Can convert multiple analog input signals sequentially.
- Can generate conversion completion and overwrite error interrupts.

Figure 17.1.1 shows the ADC10A configuration.

Table 17.1.1 ADC10A Configuration of S1C17589

Item	S1C17589
Number of channels	2 channels (Ch.0 and Ch.1)
Number of analog signal inputs per channel	Ch.0: 8 inputs (ADIN00–ADIN07) Ch.1: 8 inputs (ADIN10–ADIN17)
16-bit timer used as conversion clock and trigger sources	Ch.0 ← 16-bit timer Ch.3 Ch.1 ← 16-bit timer Ch.4

Note: Depending on the package type, some analog signal input ports are not available. Refer to "Pin Descriptions" in the "Overview" chapter for the analog signal input ports that can be used.

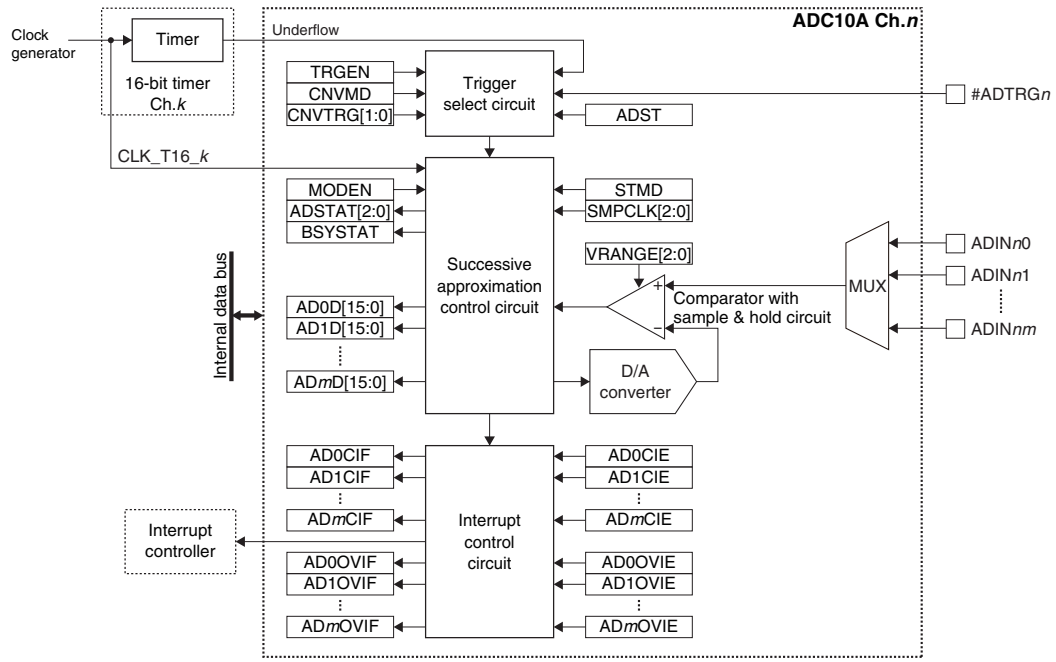


Figure 17.1.1 ADC10A Configuration

Note: In this chapter, *n*, *m*, and *k* refer to an ADC10A channel number, an analog input pin number, and a 16-bit timer channel number, respectively.

17.2 Input Pins and External Connections

17.2.1 List of Input Pins

Table 17.2.1.1 lists the ADC10A pins.

Table 17.2.1.1 List of ADC10A Pins

Pin name	I/O*	Initial status*	Function
ADIN*nm*	A	Hi-Z	Analog signal input
#ADTRG*n*	I	I	External trigger input

* Indicates the status when the pin is configured for the ADC10A.

If the port is shared with the ADC10A pin and other functions, the ADC10A input function must be assigned to the port before activating the ADC10A. For more information, refer to the "I/O Ports" chapter.

17.2.2 External Connections

Figure 17.2.2.1 shows a connection diagram between the ADC10A and external devices.

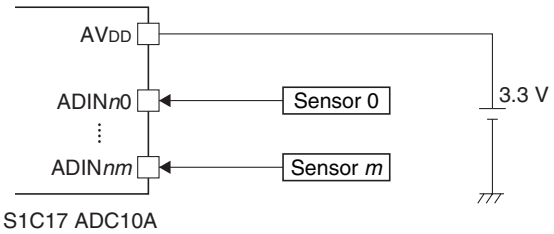


Figure 17.2.2.1 Connections between ADC10A and External Devices

17.3 Clock Settings

17.3.1 ADC10A Operating Clock

The 16-bit timer Ch.*k* operating clock CLK_T16_*k* is also used as the ADC10A operating clock. For more information on the CLK_T16_*k* settings and clock supply in SLEEP and DEBUG modes, refer to "Clock Settings" in the "16-bit Timers" chapter.

Note: When the CLK_T16_*k* supply stops during A/D conversion (e.g., when the CPU enters SLEEP or DEBUG mode), correct conversion results cannot be obtained even if the clock supply is resumed after that. In this case, perform A/D conversion again.

17.3.2 Sampling Time

The ADC10A includes a sample and hold circuit. The sampling time must be set so that it will satisfy the time required for acquiring input voltage (t_{ACQ}: acquisition time). Figure 17.3.2.1 shows an equivalent circuit of the analog input portion.

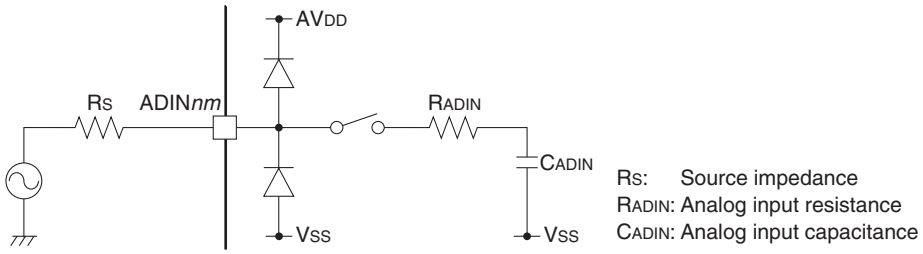


Figure 17.3.2.1 Equivalent Circuit of Analog Input Portion

For the RADIN and CADIN values in the equivalent circuit, refer to "10-bit A/D Converter Characteristics" in the "Electrical Characteristics" chapter. Based on these values, configure the ADC10A operating clock CLK_T16_*k* and the ADC10_*n*TRG.SMPCLK[2:0] bits that set the sampling time so that these settings will satisfy the equations shown below.

$$t_{ACQ} = 8 \times (R_S + R_{ADIN}) \times C_{ADIN} \quad \text{(Eq. 17.1)}$$

$$\frac{1}{f_{CLK\_ADC}} \times SMPCLK > t_{ACQ} \quad \text{(Eq. 17.2)}$$

Where

f_{CLK_ADC}: CLK_T16_*k* frequency [Hz]

SMPCLK: Sampling time = ADC10_*n*TRG.SMPCLK[2:0] bit-setting (4 to 11 CLK_T16_*k* cycles)

The following shows the relationship between the sampling time and the maximum sampling rate.

$$\text{Maximum sampling rate [sps]} = \frac{f_{CLK\_ADC}}{SMPCLK + 11} \quad \text{(Eq. 17.3)}$$

17.4 Operations

17.4.1 Initialization

The ADC10A should be initialized with the procedure shown below.

1. Assign the ADC10A input function to the ports. (Refer to the "I/O Ports" chapter.)
2. Configure the 16-bit timer Ch.*k* operating clock so that it will satisfy the sampling time.
3. Set the ADC10_*n*CTL.MODEN bit to 1. (Enable ADC10A operations)
4. Configure the following ADC10_*n*TRG register bits:
   - ADC10_*n*TRG.SMPCLK[2:0] bits (Set sampling time)
   - ADC10_*n*TRG.CNVTRG[1:0] bits (Select conversion start trigger source)
   - ADC10_*n*TRG.CNVMD bit (Set conversion mode)
   - ADC10_*n*TRG.STMD bit (Set data storing mode)
   - ADC10_*n*TRG.STAAIN[2:0] bits (Set analog input pin to be A/D converted first)
   - ADC10_*n*TRG.ENDAIN[2:0] bits (Set analog input pin to be A/D converted last)
5. Set the ADC10_*n*CFG.VRANGE[2:0] bits. (Set operating voltage range according to AVDD)
6. Set the following bits when using the interrupt:
   - Write 1 to the interrupt flags in the ADC10_*n*INTF register. (Clear interrupt flags)
   - Set the interrupt enable bits in the ADC10_*n*INTE register to 1. (Enable interrupts)

17.4.2 Conversion Start Trigger Source

The trigger source, which starts A/D conversion, can be selected from the three types shown below using the ADC10_*n*TRG.CNVTRG[1:0] bits.

External trigger (#ADTRG*n* pin)

Writing 1 to the ADC10_*n*CTL.TRGEN bit enables the ADC10A to accept trigger inputs. After that, the falling edge of the signal input to the #ADTRG*n* pin starts A/D conversion.

16-bit timer Ch.*k* underflow trigger

Writing 1 to the ADC10_*n*CTL.TRGEN bit enables the ADC10A to accept trigger inputs. After that, A/D conversion is started when an underflow occurs in the 16-bit timer Ch.*k*.

Software trigger

Writing 1 to the ADC10_*n*CTL.TRGEN bit enables the ADC10A to accept trigger inputs. After that, writing 1 to the ADC10_*n*CTL.ADST bit starts A/D conversion.

Trigger inputs can be accepted while the ADC10_*n*CTL.BSYSTAT bit is set to 0 and are ignored while set to 1. A/D conversion is actually started in sync with CLK_T16_*k* after a trigger is accepted. Writing 0 to the ADC10_*n*CTL.ADST bit stops A/D conversion after the one currently being executed has completed regardless of the trigger source selected.

17.4.3 Conversion Mode and Analog Input Pin Settings

The ADC10A can be put into two conversion modes shown below using the ADC10_*n*TRG.CNVMD bit. Each mode allows setting of analog input pin range to be A/D converted. The analog input pin range can be set using the ADC10_*n*TRG.STAAIN[2:0] bits for specifying the first analog input pin and the ADC10_*n*TRG.ENDAIN[2:0] bits for specifying the last analog input pin. The analog input signals within the specified range are A/D converted successively in ascending order of the pin numbers.

One-time conversion mode

Once the ADC10A executes A/D conversion for all the analog input signals within the specified range, it is automatically stopped.

Continuous conversion mode

The ADC10A repeatedly executes A/D conversion within the specified range until 0 is written to the ADC10_*n*CTL.ADST bit.

17.4.4 A/D Conversion Operations and Control Procedures

The following shows A/D conversion control procedures and the ADC10A operations.

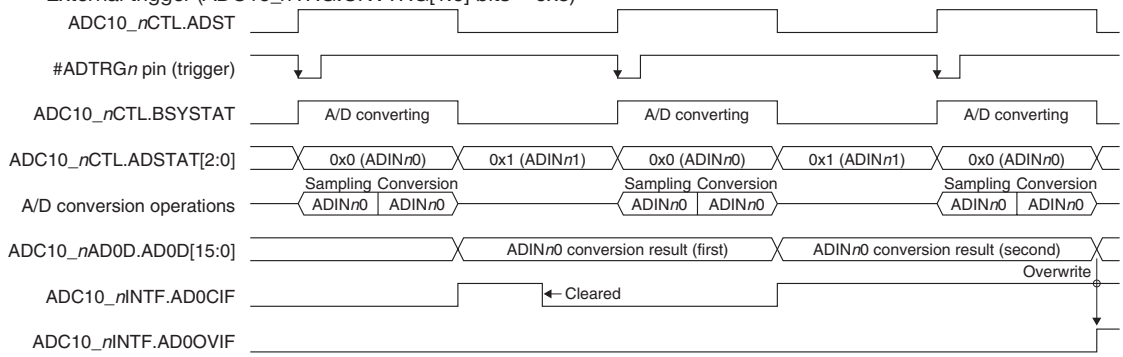
Control procedure in one-time conversion mode

1. Write 1 to the ADC10_*n*CTL.TRGEN bit. (After that, a conversion start trigger is issued.)
2. Wait for an ADC10A interrupt.
   i. If the ADC10_*n*INTF.AD*m*CIF bit = 1 (analog input signal *m* A/D conversion completion interrupt), clear the ADC10_*n*INTF.AD*m*CIF bit and then go to Step 3.
   ii. If the ADC10_*n*INTF.AD*m*OVIF bit = 1 (analog input signal *m* A/D conversion result overwrite error interrupt), clear the ADC10_*n*INTF.AD*m*OVIF bit and terminate as an error or retry A/D conversion.
3. Read the A/D conversion result of the analog input *m* (ADC10_*n*AD*m*D.AD*m*D[15:0] bits).
   * The 10-bit conversion results are located at the low-order 10 bits or high-order 10-bits within the ADC10_*n*AD*m*D.AD*m*D[15:0] bits according to the ADC10_*n*TRG.STMD bit setting.
4. Repeat Steps 2 and 3 until A/D conversion for all the analog input pins within the specified range is completed.
5. To forcefully terminate the A/D conversion being executed, write 0 to the ADC10_*n*CTL.ADST bit.
   The ADC10A stops operating after the A/D conversion currently being executed has completed.

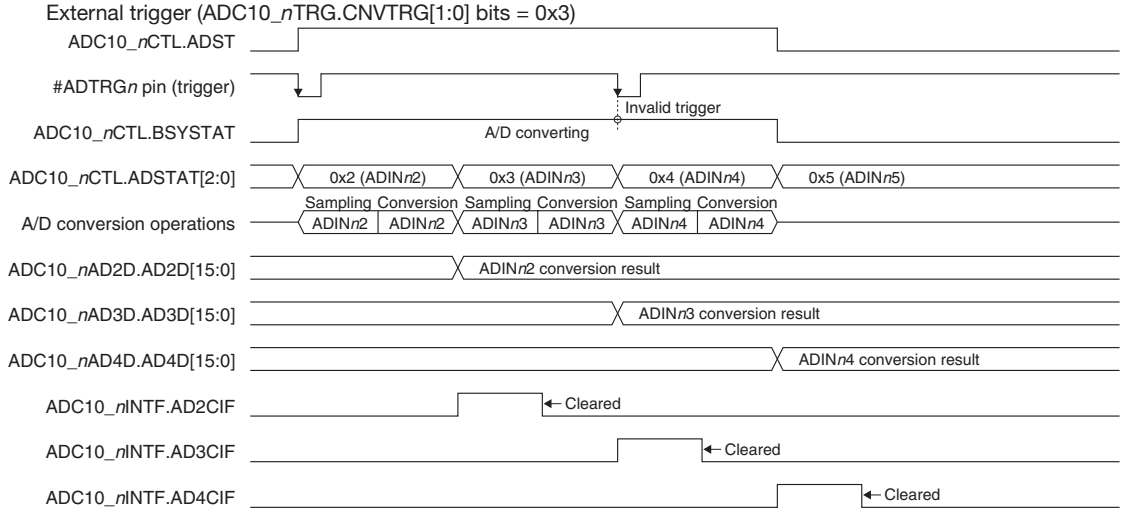
Control procedure in continuous conversion mode

1. Write 1 to the ADC10_*n*CTL.TRGEN bit. (After that, a conversion start trigger is issued.)
2. Wait for an ADC10A interrupt.
   i. If the ADC10_*n*INTF.AD*m*CIF bit = 1 (analog input signal *m* A/D conversion completion interrupt), clear the ADC10_*n*INTF.AD*m*CIF bit and then go to Step 3.
   ii. If the ADC10_*n*INTF.AD*m*OVIF bit = 1 (analog input signal *m* A/D conversion result overwrite error interrupt), clear the ADC10_*n*INTF.AD*m*OVIF bit and terminate as an error or retry A/D conversion.
3. Read the A/D conversion result of the analog input *m* (ADC10_*n*AD*m*D.AD*m*D[15:0] bits).
4. Repeat Steps 2 and 3 until terminating A/D conversion.
5. Write 0 to the ADC10_*n*CTL.ADST bit.
   The ADC10A stops operating after the A/D conversion currently being executed has completed.

(1) One-time conversion mode (ADC10_*n*TRG.CNVMD bit = 0)
A/D conversion for ADIN*n*0 (ADC10_*n*TRG.STAAIN[2:0] bits = 0x0, ADC10_*n*TRG.ENDAIN[2:0] bits = 0x0)
External trigger (ADC10_*n*TRG.CNVTRG[1:0] bits = 0x3)



(2) One-time conversion mode (ADC10_*n*TRG.CNVMD bit = 0)
A/D conversion for ADIN*n*2–4 (ADC10_*n*TRG.STAAIN[2:0] bits = 0x2, ADC10_*n*TRG.ENDAIN[2:0] bits = 0x4)
External trigger (ADC10_*n*TRG.CNVTRG[1:0] bits = 0x3)



(3) Continuous conversion mode (ADC10_*n*TRG.CNVMD bit = 1)
A/D conversion for ADIN*n*3–4 (ADC10_*n*TRG.STAAIN[2:0] bits = 0x3, ADC10_*n*TRG.ENDAIN[2:0] bits = 0x4)
Software trigger (ADC10_*n*TRG.CNVTRG[1:0] bits = 0x0)

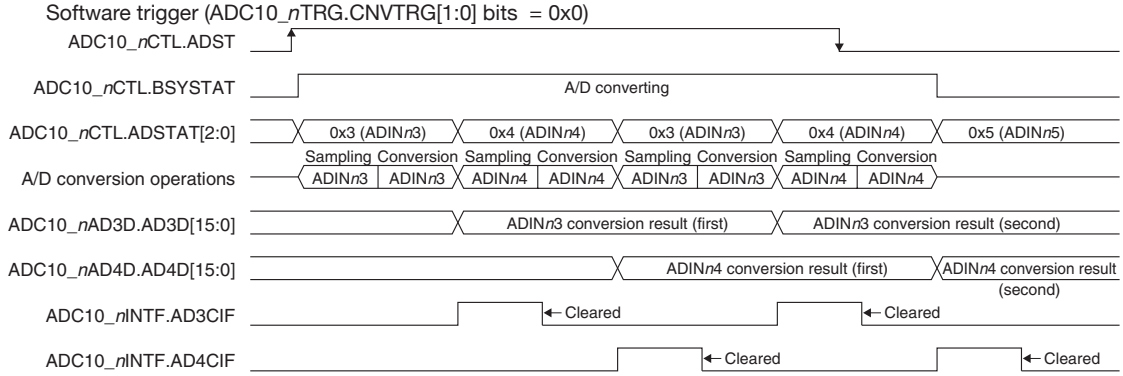


Figure 17.4.4.1 A/D Conversion Operations

17.5 Interrupts

The ADC10A has a function to generate the interrupts shown in Table 17.5.1.

Table 17.5.1 ADC10A Interrupt Function

Interrupt	Interrupt flag	Set condition	Clear condition
Analog input signal *m* A/D conversion completion	ADC10_*n*INTF.AD*m*CIF	When an analog input signal *m* A/D conversion result is loaded to the ADC10_*n*AD*m*D register	Writing 1
Analog input signal *m* A/D conversion result overwrite error	ADC10_*n*INTF.AD*m*OVIF	When a new A/D conversion result is loaded to the ADC10_*n*AD*m*D register while the ADC10_*n*INTF.AD*m*CIF bit = 1	Writing 1

Note that the A/D conversion continues even if an A/D conversion result overwrite error has occurred. A/D conversion result overwrite errors are decided regardless of whether the ADC10_*n*AD*m*D register has been read or not.

The ADC10A provides interrupt enable bits corresponding to each interrupt flag. An interrupt request is sent to the interrupt controller only when the interrupt flag, of which interrupt has been enabled by the interrupt enable bit, is set. For more information on interrupt control, refer to the "Interrupt Controller" chapter.

17.6 Control Registers

ADC10A Ch.*n* Control Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC10_*n*CTL	15	–	0	–	R	–
	14–12	ADSTAT[2:0]	0x0	H0	R	
	11	–	0	–	R	
	10	BSYSTAT	0	H0	R	
	9–8	–	0x0	–	R	
	7–5	–	0x0	–	R	
	4	TRGEN	0	H0	R/W	
	3–2	–	0x0	–	R	
	1	ADST	0	H0	R/W	
	0	MODEN	0	H0	R/W	

Bit 15 Reserved

Bits 14–12 ADSTAT[2:0]

These bits indicate the analog input pin number *m* being A/D converted.

Table 17.6.1 Relationship Between Control Bit Value and Analog Input Pin

ADC10_*n*CTL.ADSTAT[2:0] bits ADC10_*n*TRG.STAAIN[2:0] bits ADC10_*n*TRG.ENDAIN[2:0] bits	Analog input pin
0x7	ADIN*n*7
0x6	ADIN*n*6
0x5	ADIN*n*5
0x4	ADIN*n*4
0x3	ADIN*n*3
0x2	ADIN*n*2
0x1	ADIN*n*1
0x0	ADIN*n*0

These bits indicate the last converted analog input pin number after A/D conversion is forcefully terminated by writing 0 to the ADC10_*n*CTL.ADST bit or automatically terminated in one-time conversion mode (ADC10_*n*TRG.CNVMD = 0). If A/D conversion is stopped after the maximum analog input pin number (different in each model) has been completed, these bits indicate ADIN*n*0.

Bit 11 Reserved

Bit 10 BSYSTAT

This bit indicates whether the ADC10A is executing A/D conversion or not.
1 (R/W): A/D converting
0 (R/W): Idle

Bits 9–5 Reserved

Bit 4 TRGEN

This bit enables to accept triggers.
1 (R/W): Enable trigger acceptance
0 (R/W): Disable trigger acceptance

When ADC10_*n*CTL.TRGEN = 0, the triggers issued cannot be accepted regardless of the trigger source type.

Bits 3–2 Reserved

Bit 1 ADST

This bit issue a software trigger. Also terminates converting operations regardless of the trigger source while A/D conversion is being executed.
1 (W): Issue software trigger
1 (R): A/D converting
0 (R/W): Terminate conversion

This bit retains 1 during A/D conversion and automatically reverts to 0 after the conversion has completed. After 0 is written to this bit to forcefully terminate conversion, the ADC10A stops after the A/D conversion being executed is completed.

Note: After 1 is written to the ADC10_*n*CTL.ADST bit, writing 0 is ignored for a maximum of two CLK_T16_*k* cycles.

Bit 0 MODEN

This bit enables the ADC10A operations.
1 (R/W): Enable ADC10A operations (The operating clock is supplied.)
0 (R/W): Disable ADC10A operations (The operating clock is stopped.)

Note: After 0 is written to the ADC10_*n*CTL.MODEN bit, the ADC10A executes a terminate processing. Before the clock source is deactivated, read the ADC10_*n*CTL.MODEN bit to make sure that it is set to 0.

ADC10A Ch.*n* Trigger/Analog Input Select Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC10_*n*TRG	15–14	–	0x0	–	R	–
	13–11	ENDAIN[2:0]	0x0	H0	R/W	
	10–8	STAAIN[2:0]	0x0	H0	R/W	
	7	STMD	0	H0	R/W	
	6	CNVMD	0	H0	R/W	
	5–4	CNVTRG[1:0]	0x0	H0	R/W	
	3	–	0	–	R	
	2–0	SMPCLK[2:0]	0x5	H0	R/W	

Note: Make sure that the ADC10_*n*CTL.BSYSTAT bit is set to 0 before altering the ADC10_*n*TRG register.

Bits 15–14 Reserved

Bits 13–11 ENDAIN[2:0]

These bits set the analog input pin to be A/D converted last.
See Table 17.6.1 for the relationship between analog input pins and bit setting values.

Note: The analog input pin range to perform A/D conversion must be set as ADC10_*n*TRG.ENDAIN[2:0] bits ≥ ADC10_*n*TRG.STAAIN[2:0] bits.

Bits 10–8 STAAIN[2:0]

These bits set the analog input pin to be A/D converted first.
See Table 17.6.1 for the relationship between analog input pins and bit setting values.

Bit 7 STMD

This bit selects the data alignment when the conversion results are loaded into the A/D conversion result registers (ADC10_*n*AD*m*D.AD*m*D[15:0] bits).
1 (R/W): Left justify
0 (R/W): Right justify

All the A/D conversion result registers change their data alignment immediately after this bit is altered. This does not affect the conversion results.

6.1 Conversion Data Alignment

Bit 6 CNVMD

This bit sets the A/D conversion mode.
1 (R/W): Continuous conversion mode
0 (R/W): One-time conversion mode

Bits 5–4 CNVTRG[1:0]

These bits select a trigger source to start A/D conversion.

Table 17.6.2 Trigger Source Selection

ADC10_*n*TRG.CNVTRG[1:0] bits	Trigger source
0x3	#ADTRG*n* pin (external trigger)
0x2	Reserved
0x1	16-bit timer Ch.*k* underflow
0x0	ADC10_*n*CTL.ADST bit (software trigger)

Bit 3 Reserved

Bits 2–0 SMPCLK[2:0]

These bits set the analog input signal sampling time.

Table 17.6.3 Sampling Time Settings

ADC10_*n*TRG.SMPCLK[2:0] bits	Sampling time (Number of CLK_T16_*k* cycles)
0x7	11 cycles
0x6	10 cycles
0x5	9 cycles
0x4	8 cycles
0x3	7 cycles
0x2	6 cycles
0x1	5 cycles
0x0	4 cycles

ADC10A Ch.*n* Configuration Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC10_*n*CFG	15–8	–	0x00	–	R	–
	7–3	–	0x00	–	R	
	2–0	VRANGE[2:0]	0x4	H0	R/W	

Note: Make sure that the ADC10_*n*CTL.BSYSTAT bit is set to 0 before altering the ADC10_*n*CFG register.

Bits 15–3 Reserved

Bits 2–0 VRANGE[2:0]

These bits set the A/D converter operating voltage range.

Table 17.6.4 A/D Converter Operating Voltage Range Setting

ADC10_*n*CFG.VRANGE[2:0] bits	A/D converter operating voltage range
0x7–0x5	Reserved
0x4	AV_{DD} = 4.7 to 5.5 V
0x3	AV_{DD} = 4.0 to 5.0 V
0x2	AV_{DD} = 3.3 to 4.3 V
0x1	AV_{DD} = 3.0 to 3.6 V
0x0	AV_{DD} = 2.7 to 3.3 V

ADC10A Ch.*n* Interrupt Flag Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC10_*n*INTF	15	AD7OVIF	0	H0	R/W	Cleared by writing 1.
	14	AD6OVIF	0	H0	R/W	
	13	AD5OVIF	0	H0	R/W	
	12	AD4OVIF	0	H0	R/W	
	11	AD3OVIF	0	H0	R/W	
	10	AD2OVIF	0	H0	R/W	
	9	AD1OVIF	0	H0	R/W	
	8	AD0OVIF	0	H0	R/W	
	7	AD7CIF	0	H0	R/W	
	6	AD6CIF	0	H0	R/W	
	5	AD5CIF	0	H0	R/W	
	4	AD4CIF	0	H0	R/W	
	3	AD3CIF	0	H0	R/W	
	2	AD2CIF	0	H0	R/W	
	1	AD1CIF	0	H0	R/W	
	0	AD0CIF	0	H0	R/W	

Bits 15–8 AD*m*OVIF

Bits 7–0 AD*m*CIF

These bits indicate the ADC10A interrupt cause occurrence status.

1 (R): Cause of interrupt occurred

0 (R): No cause of interrupt occurred

1 (W): Clear flag

0 (W): Ineffective

The following shows the correspondence between the bit and interrupt:

ADC10_*n*INTF.AD*m*OVIF bit: Analog input signal *m* A/D conversion result overwrite error interrupt

ADC10_*n*INTF.AD*m*CIF bit: Analog input signal *m* A/D conversion completion interrupt

ADC10A Ch.*n* Interrupt Enable Register

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC10_*n*INTE	15	AD7OVIE	0	H0	R/W	–
	14	AD6OVIE	0	H0	R/W	
	13	AD5OVIE	0	H0	R/W	
	12	AD4OVIE	0	H0	R/W	
	11	AD3OVIE	0	H0	R/W	
	10	AD2OVIE	0	H0	R/W	
	9	AD1OVIE	0	H0	R/W	
	8	AD0OVIE	0	H0	R/W	
	7	AD7CIE	0	H0	R/W	
	6	AD6CIE	0	H0	R/W	
	5	AD5CIE	0	H0	R/W	
	4	AD4CIE	0	H0	R/W	
	3	AD3CIE	0	H0	R/W	
	2	AD2CIE	0	H0	R/W	
	1	AD1CIE	0	H0	R/W	
	0	AD0CIE	0	H0	R/W	

Bits 15–8 AD*m*OVIE
Bits 7–0 AD*m*CIE

These bits enable ADC10A interrupts.
1 (R/W): Enable interrupts
0 (R/W): Disable interrupts

The following shows the correspondence between the bit and interrupt:
ADC10_*n*INTE.AD*m*OVIE bit: Analog input signal *m* A/D conversion result overwrite error interrupt
ADC10_*n*INTE.AD*m*CIE bit: Analog input signal *m* A/D conversion completion interrupt

ADC10A Ch.*n* Result Register *m*

Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
ADC10_*n*AD*m*D	15–0	AD*m*D[15:0]	0x0000	H0	R	–

Bits 15–0 AD*m*D[15:0]

These bits are the A/D conversion results of the analog input signal *m*.

18 Multiplier/Divider (COPRO2)

18.1 Overview

COPRO2 is the coprocessor that provides multiplier/divider functions. The features of COPRO2 are listed below.

- Multiplication: Supports signed/unsigned multiplications.
  (16 bits × 16 bits = 32 bits)
  Can be executed in 1 cycle.
- Multiplication and accumulation (MAC): Supports signed/unsigned MAC operations with overflow detection function. (16 bits × 16 bits + 32 bits = 32 bits)
  Can be executed in 1 cycle.
- Division: Supports signed/unsigned divisions.
  (32 bits ÷ 32 bits = 32 bits with 32-bit reminder)
  Can be executed in 17 to 20 cycles.
  Overflow detection and division by zero processing are not supported.

Figure 18.1.1 shows the COPRO2 configuration.

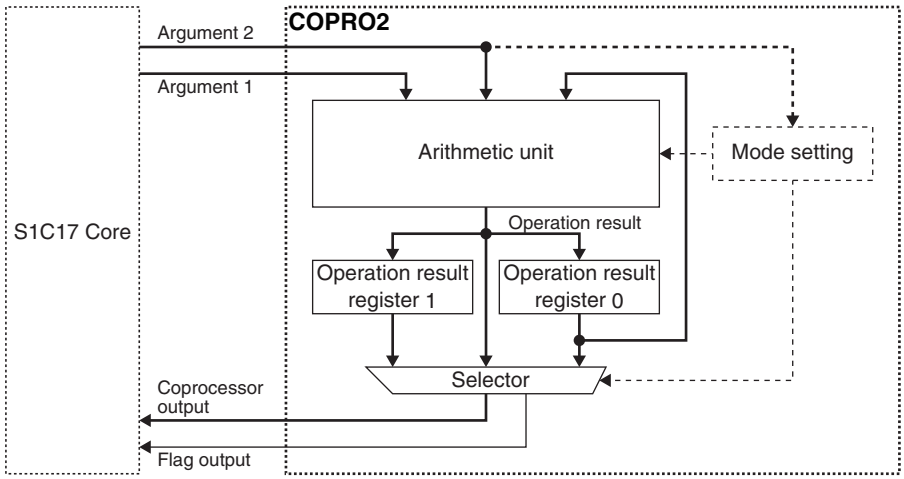


Figure 18.1.1 COPRO2 Configuration

18.2 Operation Mode and Output Mode

COPRO2 operates according to the operation mode specified by the application program. As listed in Table 18.2.1, COPRO2 supports 11 operations.
The multiplication, division and MAC results are 32-bit data, therefore, the S1C17 Core cannot read them in one access cycle. The output mode is provided to specify the high-order 16 bits or low-order 16 bits of the operation result register 0 or 1 to be read from COPRO2.
The operation and output modes can be specified with a 7-bit data by writing it to the mode setting register in COPRO2. Use a "`ld.cw`" instruction for this writing.

`ld.cw %rd,%rs` %rs[6:0] is written to the mode setting register. (%rd: not used)
`ld.cw %rd,`*`imm7`* *imm7*[6:0] is written to the mode setting register. (%rd: not used)

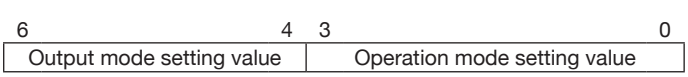


Figure 18.2.1 Mode Setting Register

Table 18.2.1 Mode Settings

Setting value (D[6:4])	Output mode	Setting value (D[3:0])	Operation mode
0x0	**16 low-order bits output mode 0** The low-order 16 bits of the operation result register 0 can be read as the coprocessor output.	0x0	**Initialize mode 0** Clears the operation result registers 0 and 1 to 0x0.
0x1	**16 high-order bits output mode 0** The high-order 16 bits of the operation result register 0 can be read as the coprocessor output.	0x1	**Initialize mode 1** Loads the 16-bit augend into the low-order 16 bits of the operation result register 0.
0x2	**16 low-order bits output mode 1** The low-order 16 bits of the operation result register 1 can be read as the coprocessor output.	0x2	**Initialize mode 2** Loads the 32-bit data into the operation result register 0.
0x3	**16 high-order bits output mode 1** The high-order 16 bits of the operation result register 1 can be read as the coprocessor output.	0x3	**Operation result read mode** Outputs the data in the operation result registers 0 and 1 without computation.
0x4–0x7	Reserved	0x4	**Unsigned multiplication mode** Performs unsigned multiplication.
		0x5	**Signed multiplication mode** Performs signed multiplication.
		0x6	**Unsigned MAC mode** Performs unsigned MAC operation.
		0x7	**Signed MAC mode** Performs signed MAC operation.
		0x8	**Unsigned division mode** Performs unsigned division.
		0x9	**Signed division mode** Performs signed division.
		0xa	**Initialize mode 3** Loads the 32-bit data into the operation result register 1.
		0xb–0xf	Reserved

18.3 Multiplication

The multiplication function performs "A (32 bits) = B (16 bits) × C (16 bits)."
The following shows a procedure to perform a multiplication:

1. Set the mode to 0x04 (unsigned multiplication, 16 low-order bits output mode 0) or 0x05 (signed multiplication, 16 low-order bits output mode 0).
2. Send the 16-bit multiplicand (B) and 16-bit multiplier (C) to COPRO2 using a "`ld.ca`" instruction.
3. Read the one-half result (16 low-order bits = A[15:0]) and the flag status.
4. Set the mode to 0x13 (operation result read, 16 high-order bits output mode 0).
5. Read another one-half result (16 high-order bits = A[31:16]).

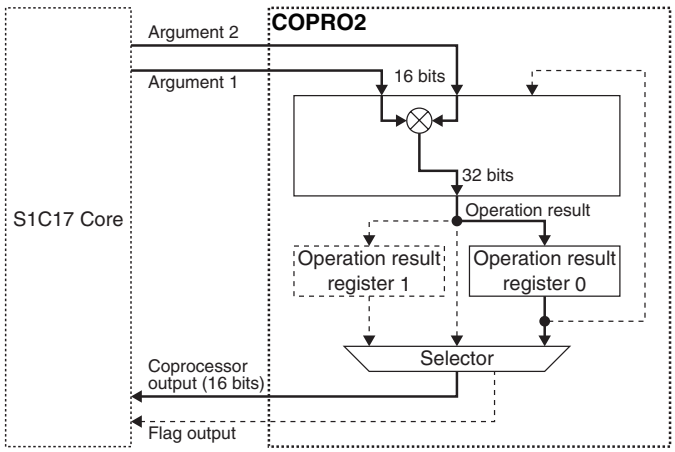


Figure 18.3.1 Data Path in Multiplication Mode

Table 18.3.1 Operation in Multiplication Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x04 or 0x05	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs %rd ← res0[15:0]	psr (CVZN) ← 0b0000	The operation result register 0 keeps the operation result until it is rewritten by other operation.
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* %rd ← res0[15:0]		
0x14 or 0x15	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs %rd ← res0[31:16]		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* %rd ← res0[31:16]		

res0: operation result register 0

Example:

```
ld.cw %r0,0x04 ; Sets the mode (unsigned multiplication mode and 16 low-order bits output mode 0).
ld.ca %r0,%r1  ; Performs "res0[31:0] = %r0[15:0] × %r1[15:0]" and loads the 16 low-order bits of the
               result to %r0.
ld.cw %r0,0x13 ; Sets the mode (operation result read mode and 16 high-order bits output mode 0).
ld.ca %r1,%r0  ; Loads the 16 high-order bits of the result to %r1.
```

18.4 Division

The division function performs "A (32 bits) = B (32 bits) ÷ C (32 bits), D (32 bits) = remainder."
The following shows a procedure to perform a division:

1. Set the mode to 0x02 (initialize mode 2).
2. Set the 32-bit dividend (B) to the operation result register 0 using a "`ld.cf`" instruction.
3. Set the mode to 0x08 (unsigned division, 16 low-order bits output mode 0) or 0x09 (signed division, 16 low-order bits output mode 0).
4. Send the 32-bit divisor (C) to COPRO2 using a "`ld.ca`" instruction.
5. Read the one-half result (16 low-order bits = A[15:0]) of the operation result register 0 (quotient) and the flag status.
6. Set the mode to 0x13 (operation result read, 16 high-order bits output mode 0).
7. Read another one-half result (16 high-order bits = A[31:16]) of the operation result register 0 (quotient).
8. Set the mode to 0x23 (operation result read, 16 low-order bits output mode 1).
9. Read the one-half result (16 low-order bits = D[15:0]) of the operation result register 1 (remainder).
10. Set the mode to 0x33 (operation result read, 16 high-order bits output mode 1).
11. Read another one-half result (16 high-order bits = D[31:16]) of the operation result register 1 (remainder).

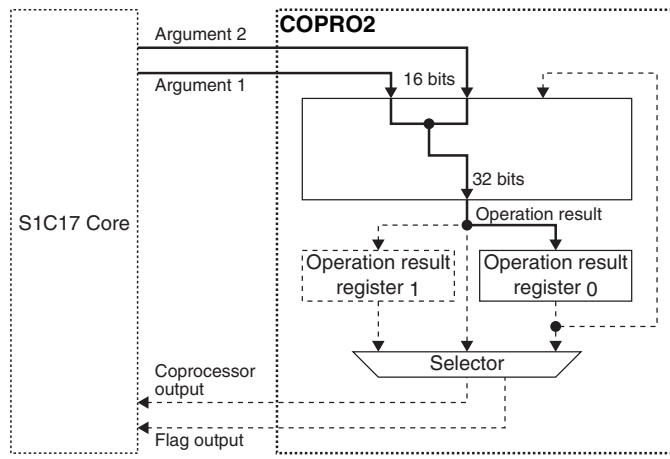


Figure 18.4.1 Data Path in Initialize Mode 2

Table 18.4.1 Initializing the Operation Result Register 0 (32 bits)

Mode setting value	Instruction	Operations	Remarks
0x02	`ld.cf %rd,%rs`	res0[31:16] ← %rd res0[15:0] ← %rs	
	(`ext` *imm9*) `ld.cf %rd,`*imm7*	res0[31:16] ← %rd res0[15:0] ← *imm7/16*	

res0: operation result register 0

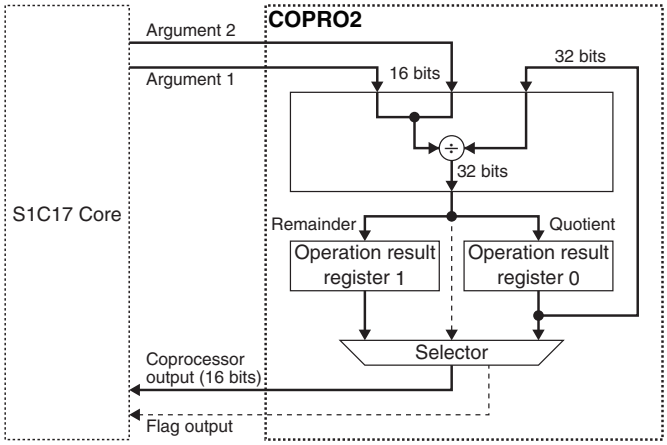


Figure 18.4.2 Data Path in Division Mode

Table 18.4.2 Operation in Division Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x08 or 0x09	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[15:0] (Quotient)	psr (CVZN) ← 0b0000	The operation result registers 0 and 1 keep the operation results until they are rewritten by other operation. COPRO2 does not support 0 ÷ 0 division.
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[15:0] (Quotient)		
0x18 or 0x19	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[31:16] (Quotient)		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res0[31:16] (Quotient)		
0x28 or 0x29	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[15:0] (Remainder)		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[15:0] (Remainder)		
0x38 or 0x39	`ld.ca %rd,%rs`	res0[31:0] ÷ {%rd, %rs} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[31:16] (Remainder)		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ÷ {%rd, *imm7/16*} res0[31:0] ← Quotient res1[31:0] ← Remainder %rd ← res1[31:16] (Remainder)		

res0: operation result register 0, res1: operation result register 1

Example:

```
ld.cw %r0,0x02 ; Sets the mode (initialize mode 2).
ld.cf %r0,%r1  ; Set the dividend {%r0, %r1} to the operation result register 0.
ld.cw %r0,0x08 ; Sets the mode (unsigned division mode and 16 low-order bits output mode 0).
ld.ca %r0,%r1  ; Performs "res0[31:0] (quotient), res1[31:0] (remainder) = res0[31:0] ÷ {%r0[15:0],
                 %r1[15:0]}" and loads the 16 low-order bits of the result (quotient) to %r0.
ld.ca %r1,%r0  ; Loads the 16 low-order bits of the result (quotient) to %r1.
ld.cw %r0,0x13 ; Sets the mode (operation result read mode and 16 high-order bits output mode 0).
ld.ca %r2,%r0  ; Loads the 16 high-order bits of the result (quotient) to %r2.
ld.cw %r0,0x23 ; Sets the mode (operation result read mode and 16 low-order bits output mode 1).
ld.ca %r3,%r0  ; Loads the 16 low-order bits of the result (remainder) to %r3.
ld.cw %r0,0x33 ; Sets the mode (operation result read mode and 16 high-order bits output mode 1).
ld.ca %r4,%r0  ; Loads the 16 high-order bits of the result (remainder) to %r4.
```

18.5 MAC

The MAC (multiplication and accumulation) function performs "A (32 bits) = B (16 bits) × C (16 bits) + A (32 bits)."
The following shows a procedure to perform a MAC operation:

1. Set the initial value (A) to the operation result register 0.
   - To clear the operation result registers (A = 0):
     Set the mode to 0x00 (initialize mode 0). (It is not necessary to send 0x00 to COPRO2 with another instruction.)
   - To load a 16-bit value to the operation result register 0:
     Set the operation mode to 0x01 (initialize mode 1) and then send the initial value (16 bits) to COPRO2 using a "`ld.cf`" instruction.
   - To load a 32-bit value to the operation result register 0:
     Set the operation mode to 0x02 (initialize mode 2) and then send the initial value (32 bits) to COPRO2 using a "`ld.cf`" instruction.
2. Set the mode to 0x06 (unsigned MAC, 16 low-order bits output mode 0) or 0x07 (signed MAC, 16 low-order bits output mode 0).
3. Repeat sending the 16-bit multiplicand (B) and 16-bit multiplier (C) to COPRO2 the number of times required using a "`ld.ca`" instruction.
4. Read the one-half result (16 low-order bits = A[15:0]) and the flag status.
5. Set the mode to 0x13 (operation result read, 16 high-order bits output mode).
6. Read another one-half result (16 high-order bits = A[31:16]).

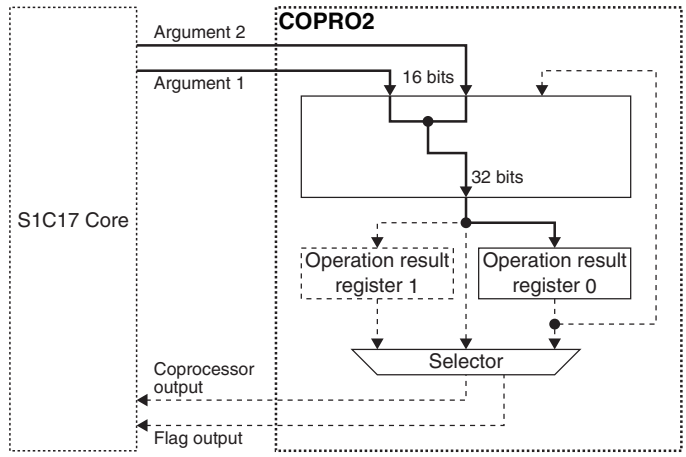


Figure 18.5.1 Data Path in Initialize Mode

Table 18.5.1 Initializing the Operation Result Register 0

Mode setting value	Instruction	Operations	Remarks
0x00	–	res0[31:0] ← 0x0 res1[31:0] ← 0x0	Setting the operating mode executes the initialization without sending data.
0x01	`ld.cf %rd,%rs`	res0[31:16] ← 0x0 res0[15:0] ← %rs	
	(`ext` *imm9*) `ld.cf %rd,`*imm7*	res0[31:16] ← 0x0 res0[15:0] ← *imm7/16*	
0x02	`ld.cf %rd,%rs`	res0[31:16] ← %rd res0[15:0] ← %rs	
	(`ext` *imm9*) `ld.cf %rd,`*imm7*	res0[31:16] ← %rd res0[15:0] ← *imm7/16*	

res0: operation result register 0, res1: operation result register 1

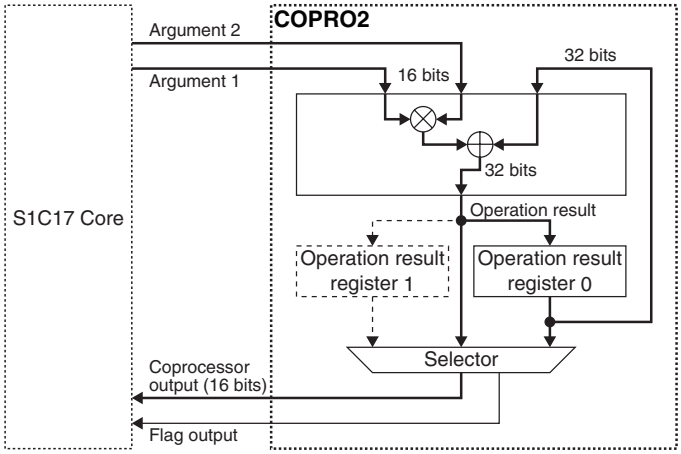


Figure 18.5.2 Data Path in MAC Mode

Table 18.5.2 Operation in MAC Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x06 or 0x07	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs + res0[31:0] %rd ← res0[15:0]	psr (CVZN) ← 0b0100 if an overflow has occurred Otherwise psr (CVZN) ← 0b0000	The operation result register 0 keeps the operation result until it is rewritten by other operation. Overflow can be detected only in signed MAC mode (it does not occur in unsigned MAC mode).
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* + res0[31:0] %rd ← res0[15:0]		
0x16 or 0x17	`ld.ca %rd,%rs`	res0[31:0] ← %rd × %rs + res0[31:0] %rd ← res0[31:16]		
	(`ext` *imm9*) `ld.ca %rd,`*imm7*	res0[31:0] ← %rd × *imm7/16* + res0[31:0] %rd ← res0[31:16]		

res0: operation result register 0

Example:

```
ld.cw %r0,0x00 ; Sets the mode (initialize mode 0) to clear the operation result register 0 to 0x0000.
ld.cw %r0,0x07 ; Sets the mode (signed MAC mode and 16 low-order bits output mode 0).
ld.ca %r0,%r1  ; Performs "res0[31:0] = %r0[15:0] × %r1[15:0] + res0[31:0]" and loads the 16 low-
                 order bits of the result to %r0.
ld.cw %r0,0x13 ; Sets the mode (operation result read mode and 16 high-order bits output mode 0).
ld.ca %r1,%r0  ; Loads the 16 high-order bits of the result to %r1.
```

Conditions to set the overflow (V) flag

An overflow occurs in a signed MAC operation and the overflow (V) flag is set to 1 when the signs of the multiplication result, operation result register value, and multiplication & accumulation result match the following conditions:

Table 18.5.3 Conditions to Set the Overflow (V) Flag

Mode setting value	Sign of multiplication result	Sign of operation result register value	Sign of multiplication & accumulation result
0x07	0 (positive)	0 (positive)	1 (negative)
0x07	1 (negative)	1 (negative)	0 (positive)

An overflow occurs when a MAC operation performs addition of positive values and a negative value results, or it performs addition of negative values and a positive value results. The coprocessor holds the operation result until the overflow (V) flag is cleared.

Conditions to clear the overflow (V) flag

The overflow (V) flag that has been set will be cleared when an overflow has not been occurred during execution of the "`ld.ca`" instruction for MAC operation or when the "`ld.ca`" or "`ld.cf`" instruction is executed in an operation mode other than operation result read mode.

18.6 Reading Operation Results

The "`ld.ca`" instruction cannot load a 32-bit operation result to a CPU register, so a multiplication, division or MAC operation returns the one-half (16 bits according to the output mode) result (A[15:0] or A[31:16]) and the flag status to the CPU registers. Another one-half should be read by setting COPRO2 into operation result read mode. The operation result register keeps the loaded operation result until it is rewritten by other operation.

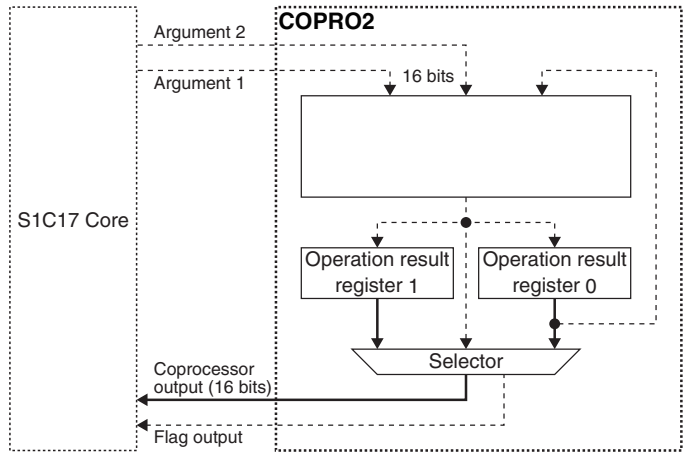


Figure 18.6.1 Data Path in Operation Result Read Mode

Table 18.6.1 Operation in Operation Result Read Mode

Mode setting value	Instruction	Operations	Flags	Remarks
0x03	`ld.ca %rd,%rs`	%rd ← res[15:0]	psr (CVZN) ← 0b0000	This operation mode does not affect the operation result registers 0 and 1.
	`ld.ca %rd,`*`imm7`*	%rd ← res[15:0]		
0x13	`ld.ca %rd,%rs`	%rd ← res[31:16]		
	`ld.ca %rd,`*`imm7`*	%rd ← res[31:16]		
0x23	`ld.ca %rd,%rs`	%rd ← res1[15:0]		
	`ld.ca %rd,`*`imm7`*	%rd ← res1[15:0]		
0x33	`ld.ca %rd,%rs`	%rd ← res1[31:16]		
	`ld.ca %rd,`*`imm7`*	%rd ← res1[31:16]		

res0: operation result register 0, res1: operation result register 1

19 Electrical Characteristics

19.1 Absolute Maximum Ratings

(V_{SS} = 0 V)

Item	Symbol	Condition		Rated value	Unit
Power supply voltage	V_{DD}			-0.3 to 7.0	V
Analog power supply voltage	AV_{DD}			-0.3 to 7.0	V
Flash programming voltage	V_{PP}			-0.3 to 8.0	V
Input voltage	V_I	P00–07, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4, #RESET		-0.3 to V_{DD} + 0.5	V
		P10–17, P20–27		-0.3 to AV_{DD} + 0.5	V
		EXSVD		-0.3 to 5.5	V
Output voltage	V_O	P00–07, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D4		-0.3 to V_{DD} + 0.5	V
		P10–17, P20–27		-0.3 to AV_{DD} + 0.5	V
High level output current	I_{OH}	1 pin	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D4	-10	mA
		Total of all pins		-20	mA
Low level output current	I_{OL}	1 pin	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D4	10	mA
		Total of all pins		20	mA
Operating temperature	Ta			-40 to 85	°C
Storage temperature	Tstg			-65 to 125	°C

19.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}		1.8	–	5.5	V
Analog power supply voltage	AV_{DD}		1.8	–	5.5	V
Flash programming voltage	V_{PP}		7.3	7.5	7.7	V
OSC1 oscillator oscillation frequency	f_{OSC1}	Crystal oscillator	–	32.768	–	kHz
OSC3 oscillator oscillation frequency	f_{OSC3}	Crystal/ceramic oscillator	0.2	–	16.8	MHz
EXOSC external clock frequency	f_{EXOSC}	When supplied from an external oscillator	0.016	–	16.8	MHz
Bypass capacitor between V_{SS} and V_{DD}	C_{PW1}		–	3.3	–	µF
Bypass capacitor between V_{SS} and AV_{DD}	C_{PW2}		–	3.3	–	µF
Capacitors between V_{SS} and V_{D1}	C_{PW3}		–	1	–	µF
Gate capacitor for OSC1 oscillator	C_{G1}	*1	0	–	25	pF
Drain capacitor for OSC1 oscillator	C_{D1}	*1	–	0	–	pF
Gate capacitor for OSC3 oscillator	C_{G3}	*1	0	–	100	pF
Drain capacitor for OSC3 oscillator	C_{D3}	*1	0	–	100	pF
DSIO pull-up resistor	R_{DBG}	*2	–	10	–	kΩ
Capacitor between V_{SS} and V_{PP}	C_{VPP}		–	0.1	–	µF

*1 The component values should be determined after performing matching evaluation of the resonator mounted on the printed circuit board actually used.

*2 R_{DBG} is not required when using the DSIO pin as a general-purpose I/O port.

19.3 Current Consumption

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25 °C, EXOSC = OFF, PWGVD1CTL.REGMOD[1:0] bits = 0x0 (automatic mode), FLASHCWAIT.RDWAIT[1:0] bits = 0x1 (2 cycles)

Item	Symbol	Condition	V_{DD}	Ta	Min.	Typ.	Max.	Unit
Current consumption in SLEEP mode	I_{SLP}	IOSC = OFF, OSC1 = OFF, OSC3 = OFF	3.6 V	25 °C	–	0.20	0.8	µA
				85 °C	–	1.5	14	µA
			5.5 V	25 °C	–	0.30	1.2	µA
				85 °C	–	2.0	19	µA
Current consumption in HALT mode	I_{HALT1}	IOSC = 8 MHz, OSC1 = 32 kHz*1, OSC3 = OFF			–	300	400	µA
	I_{HALT2}	IOSC = OFF, OSC1 = 32 kHz*1, OSC3 = OFF	3.6 V	25 °C	–	0.6	1.5	µA
			5.5 V		–	0.7	1.9	µA
	I_{HALT3}	IOSC = OFF, OSC1 = 32 kHz*1, OSC3 = 1 MHz (ceramic oscillator)*2			–	40	55	µA

Item	Symbol	Condition	V_{DD}	Ta	Min.	Typ.	Max.	Unit
Current consumption in RUN mode	I_{RUN10}*3	IOSC = 8 MHz, OSC1 = 32 kHz*1, OSC3 = OFF, SYSCLK = IOSC			–	2,300	2,800	µA
		IOSC = 8 MHz, OSC1 = 32 kHz*1, OSC3 = OFF, SYSCLK = IOSC, FLASHCWAIT.RDWAIT[1:0] bits = 0x2 (3 cycles)			–	2,100	2,500	µA
	I_{RUN20}*3	IOSC = OFF, OSC1 = 32 kHz*1, OSC3 = OFF, SYSCLK = OSC1			–	9	13	µA
		IOSC = OFF, OSC1 = 32 kHz*1, OSC3 = OFF, SYSCLK = OSC1 PWGVD1CTL.REGMOD[1:0] bits = 0x2 (normal mode)			–	20	28	µA
	I_{RUN30}*3	IOSC = OFF, OSC1 = 32 kHz*1, OSC3 = 1 MHz (ceramic oscillator)*2, SYSCLK = OSC3			–	280	350	µA
	I_{RUN11}*4	IOSC = 8 MHz, OSC1 = 32 kHz*1, SYSCLK = IOSC, running in the RAM			–	1,800	2,300	µA
	I_{RUN21}*4	IOSC = OFF, OSC1 = 32 kHz*1, SYSCLK = OSC1, running in the RAM			–	6	10	µA
	I_{RUN31}*4	IOSC = OFF, OSC1 = 32 kHz*1, OSC3 = 1 MHz (ceramic oscillator)*2, SYSCLK = OSC3, running in the RAM			–	220	280	µA

*1 OSC1 oscillator: CLGOSC1.INV1N[1:0] bits = 0x0, CLGOSC1.CGI1[2:0] bits = 0x0, CLGOSC1.OSDEN bit = 0, C_{G1} = C_{D1} = 0 pF, Crystal resonator = C-002RX (manufactured by Seiko Epson Corporation, R_1 = 50 kΩ (Max.), C_L = 7 pF)

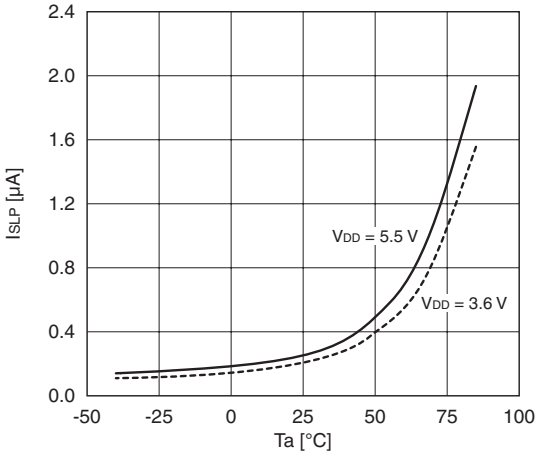
*2 OSC3 oscillator: CLGOSC3.OSC3INV[1:0] bits = 0x0, C_{G3} = C_{D3} = 100 pF, ceramic resonator = CSBLA_J (manufactured by Murata Manufacturing Co., Ltd., 1 MHz)

*3 The current consumption values were measured when a test program consisting of 60.5 % ALU instructions, 17 % branch instructions, 12 % RAM read instructions, and 10.5 % RAM write instructions was executed continuously in the Flash memory.

*4 The current consumption values were measured when a test program consisting of 60.5 % ALU instructions, 17 % branch instructions, 12 % RAM read instructions, and 10.5 % RAM write instructions was executed continuously in the RAM.

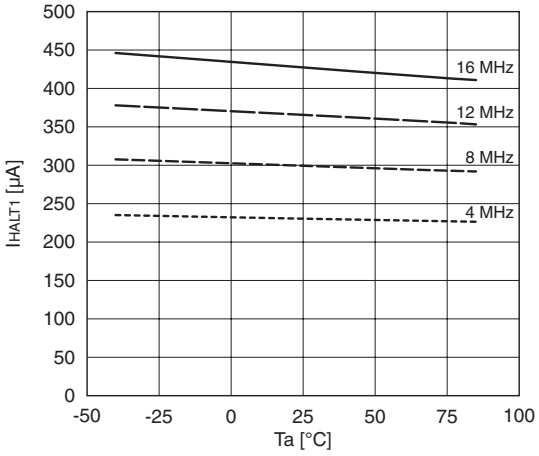
Current consumption-temperature characteristic in SLEEP mode

IOSC = OFF, OSC1 = OFF, OSC3 = OFF, Typ. value



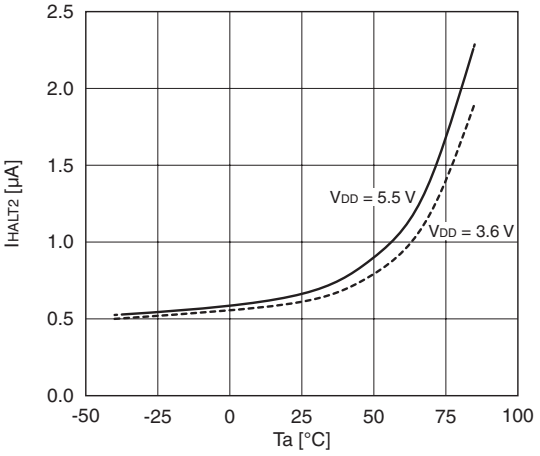
Current consumption-temperature characteristic in HALT mode (IOSC operation)

IOSC = ON, OSC1 = 32 kHz, OSC3 = OFF, Typ. value



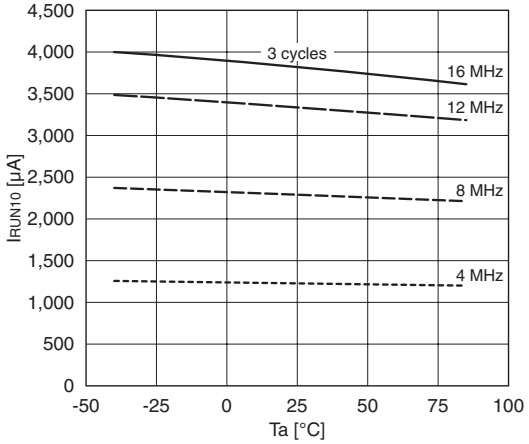
Current consumption-temperature characteristic in HALT mode (OSC1 operation)

IOSC = OFF, OSC1 = 32 kHz, OSC3 = OFF, Typ. value



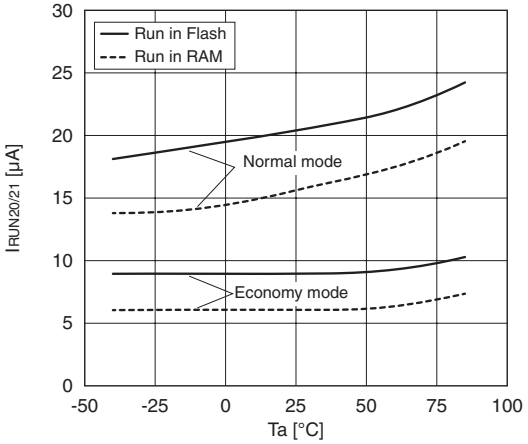
Current consumption-temperature characteristic in RUN mode (IOSC operation)

IOSC = ON, OSC1 = 32 kHz, OSC3 = OFF, Typ. value



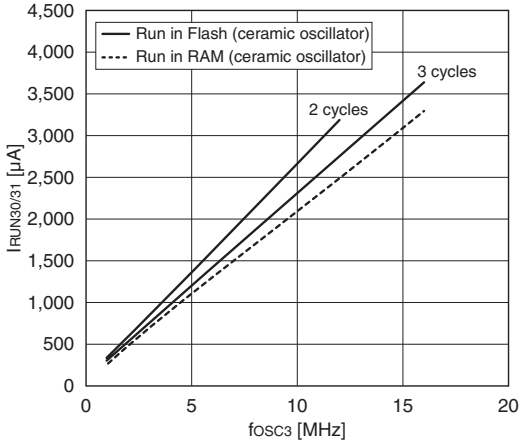
Current consumption-temperature characteristic in RUN mode (OSC1 operation)

IOSC = OFF, OSC1 = 32 kHz, OSC3 = OFF, Typ. value



Current consumption-frequency characteristic in RUN mode (OSC3 operation)

IOSC = OFF, OSC1 = 32 kHz, OSC3 = ON, Ta = 25 °C, Typ. value,
CLGOSC3.OSC3INV[1:0] bits = 0x3

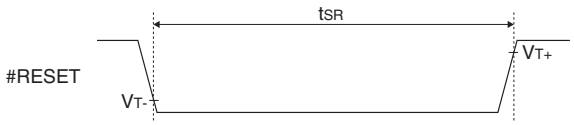


19.4 System Reset Controller (SRC) Characteristics

#RESET pin characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

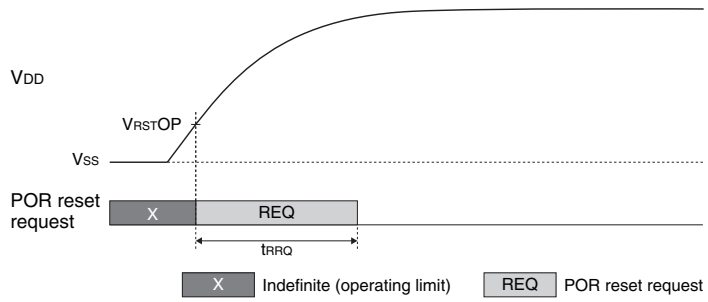
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level Schmitt input threshold voltage	V_{T+}		0.5 × V_{DD}	–	0.8 × V_{DD}	V
Low level Schmitt input threshold voltage	V_{T-}		0.2 × V_{DD}	–	0.5 × V_{DD}	V
Schmitt input hysteresis voltage	ΔV_T		180	–	–	mV
Input pull-up resistance	R_{IN}		100	270	500	kΩ
Pin capacitance	C_{IN}		–	–	15	pF
Reset Low pulse width	t_{SR}		5	–	–	µs



POR characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
POR operating limit voltage	V_{RSTOP}		–	0.5	0.95	V
POR reset request hold time	t_{RRQ}		0.01	–	4	ms



Note: When performing a power-on-reset again after the power is turned off, decrease the V_{DD} voltage to $V_{RST}OP$ or less.

Reset hold circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time*1	t_{RSTR}		–	–	200	µs

*1 Time until the internal reset signal is negated after the reset request is canceled.

19.5 Clock Generator (CLG) Characteristics

Oscillator circuit characteristics including resonators change depending on conditions (board pattern, components used, etc.). Use these characteristic values as a reference and perform matching evaluation using the actual printed circuit board.

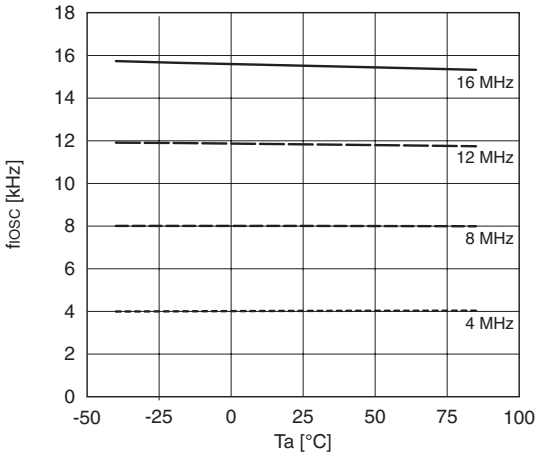
IOSC oscillator circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Ta	Min.	Typ.	Max.	Unit
Oscillation start time	t_{stal}			–	–	3	µs
Oscillation frequency	f_{IOSC}	CLGIOSC.IOSCFQ[1:0] bits = 0x3	25 °C	15.2	16.0	16.8	MHz
			-40 to 85 °C	14.9	16.0	17.1	MHz
		CLGIOSC.IOSCFQ[1:0] bits = 0x2	25 °C	11.4	12.0	12.6	MHz
			-40 to 85 °C	11.2	12.0	12.8	MHz
		CLGIOSC.IOSCFQ[1:0] bits = 0x1	25 °C	7.8	8.0	8.2	MHz
			-40 to 85 °C	7.6	8.0	8.4	MHz
		CLGIOSC.IOSCFQ[1:0] bits = 0x0	25 °C	3.8	4.0	4.2	MHz
			-40 to 85 °C	3.7	4.0	4.3	MHz

IOSC oscillation frequency-temperature characteristic

Typ. value



OSC1 oscillator circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time*1	t_{sta1}	CLGOSC1.INV1N[1:0] bits = 0x1, CLGOSC1.INV1B[1:0] bits = 0x2, CLGOSC1.OSC1BUP bit = 1	–	–	3	s
Internal gate capacitance	C_{GI1}	CLGOSC1.CGI1[2:0] bits = 0x0	–	12	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x1	–	14	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x2	–	16	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x3	–	18	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x4	–	19	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x5	–	21	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x6	–	23	–	pF
		CLGOSC1.CGI1[2:0] bits = 0x7	–	24	–	pF
Internal drain capacitance	C_{DI1}		–	6	–	pF
Oscillator circuit current - oscillation inverter drivability ratio *1	I_{OSC1}	CLGOSC1.INV1N/INV1B[1:0] bits = 0x0	–	70	–	%
		CLGOSC1.INV1N/INV1B[1:0] bits = 0x1 (reference)	–	100	–	%
		CLGOSC1.INV1N/INV1B[1:0] bits = 0x2	–	130	–	%
		CLGOSC1.INV1N/INV1B[1:0] bits = 0x3	–	300	–	%
Oscillation stop detector current	I_{OSD1}	CLGOSC1.OSDEN bit = 1	–	0.025	0.1	µA

*1 Crystal resonator = C-002RX (manufactured by Seiko Epson Corporation, R_1 = 50 kΩ (Max.), C_L = 7 pF)

OSC3 oscillator circuit characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25 °C

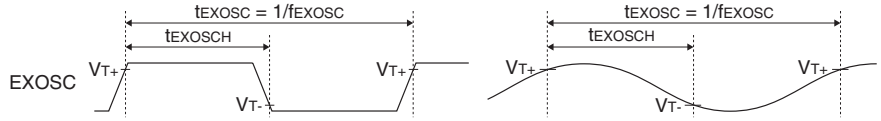
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta3}	Crystal resonator*1, CLGOSC3.OSC3INV[1:0] bits = 0x3	–	–	20	ms
		Ceramic resonator*2, CLGOSC3.OSC3INV[1:0] bits = 0x3	–	–	1	ms
Internal gate capacitance	C_{GI3}		–	8	–	pF
Internal drain capacitance	C_{DI3}		–	8	–	pF
Oscillator circuit current - oscillation inverter drivability ratio*2	I_{OSC3C}	CLGOSC3.OSC3INV[1:0] bits = 0x0	–	20	–	%
		CLGOSC3.OSC3INV[1:0] bits = 0x1	–	40	–	%
		CLGOSC3.OSC3INV[1:0] bits = 0x2	–	55	–	%
		CLGOSC3.OSC3INV[1:0] bits = 0x3 (reference)	–	100	–	%

*1 OSC3 oscillator: C_{G1} = C_{D1} = 10 pF, Crystal resonator = CA-301 (manufactured by Seiko Epson Corporation, 4 MHz)
*2 OSC3 oscillator: C_{G3} = C_{D3} = 100 pF, ceramic resonator = CSBLA_J (manufactured by Murata Manufacturing Co., Ltd., 1 MHz)

EXOSC external clock input characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXOSC external clock duty ratio	t_{EXOSCD}	t_{EXOSCD} = t_{EXOSCH}/t_{EXOSC}	46	–	54	%
High level Schmitt input threshold voltage	V_{T+}		0.5 × V_{DD}	–	0.8 × V_{DD}	V
Low level Schmitt input threshold voltage	V_{T-}		0.2 × V_{DD}	–	0.5 × V_{DD}	V
Schmitt input hysteresis voltage	ΔV_T		180	–	–	mV



19.6 Flash Memory Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

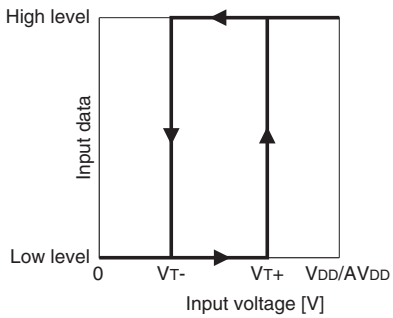
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Programming count *1	C_{FEP}	Programmed data is guaranteed to be retained for 10 years.	50	–	–	times

*1 Assumed that Erasing + Programming as count of 1. The count includes programming in the factory for shipment with ROM data programmed.

19.7 Input/Output Port (PPORT) Characteristics

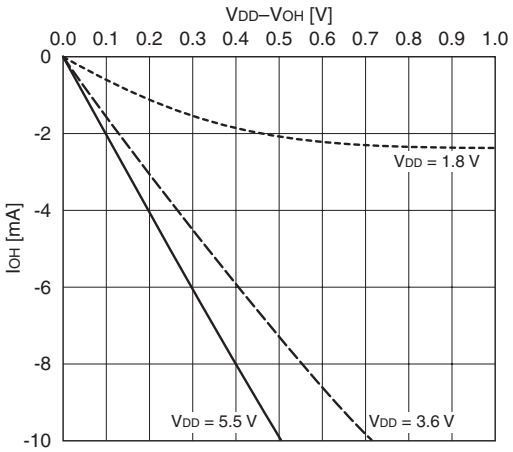
Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level Schmitt input threshold voltage	V_{T+}	P00–07, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4	0.5 × V_{DD}	–	0.8 × V_{DD}	V
		P10–17, P20–27	0.5 × AV_{DD}	–	0.8 × AV_{DD}	V
Low level Schmitt input threshold voltage	V_{T-}	P00–07, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4	0.2 × V_{DD}	–	0.5 × V_{DD}	V
		P10–17, P20–27	0.2 × AV_{DD}	–	0.5 × AV_{DD}	V
Schmitt input hysteresis voltage	ΔV_T	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4	180	–	–	mV
High level output current	I_{OH}	P00–07, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D4, V_{OH} = 0.9 × V_{DD}	–	–	-0.5	mA
		P10–17, P20–27, V_{OH} = 0.9 × AV_{DD}	–	–	-0.5	mA
Low level output current	I_{OL}	P00–07, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D4, V_{OL} = 0.1 × V_{DD}	0.5	–	–	mA
		P10–17, P20–27, V_{OL} = 0.1 × AV_{DD}	0.5	–	–	mA
Leakage current	I_{LEAK}	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D4	-150	–	150	nA
Input pull-up resistance	R_{INU}	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4	75	150	300	kΩ
Input pull-down resistance	R_{IND}	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4	75	150	300	kΩ
Pin capacitance	C_{IN}	P00–07, P10–17, P20–27, P30–37, P40–47, P50–55, P60–67, P70–77, P80–87, P90–96, PA0–A5, PD0–D1, PD3–D4	–	–	15	pF



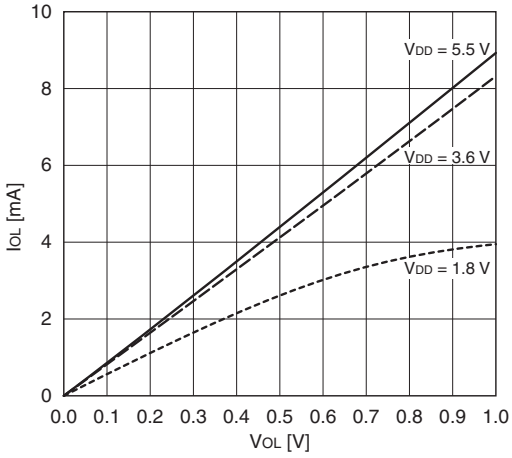
High-level output current characteristic

Ta = 85 °C, Max. value



Low-level output current characteristic

Ta = 85 °C, Min. value

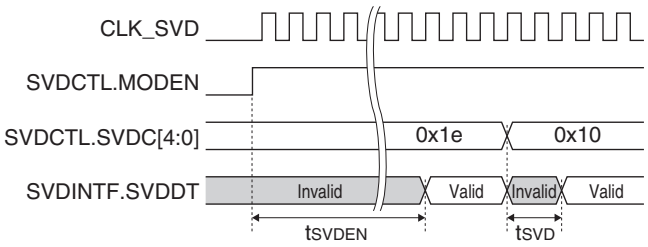


19.8 Supply Voltage Detector (SVD) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

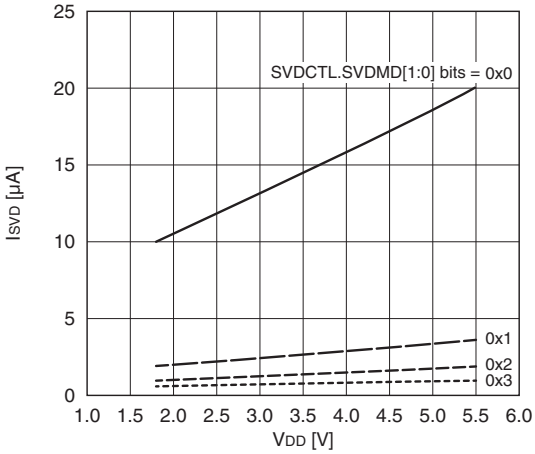
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXSVD pin input voltage range	V_{EXSVD}		1.76	–	5.50	V
EXSVD input impedance	R_{EXSVD}	SVDCTL.SVDC[4:0] bits = 0x0c	309	442	575	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0d	327	467	607	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0e	344	492	640	kΩ
		SVDCTL.SVDC[4:0] bits = 0x0f	362	517	672	kΩ
		SVDCTL.SVDC[4:0] bits = 0x10	379	542	705	kΩ
		SVDCTL.SVDC[4:0] bits = 0x11	397	567	737	kΩ
		SVDCTL.SVDC[4:0] bits = 0x12	414	592	770	kΩ
		SVDCTL.SVDC[4:0] bits = 0x13	432	617	802	kΩ
		SVDCTL.SVDC[4:0] bits = 0x14	449	642	835	kΩ
		SVDCTL.SVDC[4:0] bits = 0x15	467	667	867	kΩ
		SVDCTL.SVDC[4:0] bits = 0x16	484	692	900	kΩ
		SVDCTL.SVDC[4:0] bits = 0x17	502	717	932	kΩ
		SVDCTL.SVDC[4:0] bits = 0x18	519	742	965	kΩ
		SVDCTL.SVDC[4:0] bits = 0x19	537	767	997	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1a	554	792	1,030	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1b	572	817	1,062	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1c	589	842	1,095	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1d	607	867	1,127	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1e	624	892	1,160	kΩ
		SVDCTL.SVDC[4:0] bits = 0x1f	642	917	1,192	kΩ
SVD detection voltage	V_{SVD}	SVDCTL.SVDC[4:0] bits = 0x0c	1.76	1.80	1.85	V
		SVDCTL.SVDC[4:0] bits = 0x0d	1.85	1.90	1.95	V
		SVDCTL.SVDC[4:0] bits = 0x0e	1.95	2.00	2.05	V
		SVDCTL.SVDC[4:0] bits = 0x0f	2.05	2.10	2.15	V
		SVDCTL.SVDC[4:0] bits = 0x10	2.15	2.20	2.26	V
		SVDCTL.SVDC[4:0] bits = 0x11	2.24	2.30	2.36	V
		SVDCTL.SVDC[4:0] bits = 0x12	2.34	2.40	2.46	V
		SVDCTL.SVDC[4:0] bits = 0x13	2.44	2.50	2.56	V
		SVDCTL.SVDC[4:0] bits = 0x14	2.54	2.60	2.67	V
		SVDCTL.SVDC[4:0] bits = 0x15	2.63	2.70	2.77	V
		SVDCTL.SVDC[4:0] bits = 0x16	2.73	2.80	2.87	V
		SVDCTL.SVDC[4:0] bits = 0x17	2.83	2.90	2.97	V
		SVDCTL.SVDC[4:0] bits = 0x18	2.93	3.00	3.08	V
		SVDCTL.SVDC[4:0] bits = 0x19	3.02	3.10	3.18	V
		SVDCTL.SVDC[4:0] bits = 0x1a	3.12	3.20	3.28	V
		SVDCTL.SVDC[4:0] bits = 0x1b	3.22	3.30	3.38	V
		SVDCTL.SVDC[4:0] bits = 0x1c	3.32	3.40	3.49	V
		SVDCTL.SVDC[4:0] bits = 0x1d	3.41	3.50	3.59	V
		SVDCTL.SVDC[4:0] bits = 0x1e	3.51	3.60	3.69	V
		SVDCTL.SVDC[4:0] bits = 0x1f	3.61	3.70	3.79	V
SVD circuit enable response time	t_{SVDEN}	*1	–	–	500	µs
SVD circuit response time	t_{SVD}		–	–	60	µs
SVD circuit current	I_{SVD}	SVDCTL.SVDMD[1:0] bits = 0x0, SVDCTL.SVDC[4:0] bits = 0x0c CLK_SVD = 32 kHz, Ta = 25 °C	–	20	32	µA
		SVDCTL.SVDMD[1:0] bits = 0x1, SVDCTL.SVDC[4:0] bits = 0x0c, CLK_SVD = 32 kHz, Ta = 25 °C	–	3.6	5.5	µA
		SVDCTL.SVDMD[1:0] bits = 0x2, SVDCTL.SVDC[4:0] bits = 0x0c, CLK_SVD = 32 kHz, Ta = 25 °C	–	1.8	2.8	µA
		SVDCTL.SVDMD[1:0] bits = 0x3, SVDCTL.SVDC[4:0] bits = 0x0c, CLK_SVD = 32 kHz, Ta = 25 °C	–	1	1.5	µA

*1 If CLK_SVD is configured in the neighborhood of 32 kHz, the SVDINTF.SVDDT bit is masked during the t_{SVDEN} period and it retains the previous value.



SVD circuit current - power supply voltage characteristic

Ta = 25 °C, SVDCTL.SVDC[4:0] bits = 0x0c, CLK_SVD = 32 kHz, Typ. value



19.9 UART (UART) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer baud rate	U_{BRT1}	Normal mode	150	–	460,800	bps
	U_{BRT2}	IrDA mode	150	–	115,200	bps

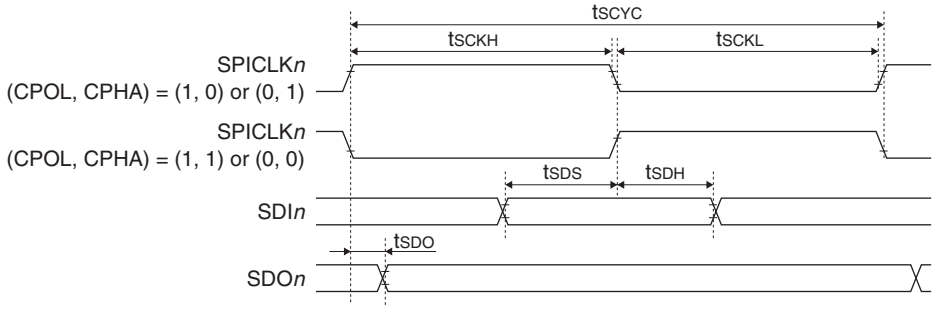
19.10 Synchronous Serial Interface (SPIA) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

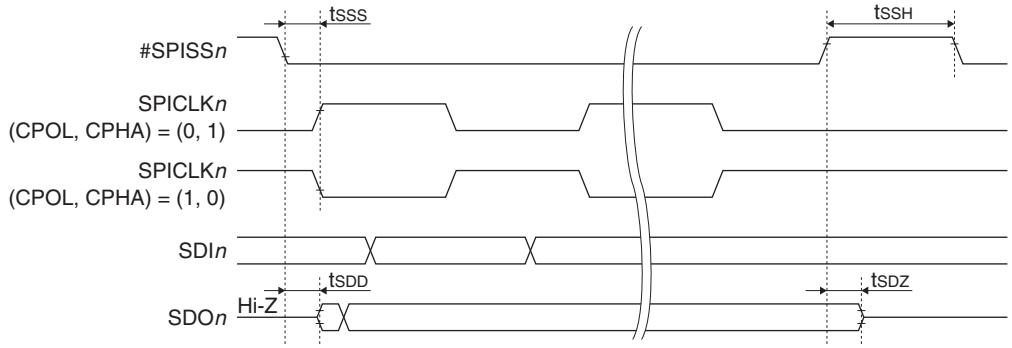
Item	Symbol	Condition	V_{DD}	Min.	Typ.	Max.	Unit
SPICLK*n* cycle time	t_{SCYC}		4.5 to 5.5 V	250	–	–	ns
			1.8 to 4.5 V	500	–	–	ns
SPICLK*n* High pulse width	t_{SCKH}		4.5 to 5.5 V	100	–	–	ns
			1.8 to 4.5 V	200	–	–	ns
SPICLK*n* Low pulse width	t_{SCKL}		4.5 to 5.5 V	100	–	–	ns
			1.8 to 4.5 V	200	–	–	ns
SDI*n* setup time	t_{SDS}		4.5 to 5.5 V	50	–	–	ns
			1.8 to 4.5 V	80	–	–	ns
SDI*n* hold time	t_{SDH}		4.5 to 5.5 V	20	–	–	ns
			1.8 to 4.5 V	30	–	–	ns
SDO*n* output delay time	t_{SDO}	C_L = 30 pF *1	4.5 to 5.5 V	–	–	60	ns
			1.8 to 4.5 V	–	–	90	ns
#SPISS*n* setup time	t_{SSS}			80	–	–	ns
#SPISS*n* High pulse width	t_{SSH}			100	–	–	ns
SDO*n* output start time	t_{SDD}	C_L = 30 pF *1		–	–	90	ns
SDO*n* output stop time	t_{SDZ}	C_L = 30 pF *1		–	–	80	ns

*1 C_L = Pin load

Master and slave modes



Slave mode

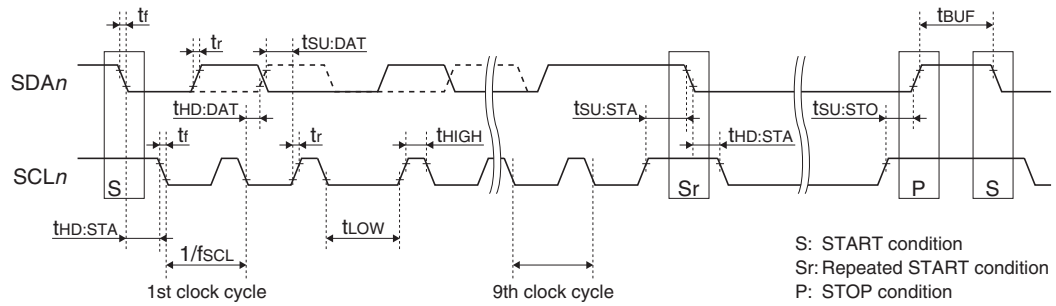


19.11 I²C (I2C) Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Item	Symbol	Condition	Standard mode			Fast mode			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL*n* frequency	f_{SCL}		0	–	100	0	–	400	kHz
Hold time (repeated) START condition *	$t_{HD:STA}$		4.0	–	–	0.6	–	–	µs
SCL*n* Low pulse width	t_{LOW}		4.7	–	–	1.3	–	–	µs
SCL*n* High pulse width	t_{HIGH}		4.0	–	–	0.6	–	–	µs
Repeated START condition setup time	$t_{SU:STA}$		4.7	–	–	0.6	–	–	µs
Data hold time	$t_{HD:DAT}$		0	–	–	0	–	–	µs
Data setup time	$t_{SU:DAT}$		250	–	–	100	–	–	ns
SDA*n*, SCL*n* rise time	t_r		–	–	1,000	–	–	300	ns
SDA*n*, SCL*n* fall time	t_f		–	–	300	–	–	300	ns
STOP condition setup time	$t_{SU:STO}$		4.0	–	–	0.6	–	–	µs
Bus free time	t_{BUF}		4.7	–	–	1.3	–	–	µs

* After this period, the first clock pulse is generated.



19.12 10-bit A/D Converter (ADC10A) Characteristics

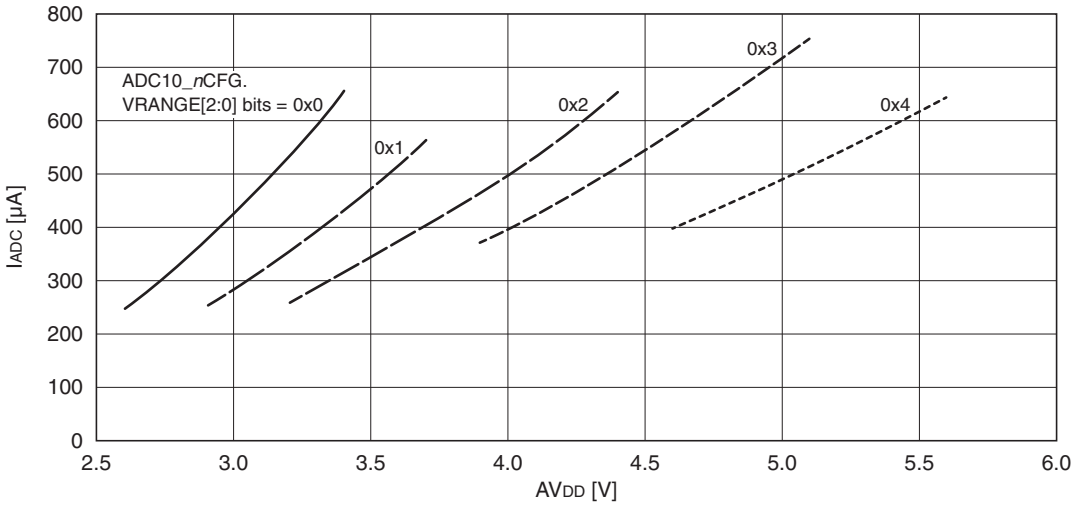
Unless otherwise specified: AV_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C, ADC10_*n*TRG.SMPCLK[2:0] bits = 0x5 (9 clocks)

Item	Symbol	Condition	AV_{DD}	Min.	Typ.	Max.	Unit
A/D conversion clock frequency	f_{CLK_ADC10A}			10	–	2,200	kHz
Sampling rate*1	f_{SMP}			–	–	100	ksps
Integral nonlinearity*2	INL			–	–	±1.5	LSB
Differential nonlinearity	DNL			–	–	±1	LSB
Zero-scale error	ZSE		2.7 to 3.6 V	–	–	±3	LSB
			3.6 to 5.5 V	–	–	±5	LSB
Full-scale error	FSE		2.7 to 3.6 V	–	–	±3	LSB
			3.6 to 5.5 V	–	–	±5	LSB
Analog input resistance	R_{ADIN}			–	12	20	kΩ
Analog input capacitance	C_{ADIN}			–	16	18	pF
A/D converter circuit current	I_{ADC}	ADC10_*n*CFG.VRANGE[2:0] bits = 0x0, ADIN = AV_{DD}/2, f_{SMP} = 100 ksps, Ta = 25 °C	2.7 to 3.3 V	–	600	1,000	µA
		ADC10_*n*CFG.VRANGE[2:0] bits = 0x1, ADIN = AV_{DD}/2, f_{SMP} = 100 ksps, Ta = 25 °C	3.0 to 3.6 V	–	520	900	µA
		ADC10_*n*CFG.VRANGE[2:0] bits = 0x2, ADIN = AV_{DD}/2, f_{SMP} = 100 ksps, Ta = 25 °C	3.3 to 4.3 V	–	620	1,000	µA
		ADC10_*n*CFG.VRANGE[2:0] bits = 0x3, ADIN = AV_{DD}/2, f_{SMP} = 100 ksps, Ta = 25 °C	4.0 to 5.0 V	–	720	1,200	µA
		ADC10_*n*CFG.VRANGE[2:0] bits = 0x4, ADIN = AV_{DD}/2, f_{SMP} = 100 ksps, Ta = 25 °C	4.7 to 5.5 V	–	620	1,000	µA

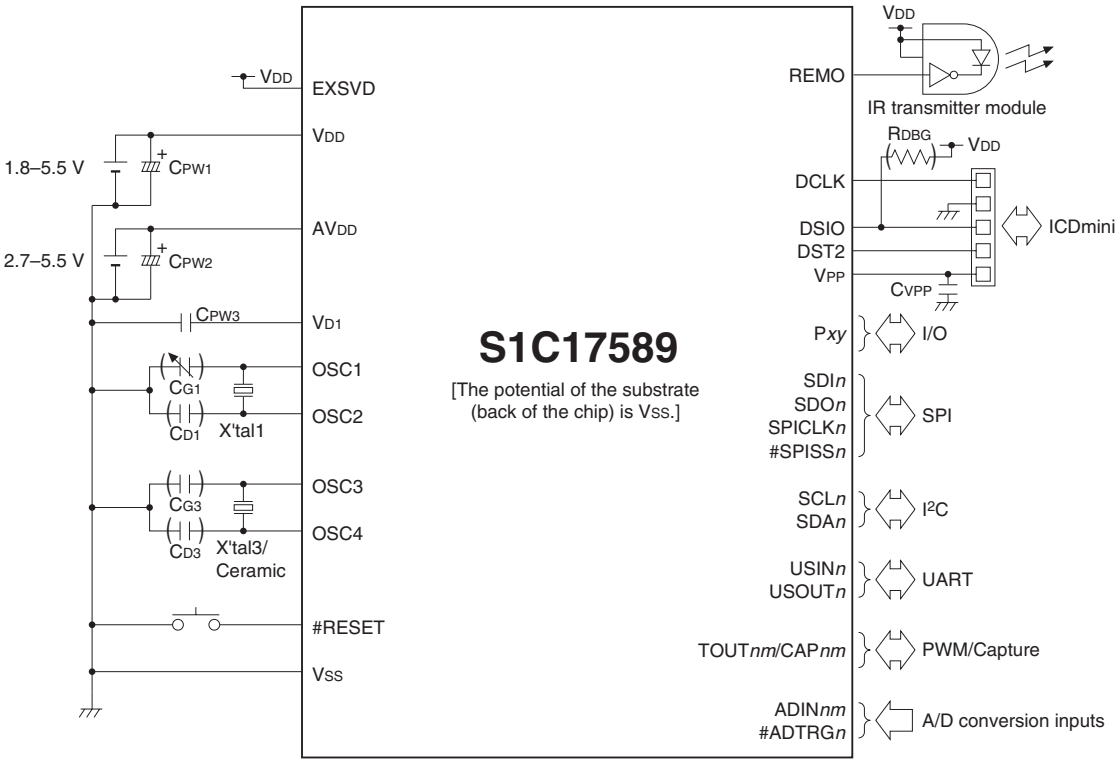
*1 The Max. value is the value when the A/D converter clock frequency f_{CLK_ADC10A} = 2,000 kHz.
*2 Integral nonlinearity error is measured at the end point line.

A/D converter current consumption-power supply voltage characteristic

ADIN = AV_{DD}/2, f_{SMP} = 100 ksps, Ta = 25 °C, Typ. value



20 Basic External Connection Diagram



( ): Do not mount components if unnecessary.

Sample external components

Symbol	Name	Recommended components
X'tal1	32 kHz crystal resonator	C-002RX (R_1 = 50 kΩ (Max.), C_L = 7 pF) manufactured by Seiko Epson Corporation
C_{G1}	OSC1 gate capacitor	Trimmer capacitor or ceramic capacitor
C_{D1}	OSC1 drain capacitor	Ceramic capacitor
X'tal3	Crystal resonator	CA-301 (4 MHz) manufactured by Seiko Epson Corporation
Ceramic	Ceramic resonator	CSBLA_J (1 MHz) manufactured by Murata Manufacturing Co., Ltd.
C_{G3}	OSC3 gate capacitor	Ceramic capacitor
C_{D3}	OSC3 drain capacitor	Ceramic capacitor
R_{CR3}	OSC3 oscillating resistor	Thick film chip resistor
C_{PW1}	Bypass capacitor between V_{SS} and V_{DD}	Ceramic capacitor or electrolytic capacitor
C_{PW2}	Bypass capacitor between V_{SS} and AV_{DD}	Ceramic capacitor or electrolytic capacitor
C_{PW3}	Capacitors between V_{SS} and V_{D1}	Ceramic capacitor
R_{DBG}	DSIO pull-up resistor	Thick film chip resistor
C_{VPP}	Capacitor between V_{SS} and V_{PP}	Ceramic capacitor

* For recommended component values, refer to “Recommended Operating Conditions” in the “Electrical Characteristics” chapter.

21 Package

QFP15-100PIN (P-LQFP100-1414-0.50)

(Unit: mm)

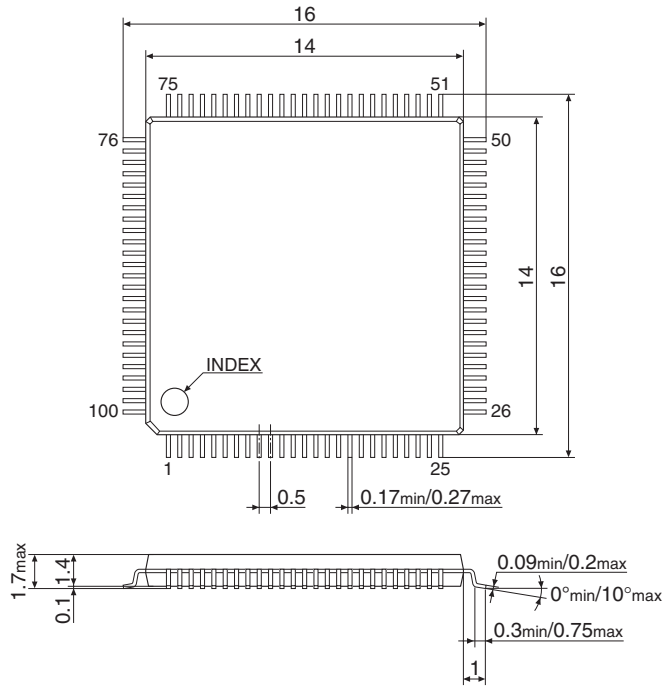


Figure 21.1 QFP15-100PIN Package Dimensions

QFP14-80PIN (P-LQFP080-1212-0.50)

(Unit: mm)

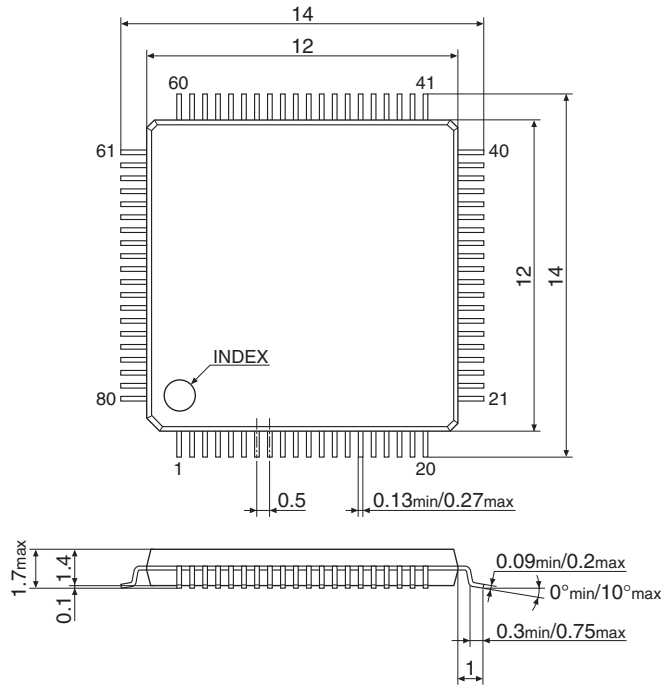


Figure 21.2 QFP14-80PIN Package Dimensions

QFP13-64PIN (P-LQFP064-1010-0.50)

(Unit: mm)

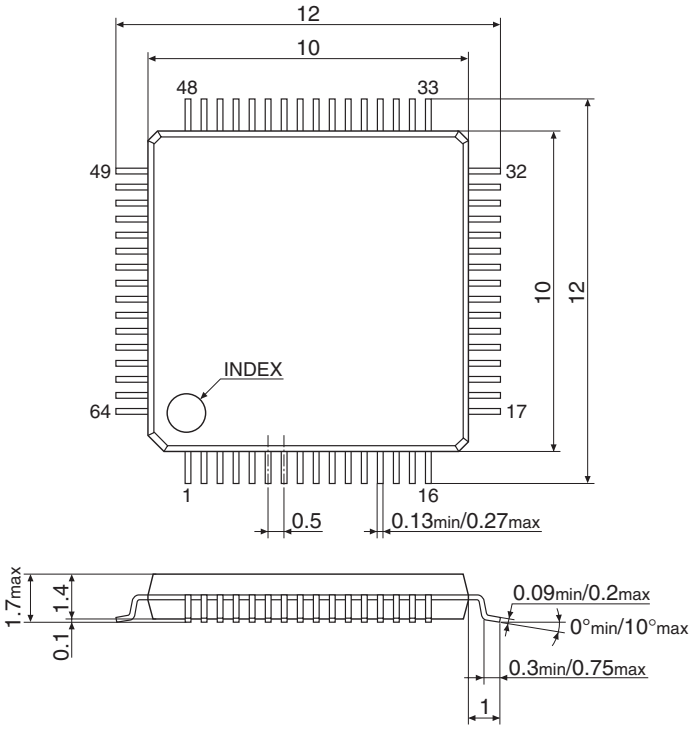


Figure 21.3 QFP13-64PIN Package Dimensions

Appendix A List of Peripheral Circuit Control Registers

0x4000–0x4008 Misc Registers (MISC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4000	MSCPROT (MISC System Protect Register)	15–0	PROT[15:0]	0x0000	H0	R/W	–
0x4002	MSCIRAMSZ (MISC IRAM Size Register)	15–9	–	0x00	–	R	–
		8	(reserved)	0	H0	R/WP	Always set to 0.
		7–3	–	0x0c	–	R	–
		2–0	IRAMSZ[2:0]	0x6	H0	R/WP	
0x4004	MSCTTBRL (MISC Vector Table Address Low Register)	15–8	TTBR[15:8]	0x80	H0	R/WP	–
		7–0	TTBR[7:0]	0x00	H0	R	
0x4006	MSCTTBRH (MISC Vector Table Address High Register)	15–8	–	0x00	–	R	–
		7–0	TTBR[23:16]	0x00	H0	R/WP	
0x4008	MSCPSR (MISC PSR Register)	15–8	–	0x00	–	R	–
		7–5	PSRIL[2:0]	0x0	H0	R	
		4	PSRIE	0	H0	R	
		3	PSRC	0	H0	R	
		2	PSRV	0	H0	R	
		1	PSRZ	0	H0	R	
		0	PSRN	0	H0	R	

0x4020 Power Generator (PWG)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4020	PWGVD1CTL	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1–0	REGMODE[1:0]	0x0	H0	R/WP	

0x4040–0x4050 Clock Generator (CLG)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4040	CLGSCLK (CLG System Clock Control Register)	15	WUPMD	0	H0	R/WP	–
		14	–	0	–	R	
		13–12	WUPDIV[1:0]	0x0	H0	R/WP	
		11–10	–	0x0	–	R	
		9–8	WUPSRC[1:0]	0x0	H0	R/WP	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x4042	CLGOSC (CLG Oscillation Control Register)	15–12	–	0x0	–	R	–
		11	EXOSCSLPC	1	H0	R/W	
		10	OSC3SLPC	1	H0	R/W	
		9	OSC1SLPC	1	H0	R/W	
		8	IOSCSLPC	1	H0	R/W	
		7–4	–	0x0	–	R	
		3	EXOSCEN	0	H0	R/W	
		2	OSC3EN	0	H0	R/W	
		1	OSC1EN	0	H0	R/W	
		0	IOSCEN	1	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4044	CLGIOSC (CLG IOSC Control Register)	15–8	–	0x00	–	R	–
		7–5	–	0x0	–	R	
		4	IOSCSTM	0	H0	R/WP	
		3–2	–	0x0	–	R	
		1-0	IOSCFQ[1:0]	0x1	H0	R/WP	
0x4046	CLGOSC1 (CLG OSC1 Control Register)	15	–	0	–	R	–
		14	OSDRB	1	H0	R/WP	
		13	OSDEN	0	H0	R/WP	
		12	OSC1BUP	1	H0	R/WP	
		11	–	0	–	R	
		10–8	CGI1[2:0]	0x0	H0	R/WP	
		7–6	INV1B[1:0]	0x2	H0	R/WP	
		5–4	INV1N[1:0]	0x1	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	OSC1WT[1:0]	0x2	H0	R/WP	
0x4048	CLGOSC3 (CLG OSC3 Control Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–4	OSC3INV[1:0]	0x3	H0	R/WP	
		3	–	0	–	R	
		2–0	OSC3WT[2:0]	0x6	H0	R/WP	
0x404c	CLGINTF (CLG Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6	(reserved)	0	H0	R	
		5	OSC1STPIF	0	H0	R/W	Cleared by writing 1.
		4	IOSCTEDIF	0	H0	R/W	
		3	–	0	–	R	–
		2	OSC3STAIF	0	H0	R/W	Cleared by writing 1.
		1	OSC1STAIF	0	H0	R/W	
		0	IOSCSTAIF	0	H0	R/W	
0x404e	CLGINTE (CLG Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6	(reserved)	0	H0	R	
		5	OSC1STPIE	0	H0	R/W	
		4	IOSCTEDIE	0	H0	R/W	
		3	–	0	–	R	
		2	OSC3STAIE	0	H0	R/W	
		1	OSC1STAIE	0	H0	R/W	
		0	IOSCSTAIE	0	H0	R/W	
0x4050	CLGFOUT (CLG FOUT Control Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–4	FOUTDIV[2:0]	0x0	H0	R/W	
		3–2	FOUTSRC[1:0]	0x0	H0	R/W	
		1	–	0	–	R	
		0	FOUTEN	0	H0	R/W	

0x4080–0x4098 Interrupt Controller (ITC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4080	ITCLV0 (ITC Interrupt Level Setup Register 0)	15–11	–	0x00	–	R	–
		10–8	ILV1[2:0]	0x0	H0	R/W	Port interrupt (ILVPPORT)
		7–3	–	0x00	–	R	–
		2–0	ILV0[2:0]	0x0	H0	R/W	Supply voltage detector interrupt (ILVSVD)
0x4082	ITCLV1 (ITC Interrupt Level Setup Register 1)	15–11	–	0x00	–	R	–
		10–8	ILV3[2:0]	0x0	H0	R/W	Clock generator interrupt (ILVCLG)
		7–3	–	0x00	–	R	–
		2–0	ILV2[2:0]	0x0	H0	R/W	(reserved)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4084	ITCLV2 (ITC Interrupt Level Setup Register 2)	15–11	–	0x00	–	R	–
		10–8	ILV5[2:0]	0x0	H0	R/W	16-bit timer Ch.0 interrupt (ILVT16_0)
		7–3	–	0x00	–	R	–
		2–0	ILV4[2:0]	0x0	H0	R/W	Real-time clock interrupt (ILVRTCA_0)
0x4086	ITCLV3 (ITC Interrupt Level Setup Register 3)	15–11	–	0x00	–	R	–
		10–8	ILV7[2:0]	0x0	H0	R/W	16-bit timer Ch.1 interrupt (ILVT16_1)
		7–3	–	0x00	–	R	–
		2–0	ILV6[2:0]	0x0	H0	R/W	UART Ch.0 interrupt (ILVUART_0)
0x4088	ITCLV4 (ITC Interrupt Level Setup Register 4)	15–11	–	0x00	–	R	–
		10–8	ILV9[2:0]	0x0	H0	R/W	I^2C Ch.0 interrupt (ILVI2C_0)
		7–3	–	0x00	–	R	–
		2–0	ILV8[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.0 interrupt (ILVSPIA_0)
0x408a	ITCLV5 (ITC Interrupt Level Setup Register 5)	15–11	–	0x00	–	R	–
		10–8	ILV11[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.1 interrupt (ILVT16B_1)
		7–3	–	0x00	–	R	–
		2–0	ILV10[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.0 interrupt (ILVT16B_0)
0x408c	ITCLV6 (ITC Interrupt Level Setup Register 6)	15–11	–	0x00	–	R	–
		10–8	ILV13[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.3 interrupt (ILVT16B_3)
		7–3	–	0x00	–	R	–
		2–0	ILV12[2:0]	0x0	H0	R/W	16-bit PWM timer Ch.2 interrupt (ILVT16B_2)
0x408e	ITCLV7 (ITC Interrupt Level Setup Register 7)	15–11	–	0x00	–	R	–
		10–8	ILV15[2:0]	0x0	H0	R/W	UART Ch.1 interrupt (ILVUART_1)
		7–3	–	0x00	–	R	–
		2–0	ILV14[2:0]	0x0	H0	R/W	16-bit timer Ch.5 interrupt (ILVT16_5)
0x4090	ITCLV8 (ITC Interrupt Level Setup Register 8)	15–11	–	0x00	–	R	–
		10–8	ILV17[2:0]	0x0	H0	R/W	Synchronous serial interface Ch.1 interrupt (ILVSPIA_1)
		7–3	–	0x00	–	R	–
		2–0	ILV16[2:0]	0x0	H0	R/W	16-bit timer Ch.2 interrupt (ILVT16_2)
0x4092	ITCLV9 (ITC Interrupt Level Setup Register 9)	15–11	–	0x00	–	R	–
		10–8	ILV19[2:0]	0x0	H0	R/W	IR remote controller interrupt (ILVREMC2_0)
		7–3	–	0x00	–	R	–
		2–0	ILV18[2:0]	0x0	H0	R/W	I^2C Ch.1 interrupt (ILVI2C_1)
0x4094	ITCLV10 (ITC Interrupt Level Setup Register 10)	15–11	–	0x00	–	R	–
		10–8	ILV21[2:0]	0x0	H0	R/W	10-bit A/D converter Ch.0 interrupt (ILVADC10_0)
		7–3	–	0x00	–	R	–
		2–0	ILV20[2:0]	0x0	H0	R/W	16-bit timer Ch.3 interrupt (ILVT16_3)
0x4096	ITCLV11 (ITC Interrupt Level Setup Register 11)	15–11	–	0x00	–	R	–
		10–8	ILV23[2:0]	0x0	H0	R/W	10-bit A/D converter Ch.1 interrupt (ILVADC10_1)
		7–3	–	0x00	–	R	–
		2–0	ILV22[2:0]	0x0	H0	R/W	16-bit timer Ch.4 interrupt (ILVT16_4)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4098	ITCLV12 (ITC Interrupt Level Setup Register 12)	15–11	–	0x00	–	R	–
		10–8	ILV25[2:0]	0x0	H0	R/W	(reserved)
		7–3	–	0x00	–	R	–
		2–0	ILV24[2:0]	0x0	H0	R/W	UART Ch.2 interrupt (ILVUART_2)

0x40a0–0x40a2 Watchdog Timer (WDT)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x40a0	WDTCLK (WDT Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/WP	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x40a2	WDTCTL (WDT Control Register)	15–10	–	0x00	–	R	–
		9	NMIXRST	0	H0	R/WP	
		8	STATNMI	0	H0	R	
		7–5	–	0x0	–	R	
		4	WDTCNTRST	0	H0	WP	Always read as 0.
		3–0	WDTRUN[3:0]	0xa	H0	R/WP	–

0x40c0–0x40d2 Real-time Clock (RTCA)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x40c0	RTCCTL (RTC Control Register)	15	RTCTRMBSY	0	H0	R	–
		14–8	RTCTRM[6:0]	0x00	H0	W	Read as 0x00.
		7	–	0	–	R	–
		6	RTCBSY	0	H0	R	
		5	RTCHLD	0	H0	R/W	Cleared by setting the RTCCTL.RTCRST bit to 1.
		4	RTC24H	0	H0	R/W	–
		3	–	0	–	R	
		2	RTCADJ	0	H0	R/W	Cleared by setting the RTCCTL.RTCRST bit to 1.
		1	RTCRST	0	H0	R/W	–
		0	RTCRUN	0	H0	R/W	
0x40c2	RTCALM1 (RTC Second Alarm Register)	15	–	0	–	R	–
		14–12	RTCSHA[2:0]	0x0	H0	R/W	
		11–8	RTCSLA[3:0]	0x0	H0	R/W	
		7–0	–	0x00	–	R	
0x40c4	RTCALM2 (RTC Hour/Minute Alarm Register)	15	–	0	–	R	–
		14	RTCAPA	0	H0	R/W	
		13–12	RTCHHA[1:0]	0x0	H0	R/W	
		11–8	RTCHLA[3:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6–4	RTCMIHA[2:0]	0x0	H0	R/W	
		3–0	RTCMILA[3:0]	0x0	H0	R/W	
0x40c6	RTCSWCTL (RTC Stopwatch Control Register)	15–12	BCD10[3:0]	0x0	H0	R	–
		11–8	BCD100[3:0]	0x0	H0	R	
		7–5	–	0x0	–	R	
		4	SWRST	0	H0	W	Read as 0.
		3–1	–	0x0	–	R	–
		0	SWRUN	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x40c8	RTCSEC (RTC Second/1Hz Register)	15	–	0	–	R	–
		14–12	RTCSH[2:0]	0x0	H0	R/W	
		11–8	RTCSL[3:0]	0x0	H0	R/W	
		7	RTC1HZ	0	H0	R	Cleared by setting the RTCCTL.RTCRST bit to 1.
		6	RTC2HZ	0	H0	R	
		5	RTC4HZ	0	H0	R	
		4	RTC8HZ	0	H0	R	
		3	RTC16HZ	0	H0	R	
		2	RTC32HZ	0	H0	R	
		1	RTC64HZ	0	H0	R	
		0	RTC128HZ	0	H0	R	
0x40ca	RTCHUR (RTC Hour/Minute Register)	15	–	0	–	R	–
		14	RTCAP	0	H0	R/W	
		13–12	RTCHH[1:0]	0x1	H0	R/W	
		11–8	RTCHL[3:0]	0x2	H0	R/W	
		7	–	0	–	R	
		6–4	RTCMIH[2:0]	0x0	H0	R/W	
		3–0	RTCMIL[3:0]	0x0	H0	R/W	
0x40cc	RTCMON (RTC Month/Day Register)	15–13	–	0x0	–	R	–
		12	RTCMOH	0	H0	R/W	
		11–8	RTCMOL[3:0]	0x1	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	RTCDH[1:0]	0x0	H0	R/W	
		3–0	RTCDL[3:0]	0x1	H0	R/W	
0x40ce	RTCYAR (RTC Year/Week Register)	15–11	–	0x00	–	R	–
		10–8	RTCWK[2:0]	0x0	H0	R/W	
		7–4	RTCYH[3:0]	0x0	H0	R/W	
		3–0	RTCYL[3:0]	0x0	H0	R/W	
0x40d0	RTCINTF (RTC Interrupt Flag Register)	15	RTCTRMIF	0	H0	R/W	Cleared by writing 1.
		14	SW1IF	0	H0	R/W	
		13	SW10IF	0	H0	R/W	
		12	SW100IF	0	H0	R/W	
		11–9	–	0x0	–	R	–
		8	ALARMIF	0	H0	R/W	Cleared by writing 1.
		7	1DAYIF	0	H0	R/W	
		6	1HURIF	0	H0	R/W	
		5	1MINIF	0	H0	R/W	
		4	1SECIF	0	H0	R/W	
		3	1_2SECIF	0	H0	R/W	
		2	1_4SECIF	0	H0	R/W	
		1	1_8SECIF	0	H0	R/W	
		0	1_32SECIF	0	H0	R/W	
0x40d2	RTCINTE (RTC Interrupt Enable Register)	15	RTCTRMIE	0	H0	R/W	–
		14	SW1IE	0	H0	R/W	
		13	SW10IE	0	H0	R/W	
		12	SW100IE	0	H0	R/W	
		11–9	–	0x0	–	R	
		8	ALARMIE	0	H0	R/W	
		7	1DAYIE	0	H0	R/W	
		6	1HURIE	0	H0	R/W	
		5	1MINIE	0	H0	R/W	
		4	1SECIE	0	H0	R/W	
		3	1_2SECIE	0	H0	R/W	
		2	1_4SECIE	0	H0	R/W	
		1	1_8SECIE	0	H0	R/W	
		0	1_32SECIE	0	H0	R/W	

0x4100–0x4106 Supply Voltage Detector (SVD)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4100	SVDCLK (SVD Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	1	H0	R/WP	
		7	–	0	–	R	
		6–4	CLKDIV[2:0]	0x0	H0	R/WP	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x4102	SVDCTL (SVD Control Register)	15	–	0	–	R	–
		14–13	SVDSC[1:0]	0x0	H0	R/WP	Writing takes effect when the SVDCTL.SVDMD[1:0] bits are not 0x0.
		12–8	SVDC[4:0]	0x1e	H1	R/WP	–
		7–4	SVDRE[3:0]	0x0	H1	R/WP	
		3	–	0	–	R	
		2–1	SVDMD[1:0]	0x0	H0	R/WP	
		0	MODEN	0	H1	R/WP	
0x4104	SVDINTF (SVD Status and Interrupt Flag Register)	15–9	–	0x00	–	R	–
		8	SVDDT	x	–	R	
		7–1	–	0x00	–	R	
		0	SVDIF	0	H1	R/W	Cleared by writing 1.
0x4106	SVDINTE (SVD Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	SVDIE	0	H0	R/W	

0x4160–0x416c 16-bit Timer (T16) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4160	T16_0CLK (T16 Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x4162	T16_0MOD (T16 Ch.0 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x4164	T16_0CTL (T16 Ch.0 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x4166	T16_0TR (T16 Ch.0 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x4168	T16_0TC (T16 Ch.0 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x416a	T16_0INTF (T16 Ch.0 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x416c	T16_0INTE (T16 Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x41b0 Flash Controller (FLASHC)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x41b0	FLASHCWAIT (FLASHC Flash Read Cycle Register)	15–8	–	0x00	–	R	–
		7	XBUSY	0	H0	R	
		6–2	–	0x00	–	R	
		1–0	RDWAIT[1:0]	0x1	H0	R/WP	

0x4200–0x42e2 I/O Ports (PPORT)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4200	P0DAT (P0 Port Data Register)	15–8	P0OUT[7:0]	0x00	H0	R/W	–
		7–0	P0IN[7:0]	0x00	H0	R	
0x4202	P0IOEN (P0 Port Enable Register)	15–8	P0IEN[7:0]	0x00	H0	R/W	–
		7–0	P0OEN[7:0]	0x00	H0	R/W	
0x4204	P0RCTL (P0 Port Pull-up/down Control Register)	15–8	P0PDPU[7:0]	0x00	H0	R/W	–
		7–0	P0REN[7:0]	0x00	H0	R/W	
0x4206	P0INTF (P0 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P0IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4208	P0INTCTL (P0 Port Interrupt Control Register)	15–8	P0EDGE[7:0]	0x00	H0	R/W	–
		7–0	P0IE[7:0]	0x00	H0	R/W	
0x420a	P0CHATEN (P0 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P0CHATEN[7:0]	0x00	H0	R/W	
0x420c	P0MODSEL (P0 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P0SEL[7:0]	0x00	H0	R/W	
0x420e	P0FNCSEL (P0 Port Function Select Register)	15–14	P07MUX[1:0]	0x0	H0	R/W	–
		13–12	P06MUX[1:0]	0x0	H0	R/W	
		11–10	P05MUX[1:0]	0x0	H0	R/W	
		9–8	P04MUX[1:0]	0x0	H0	R/W	
		7–6	P03MUX[1:0]	0x0	H0	R/W	
		5–4	P02MUX[1:0]	0x0	H0	R/W	
		3–2	P01MUX[1:0]	0x0	H0	R/W	
		1–0	P00MUX[1:0]	0x0	H0	R/W	
0x4210	P1DAT (P1 Port Data Register)	15–8	P1OUT[7:0]	0x00	H0	R/W	–
		7–0	P1IN[7:0]	0x00	H0	R	
0x4212	P1IOEN (P1 Port Enable Register)	15–8	P1IEN[7:0]	0x00	H0	R/W	–
		7–0	P1OEN[7:0]	0x00	H0	R/W	
0x4214	P1RCTL (P1 Port Pull-up/down Control Register)	15–8	P1PDPU[7:0]	0x00	H0	R/W	–
		7–0	P1REN[7:0]	0x00	H0	R/W	
0x4216	P1INTF (P1 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P1IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4218	P1INTCTL (P1 Port Interrupt Control Register)	15–8	P1EDGE[7:0]	0x00	H0	R/W	–
		7–0	P1IE[7:0]	0x00	H0	R/W	
0x421a	P1CHATEN (P1 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P1CHATEN[7:0]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x421c	P1MODSEL (P1 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P1SEL[7:0]	0x00	H0	R/W	
0x421e	P1FNCSEL (P1 Port Function Select Register)	15–14	P17MUX[1:0]	0x2	H0	R	–
		13–12	P16MUX[1:0]	0x2	H0	R	
		11–10	P15MUX[1:0]	0x2	H0	R	
		9–8	P14MUX[1:0]	0x2	H0	R	
		7–6	P13MUX[1:0]	0x2	H0	R	
		5–4	P12MUX[1:0]	0x2	H0	R	
		3–2	P11MUX[1:0]	0x2	H0	R	
		1–0	P10MUX[1:0]	0x2	H0	R	
0x4220	P2DAT (P2 Port Data Register)	15–8	P2OUT[7:0]	0x00	H0	R/W	–
		7–0	P2IN[7:0]	0x00	H0	R	
0x4222	P2IOEN (P2 Port Enable Register)	15–8	P2IEN[7:0]	0x00	H0	R/W	–
		7–0	P2OEN[7:0]	0x00	H0	R/W	
0x4224	P2RCTL (P2 Port Pull-up/down Control Register)	15–8	P2PDPU[7:0]	0x00	H0	R/W	–
		7–0	P2REN[7:0]	0x00	H0	R/W	
0x4226	P2INTF (P2 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P2IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4228	P2INTCTL (P2 Port Interrupt Control Register)	15–8	P2EDGE[7:0]	0x00	H0	R/W	–
		7–0	P2IE[7:0]	0x00	H0	R/W	
0x422a	P2CHATEN (P2 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P2CHATEN[7:0]	0x00	H0	R/W	
0x422c	P2MODSEL (P2 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P2SEL[7:0]	0x00	H0	R/W	
0x422e	P2FNCSEL (P2 Port Function Select Register)	15–14	P27MUX[1:0]	0x2	H0	R	–
		13–12	P26MUX[1:0]	0x2	H0	R	
		11–10	P25MUX[1:0]	0x2	H0	R	
		9–8	P24MUX[1:0]	0x2	H0	R	
		7–6	P23MUX[1:0]	0x2	H0	R	
		5–4	P22MUX[1:0]	0x2	H0	R	
		3–2	P21MUX[1:0]	0x2	H0	R	
		1–0	P20MUX[1:0]	0x2	H0	R	
0x4230	P3DAT (P3 Port Data Register)	15–8	P3OUT[7:0]	0x00	H0	R/W	–
		7–0	P3IN[7:0]	0x00	H0	R	
0x4232	P3IOEN (P3 Port Enable Register)	15–8	P3IEN[7:0]	0x00	H0	R/W	–
		7–0	P3OEN[7:0]	0x00	H0	R/W	
0x4234	P3RCTL (P3 Port Pull-up/down Control Register)	15–8	P3PDPU[7:0]	0x00	H0	R/W	–
		7–0	P3REN[7:0]	0x00	H0	R/W	
0x4236	P3INTF (P3 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P3IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4238	P3INTCTL (P3 Port Interrupt Control Register)	15–8	P3EDGE[7:0]	0x00	H0	R/W	–
		7–0	P3IE[7:0]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x423a	P3CHATEN (P3 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P3CHATEN[7:0]	0x00	H0	R/W	
0x423c	P3MODSEL (P3 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P3SEL[7:0]	0x00	H0	R/W	
0x423e	P3FNCSEL (P3 Port Function Select Register)	15–14	P37MUX[1:0]	0x0	H0	R/W	–
		13–12	P36MUX[1:0]	0x0	H0	R/W	
		11–10	P35MUX[1:0]	0x0	H0	R/W	
		9–8	P34MUX[1:0]	0x0	H0	R/W	
		7–6	P33MUX[1:0]	0x0	H0	R/W	
		5–4	P32MUX[1:0]	0x0	H0	R/W	
		3–2	P31MUX[1:0]	0x0	H0	R/W	
		1–0	P30MUX[1:0]	0x0	H0	R/W	
0x4240	P4DAT (P4 Port Data Register)	15–8	P4OUT[7:0]	0x00	H0	R/W	–
		7–0	P4IN[7:0]	0x00	H0	R	
0x4242	P4IOEN (P4 Port Enable Register)	15–8	P4IEN[7:0]	0x00	H0	R/W	–
		7–0	P4OEN[7:0]	0x00	H0	R/W	
0x4244	P4RCTL (P4 Port Pull-up/down Control Register)	15–8	P4PDPU[7:0]	0x00	H0	R/W	–
		7–0	P4REN[7:0]	0x00	H0	R/W	
0x4246	P4INTF (P4 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P4IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4248	P4INTCTL (P4 Port Interrupt Control Register)	15–8	P4EDGE[7:0]	0x00	H0	R/W	–
		7–0	P4IE[7:0]	0x00	H0	R/W	
0x424a	P4CHATEN (P4 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P4CHATEN[7:0]	0x00	H0	R/W	
0x424c	P4MODSEL (P4 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P4SEL[7:0]	0x00	H0	R/W	
0x424e	P4FNCSEL (P4 Port Function Select Register)	15–14	P47MUX[1:0]	0x2	H0	R	–
		13–12	P46MUX[1:0]	0x2	H0	R	
		11–10	P45MUX[1:0]	0x2	H0	R	
		9–8	P44MUX[1:0]	0x2	H0	R	
		7–6	P43MUX[1:0]	0x2	H0	R	
		5–4	P42MUX[1:0]	0x2	H0	R	
		3–2	P41MUX[1:0]	0x2	H0	R	
		1–0	P40MUX[1:0]	0x2	H0	R	
0x4250	P5DAT (P5 Port Data Register)	15–14	–	0x0	–	R	–
		13–8	P5OUT[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P5IN[5:0]	0x00	H0	R	
0x4252	P5IOEN (P5 Port Enable Register)	15–14	–	0x0	–	R	–
		13–8	P5IEN[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P5OEN[5:0]	0x00	H0	R/W	
0x4254	P5RCTL (P5 Port Pull-up/down Control Register)	15–14	–	0x0	–	R	–
		13–8	P5PDPU[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P5REN[5:0]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4256	P5INTF (P5 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	P5IF[5:0]	0x00	H0	R/W	Cleared by writing 1.
0x4258	P5INTCTL (P5 Port Interrupt Control Register)	15–14	–	0x0	–	R	–
		13–8	P5EDGE[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	P5IEN[5:0]	0x00	H0	R/W	
0x425a	P5CHATEN (P5 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	P5CHATEN[5:0]	0x00	H0	R/W	
0x425c	P5MODSEL (P5 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	P5SEL[5:0]	0x00	H0	R/W	
0x425e	P5FNCSEL (P5 Port Function Select Register)	15–12	–	0x0	–	R	–
		11–10	P55MUX[1:0]	0x2	H0	R	
		9–8	P54MUX[1:0]	0x2	H0	R	
		7–6	P53MUX[1:0]	0x2	H0	R	
		5–4	P52MUX[1:0]	0x2	H0	R	
		3–2	P51MUX[1:0]	0x2	H0	R	
		1–0	P50MUX[1:0]	0x2	H0	R	
0x4260	P6DAT (P6 Port Data Register)	15–8	P6OUT[7:0]	0x00	H0	R/W	–
		7–0	P6IN[7:0]	0x00	H0	R	
0x4262	P6IOEN (P6 Port Enable Register)	15–8	P6IEN[7:0]	0x00	H0	R/W	–
		7–0	P6OEN[7:0]	0x00	H0	R/W	
0x4264	P6RCTL (P6 Port Pull-up/down Control Register)	15–8	P6PDPU[7:0]	0x00	H0	R/W	–
		7–0	P6REN[7:0]	0x00	H0	R/W	
0x4266	P6INTF (P6 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P6IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4268	P6INTCTL (P6 Port Interrupt Control Register)	15–8	P6EDGE[7:0]	0x00	H0	R/W	–
		7–0	P6IE[7:0]	0x00	H0	R/W	
0x426a	P6CHATEN (P6 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P6CHATEN[7:0]	0x00	H0	R/W	
0x426c	P6MODSEL (P6 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P6SEL[7:0]	0x00	H0	R/W	
0x426e	P6FNCSEL (P6 Port Function Select Register)	15–14	P67MUX[1:0]	0x0	H0	R/W	–
		13–12	P66MUX[1:0]	0x0	H0	R/W	
		11–10	P65MUX[1:0]	0x0	H0	R/W	
		9–8	P64MUX[1:0]	0x0	H0	R/W	
		7–6	P63MUX[1:0]	0x0	H0	R/W	
		5–4	P62MUX[1:0]	0x0	H0	R/W	
		3–2	P61MUX[1:0]	0x0	H0	R/W	
		1–0	P60MUX[1:0]	0x0	H0	R/W	
0x4270	P7DAT (P7 Port Data Register)	15–8	P7OUT[7:0]	0x00	H0	R/W	–
		7–0	P7IN[7:0]	0x00	H0	R	
0x4272	P7IOEN (P7 Port Enable Register)	15–8	P7IEN[7:0]	0x00	H0	R/W	–
		7–0	P7OEN[7:0]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4274	P7RCTL (P7 Port Pull-up/down Control Register)	15–8	P7PDPU[7:0]	0x00	H0	R/W	–
		7–0	P7REN[7:0]	0x00	H0	R/W	
0x4276	P7INTF (P7 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P7IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4278	P7INTCTL (P7 Port Interrupt Control Register)	15–8	P7EDGE[7:0]	0x00	H0	R/W	–
		7–0	P7IE[7:0]	0x00	H0	R/W	
0x427a	P7CHATEN (P7 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P7CHATEN[7:0]	0x00	H0	R/W	
0x427c	P7MODSEL (P7 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P7SEL[7:0]	0x00	H0	R/W	
0x427e	P7FNCSEL (P7 Port Function Select Register)	15–14	P77MUX[1:0]	0x0	H0	R/W	–
		13–12	P76MUX[1:0]	0x0	H0	R/W	
		11–10	P75MUX[1:0]	0x0	H0	R/W	
		9–8	P74MUX[1:0]	0x0	H0	R/W	
		7–6	P73MUX[1:0]	0x0	H0	R/W	
		5–4	P72MUX[1:0]	0x0	H0	R/W	
		3–2	P71MUX[1:0]	0x0	H0	R/W	
		1–0	P70MUX[1:0]	0x0	H0	R/W	
0x4280	P8DAT (P8 Port Data Register)	15–8	P8OUT[7:0]	0x00	H0	R/W	–
		7–0	P8IN[7:0]	0x00	H0	R	
0x4282	P8IOEN (P8 Port Enable Register)	15–8	P8IEN[7:0]	0x00	H0	R/W	–
		7–0	P8OEN[7:0]	0x00	H0	R/W	
0x4284	P8RCTL (P8 Port Pull-up/down Control Register)	15–8	P8PDPU[7:0]	0x00	H0	R/W	–
		7–0	P8REN[7:0]	0x00	H0	R/W	
0x4286	P8INTF (P8 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–0	P8IF[7:0]	0x00	H0	R/W	Cleared by writing 1.
0x4288	P8INTCTL (P8 Port Interrupt Control Register)	15–8	P8EDGE[7:0]	0x00	H0	R/W	–
		7–0	P8IE[7:0]	0x00	H0	R/W	
0x428a	P8CHATEN (P8 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–0	P8CHATEN[7:0]	0x00	H0	R/W	
0x428c	P8MODSEL (P8 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–0	P8SEL[7:0]	0x00	H0	R/W	
0x428e	P8FNCSEL (P8 Port Function Select Register)	15–14	P87MUX[1:0]	0x2	H0	R	–
		13–12	P86MUX[1:0]	0x2	H0	R	
		11–10	P85MUX[1:0]	0x2	H0	R	
		9–8	P84MUX[1:0]	0x2	H0	R	
		7–6	P83MUX[1:0]	0x2	H0	R	
		5–4	P82MUX[1:0]	0x2	H0	R	
		3–2	P81MUX[1:0]	0x2	H0	R	
		1–0	P80MUX[1:0]	0x2	H0	R	
0x4290	P9DAT (P9 Port Data Register)	15	–	0	–	R	–
		14–8	P9OUT[6:0]	0x00	H0	R/W	
		7	–	0	–	R	
		6–0	P9IN[6:0]	0x00	H0	R	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4292	P9IOEN (P9 Port Enable Register)	15	–	0	–	R	–
		14–8	P9IEN[6:0]	0x00	H0	R/W	
		7	–	0	–	R	
		6–0	P9OEN[6:0]	0x00	H0	R/W	
0x4294	P9RCTL (P9 Port Pull-up/down Control Register)	15	–	0	–	R	–
		14–8	P9PDPU[6:0]	0x00	H0	R/W	
		7	–	0	–	R	
		6–0	P9REN[6:0]	0x00	H0	R/W	
0x4296	P9INTF (P9 Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–0	P9IF[6:0]	0x00	H0	R/W	Cleared by writing 1.
0x4298	P9INTCTL (P9 Port Interrupt Control Register)	15	–	0	–	R	–
		14–8	P9EDGE[6:0]	0x00	H0	R/W	
		7	–	0	–	R	
		6–0	P9IEN[6:0]	0x00	H0	R/W	
0x429a	P9CHATEN (P9 Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–0	P9CHATEN[6:0]	0x00	H0	R/W	
0x429c	P9MODSEL (P9 Port Mode Select Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–0	P9SEL[6:0]	0x00	H0	R/W	
0x429e	P9FNCSEL (P9 Port Function Select Register)	15–14	–	0x0	–	R	–
		13–12	P96MUX[1:0]	0x2	H0	R	
		11–10	P95MUX[1:0]	0x2	H0	R	
		9–8	P94MUX[1:0]	0x2	H0	R	
		7–6	P93MUX[1:0]	0x0	H0	R/W	
		5–4	P92MUX[1:0]	0x0	H0	R/W	
		3–2	P91MUX[1:0]	0x0	H0	R/W	
		1–0	P90MUX[1:0]	0x0	H0	R/W	
0x42a0	PADAT (Pa Port Data Register)	15–14	–	0x0	–	R	–
		13–8	PAOUT[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	PAIN[5:0]	0x00	H0	R	
0x42a2	PAIOEN (Pa Port Enable Register)	15–14	–	0x0	–	R	–
		13–8	PAIEN[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	PAOEN[5:0]	0x00	H0	R/W	
0x42a4	PARCTL (Pa Port Pull-up/down Control Register)	15–14	–	0x0	–	R	–
		13–8	PAPDPU[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	PAREN[5:0]	0x00	H0	R/W	
0x42a6	PAINTF (Pa Port Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	PAIF[5:0]	0x00	H0	R/W	Cleared by writing 1.
0x42a8	PAINTCTL (Pa Port Interrupt Control Register)	15–14	–	0x0	–	R	–
		13–8	PAEDGE[5:0]	0x00	H0	R/W	
		7–6	–	0x0	–	R	
		5–0	PAIEN[5:0]	0x00	H0	R/W	
0x42aa	PACHATEN (Pa Port Chattering Filter Enable Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	PACHATEN[5:0]	0x00	H0	R/W	
0x42ac	PAMODSEL (Pa Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5–0	PASEL[5:0]	0x00	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x42ae	PAFNCSEL (Pa Port Function Select Register)	15–12	–	0x0	–	R	–
		11–10	PA5MUX[1:0]	0x2	H0	R	
		9–8	PA4MUX[1:0]	0x2	H0	R	
		7–6	PA3MUX[1:0]	0x2	H0	R	
		5–4	PA2MUX[1:0]	0x2	H0	R	
		3–2	PA1MUX[1:0]	0x2	H0	R	
		1–0	PA0MUX[1:0]	0x2	H0	R	
0x42d0	PDDAT (Pd Port Data Register)	15–13	–	0x0	–	R	–
		12–8	PDOUT[4:0]	0x00	H0	R/W	
		7–5	–	0x0	–	R	
		4–3	PDIN[4:3]	x	H0	R	
		2	–	0	–	R	
		1–0	PDIN[1:0]	x	H0	R	
0x42d2	PDIOEN (Pd Port Enable Register)	15–13	–	0x0	–	R	–
		12–11	PDIEN[4:3]	0x0	H0	R/W	
		10	(reserved)	0	H0	R/W	
		9–8	PDIEN[1:0]	0x0	H0	R/W	
		7–5	–	0x0	–	R	
		4–0	PDOEN[4:0]	0x00	H0	R/W	
0x42d4	PDRCTL (Pd Port Pull-up/down Control Register)	15–13	–	0x0	–	R	–
		12–11	PDPDPU[4:3]	0x0	H0	R/W	
		10	(reserved)	0	H0	R/W	
		9–8	PDPDPU[1:0]	0x0	H0	R/W	
		7–5	–	0x0	–	R	
		4–3	PDREN[4:3]	0x0	H0	R/W	
		2	(reserved)	0	H0	R/W	
		1–0	PDREN[1:0]	0x0	H0	R/W	
0x42dc	PDMODSEL (Pd Port Mode Select Register)	15–8	–	0x00	–	R	–
		7–5	–	0x0	–	R	
		4–0	PDSEL[4:0]	0x07	H0	R/W	
0x42de	PDFNCSEL (Pd Port Function Select Register)	15–10	–	0x00	–	R	–
		9–8	PD4MUX[1:0]	0x0	H0	R/W	
		7–6	PD3MUX[1:0]	0x0	H0	R/W	
		5–4	PD2MUX[1:0]	0x0	H0	R/W	
		3–2	PD1MUX[1:0]	0x0	H0	R/W	
		1–0	PD0MUX[1:0]	0x0	H0	R/W	
0x42e0	PCLK (P Port Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/WP	
		7–4	CLKDIV[3:0]	0x0	H0	R/WP	
		3–2	KRSTCFG[1:0]	0x0	H0	R/WP	
		1–0	CLKSRC[1:0]	0x0	H0	R/WP	
0x42e2	PINTFGRP (P Port Interrupt Flag Group Register)	15–11	–	0x00	–	R	–
		10	PAINT	0	H0	R	
		9	P9INT	0	H0	R	
		8	P8INT	0	H0	R	
		7	P7INT	0	H0	R	
		6	P6INT	0	H0	R	
		5	P5INT	0	H0	R	
		4	P4INT	0	H0	R	
		3	P3INT	0	H0	R	
		2	P2INT	0	H0	R	
		1	P1INT	0	H0	R	
		0	P0INT	0	H0	R	

0x4300–0x431e Universal Port Multiplexer (UPMUX)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4300	P0UPMUX0 (P00–01 Universal Port Multiplexer Setting Register)	15–13	P01PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P01PERICH[1:0]	0x0	H0	R/W	
		10–8	P01PERISEL[2:0]	0x0	H0	R/W	
		7–5	P00PPFNC[2:0]	0x0	H0	R/W	
		4–3	P00PERICH[1:0]	0x0	H0	R/W	
		2–0	P00PERISEL[2:0]	0x0	H0	R/W	
0x4302	P0UPMUX1 (P02–03 Universal Port Multiplexer Setting Register)	15–13	P03PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P03PERICH[1:0]	0x0	H0	R/W	
		10–8	P03PERISEL[2:0]	0x0	H0	R/W	
		7–5	P02PPFNC[2:0]	0x0	H0	R/W	
		4–3	P02PERICH[1:0]	0x0	H0	R/W	
		2–0	P02PERISEL[2:0]	0x0	H0	R/W	
0x4304	P0UPMUX2 (P04–05 Universal Port Multiplexer Setting Register)	15–13	P05PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P05PERICH[1:0]	0x0	H0	R/W	
		10–8	P05PERISEL[2:0]	0x0	H0	R/W	
		7–5	P04PPFNC[2:0]	0x0	H0	R/W	
		4–3	P04PERICH[1:0]	0x0	H0	R/W	
		2–0	P04PERISEL[2:0]	0x0	H0	R/W	
0x4306	P0UPMUX3 (P06–07 Universal Port Multiplexer Setting Register)	15–13	P07PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P07PERICH[1:0]	0x0	H0	R/W	
		10–8	P07PERISEL[2:0]	0x0	H0	R/W	
		7–5	P06PPFNC[2:0]	0x0	H0	R/W	
		4–3	P06PERICH[1:0]	0x0	H0	R/W	
		2–0	P06PERISEL[2:0]	0x0	H0	R/W	
0x4308	P3UPMUX0 (P30–31 Universal Port Multiplexer Setting Register)	15–13	P31PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P31PERICH[1:0]	0x0	H0	R/W	
		10–8	P31PERISEL[2:0]	0x0	H0	R/W	
		7–5	P30PPFNC[2:0]	0x0	H0	R/W	
		4–3	P30PERICH[1:0]	0x0	H0	R/W	
		2–0	P30PERISEL[2:0]	0x0	H0	R/W	
0x430a	P3UPMUX1 (P32–33 Universal Port Multiplexer Setting Register)	15–13	P33PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P33PERICH[1:0]	0x0	H0	R/W	
		10–8	P33PERISEL[2:0]	0x0	H0	R/W	
		7–5	P32PPFNC[2:0]	0x0	H0	R/W	
		4–3	P32PERICH[1:0]	0x0	H0	R/W	
		2–0	P32PERISEL[2:0]	0x0	H0	R/W	
0x430c	P3UPMUX2 (P34–35 Universal Port Multiplexer Setting Register)	15–13	P35PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P35PERICH[1:0]	0x0	H0	R/W	
		10–8	P35PERISEL[2:0]	0x0	H0	R/W	
		7–5	P34PPFNC[2:0]	0x0	H0	R/W	
		4–3	P34PERICH[1:0]	0x0	H0	R/W	
		2–0	P34PERISEL[2:0]	0x0	H0	R/W	
0x430e	P3UPMUX3 (P36–37 Universal Port Multiplexer Setting Register)	15–13	P37PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P37PERICH[1:0]	0x0	H0	R/W	
		10–8	P37PERISEL[2:0]	0x0	H0	R/W	
		7–5	P36PPFNC[2:0]	0x0	H0	R/W	
		4–3	P36PERICH[1:0]	0x0	H0	R/W	
		2–0	P36PERISEL[2:0]	0x0	H0	R/W	
0x4310	P6UPMUX0 (P60–61 Universal Port Multiplexer Setting Register)	15–13	P61PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P61PERICH[1:0]	0x0	H0	R/W	
		10–8	P61PERISEL[2:0]	0x0	H0	R/W	
		7–5	P60PPFNC[2:0]	0x0	H0	R/W	
		4–3	P60PERICH[1:0]	0x0	H0	R/W	
		2–0	P60PERISEL[2:0]	0x0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4312	P6UPMUX1 (P62–63 Universal Port Multiplexer Setting Register)	15–13	P63PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P63PERICH[1:0]	0x0	H0	R/W	
		10–8	P63PERISEL[2:0]	0x0	H0	R/W	
		7–5	P62PPFNC[2:0]	0x0	H0	R/W	
		4–3	P62PERICH[1:0]	0x0	H0	R/W	
		2–0	P62PERISEL[2:0]	0x0	H0	R/W	
0x4314	P6UPMUX2 (P64–65 Universal Port Multiplexer Setting Register)	15–13	P65PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P65PERICH[1:0]	0x0	H0	R/W	
		10–8	P65PERISEL[2:0]	0x0	H0	R/W	
		7–5	P64PPFNC[2:0]	0x0	H0	R/W	
		4–3	P64PERICH[1:0]	0x0	H0	R/W	
		2–0	P64PERISEL[2:0]	0x0	H0	R/W	
0x4316	P6UPMUX3 (P66–67 Universal Port Multiplexer Setting Register)	15–13	P67PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P67PERICH[1:0]	0x0	H0	R/W	
		10–8	P67PERISEL[2:0]	0x0	H0	R/W	
		7–5	P66PPFNC[2:0]	0x0	H0	R/W	
		4–3	P66PERICH[1:0]	0x0	H0	R/W	
		2–0	P66PERISEL[2:0]	0x0	H0	R/W	
0x4318	P7UPMUX0 (P70–71 Universal Port Multiplexer Setting Register)	15–13	P71PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P71PERICH[1:0]	0x0	H0	R/W	
		10–8	P71PERISEL[2:0]	0x0	H0	R/W	
		7–5	P70PPFNC[2:0]	0x0	H0	R/W	
		4–3	P70PERICH[1:0]	0x0	H0	R/W	
		2–0	P70PERISEL[2:0]	0x0	H0	R/W	
0x431a	P7UPMUX1 (P72–73 Universal Port Multiplexer Setting Register)	15–13	P73PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P73PERICH[1:0]	0x0	H0	R/W	
		10–8	P73PERISEL[2:0]	0x0	H0	R/W	
		7–5	P72PPFNC[2:0]	0x0	H0	R/W	
		4–3	P72PERICH[1:0]	0x0	H0	R/W	
		2–0	P72PERISEL[2:0]	0x0	H0	R/W	
0x431c	P7UPMUX2 (P74–75 Universal Port Multiplexer Setting Register)	15–13	P75PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P75PERICH[1:0]	0x0	H0	R/W	
		10–8	P75PERISEL[2:0]	0x0	H0	R/W	
		7–5	P74PPFNC[2:0]	0x0	H0	R/W	
		4–3	P74PERICH[1:0]	0x0	H0	R/W	
		2–0	P74PERISEL[2:0]	0x0	H0	R/W	
0x431e	P7UPMUX3 (P76–77 Universal Port Multiplexer Setting Register)	15–13	P77PPFNC[2:0]	0x0	H0	R/W	–
		12–11	P77PERICH[1:0]	0x0	H0	R/W	
		10–8	P77PERISEL[2:0]	0x0	H0	R/W	
		7–5	P76PPFNC[2:0]	0x0	H0	R/W	
		4–3	P76PERICH[1:0]	0x0	H0	R/W	
		2–0	P76PERISEL[2:0]	0x0	H0	R/W	

0x4380–0x438e UART (UART) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4380	UA0CLK (UART Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x4382	UA0MOD (UART Ch.0 Mode Register)	15–10	–	0x00	–	R	–
		9	INVIRRX	0	H0	R/W	
		8	INVIRTX	0	H0	R/W	
		7	–	0	–	R	
		6	PUEN	0	H0	R/W	
		5	OUTMD	0	H0	R/W	
		4	IRMD	0	H0	R/W	
		3	CHLN	0	H0	R/W	
		2	PREN	0	H0	R/W	
		1	PRMD	0	H0	R/W	
		0	STPB	0	H0	R/W	
0x4384	UA0BR (UART Ch.0 Baud-Rate Register)	15–12	–	0x0	–	R	–
		11–8	FMD[3:0]	0x0	H0	R/W	
		7–0	BRT[7:0]	0x00	H0	R/W	
0x4386	UA0CTL (UART Ch.0 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x4388	UA0TXD (UART Ch.0 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x438a	UA0RXD (UART Ch.0 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	
0x438c	UA0INTF (UART Ch.0 Status and Interrupt Flag Register)	15–10	–	0x00	–	R	–
		9	RBSY	0	H0/S0	R	
		8	TBSY	0	H0/S0	R	
		7	–	0	–	R	
		6	TENDIF	0	H0/S0	R/W	Cleared by writing 1.
		5	FEIF	0	H0/S0	R/W	Cleared by writing 1 or reading the UA0RXD register.
		4	PEIF	0	H0/S0	R/W	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	RB2FIF	0	H0/S0	R	Cleared by reading the UA0RXD register.
		1	RB1FIF	0	H0/S0	R	
		0	TBEIF	1	H0/S0	R	Cleared by writing to the UA0TXD register.
0x438e	UA0INTE (UART Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6	TENDIE	0	H0	R/W	
		5	FEIE	0	H0	R/W	
		4	PEIE	0	H0	R/W	
		3	OEIE	0	H0	R/W	
		2	RB2FIE	0	H0	R/W	
		1	RB1FIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x43a0–0x43ac 16-bit Timer (T16) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43a0	T16_1CLK (T16 Ch.1 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x43a2	T16_1MOD (T16 Ch.1 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43a4	T16_1CTL (T16 Ch.1 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x43a6	T16_1TR (T16 Ch.1 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x43a8	T16_1TC (T16 Ch.1 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x43aa	T16_1INTF (T16 Ch.1 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x43ac	T16_1INTE (T16 Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x43b0–0x43ba Synchronous Serial Interface (SPIA) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43b0	SPI0MOD (SPIA Ch.0 Mode Register)	15–12	–	0x0	–	R	–
		11–8	CHLN[3:0]	0x7	H0	R/W	
		7–6	–	0x0	–	R	
		5	PUEN	0	H0	R/W	
		4	NOCLKDIV	0	H0	R/W	
		3	LSBFST	0	H0	R/W	
		2	CPHA	0	H0	R/W	
		1	CPOL	0	H0	R/W	
		0	MST	0	H0	R/W	
0x43b2	SPI0CTL (SPIA Ch.0 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x43b4	SPI0TXD (SPIA Ch.0 Transmit Data Register)	15–0	TXD[15:0]	0x0000	H0	R/W	–
0x43b6	SPI0RXD (SPIA Ch.0 Receive Data Register)	15–0	RXD[15:0]	0x0000	H0	R	–
0x43b8	SPI0INTF (SPIA Ch.0 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	BSY	0	H0	R	
		6–4	–	0x0	–	R	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	TENDIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the SPI0RXD register.
		0	TBEIF	1	H0/S0	R	Cleared by writing to the SPI0TXD register.
0x43ba	SPI0INTE (SPIA Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–4	–	0x0	–	R	
		3	OEIE	0	H0	R/W	
		2	TENDIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x43c0–0x43d2 I²C (I2C) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x43c0	I2C0CLK (I2C Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x43c2	I2C0MOD (I2C Ch.0 Mode Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2	OADR10	0	H0	R/W	
		1	GCEN	0	H0	R/W	
		0	–	0	–	R	
0x43c4	I2C0BR (I2C Ch.0 Baud-Rate Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–0	BRT[6:0]	0x7f	H0	R/W	
0x43c8	I2C0OADR (I2C Ch.0 Own Address Register)	15–10	–	0x00	–	R	–
		9–0	OADR[9:0]	0x000	H0	R/W	
0x43ca	I2C0CTL (I2C Ch.0 Control Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	MST	0	H0	R/W	
		4	TXNACK	0	H0/S0	R/W	
		3	TXSTOP	0	H0/S0	R/W	
		2	TXSTART	0	H0/S0	R/W	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x43cc	I2C0TXD (I2C Ch.0 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x43ce	I2C0RXD (I2C Ch.0 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	
0x43d0	I2C0INTF (I2C Ch.0 Status and Interrupt Flag Register)	15–13	–	0x0	–	R	–
		12	SDALOW	0	H0	R	
		11	SCLLOW	0	H0	R	
		10	BSY	0	H0/S0	R	
		9	TR	0	H0	R	
		8	–	0	–	R	
		7	BYTEENDIF	0	H0/S0	R/W	Cleared by writing 1.
		6	GCIF	0	H0/S0	R/W	
		5	NACKIF	0	H0/S0	R/W	
		4	STOPIF	0	H0/S0	R/W	
		3	STARTIF	0	H0/S0	R/W	
		2	ERRIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the I2C0RXD register.
		0	TBEIF	0	H0/S0	R	Cleared by writing to the I2C0TXD register.
0x43d2	I2C0INTE (I2C Ch.0 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	BYTEENDIE	0	H0	R/W	
		6	GCIE	0	H0	R/W	
		5	NACKIE	0	H0	R/W	
		4	STOPIE	0	H0	R/W	
		3	STARTIE	0	H0	R/W	
		2	ERRIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x5000–0x503a 16-bit PWM Timer (T16B) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5000	T16B0CLK (T16B Ch.0 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	CLKSRC[2:0]	0x0	H0	R/W	
0x5002	T16B0CTL (T16B Ch.0 Counter Control Register)	15–9	–	0x00	–	R	–
		8	MAXBSY	0	H0	R	
		7–6	–	0x0	–	R	
		5–4	CNTMD[1:0]	0x0	H0	R/W	
		3	ONEST	0	H0	R/W	
		2	RUN	0	H0	R/W	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5004	T16B0MC (T16B Ch.0 Max Counter Data Register)	15–0	MC[15:0]	0xffff	H0	R/W	–
0x5006	T16B0TC (T16B Ch.0 Timer Counter Data Register)	15–0	TC[15:0]	0x0000	H0	R	–
0x5008	T16B0CS (T16B Ch.0 Counter Status Register)	15–8	–	0x00	–	R	–
		7	CAPI5	0	H0	R	
		6	CAPI4	0	H0	R	
		5	CAPI3	0	H0	R	
		4	CAPI2	0	H0	R	
		3	CAPI1	0	H0	R	
		2	CAPI0	0	H0	R	
		1	UP_DOWN	1	H0	R	
		0	BSY	0	H0	R	
0x500a	T16B0INTF (T16B Ch.0 Interrupt Flag Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IF	0	H0	R/W	Cleared by writing 1.
		12	CMPCAP5IF	0	H0	R/W	
		11	CAPOW4IF	0	H0	R/W	
		10	CMPCAP4IF	0	H0	R/W	
		9	CAPOW3IF	0	H0	R/W	
		8	CMPCAP3IF	0	H0	R/W	
		7	CAPOW2IF	0	H0	R/W	
		6	CMPCAP2IF	0	H0	R/W	
		5	CAPOW1IF	0	H0	R/W	
		4	CMPCAP1IF	0	H0	R/W	
		3	CAPOW0IF	0	H0	R/W	
		2	CMPCAP0IF	0	H0	R/W	
		1	CNTMAXIF	0	H0	R/W	
		0	CNTZEROIF	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x500c	T16B0INTE (T16B Ch.0 Interrupt Enable Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IE	0	H0	R/W	
		12	CMPCAP5IE	0	H0	R/W	
		11	CAPOW4IE	0	H0	R/W	
		10	CMPCAP4IE	0	H0	R/W	
		9	CAPOW3IE	0	H0	R/W	
		8	CMPCAP3IE	0	H0	R/W	
		7	CAPOW2IE	0	H0	R/W	
		6	CMPCAP2IE	0	H0	R/W	
		5	CAPOW1IE	0	H0	R/W	
		4	CMPCAP1IE	0	H0	R/W	
		3	CAPOW0IE	0	H0	R/W	
		2	CMPCAP0IE	0	H0	R/W	
		1	CNTMAXIE	0	H0	R/W	
		0	CNTZEROIE	0	H0	R/W	
0x5010	T16B0CCCTL0 (T16B Ch.0 Compare/ Capture 0 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5012	T16B0CCR0 (T16B Ch.0 Compare/ Capture 0 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5018	T16B0CCCTL1 (T16B Ch.0 Compare/ Capture 1 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x501a	T16B0CCR1 (T16B Ch.0 Compare/ Capture 1 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5020	T16B0CCCTL2 (T16B Ch.0 Compare/ Capture 2 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5022	T16B0CCR2 (T16B Ch.0 Compare/ Capture 2 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5028	T16B0CCCTL3 (T16B Ch.0 Compare/ Capture 3 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x502a	T16B0CCR3 (T16B Ch.0 Compare/ Capture 3 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5030	T16B0CCCTL4 (T16B Ch.0 Compare/ Capture 4 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5032	T16B0CCR4 (T16B Ch.0 Compare/ Capture 4 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5038	T16B0CCCTL5 (T16B Ch.0 Compare/ Capture 5 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x503a	T16B0CCR5 (T16B Ch.0 Compare/ Capture 5 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

0x5040–0x507a 16-bit PWM Timer (T16B) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5040	T16B1CLK (T16B Ch.1 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	CLKSRC[2:0]	0x0	H0	R/W	
0x5042	T16B1CTL (T16B Ch.1 Counter Control Register)	15–9	–	0x00	–	R	–
		8	MAXBSY	0	H0	R	
		7–6	–	0x0	–	R	
		5–4	CNTMD[1:0]	0x0	H0	R/W	
		3	ONEST	0	H0	R/W	
		2	RUN	0	H0	R/W	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5044	T16B1MC (T16B Ch.1 Max Counter Data Register)	15–0	MC[15:0]	0xffff	H0	R/W	–
0x5046	T16B1TC (T16B Ch.1 Timer Counter Data Register)	15–0	TC[15:0]	0x0000	H0	R	–
0x5048	T16B1CS (T16B Ch.1 Counter Status Register)	15–8	–	0x00	–	R	–
		7	CAPI5	0	H0	R	
		6	CAPI4	0	H0	R	
		5	CAPI3	0	H0	R	
		4	CAPI2	0	H0	R	
		3	CAPI1	0	H0	R	
		2	CAPI0	0	H0	R	
		1	UP_DOWN	1	H0	R	
		0	BSY	0	H0	R	
0x504a	T16B1INTF (T16B Ch.1 Interrupt Flag Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IF	0	H0	R/W	Cleared by writing 1.
		12	CMPCAP5IF	0	H0	R/W	
		11	CAPOW4IF	0	H0	R/W	
		10	CMPCAP4IF	0	H0	R/W	
		9	CAPOW3IF	0	H0	R/W	
		8	CMPCAP3IF	0	H0	R/W	
		7	CAPOW2IF	0	H0	R/W	
		6	CMPCAP2IF	0	H0	R/W	
		5	CAPOW1IF	0	H0	R/W	
		4	CMPCAP1IF	0	H0	R/W	
		3	CAPOW0IF	0	H0	R/W	
		2	CMPCAP0IF	0	H0	R/W	
		1	CNTMAXIF	0	H0	R/W	
		0	CNTZEROIF	0	H0	R/W	
0x504c	T16B1INTE (T16B Ch.1 Interrupt Enable Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IE	0	H0	R/W	
		12	CMPCAP5IE	0	H0	R/W	
		11	CAPOW4IE	0	H0	R/W	
		10	CMPCAP4IE	0	H0	R/W	
		9	CAPOW3IE	0	H0	R/W	
		8	CMPCAP3IE	0	H0	R/W	
		7	CAPOW2IE	0	H0	R/W	
		6	CMPCAP2IE	0	H0	R/W	
		5	CAPOW1IE	0	H0	R/W	
		4	CMPCAP1IE	0	H0	R/W	
		3	CAPOW0IE	0	H0	R/W	
		2	CMPCAP0IE	0	H0	R/W	
		1	CNTMAXIE	0	H0	R/W	
		0	CNTZEROIE	0	H0	R/W	
0x5050	T16B1CCCTL0 (T16B Ch.1 Compare/ Capture 0 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5052	T16B1CCR0 (T16B Ch.1 Compare/ Capture 0 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5058	T16B1CCCTL1 (T16B Ch.1 Compare/ Capture 1 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x505a	T16B1CCR1 (T16B Ch.1 Compare/ Capture 1 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5060	T16B1CCCTL2 (T16B Ch.1 Compare/ Capture 2 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5062	T16B1CCR2 (T16B Ch.1 Compare/ Capture 2 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5068	T16B1CCCTL3 (T16B Ch.1 Compare/ Capture 3 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x506a	T16B1CCR3 (T16B Ch.1 Compare/ Capture 3 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5070	T16B1CCCTL4 (T16B Ch.1 Compare/ Capture 4 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5072	T16B1CCR4 (T16B Ch.1 Compare/ Capture 4 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5078	T16B1CCCTL5 (T16B Ch.1 Compare/ Capture 5 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x507a	T16B1CCR5 (T16B Ch.1 Compare/ Capture 5 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

0x5080–0x50ba 16-bit PWM Timer (T16B) Ch.2

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5080	T16B2CLK (T16B Ch.2 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	CLKSRC[2:0]	0x0	H0	R/W	
0x5082	T16B2CTL (T16B Ch.2 Counter Control Register)	15–9	–	0x00	–	R	–
		8	MAXBSY	0	H0	R	
		7–6	–	0x0	–	R	
		5–4	CNTMD[1:0]	0x0	H0	R/W	
		3	ONEST	0	H0	R/W	
		2	RUN	0	H0	R/W	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5084	T16B2MC (T16B Ch.2 Max Counter Data Register)	15–0	MC[15:0]	0xffff	H0	R/W	–
0x5086	T16B2TC (T16B Ch.2 Timer Counter Data Register)	15–0	TC[15:0]	0x0000	H0	R	–
0x5088	T16B2CS (T16B Ch.2 Counter Status Register)	15–8	–	0x00	–	R	–
		7	CAPI5	0	H0	R	
		6	CAPI4	0	H0	R	
		5	CAPI3	0	H0	R	
		4	CAPI2	0	H0	R	
		3	CAPI1	0	H0	R	
		2	CAPI0	0	H0	R	
		1	UP_DOWN	1	H0	R	
		0	BSY	0	H0	R	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x508a	T16B2INTF (T16B Ch.2 Interrupt Flag Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IF	0	H0	R/W	Cleared by writing 1.
		12	CMPCAP5IF	0	H0	R/W	
		11	CAPOW4IF	0	H0	R/W	
		10	CMPCAP4IF	0	H0	R/W	
		9	CAPOW3IF	0	H0	R/W	
		8	CMPCAP3IF	0	H0	R/W	
		7	CAPOW2IF	0	H0	R/W	
		6	CMPCAP2IF	0	H0	R/W	
		5	CAPOW1IF	0	H0	R/W	
		4	CMPCAP1IF	0	H0	R/W	
		3	CAPOW0IF	0	H0	R/W	
		2	CMPCAP0IF	0	H0	R/W	
		1	CNTMAXIF	0	H0	R/W	
		0	CNTZEROIF	0	H0	R/W	
0x508c	T16B2INTE (T16B Ch.2 Interrupt Enable Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IE	0	H0	R/W	
		12	CMPCAP5IE	0	H0	R/W	
		11	CAPOW4IE	0	H0	R/W	
		10	CMPCAP4IE	0	H0	R/W	
		9	CAPOW3IE	0	H0	R/W	
		8	CMPCAP3IE	0	H0	R/W	
		7	CAPOW2IE	0	H0	R/W	
		6	CMPCAP2IE	0	H0	R/W	
		5	CAPOW1IE	0	H0	R/W	
		4	CMPCAP1IE	0	H0	R/W	
		3	CAPOW0IE	0	H0	R/W	
		2	CMPCAP0IE	0	H0	R/W	
		1	CNTMAXIE	0	H0	R/W	
		0	CNTZEROIE	0	H0	R/W	
0x5090	T16B2CCCTL0 (T16B Ch.2 Compare/ Capture 0 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x5092	T16B2CCR0 (T16B Ch.2 Compare/ Capture 0 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x5098	T16B2CCCTL1 (T16B Ch.2 Compare/ Capture 1 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x509a	T16B2CCR1 (T16B Ch.2 Compare/ Capture 1 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x50a0	T16B2CCCTL2 (T16B Ch.2 Compare/ Capture 2 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50a2	T16B2CCR2 (T16B Ch.2 Compare/ Capture 2 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50a8	T16B2CCCTL3 (T16B Ch.2 Compare/ Capture 3 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50aa	T16B2CCR3 (T16B Ch.2 Compare/ Capture 3 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50b0	T16B2CCCTL4 (T16B Ch.2 Compare/ Capture 4 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50b2	T16B2CCR4 (T16B Ch.2 Compare/ Capture 4 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50b8	T16B2CCCTL5 (T16B Ch.2 Compare/ Capture 5 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50ba	T16B2CCR5 (T16B Ch.2 Compare/ Capture 5 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

0x50c0–0x50fa 16-bit PWM Timer (T16B) Ch.3

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x50c0	T16B3CLK (T16B Ch.3 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	CLKSRC[2:0]	0x0	H0	R/W	
0x50c2	T16B3CTL (T16B Ch.3 Counter Control Register)	15–9	–	0x00	–	R	–
		8	MAXBSY	0	H0	R	
		7–6	–	0x0	–	R	
		5–4	CNTMD[1:0]	0x0	H0	R/W	
		3	ONEST	0	H0	R/W	
		2	RUN	0	H0	R/W	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x50c4	T16B3MC (T16B Ch.3 Max Counter Data Register)	15–0	MC[15:0]	0xffff	H0	R/W	–
0x50c6	T16B3TC (T16B Ch.3 Timer Counter Data Register)	15–0	TC[15:0]	0x0000	H0	R	–
0x50c8	T16B3CS (T16B Ch.3 Counter Status Register)	15–8	–	0x00	–	R	–
		7	CAPI5	0	H0	R	
		6	CAPI4	0	H0	R	
		5	CAPI3	0	H0	R	
		4	CAPI2	0	H0	R	
		3	CAPI1	0	H0	R	
		2	CAPI0	0	H0	R	
		1	UP_DOWN	1	H0	R	
		0	BSY	0	H0	R	
0x50ca	T16B3INTF (T16B Ch.3 Interrupt Flag Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IF	0	H0	R/W	Cleared by writing 1.
		12	CMPCAP5IF	0	H0	R/W	
		11	CAPOW4IF	0	H0	R/W	
		10	CMPCAP4IF	0	H0	R/W	
		9	CAPOW3IF	0	H0	R/W	
		8	CMPCAP3IF	0	H0	R/W	
		7	CAPOW2IF	0	H0	R/W	
		6	CMPCAP2IF	0	H0	R/W	
		5	CAPOW1IF	0	H0	R/W	
		4	CMPCAP1IF	0	H0	R/W	
		3	CAPOW0IF	0	H0	R/W	
		2	CMPCAP0IF	0	H0	R/W	
		1	CNTMAXIF	0	H0	R/W	
		0	CNTZEROIF	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x50cc	T16B3INTE (T16B Ch.3 Interrupt Enable Register)	15–14	–	0x0	–	R	–
		13	CAPOW5IE	0	H0	R/W	
		12	CMPCAP5IE	0	H0	R/W	
		11	CAPOW4IE	0	H0	R/W	
		10	CMPCAP4IE	0	H0	R/W	
		9	CAPOW3IE	0	H0	R/W	
		8	CMPCAP3IE	0	H0	R/W	
		7	CAPOW2IE	0	H0	R/W	
		6	CMPCAP2IE	0	H0	R/W	
		5	CAPOW1IE	0	H0	R/W	
		4	CMPCAP1IE	0	H0	R/W	
		3	CAPOW0IE	0	H0	R/W	
		2	CMPCAP0IE	0	H0	R/W	
		1	CNTMAXIE	0	H0	R/W	
		0	CNTZEROIE	0	H0	R/W	
0x50d0	T16B3CCCTL0 (T16B Ch.3 Compare/ Capture 0 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50d2	T16B3CCR0 (T16B Ch.3 Compare/ Capture 0 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50d8	T16B3CCCTL1 (T16B Ch.3 Compare/ Capture 1 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50da	T16B3CCR1 (T16B Ch.3 Compare/ Capture 1 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50e0	T16B3CCCTL2 (T16B Ch.3 Compare/ Capture 2 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50e2	T16B3CCR2 (T16B Ch.3 Compare/ Capture 2 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x50e8	T16B3CCCTL3 (T16B Ch.3 Compare/ Capture 3 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50ea	T16B3CCR3 (T16B Ch.3 Compare/ Capture 3 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50f0	T16B3CCCTL4 (T16B Ch.3 Compare/ Capture 4 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50f2	T16B3CCR4 (T16B Ch.3 Compare/ Capture 4 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–
0x50f8	T16B3CCCTL5 (T16B Ch.3 Compare/ Capture 5 Control Register)	15	SCS	0	H0	R/W	–
		14–12	CBUFMD[2:0]	0x0	H0	R/W	
		11–10	CAPIS[1:0]	0x0	H0	R/W	
		9–8	CAPTRG[1:0]	0x0	H0	R/W	
		7	–	0	–	R	
		6	TOUTMT	0	H0	R/W	
		5	TOUTO	0	H0	R/W	
		4–2	TOUTMD[2:0]	0x0	H0	R/W	
		1	TOUTINV	0	H0	R/W	
		0	CCMD	0	H0	R/W	
0x50fa	T16B3CCR5 (T16B Ch.3 Compare/ Capture 5 Data Register)	15–0	CC[15:0]	0x0000	H0	R/W	–

0x5140–0x514c 16-bit Timer (T16) Ch.5

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5140	T16_5CLK (T16 Ch.5 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5142	T16_5MOD (T16 Ch.5 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5144	T16_5CTL (T16 Ch.5 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5146	T16_5TR (T16 Ch.5 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x5148	T16_5TC (T16 Ch.5 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x514a	T16_5INTF (T16 Ch.5 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x514c	T16_5INTE (T16 Ch.5 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x5200–0x520e UART (UART) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5200	UA1CLK (UART Ch.1 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5202	UA1MOD (UART Ch.1 Mode Register)	15–10	–	0x00	–	R	–
		9	INVIRRX	0	H0	R/W	
		8	INVIRTX	0	H0	R/W	
		7	–	0	–	R	
		6	PUEN	0	H0	R/W	
		5	OUTMD	0	H0	R/W	
		4	IRMD	0	H0	R/W	
		3	CHLN	0	H0	R/W	
		2	PREN	0	H0	R/W	
		1	PRMD	0	H0	R/W	
		0	STPB	0	H0	R/W	
0x5204	UA1BR (UART Ch.1 Baud-Rate Register)	15–12	–	0x0	–	R	–
		11–8	FMD[3:0]	0x0	H0	R/W	
		7–0	BRT[7:0]	0x00	H0	R/W	
0x5206	UA1CTL (UART Ch.1 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5208	UA1TXD (UART Ch.1 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x520a	UA1RXD (UART Ch.1 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x520c	UA1INTF (UART Ch.1 Status and Interrupt Flag Register)	15–10	–	0x00	–	R	–
		9	RBSY	0	H0/S0	R	
		8	TBSY	0	H0/S0	R	
		7	–	0	–	R	
		6	TENDIF	0	H0/S0	R/W	Cleared by writing 1.
		5	FEIF	0	H0/S0	R/W	Cleared by writing 1 or reading the UA1RXD register.
		4	PEIF	0	H0/S0	R/W	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	RB2FIF	0	H0/S0	R	Cleared by reading the UA1RXD register.
		1	RB1FIF	0	H0/S0	R	
		0	TBEIF	1	H0/S0	R	Cleared by writing to the UA1TXD register.
0x520e	UA1INTE (UART Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6	TENDIE	0	H0	R/W	
		5	FEIE	0	H0	R/W	
		4	PEIE	0	H0	R/W	
		3	OEIE	0	H0	R/W	
		2	RB2FIE	0	H0	R/W	
		1	RB1FIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x5220–0x522e UART (UART) Ch.2

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5220	UA2CLK (UART Ch.2 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5222	UA2MOD (UART Ch.2 Mode Register)	15–10	–	0x00	–	R	–
		9	INVIRRX	0	H0	R/W	
		8	INVIRTX	0	H0	R/W	
		7	–	0	–	R	
		6	PUEN	0	H0	R/W	
		5	OUTMD	0	H0	R/W	
		4	IRMD	0	H0	R/W	
		3	CHLN	0	H0	R/W	
		2	PREN	0	H0	R/W	
		1	PRMD	0	H0	R/W	
		0	STPB	0	H0	R/W	
0x5224	UA2BR (UART Ch.2 Baud-Rate Register)	15–12	–	0x0	–	R	–
		11–8	FMD[3:0]	0x0	H0	R/W	
		7–0	BRT[7:0]	0x00	H0	R/W	
0x5226	UA2CTL (UART Ch.2 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5228	UA2TXD (UART Ch.2 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x522a	UA2RXD (UART Ch.2 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x522c	UA2INTF (UART Ch.2 Status and Interrupt Flag Register)	15–10	–	0x00	–	R	–
		9	RBSY	0	H0/S0	R	
		8	TBSY	0	H0/S0	R	
		7	–	0	–	R	
		6	TENDIF	0	H0/S0	R/W	Cleared by writing 1.
		5	FEIF	0	H0/S0	R/W	Cleared by writing 1 or reading the UA2RXD register.
		4	PEIF	0	H0/S0	R/W	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	RB2FIF	0	H0/S0	R	Cleared by reading the UA2RXD register.
		1	RB1FIF	0	H0/S0	R	
		0	TBEIF	1	H0/S0	R	Cleared by writing to the UA2TXD register.
0x522e	UA2INTE (UART Ch.2 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6	TENDIE	0	H0	R/W	
		5	FEIE	0	H0	R/W	
		4	PEIE	0	H0	R/W	
		3	OEIE	0	H0	R/W	
		2	RB2FIE	0	H0	R/W	
		1	RB1FIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x5260–0x526c 16-bit Timer (T16) Ch.2

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5260	T16_2CLK (T16 Ch.2 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5262	T16_2MOD (T16 Ch.2 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x5264	T16_2CTL (T16 Ch.2 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5266	T16_2TR (T16 Ch.2 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x5268	T16_2TC (T16 Ch.2 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x526a	T16_2INTF (T16 Ch.2 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x526c	T16_2INTE (T16 Ch.2 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x5270–0x527a Synchronous Serial Interface (SPIA) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5270	SPI1MOD (SPIA Ch.1 Mode Register)	15–12	–	0x0	–	R	–
		11–8	CHLN[3:0]	0x7	H0	R/W	
		7–6	–	0x0	–	R	
		5	PUEN	0	H0	R/W	
		4	NOCLKDIV	0	H0	R/W	
		3	LSBFST	0	H0	R/W	
		2	CPHA	0	H0	R/W	
		1	CPOL	0	H0	R/W	
		0	MST	0	H0	R/W	
0x5272	SPI1CTL (SPIA Ch.1 Control Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5274	SPI1TXD (SPIA Ch.1 Transmit Data Register)	15–0	TXD[15:0]	0x0000	H0	R/W	–
0x5276	SPI1RXD (SPIA Ch.1 Receive Data Register)	15–0	RXD[15:0]	0x0000	H0	R	–
0x5278	SPI1INTF (SPIA Ch.1 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7	BSY	0	H0	R	
		6–4	–	0x0	–	R	
		3	OEIF	0	H0/S0	R/W	Cleared by writing 1.
		2	TENDIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the SPI1RXD register.
		0	TBEIF	1	H0/S0	R	Cleared by writing to the SPI1TXD register.
0x527a	SPI1INTE (SPIA Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–4	–	0x0	–	R	
		3	OEIE	0	H0	R/W	
		2	TENDIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x52c0–0x52d2 I²C (I2C) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x52c0	I2C1CLK (I2C Ch.1 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–6	–	0x0	–	R	
		5–4	CLKDIV[1:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x52c2	I2C1MOD (I2C Ch.1 Mode Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2	OADR10	0	H0	R/W	
		1	GCEN	0	H0	R/W	
		0	–	0	–	R	
0x52c4	I2C1BR (I2C Ch.1 Baud-Rate Register)	15–8	–	0x00	–	R	–
		7	–	0	–	R	
		6–0	BRT[6:0]	0x7f	H0	R/W	
0x52c8	I2C1OADR (I2C Ch.1 Own Address Register)	15–10	–	0x00	–	R	–
		9–0	OADR[9:0]	0x000	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x52ca	I2C1CTL (I2C Ch.1 Control Register)	15–8	–	0x00	–	R	–
		7–6	–	0x0	–	R	
		5	MST	0	H0	R/W	
		4	TXNACK	0	H0/S0	R/W	
		3	TXSTOP	0	H0/S0	R/W	
		2	TXSTART	0	H0/S0	R/W	
		1	SFTRST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x52cc	I2C1TXD (I2C Ch.1 Transmit Data Register)	15–8	–	0x00	–	R	–
		7–0	TXD[7:0]	0x00	H0	R/W	
0x52ce	I2C1RXD (I2C Ch.1 Receive Data Register)	15–8	–	0x00	–	R	–
		7–0	RXD[7:0]	0x00	H0	R	
0x52d0	I2C1INTF (I2C Ch.1 Status and Interrupt Flag Register)	15–13	–	0x0	–	R	–
		12	SDALOW	0	H0	R	
		11	SCLLOW	0	H0	R	
		10	BSY	0	H0/S0	R	
		9	TR	0	H0	R	
		8	–	0	–	R	
		7	BYTEENDIF	0	H0/S0	R/W	Cleared by writing 1.
		6	GCIF	0	H0/S0	R/W	
		5	NACKIF	0	H0/S0	R/W	
		4	STOPIF	0	H0/S0	R/W	
		3	STARTIF	0	H0/S0	R/W	
		2	ERRIF	0	H0/S0	R/W	
		1	RBFIF	0	H0/S0	R	Cleared by reading the I2C1RXD register.
		0	TBEIF	0	H0/S0	R	Cleared by writing to the I2C1TXD register.
0x52d2	I2C1INTE (I2C Ch.1 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7	BYTEENDIE	0	H0	R/W	
		6	GCIE	0	H0	R/W	
		5	NACKIE	0	H0	R/W	
		4	STOPIE	0	H0	R/W	
		3	STARTIE	0	H0	R/W	
		2	ERRIE	0	H0	R/W	
		1	RBFIE	0	H0	R/W	
		0	TBEIE	0	H0	R/W	

0x5320–0x5332 IR Remote Controller (REMC2)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5320	REMCLK (REMC2 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5322	REMDBCTL (REMC2 Data Bit Counter Control Register)	15–10	–	0x00	–	R	–
		9	PRESET	0	H0/S0	R/W	Cleared by writing 1 to the REMDBCTL.REMCRST bit.
		8	PRUN	0	H0/S0	R/W	
		7–5	–	0x0	–	R	–
		4	REMOINV	0	H0	R/W	
		3	BUFEN	0	H0	R/W	
		2	TRMD	0	H0	R/W	
		1	REMCRST	0	H0	W	
		0	MODEN	0	H0	R/W	

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5324	REMDBCNT (REMC2 Data Bit Counter Register)	15–0	DBCNT[15:0]	0x0000	H0/S0	R	Cleared by writing 1 to the REMDBCTL.REMCRST bit.
0x5326	REMAPLEN (REMC2 Data Bit Active Pulse Length Register)	15–0	APLEN[15:0]	0x0000	H0	R/W	Writing enabled when REMDBCTL.MODEN bit = 1.
0x5328	REMDBLEN (REMC2 Data Bit Length Register)	15–0	DBLEN[15:0]	0x0000	H0	R/W	Writing enabled when REMDBCTL.MODEN bit = 1.
0x532a	REMINTF (REMC2 Status and Interrupt Flag Register)	15–11	–	0x00	–	R	–
		10	DBCNTRUN	0	H0/S0	R	Cleared by writing 1 to the REMDBCTL.REMCRST bit.
		9	DBLENBSY	0	H0	R	Effective when the REMDBCTL.BUFEN bit = 1.
		8	APLENBSY	0	H0	R	
		7–2	–	0x00	–	R	–
		1	DBIF	0	H0/S0	R/W	Cleared by writing 1 to this bit or the REMDBCTL.REMCRST bit.
		0	APIF	0	H0/S0	R/W	
0x532c	REMINTE (REMC2 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–2	–	0x00	–	R	
		1	DBIE	0	H0	R/W	
		0	APIE	0	H0	R/W	
0x5330	REMCARR (REMC2 Carrier Waveform Register)	15–8	CRDTY[7:0]	0x00	H0	R/W	–
		7–0	CRPER[7:0]	0x00	H0	R/W	
0x5332	REMCCTL (REMC2 Carrier Modulation Control Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	CARREN	0	H0	R/W	

0x5480–0x548c 16-bit Timer (T16) Ch.3

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x5480	T16_3CLK (T16 Ch.3 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x5482	T16_3MOD (T16 Ch.3 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x5484	T16_3CTL (T16 Ch.3 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x5486	T16_3TR (T16 Ch.3 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x5488	T16_3TC (T16 Ch.3 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x548a	T16_3INTF (T16 Ch.3 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x548c	T16_3INTE (T16 Ch.3 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x54a2–0x54ba 10-bit A/D Converter (ADC10A) Ch.0

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54a2	ADC10_0CTL (ADC10A Ch.0 Control Register)	15	–	0	–	R	–
		14–12	ADSTAT[2:0]	0x0	H0	R	
		11	–	0	–	R	
		10	BSYSTAT	0	H0	R	
		9–8	–	0x0	–	R	
		7–5	–	0x0	–	R	
		4	TRGEN	0	H0	R/W	
		3–2	–	0x0	–	R	
		1	ADST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x54a4	ADC10_0TRG (ADC10A Ch.0 Trigger/Analog Input Select Register)	15–14	–	0x0	–	R	–
		13–11	ENDAIN[2:0]	0x0	H0	R/W	
		10–8	STAAIN[2:0]	0x0	H0	R/W	
		7	STMD	0	H0	R/W	
		6	CNVMD	0	H0	R/W	
		5–4	CNVTRG[1:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	SMPCLK[2:0]	0x5	H0	R/W	
0x54a6	ADC10_0CFG (ADC10A Ch.0 Configuration Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2–0	VRANGE[2:0]	0x4	H0	R/W	
0x54a8	ADC10_0INTF (ADC10A Ch.0 Interrupt Flag Register)	15	AD7OVIF	0	H0	R/W	Cleared by writing 1.
		14	AD6OVIF	0	H0	R/W	
		13	AD5OVIF	0	H0	R/W	
		12	AD4OVIF	0	H0	R/W	
		11	AD3OVIF	0	H0	R/W	
		10	AD2OVIF	0	H0	R/W	
		9	AD1OVIF	0	H0	R/W	
		8	AD0OVIF	0	H0	R/W	
		7	AD7CIF	0	H0	R/W	
		6	AD6CIF	0	H0	R/W	
		5	AD5CIF	0	H0	R/W	
		4	AD4CIF	0	H0	R/W	
		3	AD3CIF	0	H0	R/W	
		2	AD2CIF	0	H0	R/W	
		1	AD1CIF	0	H0	R/W	
		0	AD0CIF	0	H0	R/W	
0x54aa	ADC10_0INTE (ADC10A Ch.0 Interrupt Enable Register)	15	AD7OVIE	0	H0	R/W	–
		14	AD6OVIE	0	H0	R/W	
		13	AD5OVIE	0	H0	R/W	
		12	AD4OVIE	0	H0	R/W	
		11	AD3OVIE	0	H0	R/W	
		10	AD2OVIE	0	H0	R/W	
		9	AD1OVIE	0	H0	R/W	
		8	AD0OVIE	0	H0	R/W	
		7	AD7CIE	0	H0	R/W	
		6	AD6CIE	0	H0	R/W	
		5	AD5CIE	0	H0	R/W	
		4	AD4CIE	0	H0	R/W	
		3	AD3CIE	0	H0	R/W	
		2	AD2CIE	0	H0	R/W	
		1	AD1CIE	0	H0	R/W	
		0	AD0CIE	0	H0	R/W	
0x54ac	ADC10_0AD0D (ADC10A Ch.0 Result Register 0)	15–0	AD0D[15:0]	0x0000	H0	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54ae	ADC10_0AD1D (ADC10A Ch.0 Result Register 1)	15–0	AD1D[15:0]	0x0000	H0	R	–
0x54b0	ADC10_0AD2D (ADC10A Ch.0 Result Register 2)	15–0	AD2D[15:0]	0x0000	H0	R	–
0x54b2	ADC10_0AD3D (ADC10A Ch.0 Result Register 3)	15–0	AD3D[15:0]	0x0000	H0	R	–
0x54b4	ADC10_0AD4D (ADC10A Ch.0 Result Register 4)	15–0	AD4D[15:0]	0x0000	H0	R	–
0x54b6	ADC10_0AD5D (ADC10A Ch.0 Result Register 5)	15–0	AD5D[15:0]	0x0000	H0	R	–
0x54b8	ADC10_0AD6D (ADC10A Ch.0 Result Register 6)	15–0	AD6D[15:0]	0x0000	H0	R	–
0x54ba	ADC10_0AD7D (ADC10A Ch.0 Result Register 7)	15–0	AD7D[15:0]	0x0000	H0	R	–

0x54c0–0x54cc 16-bit Timer (T16) Ch.4

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54c0	T16_4CLK (T16 Ch.4 Clock Control Register)	15–9	–	0x00	–	R	–
		8	DBRUN	0	H0	R/W	
		7–4	CLKDIV[3:0]	0x0	H0	R/W	
		3–2	–	0x0	–	R	
		1–0	CLKSRC[1:0]	0x0	H0	R/W	
0x54c2	T16_4MOD (T16 Ch.4 Mode Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	TRMD	0	H0	R/W	
0x54c4	T16_4CTL (T16 Ch.4 Control Register)	15–9	–	0x00	–	R	–
		8	PRUN	0	H0	R/W	
		7–2	–	0x00	–	R	
		1	PRESET	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x54c6	T16_4TR (T16 Ch.4 Reload Data Register)	15–0	TR[15:0]	0xffff	H0	R/W	–
0x54c8	T16_4TC (T16 Ch.4 Counter Data Register)	15–0	TC[15:0]	0xffff	H0	R	–
0x54ca	T16_4INTF (T16 Ch.4 Interrupt Flag Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIF	0	H0	R/W	Cleared by writing 1.
0x54cc	T16_4INTE (T16 Ch.4 Interrupt Enable Register)	15–8	–	0x00	–	R	–
		7–1	–	0x00	–	R	
		0	UFIE	0	H0	R/W	

0x54e2–0x54fa 10-bit A/D Converter (ADC10A) Ch.1

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54e2	ADC10_1CTL (ADC10A Ch.1 Control Register)	15	–	0	–	R	–
		14–12	ADSTAT[2:0]	0x0	H0	R	
		11	–	0	–	R	
		10	BSYSTAT	0	H0	R	
		9–8	–	0x0	–	R	
		7–5	–	0x0	–	R	
		4	TRGEN	0	H0	R/W	
		3–2	–	0x0	–	R	
		1	ADST	0	H0	R/W	
		0	MODEN	0	H0	R/W	
0x54e4	ADC10_1TRG (ADC10A Ch.1 Trigger/Analog Input Select Register)	15–14	–	0x0	–	R	–
		13–11	ENDAIN[2:0]	0x0	H0	R/W	
		10–8	STAAIN[2:0]	0x0	H0	R/W	
		7	STMD	0	H0	R/W	
		6	CNVMD	0	H0	R/W	
		5–4	CNVTRG[1:0]	0x0	H0	R/W	
		3	–	0	–	R	
		2–0	SMPCLK[2:0]	0x5	H0	R/W	
0x54e6	ADC10_1CFG (ADC10A Ch.1 Configuration Register)	15–8	–	0x00	–	R	–
		7–3	–	0x00	–	R	
		2–0	VRANGE[2:0]	0x4	H0	R/W	
0x54e8	ADC10_1INTF (ADC10A Ch.1 Interrupt Flag Register)	15	AD7OVIF	0	H0	R/W	Cleared by writing 1.
		14	AD6OVIF	0	H0	R/W	
		13	AD5OVIF	0	H0	R/W	
		12	AD4OVIF	0	H0	R/W	
		11	AD3OVIF	0	H0	R/W	
		10	AD2OVIF	0	H0	R/W	
		9	AD1OVIF	0	H0	R/W	
		8	AD0OVIF	0	H0	R/W	
		7	AD7CIF	0	H0	R/W	
		6	AD6CIF	0	H0	R/W	
		5	AD5CIF	0	H0	R/W	
		4	AD4CIF	0	H0	R/W	
		3	AD3CIF	0	H0	R/W	
		2	AD2CIF	0	H0	R/W	
		1	AD1CIF	0	H0	R/W	
		0	AD0CIF	0	H0	R/W	
0x54ea	ADC10_1INTE (ADC10A Ch.1 Interrupt Enable Register)	15	AD7OVIE	0	H0	R/W	–
		14	AD6OVIE	0	H0	R/W	
		13	AD5OVIE	0	H0	R/W	
		12	AD4OVIE	0	H0	R/W	
		11	AD3OVIE	0	H0	R/W	
		10	AD2OVIE	0	H0	R/W	
		9	AD1OVIE	0	H0	R/W	
		8	AD0OVIE	0	H0	R/W	
		7	AD7CIE	0	H0	R/W	
		6	AD6CIE	0	H0	R/W	
		5	AD5CIE	0	H0	R/W	
		4	AD4CIE	0	H0	R/W	
		3	AD3CIE	0	H0	R/W	
		2	AD2CIE	0	H0	R/W	
		1	AD1CIE	0	H0	R/W	
		0	AD0CIE	0	H0	R/W	
0x54ec	ADC10_1AD0D (ADC10A Ch.1 Result Register 0)	15–0	AD0D[15:0]	0x0000	H0	R	–

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0x54ee	ADC10_1AD1D (ADC10A Ch.1 Result Register 1)	15–0	AD1D[15:0]	0x0000	H0	R	–
0x54f0	ADC10_1AD2D (ADC10A Ch.1 Result Register 2)	15–0	AD2D[15:0]	0x0000	H0	R	–
0x54f2	ADC10_1AD3D (ADC10A Ch.1 Result Register 3)	15–0	AD3D[15:0]	0x0000	H0	R	–
0x54f4	ADC10_1AD4D (ADC10A Ch.1 Result Register 4)	15–0	AD4D[15:0]	0x0000	H0	R	–
0x54f6	ADC10_1AD5D (ADC10A Ch.1 Result Register 5)	15–0	AD5D[15:0]	0x0000	H0	R	–
0x54f8	ADC10_1AD6D (ADC10A Ch.1 Result Register 6)	15–0	AD6D[15:0]	0x0000	H0	R	–
0x54fa	ADC10_1AD7D (ADC10A Ch.1 Result Register 7)	15–0	AD7D[15:0]	0x0000	H0	R	–

0xffff90 Debugger (DBG)

Address	Register name	Bit	Bit name	Initial	Reset	R/W	Remarks
0xffff90	DBRAM (Debug RAM Base Register)	31–24	–	0x00	–	R	–
		23–0	DBRAM[23:0]	0x00 0fc0	H0	R	

Appendix B Power Saving

Current consumption will vary dramatically, depending on CPU operating mode, operation clock frequency, peripheral circuits being operated, and V_{D1} regulator operating mode. Listed below are the control methods for saving power.

B.1 Operating Status Configuration Examples for Power Saving

Table B.1.1 lists typical examples of operating status configuration with consideration given to power saving.

Table B.1.1 Typical Operating Status Configuration Examples

Operating status configuration	Current consumption	V_{D1}	OSC1	IOSC/ OSC3/ EXOSC	RTCA	CPU	Current consumption listed in electrical characteristics
Standby	↑ Low	Economy	OFF	OFF	OFF	SLEEP	I_{SLP}
Clock counting			ON		ON	SLEEP or HALT	I_{HALT2}
Low-speed processing						OSC1 RUN	I_{RUN20}
Peripheral circuit operations		Normal		ON		SLEEP or HALT	I_{HALT1}
High-speed processing	High ↓					IOSC/OSC3/EXOSC RUN	I_{RUN10}

If the current consumption order by the operating status configuration shown in Table B.1.1 is different from one that is listed in "Electrical Characteristics," check the settings shown below.

PWGVD1CTL.REGMODE[1:0] bits of the power generator

If the PWGVD1CTL.REGMODE[1:0] bits of the power generator is 0x2 (normal mode) when the CPU enters SLEEP mode, current consumption in SLEEP mode will be larger than I_{SLP} that is listed in "Electrical Characteristics." Set the PWGVD1CTL.REGMODE[1:0] bits to 0x3 (economy mode) or 0x0 (automatic mode) before executing the slp instruction.

CLGOSC.IOSCSLPC/OSC1SLPC/OSC3SLPC/EXOSCSLPC bits of the clock generator

Setting the CLGOSC.IOSCSLPC, OSC1SLPC, OSC3SLPC, or EXOSCSLPC bit of the clock generator to 0 disables the oscillator circuit stop control when the slp instruction is executed. To stop the oscillator circuits during SLEEP mode, set these bits to 1.

MODEN bits of the peripheral circuits

Setting the MODEN bit of each peripheral circuit to 1 starts supplying the operating clock enabling the peripheral circuit to operate. To reduce current consumption, set the MODEN bits of unnecessary peripheral circuits to 0. Note that the real-time clock has no MODEN bit, therefore, current consumption does not vary if it is counting or idle.

OSC1 oscillator circuit configurations

The OSC1 oscillator circuit provides some configuration items to support various crystal resonators with ranges from cylinder type through surface-mount type. These configurations trade off current consumption for performance as shown below.

- The lower oscillation inverter gain setting (CLGOSC1.INV1B[1:0]/INV1N[1:0] bits) decreases current consumption.
- The lower OSC1 internal gate capacitance setting (CLGOSC1.CGI1[2:0] bits) decreases current consumption.
- Using lower OSC1 external gate and drain capacitances decreases current consumption.
- Using a crystal resonator with lower C_L value decreases current consumption.

However, these configurations may reduce the oscillation margin and increase the frequency error, therefore, be sure to perform matching evaluation using the actual printed circuit board.

OSC3 (crystal/ceramic) oscillator circuit configurations

The OSC3 (crystal/ceramic) oscillator circuit provides some configuration items to support various crystal and ceramic resonators. These configurations trade off current consumption for performance as shown below.

- The lower oscillation inverter gain setting (CLGOSC3.OSC3INV[1:0] bits) decreases current consumption.
- Using lower OSC3 external gate and drain capacitances decreases current consumption.
- Using a resonator with lower C_L value decreases current consumption.

However, these configurations may reduce the oscillation margin and increase the frequency error, therefore, be sure to perform matching evaluation using the actual printed circuit board.

B.2 Other Power Saving Methods

Supply voltage detector configuration

Continuous operation mode (SVDCTL.SVDMD[1:0] bits = 0x0) always detects the power supply voltage, therefore, it increases current consumption. Set the supply voltage detector to intermittent operation mode or turn it on only when required.

Appendix C Mounting Precautions

This section describes various precautions for circuit board design and IC mounting.

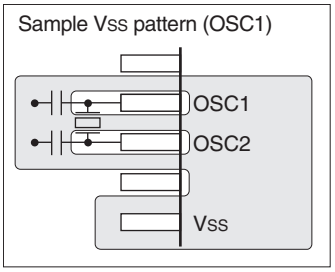
OSC1/OSC3 oscillator circuit

- Oscillation characteristics depend on factors such as components used (resonator, CG, CD) and circuit board patterns. In particular, with crystal resonators, select the appropriate capacitors (CG, CD) only after fully evaluating components actually mounted on the circuit board.
- Oscillator clock disturbances caused by noise may cause malfunctions. To prevent such disturbances, consider the following points.

(1) Components such as a resonator, resistors, and capacitors connected to the OSC1 (OSC3) and OSC2 (OSC4) pins should have the shortest connections possible.

(2) Wherever possible, avoid locating digital signal lines within 3 mm of the OSC1 (OSC3) and OSC2 (OSC4) pins or related circuit components and wiring. Rapidly-switching signals, in particular, should be kept at a distance from these components. Since the spacing between layers of multi-layer printed circuit boards is a mere 0.1 mm to 0.2 mm, the above precautions also apply when positioning digital signal lines on other layers.
Never place digital signal lines alongside such components or wiring, even if more than 3 mm distance or located on other layers. Avoid crossing wires.

(3) Use VSS to shield the OSC1 (OSC3) and OSC2 (OSC4) pins and related wiring (including wiring for adjacent circuit board layers). Layers wired should be adequately shielded as shown to the right. Fully ground adjacent layers, where possible. At minimum, shield the area at least 5 mm around the above pins and wiring.
Even after implementing these precautions, avoid configuring digital signal lines in parallel, as described in (2) above. Avoid crossing even on discrete layers, except for lines carrying signals with low switching frequencies.



(4) After implementing these precautions, check the FOUT pin output clock waveform by running the actual application program within the product.
For the OSC1 waveform, enlarge the areas before and after the clock rising and falling edges and take special care to confirm that the regions approximately 100 ns to either side are free of clock or spiking noise. For the OSC3 waveform, confirm that the frequency is as designed, is free of noise, and has minimal jitter.

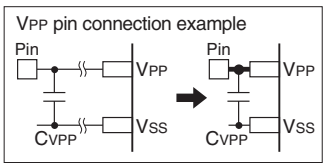
Failure to observe precautions (1) to (3) adequately may lead to noise in OSC1CLK and jitter in OSC3CLK. Noise in the OSC1CLK will destabilize timers that use OSC1CLK as well as CPU Core operations. Jitter in the OSC3 output will reduce operating frequencies.

#RESET pin

Components such as a switch and resistor connected to the #RESET pin should have the shortest connections possible to prevent noise-induced resets.

VPP pin

If fluctuations in the Flash programming voltage VPP is large, connect a capacitor CVPP between the VSS and VPP pins to suppress fluctuations within VPP ± 1 V. The CVPP should be placed as close to the VPP pin as possible and use a sufficiently thick wiring pattern that allows current of several tens of mA to flow.

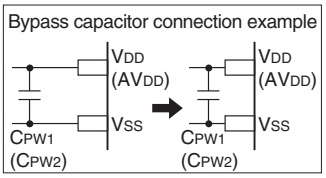


Power supply circuit

Sudden power supply fluctuations due to noise will cause malfunctions. Consider the following issues.

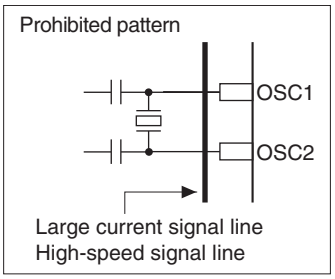
(1) Connections from the power supply to the VDD (AVDD) and VSS pins should be implemented via the shortest, thickest patterns possible.

(2) If a bypass capacitor is connected between VDD (AVDD) and VSS, connections between the VDD (AVDD) and VSS pins should be as short as possible.



Signal line location

- To prevent electromagnetically-induced noise arising from mutual induction, large-current signal lines should not be positioned close to pins susceptible to noise, such as oscillator and analog measurement pins.
- Locating signal lines in parallel over significant distances or crossing signal lines operating at high speed will cause malfunctions due to noise generated by mutual interference.
- The SEG/COM lines and voltage boost/reduce capacitor drive lines are more likely to generate noise, therefore keep a distance between the lines and pins susceptible to noise.



Handling of light (for bare chip mounting)

The characteristics of semiconductor components can vary when exposed to light. ICs may malfunction or non-volatile memory data may be corrupted if ICs are exposed to light.
Consider the following precautions for circuit boards and products in which this IC is mounted to prevent IC malfunctions attributable to light exposure.

(1) Design and mount the product so that the IC is shielded from light during use.

(2) Shield the IC from light during inspection processes.

(3) Shield the IC on the upper, underside, and side faces of the IC chip.

(4) Mount the IC chip within one week of opening the package. If the IC chip must be stored before mounting, take measures to ensure light shielding.

(5) Adequate evaluations are required to assess nonvolatile memory data retention characteristics before product delivery if the product is subjected to heat stress exceeding regular reflow conditions during mounting processes.

Unused pins

(1) I/O port (P) pins
Unused pins should be left open. The control registers should be fixed at the initial status.

(2) OSC1, OSC2, OSC3, OSC4, and EXOSC pins
If the OSC1 oscillator circuit, OSC3 oscillator circuit or EXOSC input circuit is not used, the OSC1 and OSC2 pins, the OSC3 and OSC4 pins, or the EXOSC pin should be left open. The control registers should be fixed at the initial status (disabled).

Miscellaneous

Minor variations over time may result in electrical damage arising from disturbances in the form of voltages exceeding the absolute maximum rating when mounting the product in addition to physical damage. The following factors can give rise to these variations:

(1) Electromagnetically-induced noise from industrial power supplies used in mounting reflow, reworking after mounting, and individual characteristic evaluation (testing) processes
(2) Electromagnetically-induced noise from a solder iron when soldering

In particular, during soldering, take care to ensure that the soldering iron GND (tip potential) has the same potential as the IC GND.

Appendix D Measures Against Noise

To improve noise immunity, take measures against noise as follows:

Noise Measures for V_{DD}, AV_{DD}, and V_{SS} Power Supply Pins

When noise falling below the rated voltage is input, an IC malfunction may occur. If desired operations cannot be achieved, take measures against noise on the circuit board, such as designing close patterns for circuit board power supply circuits, adding noise-filtering decoupling capacitors, and adding surge/noise prevention components on the power supply line.
For the recommended patterns on the circuit board, see "Mounting Precautions" in Appendix.

Noise Measures for #RESET Pin

If noise is input to the #RESET pin, the IC may be reset. Therefore, the circuit board must be designed properly taking noise measures into consideration.
For the recommended patterns on the circuit board, see "Mounting Precautions" in Appendix.

Noise Measures for Oscillator Pins

The oscillator input pins must pass a signal of small amplitude, so they are hypersensitive to noise. Therefore, the circuit board must be designed properly taking noise measures into consideration.
For the recommended patterns on the circuit board, see "Mounting Precautions" in Appendix.

Noise Measures for Debug Pins

This product provides the input/output pins (DCLK, DST2, and DSIO) to connect ICDmini (S5U1C17001H) for debugging. If noise is input to these pins with the debugging function enabled, the S1C17 Core may enter DEBUG mode. To prevent unexpected transitions to DEBUG mode caused by extraneous noise, switch the DCLK, DST2, and DSIO pins to general-purpose I/O port pins within the initialization routine when the debug functions are not used.
For details of the pin functions and the function switch control, see the "I/O Ports" chapter.

Note: Do not perform the function switching shown above when the application is under development, as the debug functions must be used. The debugging cannot be performed after the pin function is switched. The above processing must be added after the application development has completed and debugging is no longer necessary.

The DSIO pin should be pulled up with a 10 kΩ resistor when using the debug pin functions.

Noise Measures for Interrupt Input Pins

This product is able to generate a port input interrupt when the input signal changes. The interrupt is generated when an input signal edge is detected, therefore, an interrupt may occur if the signal changes due to extraneous noise. To prevent occurrence of unexpected interrupts due to extraneous noise, enable the chattering filter circuit when using the port input interrupt.
For details of the port input interrupt and chattering filter circuit, see the "I/O Ports" chapter.

Noise Measures for UART Pins

This product includes a UART for asynchronous communications. The UART starts receive operation when it detects a low level input from the SIN*n* pin. Therefore, a receive operation may be started if the SIN*n* pin is set to low due to extraneous noise. In this case, a receive error will occur or invalid data will be received.
To prevent the UART from malfunction caused by extraneous noise, take the following measures:

- Stop the UART operations while asynchronous communication is not performed.
- Execute the resending process via software after executing the receive error handler with a parity check.

For details of the pin functions and the function switch control, see the "I/O Ports" chapter. For the UART control and details of receive errors, see the "UART" chapter.

Appendix E Initialization Routine

The following lists typical vector tables and initialization routines:

boot.s

```
.org    0x8000
.section .rodata                                                          ...(1)

; ======================================================================
;       Vector table
; ======================================================================
                                ; interrupt  vector  interrupt
                                ; number     offset  source

.long BOOT                      ; 0x00       0x00    reset                ...(2)
.long unalign_handler           ; 0x01       0x04    unalign
.long nmi_handler               ; 0x02       0x08    NMI
.long int03_handler             ; 0x03       0x0c    -
.long svd_handler               ; 0x04       0x10    SVD
.long pport_handler             ; 0x05       0x14    PPORT
.long int06_handler             ; 0x06       0x18    -
.long clg_handler               ; 0x07       0x1c    CLG
.long rtca_handler              ; 0x08       0x20    RTCA
.long t16_0_handler             ; 0x09       0x24    T16 ch0
.long uart_0_handler            ; 0x0a       0x28    UART ch0
.long t16_1_handler             ; 0x0b       0x2c    T16 ch1
.long spia_0_handler            ; 0x0c       0x30    SPIA ch0
.long i2c_0_handler             ; 0x0d       0x34    I2C ch0
.long t16b_0_handler            ; 0x0e       0x38    T16B ch0
.long t16b_1_handler            ; 0x0f       0x3c    T16B ch1
.long t16b_2_handler            ; 0x10       0x40    T16B ch2
.long t16b_3_handler            ; 0x11       0x44    T16B ch3
.long t16_5_handler             ; 0x12       0x48    T16 ch5
.long uart_1_handler            ; 0x13       0x4c    UART ch1
.long t16_2_handler             ; 0x14       0x50    T16 ch2
.long spia_1_handler            ; 0x15       0x54    SPIA ch1
.long i2c_1_handler             ; 0x16       0x58    I2C ch1
.long remc2_handler             ; 0x17       0x5c    REMC2
.long t16_3_handler             ; 0x18       0x60    T16 ch3
.long ADC10a_0_handler          ; 0x19       0x64    ADC10A ch0
.long t16_4_handler             ; 0x1a       0x68    T16 ch4
.long ADC10a_1_handler          ; 0x1b       0x6c    ADC10A ch1
.long uart_2_handler            ; 0x1c       0x70    UART ch2
.long int1d_handler             ; 0x1d       0x74    -
.long int1e_handler             ; 0x1e       0x78    -
.long int1f_handler             ; 0x1f       0x7c    -

; ======================================================================
;       Program code
; ======================================================================

.text                                                                     ...(3)
.align 1

BOOT:
        ; ===== Initialize ============================================

        ; ----- Stack pointer --------------------
        Xld.a   %sp, 0x3fc0                                               ...(4)

        ; ----- Memory controller ----------------
        Xld.a   %r1, 0x41b0     ; FLASHC register address

        ; Flash read wait cycle
        Xld.a   %r0, 0x02       ; 0x02 = 2 wait
        ld.b    [%r1], %r0      ; [0x41b0] <= 0x02                        ...(5)

        ; ===== Main routine ==========================================
         ...
```

```
; ========================================================================
;       Interrupt handler
; ========================================================================
; ----- Address unalign --------------------------
unalign_handler:
        ...

; ----- NMI --------------------------------------
nmi_handler:
        ...
```

(1) A "`.rodata`" section is declared to locate the vector table in the "`.vector`" section.

(2) Interrupt handler routine addresses are defined as vectors.
"`int`*`XX`*`_handler`" can be used for software interrupts.

(3) The program code is written in the "`.text`" section.

(4) Sets the stack pointer.

(5) Sets the number of Flash memory read cycles.
(See the "Memory and Bus" chapter.)

Revision History

Code No.	Page	Contents
412959200	All	New establishment
412959201	1-2	1.1 Features Modified Table 1.1. Shipping form: A JEITA name was added to the package name.
	2-7	2.3.4 Operations Oscillation start time and oscillation stabilization waiting time Added the oscillation stabilization waiting time for the OSC1 oscillator circuit. The oscillation stabilization waiting time for the OSC1 oscillator circuit should be set to 16,384 OSC1CLK clocks or more.
	3-3	3.3.3 List of debugger input/output pins Added notes. Notes: • Do not drive the DCLK pin with a high level from outside (e.g. pulling up with a resistor). Also, do not connect (short-circuit) between the DCLK pin and another GPIO port. In the both cases, the IC may not start up normally due to unstable pin input/output status at power on. • Do not drive the DSIO pin with a low level from outside, as it generates a debug interrupt that puts the CPU into DEBUG mode.
	4-3	4.3.3 Flash Programming Modified Figure 4.3.3.1. C_{VPP} was changed to that must always be connected. Corrected the following description: C_{VPP} should be connected if the V_{PP} voltage is not stable due to the effect of the distance between the V_{PP} and Flash V_{CC} OUT or other causes. → When supplying the V_{PP} power source, be sure to connect C_{VPP} for stabilizing the V_{PP} voltage.
	6-22	6.7.12 Pd Port Group Modified Table 6.7.12.1. PDIOEN register: PDOEN[4:3], [1:0] → PDOEN[4:0]
	8-4	8.4 Control Registers WDT Control Register Corrected the description of the WDTRUN[3:0] bit. Bits 3–0 WDTRUN[3:0] These bits control WDT to run and stop. 0xa (WP): Stop Values other than 0xa (WP): Run 0xa (R): Idle 0x0 (R): Running
	9-2	9.3.2 Theoretical Regulation Function Corrected Step 1. 1. Measure f_{OSC1} and calculate the frequency tolerance correction value "m [ppm] = -{(f_{OSC1} - 32,768 [Hz]) / 32,768 [Hz]} × 10^6." (Eq. 9.1) m: OSC1 frequency tolerance correction value [ppm]
	9-4	9.4.2 Real-Time Clock Counter Operations Corrective operation when a value out of the effective range is set Added a note. Note: Do not set the RTCMON.RTCMOL[3:0] bits to 0x0 if the RTCMON.RTCMOH bit = 0.
	9-6	9.6 Control Registers RTC Control Register Bits 14–8 RTCTRM[6:0] Added a note. Notes: ... • Writing 0x00 to the RTCCTL.RTCTRM[6:0] bits sets the RTCCTL.RTCTRMBSY bit to 1 as well. However, no correcting operation is performed.
	9-11	9.6 Control Registers RTC Month/Day Register Bit 12 RTCMOH Bits 11–8 RTCMOL[3:0] Added a note. Notes: ... • Be sure to avoid setting the RTCMON.RTCMOH/RTCMOL[3:0] bits to 0x00.
	10-3	10.4.1 SVD Control Starting detection Corrected Step 4. 4. ... - Set the SVDINTE.SVDIE bit to 1.

REVISION HISTORY

Code No.	Page	Contents
412959201	14-7 to 8	14.4.3 Data Reception in Master Mode Data receiving procedure Added Step 1. (The old step numbers were carried down in order.) 1. When receiving one-byte data, write 1 to the I2C*n*CTL.TXNACK bit. Modified Figure 14.4.3.2. A flow for Step 1 was added.
	14-12 to 13	14.4.6 Data Reception in Slave Mode Data receiving procedure Added Step 1. (The old step numbers were carried down in order.) 1. When receiving one-byte data, write 1 to the I2C*n*CTL.TXNACK bit. Modified Figure 14.4.6.2. A flow for Step 1 was added.
	15-5	15.4.2 Counter Block Operations MAX counter data register Added a note. Note: When rewriting the MAX value, the new MAX value should be written after the counter has been reset to the previously set MAX value.
	19-1	19.1 Absolute Maximum Ratings Modified the characteristics table. V_I: #RESET was added to the condition.
	19-1	19.2 Recommended Operating Conditions Modified the characteristics table. C_{VPP}: ∗3 was deleted.
	20-1	20 Basic External Connection Diagram Modified the figure. C_{VPP} was changed to that must always be connected.
	21-1 to 2	21 Package A JEITA name was added to the package name.
	AP-A-13	Appendix A List of Peripheral Circuit Control Registers PDIOEN (Pd Port Enable Register) Modified the register table. PDOEN[4:3], [1:0] → PDOEN[4:0]

EPSON

International Sales Operations

America

Epson America, Inc.

Headquarter:
3840 Kilroy Airport Way
Long Beach, California 90806-2452 USA
Phone: +1-562-290-4677

San Jose Office:
214 Devcon Drive
San Jose, CA 95112 USA
Phone: +1-800-228-3964 or +1-408-922-0200

Europe

Epson Europe Electronics GmbH

Riesstrasse 15, 80992 Munich, Germany
Phone: +49-89-14005-0 Fax: +49-89-14005-110

Asia

Epson (China) Co., Ltd.

4th Floor, Tower 1 of China Central Place, 81 Jianguo Road,
Chaoyang District, Beijing 100025, China
Phone: +86-10-8522-1199 Fax: +86-10-8522-1120

Shanghai Branch

Room 1701 & 1704, 17 Floor, Greenland Center II,
562 Dong An Road, Xu Hui District, Shanghai, China
Phone: +86-21-5330-4888 Fax: +86-21-5423-4677

Shenzhen Branch

Room 804-805, 8 Floor, Tower 2, Ali Center, No.3331
Keyuan South RD (Shenzhen bay), Nanshan District,
Shenzhen 518054, China
Phone: +86-10-3299-0588 Fax: +86-10-3299-0560

Epson Taiwan Technology & Trading Ltd.

15F, No.100, Songren Rd, Sinyi Dist, Taipei City 110, Taiwan
Phone: +886-2-8786-6688

Epson Singapore Pte., Ltd.

1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 Fax: +65-6271-3182

Epson Korea Co., Ltd

10F Posco Tower Yeoksam, Teheranro 134 Gangnam-gu,
Seoul, 06235, Korea
Phone: +82-2-3420-6695

Seiko Epson Corp.
Sales & Marketing Division

Device Sales & Marketing Department

29th Floor, JR Shinjuku Miraina Tower, 4-1-6 Shinjuku,
Shinjuku-ku, Tokyo 160-8801, Japan

Document Code: 412959201
First issue March 2015
Revised May 2021 in JAPAN Ⓛ