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CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

S1C63003/004/008/016
Technical Manual

SEIKO EPSON CORPORATION

Rev. 1.1

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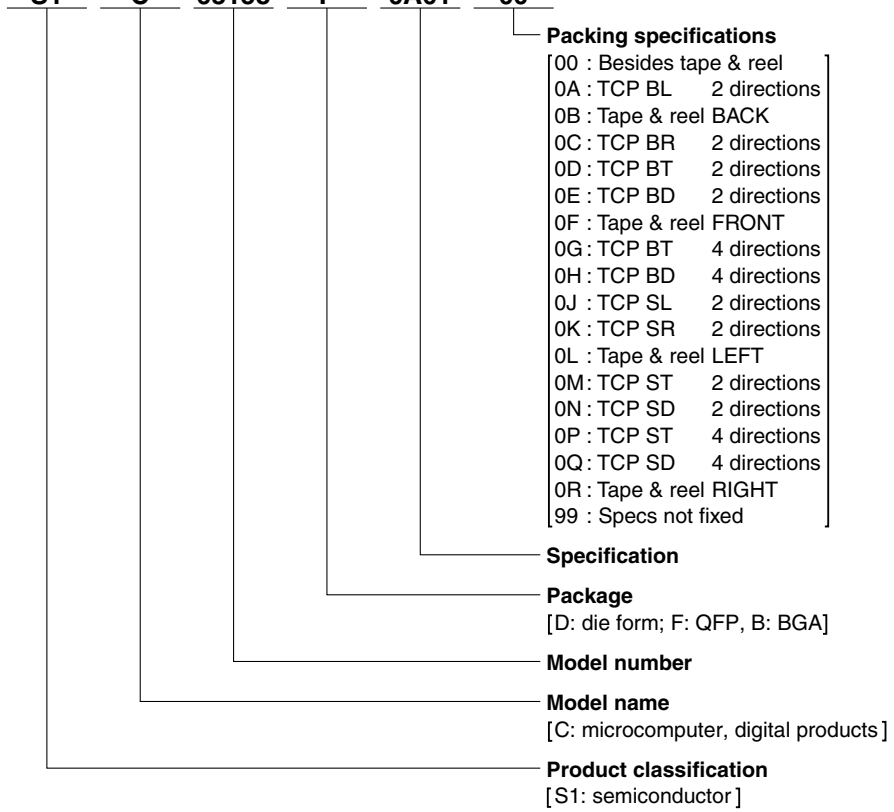
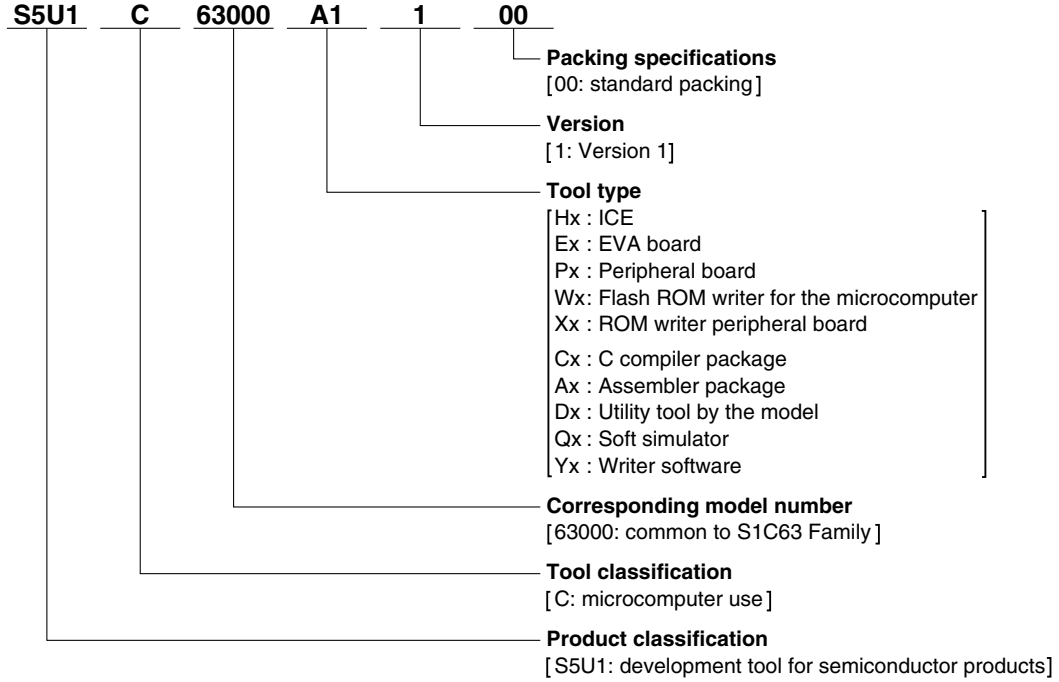
Configuration of product number

Devices



Development tools



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1 Outline

The S1C630 Series of 4-bit microcontrollers (S1C63003/004/008/016) features low voltage operations and low current consumption. It consists of a 4-bit core CPU S1C63000 as the core CPU, ROM (maximum 16K words × 13 bits), RAM (maximum 2K words × 4 bits), timers, and sound generator. It also incorporates a segment LCD controller/driver that can drive a maximum 56-segment × 8-common LCD panel, and an R/F converter that can measure temperature and humidity using sensors such as a thermistor.
The S1C630 Series is suitable for battery driven clocks and watches with temperature and humidity measurement functions.

* This manual describes the functions of four mask ROM models in S1C630 Series, S1C63016, S1C63008, S1C63004, and S1C63003. The descriptions are applied to all these four models unless otherwise specified.

1.1 Features

Table 1.1.1 Features of models

Function		S1C63016	S1C63008	S1C63004	S1C63003
Core		4-bit core CPU S1C63000			
OSC1 oscillation circuit		32.768 kHz (Typ.) crystal oscillation circuit			
OSC3 oscillation circuit		4.0 MHz (Typ., 3 V model)/1.0 MHz (Typ., 1.5 V model) ceramic oscillation circuit, 1.8 MHz (Typ., 3 V model)/500 kHz (Typ., 1.5 V model) CR oscillation circuit (external R), or 500 kHz (Typ., 3 V model)/500 kHz (Typ., 1.5 V model) CR oscillation circuit (built-in R) (*1)			550 kHz (Typ., 3 V model)/550 kHz (Typ., 1.5 V model) CR oscillation circuit (built-in R)
Instruction set		47 types of basic instructions (411 instructions with all), 8 types of addressing modes			
Instruction execution time		During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec			
ROM capacity	Code ROM	16,384 words × 13 bits	8,192 words × 13 bits	4,096 words × 13 bits	
	Data ROM	4,096 words × 4 bits	2,048 words × 4 bits	1,024 words × 4 bits	Not available
RAM capacity	Data memory	2,048 words × 4 bits	1,024 words × 4 bits	512 words × 4 bits	256 words × 4 bits
	Display memory	448 bits	400 bits	288 bits	110 bits
I/O ports		24 bits	24 bits	20 bits	16 bits
		Pull-down resistors can be included. (*1) The pins can be switched for peripheral circuit inputs/outputs. (*2)			
Serial interface		1 port (8-bit clock synchronous system with SPI supported)			Not available
LCD driver		56 segments (Max., *1) × 3 to 8 commons (*2)	50 segments (Max., *1) × 3 to 8 commons (*2)	36 segments (Max., *1) × 3 to 8 commons (*2)	22 segments (Max., *1) × 3 to 5 commons (*2)
Time base counters		Clock timer 1/1000-second stopwatch timer (with direct key input function)			Clock timer 1/1000-second stopwatch timer (without direct key input function)
Programmable timer		8-bit timer × 4 channels (Can be used as 16-bit timer × 2 or 16-bit timer × 1 + 8-bit timer × 2) (*2)	8-bit timer × 3 channels (Can be used as 16-bit timer × 1 + 8-bit timer × 1) (*2)		8-bit timer × 1 channel
Watchdog timer		Built-in			
Sound generator		With envelope and 1-shot output functions			
R/F converter		2 channels, CR oscillation type R/F converter with 20-bit counters, supports resistive humidity sensors.			
Integer multiplier		8-bit accumulator × 1 channel Multiplication: 8 bits × 8 bits → 16-bit product Division: 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder		Not available	
Supply voltage detection (SVD) circuit		Programmable 29 detection voltage levels (*2)			Not available
External interrupt					
	Key input	8 systems			4 systems
Internal interrupt					
	Watchdog timer	1 system (NMI)	1 system (NMI)		1 system (NMI)
	Clock timer	8 systems	8 systems		4 systems
	Stopwatch timer	4 systems	4 systems		2 systems
	Programmable timer	8 systems	6 systems		1 system
	Serial interface	1 system	1 system		–
	R/F converter	3 systems	3 systems		3 systems

Function		S1C63016	S1C63008	S1C63004	S1C63003
Power supply voltage		1.8 to 5.5 V (3 V normal type) or 1.1 to 1.7 V (1.5 V low-voltage type) (∗1)			
Operating temperature range		-40 to 85°C			
Current consumption (Typ.)	SLEEP (32 kHz)	0.1 µA (3 V model)/0.1 µA (1.5 V model)			
	HALT (32 kHz)	0.5 µA (3 V model)/0.5 µA (1.5 V model)			
	RUN (32 kHz)	2.3 µA (3 V model)/2.0 µA (1.5 V model)			
	RUN (4 M/1 MHz)	220 µA (4 MHz, 3 V model)/ 60 µA (1 MHz, 1.5 V model)			40 µA (550 kHz, 3 V model)/30 µA (550 kHz, 1.5 V model)
Shipment form		QFP15-100pin, TQFP14-100pin, or die form		QFP14-80pin, TQFP14-100pin, or die form	QFP12-48pin or die form

∗1: Can be selected with mask option. ∗2: Can be selected with software.

1.2 Block Diagram

S1C63016

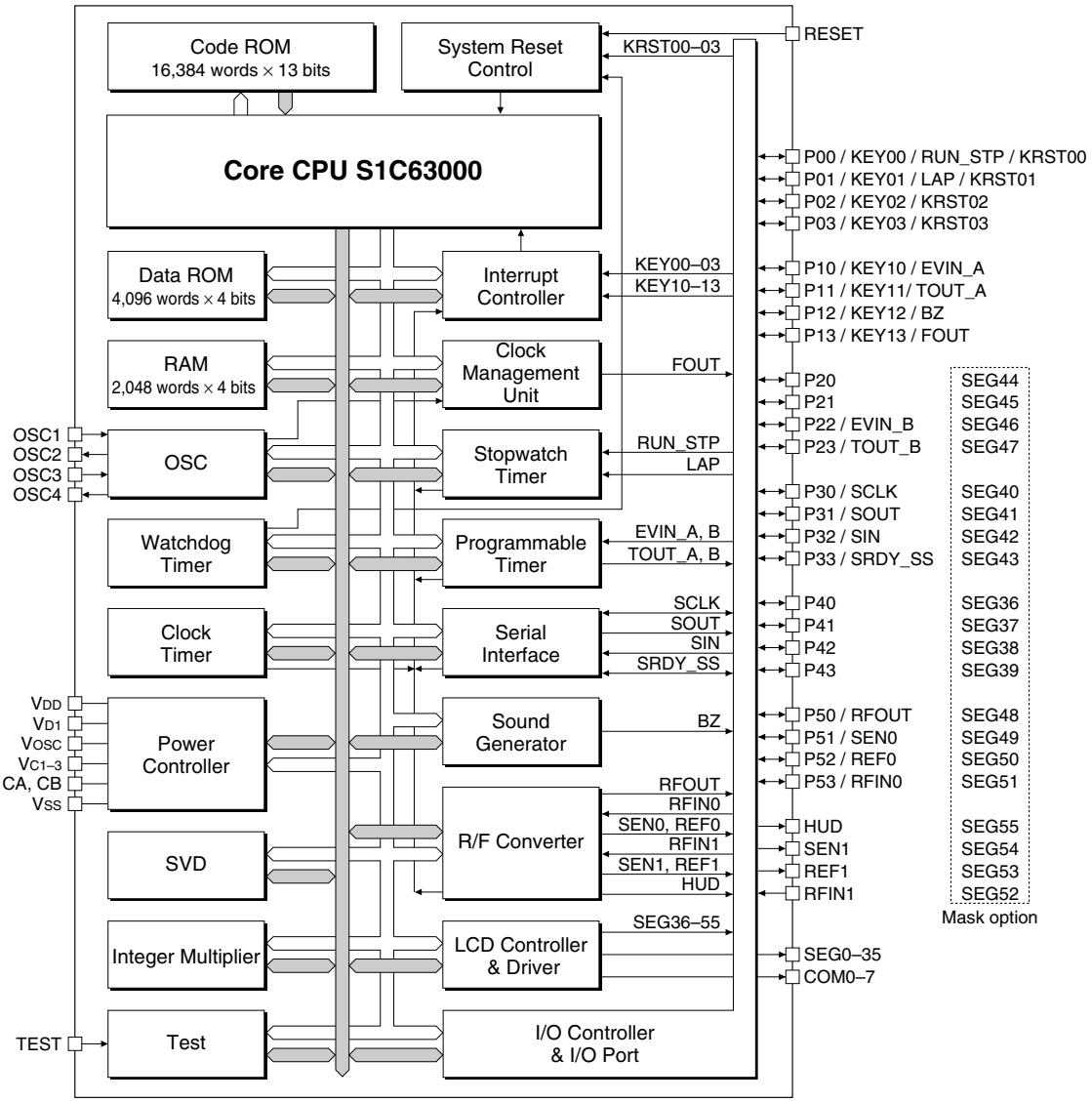


Figure 1.2.1 S1C63016 block diagram

S1C63008

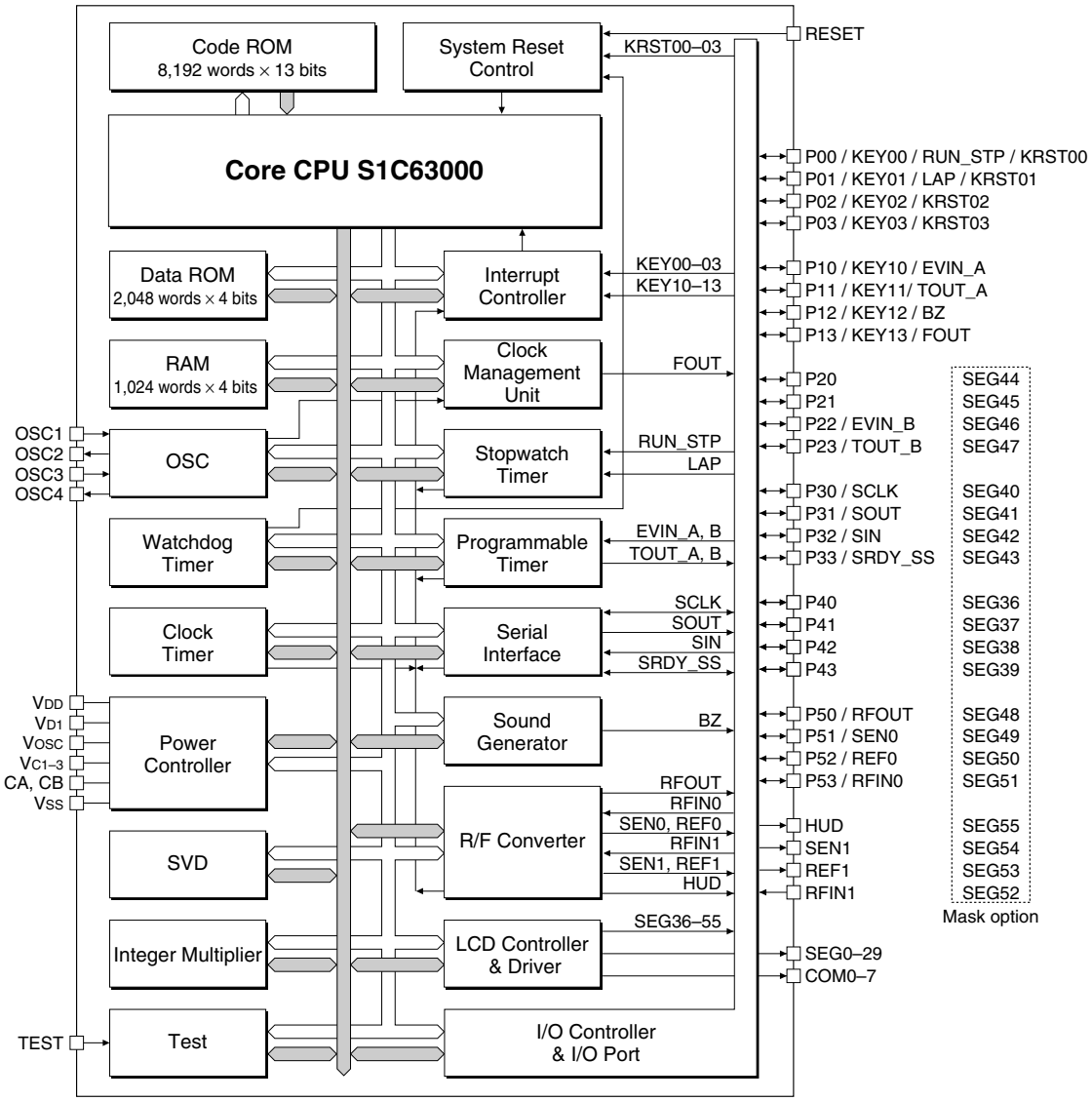


Figure 1.2.2 S1C63008 block diagram

S1C63004

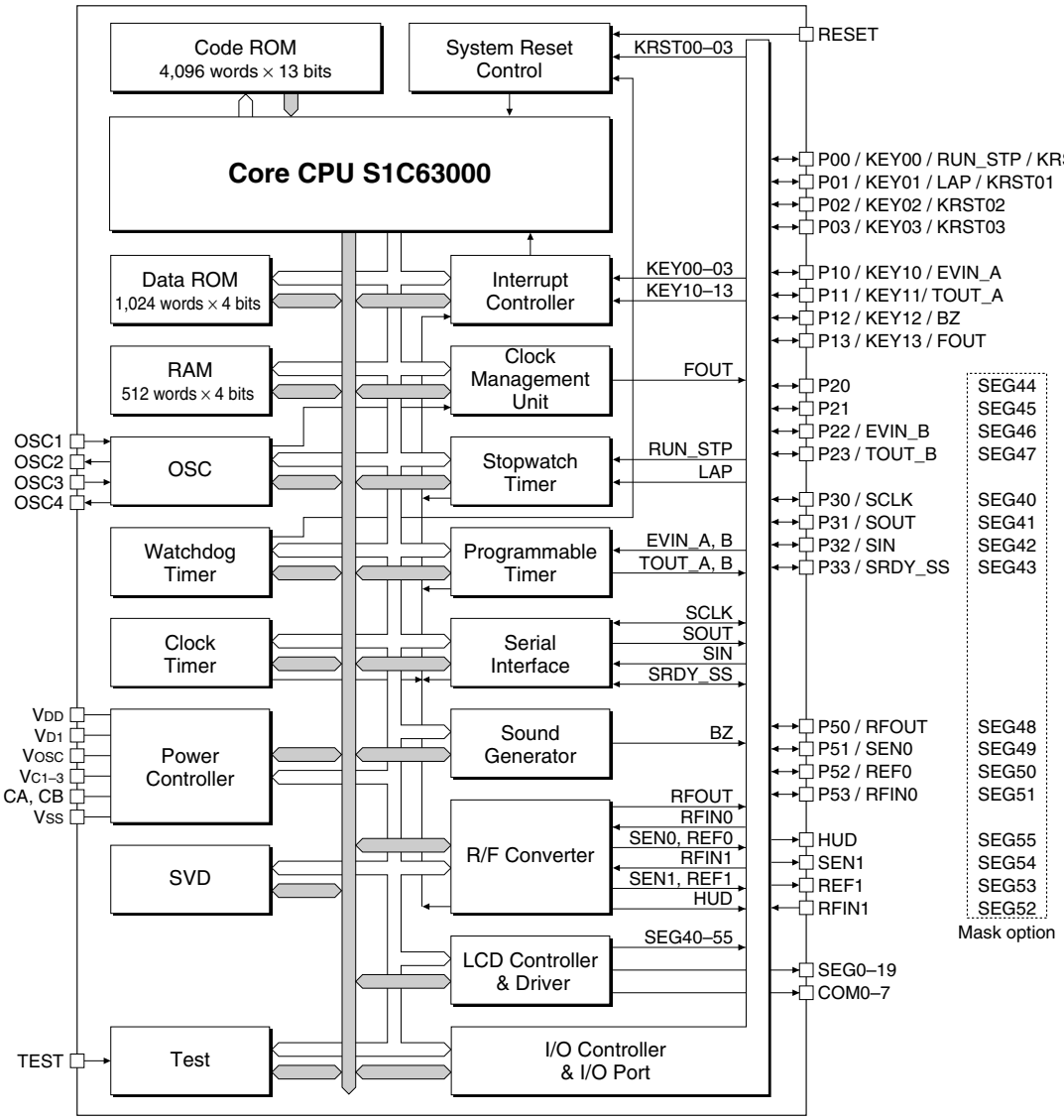


Figure 1.2.3 S1C63004 block diagram

S1C63003

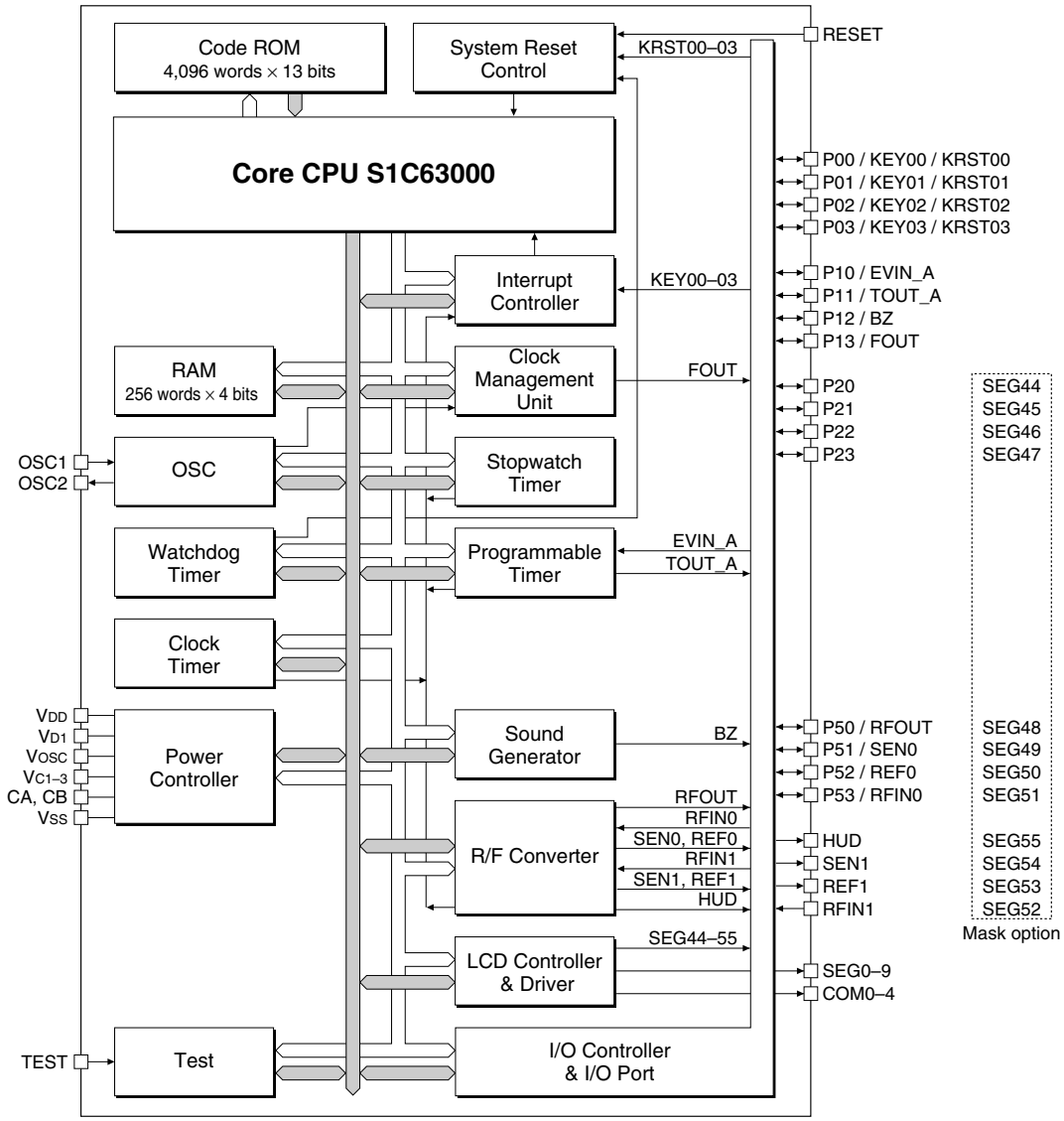


Figure 1.2.4 S1C63003 block diagram

1.3 Mask Option

S1C63003/004/008/016 provides the mask options shown below. Several hardware specifications are prepared in each optional item, and one of them can be selected according to the application. Use the function option generator "winfog" and segment option generator "winsog" provided as development tools for this selection. Mask pattern of the IC is finally generated based on the data created by winfog and winsog. Refer to the "S5U1C63000A Manual" for these tools.

<Outline of the mask option>

(1) Operating power voltage type

Either 3 V normal type (1.8 to 5.5 V) or 1.5 V low-voltage type (1.1 to 1.7 V) can be selected as the operating power voltage type.

(2) OSC3 oscillation circuit

In the S1C63004/008/016, the OSC3 oscillator type can be selected from ceramic oscillation, CR oscillation (external R) and CR oscillation (built-in R). The S1C63003 OSC3 oscillator type is fixed at CR oscillation (built-in R). Refer to "OSC3 Oscillation Circuit" in the "Oscillation Circuit and Clock Control" chapter for details.

(3) RESET terminal pull-down resistor

An internal pull-down resistor can be incorporated into the RESET port. Refer to "Reset Terminal (RESET)" in the "Initial Reset" chapter for details.

(4) SEG/GPIO/RFC selector

The I/O port (P20–P53) and R/F converter input/output pins are shared with the SEG terminals. This mask option allows selection of whether each of these pins are used for the I/O port or R/F converter or used for the SEG output. Refer to "Mask Option" in the "LCD Driver" chapter for details.

(5) I/O port pull-down resistor

An internal pull-down resistor that will be enabled in input mode can be incorporated into each I/O port (P00–P53). Refer to "Mask Option" in the "I/O Ports" chapter for details.

(6) Output specification of the I/O port

Either complementary output or P-channel open drain output can be selected as the output cell type of each I/O port (P00–P53). Refer to "Mask Option" in the "I/O Ports" chapter for details. Do not configure the P50–P53 ports to P-channel open drain output if the R/F converter (channel 0) is used.

(7) Multiple key entry reset function (by simultaneous high input to the P0x ports)

This option allows selection of whether the function to reset the IC by pressing multiple keys simultaneously is implemented or not. A combination of the P0x ports (P00–P03) to be used for this function can also be selected. Refer to "Simultaneous High Input to P0x Ports (P00–P03)" in the "Initial Reset" chapter for details.

(8) Time authorize circuit for the multiple key entry reset function

When the multiple key entry reset option (option (7)) is selected, the time authorize circuit can also be incorporated. The time authorize circuit measures the high pulse width of the simultaneous input signals and asserts the reset signal if it is longer than the predetermined time. This option is not available when the multiple key entry reset option is not selected. Refer to "Simultaneous High Input to P0x Ports (P00–P03)" in the "Initial Reset" chapter for details.

(9) LCD drive power supply

In the S1C63004/008/016, either the internal power supply or an external power supply can be selected as the LCD drive power source. When the internal power supply is selected, the reference voltage for boosting (V_{C1} or V_{C2}) can be set using a register. The S1C63003 LCD drive power source can also be selected from the internal power supply and an external power supply by mask option. When using the internal power supply, the reference voltage for boosting (V_{C1} or V_{C2}) should be selected by mask option. Refer to "Mask Option" in the "LCD Driver" chapter for details.

(10) LCD segment specification

The display memory bits can be allocated to a desired SEG terminal. It is also possible to set SEG terminals for DC output. Refer to "Mask Option" in the "LCD Driver" chapter for details.

Table 1.3.1 Option list (S1C63008/016)

Optional item		Option	
Operating power voltage		☐ 1. Normal Type (1.8–5.5 V)	☐ 2. Low Voltage Type (1.1–1.7 V)
OSC3 oscillation circuit		☐ 1. CR (built-in R) ☐ 2. CR (external R) ☐ 3. Ceramic (4.0 MHz)	
RESET terminal pull-down resistor		☐ 1. Use	☐ 2. Not Use
SEG/GPIO/RFC selector	P20	☐ 1. I/O	☐ 2. SEG
	P21	☐ 1. I/O	☐ 2. SEG
	P22	☐ 1. I/O	☐ 2. SEG
	P23	☐ 1. I/O	☐ 2. SEG
	P30	☐ 1. I/O	☐ 2. SEG
	P31	☐ 1. I/O	☐ 2. SEG
	P32	☐ 1. I/O	☐ 2. SEG
	P33	☐ 1. I/O	☐ 2. SEG
	P40	☐ 1. I/O	☐ 2. SEG
	P41	☐ 1. I/O	☐ 2. SEG
	P42	☐ 1. I/O	☐ 2. SEG
	P43	☐ 1. I/O	☐ 2. SEG
	P50	☐ 1. I/O	☐ 2. SEG
	P51	☐ 1. I/O	☐ 2. SEG
	P52	☐ 1. I/O	☐ 2. SEG
	P53	☐ 1. I/O	☐ 2. SEG
	RFIN1	☐ 1. RFC	☐ 2. SEG
	REF1	☐ 1. RFC	☐ 2. SEG
	SEN1	☐ 1. RFC	☐ 2. SEG
	HUD	☐ 1. RFC	☐ 2. SEG
I/O port pull-down resistor	P00	☐ 1. Use	☐ 2. Not Use
	P01	☐ 1. Use	☐ 2. Not Use
	P02	☐ 1. Use	☐ 2. Not Use
	P03	☐ 1. Use	☐ 2. Not Use
	P10	☐ 1. Use	☐ 2. Not Use
	P11	☐ 1. Use	☐ 2. Not Use
	P12	☐ 1. Use	☐ 2. Not Use
	P13	☐ 1. Use	☐ 2. Not Use
	P20	☐ 1. Use	☐ 2. Not Use
	P21	☐ 1. Use	☐ 2. Not Use
	P22	☐ 1. Use	☐ 2. Not Use
	P23	☐ 1. Use	☐ 2. Not Use
	P30	☐ 1. Use	☐ 2. Not Use
	P31	☐ 1. Use	☐ 2. Not Use
	P32	☐ 1. Use	☐ 2. Not Use
	P33	☐ 1. Use	☐ 2. Not Use
	P40	☐ 1. Use	☐ 2. Not Use
	P41	☐ 1. Use	☐ 2. Not Use
	P42	☐ 1. Use	☐ 2. Not Use
	P43	☐ 1. Use	☐ 2. Not Use
	P50	☐ 1. Use	☐ 2. Not Use
	P51	☐ 1. Use	☐ 2. Not Use
	P52	☐ 1. Use	☐ 2. Not Use
	P53	☐ 1. Use	☐ 2. Not Use
I/O port output specification	P00	☐ 1. Complementary	☐ 2. Pch Open Drain
	P01	☐ 1. Complementary	☐ 2. Pch Open Drain
	P02	☐ 1. Complementary	☐ 2. Pch Open Drain
	P03	☐ 1. Complementary	☐ 2. Pch Open Drain
	P10	☐ 1. Complementary	☐ 2. Pch Open Drain
	P11	☐ 1. Complementary	☐ 2. Pch Open Drain
	P12	☐ 1. Complementary	☐ 2. Pch Open Drain
	P13	☐ 1. Complementary	☐ 2. Pch Open Drain
	P20	☐ 1. Complementary	☐ 2. Pch Open Drain
	P21	☐ 1. Complementary	☐ 2. Pch Open Drain
	P22	☐ 1. Complementary	☐ 2. Pch Open Drain
	P23	☐ 1. Complementary	☐ 2. Pch Open Drain
	P30	☐ 1. Complementary	☐ 2. Pch Open Drain
	P31	☐ 1. Complementary	☐ 2. Pch Open Drain
	P32	☐ 1. Complementary	☐ 2. Pch Open Drain
	P33	☐ 1. Complementary	☐ 2. Pch Open Drain
	P40	☐ 1. Complementary	☐ 2. Pch Open Drain
	P41	☐ 1. Complementary	☐ 2. Pch Open Drain
	P42	☐ 1. Complementary	☐ 2. Pch Open Drain
	P43	☐ 1. Complementary	☐ 2. Pch Open Drain

Optional item		Option	
I/O port output specification	P50	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P51	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P52	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P53	☐ 1. Complementary	☐ 2. Pch Open Drain *
P0x port multiple key entry reset combination		☐ 1. Not Use ☐ 2. Use <P00, P01> ☐ 3. Use <P00, P01, P02> ☐ 4. Use <P00, P01, P02, P03>	
P0x port multiple key entry reset time authorization		☐ 1. Not Use	☐ 2. Use
LCD drive power supply		☐ 1. Internal 1/3 bias ☐ 2. External 1/3 bias, $V_{DD} = V_{C2}$ (4.5 V panel) ☐ 3. External 1/3 bias, $V_{DD} = V_{C3}$ (3.0 V panel) ☐ 4. External 1/2 bias, $V_{DD} = V_{C3}$, $V_{C1} = V_{C2}$ (3.0 V panel)	

☐ Selectable ■ Fixed

* Do not select "Pch Open Drain" as the P50–P53 port output specification if the R/F converter (channel 0) is used.

Table 1.3.2 Option list (S1C63004)

Optional item		Option	
Operating power voltage		☐ 1. Normal Type (1.8–5.5 V)	☐ 2. Low Voltage Type (1.1–1.7 V)
OSC3 oscillation circuit		☐ 1. CR (built-in R) ☐ 2. CR (external R) ☐ 3. Ceramic (4.0 MHz)	
RESET terminal pull-down resistor		☐ 1. Use	☐ 2. Not Use
SEG/GPIO/RFC selector	P20	☐ 1. I/O	☐ 2. SEG
	P21	☐ 1. I/O	☐ 2. SEG
	P22	☐ 1. I/O	☐ 2. SEG
	P23	☐ 1. I/O	☐ 2. SEG
	P30	☐ 1. I/O	☐ 2. SEG
	P31	☐ 1. I/O	☐ 2. SEG
	P32	☐ 1. I/O	☐ 2. SEG
	P33	☐ 1. I/O	☐ 2. SEG
	P50	☐ 1. I/O	☐ 2. SEG
	P51	☐ 1. I/O	☐ 2. SEG
	P52	☐ 1. I/O	☐ 2. SEG
	P53	☐ 1. I/O	☐ 2. SEG
	RFIN1	☐ 1. RFC	☐ 2. SEG
	REF1	☐ 1. RFC	☐ 2. SEG
	SEN1	☐ 1. RFC	☐ 2. SEG
	HUD	☐ 1. RFC	☐ 2. SEG
I/O port pull-down resistor	P00	☐ 1. Use	☐ 2. Not Use
	P01	☐ 1. Use	☐ 2. Not Use
	P02	☐ 1. Use	☐ 2. Not Use
	P03	☐ 1. Use	☐ 2. Not Use
	P10	☐ 1. Use	☐ 2. Not Use
	P11	☐ 1. Use	☐ 2. Not Use
	P12	☐ 1. Use	☐ 2. Not Use
	P13	☐ 1. Use	☐ 2. Not Use
	P20	☐ 1. Use	☐ 2. Not Use
	P21	☐ 1. Use	☐ 2. Not Use
	P22	☐ 1. Use	☐ 2. Not Use
	P23	☐ 1. Use	☐ 2. Not Use
	P30	☐ 1. Use	☐ 2. Not Use
	P31	☐ 1. Use	☐ 2. Not Use
	P32	☐ 1. Use	☐ 2. Not Use
	P33	☐ 1. Use	☐ 2. Not Use
	P50	☐ 1. Use	☐ 2. Not Use
	P51	☐ 1. Use	☐ 2. Not Use
	P52	☐ 1. Use	☐ 2. Not Use
	P53	☐ 1. Use	☐ 2. Not Use
I/O port output specification	P00	☐ 1. Complementary	☐ 2. Pch Open Drain
	P01	☐ 1. Complementary	☐ 2. Pch Open Drain
	P02	☐ 1. Complementary	☐ 2. Pch Open Drain
	P03	☐ 1. Complementary	☐ 2. Pch Open Drain
	P10	☐ 1. Complementary	☐ 2. Pch Open Drain
	P11	☐ 1. Complementary	☐ 2. Pch Open Drain
	P12	☐ 1. Complementary	☐ 2. Pch Open Drain
	P13	☐ 1. Complementary	☐ 2. Pch Open Drain

Optional item		Option	
I/O port output specification	P20	☐ 1. Complementary	☐ 2. Pch Open Drain
	P21	☐ 1. Complementary	☐ 2. Pch Open Drain
	P22	☐ 1. Complementary	☐ 2. Pch Open Drain
	P23	☐ 1. Complementary	☐ 2. Pch Open Drain
	P30	☐ 1. Complementary	☐ 2. Pch Open Drain
	P31	☐ 1. Complementary	☐ 2. Pch Open Drain
	P32	☐ 1. Complementary	☐ 2. Pch Open Drain
	P33	☐ 1. Complementary	☐ 2. Pch Open Drain
	P50	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P51	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P52	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P53	☐ 1. Complementary	☐ 2. Pch Open Drain *
P0x port multiple key entry reset combination		☐ 1. Not Use ☐ 2. Use <P00, P01> ☐ 3. Use <P00, P01, P02> ☐ 4. Use <P00, P01, P02, P03>	
P0x port multiple key entry reset time authorization		☐ 1. Not Use	☐ 2. Use
LCD drive power supply		☐ 1. Internal 1/3 bias ☐ 2. External 1/3 bias, $V_{DD} = V_{C2}$ (4.5 V panel) ☐ 3. External 1/3 bias, $V_{DD} = V_{C3}$ (3.0 V panel) ☐ 4. External 1/2 bias, $V_{DD} = V_{C3}$, $V_{C1} = V_{C2}$ (3.0 V panel)	

☐ Selectable ■ Fixed

* Do not select "Pch Open Drain" as the P50–P53 port output specification if the R/F converter (channel 0) is used.

Table 1.3.3 Option list (S1C63003)

Optional item		Option	
Operating power voltage		☐ 1. Normal Type (1.8–5.5 V)	☐ 2. Low Voltage Type (1.1–1.7 V)
OSC3 oscillation circuit		■ 1. CR (built-in R) ☐ 2. CR (external R) ☐ 3. Ceramic (4.0 MHz)	
RESET terminal pull-down resistor		☐ 1. Use	☐ 2. Not Use
SEG/GPIO/RFC selector	P20	☐ 1. I/O	☐ 2. SEG
	P21	☐ 1. I/O	☐ 2. SEG
	P22	☐ 1. I/O	☐ 2. SEG
	P23	☐ 1. I/O	☐ 2. SEG
	P50	☐ 1. I/O	☐ 2. SEG
	P51	☐ 1. I/O	☐ 2. SEG
	P52	☐ 1. I/O	☐ 2. SEG
	P53	☐ 1. I/O	☐ 2. SEG
	RFIN1	☐ 1. RFC	☐ 2. SEG
	REF1	☐ 1. RFC	☐ 2. SEG
	SEN1	☐ 1. RFC	☐ 2. SEG
	HUD	☐ 1. RFC	☐ 2. SEG
I/O port pull-down resistor	P00	☐ 1. Use	☐ 2. Not Use
	P01	☐ 1. Use	☐ 2. Not Use
	P02	☐ 1. Use	☐ 2. Not Use
	P03	☐ 1. Use	☐ 2. Not Use
	P10	☐ 1. Use	☐ 2. Not Use
	P11	☐ 1. Use	☐ 2. Not Use
	P12	☐ 1. Use	☐ 2. Not Use
	P13	☐ 1. Use	☐ 2. Not Use
	P20	☐ 1. Use	☐ 2. Not Use
	P21	☐ 1. Use	☐ 2. Not Use
	P22	☐ 1. Use	☐ 2. Not Use
	P23	☐ 1. Use	☐ 2. Not Use
	P50	☐ 1. Use	☐ 2. Not Use
	P51	☐ 1. Use	☐ 2. Not Use
	P52	☐ 1. Use	☐ 2. Not Use
	P53	☐ 1. Use	☐ 2. Not Use
I/O port output specification	P00	☐ 1. Complementary	☐ 2. Pch Open Drain
	P01	☐ 1. Complementary	☐ 2. Pch Open Drain
	P02	☐ 1. Complementary	☐ 2. Pch Open Drain
	P03	☐ 1. Complementary	☐ 2. Pch Open Drain
	P10	☐ 1. Complementary	☐ 2. Pch Open Drain
	P11	☐ 1. Complementary	☐ 2. Pch Open Drain
	P12	☐ 1. Complementary	☐ 2. Pch Open Drain
	P13	☐ 1. Complementary	☐ 2. Pch Open Drain

Optional item		Option	
I/O port output specification	P20	☐ 1. Complementary	☐ 2. Pch Open Drain
	P21	☐ 1. Complementary	☐ 2. Pch Open Drain
	P22	☐ 1. Complementary	☐ 2. Pch Open Drain
	P23	☐ 1. Complementary	☐ 2. Pch Open Drain
	P50	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P51	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P52	☐ 1. Complementary	☐ 2. Pch Open Drain *
	P53	☐ 1. Complementary	☐ 2. Pch Open Drain *
P0x port multiple key entry reset combination		☐ 1. Not Use ☐ 2. Use <P00, P01> ☐ 3. Use <P00, P01, P02> ☐ 4. Use <P00, P01, P02, P03>	
P0x port multiple key entry reset time authorization		☐ 1. Not Use	☐ 2. Use
LCD drive power supply		☐ 1. Internal (V_{C2} reference) 1/3 bias (3.0 V panel) ☐ 2. Internal (V_{C1} reference) 1/3 bias (3.0 V panel) ☐ 3. External 1/3 bias, $V_{DD} = V_{C2}$ (4.5 V panel) ☐ 4. External 1/3 bias, $V_{DD} = V_{C3}$ (3.0 V panel) ☐ 5. External 1/2 bias, $V_{DD} = V_{C3}$, $V_{C1} = V_{C2}$ (3.0 V panel)	

☐ Selectable ■ Fixed

* Do not select "Pch Open Drain" as the P50–P53 port output specification if the R/F converter (channel 0) is used.

Table 1.3.4 Segment option (S1C63016)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									□S □C □N
SEG1																									□S □C □N
SEG2																									□S □C □N
SEG3																									□S □C □N
SEG4																									□S □C □N
SEG5																									□S □C □N
SEG6																									□S □C □N
SEG7																									□S □C □N
SEG8																									□S □C □N
SEG9																									□S □C □N
SEG10																									□S □C □N
SEG11																									□S □C □N
SEG12																									□S □C □N
SEG13																									□S □C □N
SEG14																									□S □C □N
SEG15																									□S □C □N
SEG16																									□S □C □N
SEG17																									□S □C □N
SEG18																									□S □C □N
SEG19																									□S □C □N
SEG20																									□S □C □N
SEG21																									□S □C □N
SEG22																									□S □C □N
SEG23																									□S □C □N
SEG24																									□S □C □N
SEG25																									□S □C □N
SEG26																									□S □C □N
SEG27																									□S □C □N
SEG28																									□S □C □N
SEG29																									□S □C □N
SEG30																									□S □C □N
SEG31																									□S □C □N
SEG32																									□S □C □N
SEG33																									□S □C □N
SEG34																									□S □C □N
SEG35																									□S □C □N
SEG36																									■S □C □N
SEG37																									■S □C □N
SEG38																									■S □C □N
SEG39																									■S □C □N
SEG40																									■S □C □N
SEG41																									■S □C □N
SEG42																									■S □C □N
SEG43																									■S □C □N
SEG44																									■S □C □N
SEG45																									■S □C □N
SEG46																									■S □C □N
SEG47																									■S □C □N
SEG48																									■S □C □N
SEG49																									■S □C □N
SEG50																									■S □C □N
SEG51																									■S □C □N
SEG52																									■S □C □N
SEG53																									■S □C □N
SEG54																									■S □C □N
SEG55																									■S □C □N

<address> H: RAM data high-order address (0–7)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63016)

1. The output specification of SEG0 to SEG35 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG36 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG36 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.

Table 1.3.5 Segment option (S1C63008)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									□S □C □N
SEG1																									□S □C □N
SEG2																									□S □C □N
SEG3																									□S □C □N
SEG4																									□S □C □N
SEG5																									□S □C □N
SEG6																									□S □C □N
SEG7																									□S □C □N
SEG8																									□S □C □N
SEG9																									□S □C □N
SEG10																									□S □C □N
SEG11																									□S □C □N
SEG12																									□S □C □N
SEG13																									□S □C □N
SEG14																									□S □C □N
SEG15																									□S □C □N
SEG16																									□S □C □N
SEG17																									□S □C □N
SEG18																									□S □C □N
SEG19																									□S □C □N
SEG20																									□S □C □N
SEG21																									□S □C □N
SEG22																									□S □C □N
SEG23																									□S □C □N
SEG24																									□S □C □N
SEG25																									□S □C □N
SEG26																									□S □C □N
SEG27																									□S □C □N
SEG28																									□S □C □N
SEG29																									□S □C □N
SEG30																									■S □C □N
SEG31																									■S □C □N
SEG32																									■S □C □N
SEG33																									■S □C □N
SEG34																									■S □C □N
SEG35																									■S □C □N
SEG36																									■S □C □N
SEG37																									■S □C □N
SEG38																									■S □C □N
SEG39																									■S □C □N
SEG40																									■S □C □N
SEG41																									■S □C □N
SEG42																									■S □C □N
SEG43																									■S □C □N
SEG44																									■S □C □N
SEG45																									■S □C □N
SEG46																									■S □C □N
SEG47																									■S □C □N
SEG48																									■S □C □N
SEG49																									■S □C □N
SEG50																									■S □C □N
SEG51																									■S □C □N
SEG52																									■S □C □N
SEG53																									■S □C □N
SEG54																									■S □C □N
SEG55																									■S □C □N

<address> H: RAM data high-order address (0–7)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63008)

1. The output specification of SEG0 to SEG29 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG36 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG36 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.
3. Configurations for nonexistent SEG pins (SEG30 to SEG35)
   - Always select "LCD segment output (S)" as the output specification of SEG30 to SEG35.
   - Leave the address cells for SEG30 to SEG35 blank. (Unused addresses will be allocated.)

Table 1.3.6 Segment option (S1C63004)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									☐S ☐C ☐N
SEG1																									☐S ☐C ☐N
SEG2																									☐S ☐C ☐N
SEG3																									☐S ☐C ☐N
SEG4																									☐S ☐C ☐N
SEG5																									☐S ☐C ☐N
SEG6																									☐S ☐C ☐N
SEG7																									☐S ☐C ☐N
SEG8																									☐S ☐C ☐N
SEG9																									☐S ☐C ☐N
SEG10																									☐S ☐C ☐N
SEG11																									☐S ☐C ☐N
SEG12																									☐S ☐C ☐N
SEG13																									☐S ☐C ☐N
SEG14																									☐S ☐C ☐N
SEG15																									☐S ☐C ☐N
SEG16																									☐S ☐C ☐N
SEG17																									☐S ☐C ☐N
SEG18																									☐S ☐C ☐N
SEG19																									☐S ☐C ☐N
SEG20																									■S ☐C ☐N
SEG21																									■S ☐C ☐N
SEG22																									■S ☐C ☐N
SEG23																									■S ☐C ☐N
SEG24																									■S ☐C ☐N
SEG25																									■S ☐C ☐N
SEG26																									■S ☐C ☐N
SEG27																									■S ☐C ☐N
SEG28																									■S ☐C ☐N
SEG29																									■S ☐C ☐N
SEG30																									■S ☐C ☐N
SEG31																									■S ☐C ☐N
SEG32																									■S ☐C ☐N
SEG33																									■S ☐C ☐N
SEG34																									■S ☐C ☐N
SEG35																									■S ☐C ☐N
SEG36																									■S ☐C ☐N
SEG37																									■S ☐C ☐N
SEG38																									■S ☐C ☐N
SEG39																									■S ☐C ☐N
SEG40																									■S ☐C ☐N
SEG41																									■S ☐C ☐N
SEG42																									■S ☐C ☐N
SEG43																									■S ☐C ☐N
SEG44																									■S ☐C ☐N
SEG45																									■S ☐C ☐N
SEG46																									■S ☐C ☐N
SEG47																									■S ☐C ☐N
SEG48																									■S ☐C ☐N
SEG49																									■S ☐C ☐N
SEG50																									■S ☐C ☐N
SEG51																									■S ☐C ☐N
SEG52																									■S ☐C ☐N
SEG53																									■S ☐C ☐N
SEG54																									■S ☐C ☐N
SEG55																									■S ☐C ☐N

<address> H: RAM data high-order address (0–7)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63004)

1. The output specification of SEG0 to SEG19 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG40 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG40 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.
3. Configurations for nonexistent SEG pins (SEG20 to SEG39)
   - Always select "LCD segment output (S)" as the output specification of SEG20 to SEG39.
   - Leave the address cells for SEG20 to SEG39 blank. (Unused addresses will be allocated.)

Table 1.3.7 Segment option (S1C63003)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									☐S ☐C ☐N
SEG1																									☐S ☐C ☐N
SEG2																									☐S ☐C ☐N
SEG3																									☐S ☐C ☐N
SEG4																									☐S ☐C ☐N
SEG5																									☐S ☐C ☐N
SEG6																									☐S ☐C ☐N
SEG7																									☐S ☐C ☐N
SEG8																									☐S ☐C ☐N
SEG9																									☐S ☐C ☐N
SEG10																									■S ☐C ☐N
SEG11																									■S ☐C ☐N
SEG12																									■S ☐C ☐N
SEG13																									■S ☐C ☐N
SEG14																									■S ☐C ☐N
SEG15																									■S ☐C ☐N
SEG16																									■S ☐C ☐N
SEG17																									■S ☐C ☐N
SEG18																									■S ☐C ☐N
SEG19																									■S ☐C ☐N
SEG20																									■S ☐C ☐N
SEG21																									■S ☐C ☐N
SEG22																									■S ☐C ☐N
SEG23																									■S ☐C ☐N
SEG24																									■S ☐C ☐N
SEG25																									■S ☐C ☐N
SEG26																									■S ☐C ☐N
SEG27																									■S ☐C ☐N
SEG28																									■S ☐C ☐N
SEG29																									■S ☐C ☐N
SEG30																									■S ☐C ☐N
SEG31																									■S ☐C ☐N
SEG32																									■S ☐C ☐N
SEG33																									■S ☐C ☐N
SEG34																									■S ☐C ☐N
SEG35																									■S ☐C ☐N
SEG36																									■S ☐C ☐N
SEG37																									■S ☐C ☐N
SEG38																									■S ☐C ☐N
SEG39																									■S ☐C ☐N
SEG40																									■S ☐C ☐N
SEG41																									■S ☐C ☐N
SEG42																									■S ☐C ☐N
SEG43																									■S ☐C ☐N
SEG44																									■S ☐C ☐N
SEG45																									■S ☐C ☐N
SEG46																									■S ☐C ☐N
SEG47																									■S ☐C ☐N
SEG48																									■S ☐C ☐N
SEG49																									■S ☐C ☐N
SEG50																									■S ☐C ☐N
SEG51																									■S ☐C ☐N
SEG52																									■S ☐C ☐N
SEG53																									■S ☐C ☐N
SEG54																									■S ☐C ☐N
SEG55																									■S ☐C ☐N

<address> H: RAM data high-order address (0–3)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63003)

1. The output specification of SEG0 to SEG9 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG44 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG44 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.
3. Configurations for nonexistent SEG pins (SEG10 to SEG43)
   - Always select "LCD segment output (S)" as the output specification of SEG10 to SEG43.
   - Leave the address cells for SEG10 to SEG43 blank. (Unused addresses will be allocated.)
4. Configurations for nonexistent COM pins (COM5 to COM7)
   - Leave the address cells for COM5 to COM7 blank. (Unused addresses will be allocated.)

2 Pins and Packages

2.1 S1C63016 Pins

2.1.1 S1C63016 Pin/Pad Layout Diagrams

QFP15-100pin/TQFP14-100pin

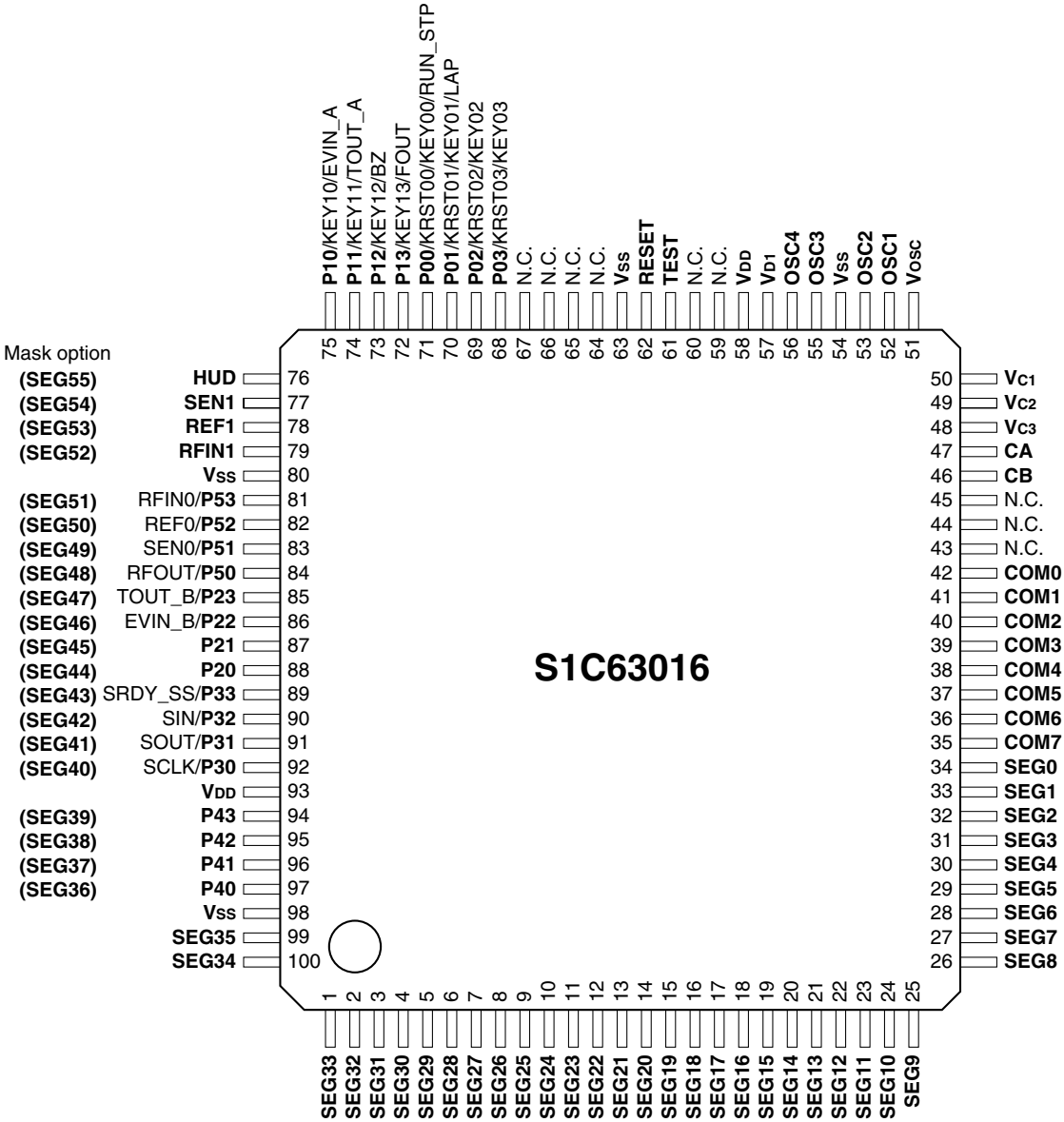


Figure 2.1.1.1 S1C63016 pin layout diagram (QFP15-100pin/TQFP14-100pin)

Diagram of pad layout

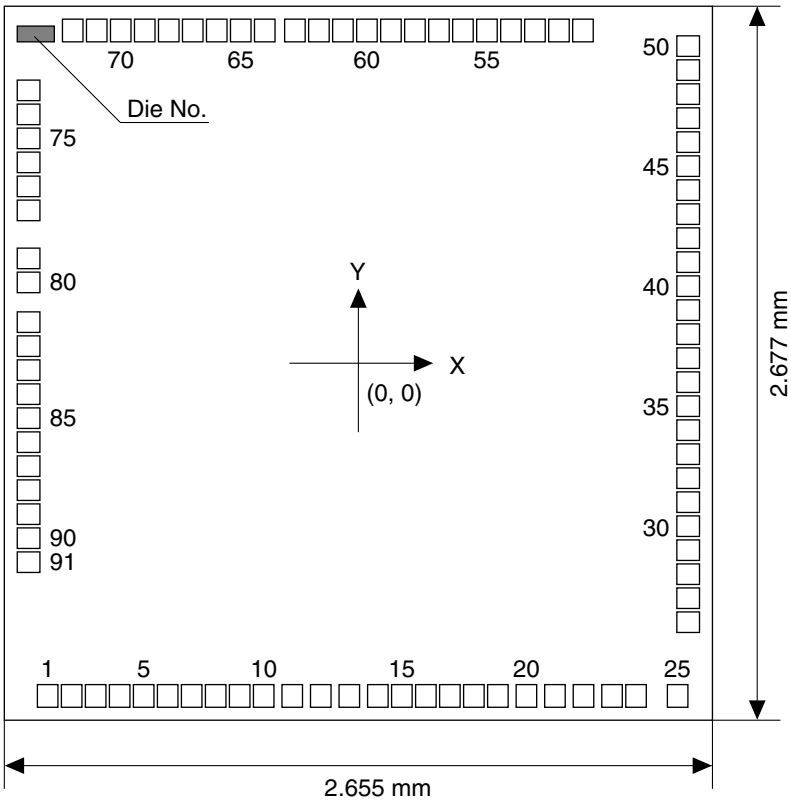


Figure 2.1.1.2 S1C63016 pad layout diagram

Chip thickness: 400 µm
Pad opening (X × Y): 77 × 85 µm (No. 1 to No. 25, No. 51 to No. 72)
85 × 77 µm (No. 26 to No. 50, No. 73 to No. 91)

Note: A chip thickness that exceeds 400 µm cannot be specified even if a chip other than the standard thickness type is required.

Pad coordinates

Table 2.1.1.1 S1C63016 pad coordinates

No.	Pad name		X (µm)	Y (µm)
1	HUD	(SEG55)	-1165.0	-1247.5
2	SEN1	(SEG54)	-1075.0	-1247.5
3	REF1	(SEG53)	-985.0	-1247.5
4	RFIN1	(SEG52)	-895.0	-1247.5
5	V_{SS}		-805.0	-1247.5
6	P53/RFIN0	(SEG51)	-715.0	-1247.5
7	P52/REF0	(SEG50)	-625.0	-1247.5
8	P51/SEN0	(SEG49)	-535.0	-1247.5
9	P50/RFOUT	(SEG48)	-445.0	-1247.5
10	P23/TOUT_B	(SEG47)	-355.0	-1247.5
11	P22/EVIN_B	(SEG46)	-248.0	-1247.5
12	P21	(SEG45)	-141.0	-1247.5
13	P20	(SEG44)	-34.0	-1247.5
14	P33/SRDY_SS	(SEG43)	73.0	-1247.5
15	P32/SIN	(SEG42)	163.0	-1247.5
16	P31/SOUT	(SEG41)	253.0	-1247.5
17	P30/SCLK	(SEG40)	343.0	-1247.5
18	V_{DD}		433.0	-1247.5
19	P43	(SEG39)	523.0	-1247.5
20	P42	(SEG38)	630.0	-1247.5
21	P41	(SEG37)	737.0	-1247.5
22	P40	(SEG36)	844.0	-1247.5
23	V_{SS}		951.0	-1247.5
24	SEG35		1041.0	-1247.5
25	SEG34		1197.0	-1247.5
26	SEG33		1236.5	-971.0
27	SEG32		1236.5	-881.0
28	SEG31		1236.5	-791.0
29	SEG30		1236.5	-701.0
30	SEG29		1236.5	-611.0
31	SEG28		1236.5	-521.0
32	SEG27		1236.5	-431.0
33	SEG26		1236.5	-341.0
34	SEG25		1236.5	-251.0
35	SEG24		1236.5	-161.0
36	SEG23		1236.5	-71.0
37	SEG22		1236.5	19.0
38	SEG21		1236.5	109.0
39	SEG20		1236.5	199.0
40	SEG19		1236.5	289.0
41	SEG18		1236.5	379.0
42	SEG17		1236.5	469.0
43	SEG16		1236.5	559.0
44	SEG15		1236.5	649.0
45	SEG14		1236.5	739.0
46	SEG13		1236.5	829.0
47	SEG12		1236.5	919.0
48	SEG11		1236.5	1009.0
49	SEG10		1236.5	1099.0
50	SEG9		1236.5	1189.0

No.	Pad name	X (µm)	Y (µm)
51	SEG8	842.0	1247.5
52	SEG7	752.0	1247.5
53	SEG6	662.0	1247.5
54	SEG5	572.0	1247.5
55	SEG4	482.0	1247.5
56	SEG3	392.0	1247.5
57	SEG2	302.0	1247.5
58	SEG1	212.0	1247.5
59	SEG0	122.0	1247.5
60	COM7	32.0	1247.5
61	COM6	-58.0	1247.5
62	COM5	-148.0	1247.5
63	COM4	-238.0	1247.5
64	COM3	-351.0	1247.5
65	COM2	-441.0	1247.5
66	COM1	-531.0	1247.5
67	COM0	-621.0	1247.5
68	CB	-711.0	1247.5
69	CA	-801.0	1247.5
70	V_{C3}	-891.0	1247.5
71	V_{C2}	-981.0	1247.5
72	V_{C1}	-1071.0	1247.5
73	V_{OSC}	-1236.5	1023.0
74	OSC1	-1236.5	933.0
75	OSC2	-1236.5	843.0
76	V_{SS}	-1236.5	753.0
77	OSC3	-1236.5	663.0
78	OSC4	-1236.5	573.0
79	V_{D1}	-1236.5	393.0
80	V_{DD}	-1236.5	303.0
81	TEST	-1236.5	154.0
82	RESET	-1236.5	64.0
83	V_{SS}	-1236.5	-26.0
84	P03/KRST03/KEY03	-1236.5	-116.0
85	P02/KRST02/KEY02	-1236.5	-206.0
86	P01/KRST01/KEY01/LAP	-1236.5	-296.0
87	P00/KRST00/KEY00/RUN_STP	-1236.5	-386.0
88	P13/KEY13/FOUT	-1236.5	-476.0
89	P12/KEY12/BZ	-1236.5	-566.0
90	P11/KEY11/TOUT_A	-1236.5	-656.0
91	P10/KEY10/EVIN_A	-1236.5	-746.0

2.1.2 S1C63016 Pin Description

Table 2.1.2.1 S1C63016 pin description

Pin name		Pad/pin No.		I/O	OP	SFT	Function
Default	Shared function	Chip	QFP15/ TQFP14				
V_{DD}		18, 80	58, 93	–	–	–	Power (+) supply pins
V_{SS}		5, 23, 76, 83	54, 63, 80, 98	–	–	–	Power (-) supply pins
V_{D1}		79	57	–	–	–	Internal logic voltage regulator output pin
V_{OSC}		73	51	–	–	–	Crystal oscillation circuit operating voltage output pin
V_{C1}–V_{C3}		72–70	50–48	–	–	–	LCD system power supply pins
CA, CB		69, 68	47, 46	–	–	–	LCD system voltage boost/reduce capacitor connecting pins
OSC1		74	52	I	–	–	Crystal oscillation input pin
OSC2		75	53	O	–	–	Crystal oscillation output pin
OSC3		77	55	I	OP	–	Ceramic oscillation input pin
				I	OP	–	CR oscillation (external R) input pin
				–	OP	–	CR oscillation (built-in R) input pin (Leave the pin open.)
OSC4		78	56	O	OP	–	Ceramic oscillation output pin
				O	OP	–	CR oscillation (external R) output pin
				–	OP	–	CR oscillation (built-in R) output pin (Leave the pin open.)
P00	P00	87	71	I/o	–	D	I/O port pin
	KRST00			I	OP	–	Key reset input pin
	KEY00			I	–	SFT	Port interrupt input pin
	RUN_STP			I	–	SFT	Stopwatch direct RUN/STOP input pin (Can be switched to LAP input.)
P01	P01	86	70	I/o	–	D	I/O port pin
	KRST01			I	OP	–	Key reset input pin
	KEY01			I	–	SFT	Port interrupt input pin
	LAP			I	–	SFT	Stopwatch direct LAP input pin (Can be switched to RUN/STOP input.)
P02	P02	85	69	I/o	–	D	I/O port pin
	KRST02			I	OP	–	Key reset input pin
	KEY02			I	–	SFT	Port interrupt input pin
P03	P03	84	68	I/o	–	D	I/O port pin
	KRST03			I	OP	–	Key reset input pin
	KEY03			I	–	SFT	Port interrupt input pin
P10	P10	91	75	I/o	–	D	I/O port pin
	KEY10			I	–	SFT	Port interrupt input pin
	EVIN_A			I	–	SFT	Event counter (programmable timer 0) input pin
P11	P11	90	74	I/o	–	D	I/O port pin
	KEY11			I	–	SFT	Port interrupt input pin
	TOUT_A			O	–	SFT	Programmable timer 0/1 output pin
P12	P12	89	73	I/o	–	D	I/O port pin
	KEY12			I	–	SFT	Port interrupt input pin
	BZ			O	–	SFT	Sound generator output pin
P13	P13	88	72	I/o	–	D	I/O port pin
	KEY13			I	–	SFT	Port interrupt input pin
	FOUT			O	–	SFT	FOUT clock output pin
P20	P20	13	88	I/o	OP	–	I/O port pin
	SEG44			O	OP	–	LCD segment output pin
P21	P21	12	87	I/o	OP	–	I/O port pin
	SEG45			O	OP	–	LCD segment output pin
P22	P22	11	86	I/o	OP	D	I/O port pin
	EVIN_B			I		SFT	Event counter (programmable timer 2) input pin
	SEG46			O	OP	–	LCD segment output pin
P23	P23	10	85	I/o	OP	D	I/O port pin
	TOUT_B			O		SFT	Programmable timer 2 output pin
	SEG47			O	OP	–	LCD segment output pin
P30	P30	17	92	I/o	OP	D	I/O port pin
	SCLK			I/o		SFT	Serial I/F clock input/output pin
	SEG40			O	OP	–	LCD segment output pin
P31	P31	16	91	I/o	OP	D	I/O port pin
	SOUT			O		SFT	Serial I/F data output pin
	SEG41			O	OP	–	LCD segment output pin
P32	P32	15	90	I/o	OP	D	I/O port pin
	SIN			I		SFT	Serial I/F data input pin
	SEG42			O	OP	–	LCD segment output pin
P33	P33	14	89	I/o	OP	D	I/O port pin
	SRDY_SS			i/O		SFT	Serial I/F ready output/slave-select input pin
	SEG43			O	OP	–	LCD segment output pin

Pin name		Pad/pin No.		I/O	OP	SFT	Function
Default	Shared function	Chip	QFP15/ TQFP14				
P40	P40	22	97	I/o	OP	–	I/O port pin
	SEG36			O	OP	–	LCD segment output pin
P41	P41	21	96	I/o	OP	–	I/O port pin
	SEG37			O	OP	–	LCD segment output pin
P42	P42	20	95	I/o	OP	–	I/O port pin
	SEG38			O	OP	–	LCD segment output pin
P43	P43	19	94	I/o	OP	–	I/O port pin
	SEG39			O	OP	–	LCD segment output pin
P50	P50	9	84	I/o	OP	D	I/O port pin
	RFOUT			O		SFT	R/F converter CR oscillation clock output pin
	SEG48			O	OP	–	LCD segment output pin
P51	P51	8	83	I/o	OP	D	I/O port pin
	SEN0			O		SFT	R/F converter Ch.0 CR oscillation output pin for DC bias sensor
	SEG49			O	OP	–	LCD segment output pin
P52	P52	7	82	I/o	OP	D	I/O port pin
	REF0			O		SFT	R/F converter Ch.0 CR oscillation output pin for reference resistor
	SEG50			O	OP	–	LCD segment output pin
P53	P53	6	81	I/o	OP	D	I/O port pin
	RFIN0			I		SFT	R/F converter Ch.0 CR oscillation input pin
	SEG51			O	OP	–	LCD segment output pin
RFIN1	RFIN1	4	79	I	OP	–	R/F converter Ch.1 CR oscillation input pin
	SEG52			O	OP	–	LCD segment output pin
REF1	REF1	3	78	O	OP	–	R/F converter Ch.1 CR oscillation output pin for reference resistor
	SEG53			O	OP	–	LCD segment output pin
SEN1	SEN1	2	77	O	OP	–	R/F converter Ch.1 CR oscillation output pin for DC bias sensor
	SEG54			O	OP	–	LCD segment output pin
HUD	HUD	1	76	O	OP	–	R/F converter CR oscillation output pin for AC bias sensor
	SEG55			O	OP	–	LCD segment output pin
COM0–COM7		67–60	42–35	O	–	–	LCD common output pins
SEG0–SEG35		59–24	34–1, 100, 99	O	–	–	LCD segment output pins
RESET		82	62	I	–	–	Initial reset input pin
TEST		81	61	I	–	–	Test pin (Connect to VSS during normal operation.)

I/O: Capital letters (I, O) represent the input/output direction in the initial settings.

OP: Selected by mask option ("–" means "no option provided.")

SFT: Switched by software ("–" means "no software switch provided" and "D" means default function.)

Note: The TEST terminal must be connected to the VSS power supply. Be sure to avoid applying other conditions to the terminals during normal operation.

2.2 S1C63008 Pins

2.2.1 S1C63008 Pin/Pad Layout Diagrams

QFP15-100pin/TQFP14-100pin

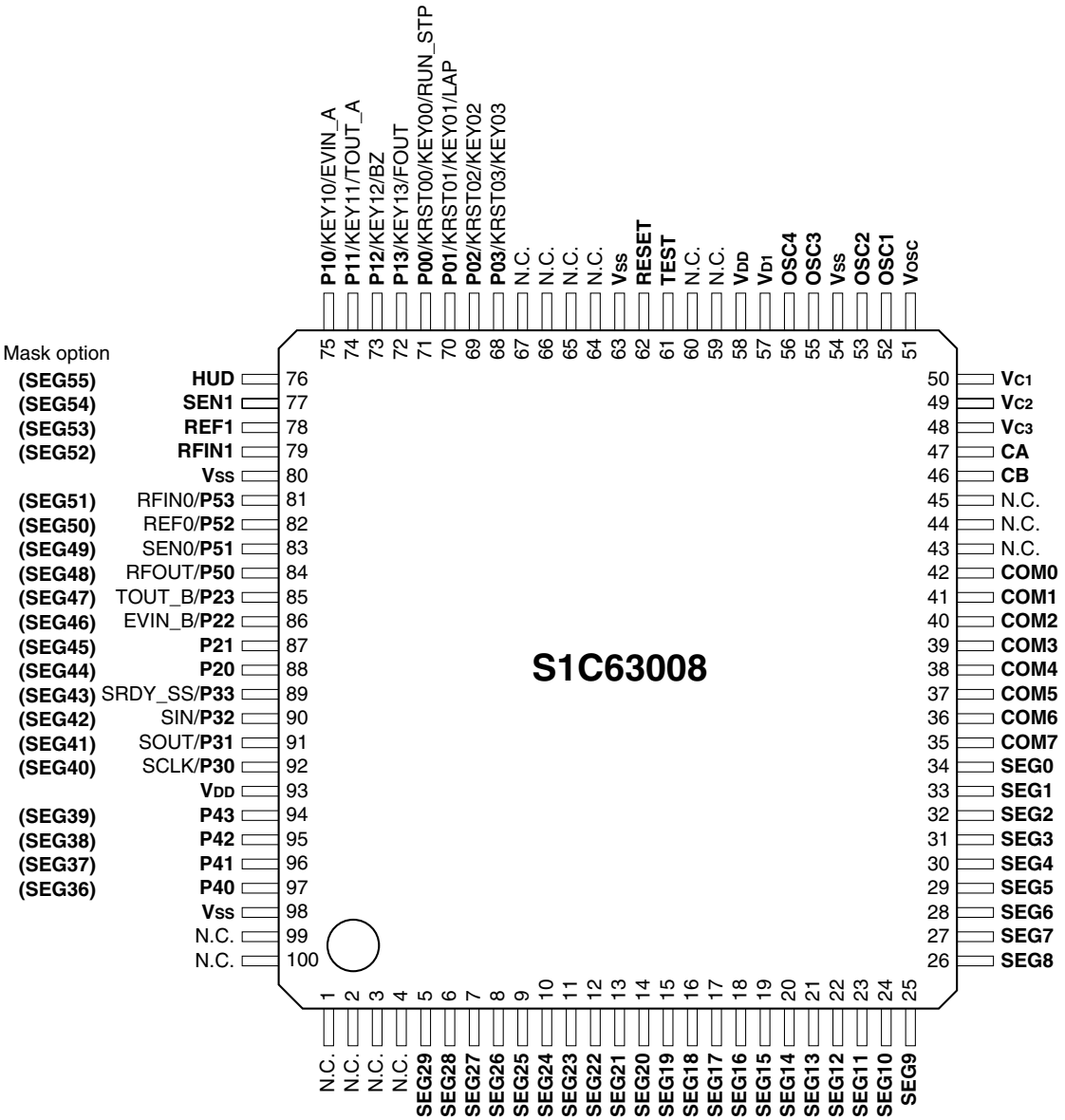


Figure 2.2.1.1 S1C63008 pin layout diagram (QFP15-100pin/TQFP14-100pin)

Diagram of pad layout

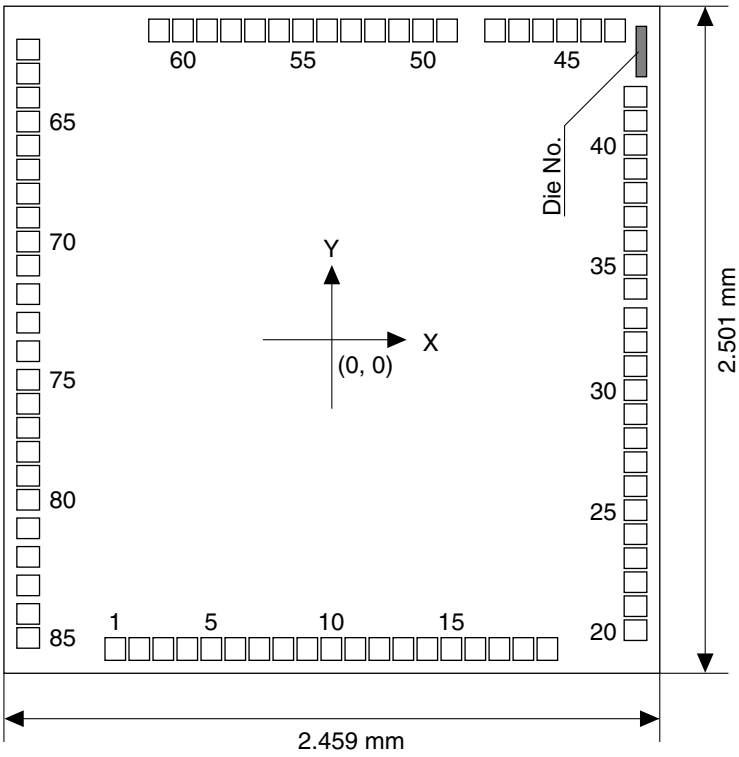


Figure 2.2.1.2 S1C63008 pad layout diagram

Chip thickness: 400 µm
Pad opening (X × Y): 77 × 85 µm (No. 1 to No. 19, No. 43 to No. 61)
85 × 77 µm (No. 20 to No. 42, No. 62 to No. 85)

Note: A chip thickness that exceeds 400 µm cannot be specified even if a chip other than the standard thickness type is required.

Pad coordinates

Table 2.2.1.1 S1C63008 pad coordinates

No.	Pad name	X (µm)	Y (µm)
1	SEG28	-812.0	-1159.5
2	SEG27	-722.0	-1159.5
3	SEG26	-632.0	-1159.5
4	SEG25	-542.0	-1159.5
5	SEG24	-452.0	-1159.5
6	SEG23	-362.0	-1159.5
7	SEG22	-272.0	-1159.5
8	SEG21	-182.0	-1159.5
9	SEG20	-92.0	-1159.5
10	SEG19	-2.0	-1159.5
11	SEG18	88.0	-1159.5
12	SEG17	178.0	-1159.5
13	SEG16	268.0	-1159.5
14	SEG15	358.0	-1159.5
15	SEG14	448.0	-1159.5
16	SEG13	538.0	-1159.5
17	SEG12	628.0	-1159.5
18	SEG11	718.0	-1159.5
19	SEG10	808.0	-1159.5
20	SEG9	1138.5	-1089.0
21	SEG8	1138.5	-999.0
22	SEG7	1138.5	-909.0
23	SEG6	1138.5	-819.0
24	SEG5	1138.5	-729.0
25	SEG4	1138.5	-639.0
26	SEG3	1138.5	-549.0
27	SEG2	1138.5	-459.0
28	SEG1	1138.5	-369.0
29	SEG0	1138.5	-279.0
30	COM7	1138.5	-189.0
31	COM6	1138.5	-99.0
32	COM5	1138.5	-9.0
33	COM4	1138.5	81.0
34	COM3	1138.5	191.0
35	COM2	1138.5	281.0
36	COM1	1138.5	371.0
37	COM0	1138.5	461.0
38	CB	1138.5	551.0
39	CA	1138.5	641.0
40	V_{C3}	1138.5	731.0
41	V_{C2}	1138.5	821.0
42	V_{C1}	1138.5	911.0

No.	Pad name	X (µm)	Y (µm)
43	V_{OSC}	1062.0	1159.5
44	OSC1	972.0	1159.5
45	OSC2	882.0	1159.5
46	V_{SS}	792.0	1159.5
47	OSC3	702.0	1159.5
48	OSC4	612.0	1159.5
49	V_{D1}	432.0	1159.5
50	V_{DD}	342.0	1159.5
51	TEST	252.0	1159.5
52	RESET	162.0	1159.5
53	V_{SS}	72.0	1159.5
54	P03/KRST03/KEY03	-18.0	1159.5
55	P02/KRST02/KEY02	-108.0	1159.5
56	P01/KRST01/KEY01/LAP	-198.0	1159.5
57	P00/KRST00/KEY00/RUN_STP	-288.0	1159.5
58	P13/KEY13/FOUT	-378.0	1159.5
59	P12/KEY12/BZ	-468.0	1159.5
60	P11/KEY11/TOUT_A	-558.0	1159.5
61	P10/KEY10/EVIN_A	-648.0	1159.5
62	HUD (SEG55)	-1138.5	1088.0
63	SEN1 (SEG54)	-1138.5	998.0
64	REF1 (SEG53)	-1138.5	908.0
65	RFIN1 (SEG52)	-1138.5	818.0
66	V_{SS}	-1138.5	728.0
67	P53/RFIN0 (SEG51)	-1138.5	638.0
68	P52/REF0 (SEG50)	-1138.5	548.0
69	P51/SEN0 (SEG49)	-1138.5	458.0
70	P50/RFOUT (SEG48)	-1138.5	368.0
71	P23/TOUT_B (SEG47)	-1138.5	278.0
72	P22/EVIN_B (SEG46)	-1138.5	171.0
73	P21 (SEG45)	-1138.5	64.0
74	P20 (SEG44)	-1138.5	-43.0
75	P33/SRDY_SS (SEG43)	-1138.5	-150.0
76	P32/SIN (SEG42)	-1138.5	-240.0
77	P31/SOUT (SEG41)	-1138.5	-330.0
78	P30/SCLK (SEG40)	-1138.5	-420.0
79	V_{DD}	-1138.5	-510.0
80	P43 (SEG39)	-1138.5	-600.0
81	P42 (SEG38)	-1138.5	-707.0
82	P41 (SEG37)	-1138.5	-814.0
83	P40 (SEG36)	-1138.5	-921.0
84	V_{SS}	-1138.5	-1028.0
85	SEG29	-1138.5	-1118.0

2.2.2 S1C63008 Pin Description

Table 2.2.2.1 S1C63008 pin description

Pin name		Pad/pin No.		I/O	OP	SFT	Function
Default	Shared function	Chip	QFP15/ TQFP14				
V_{DD}		50, 79	58, 93	–	–	–	Power (+) supply pins
V_{SS}		46, 53, 66, 84	54, 63, 80, 98	–	–	–	Power (-) supply pins
V_{D1}		49	57	–	–	–	Internal logic voltage regulator output pin
V_{OSC}		43	51	–	–	–	Crystal oscillation circuit operating voltage output pin
V_{C1}–V_{C3}		42–40	50–48	–	–	–	LCD system power supply pins
CA, CB		39, 38	47, 46	–	–	–	LCD system voltage boost/reduce capacitor connecting pins
OSC1		44	52	I	–	–	Crystal oscillation input pin
OSC2		45	53	O	–	–	Crystal oscillation output pin
OSC3		47	55	I	OP	–	Ceramic oscillation input pin
				I	OP	–	CR oscillation (external R) input pin
				–	OP	–	CR oscillation (built-in R) input pin (Leave the pin open.)
OSC4		48	56	O	OP	–	Ceramic oscillation output pin
				O	OP	–	CR oscillation (external R) output pin
				–	OP	–	CR oscillation (built-in R) output pin (Leave the pin open.)
P00	P00	57	71	I/o	–	D	I/O port pin
	KRST00			I	OP	–	Key reset input pin
	KEY00			I	–	SFT	Port interrupt input pin
	RUN_STP			I	–	SFT	Stopwatch direct RUN/STOP input pin (Can be switched to LAP input.)
P01	P01	56	70	I/o	–	D	I/O port pin
	KRST01			I	OP	–	Key reset input pin
	KEY01			I	–	SFT	Port interrupt input pin
	LAP			I	–	SFT	Stopwatch direct LAP input pin (Can be switched to RUN/STOP input.)
P02	P02	55	69	I/o	–	D	I/O port pin
	KRST02			I	OP	–	Key reset input pin
	KEY02			I	–	SFT	Port interrupt input pin
P03	P03	54	68	I/o	–	D	I/O port pin
	KRST03			I	OP	–	Key reset input pin
	KEY03			I	–	SFT	Port interrupt input pin
P10	P10	61	75	I/o	–	D	I/O port pin
	KEY10			I	–	SFT	Port interrupt input pin
	EVIN_A			I	–	SFT	Event counter (programmable timer 0) input pin
P11	P11	60	74	I/o	–	D	I/O port pin
	KEY11			I	–	SFT	Port interrupt input pin
	TOUT_A			O	–	SFT	Programmable timer 0/1 output pin
P12	P12	59	73	I/o	–	D	I/O port pin
	KEY12			I	–	SFT	Port interrupt input pin
	BZ			O	–	SFT	Sound generator output pin
P13	P13	58	72	I/o	–	D	I/O port pin
	KEY13			I	–	SFT	Port interrupt input pin
	FOUT			O	–	SFT	FOUT clock output pin
P20	P20	74	88	I/o	OP	–	I/O port pin
	SEG44			O	OP	–	LCD segment output pin
P21	P21	73	87	I/o	OP	–	I/O port pin
	SEG45			O	OP	–	LCD segment output pin
P22	P22	72	86	I/o	OP	D	I/O port pin
	EVIN_B			I		SFT	Event counter (programmable timer 2) input pin
	SEG46			O	OP	–	LCD segment output pin
P23	P23	71	85	I/o	OP	D	I/O port pin
	TOUT_B			O		SFT	Programmable timer 2 output pin
	SEG47			O	OP	–	LCD segment output pin
P30	P30	78	92	I/o	OP	D	I/O port pin
	SCLK			I/o		SFT	Serial I/F clock input/output pin
	SEG40			O	OP	–	LCD segment output pin
P31	P31	77	91	I/o	OP	D	I/O port pin
	SOUT			O		SFT	Serial I/F data output pin
	SEG41			O	OP	–	LCD segment output pin
P32	P32	76	90	I/o	OP	D	I/O port pin
	SIN			I		SFT	Serial I/F data input pin
	SEG42			O	OP	–	LCD segment output pin
P33	P33	75	89	I/o	OP	D	I/O port pin
	SRDY_SS			i/O		SFT	Serial I/F ready output/slave-select input pin
	SEG43			O	OP	–	LCD segment output pin

Pin name		Pad/pin No.		I/O	OP	SFT	Function
Default	Shared function	Chip	QFP15/ TQFP14				
P40	P40	83	97	I/o	OP	–	I/O port pin
	SEG36			O	OP	–	LCD segment output pin
P41	P41	82	96	I/o	OP	–	I/O port pin
	SEG37			O	OP	–	LCD segment output pin
P42	P42	81	95	I/o	OP	–	I/O port pin
	SEG38			O	OP	–	LCD segment output pin
P43	P43	80	94	I/o	OP	–	I/O port pin
	SEG39			O	OP	–	LCD segment output pin
P50	P50	70	84	I/o	OP	D	I/O port pin
	RFOUT			O		SFT	R/F converter CR oscillation clock output pin
	SEG48			O	OP	–	LCD segment output pin
P51	P51	69	83	I/o	OP	D	I/O port pin
	SEN0			O		SFT	R/F converter Ch.0 CR oscillation output pin for DC bias sensor
	SEG49			O	OP	–	LCD segment output pin
P52	P52	68	82	I/o	OP	D	I/O port pin
	REF0			O		SFT	R/F converter Ch.0 CR oscillation output pin for reference resistor
	SEG50			O	OP	–	LCD segment output pin
P53	P53	67	81	I/o	OP	D	I/O port pin
	RFIN0			I		SFT	R/F converter Ch.0 CR oscillation input pin
	SEG51			O	OP	–	LCD segment output pin
RFIN1	RFIN1	65	79	I	OP	–	R/F converter Ch.1 CR oscillation input pin
	SEG52			O	OP	–	LCD segment output pin
REF1	REF1	64	78	O	OP	–	R/F converter Ch.1 CR oscillation output pin for reference resistor
	SEG53			O	OP	–	LCD segment output pin
SEN1	SEN1	63	77	O	OP	–	R/F converter Ch.1 CR oscillation output pin for DC bias sensor
	SEG54			O	OP	–	LCD segment output pin
HUD	HUD	62	76	O	OP	–	R/F converter CR oscillation output pin for AC bias sensor
	SEG55			O	OP	–	LCD segment output pin
COM0–COM7		37–30	42–35	O	–	–	LCD common output pins
SEG0–SEG29		29–1, 85	34–5	O	–	–	LCD segment output pins
RESET		52	62	I	–	–	Initial reset input pin
TEST		51	61	I	–	–	Test pin (Connect to Vss during normal operation.)

I/O: Capital letters (I, O) represent the input/output direction in the initial settings.

OP: Selected by mask option ("–" means "no option provided.")

SFT: Switched by software ("–" means "no software switch provided" and "D" means default function.)

Note: The TEST terminal must be connected to the Vss power supply. Be sure to avoid applying other conditions to the terminals during normal operation.

2.3 S1C63004 Pins

2.3.1 S1C63004 Pin/Pad Layout Diagrams

QFP14-80pin

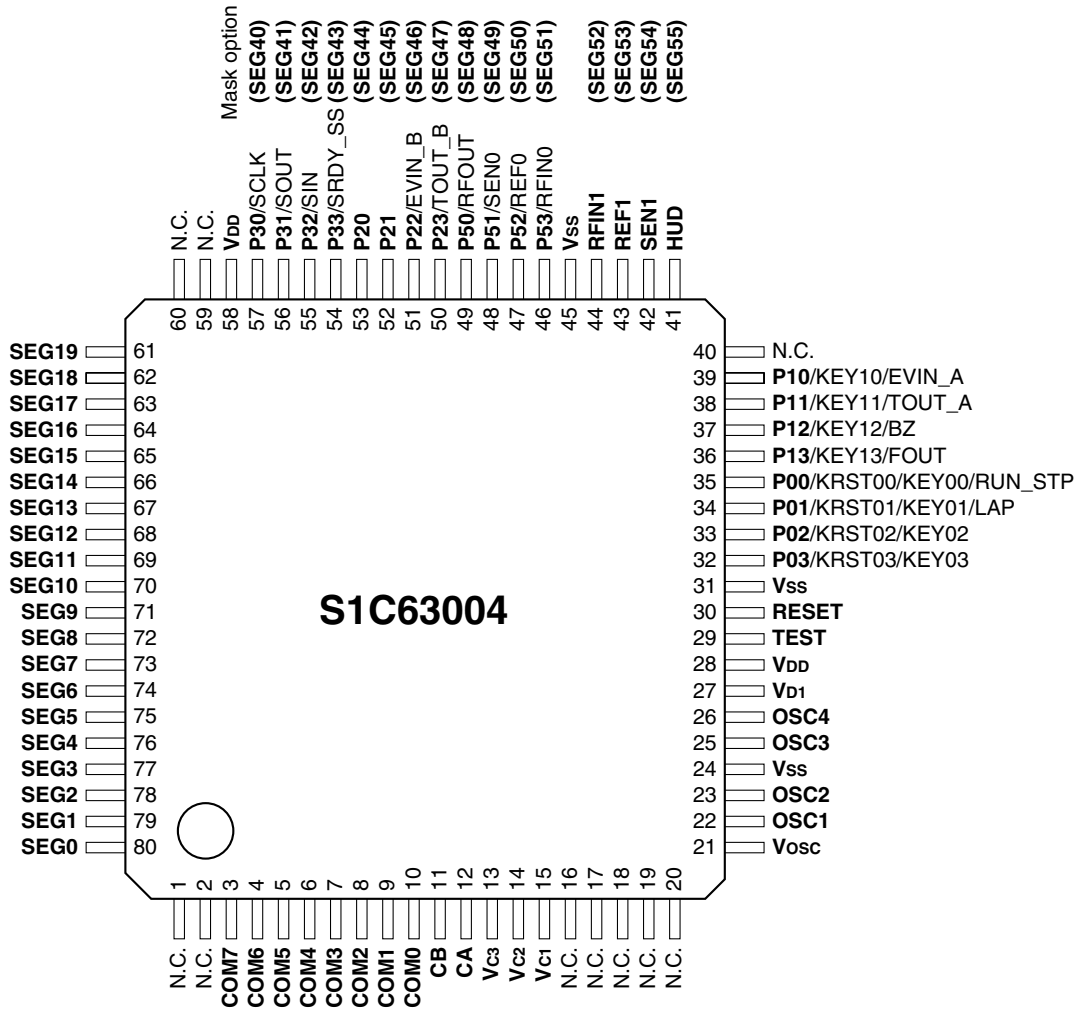


Figure 2.3.1.1 S1C63004 pin layout diagram (QFP14-80pin)

TQFP14-100pin

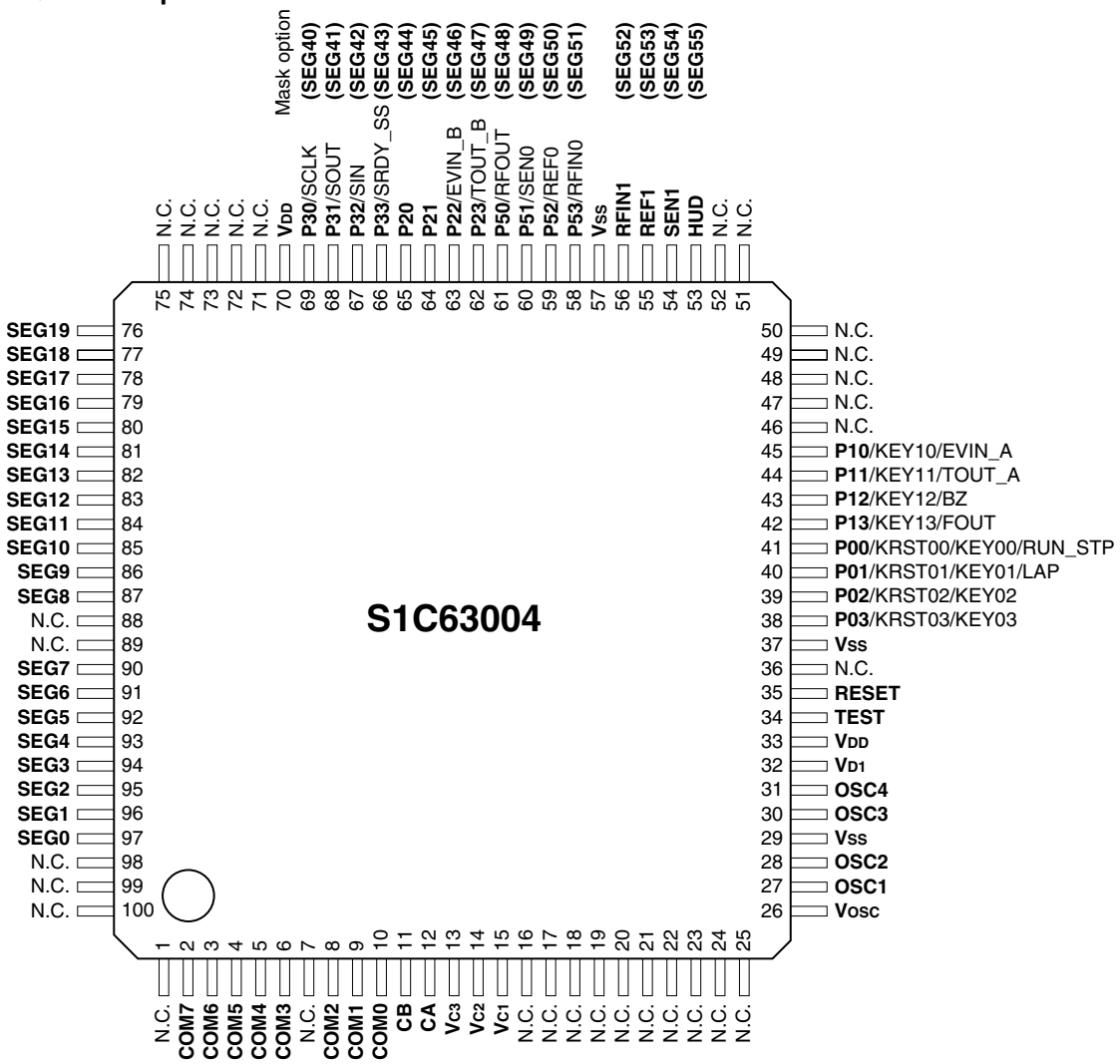


Figure 2.3.1.2 S1C63004 pin layout diagram (TQFP14-100pin)

Diagram of pad layout

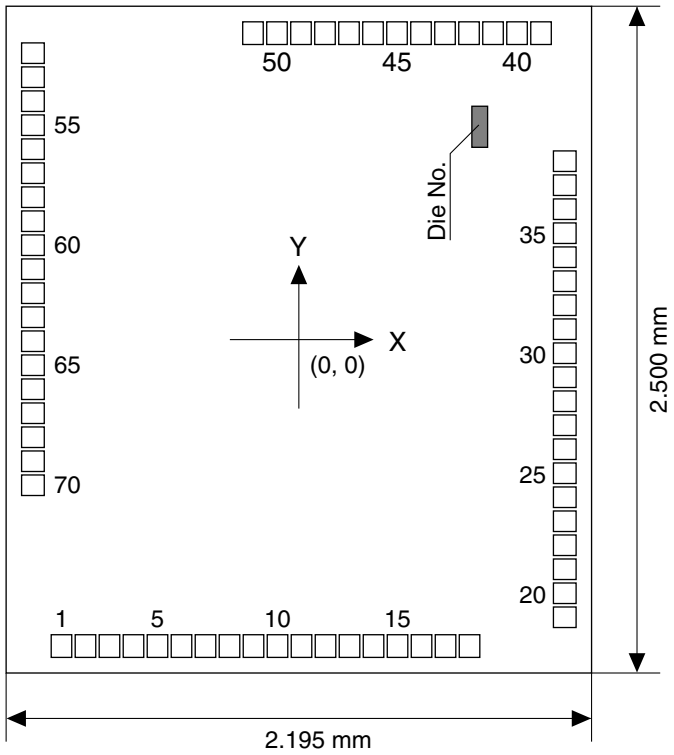


Figure 2.3.1.3 S1C63004 pad layout diagram

Chip thickness: 400 µm
Pad opening (X × Y): 77 × 85 µm (No. 1 to No. 18, No. 39 to No. 51)
85 × 77 µm (No. 19 to No. 38, No. 52 to No. 70)

Pad coordinates

Table 2.3.1.1 S1C63004 pad coordinates

No.	Pad name		X (µm)	Y (µm)
1	HUD	(SEG55)	-889.5	-1149.0
2	SEN1	(SEG54)	-799.5	-1149.0
3	REF1	(SEG53)	-709.5	-1149.0
4	RFIN1	(SEG52)	-619.5	-1149.0
5	V_{SS}		-529.5	-1149.0
6	P53/RFIN0	(SEG51)	-439.5	-1149.0
7	P52/REF0	(SEG50)	-349.5	-1149.0
8	P51/SEN0	(SEG49)	-259.5	-1149.0
9	P50/RFOUT	(SEG48)	-169.5	-1149.0
10	P23/TOUT_B	(SEG47)	-79.5	-1149.0
11	P22/EVIN_B	(SEG46)	10.5	-1149.0
12	P21	(SEG45)	100.5	-1149.0
13	P20	(SEG44)	190.5	-1149.0
14	P33/SRDY_SS	(SEG43)	280.5	-1149.0
15	P32/SIN	(SEG42)	370.5	-1149.0
16	P31/SOUT	(SEG41)	460.5	-1149.0
17	P30/SCLK	(SEG40)	550.5	-1149.0
18	V_{DD}		640.5	-1149.0
19	SEG19		996.5	-1040.5
20	SEG18		996.5	-950.5
21	SEG17		996.5	-860.5
22	SEG16		996.5	-770.5
23	SEG15		996.5	-680.5
24	SEG14		996.5	-590.5
25	SEG13		996.5	-500.5
26	SEG12		996.5	-410.5
27	SEG11		996.5	-320.5
28	SEG10		996.5	-230.5
29	SEG9		996.5	-140.5
30	SEG8		996.5	-50.5
31	SEG7		996.5	39.5
32	SEG6		996.5	129.5
33	SEG5		996.5	219.5
34	SEG4		996.5	309.5
35	SEG3		996.5	399.5
36	SEG2		996.5	489.5
37	SEG1		996.5	579.5
38	SEG0		996.5	669.5
39	COM7		907.5	1149.0
40	COM6		817.5	1149.0
41	COM5		727.5	1149.0
42	COM4		637.5	1149.0
43	COM3		547.5	1149.0
44	COM2		457.5	1149.0
45	COM1		367.5	1149.0
46	COM0		277.5	1149.0
47	CB		187.5	1149.0
48	CA		97.5	1149.0
49	V_{C3}		7.5	1149.0
50	V_{C2}		-82.5	1149.0
51	V_{C1}		-172.5	1149.0
52	V_{OSC}		-996.5	1074.0
53	OSC1		-996.5	984.0
54	OSC2		-996.5	894.0
55	V_{SS}		-996.5	804.0
56	OSC3		-996.5	714.0
57	OSC4		-996.5	624.0
58	V_{D1}		-996.5	534.0
59	V_{DD}		-996.5	444.0
60	TEST		-996.5	354.0
61	RESET		-996.5	264.0
62	V_{SS}		-996.5	174.0
63	P03/KRST03/KEY03		-996.5	84.0
64	P02/KRST02/KEY02		-996.5	-6.0
65	P01/KRST01/KEY01/LAP		-996.5	-96.0
66	P00/KRST00/KEY00/RUN_STP		-996.5	-186.0
67	P13/KEY13/FOUT		-996.5	-276.0
68	P12/KEY12/BZ		-996.5	-366.0
69	P11/KEY11/TOUT_A		-996.5	-456.0
70	P10/KEY10/EVIN_A		-996.5	-546.0

2.3.2 S1C63004 Pin Description

Table 2.3.2.1 S1C63004 pin description

Pin name		Pad/pin No.			I/O	OP	SFT	Function
Default	Shared function	Chip	QFP14 -80	TQFP14 -100				
V_{DD}		18, 59	28, 58	33, 70	–	–	–	Power (+) supply pins
V_{SS}		5, 55, 62	24, 31, 45	29, 37, 57	–	–	–	Power (-) supply pins
V_{D1}		58	27	32	–	–	–	Internal logic voltage regulator output pin
V_{OSC}		52	21	26	–	–	–	Crystal oscillation circuit operating voltage output pin
V_{C1}–V_{C3}		51–49	15–13	15–13	–	–	–	LCD system power supply pins
CA, CB		48, 47	12, 11	12, 11	–	–	–	LCD system voltage boost/reduce capacitor connecting pins
OSC1		53	22	27	I	–	–	Crystal oscillation input pin
OSC2		54	23	28	O	–	–	Crystal oscillation output pin
OSC3		56	25	30	I	OP	–	Ceramic oscillation input pin
					I	OP	–	CR oscillation (external R) input pin
					–	OP	–	CR oscillation (built-in R) input pin (Leave the pin open.)
OSC4		57	26	31	O	OP	–	Ceramic oscillation output pin
					O	OP	–	CR oscillation (external R) output pin
					–	OP	–	CR oscillation (built-in R) output pin (Leave the pin open.)
P00	P00	66	35	41	I/o	–	D	I/O port pin
	KRST00				I	OP	–	Key reset input pin
	KEY00				I	–	SFT	Port interrupt input pin
	RUN_STP				I	–	SFT	Stopwatch direct RUN/STOP input pin (Can be switched to LAP input.)
P01	P01	65	34	40	I/o	–	D	I/O port pin
	KRST01				I	OP	–	Key reset input pin
	KEY01				I	–	SFT	Port interrupt input pin
	LAP				I	–	SFT	Stopwatch direct LAP input pin (Can be switched to RUN/STOP input.)
P02	P02	64	33	39	I/o	–	D	I/O port pin
	KRST02				I	OP	–	Key reset input pin
	KEY02				I	–	SFT	Port interrupt input pin
P03	P03	63	32	38	I/o	–	D	I/O port pin
	KRST03				I	OP	–	Key reset input pin
	KEY03				I	–	SFT	Port interrupt input pin
P10	P10	70	39	45	I/o	–	D	I/O port pin
	KEY10				I	–	SFT	Port interrupt input pin
	EVIN_A				I	–	SFT	Event counter (programmable timer 0) input pin
P11	P11	69	38	44	I/o	–	D	I/O port pin
	KEY11				I	–	SFT	Port interrupt input pin
	TOUT_A				O	–	SFT	Programmable timer 0/1 output pin
P12	P12	68	37	43	I/o	–	D	I/O port pin
	KEY12				I	–	SFT	Port interrupt input pin
	BZ				O	–	SFT	Sound generator output pin
P13	P13	67	36	42	I/o	–	D	I/O port pin
	KEY13				I	–	SFT	Port interrupt input pin
	FOUT				O	–	SFT	FOUT clock output pin
P20	P20	13	53	65	I/o	OP	–	I/O port pin
	SEG44				O	OP	–	LCD segment output pin
P21	P21	12	52	64	I/o	OP	–	I/O port pin
	SEG45				O	OP	–	LCD segment output pin
P22	P22	11	51	63	I/o	OP	D	I/O port pin
	EVIN_B				I		SFT	Event counter (programmable timer 2) input pin
	SEG46				O	OP	–	LCD segment output pin
P23	P23	10	50	62	I/o	OP	D	I/O port pin
	TOUT_B				O		SFT	Programmable timer 2 output pin
	SEG47				O	OP	–	LCD segment output pin
P30	P30	17	57	69	I/o	OP	D	I/O port pin
	SCLK				I/o		SFT	Serial I/F clock input/output pin
	SEG40				O	OP	–	LCD segment output pin
P31	P31	16	56	68	I/o	OP	D	I/O port pin
	SOUT				O		SFT	Serial I/F data output pin
	SEG41				O	OP	–	LCD segment output pin
P32	P32	15	55	67	I/o	OP	D	I/O port pin
	SIN				I		SFT	Serial I/F data input pin
	SEG42				O	OP	–	LCD segment output pin
P33	P33	14	54	66	I/o	OP	D	I/O port pin
	SRDY_SS				i/O		SFT	Serial I/F ready output/slave-select input pin
	SEG43				O	OP	–	LCD segment output pin

Pin name		Pad/pin No.			I/O	OP	SFT	Function
Default	Shared function	Chip	QFP14 -80	TQFP14 -100				
P50	P50	9	49	61	I/o	OP	D	I/O port pin
	RFOUT				O		SFT	R/F converter CR oscillation clock output pin
	SEG48				O	OP	–	LCD segment output pin
P51	P51	8	48	60	I/o	OP	D	I/O port pin
	SEN0				O		SFT	R/F converter Ch.0 CR oscillation output pin for DC bias sensor
	SEG49				O	OP	–	LCD segment output pin
P52	P52	7	47	59	I/o	OP	D	I/O port pin
	REF0				O		SFT	R/F converter Ch.0 CR oscillation output pin for reference resistor
	SEG50				O	OP	–	LCD segment output pin
P53	P53	6	46	58	I/o	OP	D	I/O port pin
	RFIN0				I		SFT	R/F converter Ch.0 CR oscillation input pin
	SEG51				O	OP	–	LCD segment output pin
RFIN1	RFIN1	4	44	56	I	OP	–	R/F converter Ch.1 CR oscillation input pin
	SEG52				O	OP	–	LCD segment output pin
REF1	REF1	3	43	55	O	OP	–	R/F converter Ch.1 CR oscillation output pin for reference resistor
	SEG53				O	OP	–	LCD segment output pin
SEN1	SEN1	2	42	54	O	OP	–	R/F converter Ch.1 CR oscillation output pin for DC bias sensor
	SEG54				O	OP	–	LCD segment output pin
HUD	HUD	1	41	53	O	OP	–	R/F converter CR oscillation output pin for AC bias sensor
	SEG55				O	OP	–	LCD segment output pin
COM0–COM7		46–39	10–3	10–8, 6–2	O	–	–	LCD common output pins
SEG0–SEG19		38–19	80–61	97–90, 87–76	O	–	–	LCD segment output pins
RESET		61	30	35	I	–	–	Initial reset input pin
TEST		60	29	34	I	–	–	Test pin (Connect to VSS during normal operation.)

I/O: Capital letters (I, O) represent the input/output direction in the initial settings.

OP: Selected by mask option ("–" means "no option provided.")

SFT: Switched by software ("–" means "no software switch provided" and "D" means default function.)

Note: The TEST terminal must be connected to the VSS power supply. Be sure to avoid applying other conditions to the terminals during normal operation.

2.4 S1C63003 Pins

2.4.1 S1C63003 Pin/Pad Layout Diagrams

QFP12-48pin

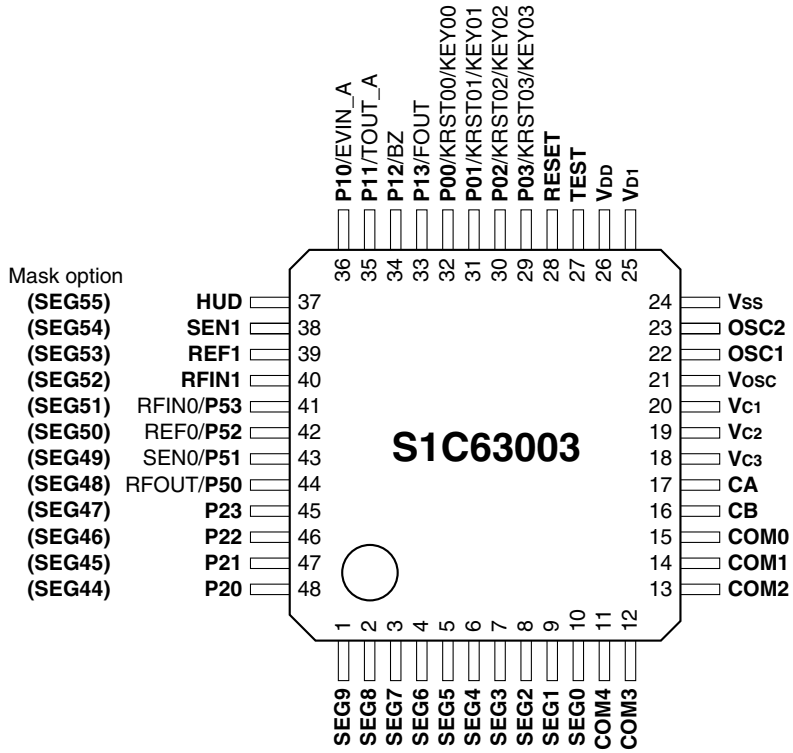


Figure 2.4.1.1 S1C63003 pin layout diagram (QFP12-48pin)

Diagram of pad layout

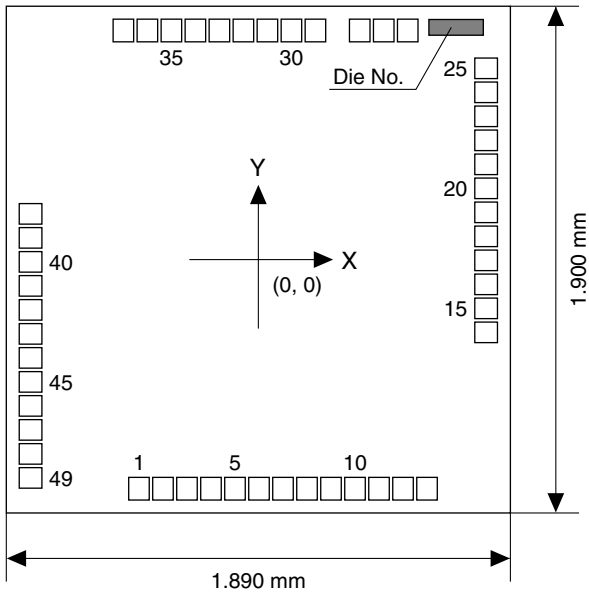


Figure 2.4.1.2 S1C63003 pad layout diagram

Chip thickness: 400 µm
Pad opening (X × Y): 77 × 85 µm (No. 1 to No. 13, No. 26 to No. 37)
85 × 77 µm (No. 14 to No. 25, No. 38 to No. 49)

Note: A chip thickness that exceeds 400 µm cannot be specified even if a chip other than the standard thickness type is required.

Pad coordinates

Table 2.4.1.1 S1C63003 pad coordinates

No.	Pad name		X (µm)	Y (µm)
1	HUD	(SEG55)	-447.6	-859.0
2	SEN1	(SEG54)	-357.6	-859.0
3	REF1	(SEG53)	-267.6	-859.0
4	RFIN1	(SEG52)	-177.6	-859.0
5	V_{SS}		-87.6	-859.0
6	P53/RFIN0	(SEG51)	2.4	-859.0
7	P52/REF0	(SEG50)	92.4	-859.0
8	P51/SEN0	(SEG49)	182.4	-859.0
9	P50/RFOUT	(SEG48)	272.4	-859.0
10	P23	(SEG47)	362.4	-859.0
11	P22	(SEG46)	452.4	-859.0
12	P21	(SEG45)	542.4	-859.0
13	P20	(SEG44)	632.4	-859.0
14	SEG9		854.0	-272.8
15	SEG8		854.0	-182.8
16	SEG7		854.0	-92.8
17	SEG6		854.0	-2.8
18	SEG5		854.0	87.2
19	SEG4		854.0	177.2
20	SEG3		854.0	267.2
21	SEG2		854.0	357.2
22	SEG1		854.0	447.2
23	SEG0		854.0	537.2
24	COM4		854.0	627.2
25	COM3		854.0	717.2

No.	Pad name	X (µm)	Y (µm)
26	COM2	560.1	859.0
27	COM1	470.1	859.0
28	COM0	380.1	859.0
29	CB	214.0	859.0
30	CA	124.0	859.0
31	V_{C3}	34.0	859.0
32	V_{C2}	-56.0	859.0
33	V_{C1}	-146.0	859.0
34	V_{OSC}	-236.0	859.0
35	OSC1	-326.0	859.0
36	OSC2	-416.0	859.0
37	V_{SS}	-506.0	859.0
38	V_{D1}	-854.0	171.5
39	V_{DD}	-854.0	81.5
40	TEST	-854.0	-8.5
41	RESET	-854.0	-98.5
42	P03/KRST03/KEY03	-854.0	-188.5
43	P02/KRST02/KEY02	-854.0	-278.5
44	P01/KRST01/KEY01	-854.0	-368.5
45	P00/KRST00/KEY00	-854.0	-458.5
46	P13/FOUT	-854.0	-548.5
47	P12/BZ	-854.0	-638.5
48	P11/TOUT_A	-854.0	-728.5
49	P10/EVIN_A	-854.0	-818.5

2.4.2 S1C63003 Pin Description

Table 2.4.2.1 S1C63003 pin description

Pin name		Pad/pin No.		I/O	OP	SFT	Function
Default	Shared function	Chip	QFP12-48				
V_{DD}		39	26	–	–	–	Power (+) supply pin
V_{SS}		5, 37	24	–	–	–	Power (-) supply pins
V_{D1}		38	25	–	–	–	Internal logic voltage regulator output pin
V_{OSC}		34	21	–	–	–	Crystal oscillation circuit operating voltage output pin
V_{C1}–V_{C3}		33–31	20–18	–	–	–	LCD system power supply pins
CA, CB		30, 29	17, 16	–	–	–	LCD system voltage boost/reduce capacitor connecting pins
OSC1		35	22	I	–	–	Crystal oscillation input pin
OSC2		36	23	O	–	–	Crystal oscillation output pin
P00	P00	45	32	I/o	–	D	I/O port pin
	KRST00			I	OP	–	Key reset input pin
	KEY00			I	–	SFT	Port interrupt input pin
P01	P01	44	31	I/o	–	D	I/O port pin
	KRST01			I	OP	–	Key reset input pin
	KEY01			I	–	SFT	Port interrupt input pin
P02	P02	43	30	I/o	–	D	I/O port pin
	KRST02			I	OP	–	Key reset input pin
	KEY02			I	–	SFT	Port interrupt input pin
P03	P03	42	29	I/o	–	D	I/O port pin
	KRST03			I	OP	–	Key reset input pin
	KEY03			I	–	SFT	Port interrupt input pin
P10	P10	49	36	I/o	–	D	I/O port pin
	EVIN_A			I	–	SFT	Event counter (programmable timer 0) input pin
P11	P11	48	35	I/o	–	D	I/O port pin
	TOUT_A			O	–	SFT	Programmable timer 0 output pin
P12	P12	47	34	I/o	–	D	I/O port pin
	BZ			O	–	SFT	Sound generator output pin
P13	P13	46	33	I/o	–	D	I/O port pin
	FOUT			O	–	SFT	FOUT clock output pin
P20	P20	13	48	I/o	OP	–	I/O port pin
	SEG44			O	OP	–	LCD segment output pin
P21	P21	12	47	I/o	OP	–	I/O port pin
	SEG45			O	OP	–	LCD segment output pin
P22	P22	11	46	I/o	OP	–	I/O port pin
	SEG46			O	OP	–	LCD segment output pin
P23	P23	10	45	I/o	OP	–	I/O port pin
	SEG47			O	OP	–	LCD segment output pin
P50	P50	9	44	I/o	OP	D	I/O port pin
	RFOUT			O		SFT	R/F converter CR oscillation clock output pin
	SEG48			O	OP	–	LCD segment output pin
P51	P51	8	43	I/o	OP	D	I/O port pin
	SEN0			O		SFT	R/F converter Ch.0 CR oscillation output pin for DC bias sensor
	SEG49			O	OP	–	LCD segment output pin
P52	P52	7	42	I/o	OP	D	I/O port pin
	REF0			O		SFT	R/F converter Ch.0 CR oscillation output pin for reference resistor
	SEG50			O	OP	–	LCD segment output pin
P53	P53	6	41	I/o	OP	D	I/O port pin
	RFIN0			I		SFT	R/F converter Ch.0 CR oscillation input pin
	SEG51			O	OP	–	LCD segment output pin
RFIN1	RFIN1	4	40	I	OP	–	R/F converter Ch.1 CR oscillation input pin
	SEG52			O	OP	–	LCD segment output pin
REF1	REF1	3	39	O	OP	–	R/F converter Ch.1 CR oscillation output pin for reference resistor
	SEG53			O	OP	–	LCD segment output pin
SEN1	SEN1	2	38	O	OP	–	R/F converter Ch.1 CR oscillation output pin for DC bias sensor
	SEG54			O	OP	–	LCD segment output pin
HUD	HUD	1	37	O	OP	–	R/F converter CR oscillation output pin for AC bias sensor
	SEG55			O	OP	–	LCD segment output pin
COM0–COM4		28–24	15–11	O	–	–	LCD common output pins
SEG0–SEG9		23–14	10–1	O	–	–	LCD segment output pins
RESET		41	28	I	–	–	Initial reset input pin
TEST		40	27	I	–	–	Test pin (Connect to V_{SS} during normal operation.)

I/O: Capital letters (I, O) represent the input/output direction in the initial settings.

OP: Selected by mask option ("–" means "no option provided.")

SFT: Switched by software ("–" means "no software switch provided" and "D" means default function.)

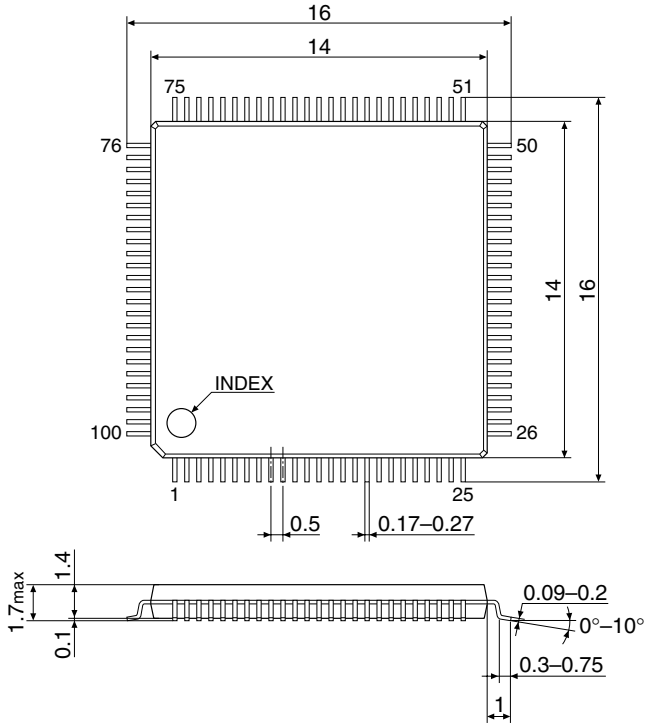
Note: The TEST terminal must be connected to the V_{SS} power supply. Be sure to avoid applying other conditions to the terminals during normal operation.

2.5 Package

2.5.1 Plastic Package

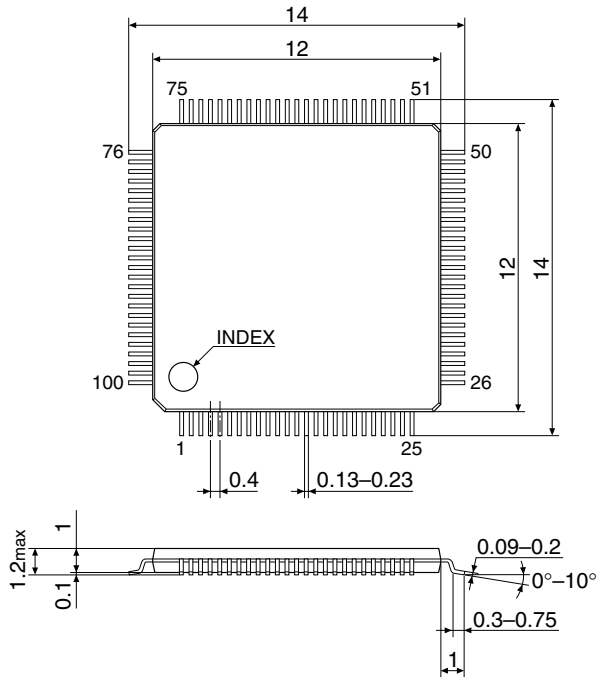
QFP15-100pin (S1C63008/016)

(Unit: mm)



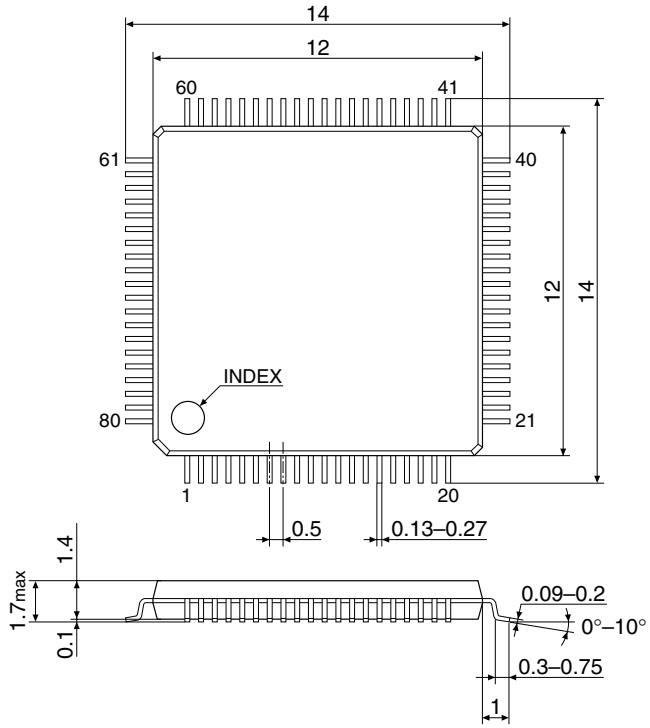
TQFP14-100pin (S1C63004/008/016)

(Unit: mm)



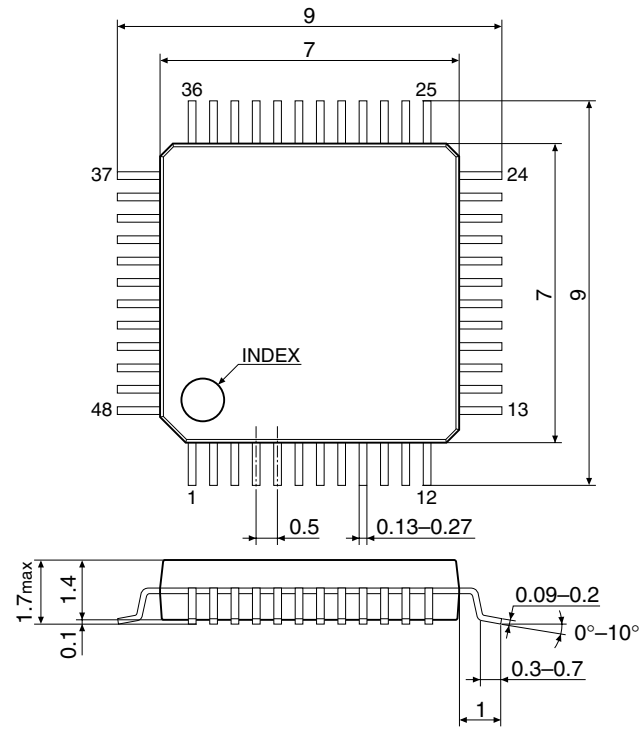
QFP14-80pin (S1C63004)

(Unit: mm)



QFP12-48pin (S1C63003)

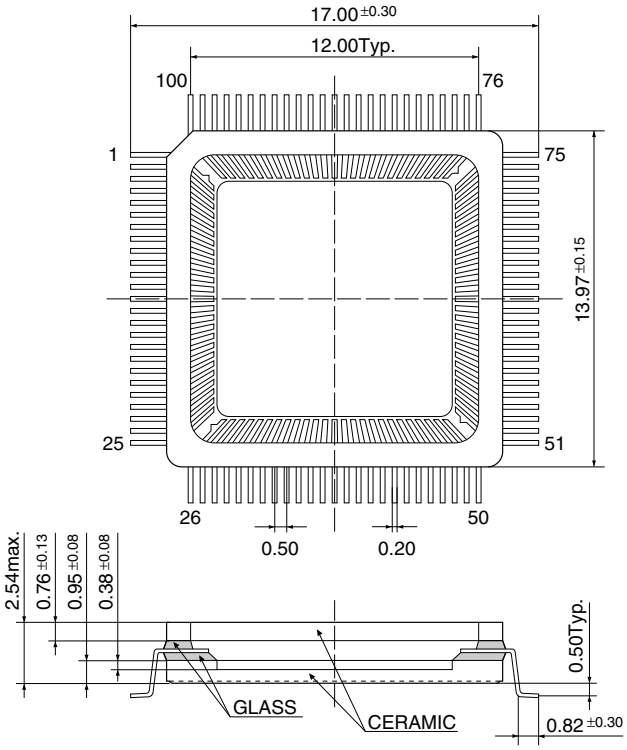
(Unit: mm)



2.5.2 Ceramic Package for Test Samples

QFP15-100pin (S1C63004/008/016)

(Unit: mm)



* Pin configuration
  S1C63016: Same as that of the QFP15-100pin/TQFP14-100pin plastic package.
  S1C63008: Same as that of the QFP15-100pin/TQFP14-100pin plastic package.
  S1C63004: Same as that of the TQFP14-100pin plastic package.

QFP13-64pin (S1C63003)

(Unit: mm)

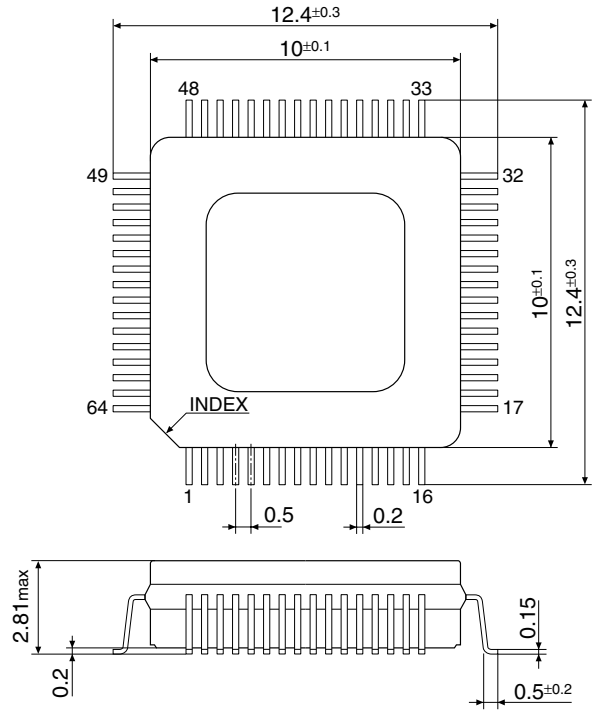


Table 2.5.2.1 Pin layout

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	17	N.C.	33	N.C.	49	N.C.
2	N.C.	18	N.C.	34	N.C.	50	N.C.
3	N.C.	19	COM2	35	N.C.	51	HUD (SEG55)
4	SEG9	20	COM1	36	V_{D1}	52	SEN1 (SEG54)
5	SEG8	21	COM0	37	V_{DD}	53	REF1 (SEG53)
6	SEG7	22	CB	38	TEST	54	RFIN1 (SEG52)
7	SEG6	23	CA	39	RESET	55	V_{SS}
8	SEG5	24	V_{C3}	40	P03/KRST03/KEY03	56	P53/RFIN0 (SEG51)
9	SEG4	25	V_{C2}	41	P02/KRST02/KEY02	57	P52/REF0 (SEG50)
10	SEG3	26	V_{C1}	42	P01/KRST01/KEY01	58	P51/SEN0 (SEG49)
11	SEG2	27	V_{OSC}	43	P00/KRST00/KEY00	59	P50/RFOUT (SEG48)
12	SEG1	28	OSC1	44	P13/FOUT	60	P23 (SEG47)
13	SEG0	29	OSC2	45	P12/BZ	61	P22 (SEG46)
14	COM4	30	V_{SS}	46	P11/TOUT_A	62	P21 (SEG45)
15	COM3	31	N.C.	47	P10/EVIN_A	63	P20 (SEG44)
16	N.C.	32	N.C.	48	N.C.	64	N.C.

3 CPU and Memory

3.1 CPU

The S1C63003/004/008/016 has a 4-bit core CPU S1C63000 built-in as its CPU part.
Refer to the "S1C63000 Core CPU Manual" for the S1C63000.

3.2 Code Memory Area

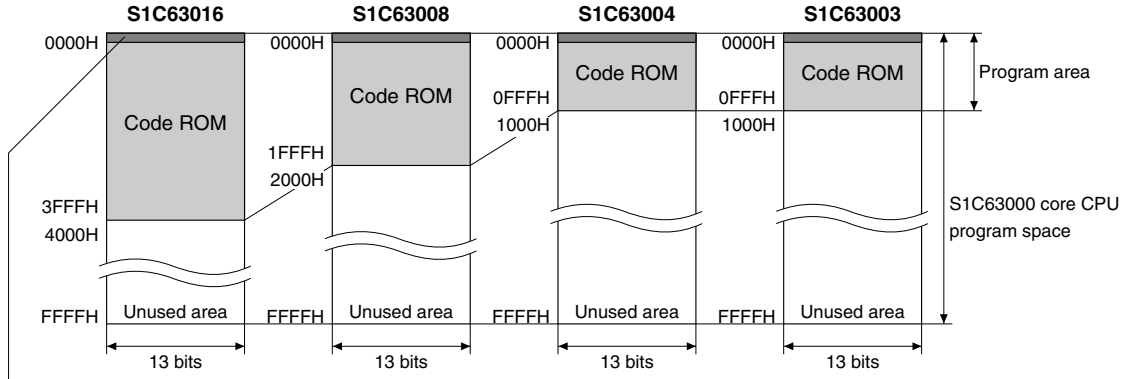
3.2.1 Code ROM

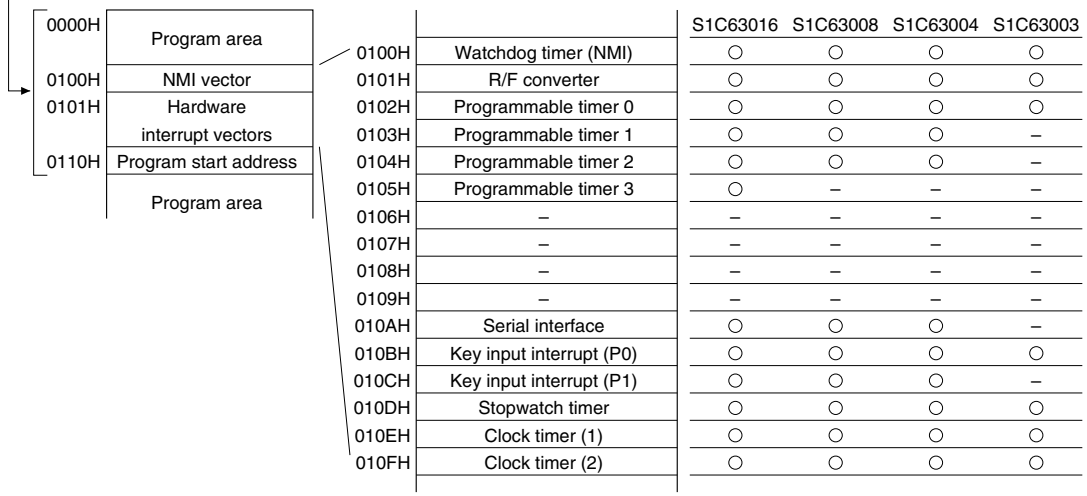
The built-in code ROM is a mask ROM for loading programs.

Table 3.2.1.1 Code ROM capacity

Model	Capacity	Address
S1C63016	16,384 words × 13 bits	0000H to 3FFFH
S1C63008	8,192 words × 13 bits	0000H to 1FFFH
S1C63004	4,096 words × 13 bits	0000H to 0FFFH
S1C63003	4,096 words × 13 bits	0000H to 0FFFH

The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0101H–010FH, respectively.





		S1C63016	S1C63008	S1C63004	S1C63003
0100H	Watchdog timer (NMI)	○	○	○	○
0101H	R/F converter	○	○	○	○
0102H	Programmable timer 0	○	○	○	○
0103H	Programmable timer 1	○	○	○	–
0104H	Programmable timer 2	○	○	○	–
0105H	Programmable timer 3	○	–	–	–
0106H	–	–	–	–	–
0107H	–	–	–	–	–
0108H	–	–	–	–	–
0109H	–	–	–	–	–
010AH	Serial interface	○	○	○	–
010BH	Key input interrupt (P0)	○	○	○	○
010CH	Key input interrupt (P1)	○	○	○	–
010DH	Stopwatch timer	○	○	○	○
010EH	Clock timer (1)	○	○	○	○
010FH	Clock timer (2)	○	○	○	○

Figure 3.2.1.1 Configuration of code ROM

3.3 Data Memory Area

The S1C63004/008/016 data memory consists of a RAM, data ROM, display memory and peripheral I/O memory. The S1C63003 data memory consists of a RAM, display memory and peripheral I/O memory. Figure 3.3.1 shows the overall memory map.

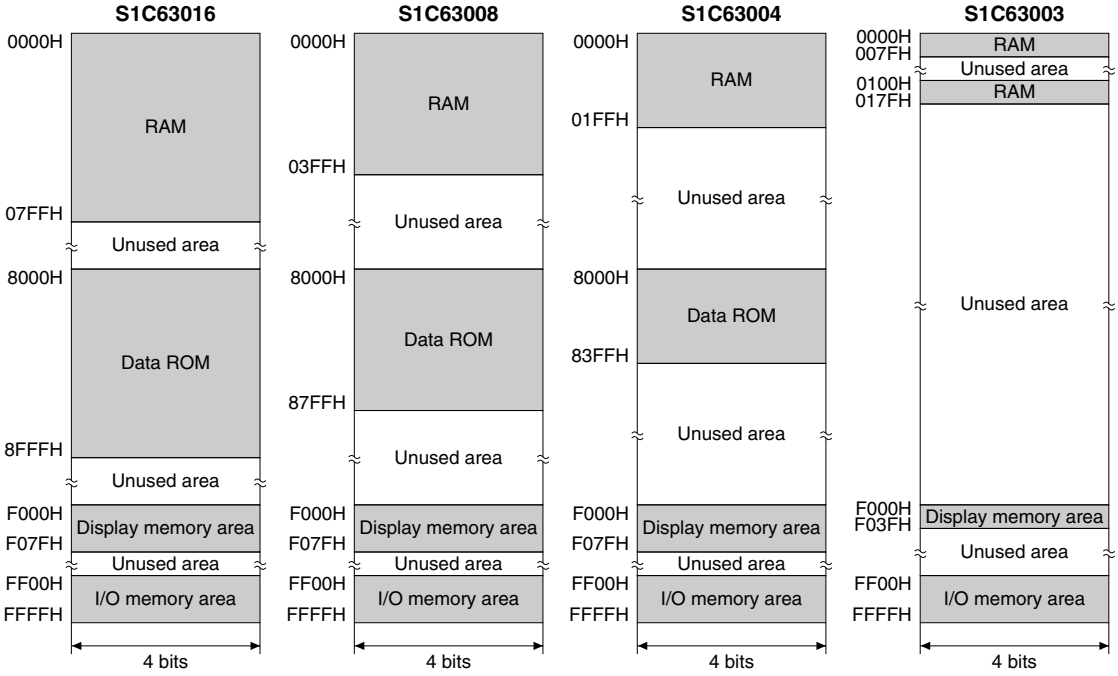


Figure 3.3.1 Data memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps in the Appendix for the peripheral I/O area.

3.3.1 RAM

The RAM is a data memory for storing various kinds of data.

Table 3.3.1.1 RAM capacity

Model	Capacity	Address
S1C63016	2,048 words × 4 bits	0000H to 07FFH
S1C63008	1,024 words × 4 bits	0000H to 03FFH
S1C63004	512 words × 4 bits	0000H to 01FFH
S1C63003	256 words × 4 bits	0000H to 007FH, 0100H to 017FH

Addresses 0100H to 01FFH (0100H to 017FH in the S1C63003) are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1). 16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH, 0100H to 017FH in the S1C63003). Memory accesses except for stack operations by SP1 are 4-bit data access.
The stack address management requires caution as the stack pointers may be set to an address out of the RAM address range.

After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

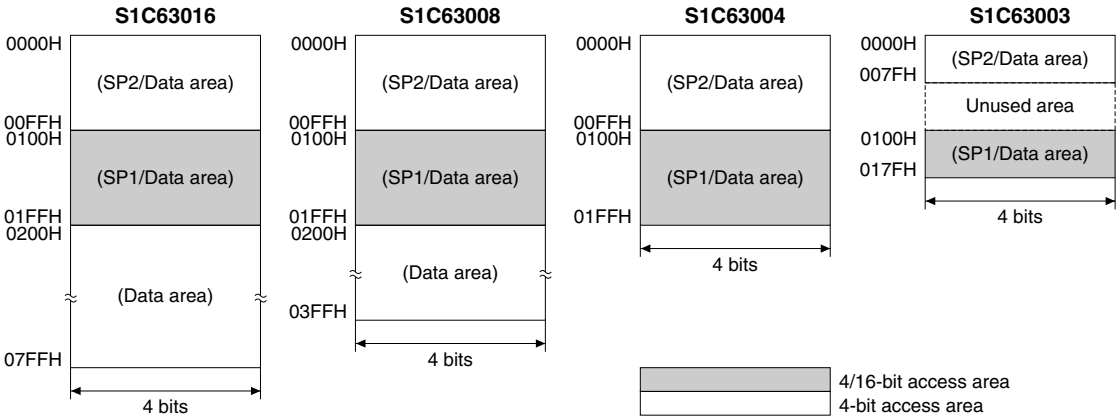


Figure 3.3.1.1 RAM configuration

3.3.2 Data ROM

The data ROM is used for loading various static data such as a character generator, and data can be read using the same data memory access instructions as the RAM.

Table 3.3.2.1 Data ROM capacity

Model	Capacity	Address
S1C63016	4,096 words × 4 bits	8000H to 8FFFH
S1C63008	2,048 words × 4 bits	8000H to 87FFH
S1C63004	1,024 words × 4 bits	8000H to 83FFH
S1C63003	Not available	

3.3.3 Display Memory

The display memory is a RAM used for storing LCD display data and is assigned to the data memory area. Each bit can be assigned to the specific segment terminal by mask option.
The addresses that are not used for LCD display can be used as general purpose registers.

Table 3.3.3.1 Display memory capacity

Model	Capacity *	Address
S1C63016	448 bits	F000H to F07FH
S1C63008	400 bits	F000H to F07FH
S1C63004	288 bits	F000H to F07FH
S1C63003	110 bits	F000H to F03FH

* These values are the maximum number of bits that can be allocated for the segment outputs. Any address within the range listed above can be specified.

3.3.4 I/O Memory

The peripheral circuits of S1C63003/004/008/016 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions.
The control registers for the peripheral circuits are located in the I/O memory area as shown in the figure below. Refer to the Appendix for the register list and descriptions of each peripheral circuit for details of the registers.

		S1C63xxx			
Address	Peripheral circuit	016	008	004	003
FF00H	Oscillation circuit	○	○	○	○
FF01H	Watchdog timer	○	○	○	○
FF03H	Power supply circuit	○	○	○	○
FF04H–FF05H	SVD circuit	○	○	○	–
FF10H–FF1BH	Clock manager	○	○	○	○
FF20H–FF3FH	I/O ports and input interrupt control	○	○	○	○
FF40H–FF42H	Clock timer	○	○	○	○
FF44H–FF47H	Sound generator	○	○	○	○
FF48H–FF4DH	Stopwatch timer	○	○	○	○
FF50H–FF52H	LCD driver	○	○	○	○
FF58H–FF5CH	Serial interface	○	○	○	–
FF60H–FF6BH	R/F converter	○	○	○	○
FF70H–FF76H	Integer multiplier	○	○	–	–
FF80H–FF9FH	Programmable timer	○	○	○	○
FFE1H–FFFFH	Interrupt controller	○	○	○	○

Figure 3.3.4.1 I/O memory map

4 Initial Reset

4.1 Initial Reset Circuit

The S1C63003/004/008/016 should be reset to initialize the internal circuits. There are two ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous high input to P00–P03 ports (mask option)

The circuits are initialized by either (1) or (2). When the power is turned on, be sure to initialize using the reset function. It is not guaranteed that the circuits are initialized by only turning the power on.
Figure 4.1.1 shows the configuration of the initial reset circuit.

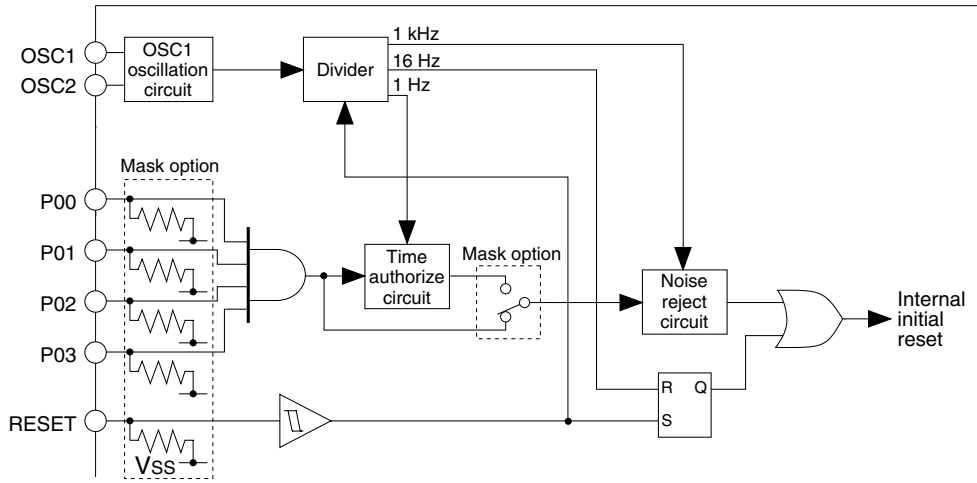


Figure 4.1.1 Configuration of initial reset circuit

4.2 Reset Terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level (V_{DD}). After that the initial reset is released by setting the reset terminal to a low level (V_{SS}) and the CPU starts operating. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 16 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 1,024/f_{OSC1} seconds (32 msec when f_{OSC1} = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to low level. Be sure to maintain a reset input of 0.1 msec or more. However, when turning the power on, the reset terminal should be set at a high level as in the timing shown in Figure 4.2.1.
Note that a reset pulse shorter than 100 nsec is rejected as noise.

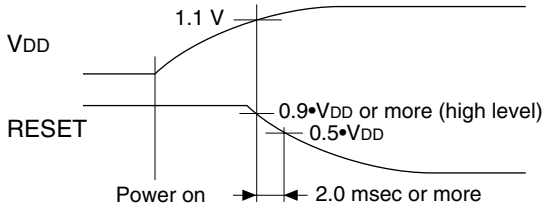


Figure 4.2.1 Initial reset at power on

The reset terminal should be set to 0.9•V_{DD} or more (high level) until the supply voltage becomes 1.1 V or more. After that, a level of 0.5•V_{DD} or more should be maintained more than 2.0 msec.
The reset terminal incorporates a pull-down resistor and a mask option is provided to select whether the resistor is used or not.

4.3 Simultaneous High Input to P0x Ports (P00–P03)

Another way of executing initial reset externally is to input high level signals simultaneously to the P0x ports (P00–P03) selected by a mask option. Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency fosc1 is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at high level for at least 1.5 msec (when the oscillation frequency fosc1 is 32.768 kHz) after oscillation starts. Table 4.3.1 shows the combinations of P0x ports (P00–P03) that can be selected by a mask option.

Table 4.3.1 Combinations of P0x ports

No.	Combination
1	Not used
2	P00 * P01
3	P00 * P01 * P02
4	P00 * P01 * P02 * P03

When, for instance, mask option 4 (P00 * P01 * P02 * P03) is selected, initial reset is executed when the signals input to the four ports P00–P03 are all high at the same time. When 2 or 3 is selected, the initial reset is done when a key entry including a combination of selected input ports is made. Further, the time authorize circuit mask option is selected when this reset function is selected. The time authorize circuit checks the input time of the simultaneous high input and performs initial reset if that time is the defined time (1 to 2 sec) or more. If using this function, make sure that the specified ports do not go high at the same time during ordinary operation.

4.4 Internal Register at Initial Resetting

Initial reset initializes the CPU as shown in Table 4.4.1.
The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.
When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 4.4.1 Initial values

CPU core			
Name	Symbol	Bit length	Set value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuit		
Name	Bit length	Set value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	–	*

* See "I/O Memory Map."

4.5 Terminal Settings at Initial Resetting

The I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface, R/F converter, stopwatch timer and programmable timer (event counter). These functions are selected by software. At initial reset, these terminals are configured to the general purpose I/O port terminals. Set them according to the system in the initial routine.
Table 4.5.1 shows the list of the shared terminal settings.

Table 4.5.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	When special outputs/peripheral functions are used (selected by software)							
		Special output			Serial I/F *2		R/F converter	Stopwatch direct input *2	Event counter
		TOUT	FOUT	BZ	Master	Slave			
P00	P00 (IN & PD *1)							RUN/STOP	
P01	P01 (IN & PD *1)							LAP	
P02	P02 (IN & PD *1)								
P03	P03 (IN & PD *1)								
P10	P10 (IN & PD *1)								EVIN_A
P11	P11 (IN & PD *1)	TOUT_A							
P12	P12 (IN & PD *1)			BZ					
P13	P13 (IN & PD *1)		FOUT						
P20–P21	P20–P21 (IN & PD *1)								
P22	P22 (IN & PD *1)								EVIN_B *2
P23	P23 (IN & PD *1)	TOUT_B *2							
P30 *2	P30 (IN & PD *1)				SCLK(O)	SCLK(I)			
P31 *2	P31 (IN & PD *1)				SOUT(O)	SOUT(O)			
P32 *2	P32 (IN & PD *1)				SIN(I)	SIN(I)			
P33 *2	P33 (IN & PD *1)					SRDY(O)/$\overline{SS}$(I)			
P40–P43 *3	P40–P43 (IN & PD *1)								
P50	P50 (IN & PD *1)						RFOUT		
P51	P51 (IN & PD *1)						SEN0		
P52	P52 (IN & PD *1)						REF0		
P53	P53 (IN & PD *1)						RFIN0		

*1: IN & PD (Input with pulled down): When "Pull-Down Used" is selected by mask option (high impedance when "Pull-Down Not Used" is selected)
*2: The P30 to P33 ports, serial interface, stopwatch direct input, TOUT_B output, and EVIN_B input functions are not available in the S1C63003.
*3: The P40 to P43 ports are not available in the S1C63003/004.

For setting procedure of the functions, see explanations for each of the peripheral circuits.

5 Power Supply

5.1 Operating Voltage

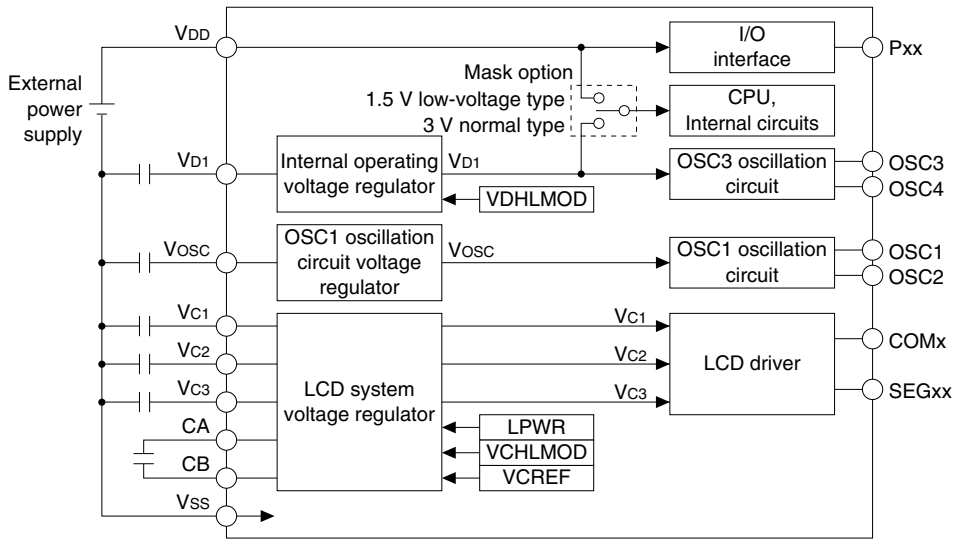
The S1C63003/004/008/016 operating power voltage (V_{DD}) is as follows. It depends on the mask option selection (3 V normal type or 1.5 V low-voltage type).

3 V normal type: V_{DD} = 1.8 to 5.5 V
1.5 V low-voltage type: V_{DD} = 1.1 to 1.7 V

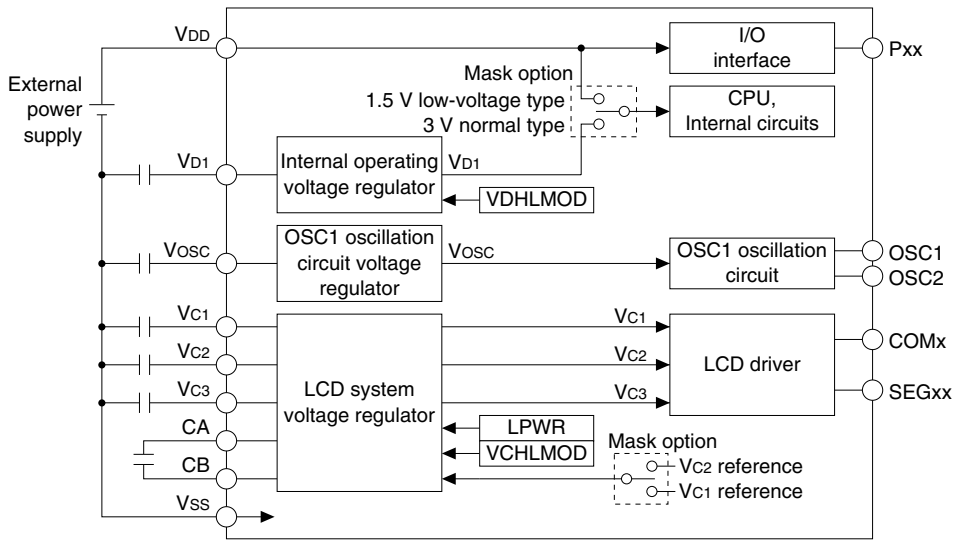
Supply a voltage within this range to between V_{DD} (+) and V_{SS} (GND).

5.2 Internal Power Supply Circuit

The S1C63003/004/008/016 incorporates the power supply circuits shown in Figure 5.2.1 so the voltages to drive the CPU, internal logic circuits, oscillation circuits and LCD driver can be generated on the chip.



(a) S1C63004/008/016



(b) S1C63003

Figure 5.2.1 Internal power supply circuit

The power supply circuit is broadly divided into three blocks.

Table 5.2.1 Power supply circuit

Power supply circuit/power supply voltage	Output voltage	Circuits to be driven	
		3 V normal type	1.5 V low-voltage type
Internal operating voltage regulator	V_{D1}	CPU, internal circuits, and OSC3 oscillation circuit	OSC3 oscillation circuit
OSC1 oscillation circuit voltage regulator	V_{OSC}	OSC1 oscillation circuit	
LCD system voltage regulator	V_{C1}–V_{C3}	LCD driver	
Power supply voltage V_{DD}	–	Power supply circuit, and I/O	Power supply circuit, CPU, internal circuits, and I/O

Internal operating voltage regulator

This voltage regulator always operates to generate the V_{D1} operating voltage for the CPU, internal logic circuits and the OSC3 oscillation circuits.

(The CPU and internal logic circuits in the 1.5 V low-voltage type operate with the power supply voltage V_{DD}.)

OSC1 oscillation circuit voltage regulator

This voltage regulator always operates to generate the V_{OSC} operating voltage for the OSC1 oscillation circuit.

LCD system voltage regulator

The LCD system voltage regulator generates the LCD drive voltages V_{C1} to V_{C3}. See "Electrical Characteristics" for the voltage values. In the S1C63003/004/008/016, the LCD drive voltage is supplied to the built-in LCD driver that drives the LCD panel connected to the SEG and COM terminals.

The LCD system voltage regulator can be disabled by mask option to supply external voltages. In this case, external elements can be minimized because the external capacitors for the LCD system voltage regulator are not necessary. However when the LCD system voltage regulator is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system voltage regulator is used.

Figure 5.2.2 shows the external element configuration when an external LCD power supply is used.

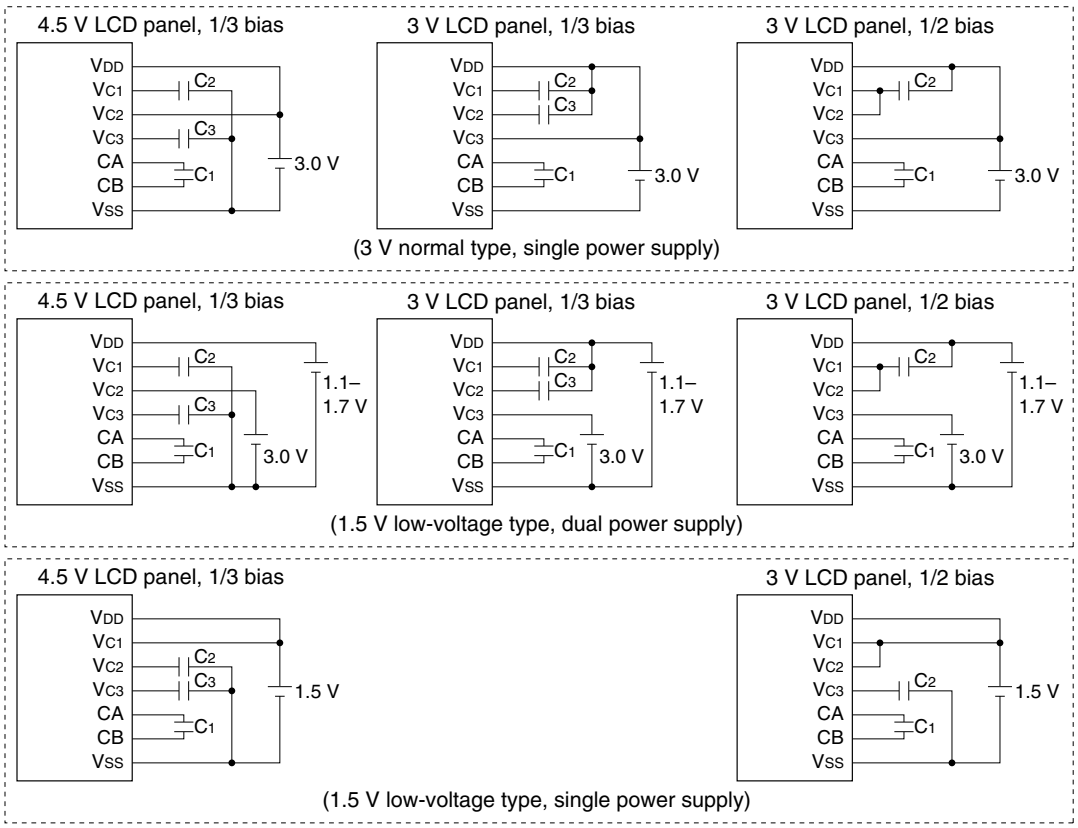


Figure 5.2.2 External elements when an external LCD power supply is used

Notes: • Do not use the V_{D1}, V_{OSC}, and V_{C1} to V_{C3} terminal output voltages to drive external circuits.

• When 1/2 bias is selected, the V_{C1} and V_{C2} pins are connected inside the IC.

5.3 Controlling LCD Power Supply

The LCD system voltage regulator generates the reference voltage V_{C1} or V_{C2} and generates two other voltages ($V_{C2} = V_{C1} \times 2$, $V_{C3} = V_{C1} \times 3$, or $V_{C1} = V_{C2} \times 1/2$, $V_{C3} = V_{C2} \times 3/2$) by boosting or reducing V_{C1}/V_{C2}.
The reference voltage to be generated should be selected from V_{C1} and V_{C2} according to the supply voltage V_{DD}. In the S1C63004/008/016, use the VCREF register to select the reference voltage with consideration given to the contrast of display in addition to the supply voltage. In the S1C63003, it can be selected by mask option. Also refer to the LCD drive voltage - supply voltage characteristics (in the “Electrical Characteristics - Characteristics Curves” section) and select the appropriate reference voltage according to the system.
To generate the LCD drive voltages by the LCD system voltage regulator (to start LCD display), turn the LCD system voltage regulator on using the LPWR register. When "1" is written to LPWR, the LCD system voltage regulator goes on and generates the LCD drive voltages. At initial reset, LPWR is set to "0" (Off).
When LCD display is not needed, turn the LCD system voltage regulator off to reduce power consumption.

Notes: • The LCD system voltage regulator takes about 100 msec for stabilizing the LCD drive voltages after writing "1" to LPWR.

• Do not select the reference voltage V_{C2} for the S1C63003 1.5 V low-voltage type.

Furthermore, the LCD system voltage regulator uses the boost clock supplied from the clock manager for boosting/reducing the voltage. The clock supply is controlled by the VCCKS[1:0] register. Set VCCKS[1:0] to "1" before writing "1" to LPWR. When LCD display is not necessary, stop the clock supply by setting VCCKS[1:0] to "0" to reduce power consumption.

Table 5.3.1 Controlling boost clock

VCCKS[1:0]	Boost clock control
3 or 2	Prohibited
1	On (2 kHz)
0	Off

5.4 Heavy Load Protection Function

In order to ensure a stable circuit behavior and LCD display quality even if the power supply voltage fluctuates due to driving an external load, the internal operating voltage regulator and the LCD system voltage regulator have a heavy load protection function.
The internal operating voltage regulator enters heavy load protection mode by writing "1" to the VDHLMOD register and it ensures stable V_{D1} output. Use the heavy load protection function when a heavy load such as a lamp or buzzer is driven with a port output.

The LCD system voltage regulator enters heavy load protection mode by writing "1" to the VCHLMOD register and it ensures stable V_{C1}–V_{C3} outputs. Use the heavy load protection function when the LCD display has inconsistencies in density.

Note: Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode with software if unnecessary.

5.5 I/O Memory for Power Supply Circuit

Table 5.5.1 shows the I/O address and the control bits for power supply control.

Table 5.5.1 Power supply control bits

Address		Register name	R/W	Default	Setting/data				Function
FF03H	D3	**VCHLMOD**	R/W	0	1	On	0	Off	V_C regulator heavy load protection mode On/Off
	D2	**VDHLMOD**	R/W	0	1	On	0	Off	V_D regulator heavy load protection mode On/Off
	D1	**VCREF** (∗6)	R/W	0	1	V_{C2}	0	V_{C1}	V_C regulator reference voltage selection
	D0	**LPWR**	R/W	0	1	On	0	Off	V_C regulator On/Off
FF12H	D3	FLCKS1	R/W	0	3	–	1	21.3	Frame frequency (Hz) selection
	D2	FLCKS0	R/W	0	2	16.0	0	32.0	
	D1	**VCCKS1**	R/W	0	3	–	1	2048	V_C boost frequency (Hz) selection
	D0	**VCCKS0**	R/W	0	2	–	0	Off	

∗1 Initial value at initial reset ∗2 Not set in the circuit ∗3 Constantly "0" when being read
∗4 Unused in the S1C63003/004/008 ∗5 Unused in the S1C63003/004 ∗6 Unused in the S1C63003

LPWR: V_C regulator On/Off register (FF03H•D0)

Turns the LCD system voltage regulator on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to LPWR, the LCD system voltage regulator goes on and generates the LCD drive voltages. When "0" is written, all the LCD drive voltages go to Vss level. It takes about 100 msec for the LCD drive voltages to stabilize after starting up the LCD system voltage regulator by writing "1" to LPWR. At initial reset, this register is set to "0."

VCREF: V_C regulator reference voltage select register (FF03H•D1) – S1C63004/008/016

Selects the reference voltage generated in the LCD system voltage regulator.

When "1" is written: V_{C2}
When "0" is written: V_{C1}
Reading: Valid

When "1" is written to VCREF, the LCD system voltage regulator generates the reference voltage V_{C2} and generates two other voltages ($V_{C1} = V_{C2} \times 1/2$, $V_{C3} = V_{C2} \times 3/2$) by boosting and reducing V_{C2}. When VCREF is "0," the LCD system voltage regulator generates the reference voltage V_{C1} and generates two other voltages ($V_{C2} = V_{C1} \times 2$, $V_{C3} = V_{C1} \times 3$) by boosting V_{C1}. The reference voltage should be selected from V_{C1} and V_{C2} with consideration given to the supply voltage V_{DD} and contrast of display. Also refer to the LCD drive voltage - supply voltage characteristics (in the "Electrical Characteristics - Characteristics Curves" section) and select the appropriate reference voltage according to the system. At initial reset, this register is set to "0."
In the S1C63003, the reference voltage is selected by mask option.

VDHLMOD: V_D regulator heavy load protection mode On/Off register (FF03H•D2)

Enables heavy load protection function for the internal operating voltage regulator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

By writing "1" to VDHLMOD, the internal operating voltage regulator enters heavy load protection mode and it ensures stable V_{D1} output. The heavy load protection function is effective when the buzzer/FOUT signal is being output. However, heavy load protection mode increases current consumption compared with normal operation mode. Therefore, do not set heavy load protection mode unless it is necessary. At initial reset, this register is set to "0."

VCHLMOD: Vc regulator heavy load protection mode On/Off register (FF03H•D3)

Enables heavy load protection function for the LCD system voltage regulator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

By writing "1" to VCHLMOD, the LCD system voltage regulator enters heavy load protection mode to minimize degradation in display quality when fluctuations in the supply voltage occurs due to driving a heavy load. The heavy load protection function is effective when the OSC3 clock is used or the buzzer/FOUT signal is being output. However, heavy load protection mode increases current consumption compared with normal operation mode. Therefore, do not set heavy load protection mode unless it is necessary. At initial reset, this register is set to "0."

VCCKS[1:0]: Vc boost frequency select register (FF12H•D[1:0])

Controls the boost clock supply to the LCD system voltage regulator.

Table 5.5.2 Controlling boost clock

VCCKS[1:0]	Boost clock control
3 or 2	Prohibited
1	On (2 kHz)
0	Off

The LCD system voltage regulator uses the boost clock supplied from the clock manager for boosting/reducing the voltage. Use this register to control the clock supply. Set VCCKS[1:0] to "1" before writing "1" to LPWR. When LCD display is not necessary, stop the clock supply by setting VCCKS[1:0] to "0" to reduce power consumption. At initial reset, this register is set to "0."

5.6 Precautions

- When a 3.0 V LCD drive voltage is supplied to the V_{C3} or V_{C2} terminal in the 1.5 V low-voltage type, use separated power sources for V_{DD} and V_{C3}/V_{C2} and supply a voltage within 1.1 V to 1.7 V to the V_{DD} terminal.
- Do not use the V_{D1}, V_{OSC}, and V_{C1} to V_{C3} terminal output voltages to drive external circuits.
- The LCD system voltage regulator takes about 100 msec for stabilizing the LCD drive voltages after writing "1" to LPWR.
- Do not select the reference voltage V_{C2} for the S1C63003 1.5 V low-voltage type.
- Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode with software if unnecessary.

6 Interrupt Controller

6.1 Configuration of Interrupt Controller

The S1C63003/004/008/016 supports the interrupts listed below.

Table 6.1.1 Interrupt types

Interrupt		S1C63016	S1C63008	S1C63004	S1C63003
External interrupt	Key input interrupt	8 systems			4 systems
Internal interrupt	Watchdog timer interrupt	NMI, 1 system			
	Programmable timer interrupt	8 systems	6 systems		1 system
	Serial interface interrupt	1 system			–
	Clock timer interrupt	8 systems			4 systems
	Stopwatch timer interrupt	4 systems			2 systems
	R/F converter interrupt	3 systems			

To enable an interrupt, the interrupt flag must be set to "1" (EI) and the corresponding interrupt mask register must be set to "1" (enable).
When an interrupt occurs, the interrupt flag is automatically reset to "0" (DI), and interrupts after that are disabled.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to disable NMI since software can stop the watchdog timer operation.

Figure 6.1.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

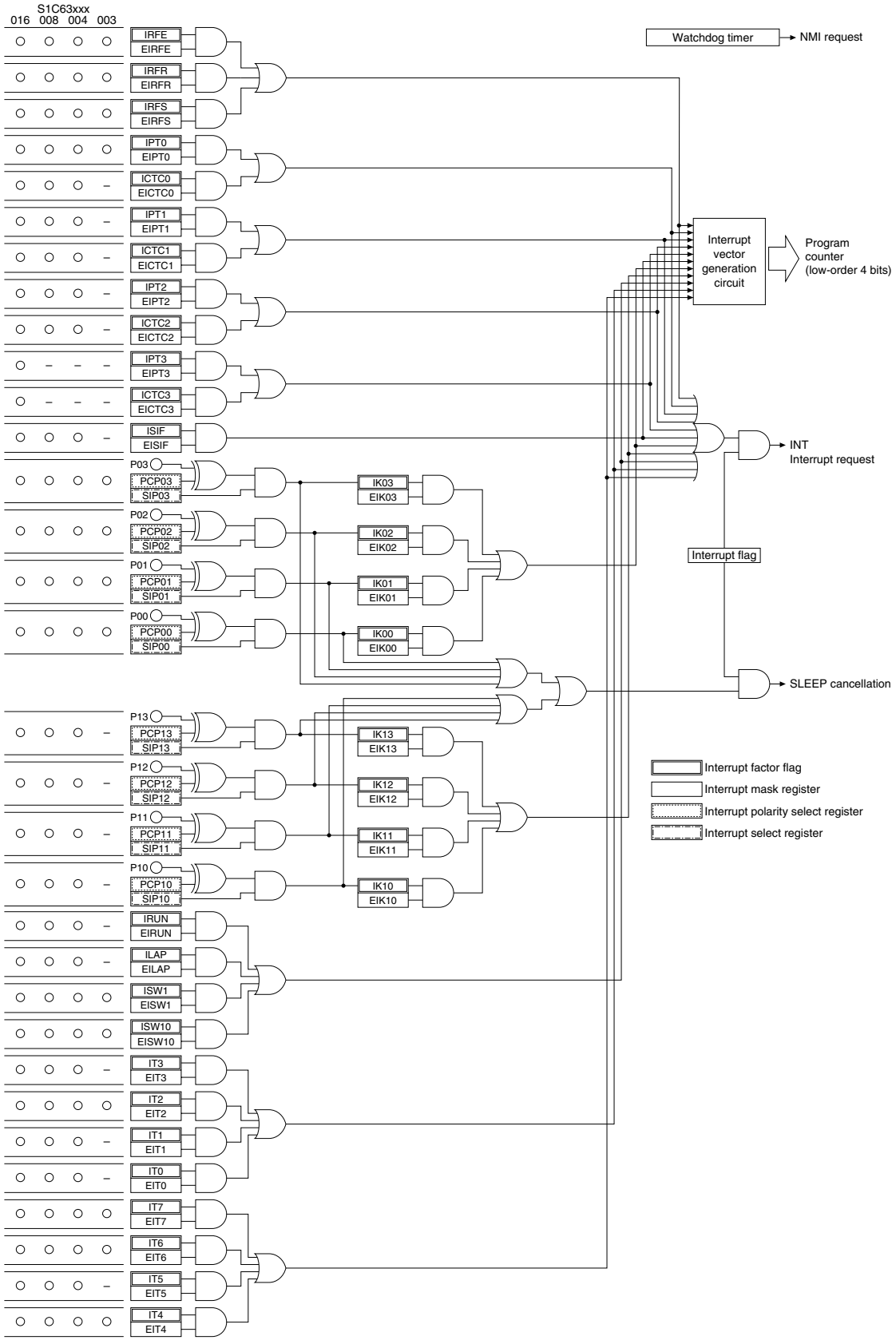


Figure 6.1.1 Configuration of the interrupt circuit

6.2 Interrupt Factors

Table 6.2.1 shows the factors for generating interrupt requests. The interrupt flags are set to "1" depending on the corresponding interrupt factors. The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0."

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 6.2.1 Interrupt factors

Interrupt factor	Interrupt factor flag		Interrupt mask register		S1C63xxx			
					016	008	004	003
R/F converter (error)	IRFE	(FFF1H•D2)	EIRFE	(FFE1H•D2)	○	○	○	○
R/F converter (end of reference conversion)	IRFR	(FFF1H•D1)	EIRFR	(FFE1H•D1)	○	○	○	○
R/F converter (end of sensor conversion)	IRFS	(FFF1H•D0)	EIRFS	(FFE1H•D0)	○	○	○	○
Programmable timer 0 (underflow)	IPT0	(FFF2H•D1)	EIPT0	(FFE2H•D1)	○	○	○	○
Programmable timer 0 (compare match)	ICTC0	(FFF2H•D0)	EICTC0	(FFE2H•D0)	○	○	○	–
Programmable timer 1 (underflow)	IPT1	(FFF3H•D1)	EIPT1	(FFE3H•D1)	○	○	○	–
Programmable timer 1 (compare match)	ICTC1	(FFF3H•D0)	EICTC1	(FFE3H•D0)	○	○	○	–
Programmable timer 2 (underflow)	IPT2	(FFF4H•D1)	EIPT2	(FFE4H•D1)	○	○	○	–
Programmable timer 2 (compare match)	ICTC2	(FFF4H•D0)	EICTC2	(FFE4H•D0)	○	○	○	–
Programmable timer 3 (underflow)	IPT3	(FFF5H•D1)	EIPT3	(FFE5H•D1)	○	–	–	–
Programmable timer 3 (compare match)	ICTC3	(FFF5H•D0)	EICTC3	(FFE5H•D0)	○	–	–	–
Serial interface (8-bit data input/output completion)	ISIF	(FFFAH•D0)	EISEIF	(FFEAH•D0)	○	○	○	–
Key input interrupt <P03>	IK03	(FFFBH•D3)	EIK03	(FFEBH•D3)	○	○	○	○
Key input interrupt <P02>	IK02	(FFFBH•D2)	EIK02	(FFEBH•D2)	○	○	○	○
Key input interrupt <P01>	IK01	(FFFBH•D1)	EIK01	(FFEBH•D1)	○	○	○	○
Key input interrupt <P00>	IK00	(FFFBH•D0)	EIK00	(FFEBH•D0)	○	○	○	○
Key input interrupt <P13>	IK13	(FFFCH•D3)	EIK13	(FFECH•D3)	○	○	○	–
Key input interrupt <P12>	IK12	(FFFCH•D2)	EIK12	(FFECH•D2)	○	○	○	–
Key input interrupt <P11>	IK11	(FFFCH•D1)	EIK11	(FFECH•D1)	○	○	○	–
Key input interrupt <P10>	IK10	(FFFCH•D0)	EIK10	(FFECH•D0)	○	○	○	–
Stopwatch timer (Direct RUN)	IRUN	(FFFDH•D3)	EIRUN	(FFEDH•D3)	○	○	○	–
Stopwatch timer (Direct LAP)	ILAP	(FFFDH•D2)	EILAP	(FFEDH•D2)	○	○	○	–
Stopwatch timer (1 Hz)	ISW1	(FFFDH•D1)	EISW1	(FFEDH•D1)	○	○	○	○
Stopwatch timer (10 Hz)	ISW10	(FFFDH•D0)	EISW10	(FFEDH•D0)	○	○	○	○
Clock timer 16 Hz (falling edge)	IT3	(FFFEH•D3)	EIT3	(FFEEH•D3)	○	○	○	–
Clock timer 32 Hz (falling edge)	IT2	(FFFEH•D2)	EIT2	(FFEEH•D2)	○	○	○	○
Clock timer 64 Hz (falling edge)	IT1	(FFFEH•D1)	EIT1	(FFEEH•D1)	○	○	○	–
Clock timer 128 Hz (falling edge)	IT0	(FFFEH•D0)	EIT0	(FFEEH•D0)	○	○	○	–
Clock timer 1 Hz (falling edge)	IT7	(FFFFH•D3)	EIT7	(FFEFH•D3)	○	○	○	○
Clock timer 2 Hz (falling edge)	IT6	(FFFFH•D2)	EIT6	(FFEFH•D2)	○	○	○	○
Clock timer 4 Hz (falling edge)	IT5	(FFFFH•D1)	EIT5	(FFEFH•D1)	○	○	○	–
Clock timer 8 Hz (falling edge)	IT4	(FFFFH•D0)	EIT4	(FFEFH•D0)	○	○	○	○

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt handler routine before shifting to the interrupt enabled state.

6.3 Interrupt Mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them. At initial reset, the interrupt mask register is reset to "0." Table 6.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

6.4 Interrupt Vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1. The content of the flag register is evacuated, then the I flag is reset.
2. The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
3. The interrupt request causes the value of the interrupt vector (0100H–010FH) to be set in the program counter.
4. The program at the specified address is executed (execution of interrupt handler routine by software).

Table 6.4.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 6.4.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	S1C63xxx				Priority
		016	008	004	003	
0100H	Watchdog timer	○	○	○	○	High
0101H	R/F converter	○	○	○	○	↑
0102H	Programmable timer 0	○	○	○	○	
0103H	Programmable timer 1	○	○	○	–	
0104H	Programmable timer 2	○	○	○	–	
0105H	Programmable timer 3	○	–	–	–	
0106H	Reserved	–	–	–	–	
0107H	Reserved	–	–	–	–	
0108H	Reserved	–	–	–	–	
0109H	Reserved	–	–	–	–	
010AH	Serial interface	○	○	○	–	
010BH	Key input interrupt <P0>	○	○	○	○	
010CH	Key input interrupt <P1>	○	○	○	–	
010DH	Stopwatch timer	○	○	○	○	
010EH	Clock timer (128 Hz, 64 Hz, 32 Hz, 16 Hz)*	○	○	○	○	↓
010FH	Clock timer (8 Hz, 4 Hz, 2 Hz, 1 Hz)*	○	○	○	○	Low

* The S1C63003 supports 32 Hz, 8 Hz, 2 Hz, and 1 Hz interrupts only.

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

Note: The interrupt handler routine must be located within the range from "Interrupt vector address (100H–10FH)" -7FH to +80H. If it is difficult, make a relay point within that range as the destination of the vector jump and branch the program to the interrupt handler from there.
Example:

```
;******************************************************************************
;**  interrupt vector area  **
;******************************************************************************
      .org  0x0100
      JR    INT_DUMMY   ;WATCH DOG TIMER INTERRUPT VECTOR(0x100)
      JR    INT_RFC     ;RFC INTERRUPT VECTOR(0x101)
      JR    INT_DUMMY   ;PTIMER0 INTERRUPT VECTOR(0x102)
      JR    INT_DUMMY   ;PTIMER1 INTERRUPT VECTOR(0x103)
      JR    INT_DUMMY   ;PTIMER2 INTERRUPT VECTOR(0x104)
      JR    INT_DUMMY   ;PTIMER3 INTERRUPT VECTOR(0x105)
      JR    INT_DUMMY   ;Reserved
      JR    INT_DUMMY   ;Reserved
      JR    INT_DUMMY   ;Reserved
      JR    INT_DUMMY   ;Reserved
      JR    INT_DUMMY   ;SIF INTERRUPT VECTOR(0x10A)
      JR    INT_DUMMY   ;P0x PORT INTERRUPT VECTOR(0x10B)
      JR    INT_DUMMY   ;P1x PORT INTERRUPT VECTOR(0x10C)
      JR    INT_DUMMY   ;STOPWATCH INTERRUPT VECTOR(0x10D)
      JR    INT_DUMMY   ;CLOCK TIMER1 INTERRUPT VECTOR(0x10E)
      JR    INT_DUMMY   ;CLOCK TIMER2 INTERRUPT VECTOR(0x10F)

;******************************************************************************
;**  subinterrupt vector area  **
;******************************************************************************
      .org  0x120
INT_RFC:
```

```
      CALR  INTRFC      ;call Interrupt RFC
      RETI
INT_DUMMY:
      RETI

;*****************************************************************************
;**  Interrupt RFC  **
;*****************************************************************************
      .org  0x800
INTRFC:
      LDB   %yl,P5CTL0@l
      LDB   %xl,ITC_RFC1@l
      LD    [%y],[%x]   ;Port Output
      RET
```

6.5 I/O Memory of Interrupt Controller

Table 6.5.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 6.5.1 Control bits of interrupt controller

Address		Register name	R/W	Default	Setting/data				Function
FFE1H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	**EIRFE**	R/W	0	1	Enable	0	Mask	Interrupt mask register (RFC error)
	D1	**EIRFR**	R/W	0	1	Enable	0	Mask	Interrupt mask register (RFC REF completion)
	D0	**EIRFS**	R/W	0	1	Enable	0	Mask	Interrupt mask register (RFC SEN completion)
FFE2H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT0**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT0 underflow)
	D0	**EICTC0** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT0 compare match)
FFE3H (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT1**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT1 underflow)
	D0	**EICTC1**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT1 compare match)
FFE4H (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT2**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT2 underflow)
	D0	**EICTC2**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT2 compare match)
FFE5H (*4)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT3**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT3 underflow)
	D0	**EICTC3**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT3 compare match)
FFEAH (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	0 (*3)	R	– (*2)	–				Unused
	D0	**EISIF**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Serial I/F)
FFEBH	D3	**EIK03**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY03<P03>)
	D2	**EIK02**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY02<P02>)
	D1	**EIK01**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY01<P01>)
	D0	**EIK00**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY00<P00>)
FFECH (*6)	D3	**EIK13**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY13<P13>)
	D2	**EIK12**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY12<P12>)
	D1	**EIK11**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY11<P11>)
	D0	**EIK10**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY10<P10>)
FFEDH	D3	**EIRUN** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (SW direct RUN)
	D2	**EILAP** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (SW direct LAP)
	D1	**EISW1**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Stopwatch 1 Hz)
	D0	**EISW10**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Stopwatch 10 Hz)
FFEEH	D3	**EIT3** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 16 Hz)
	D2	**EIT2**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 32 Hz)
	D1	**EIT1** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 64 Hz)
	D0	**EIT0** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 128 Hz)
FFEFH	D3	**EIT7**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 1 Hz)
	D2	**EIT6**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 2 Hz)
	D1	**EIT5** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 4 Hz)
	D0	**EIT4**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 8 Hz)

Address		Register name	R/W	Default	Setting/data				Function
FFF1H	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	**IRFE**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (RFC error)
	D1	**IRFR**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (RFC REF completion)
	D0	**IRFS**	R/W	0					Interrupt factor flag (RFC SEN completion)
FFF2H	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	0 (∗3)	R	– (∗2)	–				Unused
	D1	**IPT0**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT0 underflow)
	D0	**ICTC0** (∗6)	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT0 compare match)
FFF3H (∗6)	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	0 (∗3)	R	– (∗2)	–				Unused
	D1	**IPT1**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT1 underflow)
	D0	**ICTC1**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT1 compare match)
FFF4H (∗6)	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	0 (∗3)	R	– (∗2)	–				Unused
	D1	**IPT2**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT2 underflow)
	D0	**ICTC2**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT2 compare match)
FFF5H (∗4)	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	0 (∗3)	R	– (∗2)	–				Unused
	D1	**IPT3**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT3 underflow)
	D0	**ICTC3**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT3 compare match)
FFFAH (∗6)	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	0 (∗3)	R	– (∗2)	–				Unused
	D1	0 (∗3)	R	– (∗2)	–				Unused
	D0	**ISIF**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (Serial I/F)
						Reset (W)		Invalid (W)	
FFFBH	D3	**IK03**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (KEY03<P03>)
	D2	**IK02**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (KEY02<P02>)
	D1	**IK01**	R/W	0					Interrupt factor flag (KEY01<P01>)
	D0	**IK00**	R/W	0					Interrupt factor flag (KEY00<P00>)
FFFCH (∗6)	D3	**IK13**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (KEY13<P13>)
	D2	**IK12**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (KEY12<P12>)
	D1	**IK11**	R/W	0					Interrupt factor flag (KEY11<P11>)
	D0	**IK10**	R/W	0					Interrupt factor flag (KEY10<P10>)
FFFDH	D3	**IRUN** (∗6)	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (SW direct RUN)
	D2	**ILAP** (∗6)	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (SW direct LAP)
	D1	**ISW1**	R/W	0					Interrupt factor flag (Stopwatch 1 Hz)
	D0	**ISW10**	R/W	0					Interrupt factor flag (Stopwatch 10 Hz)
FFFEH	D3	**IT3** (∗6)	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (Clock timer 16 Hz)
	D2	**IT2**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (Clock timer 32 Hz)
	D1	**IT1** (∗6)	R/W	0					Interrupt factor flag (Clock timer 64 Hz)
	D0	**IT0** (∗6)	R/W	0					Interrupt factor flag (Clock timer 128 Hz)
FFFFH	D3	**IT7**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (Clock timer 1 Hz)
	D2	**IT6**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (Clock timer 2 Hz)
	D1	**IT5** (∗6)	R/W	0					Interrupt factor flag (Clock timer 4 Hz)
	D0	**IT4**	R/W	0					Interrupt factor flag (Clock timer 8 Hz)

∗1 Initial value at initial reset ∗2 Not set in the circuit ∗3 Constantly "0" when being read
∗4 Unused in the S1C63003/004/008 ∗5 Unused in the S1C63003/004 ∗6 Unused in the S1C63003

EI∗∗∗: Interrupt mask registers (FFE1H–FFEFH)

Selects whether interrupts generated by interrupt factors are masked or not.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

When the interrupt mask register is set to "1," an interrupt to the CPU will be generated if the corresponding interrupt flag is set to 1. Setting the interrupt mask register to "0" masks the interrupt factor and no interrupt will be generated. At initial reset, the interrupt mask registers are set to "0."

I***: Interrupt factor flags (FFF1H–FFFFH)

These flags indicate that the interrupt factor has occurred or not.

When "1" is read: Interrupt factor has occurred
When "0" is read: Interrupt factor has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags are set to "1" when each interrupt factor in the peripheral circuit has occurred. From the status of the interrupt factor flag, the software can determine if the interrupt factor has occurred. If the corresponding interrupt mask register has been set to "1" (interrupt enabled), an interrupt is generated to the CPU when the interrupt factor flag is set to 1.
The interrupt factor flag is always set to "1" when the interrupt factor occurs regardless of the interrupt mask register setting. The interrupt flag is reset to "0" by writing "1."
After an interrupt has occurred, the same interrupt will occur again if interrupts are enabled (I flag = "1") or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt handler routine before enabling the interrupt.
After an initial reset, the interrupt factor flags are set to "0."

Table 6.5.2 Interrupt factors

Interrupt factor	Interrupt factor flag		Interrupt mask register		S1C63xxx			
					016	008	004	003
R/F converter (error)	IRFE	(FFF1H•D2)	EIRFE	(FFE1H•D2)	○	○	○	○
R/F converter (end of reference conversion)	IRFR	(FFF1H•D1)	EIRFR	(FFE1H•D1)	○	○	○	○
R/F converter (end of sensor conversion)	IRFS	(FFF1H•D0)	EIRFS	(FFE1H•D0)	○	○	○	○
Programmable timer 0 (underflow)	IPT0	(FFF2H•D1)	EIPT0	(FFE2H•D1)	○	○	○	○
Programmable timer 0 (compare match)	ICTC0	(FFF2H•D0)	EICTC0	(FFE2H•D0)	○	○	○	–
Programmable timer 1 (underflow)	IPT1	(FFF3H•D1)	EIPT1	(FFE3H•D1)	○	○	○	–
Programmable timer 1 (compare match)	ICTC1	(FFF3H•D0)	EICTC1	(FFE3H•D0)	○	○	○	–
Programmable timer 2 (underflow)	IPT2	(FFF4H•D1)	EIPT2	(FFE4H•D1)	○	○	○	–
Programmable timer 2 (compare match)	ICTC2	(FFF4H•D0)	EICTC2	(FFE4H•D0)	○	○	○	–
Programmable timer 3 (underflow)	IPT3	(FFF5H•D1)	EIPT3	(FFE5H•D1)	○	–	–	–
Programmable timer 3 (compare match)	ICTC3	(FFF5H•D0)	EICTC3	(FFE5H•D0)	○	–	–	–
Serial interface (8-bit data input/output completion)	ISIF	(FFFAH•D0)	EISEIF	(FFEAH•D0)	○	○	○	–
Key input interrupt <P03>	IK03	(FFFBH•D3)	EIK03	(FFEBH•D3)	○	○	○	○
Key input interrupt <P02>	IK02	(FFFBH•D2)	EIK02	(FFEBH•D2)	○	○	○	○
Key input interrupt <P01>	IK01	(FFFBH•D1)	EIK01	(FFEBH•D1)	○	○	○	○
Key input interrupt <P00>	IK00	(FFFBH•D0)	EIK00	(FFEBH•D0)	○	○	○	○
Key input interrupt <P13>	IK13	(FFFCH•D3)	EIK13	(FFECH•D3)	○	○	○	–
Key input interrupt <P12>	IK12	(FFFCH•D2)	EIK12	(FFECH•D2)	○	○	○	–
Key input interrupt <P11>	IK11	(FFFCH•D1)	EIK11	(FFECH•D1)	○	○	○	–
Key input interrupt <P10>	IK10	(FFFCH•D0)	EIK10	(FFECH•D0)	○	○	○	–
Stopwatch timer (Direct RUN)	IRUN	(FFFDH•D3)	EIRUN	(FFEDH•D3)	○	○	○	–
Stopwatch timer (Direct LAP)	ILAP	(FFFDH•D2)	EILAP	(FFEDH•D2)	○	○	○	–
Stopwatch timer (1 Hz)	ISW1	(FFFDH•D1)	EISW1	(FFEDH•D1)	○	○	○	○
Stopwatch timer (10 Hz)	ISW10	(FFFDH•D0)	EISW10	(FFEDH•D0)	○	○	○	○
Clock timer 16 Hz (falling edge)	IT3	(FFFEH•D3)	EIT3	(FFEEH•D3)	○	○	○	–
Clock timer 32 Hz (falling edge)	IT2	(FFFEH•D2)	EIT2	(FFEEH•D2)	○	○	○	○
Clock timer 64 Hz (falling edge)	IT1	(FFFEH•D1)	EIT1	(FFEEH•D1)	○	○	○	–
Clock timer 128 Hz (falling edge)	IT0	(FFFEH•D0)	EIT0	(FFEEH•D0)	○	○	○	–
Clock timer 1 Hz (falling edge)	IT7	(FFFFH•D3)	EIT7	(FFEFH•D3)	○	○	○	○
Clock timer 2 Hz (falling edge)	IT6	(FFFFH•D2)	EIT6	(FFEFH•D2)	○	○	○	○
Clock timer 4 Hz (falling edge)	IT5	(FFFFH•D1)	EIT5	(FFEFH•D1)	○	○	○	–
Clock timer 8 Hz (falling edge)	IT4	(FFFFH•D0)	EIT4	(FFEFH•D0)	○	○	○	○

Refer to the descriptions of the peripheral circuits for interrupt factor occurrence conditions.

6.6 Precautions

- The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0."
- After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt handler routine before shifting to the interrupt enabled state.
- After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.
- The interrupt handler routine must be located within the range from "Interrupt vector address (100H–10FH)" -7FH to +80H. If it is difficult, make a relay point within that range as the destination of the vector jump and branch the program to the interrupt handler from there.
- Both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

7 Oscillation Circuit and Clock Control

7.1 Oscillation Circuit

7.1.1 Configuration of Oscillation Circuit

The S1C63003/004/008/016 is configured as a twin clock system with two internal oscillation circuits (OSC1 and OSC3). The OSC1 oscillation circuit generates the main-clock (Typ. 32.768 kHz) for low-power operation and the OSC3 oscillation circuit generates the sub-clock (Typ. 4.0 MHz/3 V normal type or 1.0 MHz/1.5 V low-voltage type) to run the CPU and some peripheral circuits in high speed. Figure 7.1.1.1 shows the configuration of the oscillation circuit.

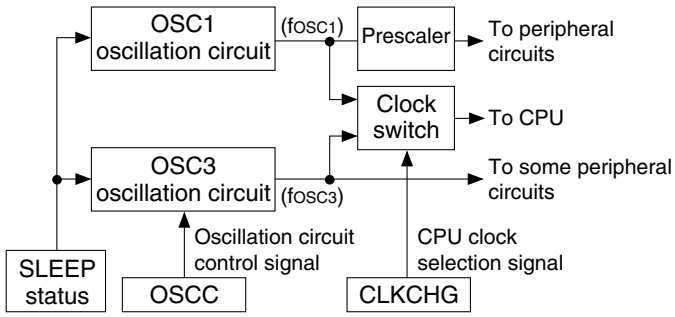


Figure 7.1.1.1 Oscillation circuit block diagram

At initial reset, OSC1 oscillation circuit is selected as the CPU operating clock source. The S1C63003/004/008/016 allows the software to turn the OSC3 oscillation circuit on and off, and to switch the system clock between OSC3 and OSC1. The OSC3 oscillation circuit is used when the CPU and some peripheral circuits need high speed operation. Otherwise, use the OSC1 oscillation circuit to generate the operating clock and stop the OSC3 oscillation circuit to reduce current consumption.

7.1.2 Mask Option

In the S1C63004/008/016, the OSC3 oscillator type can be selected from ceramic, CR (external R) and CR (built-in R). The S1C63003 OSC3 oscillator type is fixed at CR oscillation (built-in R).

7.1.3 OSC1 Oscillation Circuit

The OSC1 oscillation circuit (crystal oscillation circuit) generates the 32.768 kHz (Typ.) system clock which is used during low speed (low power) operation of the CPU and peripheral circuits. Furthermore, even when OSC3 is used as the system clock, OSC1 continues to generate the source clock for the clock timer and stopwatch timer. This oscillation circuit stops when the SLP instruction is executed.
Figure 7.1.3.1 shows the configuration of the OSC1 oscillation circuit.

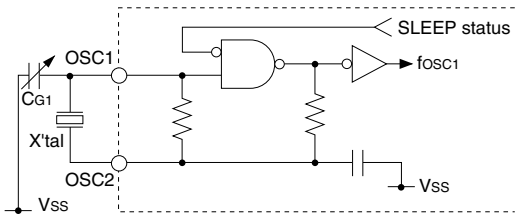
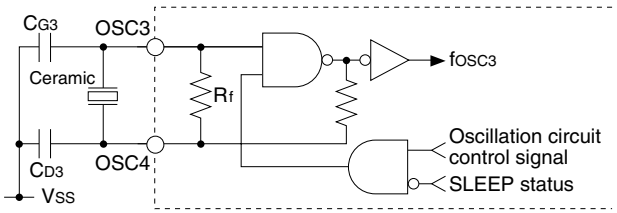


Figure 7.1.3.1 OSC1 oscillation circuit

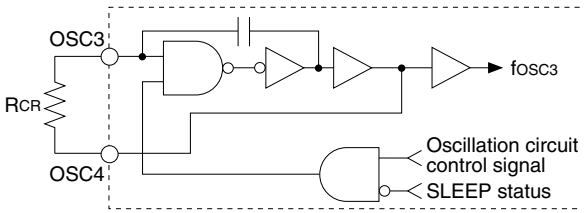
A crystal oscillation circuit can be configured simply by connecting a crystal resonator X'tal (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals along with a trimmer capacitor C_{G1} (0–25 pF) between the OSC1 terminal and V_{SS}.

7.1.4 OSC3 Oscillation Circuit

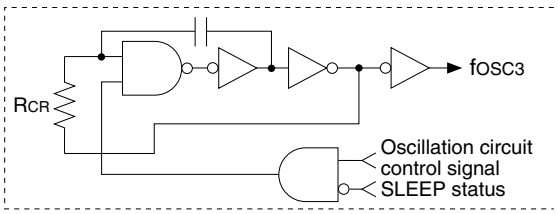
The OSC3 oscillation circuit generates the system clock to run the CPU and some peripheral circuits at high speed. This oscillation circuit stops when the SLP instruction is executed or the OSCC register is set to "0."
In the S1C63004/008/016, the oscillator type can be selected from ceramic, CR (external R), and CR (built-in R) by mask option. The S1C63003 OSC3 oscillator type is fixed at CR oscillation (built-in R).
Figure 7.1.4.1 shows the configuration of the OSC3 oscillation circuit.



(1) Ceramic oscillation circuit – S1C63004/008/016



(2) CR oscillation circuit (external R) – S1C63004/008/016



(3) CR oscillation circuit (built-in R) – S1C63003/004/008/016

Figure 7.1.4.1 OSC3 oscillation circuit

When ceramic oscillation circuit is selected, connect a ceramic resonator (Ceramic) between the OSC3 and OSC4 terminals and connecting two capacitors (C_{G3}, C_{D3}) between the OSC3 terminal and V_{SS}, and between the OSC4 terminal and V_{SS}, respectively.
When CR (external R) is selected, connect a resistor (R_{CR}) between the OSC3 and OSC4 terminals.
The CR (built-in R) oscillator does not need any external elements. Leave the OSC3 and OSC4 terminals open.

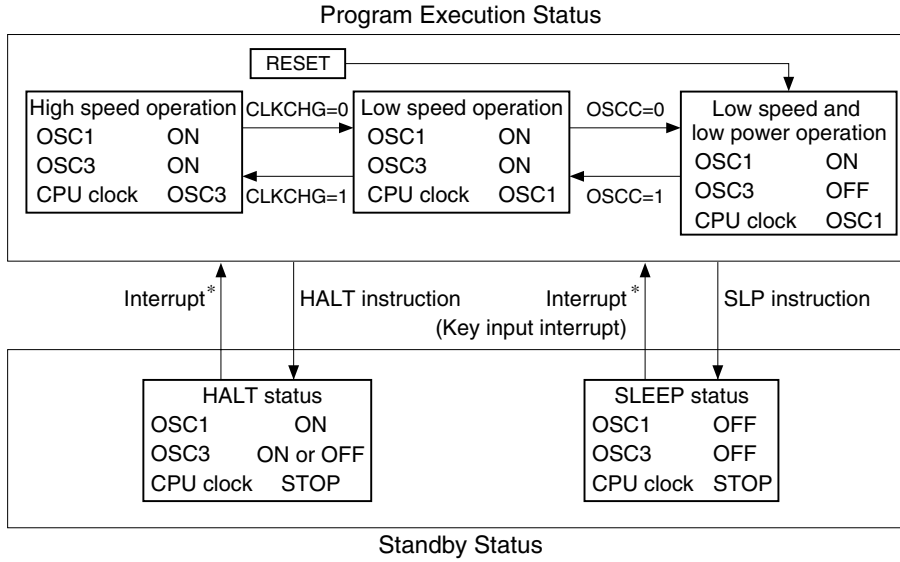
Table 7.1.4.1 OSC3 oscillation frequency

Oscillator type	Oscillation frequency	
	S1C63004/008/016	S1C63003
Ceramic	Typ. 4.0 MHz (3 V normal type) or Typ. 1.0 MHz (1.5 V low-voltage type)	–
CR (external R)	Typ. 1.8 MHz (3 V normal type) or Typ. 500 kHz (1.5 V low-voltage type)	–
CR (built-in R)	Typ. 500 kHz (3 V normal type) or Typ. 500 kHz (1.5 V low-voltage type)	Typ. 550 kHz (3 V normal type) or Typ. 550 kHz (1.5 V low-voltage type)

7.2 Switching the CPU Clock

Either the OSC1 clock or the OSC3 clock can be selected as the CPU system clock using the CLKCHG register.
The OSC3 oscillation circuit can be turned off (OSCC = "0") to save power while the CPU is operating with the OSC1 clock (CLKCHG = "0").
If the system needs high speed operation, turn the OSC3 oscillation circuit on (OSCC = "1") and switch over the system clock to OSC3 (CLKCHG = "0" → "1").

In this case, since several tens of μsec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit on, you should switch over the clock after the stabilization time has elapsed.
The oscillation start time will vary somewhat depending on the resonator and on the externally attached parts. Refer to the oscillation start time example indicated in the "Electrical Characteristics" chapter.
When switching the clock from OSC3 to OSC1 (CLKCHG = "1" → "0"), be sure to switch OSC3 oscillation off with separate instructions. Using a single instruction to process simultaneously may cause a malfunction of the CPU.
Figure 7.2.1 indicates the status transition diagram for the clock switch over.



* The return destination from the standby status becomes the program execution status prior to shifting to the standby status.

Figure 7.2.1 Status transition diagram for clock switch over

7.3 HALT and SLEEP

The S1C63003/004/008/016 supports both HALT and SLEEP modes for power saving during standby.

HALT mode

The CPU enters HALT mode and stops operating when it executes the HALT instruction. However, timer counters and peripheral circuits continue operating since the oscillation circuit operates in HALT mode. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

SLEEP mode

The CPU enters SLEEP mode when it executes the SLP instruction. In this mode, the CPU and oscillation circuits (both OSC1 and OSC3) stop operating. Current consumption can considerably be reduced, as SLEEP mode stop all the peripheral circuits that operate with the internal clocks. To prevent improper operation after the CPU wakes up, be sure to run the CPU with the OSC1 clock before setting the CPU into SLEEP mode.
The system can only be reactivated from SLEEP mode by a key input interrupt request from a P0x or P1x port. To ensure that the system enters and cancels SLEEP mode properly, follow the procedure shown below to configure/confirm the CPU clock, interrupt flag, the P0x (P1x) I/O port used to cancel SLEEP mode, and the port input level.

1. Set the CPU system clock switching register CLKCHG to "0." (The OSC1 clock is selected.)
2. Set the interrupt select register SIPxx to "1." (The P0x (P1x) I/O port interrupt is selected.)
3. Set the interrupt mask register EIKxx to "1." (The P0x (P1x) I/O port interrupt is enabled.)
4. Set the key input interrupt noise reject frequency select register NRSPxx to "0H." (The noise rejector is bypassed.)
5. Write "1" to the interrupt factor flag IKxx. (the P0x (P1x) interrupt factor flag is reset.)
6. Set the interrupt flag (I flag) to "1." (Interrupts are enabled.)

7a. Make sure the P0x (P1x) port input level is high when P0x (P1x) port interrupt polarity select register = "1" (generates an interrupt request at the falling edge).
7b. Make sure the P0x (P1x) port input level is low when P0x (P1x) port interrupt polarity select register = "0" (generates an interrupt request at the rising edge).
8. Execute the SLP instruction.

When SLEEP status is canceled by an I/O port interrupt, the CPU restarts operating (input port interrupt processing) after waiting for oscillation to stabilize. Refer to the "S1C63000 Core CPU Manual" for transition to HALT/SLEEP mode and timing of its cancellation.

7.4 Control of Peripheral Circuit Clocks

The S1C63003/004/008/016 incorporates a clock manager that generates operating clocks by dividing the OSC1/OSC3 clock output from the oscillation circuit and supplies the clocks to the peripheral circuits. Some peripheral circuits can select the operating clock to be used from several dividing clocks in the clock manager. If the current processing does not use peripheral circuits, the clock supply to those circuits can be stopped in the clock manager. Disabling unnecessary clocks to be supplied or operating the peripheral circuits with a clock as low frequency as possible can reduce current consumption. For controlling the clock manager, see the descriptions in each peripheral circuit.

7.5 Clock Output (FOUT)

In order for the S1C63003/004/008/016 to provide a clock signal to an external device, the FOUT signal (oscillation clock f_{OSC1}, f_{OSC3}, or a dividing clock) can be output from the FOUT (P13) terminal. The FOUT output is controlled using the FOUT[3:0] register. When the output clock frequency is selected using FOUT[3:0], the FOUT signal is output from the FOUT terminal. The P13 I/O port functions are disabled while the FOUT signal is being output. Setting FOUT[3:0] to 0H disables FOUT output and the P13 port is configured as a general-purpose input/output port. The FOUT signal frequency can be selected from among 15 settings as shown in Table 7.5.1.

Table 7.5.1 FOUT frequency selection

FOUT[3:0]	FOUT frequency
FH	f_{OSC3}
EH	f_{OSC3} / 2
DH	f_{OSC3} / 4
CH	f_{OSC3} / 8
BH	f_{OSC3} / 16
AH	f_{OSC3} / 32
9H	f_{OSC3} / 64
8H	f_{OSC3} / 256
7H	f_{OSC1} (32 kHz)
6H	f_{OSC1} / 2 (16 kHz)
5H	f_{OSC1} / 4 (8 kHz)
4H	f_{OSC1} / 16 (2 kHz)
3H	f_{OSC1} / 32 (1 kHz)
2H	f_{OSC1} / 64 (512 Hz)
1H	f_{OSC1} / 256 (128 Hz)
0H	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the clock frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

When the FOUT frequency is set to "f_{OSC3}/n," the OSC3 oscillation circuit must be turned on before outputting the FOUT signal. A time interval of several tens of µsec to several tens of msec, from turning the OSC3 oscillation circuit on until the oscillation stabilizes, is necessary. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning the OSC3 oscillation on, before starting FOUT output. Since the FOUT signal is generated asynchronously from the FOUT[3:0] register, a hazard of a 1/2 cycle or less is generated when the signal is turned on or off by setting the registers. Figure 7.5.1 shows the output waveform of the FOUT signal.

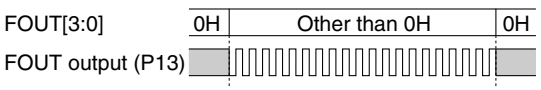


Figure 7.5.1 Output waveform of FOUT signal

7.6 I/O Memory for Oscillation Circuit/Clock Output Control

Table 7.6.1 shows the I/O address and the control bits for the oscillation circuit and FOUT output.

Table 7.6.1 Control bits of oscillation circuit/FOUT

Address		Register name	R/W	Default	Setting/data								Function
FF00H	D3	**CLKCHG**	R/W	0	1	OSC3			0	OSC1			CPU clock switch
	D2	**OSCC**	R/W	0	1	On			0	Off			OSC3 oscillation On/Off
	D1	0 (∗3)	R	– (∗2)	–								Unused
	D0	0 (∗3)	R	– (∗2)	–								Unused
FF10H	D3	**FOUT3**	R/W	0	F	f_3	B	$f_3/16$	7	f_1	3	$f_1/32$	FOUT frequency selection
	D2	**FOUT2**	R/W	0	E	$f_3/2$	A	$f_3/32$	6	$f_1/2$	2	$f_1/64$	($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D1	**FOUT1**	R/W	0	D	$f_3/4$	9	$f_3/64$	5	$f_1/4$	1	$f_1/256$	
	D0	**FOUT0**	R/W	0	C	$f_3/8$	8	$f_3/256$	4	$f_1/16$	0	Off	

∗1 Initial value at initial reset ∗2 Not set in the circuit ∗3 Constantly "0" when being read
∗4 Unused in the S1C63003/004/008 ∗5 Unused in the S1C63003/004 ∗6 Unused in the S1C63003

OSCC: OSC3 oscillation control register (FF00H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation On
When "0" is written: OSC3 oscillation Off
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1." At other times, set it to "0" to reduce current consumption. At initial reset, this register is set to "0."

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0." At initial reset, this register is set to "0."

FOUT[3:0]: FOUT frequency select register (FF10H)

Selects the frequency of the FOUT signal and controls the FOUT output.

Table 7.6.2 FOUT clock frequency

FOUT[3:0]	FOUT frequency
FH	f_{OSC3}
EH	f_{OSC3} / 2
DH	f_{OSC3} / 4
CH	f_{OSC3} / 8
BH	f_{OSC3} / 16
AH	f_{OSC3} / 32
9H	f_{OSC3} / 64
8H	f_{OSC3} / 256
7H	f_{OSC1} (32 kHz)
6H	f_{OSC1} / 2 (16 kHz)
5H	f_{OSC1} / 4 (8 kHz)
4H	f_{OSC1} / 16 (2 kHz)
3H	f_{OSC1} / 32 (1 kHz)
2H	f_{OSC1} / 64 (512 Hz)
1H	f_{OSC1} / 256 (128 Hz)
0H	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the clock frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

Selecting an FOUT frequency (writing 1H–FH to this register) outputs the FOUT signal from the FOUT (P13) terminal. Set FOUT[3:0] to "0" to use P13 as a general-purpose input/output port. At initial reset, this register is set to "0."

7.7 Precautions

- When high speed CPU operations are not necessary, you should operate the peripheral circuits with the setting shown below.
  - CPU operating clock: OSC1
  - OSC3 oscillation circuit: Off (When the OSC3 clock is not necessary for peripheral circuits.)
  - Clock manager: Disable the clock supply to unnecessary peripheral circuits.
- Since several tens of μsec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit on. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes on. The oscillation start time will vary somewhat depending on the resonator and externally attached parts. Refer to the oscillation start time example indicated in the "Electrical Characteristics" chapter.
- When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation off with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.
- Both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

8 Watchdog Timer

8.1 Configuration of Watchdog Timer

The S1C63003/004/008/016 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 8.1.1 is the block diagram of the watchdog timer.

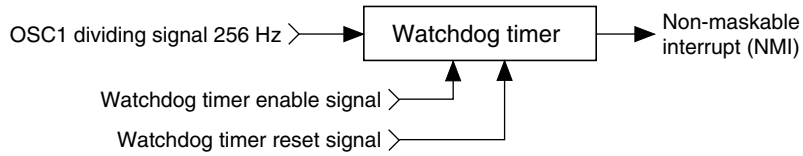


Figure 8.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

8.2 Interrupt Function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

8.3 I/O Memory of Watchdog Timer

Table 8.3.1 shows the I/O address and control bits for the watchdog timer.

Table 8.3.1 Control bits of watchdog timer

Address		Register name	R/W	Default	Setting/data				Function
FF01H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**WDEN**	R/W	1	1	Enable	0	Disable	Watchdog timer enable
	D0	**WDRST** (*3)	W	(Reset)	1	Reset	0	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

WDRST: Watchdog timer reset (FF01H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results. This bit is dedicated for writing, and is always "0" for reading.

WDEN: Watchdog timer enable register (FF01H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI). At initial reset, this register is set to "1."

8.4 Precautions

- When the watchdog timer is being used, the software must reset it within 3-second cycles.
- Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

9 Clock Timer

9.1 Configuration of Clock Timer

The S1C63003/004/008/016 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer consists of an 8-bit binary counter that counts an fosc1 dividing clock. Timer data (128–16 Hz and 8–1 Hz) can be read out by software. Figure 9.1.1 is the block diagram for the clock timer.

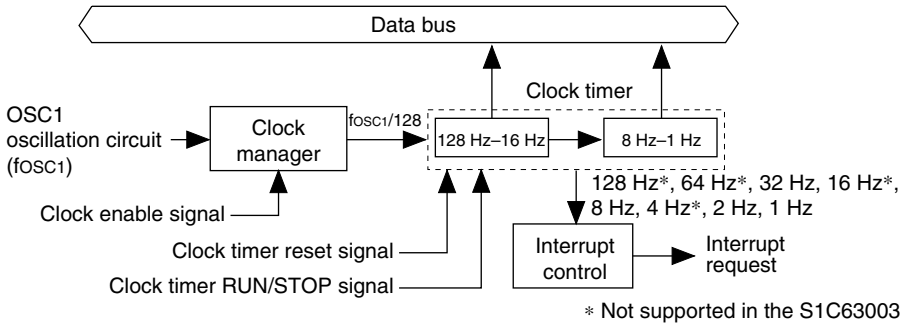


Figure 9.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

9.2 Controlling Operating Clock

The clock manager generates the clock timer operating clock by dividing the OSC1 clock by 128. Before the clock timer can be run, write "1" to the RTCKE register to supply the operating clock to the clock timer.

Table 9.2.1 Controlling clock timer operating clock

RTCKE	Clock timer operating clock
1	fosc1 / 128 (256 Hz)
0	Off

If it is not necessary to run the clock timer, stop the clock supply by setting RTCKE to "0" to reduce current consumption.

9.3 Data Read and Hold Function

The 8 bits timer data are allocated to the address FF41H and FF42H.

<FF41H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF42H>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since two addresses are allocated for the clock timer data, a carry is generated from the low-order data (TM[3:0]: 128–16 Hz) to the high-order data (TM[7:4]: 8–1 Hz) during counting. If this carry is generated between readings of the low-order data and the high-order data, the combined data does not represent the correct value (if a carry occurs after the low-order data is read as FFH, the incremented (+1) value is read as the high-order data). To avoid this problem, the clock timer is designed to latch the high-order data at the time the low-order data is read. The latched high-order data will be maintained until the next reading of the low-order data.

Note: The latched value, not the current value, is always read as the high-order data. Therefore, be sure to read the low-order data first.

9.4 Interrupt Function

The clock timer can generate an interrupt at the falling edge of 128 Hz*, 64 Hz*, 32 Hz, 16 Hz*, 8 Hz, 4 Hz*, 2 Hz and 1 Hz signals. Software can enable or mask any of these frequencies to generate interrupts.
Figure 9.4.1 is the timing chart of the clock timer.

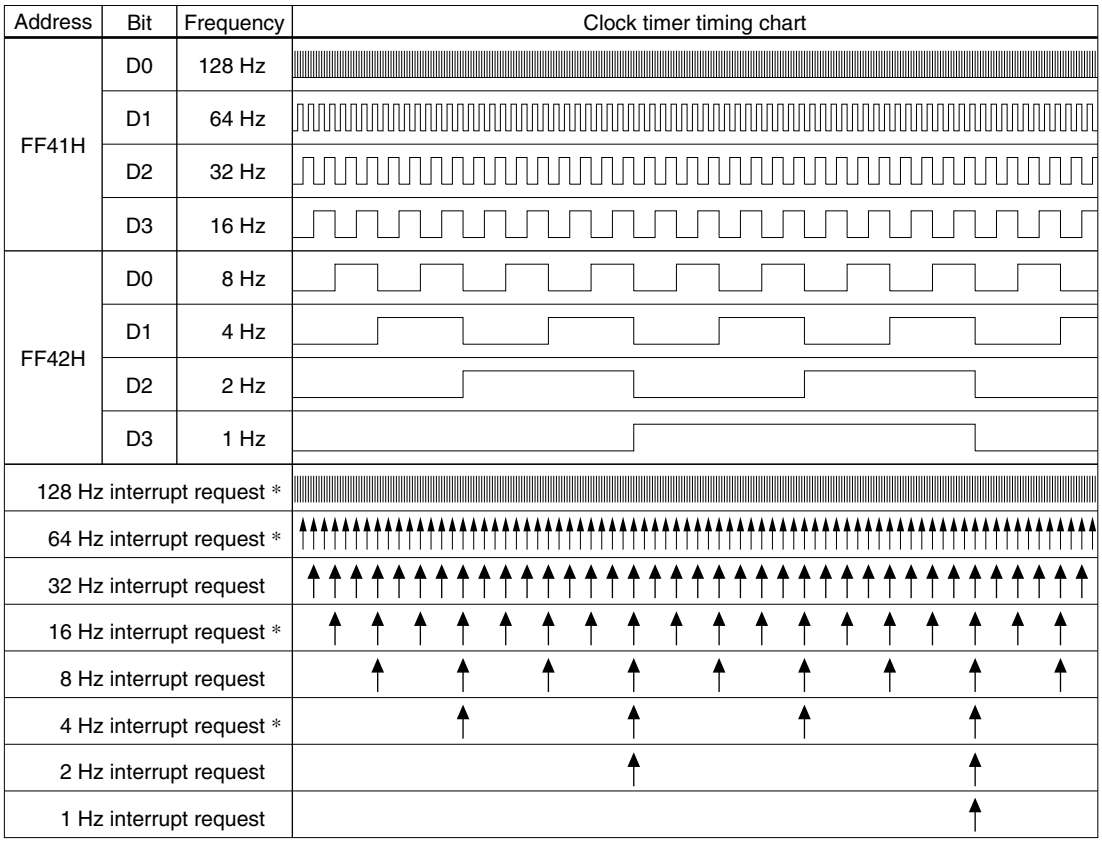


Figure 9.4.1 Timing chart of clock timer

As shown in Figure 9.4.1, an interrupt is generated at the falling edge of each frequency signal (128 Hz*, 64 Hz*, 32 Hz, 16 Hz*, 8 Hz, 4 Hz*, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0*, IT1*, IT2, IT3*, IT4, IT5*, IT6, IT7) is set to "1." The interrupt mask registers (EIT0*, EIT1*, EIT2, EIT3*, EIT4, EIT5*, EIT6, EIT7) are used to enable or mask each interrupt factor. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

* Not supported in the S1C63003

9.5 I/O Memory of Clock Timer

Table 9.5.1 shows the I/O addresses and the control bits for the clock timer.

Table 9.5.1 Control bits of clock timer

Address		Register name	R/W	Default	Setting/data				Function
FF16H	D3	MDCKE (*5)	R/W	0	1	Enable	0	Disable	Integer multiplier clock enable
	D2	SGCKE	R/W	0	1	Enable	0	Disable	Sound generator clock enable
	D1	SWCKE	R/W	0	1	Enable	0	Disable	Stopwatch timer clock enable
	D0	**RTCKE**	R/W	0	1	Enable	0	Disable	Clock timer clock enable
FF40H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**TMRST** (*3)	W	(Reset)	1	Reset	0	Invalid	Clock timer reset (writing)
	D0	**TMRUN**	R/W	0	1	Run	0	Stop	Clock timer Run/Stop

Address		Register name	R/W	Default	Setting/data	Function
FF41H	D3	**TM3**	R	0	0H–FH	Clock timer data (16 Hz)
	D2	**TM2**	R	0		Clock timer data (32 Hz)
	D1	**TM1**	R	0		Clock timer data (64 Hz)
	D0	**TM0**	R	0		Clock timer data (128 Hz)
FF42H	D3	**TM7**	R	0	0H–FH	Clock timer data (1 Hz)
	D2	**TM6**	R	0		Clock timer data (2 Hz)
	D1	**TM5**	R	0		Clock timer data (4 Hz)
	D0	**TM4**	R	0		Clock timer data (8 Hz)

∗1 Initial value at initial reset ∗2 Not set in the circuit ∗3 Constantly "0" when being read
∗4 Unused in the S1C63003/004/008 ∗5 Unused in the S1C63003/004 ∗6 Unused in the S1C63003

RTCKE: Clock timer clock enable register (FF16H•D0)

Controls the operating clock supply to the clock timer.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to RTCKE, the clock timer operating clock is supplied from the clock manager. If it is not necessary to run the clock timer, stop the clock supply by setting RTCKE to "0" to reduce current consumption. At initial reset, this register is set to "0."

TMRUN: Clock timer Run/Stop control register (FF40H•D0)

Controls run/stop of the clock timer.

When "1" is written: Run
When "0" is written: Stop
Reading: Valid

The clock timer starts running when "1" is written to the TMRUN register, and stops when "0" is written. In stop status, the timer data is maintained until the next run status or the timer is reset. Also, when stop status changes to run status, the data that is maintained can be used for resuming the count. At initial reset, this register is set to "0."

TMRST: Clock timer reset (FF40H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer must be reset when it is stopped (TMRUN = "0"). No operation results when "0" is written to TMRST. This bit is write-only, and so is always "0" at reading.

TM[7:0]: Timer data (FF42H, FF41H)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid. By reading the low-order data (FF41H), the high-order data (FF42H) is latched. The latched value, not the current value, is always read as the high-order data. Therefore, be sure to read the low-order data first. At initial reset, the timer data is initialized to "00H."

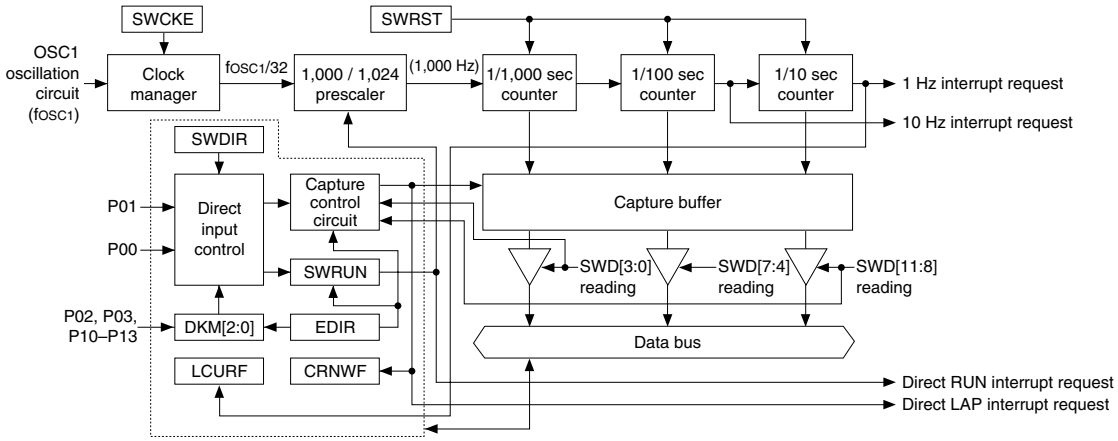
9.6 Precautions

- Be sure to read timer data in the order of low-order data (TM[3:0]) then high-order data (TM[7:4]).
- The clock timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the clock timer count data should be read by one of the procedures shown below.
  - Read the count data twice and verify if there is any difference between them.
  - Temporarily stop the clock timer when the counter data is read to obtain proper data.
- When resetting the clock timer (TMRST = "1"), do not start the clock timer (TMRUN = "1") simultaneously. If both control bits are set to "1," the clock timer may not reset properly.

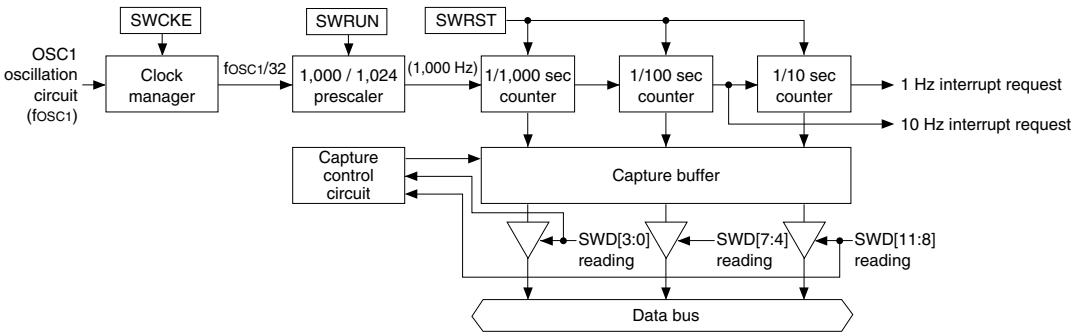
10 Stopwatch Timer

10.1 Configuration of Stopwatch Timer

The S1C63003/004/008/016 has a 1/1,000 sec stopwatch timer. The stopwatch timer is configured of a 3-stage, 4-bit BCD counter serving as the input clock of a 1,000 Hz signal output from the prescaler. Data can be read out four bits (1/1,000 sec, 1/100 sec and 1/10 sec) at a time by software. In addition the S1C63004/008/016 has a direct input function that controls the stopwatch timer RUN/STOP and LAP using the input ports P00 and P01. Figure 10.1.1 is the block diagram of the stopwatch timer.



(a) S1C63004/008/016



(b) S1C63003

Figure 10.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

10.2 Controlling Operating Clock

The clock manager generates the stopwatch timer operating clock by dividing the OSC1 clock by 32. Before the stopwatch timer can be run, write "1" to the SWCKE register to supply the operating clock to the stopwatch timer.

Table 10.2.1 Controlling stopwatch timer operating clock

SWCKE	Stopwatch timer clock
1	fOSC1 / 32 (1 kHz)
0	Off

If it is not necessary to run the stopwatch timer, stop the clock supply by setting SWCKE to "0" to reduce current consumption.

10.3 Counter and Prescaler

The stopwatch timer is configured of four-bit BCD counters SWD[3:0], SWD[7:4] and SWD[11:8].
The counter SWD[3:0], at the stage preceding the stopwatch timer, has a 1,000 Hz signal generated by the prescaler for the input clock. It counts up every 1/1,000 sec, and generates 100 Hz signal. The counter SWD[7:4] has a 100 Hz signal generated by the counter SWD[3:0] for the input clock. It count-up every 1/100 sec, and generated 10 Hz signal. The counter SWD[11:8] has an approximated 10 Hz signal generated by the counter SWD[7:4] for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.
The prescaler inputs a 1,024 Hz clock dividing fosc1 (output from the OSC1 oscillation circuit), and outputs 1,000 Hz counting clock for SWD[3:0]. To generate a 1,000 Hz clock from 1,024 Hz, 24 pulses from 1,024 pulses that are input to the prescaler every second are taken out.
When the counter becomes the value indicated below, one pulse (1,024 Hz) that is input immediately after to the prescaler will be pulled out.

<Counter value (msec) in which the pulse correction is performed>
39, 79, 139, 179, 219, 259, 299, 319, 359, 399, 439, 479, 539, 579, 619, 659, 699, 719, 759, 799, 839, 879, 939, 979

Figure 10.3.1 shows the operation of the prescaler.

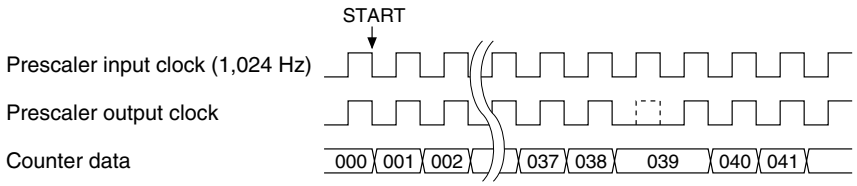


Figure 10.3.1 Timing of the prescaler operation

For the above reason, the counting clock is 1,024 Hz (0.9765625 msec) except during pulse correction. Consequently, frequency of the prescaler output clock (1,000 Hz), 100 Hz generated by SWD[3:0] and 10 Hz generated by SWD[7:4] are approximate values.

10.4 Capture Buffer and Hold Function

The stopwatch timer data, 1/1,000 sec, 1/100 sec and 1/10 sec, can be read from SWD[3:0] (FF4BH), SWD[7:4] (FF4CH) and SWD[11:8] (FF4DH), respectively. The counter data are latched in the capture buffer when reading, and are held until reading of three words is completed. For this reason, correct data can be read even when a carry from lower digits occurs during reading the three words. Further, three counter data are latched in the capture buffer at the same time when SWD[3:0] (1/1,000 sec) is read. The data hold is released when SWD[11:8] (1/10 sec) reading is completed. Therefore, data should be read in order of SWD[3:0] → SWD[7:4] → SWD[11:8]. If SWD[7:4] or SWD[11:8] is first read when data have not been held, the hold function does not work and data in the counter is directly read out. When data that has not been held is read in the stopwatch timer RUN status, you cannot judge whether it is correct or not.

The S1C63004/008/016 stopwatch timer has a LAP function using an external key input (explained later). The capture buffer is also used to hold LAP data. In this case, data is held until SWD[11:8] is read. However, when a LAP input is performed before completing the reading, the content of the capture buffer is renewed at that point. Remaining data that have not been read become invalid by the renewal, and the hold status is not released if SWD[11:8] is read. When SWD[11:8] is read after the capture buffer is updated, the capture renewal flag CRNWF is set to "1" at that point. In this case, it is necessary to read from SWD[3:0] again. The capture renewal flag is renewed by reading SWD[11:8].

Figure 10.4.1 shows the timing for data holding and reading.

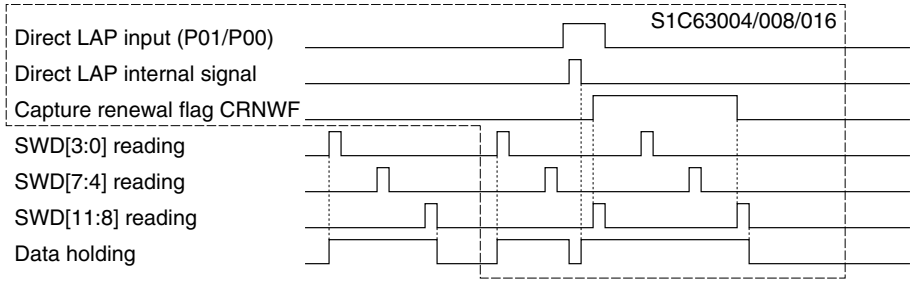


Figure 10.4.1 Timing for data holding and reading

10.5 Stopwatch Timer RUN/STOP and Reset

RUN/STOP control and reset of the stopwatch timer can be done by software.

Stopwatch timer RUN/STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. The RUN/STOP operation of the stopwatch timer by writing to the SWRUN register is performed in synchronization with the falling edge of the 1,024 Hz same as the prescaler input clock. The SWRUN register can be read, and in this case it indicates the operating status of the stopwatch timer.

Figure 10.5.1 shows the operating timing when controlling the SWRUN register.

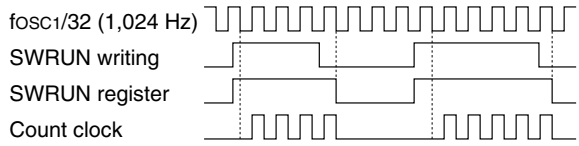


Figure 10.5.1 Operating timing when controlling SWRUN

When the direct input function (explained in next section) is set, RUN/STOP control is done by an external key input. In this case, SWRUN becomes read only register that indicates the operating status of the stopwatch timer (S1C63004/008/016).

Stopwatch timer reset

The stopwatch timer is reset when "1" is written to SWRST. With this, the counter value is cleared to "000." Since this resetting does not affect the capture buffer, data that has been held in the capture buffer is not cleared and is maintained as is. When the stopwatch timer is reset in the RUN status, counting restarts from count "000." Also, in the STOP status the reset data "000" is maintained until the next RUN.

10.6 Direct Input Function and Key Mask [S1C63004/008/016]

The S1C63004/008/016 stopwatch timer has a direct input function that can control the RUN/STOP and LAP operation of the stopwatch timer by external key input. This function is set by writing "1" to the EDIR register. When EDIR is set to "0," only the software control is possible as explained in the previous section.

Input port configuration

In the direct input function, the input ports P00 and P01 are used as the RUN/STOP and LAP input ports. The key assignment can be selected using the SWDIR register.

Table 10.6.1 RUN/STOP and LAP input ports

SWDIR	P00	P01
0	RUN/STOP	LAP
1	LAP	RUN/STOP

Direct RUN

When the direct input function is selected, RUN/STOP operation of the stopwatch timer can be controlled by using the key connected to the input port P00/P01 (selected by SWDIR). P00/P01 works as a normal input port, but the input signal is sent to the stopwatch control circuit. The key input signal from the P00/P01 port works as a toggle switch. When it is input in STOP status, the stopwatch timer runs, and in RUN status, the stopwatch timer stops. RUN/STOP status of the stopwatch timer can be checked by reading the SWRUN register. An interrupt is generated by direct RUN input.

The sampling for key input signal is performed at the falling edge of 1,024 Hz signal same as the SWRUN control. The chattering judgment is performed at the point where the key turns off, and a chattering less than 46.8–62.5 msec is removed. Therefore, more time is needed for an interval between RUN and STOP key inputs.

Figure 10.6.1 shows the operating timing for the direct RUN input.

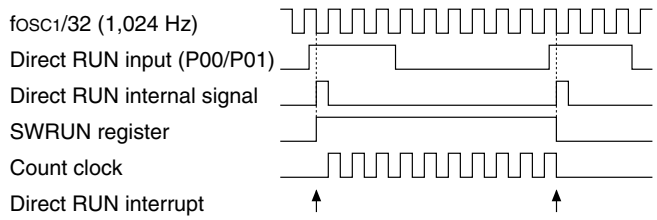


Figure 10.6.1 Operating timing for direct RUN input

Direct LAP

Control for the LAP can also be done by key input same as the direct RUN. When the direct input function is selected, the input port P01/P00 (selected by SWDIR) becomes the LAP key input port. Sampling for the input signal and the chattering judgment are the same as a direct RUN.

By entering the LAP key, the counter data at that point is latched into the capture buffer and is held. The counter continues counting operation. Furthermore, an interrupt occurs by direct LAP input.

As stated above, the capture buffer data is held until SWD[11:8] is read. If the LAP key is input when data has been already held, it renews the content of the capture buffer. When SWD[11:8] is read after renewing, the capture renewal flag is set to "1." In this case, the hold status is not released by reading SWD[11:8], and it continues. Normally the LAP data should be read after the interrupt is generated. After that, be sure to check the capture renewal flag. When the capture renewal flag is set, renewed data is held in the capture buffer. So it is necessary to read from SWD[3:0] again.

The stopwatch timer sets the 1 Hz interrupt factor flag ISW1 to "1" when requiring a carry-up to 1-sec digit by an SWD[11:8] overflow. If the capture buffer shifts into hold status (when SWD[3:0] is read or when LAP is input) while the 1 Hz interrupt factor flag ISW1 is set to "1," the lap data carry-up request flag LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required for the processing of LAP input. In normal software processing, LAP processing may take precedence over 1-sec or higher digits processing by a 1 Hz interrupt, therefore carry-up processing using this flag should be used for time display in the LAP processing to prevent the 1-sec digit data decreasing by 1 second. This flag is renewed when the capture buffer shifts into hold status.

Figure 10.6.2 shows the operating timing for the direct LAP input, and Figure 10.6.3 shows the timings for data holding and reading during a direct LAP input and reading.

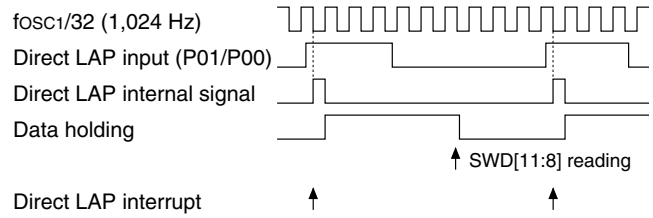


Figure 10.6.2 Operating timing for direct LAP input

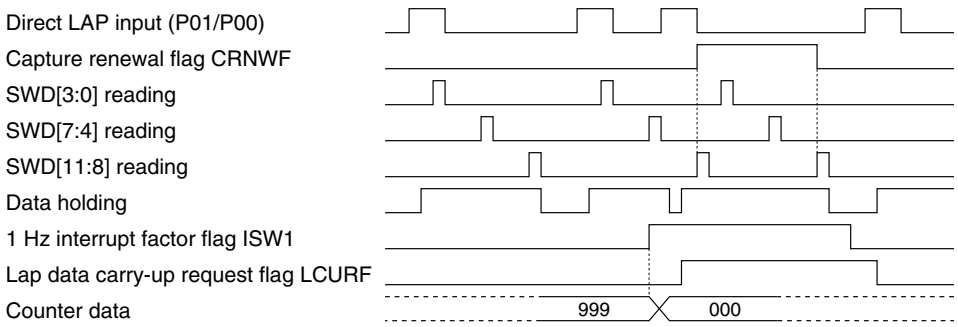


Figure 10.6.3 Timing for data holding and reading during direct LAP input

Key mask

In stopwatch applications, some functions may be controlled by a combination of keys including direct RUN or direct LAP. For instance, the RUN key can be used for other functions, such as reset and setting a watch, by pressing the RUN key with another key. In this case, the direct RUN function or direct LAP function must be invalid so that it does not function. For this purpose, the key mask function is set so that it judges concurrence of input keys and invalidates RUN and LAP functions. A combination of the key inputs for this judgment can be selected using the DKM[2:0] register.

Table 10.6.2 Key mask selection

DKM[2:0]	Mask key combination
0H	None (at initial reset)
1H	P02
2H	P02, P03
3H	P02, P03, P10
4H	P10
5H	P10, P11
6H	P10, P11, P12
7H	P10, P11, P12, P13

RUN or LAP inputs become invalid in the following status.

1. The RUN or LAP key is pressed when one or more keys that are included in the selected combination (here in after referred to as mask) are held down.
2. The RUN or LAP key has been pressed when the mask is released.

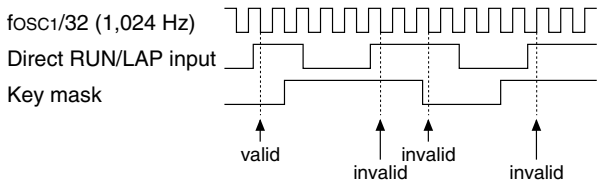


Figure 10.6.4 Operation of key mask

RUN or LAP inputs become valid in the following status.

1. Either the RUN or LAP key is pressed independently if no other key is been held down.
2. Both the RUN and LAP keys are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)
3. The RUN or LAP key is pressed if either is held down. (RUN and LAP functions are effective.)
4. Either the RUN or LAP key and the mask key are pressed at the same time if no other key is held down.
5. Both the RUN and LAP keys and the mask key are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)

* Simultaneous key input is referred to as two or more key inputs are sampled at the same falling edge of 1,024 Hz clock.

10.7 Interrupt Function

10 Hz and 1 Hz interrupts

The 10 Hz and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWD[7:4] and SWD[11:8] respectively. Also, software can set whether to separately mask the frequencies described earlier.
Figure 10.7.1 is the timing chart for the counters.

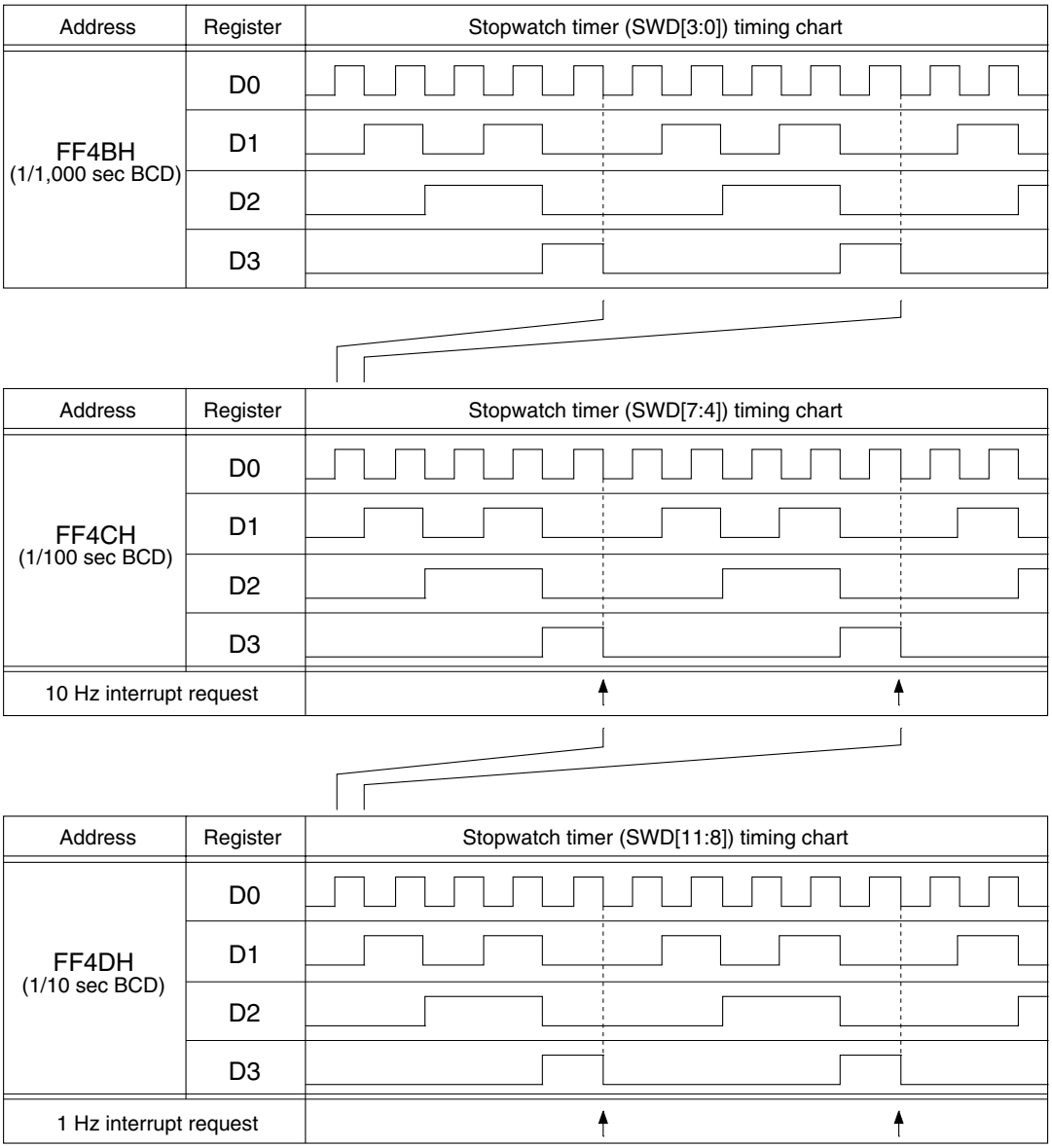


Figure 10.7.1 Timing chart for counters

As shown in Figure 10.7.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flag (ISW10, ISW1) is set to "1."
The respective interrupts can be masked separately through the interrupt mask registers (EISW10, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Direct RUN and direct LAP interrupts [S1C63004/008/016]

When the direct input function is selected, the direct RUN and direct LAP interrupts can be generated. The respective interrupts occur at the rising edge of the internal signal for direct RUN and direct LAP after sampling the direct input signal in the falling edge of 1,024 Hz signal. Also, at this time the corresponding interrupt factor flag (IRUN, ILAP) is set to "1."
The respective interrupts can be masked separately through the interrupt mask registers (EIRUN, EILAP). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the inputs of the RUN and LAP.

The direct RUN and LAP functions use the P00 and P01 ports. Therefore, the direct input interrupt and the P00–P03 inputs interrupt may generate at the same time depending on the interrupt condition setting for the input port P00–P03. Consequently, when using the direct input interrupt, set the interrupt select registers SIP00 and SIP01 to "0" so that the input interrupt does not generate by P00 and P01 inputs.

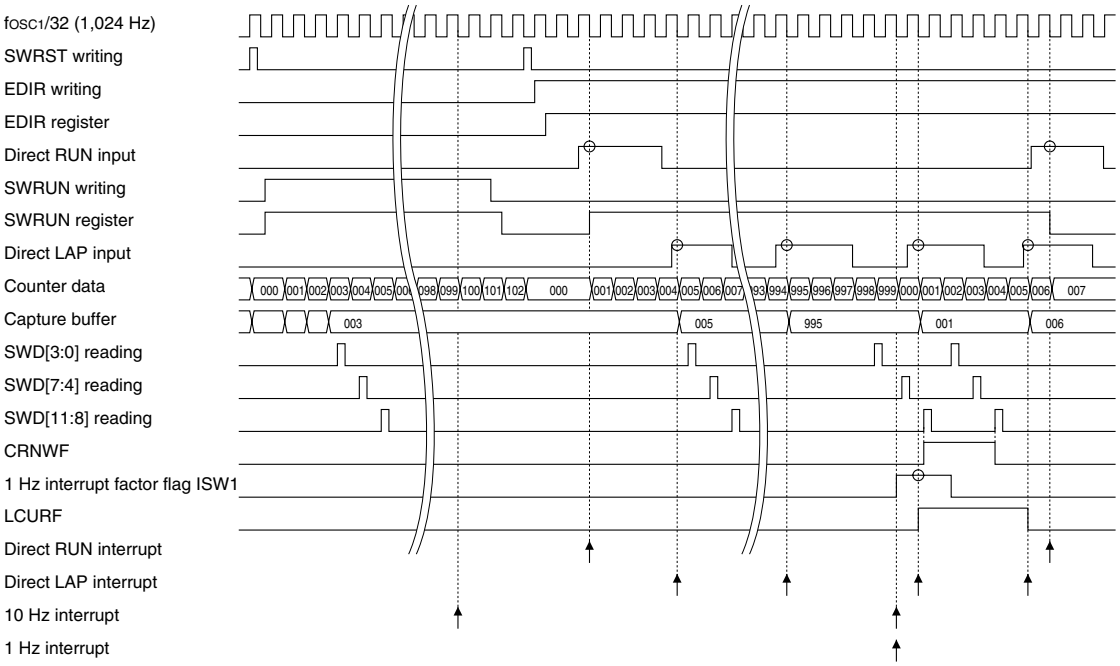


Figure 10.7.2 Timing chart for stopwatch timer

10.8 I/O Memory of Stopwatch Timer

Table 10.8.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 10.8.1 Control bits of stopwatch timer

Address		Register name	R/W	Default	Setting/data				Function
FF16H	D3	MDCKE (*5)	R/W	0	1	Enable	0	Disable	Integer multiplier clock enable
	D2	SGCKE	R/W	0	1	Enable	0	Disable	Sound generator clock enable
	D1	**SWCKE**	R/W	0	1	Enable	0	Disable	Stopwatch timer clock enable
	D0	RTCKE	R/W	0	1	Enable	0	Disable	Clock timer clock enable
FF48H	D3	0 (*3)	R	– (*2)	–				Unused
(*6)	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**SWDIR**	R/W	0	1	P00 = Lap P01 = Run/Stop	0	P00 = Run/Stop P01 = Lap	Stopwatch direct input switch
	D0	**EDIR**	R/W	0	1	Enable	0	Disable	Direct input enable
FF49H	D3	0 (*3)	R	– (*2)	–				Unused
(*6)	D2	**DKM2**	R/W	0	7	P10–13	4	P10	1 P02	Key mask selection
	D1	**DKM1**	R/W	0	6	P10–12	3	P02–03,10	0 No mask	
	D0	**DKM0**	R/W	0	5	P10–11	2	P02–03	

Address		Register name	R/W	Default	Setting/data				Function
FF4AH	D3	**LCURF** (*6)	R	0	1	Request	0	No	Lap data carry-up request flag
	D2	**CRNWF** (*6)	R	0	1	Renewal	0	No	Capture renewal flag
	D1	**SWRUN**	R/W	0	1	Run	0	Stop	Stopwatch timer Run/Stop
	D0	**SWRST** (*3)	W	(Reset)	1	Reset	0	Invalid	Stopwatch timer reset (writing)
FF4BH	D3	**SWD3**	R	0	0–9				Stopwatch timer data BCD (1/1000 sec)
	D2	**SWD2**	R	0					
	D1	**SWD1**	R	0					
	D0	**SWD0**	R	0					
FF4CH	D3	**SWD7**	R	0	0–9				Stopwatch timer data BCD (1/100 sec)
	D2	**SWD6**	R	0					
	D1	**SWD5**	R	0					
	D0	**SWD4**	R	0					
FF4DH	D3	**SWD11**	R	0	0–9				Stopwatch timer data BCD (1/10 sec)
	D2	**SWD10**	R	0					
	D1	**SWD9**	R	0					
	D0	**SWD8**	R	0					

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

SWCKE: Stopwatch timer clock enable register (FF16H•D1)

Controls the operating clock supply to the stopwatch timer.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to SWCKE, the stopwatch timer operating clock is supplied from the clock manager. If it is not necessary to run the stopwatch timer, stop the clock supply by setting SWCKE to "0" to reduce current consumption. At initial reset, this register is set to "0."

EDIR: Direct input function enable register (FF48H•D0) – S1C63004/008/016

Enables the direct input (RUN/LAP) function.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function is enabled by writing "1" to EDIR, and then RUN/STOP and LAP control can be done by external key input. When "0" is written, the direct input function is disabled, and the stopwatch timer is controlled by the software only. Further the function switching is actually done by synchronizing with the falling edge of fOSC1/32 (1,024 Hz) after the data is written to this register (after 977 µsec maximum). At initial reset, this register is set to "0."

SWDIR: Direct input switch register (FF48H•D1) – S1C63004/008/016

Switches the direct-input key assignment for the P00 and P01 ports.

When "1" is written: P00 = LAP, P01 = RUN/STOP
When "0" is written: P00 = RUN/STOP, P01 = LAP
Reading: Valid

The direct-input key assignment is selected using this register. The P00 and P01 port statuses are input to the stopwatch timer as the RUN/STOP and LAP inputs according to this selection. At initial reset, this register is set to "0."

DKM[2:0]: Direct key mask select register (FF49H•D[2:0]) – S1C63004/008/016

Selects a combination of the key inputs for concurrence judgment with RUN and LAP inputs when the direct input function is set.

Table 10.8.2 Key mask selection

DKM[2:0]	Mask key combination
0H	None (at initial reset)
1H	P02
2H	P02, P03
3H	P02, P03, P10
4H	P10
5H	P10, P11
6H	P10, P11, P12
7H	P10, P11, P12, P13

When the concurrence is detected, RUN and LAP inputs cannot be accepted until the concurrence is released. At initial reset, this register is set to "0."

SWRST: Stopwatch timer reset (FF4AH•D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. Since this reset does not affect the capture buffer, the capture buffer data in hold status is not cleared and is maintained. This bit is write-only, and is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP (FF4AH•D1)

This register controls the RUN/STOP of the stopwatch timer, and the operating status can be monitored by reading this register.

When writing data

When "1" is written: RUN
When "0" is written: STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. RUN/STOP control with this register is valid only when the direct input function is set to disable (always effective in the S1C63003). When the direct input function is set, it becomes invalid.

When reading data

When "1" is read: RUN
When "0" is read: STOP

Reading is always valid regardless of the direct input function setting. "1" is read when the stopwatch timer is in the RUN status, and "0" is read in the STOP status.
At initial reset, this register is set to "0."

CRNWF: Capture renewal flag (FF4AH•D2) – S1C63004/008/016

This flag indicates that the content of the capture buffer has been renewed.

When "1" is read: Renewed
When "0" is read: Not renewed
Writing: Invalid

The content of the capture buffer is renewed if the LAP key is input when the data held into the capture buffer has not yet been read. Reading SWD[11:8] in that status sets this flag to "1," and the hold status is maintained. Consequently, when data that is held by a LAP input is read, read this flag after reading the SWD[11:8] and check whether the data has been renewed or not. This flag is renewed when SWD[11:8] is read. At initial reset, this flag is set to "0."

LCURF: Lap data carry-up request flag (FF4AH•D3) – S1C63004/008/016

This flag indicates a carry that has been generated to 1 sec-digit when the data is held. Note that this flag is invalid when the direct input function is disabled.

When "1" is read: Carry is required
When "0" is read: Carry is not required
Writing: Invalid

If the capture buffer shifts into hold status while the 1 Hz interrupt factor flag ISW1 is set to "1," LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required. When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read this flag before processing and check whether carry-up is needed or not. This flag is renewed (set/reset) every time the capture buffer shifts into hold status. At initial reset, this flag is set to "0."

SWD[3:0]: Stopwatch timer data 1/1,000 sec (FF4BH)

Data (BCD) of the 1/1,000 sec column of the capture buffer can be read out. The hold function of the capture buffer works by reading this data. These 4 bits are read-only, and cannot be used for writing operations. At initial reset, the timer data is set to "0."

SWD[7:4]: Stopwatch timer data 1/100 sec (FF4CH)

Data (BCD) of the 1/100 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations. At initial reset, the timer data is set to "0."

SWD[11:8]: Stopwatch timer data 1/10 sec (FF4DH)

Data (BCD) of the 1/10 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations. At initial reset, the timer data is set to "0."

Note: Be sure to data reading in the order of SWD[3:0] → SWD[7:4] → SWD[11:8].

10.9 Precautions

- The interrupt factor flag should be reset after resetting the stopwatch timer.
- Be sure to data reading in the order of SWD[3:0] → SWD[7:4] → SWD[11:8].
- When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD[11:8] and check whether the data has been renewed or not.
- When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

11 Programmable Timer

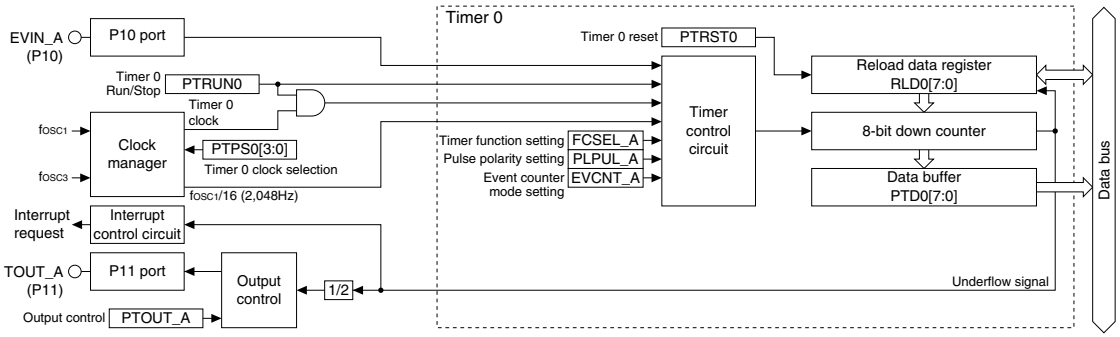
11.1 Configuration of Programmable Timer

The S1C63004/008/016 has built-in two (Ch.A and Ch.B) units of programmable timers. The S1C63003 has a built-in single unit of programmable timer (Ch.A). The timer configurations of Ch.A and Ch.B are shown below. This module allows the software to configure timer channels.

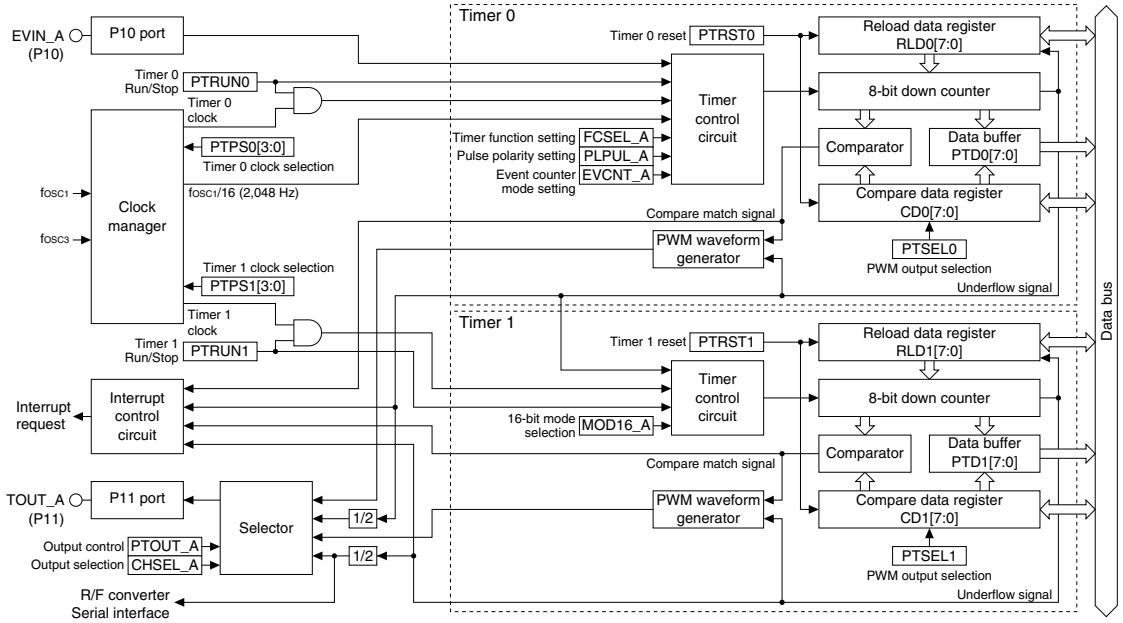
Table 11.1.1 Configuration of programmable timer

Model	Ch.A		Ch.B	
	8-bit mode	16-bit mode	8-bit mode	16-bit mode
S1C63016	Timer 0 and Timer 1 (8 bits × 2 channels)	Timer 0 + Timer 1 (16 bits × 1 channel)	Timer 2 and Timer 3 (8 bits × 2 channels)	Timer 2 + Timer 3 (16 bits × 1 channel)
S1C63008			Timer 2 (8 bits × 1 channel)	Not available
S1C63004				
S1C63003	Timer 0 (8 bits × 1 channel)	Not available		

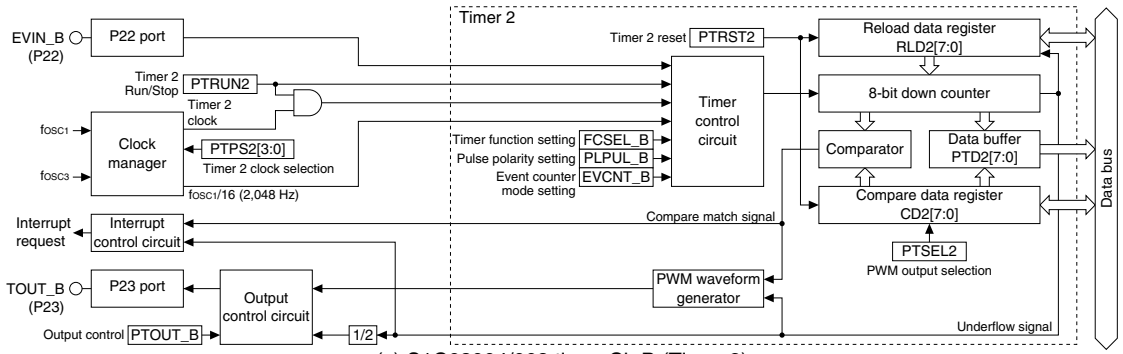
Figure 11.1.1 shows the configuration of the programmable timer.
Each timer has an 8-bit down counter and an 8-bit reload data register. The down counter counts the internal clock of which the frequency can be selected with software. Furthermore, Timers 0 and 2 also have an event counter function to count the clock input from the EVIN_A (P10) and EVIN_B (P22) terminals. When the down counter underflows during counting with the specified clock, the timer outputs the underflow and interrupt signals and resets the counter to its initial value. The reload data register is used to set the initial value.
The underflow signal of Timer 1 (S1C63004/008/016) is used as the source clock of the R/F converter and serial interface, this makes it possible to program a flexible R/F converter count clock and the transfer rate of the serial interface.
Each timer of the S1C63004/008/016 has an 8-bit compare data register in addition to the above registers. This register is used to store data to be compared with the contents of the down counter. When the timer is set to PWM mode, the timer outputs the compare match signal if the contents between the down counter and the compare data register are matched, and an interrupt occurs at the same time. Also the compare match signal is used with the underflow signal to generate a PWM waveform.
The signal generated by the programmable timer can be output from the TOUT_A (P11) or TOUT_B (P23) port terminal.



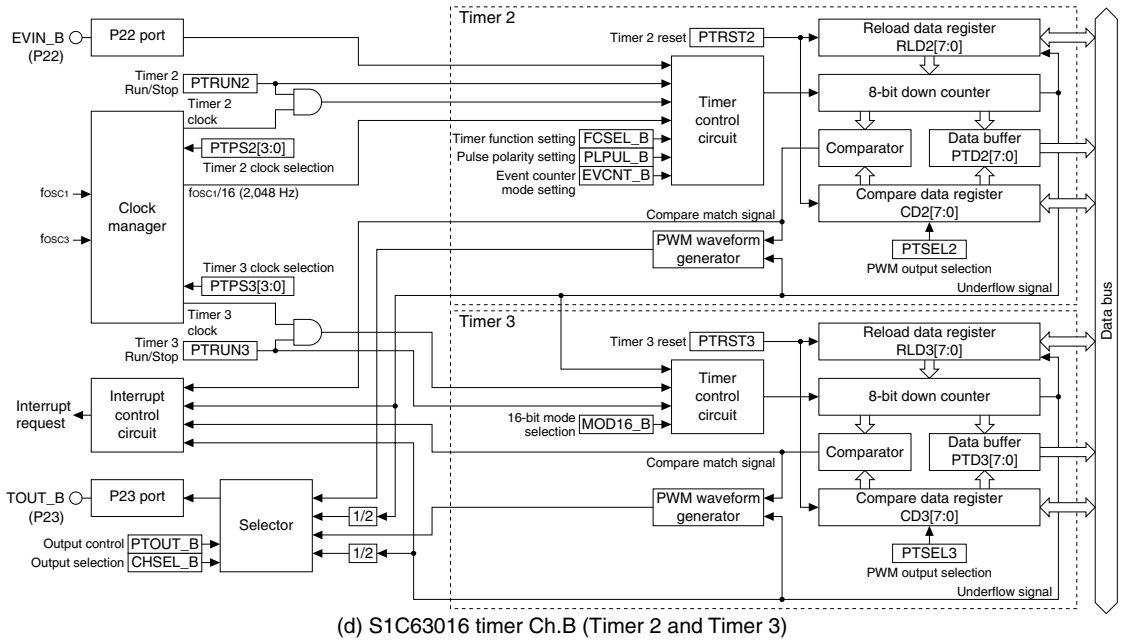
(a) S1C63003 timer Ch.A (Timer 0)



(b) S1C63004/008/016 timer Ch.A (Timer 0 and Timer 1)



(c) S1C63004/008 timer Ch.B (Timer 2)



(d) S1C63016 timer Ch.B (Timer 2 and Timer 3)

Figure 11.1.1 Configuration of programmable timer

Notes:
- The functions shown below are not implemented in the S1C63003 programmable timer.
  - Timer 1 to Timer 3
  - EVIN_B input and TOUT_B output
  - 16-bit mode
  - Compare data register and comparator
  - PWM output function and compare match interrupt
  - R/F converter clock supply
- The functions shown below are not implemented in the S1C63004/008 programmable timer.
  - Timer 3
  - 16-bit mode in Ch.B
- Each timer has the same basic functions except the register names, I/O ports used and their signal names. The description in this section applies to all timers otherwise a timer number (0 to 3) or a unit number (A or B) is specified. The 'x' in the register name refers to the timer number (0 to 3).
  Examples:
  Timer x → Can be replaced with Timer 0 to Timer 3.
  PTRUNx register → Can be replaced with PTRUN0 to PTRUN3 registers.
- If the TOUT_A and/or TOUT_B terminals are used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to "Precautions on Mounting" in the Appendix for more information.

11.2 Controlling Operating Clock

The clock manager generates the down-count clock for each timer by dividing the OSC1 or OSC3 clock. Table 11.2.1 lists the 15 count clocks that can be generated by the clock manager, and the clock to be used for each timer can be selected using the count clock frequency select register PTPSx[3:0]. At initial reset, the PTPSx[3:0] register is set to "0H" and the clock supply from the clock manager to the programmable timer is disabled. Before the timer can be run, select a clock to enable the clock supply.

Table 11.2.1 Selecting count clock frequency

PTPSx[3:0]	Timer clock
FH	f_{OSC3}
EH	f_{OSC3} / 2
DH	f_{OSC3} / 4
CH	f_{OSC3} / 8
BH	f_{OSC3} / 16
AH	f_{OSC3} / 32
9H	f_{OSC3} / 64
8H	f_{OSC3} / 256
7H	f_{OSC1} (32 kHz)
6H	f_{OSC1} / 2 (16 kHz)
5H	f_{OSC1} / 4 (8 kHz)
4H	f_{OSC1} / 16 (2 kHz)
3H	f_{OSC1} / 32 (1 kHz)
2H	f_{OSC1} / 64 (512 Hz)
1H	f_{OSC1} / 256 (128 Hz)
0H	Off

f_{OSC1}: OSC1 oscillation frequency. ( ) indicates the frequency when f_{OSC1} = 32 kHz.
f_{OSC3}: OSC3 oscillation frequency

Stop the clock supply to the timers shown below by setting PTPSx[3:0] to "0H" to reduce current consumption.
- Unused timer
- Timer used as an event counter that inputs an external clock
- Upper 8-bit timer (Timer 1, Timer 3) when a timer unit is used as a 16-bit × 1 channel configuration.

11.3 Basic Counter Operation

This section explains the basic count operation when each timer is used as an individual 8-bit timer.
Each timer has an 8-bit down counter and an 8-bit reload data register.
The reload data register RLDx[7:0] is used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRSTx, the down counter loads the initial value set in the reload register. Therefore, down-counting is executed from the stored initial value by the count clock.
The PTRUNx register is provided to control the RUN/STOP for each timer. By writing "1" to this register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.
The counter data can be read via the data buffer PTDx[7:0] in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data (PTDx[7:4]) when the low-order data (PTDx[3:0]) is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.
The counter reloads the initial value set in the reload data register when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation and pulse (TOUT_A/TOUT_B signal) output. The underflow signal of Timer 1 (S1C63004/008/016) is also used to generate the clock to be supplied to the serial interface and R/F converter.

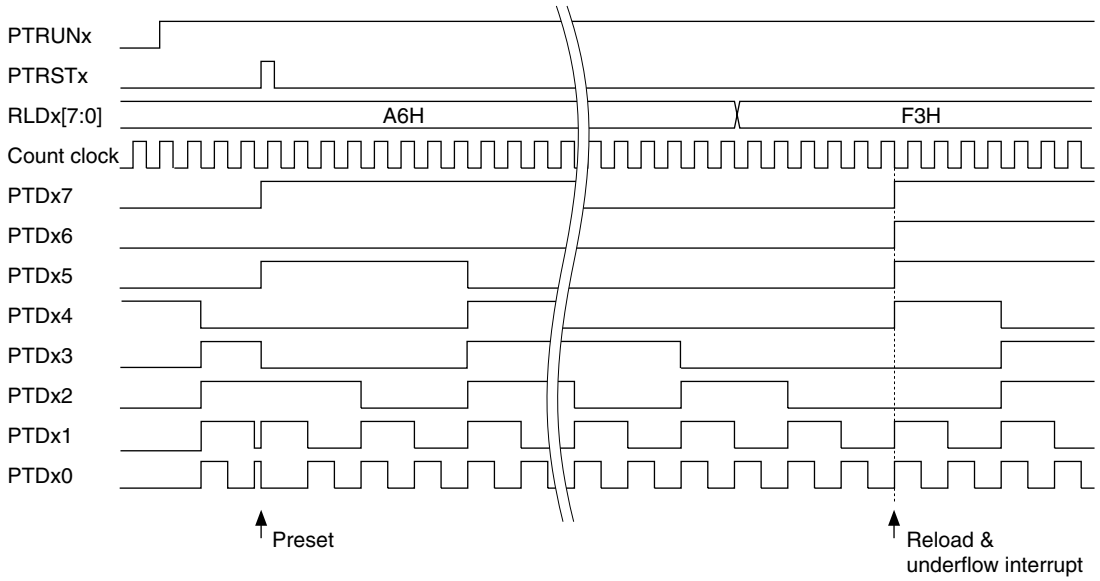


Figure 11.3.1 Basic operation timing of down counter

11.4 Event Counter Mode (Timers 0 and 2)

Timer 0/Timer 2 has an event counter function that counts an external clock input to an I/O port. Table 11.4.1 lists the timers and their clock input ports.

Table 11.4.1 Event counter clock input port

Timer	External clock input terminal	Control register
Timer 0 (Ch.A)	EVIN_A (P10)	EVCNT_A
Timer 2 (Ch.B) *	EVIN_B (P22) *	EVCNT_B *

* S1C63004/008/016

This function is selected by writing "1" to the counter mode select register EVCNT_A/EVCNT_B. This sets the corresponding I/O port to input mode and enables the port to send the input signal to Timer 0/Timer 2 as the count clock. At initial reset, EVCNT_A/EVCNT_B is set to "0" and Timer 0/Timer 2 is configured as a normal timer that counts the internal clock.

In the event counter mode, the clock is supplied to Timer 0/Timer 2 from outside the IC, therefore, the settings of the count clock frequency select register PTPS0[3:0]/PTPS2[3:0] becomes invalid.
Count down timing can be selected from either the falling or rising edge of the input clock using the pulse polarity select register PLPUL_A/PLPUL_B. When "0" is written to the PLPUL_A/PLPUL_B register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 11.4.1.

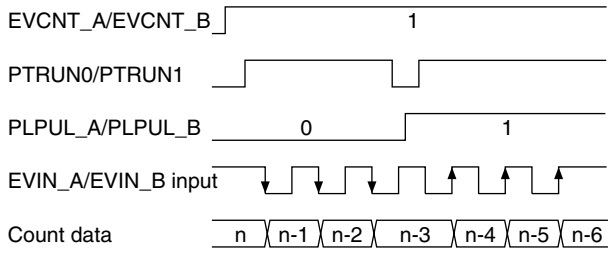


Figure 11.4.1 Timing chart in event counter mode

The event counter mode also allows use of a noise reject function to eliminate noise such as chattering on the external clock (EVIN_A/EVIN_B). This function is selected by writing "1" to the timer function select register FCSEL_A/FCSEL_B.
When the noise rejector is enabled, an input pulse width for both low and high levels must be 0.98 msec∗ or more to count reliably. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz∗ signal after changing the input level of the EVIN_A/EVIN_B input terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec∗ or less. (∗: when f_{OSC1} = 32.768 kHz)
Figure 11.4.2 shows the count down timing with noise rejector.

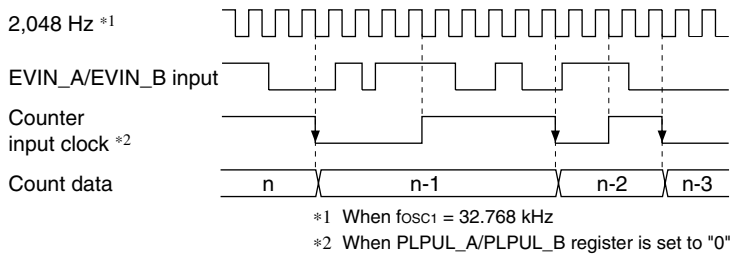


Figure 11.4.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the normal timer except it uses the EVIN_A/EVIN_B input as the count clock. Refer to "11.3 Basic Counter Operation" for basic operation and control.

11.5 PWM mode (Timers 0–3) [S1C63004/008/016]

Each timer of the S1C63004/008/016 can generate a PWM waveform. When using this function, write "1" to the PTSELx register to set the timer to PWM mode.
The compare data register CDx[7:0] is provided for each timer to control the PWM waveform. In PWM mode, the timer compares data between the down counter and the compare data register and outputs the compare match signal if their contents are matched. At the same time a compare match interrupt occurs. Furthermore, the timer output signal rises with the underflow signal and falls with the compare match signal. As shown in Figure 11.5.1, the cycle and duty ratio of the output signal can be controlled using the reload data register and the compare data register, respectively, to generate a PWM signal. Note, however, the following condition must be met: RLD (reload data) > CD (compare data) and CD ≠ 0. If RLD ≤ CD, the output signal is fixed at "1" after the first underflow occurs and does not fall to "0."
The generated PWM signal can be output from the TOUT_A (P11) or TOUT_B (P23) terminal (see Section 11.8).

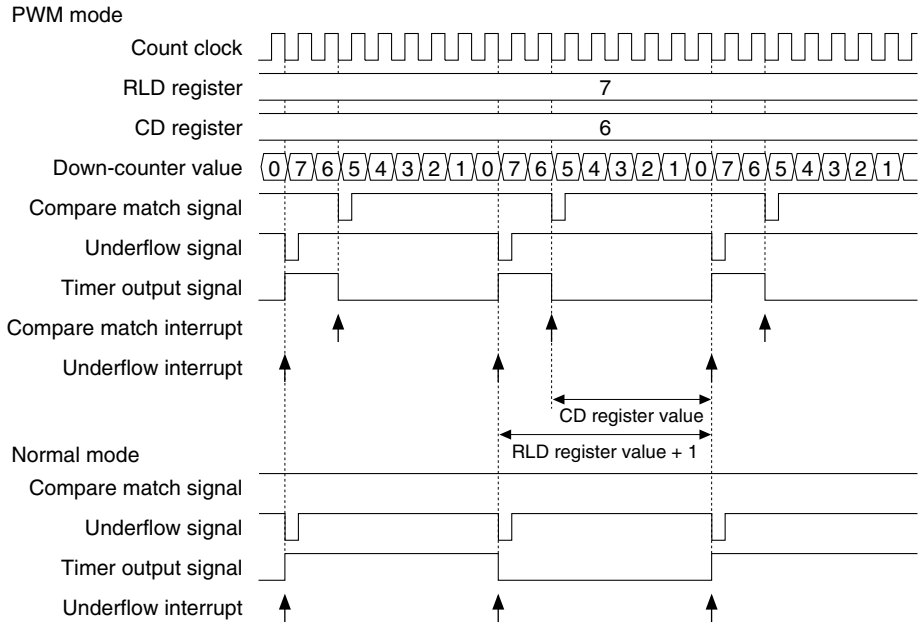


Figure 11.5.1 Generating PWM waveform

11.6 16-bit timer mode (Timer 0 + 1, Timer 2 + 3) [S1C63004/008/016]

In the S1C63004/008/016, Ch.A can be used as a 16-bit timer by coupling Timers 0 and 1. In the S1C63016, Ch.B can also be used as a 16-bit timer by coupling Timers 2 and 3.
To use Ch.A (Timers 0 and 1) as a 16-bit timer, write "1" to the Timer 0 16-bit mode select register MOD16_A. The 16-bit timer is configured with Timer 0 for low-order byte and Timer 1 for high-order byte as shown in Figure 11.6.1.

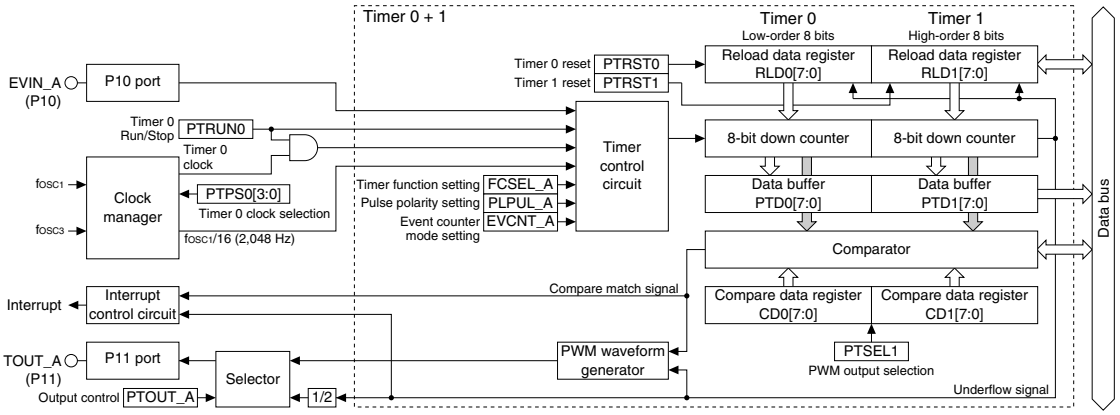


Figure 11.6.1 Configuration of 16-bit timer (Timer 0 + 1)

In 16-bit timer mode, the Timer 0 register settings are effective for timer RUN/STOP control and count clock frequency selection. The event counter function can also be used. Timer 1 uses the Timer 0 underflow signal as the count clock, therefore, the Timer 1 RUN/STOP control and count clock frequency select registers become invalid. However, the PWM output function must be controlled using the Timer 1 control register. Timer 1 output signal is automatically selected for the TOUT_A output (the TOUT_A output select register is ineffective). The reload data must be preset to Timer 0 and Timer 1 separately using each PTRSTx register.

The counter data of a 16-bit timer must be read from the low-order 4 bits. In 16-bit timer mode, the high-order data (PTD0[7:4], PTD1[3:0], PTD1[7:4]) is latched by reading the low-order 4 bits (PTD0[3:0]). The counter keeps counting. However, the latched high-order data is maintained until the next reading of low-order data. Therefore, after the low-order 4-bit data (PTD0[3:0]) is read, the high-order data (PTD0[7:4], PTD1[3:0], PTD1[7:4]) can be read regardless of the order for reading. If data other than the low-order 4 bits (PTD0[3:0]) is read first, the hold function is not activated. In this case, the correct counter data cannot be read.

The description above is applied when Ch. B (Timers 2 and 3) is used as a 16-bit timer in the S1C63016.

11.7 Interrupt Function

The programmable timer can generate interrupts from the underflow and compare match signals of each timer. See Figures 11.3.1 and 11.5.1 for the interrupt timing.

Notes:
- The compare match interrupt can be generated only when the timer is set to PWM mode.
- The compare match interrupt can not be used in the S1C63003.

The underflow and compare match signals set the corresponding interrupt factor flag IPTx and ICTCx to "1," and an interrupt is generated. The interrupt can also be masked by setting the corresponding interrupt mask registers EIPTx and EICTCx. However, the interrupt factor flag is set to "1" by an underflow/compare match of the corresponding timer regardless of the interrupt mask register setting.

When Ch.A is used as a 16-bit timer, an interrupt is generated by an underflow of Timer 1. In this case, IPT0 is not set to "1" by a Timer 0 underflow. The compare match interrupt uses ICTC1 of Timer 1. The same applies when Ch.B is used as a 16-bit timer.

11.8 TOUT Output Control

The programmable timer Ch.A/Ch.B can generate the TOUT_A/TOUT_B signal from the timer underflow and compare match signals. The TOUT_A/TOUT_B signal is generated by dividing the underflow signal by 2 in normal mode. In PWM mode (S1C63004/008/016), the PWM signal generated as described above is output as the TOUT_A/TOUT_B signal.

Table 11.8.1 TOUT outputs and control registers (S1C63016)

Output terminal	Output control register	Output select register	Output timer
TOUT_A (P11)	PTOUT_A	CHSEL_A = "0"	Timer 0
		CHSEL_A = "1"	Timer 1
TOUT_B (P23)	PTOUT_B	CHSEL_B = "0"	Timer 2
		CHSEL_B = "1"	Timer 3

Table 11.8.2 TOUT outputs and control registers (S1C63004/008)

Output terminal	Output control register	Output select register	Output timer
TOUT_A (P11)	PTOUT_A	CHSEL_A = "0"	Timer 0
		CHSEL_A = "1"	Timer 1
TOUT_B (P23)	PTOUT_B	–	Timer 2

Table 11.8.3 TOUT output and control register (S1C63003)

Output terminal	Output control register	Output select register	Output timer
TOUT_A (P11)	PTOUT_A	–	Timer 0

The TOUT output select register CHSEL_A/CHSEL_B allows selection of either Timer 0/Timer 2 or Timer 1/Timer 3 to be used as the TOUT output (the S1C63003 TOUT channel is fixed at Timer 0). In 16-bit timer mode, Timer 1/Timer 3 is always selected for generating the TOUT_A/TOUT_B signal regardless of how CHSEL_A/CHSEL_B is set.

The TOUT signal generated by each timer can be output from the TOUT_A (P11) or TOUT_B (P23) terminal to supply a clock to an external device.

The TOUT_A/TOUT_B signal output is controlled by the PTOUT_A/PTOUT_B register. When "1" is written to the PTOUT_A/PTOUT_B register, the TOUT_A/TOUT_B signal is output from the corresponding I/O port terminal.

When TOUT output is enabled, the I/O port is automatically set to output mode and it outputs the TOUT signal sent from the timer. The I/O control register (IOC11/IOC23) and the data register (P11/P23) are ineffective. When PTOUT_A/PTOUT_B is set to "0," the I/O port control registers become effective.
Since the TOUT_A/TOUT_B signal is generated asynchronously from the PTOUT_A/PTOUT_B register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
Figure 11.8.1 shows the output waveform of the TOUT_A/TOUT_B signal.

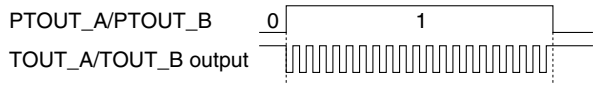


Figure 11.8.1 Output waveform of the TOUT signal

11.9 Clock Output to Serial Interface and R/F Converter [S1C63004/008/016]

In the S1C63004/008/016, the signal that is made from underflows of Timer 1 by dividing them by 2, can be used as the clock source for the serial interface and R/F converter. Timer 1 always outputs the clock to the serial interface and R/F converter by setting Timer 1 into RUN state (PTRUN1 = "1"). It is not necessary to control with the PTOUT_A register.

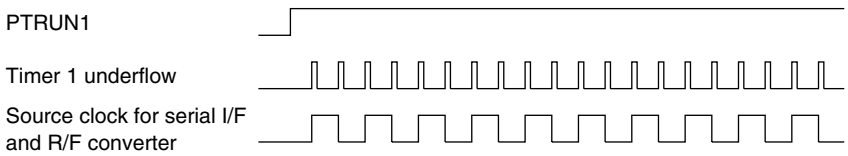


Figure 11.9.1 Clock output to serial interface and R/F converter

A setting value for the RLD1x register according to a transfer rate of the serial interface is calculated by the following expression:

$$RLD1x = \frac{f_{CNT1}}{2*bps} - 1$$

f_{CNT1}: Timer 1 count clock frequency set by the PTPS1 register (See Table 11.2.1.)
bps: Transfer rate
(00H can be set to RLD1x)

Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source.

11.10 I/O Memory of Programmable Timer

Table 11.10.1 shows the I/O addresses and the control bits for the programmable timer.

Table 11.10.1 Control bits of programmable timer

Address		Register name	R/W	Default	Setting/data								Function
FF18H	D3	**PTPS03**	R/W	0	F	f_3	B	$f_3/16$	7	f_1	3	$f_1/32$	Programmable timer 0 count clock frequency selection ($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D2	**PTPS02**	R/W	0	E	$f_3/2$	A	$f_3/32$	6	$f_1/2$	2	$f_1/64$	
	D1	**PTPS01**	R/W	0	D	$f_3/4$	9	$f_3/64$	5	$f_1/4$	1	$f_1/256$	
	D0	**PTPS00**	R/W	0	C	$f_3/8$	8	$f_3/256$	4	$f_1/16$	0	Off	
FF19H (*6)	D3	**PTPS13**	R/W	0	F	f_3	B	$f_3/16$	7	f_1	3	$f_1/32$	Programmable timer 1 count clock frequency selection ($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D2	**PTPS12**	R/W	0	E	$f_3/2$	A	$f_3/32$	6	$f_1/2$	2	$f_1/64$	
	D1	**PTPS11**	R/W	0	D	$f_3/4$	9	$f_3/64$	5	$f_1/4$	1	$f_1/256$	
	D0	**PTPS10**	R/W	0	C	$f_3/8$	8	$f_3/256$	4	$f_1/16$	0	Off	
FF1AH (*6)	D3	**PTPS23**	R/W	0	F	f_3	B	$f_3/16$	7	f_1	3	$f_1/32$	Programmable timer 2 count clock frequency selection ($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D2	**PTPS22**	R/W	0	E	$f_3/2$	A	$f_3/32$	6	$f_1/2$	2	$f_1/64$	
	D1	**PTPS21**	R/W	0	D	$f_3/4$	9	$f_3/64$	5	$f_1/4$	1	$f_1/256$	
	D0	**PTPS20**	R/W	0	C	$f_3/8$	8	$f_3/256$	4	$f_1/16$	0	Off	
FF1BH (*4)	D3	**PTPS33**	R/W	0	F	f_3	B	$f_3/16$	7	f_1	3	$f_1/32$	Programmable timer 3 count clock frequency selection ($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D2	**PTPS32**	R/W	0	E	$f_3/2$	A	$f_3/32$	6	$f_1/2$	2	$f_1/64$	
	D1	**PTPS31**	R/W	0	D	$f_3/4$	9	$f_3/64$	5	$f_1/4$	1	$f_1/256$	
	D0	**PTPS30**	R/W	0	C	$f_3/8$	8	$f_3/256$	4	$f_1/16$	0	Off	

Address		Register name	R/W	Default	Setting/data				Function
FF80H	D3	**MOD16_A** (*6)	R/W	0	1	16 bits	0	8 bits	PTM0–1 16-bit mode selection
	D2	**EVCNT_A**	R/W	0	1	Event counter	0	Timer	PTM0 counter mode selection
	D1	**FCSEL_A**	R/W	0	1	With noise reject	0	No noise reject	PTM0 function selection (for event counter mode)
	D0	**PLPUL_A**	R/W	0	1	↑ (positive)	0	↓ (negative)	PTM0 pulse polarity selection (event counter mode)
FF81H	D3	**PTSEL1** (*6)	R/W	0	1	PWM	0	Normal	Programmable timer 1 PWM output selection
	D2	**PTSEL0** (*6)	R/W	0	1	PWM	0	Normal	Programmable timer 0 PWM output selection
	D1	**CHSEL_A** (*6)	R/W	0	1	Timer 1	0	Timer 0	PTM0–1 TOUT_A output selection
	D0	**PTOUT_A**	R/W	0	1	On	0	Off	PTM0–1 TOUT_A output control
FF82H	D3	**PTRST1** (*3,*6)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 1 reset (reload)
	D2	**PTRUN1** (*6)	R/W	0	1	Run	0	Stop	Programmable timer 1 Run/Stop
	D1	**PTRST0** (*3)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 0 reset (reload)
	D0	**PTRUN0**	R/W	0	1	Run	0	Stop	Programmable timer 0 Run/Stop
FF84H	D3	**RLD03**	R/W	0	0H–FH				Programmable timer 0 reload data (low-order 4 bits) RLD00 = LSB
	D2	**RLD02**	R/W	0					
	D1	**RLD01**	R/W	0					
	D0	**RLD00**	R/W	0					
FF85H	D3	**RLD07**	R/W	0	0H–FH				Programmable timer 0 reload data (high-order 4 bits) RLD07 = MSB
	D2	**RLD06**	R/W	0					
	D1	**RLD05**	R/W	0					
	D0	**RLD04**	R/W	0					
FF86H (*6)	D3	**RLD13**	R/W	0	0H–FH				Programmable timer 1 reload data (low-order 4 bits) RLD10 = LSB
	D2	**RLD12**	R/W	0					
	D1	**RLD11**	R/W	0					
	D0	**RLD10**	R/W	0					
FF87H (*6)	D3	**RLD17**	R/W	0	0H–FH				Programmable timer 1 reload data (high-order 4 bits) RLD17 = MSB
	D2	**RLD16**	R/W	0					
	D1	**RLD15**	R/W	0					
	D0	**RLD14**	R/W	0					
FF88H	D3	**PTD03**	R	0	0H–FH				Programmable timer 0 data (low-order 4 bits) PTD00 = LSB
	D2	**PTD02**	R	0					
	D1	**PTD01**	R	0					
	D0	**PTD00**	R	0					
FF89H	D3	**PTD07**	R	0	0H–FH				Programmable timer 0 data (high-order 4 bits) PTD07 = MSB
	D2	**PTD06**	R	0					
	D1	**PTD05**	R	0					
	D0	**PTD04**	R	0					
FF8AH (*6)	D3	**PTD13**	R	0	0H–FH				Programmable timer 1 data (low-order 4 bits) PTD10 = LSB
	D2	**PTD12**	R	0					
	D1	**PTD11**	R	0					
	D0	**PTD10**	R	0					
FF8BH (*6)	D3	**PTD17**	R	0	0H–FH				Programmable timer 1 data (high-order 4 bits) PTD17 = MSB
	D2	**PTD16**	R	0					
	D1	**PTD15**	R	0					
	D0	**PTD14**	R	0					
FF8CH (*6)	D3	**CD03**	R/W	0	0H–FH				Programmable timer 0 compare data (high-order 4 bits) CD00 = LSB
	D2	**CD02**	R/W	0					
	D1	**CD01**	R/W	0					
	D0	**CD00**	R/W	0					
FF8DH (*6)	D3	**CD07**	R/W	0	0H–FH				Programmable timer 0 compare data (high-order 4 bits) CD07 = MSB
	D2	**CD06**	R/W	0					
	D1	**CD05**	R/W	0					
	D0	**CD04**	R/W	0					
FF8EH (*6)	D3	**CD13**	R/W	0	0H–FH				Programmable timer 1 compare data (low-order 4 bits) CD10 = LSB
	D2	**CD12**	R/W	0					
	D1	**CD11**	R/W	0					
	D0	**CD10**	R/W	0					
FF8FH (*6)	D3	**CD17**	R/W	0	0H–FH				Programmable timer 1 compare data (high-order 4 bits) CD17 = MSB
	D2	**CD16**	R/W	0					
	D1	**CD15**	R/W	0					
	D0	**CD14**	R/W	0					
FF90H (*6)	D3	**MOD16_B** (*4)	R/W	0	1	16 bits	0	8 bits	PTM2–3 16-bit mode selection
	D2	**EVCNT_B**	R/W	0	1	Event counter	0	Timer	PTM2 counter mode selection
	D1	**FCSEL_B**	R/W	0	1	With noise reject	0	No noise reject	PTM2 function selection (for event counter mode)
	D0	**PLPUL_B**	R/W	0	1	↑ (positive)	0	↓ (negative)	PTM2 pulse polarity selection (event counter mode)

Address		Register name	R/W	Default	Setting/data				Function
FF91H (*6)	D3	**PTSEL3** (*4)	R/W	0	1	PWM	0	Normal	Programmable timer 3 PWM output selection
	D2	**PTSEL2**	R/W	0	1	PWM	0	Normal	Programmable timer 2 PWM output selection
	D1	**CHSEL_B** (*4)	R/W	0	1	Timer 3	0	Timer 2	PTM2–3 TOUT_B output selection
	D0	**PTOUT_B**	R/W	0	1	On	0	Off	PTM2–3 TOUT_B output control
FF92H (*6)	D3	**PTRST3** (*3,*4)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 3 reset (reload)
	D2	**PTRUN3** (*4)	R/W	0	1	Run	0	Stop	Programmable timer 3 Run/Stop
	D1	**PTRST2** (*3)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 2 reset (reload)
	D0	**PTRUN2**	R/W	0	1	Run	0	Stop	Programmable timer 2 Run/Stop
FF94H (*6)	D3	**RLD23**	R/W	0	0H–FH				Programmable timer 2 reload data (low-order 4 bits) RLD20 = LSB
	D2	**RLD22**	R/W	0					
	D1	**RLD21**	R/W	0					
	D0	**RLD20**	R/W	0					
FF95H (*6)	D3	**RLD27**	R/W	0	0H–FH				Programmable timer 2 reload data (high-order 4 bits) RLD27 = MSB
	D2	**RLD26**	R/W	0					
	D1	**RLD25**	R/W	0					
	D0	**RLD24**	R/W	0					
FF96H (*4)	D3	**RLD33**	R/W	0	0H–FH				Programmable timer 3 reload data (low-order 4 bits) RLD30 = LSB
	D2	**RLD32**	R/W	0					
	D1	**RLD31**	R/W	0					
	D0	**RLD30**	R/W	0					
FF97H (*4)	D3	**RLD37**	R/W	0	0H–FH				Programmable timer 3 reload data (high-order 4 bits) RLD37 = MSB
	D2	**RLD36**	R/W	0					
	D1	**RLD35**	R/W	0					
	D0	**RLD34**	R/W	0					
FF98H (*6)	D3	**PTD23**	R	0	0H–FH				Programmable timer 2 data (low-order 4 bits) PTD20 = LSB
	D2	**PTD22**	R	0					
	D1	**PTD21**	R	0					
	D0	**PTD20**	R	0					
FF99H (*6)	D3	**PTD27**	R	0	0H–FH				Programmable timer 2 data (high-order 4 bits) PTD27 = MSB
	D2	**PTD26**	R	0					
	D1	**PTD25**	R	0					
	D0	**PTD24**	R	0					
FF9AH (*4)	D3	**PTD33**	R	0	0H–FH				Programmable timer 3 data (low-order 4 bits) PTD30 = LSB
	D2	**PTD32**	R	0					
	D1	**PTD31**	R	0					
	D0	**PTD30**	R	0					
FF9BH (*4)	D3	**PTD37**	R	0	0H–FH				Programmable timer 3 data (high-order 4 bits) PTD37 =MSB
	D2	**PTD36**	R	0					
	D1	**PTD35**	R	0					
	D0	**PTD34**	R	0					
FF9CH (*6)	D3	**CD23**	R/W	0	0H–FH				Programmable timer 2 compare data (low-order 4 bits) CD20 = LSB
	D2	**CD22**	R/W	0					
	D1	**CD21**	R/W	0					
	D0	**CD20**	R/W	0					
FF9DH (*6)	D3	**CD27**	R/W	0	0H–FH				Programmable timer 2 compare data (high-order 4 bits) CD27 = MSB
	D2	**CD26**	R/W	0					
	D1	**CD25**	R/W	0					
	D0	**CD24**	R/W	0					
FF9EH (*4)	D3	**CD33**	R/W	0	0H–FH				Programmable timer 3 compare data (low-order 4 bits) CD30 = LSB
	D2	**CD32**	R/W	0					
	D1	**CD31**	R/W	0					
	D0	**CD30**	R/W	0					
FF9FH (*4)	D3	**CD37**	R/W	0	0H–FH				Programmable timer 3 compare data (high-order 4 bits) CD37 = MSB
	D2	**CD36**	R/W	0					
	D1	**CD35**	R/W	0					
	D0	**CD34**	R/W	0					

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

PTPS0[3:0]: Timer 0 count clock frequency select register (FF18H)
PTPS1[3:0]: Timer 1 count clock frequency select register (FF19H) – S1C63004/008/016
PTPS2[3:0]: Timer 2 count clock frequency select register (FF1AH) – S1C63004/008/016
PTPS3[3:0]: Timer 3 count clock frequency select register (FF1BH) – S1C63016

Selects the count clock frequency for each timer.

Table 11.10.2 Selecting count clock frequency

PTPSx[3:0]	Timer clock
FH	fosc3
EH	fosc3 / 2
DH	fosc3 / 4
CH	fosc3 / 8
BH	fosc3 / 16
AH	fosc3 / 32
9H	fosc3 / 64
8H	fosc3 / 256
7H	fosc1 (32 kHz)
6H	fosc1 / 2 (16 kHz)
5H	fosc1 / 4 (8 kHz)
4H	fosc1 / 16 (2 kHz)
3H	fosc1 / 32 (1 kHz)
2H	fosc1 / 64 (512 Hz)
1H	fosc1 / 256 (128 Hz)
0H	Off

fosc1: OSC1 oscillation frequency. ( ) indicates the frequency when fosc1 = 32 kHz.
fosc3: OSC3 oscillation frequency

The clock manager generates the down-count clock for each timer by dividing the OSC1 or OSC3 clock. Table 11.10.2 lists the 15 count clocks that can be generated by the clock manager, and the clock to be used for each timer can be selected using PTPSx[3:0]. At initial reset, the PTPSx[3:0] register is set to "0H" and the clock supply from the clock manager to the programmable timer is disabled. Before the timer can be run, select a clock to enable the clock supply.
Stop the clock supply to the timers shown below by setting PTPSx[3:0] to "0H" to reduce current consumption.
- Unused timer
- Timer used as an event counter that inputs an external clock
- Upper 8-bit timer (Timer 1, Timer 3) when a timer unit is used as 16-bit × 1 channel configuration.

At initial reset, these registers are set to "0."
The S1C63004/008 does not include a register at FF1BH. The S1C63003 does not include registers at FF19H–FF1BH.

PLPUL_A: Timer 0 pulse polarity select register (FF80H•D0)
PLPUL_B: Timer 2 pulse polarity select register (FF90H•D0) – S1C63004/008/016

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode is selected from either the falling edge of the external clock input to the EVIN_A (P10) and EVIN_B (P22) terminals or the rising edge. When "0" is written to these registers, the falling edge is selected and when "1" is written, the rising edge is selected. These registers are effective only when the timer is used in the event counter mode. At initial reset, these registers are set to "0."
The S1C63003 does not include a register at FF90H.

FCSEL_A: Timer 0 function select register (FF80H•D1)
FCSEL_B: Timer 2 function select register (FF90H•D1) – S1C63004/008/016

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector
When "0" is written: Without noise rejector
Reading: Valid

When "1" is written to these registers, the noise rejector is used and counting is done by an external clock (input from EVIN_A or EVIN_B) with 0.98 msec* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the I/O port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less.
(*: When fosc1 = 32.768 kHz)

When "0" is written to these registers, the noise rejector is not used and the counting is done directly by an external clock input to the EVIN_A (P10) or EVIN_B (P22) terminal. These registers are effective only when the timer is used in the event counter mode. At initial reset, these registers are set to "0."
The S1C63003 does not include a register at FF90H.

EVCNT_A: Timer 0 counter mode select register (FF80H•D2)
EVCNT_B: Timer 2 counter mode select register (FF90H•D2) – S1C63004/008/016

Selects the counter mode for each timer.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter modes for Timers 0 and 2 are selected from either the event counter mode or timer mode.
When "1" is written to these registers, event counter mode is selected. In this mode, Timers 0 and 2 count the external clock input from the EVIN_A (P10) and EVIN_B (P22) terminals, respectively. When "0" is written, timer mode is selected. In this mode, the timer counts the internal clock selected by the PTPSx[3:0] register. This selection is effective even when Ch.A/Ch.B is used in 16-bit timer mode. At initial reset, these registers are set to "0."
The S1C63003 does not include a register at FF90H.

MOD16_A: Timer 0–1 16-bit timer mode select register (FF80H•D3) – S1C63004/008/016
MOD16_B: Timer 2–3 16-bit timer mode select register (FF90H•D3) – S1C63016

Selects 8-bit or 16-bit timer mode.

When "1" is written: 16-bit timer mode
When "0" is written: 8-bit timer mode
Reading: Valid

These registers are used to select whether Timers 0 and 1 in Ch.A or Timers 2 and 3 in Ch.B are used as two channels of independent 8-bit timers or one channel of combined 16-bit timer. When "0" is written to the register, the timers are set to 8-bit timer mode. When "1" is written, the timers are set to 16-bit timer mode. When Ch.A/Ch.B is used in 16-bit timer mode, Timer 1/Timer 3 operates with the Timer 0/Timer 2 underflow signal as the count clock (both timer mode and event counter mode). In 16-bit timer mode, the Timer 0/Timer 2 register settings are effective for timer RUN/STOP control and count clock frequency selection (Timer 1/Timer 3 registers are ineffective). However, the PWM output function must be controlled using the Timer 1/Timer 3 control register. The reload data must be preset to Timer 0/Timer 2 and Timer 1/Timer 3 separately using each PTRSTx register. At initial reset, these registers are set to "0."
FF90H•D3 in the S1C63004/008 and FF80H•D3 in the S1C63003 are read only bits and always "0" will be read.
The S1C63003 does not include a register at FF90H.

PTOUT_A: TOUT_A output control register (FF81H•D0)
PTOUT_B: TOUT_B output control register (FF91H•D0) – S1C63004/008/016

Controls TOUT signal outputs.

When "1" is written: TOUT output On
When "0" is written: TOUT output Off
Reading: Valid

When "1" is written to the register, the corresponding TOUT_A/TOUT_B signal is output from the P11/P23 terminal. When TOUT output is enabled, the I/O port is automatically set to output mode and it outputs the TOUT signal sent from the timer. The I/O control register (IOC11/IOC23) and the data register (P11/P23) are ineffective. When this register is set to "0," the I/O port control registers become effective. At initial reset, these registers are set to "0."
The S1C63003 does not include a register at FF91H.

CHSEL_A: TOUT_A output select register (FF81H•D1) – S1C63004/008/016
CHSEL_B: TOUT_B output select register (FF91H•D1) – S1C63016

Selects the timer used for TOUT_A/TOUT_B signal output.

When "1" is written: Timer 1 (Ch.A)/Timer 3 (Ch.B)
When "0" is written: Timer 0 (Ch.A)/Timer 2 (Ch.B)
Reading: Valid

These register are used to select whether the Timer 0/Timer 2 output is used as the TOUT_A/TOUT_B signal or the Timer 1/Timer 3 output is used. When "0" is written to the register, the Timer 0/Timer 2 output is selected. When "1" is written, the Timer 1/Timer 3 output is selected. In 16-bit timer mode, the Timer 1/Timer 3 output is always selected regardless of how the register is set.
At initial reset, these registers are set to "0."
FF91H•D1 in the S1C63004/008 and FF81H•D1 in the S1C63003 are read only bits and always "0" will be read. The S1C63003 does not include a register at FF91H.

PTSEL0: Timer 0 PWM mode select register (FF81H•D2) – S1C63004/008/016
PTSEL1: Timer 1 PWM mode select register (FF81H•D3) – S1C63004/008/016
PTSEL2: Timer 2 PWM mode select register (FF91H•D2) – S1C63004/008/016
PTSEL3: Timer 3 PWM mode select register (FF91H•D3) – S1C63016

Sets Timer x for PWM output.

When "1" is written: PWM output
When "0" is written: Normal output
Reading: Valid

When "1" is written to the PTSELx, the compare data register becomes effective and PWM waveform is generated using the underflow and compare match signals. When "0" is written, the timer outputs the normal clock generated from the underflow signal. When Ch.A/Ch.B is set to 16-bit timer mode, the PTSEL0/PTSEL2 register for Timer 0/Timer 2 is ineffective. At initial reset, these registers are set to "0."
FF91H•D3 in the S1C63004/008 and FF81H•D2–D3 in the S1C63003 are read only bits and always "0" will be read. The S1C63003 does not include a register at FF91H.

PTRUN0: Timer 0 RUN/STOP control register (FF82H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FF82H•D2) – S1C63004/008/016
PTRUN2: Timer 2 RUN/STOP control register (FF92H•D0) – S1C63004/008/016
PTRUN3: Timer 3 RUN/STOP control register (FF92H•D2) – S1C63016

Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in Timer x starts counting down by writing "1" to the PTRUNx register and stops by writing "0." In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
When Ch.A/Ch.B is set to 16-bit timer mode, the PTRUN1/PTRUN3 register for Timer 1/Timer 3 is ineffective. At initial reset, these registers are set to "0."
FF92H•D2 in the S1C63004/008 and FF82H•D2 in the S1C63003 are read only bits and always "0" will be read. The S1C63003 does not include a register at FF92H.

PTRST0: Timer 0 reset (reload) (FF82H•D1)
PTRST1: Timer 1 reset (reload) (FF82H•D3) – S1C63004/008/016
PTRST2: Timer 2 reset (reload) (FF92H•D1) – S1C63004/008/016
PTRST3: Timer 3 reset (reload) (FF92H•D3) – S1C63016

Resets the timer and preset reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRSTx, the reload data in the reload register RLDx[7:0] is preset to the counter in Timer x. When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained. No operation results when "0" is written.

The PTRSTx registers are all effective even in 16-bit timer mode, and reload data must be preset to all Timers separately. Since these bits are exclusively for writing, always set to "0" during reading.

FF92H•D3 in the S1C63004/008 and FF82H•D3 in the S1C63003 are read only bits and always "0" will be read. The S1C63003 does not include a register at FF92H.

RLD0[7:0]: Timer 0 reload data register (FF85H, FF84H)
RLD1[7:0]: Timer 1 reload data register (FF87H, FF86H) – S1C63004/008/016
RLD2[7:0]: Timer 2 reload data register (FF95H, FF94H) – S1C63004/008/016
RLD3[7:0]: Timer 3 reload data register (FF97H, FF96H) – S1C63016

Sets the initial value for the counter. The reload data written in these registers are loaded to the respective counters. The counter counts down using the data as the initial value for counting. Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRSTx register, or when counter underflow occurs. At initial reset, these registers are set to "00H."

The S1C63004/008 does not include registers at FF96H–FF97H. The S1C63003 does not include registers at FF86H–FF87H and FF94H–FF97H.

PTD0[7:0]: Timer 0 counter data (FF89H, FF88H)
PTD1[7:0]: Timer 1 counter data (FF8BH, FF8AH) – S1C63004/008/016
PTD2[7:0]: Timer 2 counter data (FF99H, FF98H) – S1C63004/008/016
PTD3[7:0]: Timer 3 counter data (FF9BH, FF9AH) – S1C63016

Count data in the programmable timer can be read from these latches. The low-order 4 bits of the count data in Timer x can be read from PTDx[3:0], and the high-order data can be read from PTDx[7:4]. Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first. In 16-bit timer mode, the high-order 12 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first. Since these latches are exclusively for reading, the writing operation is invalid. At initial reset, these counter data are set to "00H."

The S1C63004/008 does not include registers at FF9AH–FF9BH. The S1C63003 does not include registers at FF8AH–FF8BH and FF98H–FF9BH.

CD0[7:0]: Timer 0 compare data register (FF8DH, FF8CH) – S1C63004/008/016
CD1[7:0]: Timer 1 compare data register (FF8FH, FF8EH) – S1C63004/008/016
CD2[7:0]: Timer 2 compare data register (FF9DH, FF9CH) – S1C63004/008/016
CD3[7:0]: Timer 3 compare data register (FF9FH, FF9EH) – S1C63016

Sets the compare data for PWM output. When the timer is set to PWM mode, the compare data set in this register is compared with the counter data and outputs the compare match signal if they are matched. The compare match signal is used for generating an interrupt and controlling the duty ratio of the PWM waveform.

At initial reset, these registers are set to "00H."

The S1C63004/008 does not include registers at FF9EH–FF9FH. The S1C63003 does not include registers at FF8CH–FF8FH and FF9CH–FF9FH.

11.11 Precautions

- When reading counter data, be sure to read the low-order 4 bits (PTDx[3:0]) first. The high-order 4 bits (PTDx[7:4]) are latched when the low-order 4 bits are read and they are held until the next reading of the low-order 4 bits. In 16-bit timer mode, the high-order 12 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first. When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data to read the proper data.
- The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.

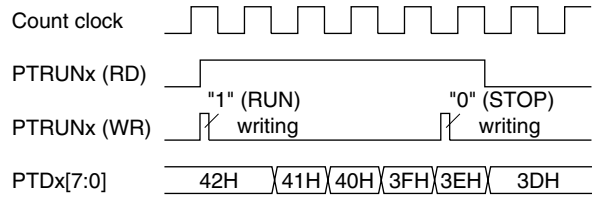


Figure 11.11.1 Timing chart for RUN/STOP control (timer mode)

In event counter mode, the timer starts counting at the first event clock.

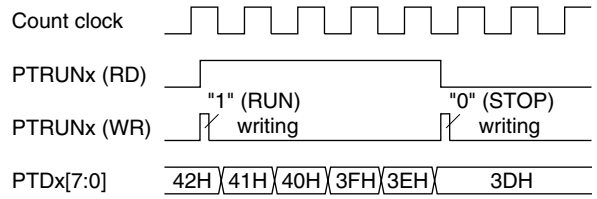


Figure 11.11.2 Timing chart for RUN/STOP control (event counter mode)

- Since the TOUT_A/TOUT_B signal is generated asynchronously from the PTOUT_A/PTOUT_B register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
- When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation on, prior to using the programmable timer. However the OSC3 oscillation circuit requires several tens of µsec to several tens of msec after turning the circuit on until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit on to starting the programmable timer. Refer to the "Oscillation Circuit and Clock Control" chapter, for the control and notes of the OSC3 oscillation circuit.
  At initial reset, the OSC3 oscillation circuit is set in off state.
- For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
  The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

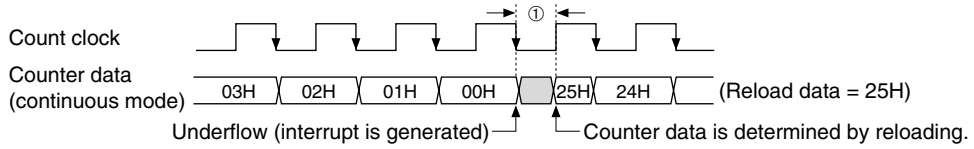


Figure 11.11.3 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

- The programmable timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the programmable timer count data should be read by one of the procedures shown below.

  - Read the count data twice and verify if there is any difference between them.
  - Temporarily stop the programmable timer when the counter data is read to obtain proper data.

12 I/O Ports

12.1 Configuration of I/O Ports

The S1C63003/004/008/016 is equipped with I/O ports in which the input/output direction can be switched with software. Figure 12.1.1 shows the structure of an I/O port.

S1C63016: 24 bits (P00–P03, P10–P13, P20–P23, P30–P33, P40–P43, and P50–P53)
S1C63008: 24 bits (P00–P03, P10–P13, P20–P23, P30–P33, P40–P43, and P50–P53)
S1C63004: 20 bits (P00–P03, P10–P13, P20–P23, P30–P33, and P50–P53)
S1C63003: 16 bits (P00–P03, P10–P13, P20–P23, and P50–P53)

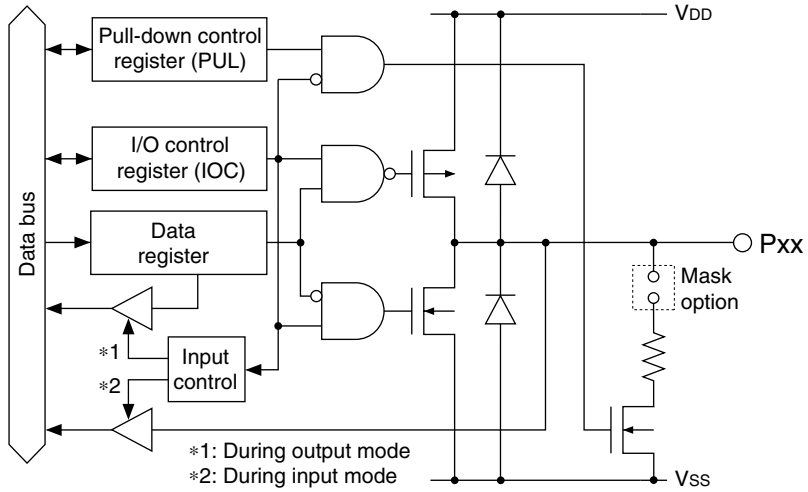


Figure 12.1.1 Structure of I/O port

Note: If an output terminal (including a special output terminal) of this IC is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to "Precautions on Mounting" in the Appendix, for more information.

Each I/O port terminal provides an internal pull-down resistor and it can be connected or disconnected in 1-bit units by mask option. When "Use" is selected by mask option, the port suits input from the push switch, key matrix, and so forth. When "Not use" is selected, the port can be used for slide switch input and interfacing with other LSIs.

The P00 and P01 I/O ports can also be used as the Run/Stop and Lap direct inputs for the stopwatch timer (S1C63004/008/016). The P10 and P22 ports can also be used as the event counter inputs for the programmable timer.
The I/O port terminals P11–P13 and P23 are shared with the special output (TOUT_A, BZ, FOUT, TOUT_B) terminals, P30–P33 are shared with the serial interface input/output terminals, and P50–P53 are shared with the R/F converter input/output terminals. The software can select the function to be used. At initial reset, these terminals are all set to the I/O port.
Table 12.1.1 shows the setting of the input/output terminals by function selection.

Table 12.1.1 Function settings of input/output terminals

Terminal name	Terminal status at initial reset	When special outputs/peripheral functions are used (selected by software)							
		Special output			Serial I/F *2		R/F converter	Stopwatch direct input *2	Event counter
		TOUT	FOUT	BZ	Master	Slave			
P00	P00 (IN & PD *1)							RUN/STOP	
P01	P01 (IN & PD *1)							LAP	
P02	P02 (IN & PD *1)								
P03	P03 (IN & PD *1)								
P10	P10 (IN & PD *1)								EVIN_A
P11	P11 (IN & PD *1)	TOUT_A							
P12	P12 (IN & PD *1)			BZ					
P13	P13 (IN & PD *1)		FOUT						
P20–P21	P20–P21 (IN & PD *1)								
P22	P22 (IN & PD *1)								EVIN_B *2
P23	P23 (IN & PD *1)	TOUT_B *2							
P30 *2	P30 (IN & PD *1)				SCLK(O)	SCLK(I)			
P31 *2	P31 (IN & PD *1)				SOUT(O)	SOUT(O)			
P32 *2	P32 (IN & PD *1)				SIN(I)	SIN(I)			
P33 *2	P33 (IN & PD *1)					SRDY(O)/SS(I)			
P40–P43 *3	P40–P43 (IN & PD *1)								
P50	P50 (IN & PD *1)						RFOUT		
P51	P51 (IN & PD *1)						SEN0		
P52	P52 (IN & PD *1)						REF0		
P53	P53 (IN & PD *1)						RFIN0		

*1: IN & PD (Input with pulled down): When "Pull-Down Used" is selected by mask option (high impedance when "Pull-Down Not Used" is selected)
*2: The P30 to P33 ports, serial interface, stopwatch direct input, TOUT_B output, and EVIN_B input functions are not available in the S1C63003.
*3: The P40 to P43 ports are not available in the S1C63003/004.

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit units). The mode can be set by writing data to the I/O control registers.
When the special output or peripheral function is used, the input/output direction of the port is automatically configured by switching the terminal function and the I/O control registers becomes ineffective. For switching the terminal function and input/output control, refer to respective peripheral circuit chapter.

Note: Before the port function is configured, the circuit that uses the port (e.g. input interrupt, multiple key entry reset, serial interface, R/F converter, event counter input, direct RUN/LAP input for stopwatch) must be disabled.

12.2 Mask Option

Output specification

The output specification of each I/O port during output mode can be selected from either complementary output or P-channel open drain output by mask option. This selection can be done in 1-bit units. When P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

Pull-down resistor

The mask option also allows selection of whether the pull-down resistor is used or not during input mode. This selection can be done in 1-bit units. When "Not use" is selected, take care that the floating status does not occur during input mode.

The pull-down resistor for input mode and output specification (complementary output or P-channel open drain output) selected by mask option are effective even when I/O ports are used for input/output of the serial interface and R/F converter.

SEG outputs

The I/O ports P20–P53 input/output pins are shared with the SEG terminals. This mask option allows selection of whether each of these pins are used for the I/O port or the SEG output. Refer to "Mask Option" in the "LCD Driver" chapter for details.

12.3 I/O Control Registers and Input/Output Mode

The I/O ports can be placed into input or output mode by writing data to the corresponding I/O control registers IOCxx.
To set a port to input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-down explained in Section 12.5 has been enabled by software, the input line is pulled down only during this input mode.
To set a port to output mode, write "1" to the I/O control register. When an I/O port is set to output mode, it works as an output port. The port outputs a high level (V_{DD}) when the port output data is "1," and a low level (V_{SS}) when the port output data is "0." The I/O ports allow software to read data even in output mode. In this case, the data register value is read out.
At initial reset, the I/O control registers are set to "0," and the I/O ports enter input mode.
When the peripheral input/output or special output function is selected (see Table 12.1.1), the input/output direction is controlled by the hardware. In this case, I/O control register settings are ineffective.

12.4 Input Interface Level

The I/O ports P00–P03 and P10–P13 allow software to select an input interface level. When the input interface level select register SMTxx is set to "0," the corresponding port is configured with a CMOS level input interface. When SMTxx is set to "1," the port is configured with a CMOS Schmitt level input interface. At initial reset, all the ports are configured with a CMOS Schmitt level interface.
The input interface level select register of the port that is set for a peripheral input functions the same as the I/O port.
The input interface level of the P2 to P5 ports are fixed at a CMOS Schmitt level.

12.5 Pull-down During Input Mode

A pull-down resistor that activates during the input mode can be built into the I/O ports of the S1C63003/004/008/016 by mask option. The pull-down resistor becomes effective by writing "1" to the pull-down control register PULxx that corresponds to each port, and the input line is pulled down during input mode. When "0" is written to PULxx or in output mode, the port will not be pulled down.
At initial reset, the pull-down control registers are set to "1."
The pull-down control registers of the ports in which the pull-down resistor is disconnected by mask option can be used as general purpose registers.
Even if the pull-down resistor has been connected, the pull-down control register of the port that is set for a peripheral output, R/F converter input/output or output special output (see Table 12.1.1) can be used as a general purpose register that does not affect the pull-down control. The pull-down control register of the port that is set for a peripheral input (except for the R/F converter) functions the same as the I/O port.

12.6 Key Input Interrupt Function

Eight bits of the I/O ports (P00–P03 and P10–P13, four bits of P00–P03 in the S1C63003) provide the interrupt function. The conditions for generating an interrupt can be set with software. Further, whether to mask the interrupt function can be selected with software. Figure 12.6.1 shows the configuration of the key input interrupt circuit.

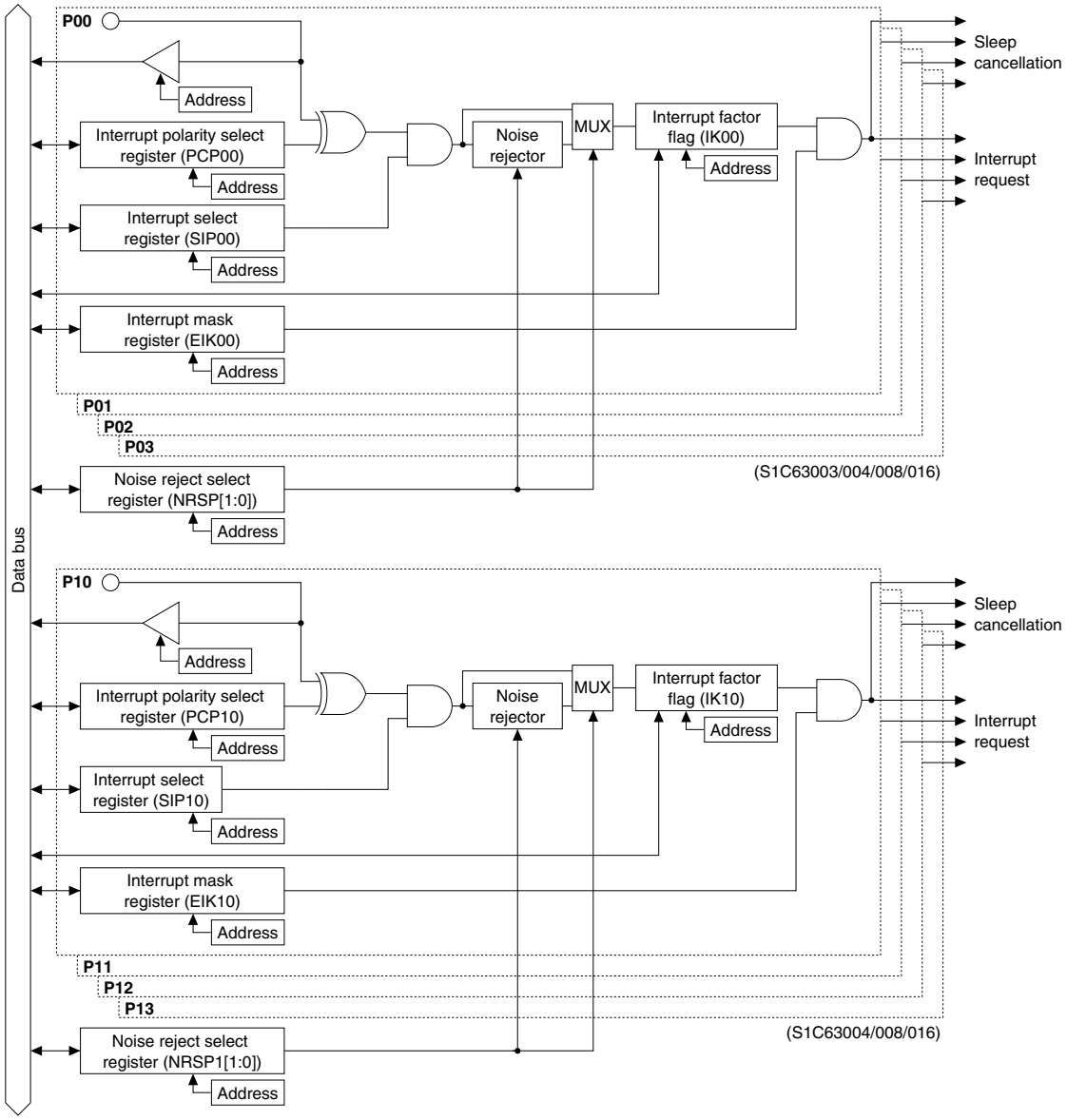


Figure 12.6.1 Key input interrupt circuit configuration

The interrupt select registers (SIP0[3:0], SIP1[3:0]) and interrupt polarity select registers (PCP0[3:0], PCP1[3:0]) are individually provided for the I/O ports P00–P03 and P10–P13.

The interrupt select registers (SIPxx) select the ports to be used for generating interrupts or canceling SLEEP mode. Writing "1" to an interrupt select register incorporates that port into the key input interrupt generation conditions. Changing the port where the interrupt select register has been set to "0" does not affect the generation of the interrupt.

The key input interrupt timing can be selected using the interrupt polarity select registers (PCPxx) so that an interrupt will be generated at the rising edge or falling edge of the input.

By setting these two conditions, an interrupt request signal and a SLEEP cancellation signal are generated at the rising or falling edge (selected by PCPxx) of the signal input to the port (selected by SIPxx).

When a key input interrupt factor occurs, the interrupt factor flag (IK00–IK03, IK10–IK13) is set to "1." At the same time, an interrupt request is generated to the CPU if the corresponding interrupt mask register (EIK00–EIK03, EIK10–EIK13) is set to "1."

When the interrupt mask register (EIKxx) is set to "0," the interrupt request is masked and no interrupt is generated to the CPU.

The key input interrupt circuit has a noise rejector to avoid unnecessary interrupt generation due to noise or chattering. This noise rejector allows selection of a noise-reject frequency from among three types shown in Table 12.6.1. Use the NRSP0[1:0] register for P00–P03 ports or NRSP1[1:0] register for P10–P13 ports to select a noise-reject frequency. If a pulse shorter than the selected width is input to the port, an interrupt is not generated. When high speed response is required, turns the noise rejecter off (bypassed).

Table 12.6.1 Setting up noise rejector

NRSP0[1:0]/NRSP1[1:0]	Noise reject frequency	Reject pulse width
3	f_{OSC1} / 256 (128 Hz)	7.8 msec
2	f_{OSC1} / 64 (512 Hz)	2.0 msec
1	f_{OSC1} / 16 (2 kHz)	0.5 msec
0	Off (bypassed)	–

Notes:
- Be sure to turn the noise rejector off before executing the SLP instruction.
- Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the key input interrupt using the corresponding interrupt mask register (EIKxx = "1") before executing the SLP instruction to run key input interrupt handler routine after SLEEP status is released.

12.7 I/O memory of I/O ports

Table 12.7.1 shows the I/O addresses and the control bits for the I/O ports.

Table 12.7.1 Control bits of I/O ports

Address		Register name	R/W	Default	Setting/data				Function
FF11H	D3	**NRSP11** (*6)	R/W	0	3	f_1/256	1	f_1/16	P1 key input interrupt noise reject frequency selection ($f_1 = f_{OSC1}$)
	D2	**NRSP10** (*6)	R/W	0	2	f_1/64	0	Off	
	D1	**NRSP01**	R/W	0	3	f_1/256	1	f_1/16	P0 key input interrupt noise reject frequency selection ($f_1 = f_{OSC1}$)
	D0	**NRSP00**	R/W	0	2	f_1/64	0	Off	
FF20H	D3	**P03**	R/W	1	1	High	0	Low	P03 I/O port data
	D2	**P02**	R/W	1	1	High	0	Low	P02 I/O port data
	D1	**P01**	R/W	1	1	High	0	Low	P01 I/O port data
	D0	**P00**	R/W	1	1	High	0	Low	P00 I/O port data
FF21H	D3	**IOC03**	R/W	0	1	Output	0	Input	P03 I/O control register
	D2	**IOC02**	R/W	0	1	Output	0	Input	P02 I/O control register
	D1	**IOC01**	R/W	0	1	Output	0	Input	P01 I/O control register
	D0	**IOC00**	R/W	0	1	Output	0	Input	P00 I/O control register
FF22H	D3	**PUL03**	R/W	1	1	Enable	0	Disable	P03 pull-down control register
	D2	**PUL02**	R/W	1	1	Enable	0	Disable	P02 pull-down control register
	D1	**PUL01**	R/W	1	1	Enable	0	Disable	P01 pull-down control register
	D0	**PUL00**	R/W	1	1	Enable	0	Disable	P00 pull-down control register
FF23H	D3	**SMT03**	R/W	1	1	Schmitt	0	CMOS	P03 input I/F level select register
	D2	**SMT02**	R/W	1	1	Schmitt	0	CMOS	P02 input I/F level select register
	D1	**SMT01**	R/W	1	1	Schmitt	0	CMOS	P01 input I/F level select register
	D0	**SMT00**	R/W	1	1	Schmitt	0	CMOS	P00 input I/F level select register
FF24H	D3	**P13**	R/W	1	1	High	0	Low	P13 I/O port data
	D2	**P12**	R/W	1	1	High	0	Low	P12 I/O port data
	D1	**P11**	R/W	1	1	High	0	Low	P11 I/O port data
	D0	**P10**	R/W	1	1	High	0	Low	P10 I/O port data
FF25H	D3	**IOC13**	R/W	0	1	Output	0	Input	P13 I/O control register
	D2	**IOC12**	R/W	0	1	Output	0	Input	P12 I/O control register
	D1	**IOC11**	R/W	0	1	Output	0	Input	P11 I/O control register
	D0	**IOC10**	R/W	0	1	Output	0	Input	P10 I/O control register

Address		Register name	R/W	Default	Setting/data				Function
FF26H	D3	**PUL13**	R/W	1	1	Enable	0	Disable	P13 pull-down control register
	D2	**PUL12**	R/W	1	1	Enable	0	Disable	P12 pull-down control register
	D1	**PUL11**	R/W	1	1	Enable	0	Disable	P11 pull-down control register
	D0	**PUL10**	R/W	1	1	Enable	0	Disable	P10 pull-down control register
FF27H	D3	**SMT13**	R/W	1	1	Schmitt	0	CMOS	P13 input I/F level select register
	D2	**SMT12**	R/W	1	1	Schmitt	0	CMOS	P12 input I/F level select register
	D1	**SMT11**	R/W	1	1	Schmitt	0	CMOS	P11 input I/F level select register
	D0	**SMT10**	R/W	1	1	Schmitt	0	CMOS	P10 input I/F level select register
FF28H	D3	**P23**	R/W	1	1	High	0	Low	P23 I/O port data
	D2	**P22**	R/W	1	1	High	0	Low	P22 I/O port data
	D1	**P21**	R/W	1	1	High	0	Low	P21 I/O port data
	D0	**P20**	R/W	1	1	High	0	Low	P20 I/O port data
FF29H	D3	**IOC23**	R/W	0	1	Output	0	Input	P23 I/O control register
	D2	**IOC22**	R/W	0	1	Output	0	Input	P22 I/O control register
	D1	**IOC21**	R/W	0	1	Output	0	Input	P21 I/O control register
	D0	**IOC20**	R/W	0	1	Output	0	Input	P20 I/O control register
FF2AH	D3	**PUL23**	R/W	1	1	Enable	0	Disable	P23 pull-down control register
	D2	**PUL22**	R/W	1	1	Enable	0	Disable	P22 pull-down control register
	D1	**PUL21**	R/W	1	1	Enable	0	Disable	P21 pull-down control register
	D0	**PUL20**	R/W	1	1	Enable	0	Disable	P20 pull-down control register
FF2CH (*6)	D3	**P33**	R/W	1	1	High	0	Low	P33 I/O port data
	D2	**P32**	R/W	1	1	High	0	Low	P32 I/O port data
	D1	**P31**	R/W	1	1	High	0	Low	P31 I/O port data
	D0	**P30**	R/W	1	1	High	0	Low	P30 I/O port data
FF2DH (*6)	D3	**IOC33**	R/W	0	1	Output	0	Input	P33 I/O control register
	D2	**IOC32**	R/W	0	1	Output	0	Input	P32 I/O control register
	D1	**IOC31**	R/W	0	1	Output	0	Input	P31 I/O control register
	D0	**IOC30**	R/W	0	1	Output	0	Input	P30 I/O control register
FF2EH (*6)	D3	**PUL33**	R/W	1	1	Enable	0	Disable	P33 pull-down control register
	D2	**PUL32**	R/W	1	1	Enable	0	Disable	P32 pull-down control register
	D1	**PUL31**	R/W	1	1	Enable	0	Disable	P31 pull-down control register
	D0	**PUL30**	R/W	1	1	Enable	0	Disable	P30 pull-down control register
FF30H (*5)	D3	**P43**	R/W	1	1	High	0	Low	P43 I/O port data
	D2	**P42**	R/W	1	1	High	0	Low	P42 I/O port data
	D1	**P41**	R/W	1	1	High	0	Low	P41 I/O port data
	D0	**P40**	R/W	1	1	High	0	Low	P40 I/O port data
FF31H (*5)	D3	**IOC43**	R/W	0	1	Output	0	Input	P43 I/O control register
	D2	**IOC42**	R/W	0	1	Output	0	Input	P42 I/O control register
	D1	**IOC41**	R/W	0	1	Output	0	Input	P41 I/O control register
	D0	**IOC40**	R/W	0	1	Output	0	Input	P40 I/O control register
FF32H (*5)	D3	**PUL43**	R/W	1	1	Enable	0	Disable	P43 pull-down control register
	D2	**PUL42**	R/W	1	1	Enable	0	Disable	P42 pull-down control register
	D1	**PUL41**	R/W	1	1	Enable	0	Disable	P41 pull-down control register
	D0	**PUL40**	R/W	1	1	Enable	0	Disable	P40 pull-down control register
FF34H	D3	**P53**	R/W	1	1	High	0	Low	P53 I/O port data
	D2	**P52**	R/W	1	1	High	0	Low	P52 I/O port data
	D1	**P51**	R/W	1	1	High	0	Low	P51 I/O port data
	D0	**P50**	R/W	1	1	High	0	Low	P50 I/O port data
FF35H	D3	**IOC53**	R/W	0	1	Output	0	Input	P53 I/O control register
	D2	**IOC52**	R/W	0	1	Output	0	Input	P52 I/O control register
	D1	**IOC51**	R/W	0	1	Output	0	Input	P51 I/O control register
	D0	**IOC50**	R/W	0	1	Output	0	Input	P50 I/O control register
FF36H	D3	**PUL53**	R/W	1	1	Enable	0	Disable	P53 pull-down control register
	D2	**PUL52**	R/W	1	1	Enable	0	Disable	P52 pull-down control register
	D1	**PUL51**	R/W	1	1	Enable	0	Disable	P51 pull-down control register
	D0	**PUL50**	R/W	1	1	Enable	0	Disable	P50 pull-down control register
FF3CH	D3	**SIP03**	R/W	0	1	Enable	0	Disable	P03 (KEY03) interrupt select register
	D2	**SIP02**	R/W	0	1	Enable	0	Disable	P02 (KEY02) interrupt select register
	D1	**SIP01**	R/W	0	1	Enable	0	Disable	P01 (KEY01) interrupt select register
	D0	**SIP00**	R/W	0	1	Enable	0	Disable	P00 (KEY00) interrupt select register
FF3DH	D3	**PCP03**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P03 (KEY03) interrupt polarity select register
	D2	**PCP02**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P02 (KEY02) interrupt polarity select register
	D1	**PCP01**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P01 (KEY01) interrupt polarity select register
	D0	**PCP00**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P00 (KEY00) interrupt polarity select register

Address		Register name	R/W	Default	Setting/data				Function
FF3EH (*6)	D3	**SIP13**	R/W	0	1	Enable	0	Disable	P13(KEY13) interrupt select register
	D2	**SIP12**	R/W	0	1	Enable	0	Disable	P12(KEY12) interrupt select register
	D1	**SIP11**	R/W	0	1	Enable	0	Disable	P11(KEY11) interrupt select register
	D0	**SIP10**	R/W	0	1	Enable	0	Disable	P10(KEY10) interrupt select register
FF3FH (*6)	D3	**PCP13**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P13(KEY13) interrupt polarity select register
	D2	**PCP12**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P12(KEY12) interrupt polarity select register
	D1	**PCP11**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P11(KEY11) interrupt polarity select register
	D0	**PCP10**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P10(KEY10) interrupt polarity select register

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

P0[3:0]: P0 I/O port data register (FF20H)
P1[3:0]: P1 I/O port data register (FF24H)
P2[3:0]: P2 I/O port data register (FF28H)
P3[3:0]: P3 I/O port data register (FF2CH) – S1C63004/008/016
P4[3:0]: P4 I/O port data register (FF30H) – S1C63008/016
P5[3:0]: P5 I/O port data register (FF34H)

I/O port data can be read and output data can be set through these registers.

When writing data

When "1" is written: High level
When "0" is written: Low level

When an I/O port is placed into output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}). Port data can be written also in the input mode.

When reading data

When "1" is read: High level
When "0" is read: Low level

When the I/O port is placed into input mode, the voltage level being input to the port terminal can be read out. When the terminal voltage is high (V_{DD}), the port data that can be read is "1," and when the terminal voltage is low (V_{SS}) the read data is "0." When the pull-down resistor option has been selected and the PULxx register is set to "1," the built-in pull-down resistor goes on during input mode, so that the I/O port terminal is pulled down. When the I/O port is placed into output mode, the register value is read. Therefore, when using the data register of a port that is not used for signal input/output as a general-purpose register, set the port to output mode.

At initial reset, these registers are set to "1."

The data register of the port, which is set for an input/output of the serial interface or R/F converter or a special output, becomes a general-purpose register that does not affect the input/output status.

Note: When I/O ports set in input mode is changed from high to low by the pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 15 pF + parasitic capacitance ? pF
R: pull-down resistance 500 kΩ (Max.)

IOC0[3:0]: P0 port I/O control register (FF21H)
IOC1[3:0]: P1 port I/O control register (FF25H)
IOC2[3:0]: P2 port I/O control register (FF29H)
IOC3[3:0]: P3 port I/O control register (FF2DH) – S1C63004/008/016
IOC4[3:0]: P4 port I/O control register (FF31H) – S1C63008/016
IOC5[3:0]: P5 port I/O control register (FF35H)

Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input/output mode of the I/O ports are set in 1-bit units. Writing "1" to the I/O control register places the corresponding I/O port into output mode, and writing "0" sets input mode. At initial reset, these registers are all set to "0," so the I/O ports are placed in input mode.

The I/O control register of the port, which is set for an input/output of the serial interface or R/F converter or a special output, are ineffective.

PUL0[3:0]: P0 port pull-down control register (FF22H)
PUL1[3:0]: P1 port pull-down control register (FF26H)
PUL2[3:0]: P2 port pull-down control register (FF2AH)
PUL3[3:0]: P3 port pull-down control register (FF2EH) – S1C63004/008/016
PUL4[3:0]: P4 port pull-down control register (FF32H) – S1C63008/016
PUL5[3:0]: P5 port pull-down control register (FF36H)

Enables the pull-down during input mode.

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

These registers enable the built-in pull-down resistor to be effective during input mode in 1-bit units. (The pull-down resistor is included into the ports selected by mask option.)
By writing "1" to the pull-down control register, the corresponding I/O ports are pulled down during input mode, while writing "0" or output mode disables the pull-down function. At initial reset, these registers are all set to "1," so the pull-down function is enabled.

The pull-down control register of the port in which the pull-down resistor is not included becomes a general-purpose register. The register of the port that is set as output for the serial interface, input/output for the R/F converter or a special output can also be used as a general-purpose register that does not affect the pull-down control. The pull-down control register of the port that is set as input for the serial interface functions the same as the I/O port.

SMT0[3:0]: P0 port input interface level select register (FF23H)
SMT1[3:0]: P1 port input interface level select register (FF27H)

Selects an input interface level.

When "1" is written: CMOS Schmitt level
When "0" is written: CMOS level
Reading: Valid

These registers select the input interface level of the P0 and P1 I/O ports in 1-bit units. When "1" is written to SMTxx, the corresponding I/O port Pxx is configured with a CMOS Schmitt level input interface. When "0" is written, the port is configured with a CMOS level input interface. At initial reset, these registers are set to "1."
The input interface level of the P2 to P5 ports are fixed at a CMOS Schmitt level.

SIP0[3:0]: P0 port interrupt select register (FF3CH)
SIP1[3:0]: P1 port interrupt select register (FF3EH) – S1C63004/008/016

Selects the ports used for the key input interrupt from P00–P03 and P10–P13.

When "1" is written: Interrupt enable
When "0" is written: Interrupt disable
Reading: Valid

By writing "1" to an interrupt select register (SIP0[3:0], SIP1[3:0]), the corresponding I/O port (P00–P03, P10–P13) is enabled to generate interrupts. When "0" is written, the I/O port does not affect the interrupt generation.
Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction.
At initial reset, these registers are set to "0."

PCP0[3:0]: P0 port interrupt polarity select register (FF3DH)
PCP1[3:0]: P1 port interrupt polarity select register (FF3FH) – S1C63004/008/016

Sets the interrupt conditions.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

When "1" is written to an interrupt polarity select register (PCP0[3:0], PCP1[3:0]), the corresponding I/O port (P00–P03, P10–P13) generates an interrupt at the falling edge of the input signal. When "0" is written, the I/O port generates an interrupt at the rising edge of the input signal. At initial reset, these registers are set to "1."

NRSP0[1:0]: Key input interrupt 0–3 noise reject frequency select register (FF11H•D[1:0])
NRSP1[1:0]: Key input interrupt 4–7 noise reject frequency select register (FF11H•D[3:2])*

* **S1C63004/008/016**

Selects the noise reject frequency for the key input interrupts.

Table 12.7.2 Setting up noise rejector

NRSP0[1:0]/NRSP1[1:0]	Noise reject frequency	Reject pulse width
3	f_{OSC1} / 256 (128 Hz)	7.8 msec
2	f_{OSC1} / 64 (512 Hz)	2.0 msec
1	f_{OSC1} / 16 (2 kHz)	0.5 msec
0	Off (bypassed)	–

NRSP0[1:0] and NRSP1[1:0] are the noise reject frequency select registers that correspond to the key input interrupts 0–3 (P00–P03) and the key input interrupts 4–7 (P10–P13), respectively. At initial reset, these registers are set to "0."

12.8 Precautions

- When an I/O ports in input mode is changed from high to low by the pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
  Particular care needs to be taken of the key scan during key matrix configuration.
  Make this waiting time the amount of time or more calculated by the following expression.
  $10 \times C \times R$
  C: terminal capacitance 15 pF + parasitic capacitance ? pF
  R: pull-down resistance 500 kΩ (Max.)
- Be sure to turn the noise rejector off before executing the SLP instruction.

- Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the key input interrupt using the corresponding interrupt mask register (EIKxx = "1") before executing the SLP instruction to run key input interrupt handler routine after SLEEP status is released.
- Before the port function is configured, the circuit that uses the port (e.g. input interrupt, multiple key entry reset, serial interface, R/F converter, event counter input, direct RUN/LAP input for stopwatch) must be disabled.

13 Serial Interface [S1C63004/008/016]

Note: The S1C63003 has no serial interface included.

13.1 Configuration of Serial Interface

The S1C63004/008/016 has a built-in 8-bit clock synchronous type serial interface. The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal. The synchronous clock for serial data input/output may be set by software any one of seven types of master mode (internal clock mode: when the S1C63004/008/016 is to be the master for serial input/output) and one type of slave mode (external clock mode: when the S1C63004/008/016 is to be the slave for serial input/output).
The configuration of the serial interface is shown in Figure 13.1.1.

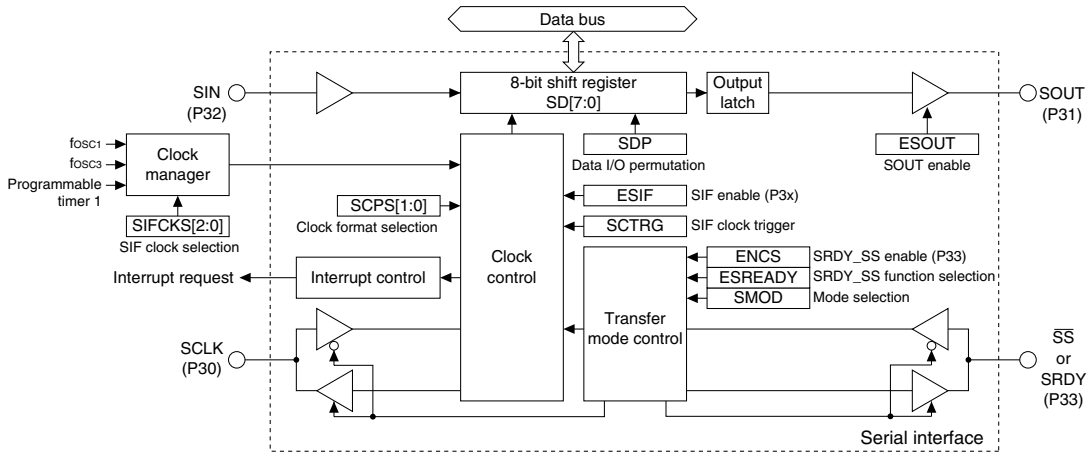


Figure 13.1.1 Configuration of serial interface

13.2 Serial Interface Terminals

The following shows the terminals used in the serial interface and their functions:

SCLK (P30)

Inputs or outputs the serial clock. By writing "1" to the ESIF register to enable the serial interface, the P30 terminal is switched to the SCLK terminal. In master mode, the SCLK terminal is configured for output and it outputs the synchronous clock generated in the IC during data transfer. In slave mode, the SCLK terminal inputs the synchronous clock output by the external master device.

SIN (P32)

Inputs serial data. By writing "1" to the ESIF register to enable the serial interface, the P32 terminal is switched to the SIN terminal.

SOUT (P31)

Outputs serial data. By default, the SOUT terminal is not enabled even if "1" is written to the ESIF register. When using the SOUT output, write "1" to the ESOUT register.
If serial input only is required, the P31 terminal can be used as an I/O port terminal.

SRDY (P33)

In slave mode, this terminal outputs the SRDY signal to the master device to indicate that the serial interface is ready to transfer. By default, the SRDY terminal is not enabled even if the serial interface is set to slave mode. When using the SRDY output in slave mode, write "1" to the ENCS and ESREADY registers.

$\overline{SS}$ (P33)

Inputs the $\overline{SS}$ (Slave Select) signal when the S1C63004/008/016 is used as an SPI slave device. When using the $\overline{SS}$ input, write "1" to ENCS and write "0" to ESREADY.

The serial interface input/output ports are shared with the I/O port (P30–P33), and they are configured to the I/O port terminals at initial reset. When using these terminals for the serial interface, switch the function with software as described above. At least ESIF must be set to 1.
The switch operation automatically sets the input/output direction of the terminals. It is not necessary to set the I/O port control registers. The I/O control registers and data registers of the I/O ports are ineffective. However, the pull-up control registers of the I/O ports are effective when they are used for the serial inputs.

13.3 Mask Option

Since the input/output terminals of the serial interface are shared with the I/O ports (P30–P33), the mask option that selects the terminal specification for the I/O port is also applied to the serial interface terminals.

Output specification

The output specification of the SOUT, SCLK (in master mode) and SRDY (in slave mode) terminals that are used as the serial interface outputs is respectively selected by the mask options for P31, P30 and P33. Either complementary output or P-channel open drain output can be selected as the output specification. However, when P-channel open drain output is selected, do not apply voltage exceeding the power supply voltage to the terminal.

Pull-down resistor

The pull-down resistors for the SIN, SCLK (in slave mode) and $\overline{SS}$ (in SPI slave mode) terminals that are used as inputs can be incorporated by the mask options for P32, P30 and P33. When the pull-down resistor is not used, take care that a floating status does not occur.

Pull-down control when pull-down resistor is incorporated

When a pull-down resistor is incorporated at the serial input terminal, the pull-down resistor should be enabled/disabled using the pull-down control register of the I/O port.

SIN terminal: PUL32 register
SCLK terminal: PUL30 register
$\overline{SS}$ terminal: PUL33 register

Refer to the "I/O Ports" chapter for controlling the pull-down resistors.

13.4 Operating Mode of Serial Interface

The serial interface supports three operating modes: master mode, slave mode and SPI slave mode.

Master mode

Master mode is provided to use the S1C63004/008/016 as the master device for serial transfer. In this mode, the serial interface uses the internal clock supplied from the clock manager as the synchronous clock for serial transfer. The synchronous clock is also output from the SCLK terminal to the slave device. The ready signal sent from the slave device should be input through an I/O port (in input mode) and it should be read with software to control data transfer.
The S1C63004/008/016 set to master mode is also used as an SPI master device. The $\overline{SS}$ (Slave Select) signal should be output by controlling an I/O port (in output mode) with software.

Slave mode

Slave mode is provided to use the S1C63004/008/016 as a slave device for serial transfer. In this mode, the serial interface inputs the synchronous clock that is sent by the external master device from the SCLK terminal to perform serial transfer. For the external master device to control data transfer, the serial interface can output a ready signal indicating that it is ready to transfer from the SRDY terminal by hardware control.

SPI slave mode

SPI slave mode is provided to use the S1C63004/008/016 as an SPI slave device. In this mode, the serial interface inputs the synchronous clock that is sent by the external master device from the SCLK terminal to perform serial transfer. The SPI master device outputs the $\overline{SS}$ (Slave Select) signal to select a slave device. SPI slave mode supports the $\overline{SS}$ signal input.

Sample basic serial connection diagrams are shown in Figure 13.4.1.

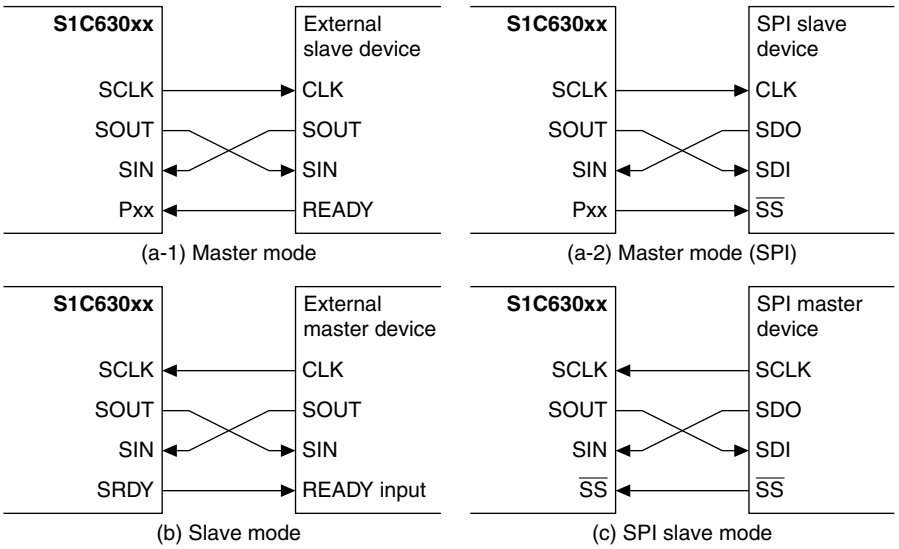


Figure 13.4.1 Sample basic connection of serial input/output terminals

The SMOD, ENCS and ESREADY registers are used for setting the mode.

Master mode: SMOD = "1," ENCS = "0," ESREADY = "0"
Slave mode: SMOD = "0," ENCS = "1," ESREADY = "1"
SPI slave mode: SMOD = "0," ENCS = "1," ESREADY = "0"

Table 13.4.1 lists the combination of mode settings and used terminal configurations.

Table 13.4.1 Mode settings and configurations of serial interface terminals

ESIF	SMOD	ENCS	ESREADY	ESOUT	Mode	P30 terminal	P31 terminal	P32 terminal	P33 terminal
1	1	1	1	*	Master mode	Prohibited			
1	1	*	0	1		SCLK (O)	SOUT (O)	SIN (I)	P33 (I/O)
1	1	0	1	1		SCLK (O)	SOUT (O)	SIN (I)	P33 (I/O)
1	1	*	0	0		SCLK (O)	P31 (I/O)	SIN (I)	P33 (I/O)
1	1	0	1	0		SCLK (O)	P31 (I/O)	SIN (I)	P33 (I/O)
1	0	1	1	1	Slave mode	SCLK (I)	SOUT (O)	SIN (I)	SRDY (O)
1	0	1	1	0		SCLK (I)	P31 (I/O)	SIN (I)	SRDY (O)
1	0	0	*	1		SCLK (I)	SOUT (O)	SIN (I)	P33 (I/O)
1	0	0	*	0		SCLK (I)	P31 (I/O)	SIN (I)	P33 (I/O)
1	0	1	0	1	SPI slave mode	SCLK (I)	SOUT (O)	SIN (I)	$\overline{SS}$ (I)
1	0	1	0	0		SCLK (I)	P31 (I/O)	SIN (I)	$\overline{SS}$ (I)
0	*	*	*	*	Serial I/F not used	P30 (I/O)	P31 (I/O)	P32 (I/O)	P33 (I/O)

13.5 Setting Synchronous Clock

13.5.1 Selecting Source Clock

When the serial interface is used in master mode, it uses the internal clock supplied from the clock manager as the synchronous clock for data transfer. The clock manager generates six serial interface clocks by dividing the OSC1 or OSC3 clock. The synchronous clock used in master mode can be selected from seven types (the above six clocks and the programmable timer 1 output clock). Use the SIFCKS[2:0] register to select one of them as shown in Table 13.5.1.1.

Table 13.5.1.1 Serial interface clock frequencies

SIFCKS[2:0]	SIF clock (master mode)
7	fOSC3 / 4 *
6	fOSC3 / 2 *
5	fOSC3 / 1 *
4	Programmable timer 1 *
3	fOSC1 / 4 (8 kHz)
2	fOSC1 / 2 (16 kHz)
1	fOSC1 / 1 (32 kHz)
0	Off (slave mode) *

fOSC1: OSC1 oscillation frequency. ( ) indicates the frequency when fOSC1 = 32 kHz.
fOSC3: OSC3 oscillation frequency
* The maximum clock frequency is limited to 1 MHz.

When programmable timer 1 is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to the "Programmable Timer" chapter for controlling the programmable timer.
Fix SIFCKS[2:0] at "0" in slave mode.
At initial reset, "Off (slave mode)" is selected.

13.5.2 Selecting Synchronous Clock Format

The format (polarity and phase) of the synchronous clock for the serial interface can be configured using the SCPS[1:0] register.

Table 13.5.2.1 Configuration of synchronous clock format

SCPS[1:0]	Polarity	Phase
3	Negative (SCLK)	Rising edge (↑)
2	Negative (SCLK)	Falling edge (↓)
1	Positive (SCLK)	Falling edge (↓)
0	Positive (SCLK)	Rising edge (↑)

At initial reset, the clock polarity is set to positive and the phase is set to the rising edge.
See Figure 13.6.5.1 for the data transfer timings by the synchronous clock format selected.

13.6 Data Input/Output and Interrupt Function

The serial interface of S1C63004/008/016 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the SCLK (P30) terminal (master mode), or the synchronous clock input to the SCLK (P30) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock SCLK; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

13.6.1 Serial Data Output Procedure and Interrupt

The S1C63004/008/016 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to the data registers SD[3:0] and SD[7:4], and writing "1" to SCTRG, it synchronizes with the synchronous clock and the serial data is output to the SOUT (P31) terminal. The synchronous clock used here is as follows: in master mode, internal clock which is output to the SCLK (P30) terminal while in slave mode, external clock which is input from the SCLK (P30) terminal.
Shift timing of serial data is as follows:

• When positive polarity (SCPS1 = "0") is selected for the synchronous clock:
The serial data output to the SOUT (P31) terminal changes at the rising edge of the clock input or output from/to the SCLK (P30) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1."

• When negative polarity (SCPS1 = "1") is selected for the synchronous clock:
The serial data output to the SOUT (P31) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P30) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "1."

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

13.6.2 Serial Data Input Procedure and Interrupt

The S1C63004/008/016 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. The serial data is input from the SIN (P32) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. The synchronous clock used here is the internal clock in master mode or the external clock in slave mode.
Shift timing of serial data is as follows:

• When positive polarity (SCPS1 = "0") is selected for the synchronous clock:
The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1." The shift register is sequentially shifted as the data is fetched.

• When negative polarity (SCPS1 = "1") is selected for the synchronous clock:
The serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "1." The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD[7:0] by software.

13.6.3 Serial Data Input/Output Permutation

The S1C63004/008/016 allows the input/output permutation of serial data to be selected by the SDP register as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 13.6.3.1. The SDP register should be set before setting data to SD[7:0].

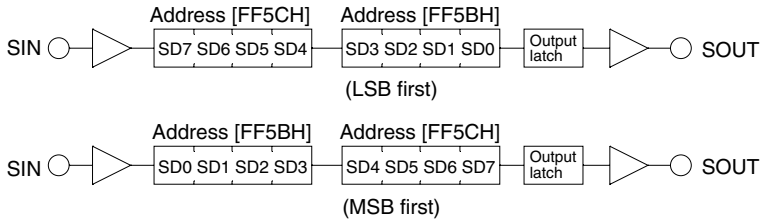


Figure 13.6.3.1 Serial data input/output permutation

13.6.4 SRDY Signal

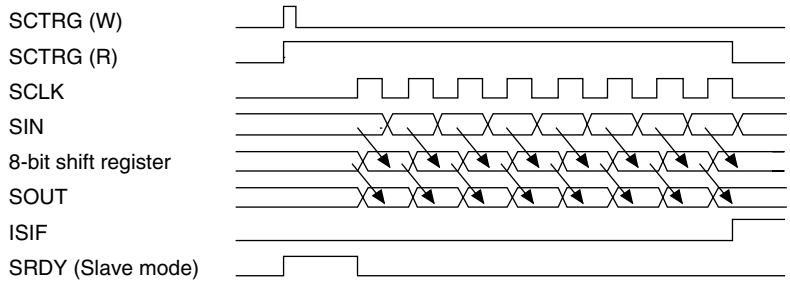
When the S1C63004/008/016 serial interface is used in the slave mode, the SRDY signal is used to indicate whether the internal serial interface is ready to transmit or receive data for the master side (external) serial device. The SRDY signal is output from the SRDY (P33) terminal. When using the SRDY output in slave mode, write "1" to the ENCS and ESREADY registers (this signal cannot be used in SPI slave mode).
Output timing of SRDY signal is as follows:

- **When positive polarity (SCPS1 = "0") is selected for the synchronous clock:**
  The SRDY signal goes "1" (high) when the S1C63004/008/016 serial interface is ready to transmit or receive data; normally, it is at "0" (low).
  The SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P30) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD[7:4], the SRDY signal returns to "0."

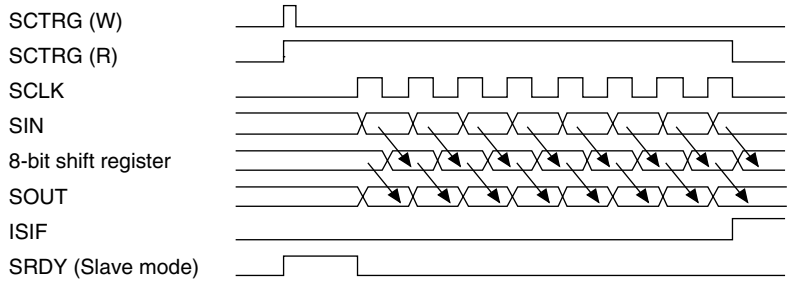
- **When negative polarity (SCPS1 = "1") is selected for the synchronous clock:**
  The $\overline{\text{SRDY}}$ signal goes "0" (low) when the S1C63004/008/016 serial interface is ready to transmit or receive data; normally, it is at "1" (high).
  The $\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P30) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD[7:4], the $\overline{\text{SRDY}}$ signal returns to "1."

13.6.5 Timing Chart

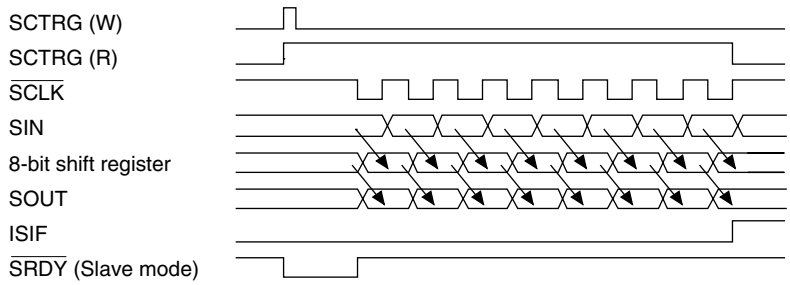
The S1C63004/008/016 serial interface timing charts are shown in Figure 13.6.5.1.



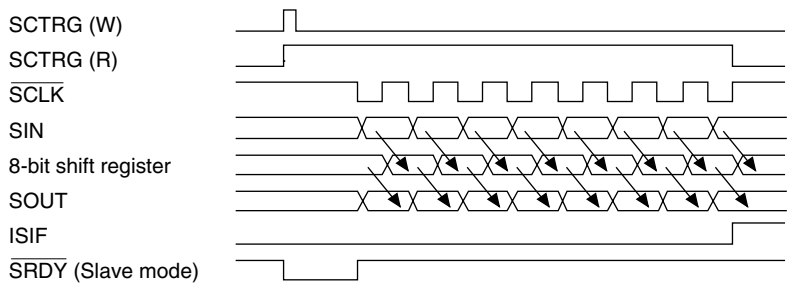
(a) When SCPS1 = "0" and SCPS0="0"



(b) When SCPS1 = "0" and SCPS0 = "1"



(c) When SCPS1 = "1" and SCPS0 = "0"



(d) When SCPS1 = "1" and SCPS0 = "1"

Figure 13.6.5.1 Serial interface timing chart

13.7 Data Transfer in SPI Mode

The serial interface supports serial data transfer in SPI mode.
This mode has the same serial master and slave functions and control method except that the SRDY output cannot be used when P33 is configured to the $\overline{SS}$ terminal. Refer to Section 13.4, "Operating mode of serial interface," and Section 13.6, "Data input/output and interrupt function," for these common descriptions.

SPI slave device

When using the S1C63004/008/016 as an SPI slave device, set the serial interface to SPI slave mode.

ESIF = "1," SMOD = "0," ENCS = "1," ESREADY = "0," ESOUT = "1" (when SOUT is used)

The P33 terminal functions as the $\overline{SS}$ (Slave Select) signal input terminal.
To perform data transfer in this mode, write "1" to SCTRG to enable the serial interface to transmit/receive data the same as the slave mode described above. The serial interface starts data transfer when the external master device outputs the synchronous clock to the SCLK terminal after it asserts the slave select signal (set to low) input to the $\overline{SS}$ (P33) terminal. The external device must hold the $\overline{SS}$ signal (P33 terminal) active while data is being transferred. When the $\overline{SS}$ signal is inactive, the serial interface does not start data transfer even if the synchronous clock is input to the SCLK terminal.

SPI master device

When using the S1C63004/008/016 as an SPI master device, set the serial interface to master mode.

ESIF = "1," SMOD = "1," ENCS = "0," ESREADY = "0," ESOUT = "1" (when SOUT is used)

The $\overline{SS}$ signal output terminal is not available in master mode, set an I/O port to output mode and use it as the $\overline{SS}$ signal output terminal. The $\overline{SS}$ signal must be set to low before writing "1" to SCTRG and hold that active level while data is being transferred. After 8-bit data is transmitted/received, set the $\overline{SS}$ signal to high.

Timing chart

The data transfer timing chart in SPI mode is shown in Figure 13.7.1.

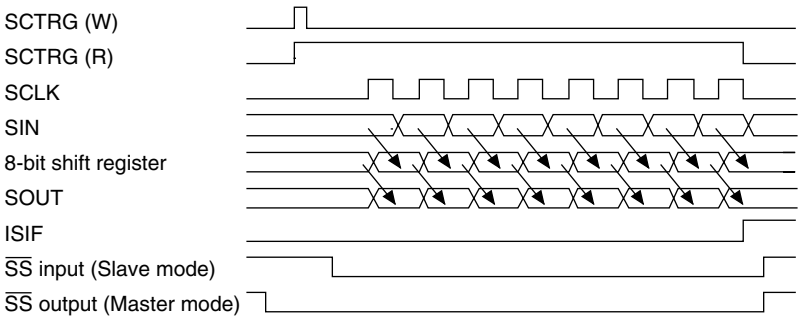


Figure 13.7.1 Timing chart in SPI mode (when SCPS1 = SCPS0 = "0")

Notes:
- The S1C63004/008/016 serial interface does not have a transmit buffer and a receive buffer, therefore, data transfer must be processed in every one-byte transfer. The interrupt factor flag is set after a transfer for one byte has been completed. A start of data transfer from/to the SPI device cannot be used as a trigger to start the interrupt handler.
- If the $\overline{SS}$ signal becomes inactive during data transfer in SPI slave mode or if the master device outputs the SCLK signal before it asserts the $\overline{SS}$ signal, the serial interface cannot transmit/receive data normally.

13.8 I/O Memory of Serial Interface

Table 13.8.1 shows the I/O addresses and the control bits for the serial interface.

Table 13.8.1 Control bits of serial interface

Address		Register name	R/W	Default	Setting/data	Function
FF14H	D3	0 (*3)	R	– (*2)	–	Unused
(*6)	D2	**SIFCKS2**	R/W	0	7 f3/4 4 PT1 1 f1	Serial I/F clock frequency selection
	D1	**SIFCKS1**	R/W	0	6 f3/2 3 f1/4 0 Off/	(f1 = fosc1, f3 = fosc3)
	D0	**SIFCKS0**	R/W	0	5 f3 2 f1/2 External	
FF58H	D3	0 (*3)	R	– (*2)	–	Unused
(*6)	D2	**ESOUT**	R/W	0	1 Enable 0 Disable	SOUT enable
	D1	**SCTRG**	R/W	0	1 Trigger (W) 0 Invalid (W)	Serial I/F clock trigger (writing)
					Run (R) Stop (R)	Serial I/F clock status (reading)
	D0	**ESIF**	R/W	0	1 SIF 0 I/O	Serial I/F enable (P3 port function selection)
FF59H	D3	**SCPS1**	R/W	0	3 Negative, ↑ 1 Positive, ↓	Serial I/F clock format selection
(*6)	D2	**SCPS0**	R/W	0	2 Negative, ↓ 0 Positive, ↑	(polarity, phase)
	D1	**SDP**	R/W	0	1 MSB first 0 LSB first	Serial I/F data input/output permutation
	D0	**SMOD**	R/W	0	1 Master 0 Slave	Serial I/F mode selection
FF5AH	D3	0 (*3)	R	– (*2)	–	Unused
(*6)	D2	0 (*3)	R	– (*2)	–	Unused
	D1	**ESREADY**	R/W	0	1 SRDY 0 $\overline{SS}$	SRDY_SS function selection (ENCS = "1")
	D0	**ENCS**	R/W	0	1 SRDY_SS 0 P33	SRDY_SS enable (P33 port function selection)
FF5BH	D3	**SD3**	R/W	×	0H–FH	Serial I/F transmit/receive data
(*6)	D2	**SD2**	R/W	×		(low-order 4 bits)
	D1	**SD1**	R/W	×		SD0 = LSB
	D0	**SD0**	R/W	×		
FF5CH	D3	**SD7**	R/W	×	0H–FH	Serial I/F transmit/receive data
(*6)	D2	**SD6**	R/W	×		(high-order 4 bits)
	D1	**SD5**	R/W	×		SD7 = MSB
	D0	**SD4**	R/W	×		

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

SIFCKS[2:0]: Serial interface clock frequency select register (FF14H•D[2:0])

Selects the synchronous clock frequency in master mode.

Table 13.8.2 Serial interface clock frequencies

SIFCKS[2:0]	SIF clock (master mode)
7	fosc3 / 4 *
6	fosc3 / 2 *
5	fosc3 / 1 *
4	Programmable timer 1 *
3	fosc1 / 4 (8 kHz)
2	fosc1 / 2 (16 kHz)
1	fosc1 / 1 (32 kHz)
0	Off (slave mode) *

fosc1: OSC1 oscillation frequency. ( ) indicates the frequency when fosc1 = 32 kHz.
fosc3: OSC3 oscillation frequency
* The maximum clock frequency is limited to 1 MHz.

When programmable timer 1 is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to the "Programmable Timer" chapter for controlling the programmable timer.
Fix at "0" in slave mode.
At initial reset, this register is set to "0."

ESIF: Serial interface enable register (P3 port function selection) (FF58H•D0)

Sets P30–P33 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P30, P31, P32 and P33 function as SIN, SOUT, SCLK and SRDY or $\overline{SS}$, respectively. In slave mode, the P33 terminal functions as SRDY output or $\overline{SS}$ input terminal, while in master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0."

SCTRG: Clock trigger/status (FF58H•D1)

This is a trigger to start input/output of synchronous clock (SCLK).

When writing

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started. As a trigger condition, it is required that data writing or reading on data registers SD[7:0] be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD[7:0].) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger. Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

When reading

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)

When this bit is read, it indicates the status of serial interface clock. After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation. When the synchronous clock input/output is completed, this latch is reset to "0."

At initial reset, this bit is set to "0."

ESOUT: SOUT enable register (FF58H•D2)

Enables serial data output from the P31 port.

When "1" is written: Enabled (SOUT)
When "0" is written: Disabled (I/O port)
Reading: Valid

When serial data output is not used, the SOUT output can be disabled to use P31 as an I/O port. When performing serial output, write "1" to ESOUT to set P31 as the SOUT output port. At initial reset, this register is set to "0."

SMOD: Operating mode select register (FF59H•D0)

Selects the serial interface operating mode from master mode and slave mode.

When "1" is written: Master mode
When "0" is written: Slave mode
Reading: Valid

In master mode, the serial interface uses the internal clock (selected in the clock manager) as the synchronous clock for serial transfer. The synchronous clock is also output from the SCLK (P30) terminal to control the external serial interface (slave device). In slave mode, the serial interface inputs the synchronous clock that is sent by the external serial interface (master device) from the SCLK terminal to perform serial transfer. Master mode is selected by writing "1" to SMOD, and slave mode is selected by writing "0."
At initial reset, this register is set to "0."

SDP: Data input/output permutation select register (FF59H•D1)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first. At initial reset, this register is set to "0."

SCPS[1:0]: Clock format select register (FF59H•D[3:2])

Selects the timing for reading in the serial data input from the SIN (P32) terminal.

Table 13.8.3 Configuration of synchronous clock format

SCPS[1:0]	Polarity	Phase
3	Negative ($\overline{\text{SCLK}}$)	Rising edge (↑)
2	Negative ($\overline{\text{SCLK}}$)	Falling edge (↓)
1	Positive (SCLK)	Falling edge (↓)
0	Positive (SCLK)	Rising edge (↑)

• When positive polarity (SCPS1 = "0") is selected for the synchronous clock:

During receiving, the serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1." The shift register is sequentially shifted as the data is fetched.
During transmitting, the serial data output to the SOUT (P31) terminal changes at the rising edge of the clock input or output from/to the SCLK (P30) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS0 register is "0" or at the falling edge of the SCLK signal when the SCPS0 register is "1."

• When negative polarity (SCPS1 = "1") is selected for the synchronous clock:

During receiving, the serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "1." The shift register is sequentially shifted as the data is fetched.

During transmitting, the serial data output to the SOUT (P31) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P30) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "0" or at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS0 register is "1."

At initial reset, this register is set to "0."

ENCS: SRDY_SS enable register (P33 port function selection) (FF5AH•D0)

Enables the serial interface function of P33. Use this register with ESREADY.

When "1" is written: Enabled (Serial interface)
When "0" is written: Disabled (I/O port)
Reading: Valid

When ENCS is enabled, the P33 terminal can be used as SRDY output or $\overline{\text{SS}}$ input terminal in slave mode (SMOD = "0"). At initial reset, this register is set to "0."

ESREADY: SRDY_SS function select register (FF5AH•D1)

Selects the P33 port function when ENCS = "1."

When "1" is written: SRDY output
When "0" is written: $\overline{\text{SS}}$ input
Reading: Valid

The P33 port function can be selected from SRDY output and $\overline{\text{SS}}$ input in slave mode (SMOD = "0"). At initial reset, this register is set to "0."

Table 13.8.4 Selecting P33 port function

Slave mode: SMOD="0"

ESREADY	ENCS	P33 terminal
*	0	P33 (I/O)
0	1	$\overline{SS}$ (I)
1	1	SRDY (O)

Master mode: SMOD="1"

ESREADY	ENCS	P33 terminal
*	0	P33 (I/O)
0	1	P33 (I/O)
1	1	Prohibited

SD[7:0]: Serial interface data register (FF5CH, FF5BH)

These registers are used for writing and reading serial data.

When writing

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P31) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

When reading

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P32) terminal can be read from these registers. The serial data input from the SIN (P32) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0," and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output). At initial reset, these registers are undefined.

13.9 Precautions

- Perform data writing/reading to the data registers SD[7:0] only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).
- As a trigger condition, it is required that data writing or reading on data registers SD[7:0] be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD[7:0].) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
  Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.
- Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD[7:0].
- Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when the programmable timer is used as the clock source or the serial interface is used in slave mode.

14 LCD Driver

14.1 Configuration of LCD Driver

The S1C63003/004/008/016 LCD output configuration is shown in the table below.

Table 14.1.1 LCD outputs

Model	Common terminals	Segment terminals	Maximum number of dots
S1C63016	8 terminals (COM0–COM7)	56 terminals (SEG0–SEG55)	448 dots (56 × 8)
S1C63008	8 terminals (COM0–COM7)	50 terminals (SEG0–SEG29, SEG36–SEG55)	400 dots (50 × 8)
S1C63004	8 terminals (COM0–COM7)	36 terminals (SEG0–SEG19, SEG40–SEG55)	288 dots (36 × 8)
S1C63003	5 terminals (COM0–COM4)	22 terminals (SEG0–SEG9, SEG44–SEG55)	110 dots (22 × 5)

The driving method is 1/3, 1/4, 1/5, 1/6, 1/7 or 1/8 duty dynamic drive (1/3, 1/4 or 1/5 duty dynamic drive in the S1C63003) with three drive voltages (1/3 bias), V_{C1}, V_{C2} and V_{C3}. LCD display can be controlled (turned on and off) by software.

14.2 Mask Option

14.2.1 SEG/GPIO/RFC Terminal Configuration

The SEG0 to SEG35 terminals of the S1C63016, the SEG0 to SEG29 terminals of the S1C63008, the SEG0 to SEG19 terminals of the S1C63004, and the SEG0 to SEG9 terminals of the S1C63003 are fixed at segment/DC outputs.
The SEG36 to SEG55 terminals of the S1C63008/016, the SEG40 to SEG55 terminals of the S1C63004, and the SEG44 to SEG55 terminals of the S1C63003 are shared with I/O port or R/F converter, and each terminal can be set to the function to be used by mask option.

Table 14.2.1.1 SEG/GPIO/RFC terminal configuration option

Function 1 (GPIO/RFC terminal)	Function 2 (SEG terminal)	S1C63xxx			
		016	008	004	003
P40	SEG36	○	○	–	–
P41	SEG37	○	○	–	–
P42	SEG38	○	○	–	–
P43	SEG39	○	○	–	–
P30/SCLK	SEG40	○	○	○	–
P31/SOUT	SEG41	○	○	○	–
P32/SIN	SEG42	○	○	○	–
P33/SRDY_SS	SEG43	○	○	○	–
P20	SEG44	○	○	○	○
P21	SEG45	○	○	○	○
P22/EVIN_B*	SEG46	○	○	○	○
P23/TOUT_B*	SEG47	○	○	○	○
P50/RFOUT	SEG48	○	○	○	○
P51/SEN0	SEG49	○	○	○	○
P52/REF0	SEG50	○	○	○	○
P53/RFIN0	SEG51	○	○	○	○
RFIN1	SEG52	○	○	○	○
REF1	SEG53	○	○	○	○
SEN1	SEG54	○	○	○	○
HUD	SEG55	○	○	○	○

* EVIN_B and TOUT_B are not available in the S1C63003.

14.2.2 Power Source for LCD Driving

The power source for driving LCD can be selected from the internal power supply and an external power supply.

When the internal power supply is selected, the internal LCD system voltage regulator is enabled to generate the LCD drive voltages V_{C1}–V_{C3}. The LCD system voltage regulator starts operating and outputs the LCD drive voltages V_{C1}–V_{C3} to the LCD driver when the LPWR register is set to "1."
The LCD system voltage regulator generates the reference voltage V_{C1} or V_{C2} and generates two other voltages ($V_{C2} = V_{C1} \times 2$, $V_{C3} = V_{C1} \times 3$, or $V_{C1} = V_{C2} \times 1/2$, $V_{C3} = V_{C2} \times 3/2$) by boosting or reducing V_{C1}/V_{C2}.
When the internal power supply is used in the S1C63003, the reference voltage (V_{C1} or V_{C2}) should be selected according to the supply voltage V_{DD} by mask option.
1. Internal power supply (V_{C2} reference) 1/3 bias (for 3.0 V panel)
2. Internal power supply (V_{C1} reference) 1/3 bias (for 3.0 V panel)

In the S1C63004/008/016, the reference voltage can be selected using use the VCREF register.
For more information on the LCD system voltage regulator, refer to the "Power Supply" chapter.

When using an external power supply, select a drive voltage configuration from the following 3 types and supply the LCD drive voltage to the V_{C1}–V_{C3} terminals.
1. External power supply 1/3 bias (for 4.5 V panel) $V_{DD} = V_{C2}$
2. External power supply 1/3 bias (for 3.0 V panel) $V_{DD} = V_{C3}$
3. External power supply 1/2 bias (for 3.0 V panel) $V_{DD} = V_{C3}$, $V_{C1} = V_{C2}$

For the external connection diagram when an external supply is used, refer to the "Power Supply" chapter.
Note that the power control using the LPWR register is necessary even if an external power supply is used.

14.2.3 Segment Option

Segment allocation

Note: Refer to Appendix D, "Mask Data Creation Procedure," for mask data creation including segment allocation and precautions.

The display memory addresses and data bits can be allocated to a segment terminal individually. This makes design easy by increasing the degree of freedom with which the LCD panel can be designed.
Figure 14.2.3.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/4 duty.

Display memory allocation

Address	Data bit			
	D3	D2	D1	D0
F010H	d	c	b	a
F011H	p	g	f	c

Pin address allocation

	COM0	COM1	COM2	COM3
SEG10	11, D1 (f)	11, D0 (e)	10, D2 (c)	10, D3 (d)
SEG11	10, D0 (a)	11, D2 (g)	10, D1 (b)	11, D3 (p)

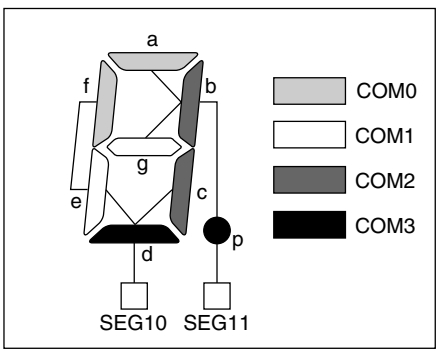


Figure 14.2.3.1 Segment allocation

Output specification

Each of the SEG0 to SEG35 terminals of the S1C63016, the SEG0 to SEG29 terminals of the S1C63008, the SEG0 to SEG19 terminals of the S1C63004, or the SEG0 to SEG9 terminals of the S1C63003 can be configured for either segment signal output or DC output (V_{DD} and V_{SS} binary output) by mask option.
When DC output is selected, either complementary output or N-channel open drain output can be selected as the output specification for each terminal pair. When DC output is selected, the data corresponding to COM0 of each segment terminal is output. DC output can be performed even if the LCD system voltage regulator is off (LPWR = "0").

Other SEG terminals can be used only for segment signal output. DC output cannot be selected.

Table 14.2.3.1 Segment option (S1C63016)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									☐S ☐C ☐N
SEG1																									☐S ☐C ☐N
SEG2																									☐S ☐C ☐N
SEG3																									☐S ☐C ☐N
SEG4																									☐S ☐C ☐N
SEG5																									☐S ☐C ☐N
SEG6																									☐S ☐C ☐N
SEG7																									☐S ☐C ☐N
SEG8																									☐S ☐C ☐N
SEG9																									☐S ☐C ☐N
SEG10																									☐S ☐C ☐N
SEG11																									☐S ☐C ☐N
SEG12																									☐S ☐C ☐N
SEG13																									☐S ☐C ☐N
SEG14																									☐S ☐C ☐N
SEG15																									☐S ☐C ☐N
SEG16																									☐S ☐C ☐N
SEG17																									☐S ☐C ☐N
SEG18																									☐S ☐C ☐N
SEG19																									☐S ☐C ☐N
SEG20																									☐S ☐C ☐N
SEG21																									☐S ☐C ☐N
SEG22																									☐S ☐C ☐N
SEG23																									☐S ☐C ☐N
SEG24																									☐S ☐C ☐N
SEG25																									☐S ☐C ☐N
SEG26																									☐S ☐C ☐N
SEG27																									☐S ☐C ☐N
SEG28																									☐S ☐C ☐N
SEG29																									☐S ☐C ☐N
SEG30																									☐S ☐C ☐N
SEG31																									☐S ☐C ☐N
SEG32																									☐S ☐C ☐N
SEG33																									☐S ☐C ☐N
SEG34																									☐S ☐C ☐N
SEG35																									☐S ☐C ☐N
SEG36																									■S ☐C ☐N
SEG37																									■S ☐C ☐N
SEG38																									■S ☐C ☐N
SEG39																									■S ☐C ☐N
SEG40																									■S ☐C ☐N
SEG41																									■S ☐C ☐N
SEG42																									■S ☐C ☐N
SEG43																									■S ☐C ☐N
SEG44																									■S ☐C ☐N
SEG45																									■S ☐C ☐N
SEG46																									■S ☐C ☐N
SEG47																									■S ☐C ☐N
SEG48																									■S ☐C ☐N
SEG49																									■S ☐C ☐N
SEG50																									■S ☐C ☐N
SEG51																									■S ☐C ☐N
SEG52																									■S ☐C ☐N
SEG53																									■S ☐C ☐N
SEG54																									■S ☐C ☐N
SEG55																									■S ☐C ☐N

<address> H: RAM data high-order address (0–7)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63016)

1. The output specification of SEG0 to SEG35 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG36 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG36 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.

Table 14.2.3.2 Segment option (S1C63008)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									☐S ☐C ☐N
SEG1																									☐S ☐C ☐N
SEG2																									☐S ☐C ☐N
SEG3																									☐S ☐C ☐N
SEG4																									☐S ☐C ☐N
SEG5																									☐S ☐C ☐N
SEG6																									☐S ☐C ☐N
SEG7																									☐S ☐C ☐N
SEG8																									☐S ☐C ☐N
SEG9																									☐S ☐C ☐N
SEG10																									☐S ☐C ☐N
SEG11																									☐S ☐C ☐N
SEG12																									☐S ☐C ☐N
SEG13																									☐S ☐C ☐N
SEG14																									☐S ☐C ☐N
SEG15																									☐S ☐C ☐N
SEG16																									☐S ☐C ☐N
SEG17																									☐S ☐C ☐N
SEG18																									☐S ☐C ☐N
SEG19																									☐S ☐C ☐N
SEG20																									☐S ☐C ☐N
SEG21																									☐S ☐C ☐N
SEG22																									☐S ☐C ☐N
SEG23																									☐S ☐C ☐N
SEG24																									☐S ☐C ☐N
SEG25																									☐S ☐C ☐N
SEG26																									☐S ☐C ☐N
SEG27																									☐S ☐C ☐N
SEG28																									☐S ☐C ☐N
SEG29																									☐S ☐C ☐N
SEG30																									■S ☐C ☐N
SEG31																									■S ☐C ☐N
SEG32																									■S ☐C ☐N
SEG33																									■S ☐C ☐N
SEG34																									■S ☐C ☐N
SEG35																									■S ☐C ☐N
SEG36																									■S ☐C ☐N
SEG37																									■S ☐C ☐N
SEG38																									■S ☐C ☐N
SEG39																									■S ☐C ☐N
SEG40																									■S ☐C ☐N
SEG41																									■S ☐C ☐N
SEG42																									■S ☐C ☐N
SEG43																									■S ☐C ☐N
SEG44																									■S ☐C ☐N
SEG45																									■S ☐C ☐N
SEG46																									■S ☐C ☐N
SEG47																									■S ☐C ☐N
SEG48																									■S ☐C ☐N
SEG49																									■S ☐C ☐N
SEG50																									■S ☐C ☐N
SEG51																									■S ☐C ☐N
SEG52																									■S ☐C ☐N
SEG53																									■S ☐C ☐N
SEG54																									■S ☐C ☐N
SEG55																									■S ☐C ☐N

<address> H: RAM data high-order address (0–7)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63008)

1. The output specification of SEG0 to SEG29 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG36 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG36 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.
3. Configurations for nonexistent SEG pins (SEG30 to SEG35)
   - Always select "LCD segment output (S)" as the output specification of SEG30 to SEG35.
   - Leave the address cells for SEG30 to SEG35 blank. (Unused addresses will be allocated.)

Table 14.2.3.3 Segment option (S1C63004)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									□S □C □N
SEG1																									□S □C □N
SEG2																									□S □C □N
SEG3																									□S □C □N
SEG4																									□S □C □N
SEG5																									□S □C □N
SEG6																									□S □C □N
SEG7																									□S □C □N
SEG8																									□S □C □N
SEG9																									□S □C □N
SEG10																									□S □C □N
SEG11																									□S □C □N
SEG12																									□S □C □N
SEG13																									□S □C □N
SEG14																									□S □C □N
SEG15																									□S □C □N
SEG16																									□S □C □N
SEG17																									□S □C □N
SEG18																									□S □C □N
SEG19																									□S □C □N
SEG20																									■S □C □N
SEG21																									■S □C □N
SEG22																									■S □C □N
SEG23																									■S □C □N
SEG24																									■S □C □N
SEG25																									■S □C □N
SEG26																									■S □C □N
SEG27																									■S □C □N
SEG28																									■S □C □N
SEG29																									■S □C □N
SEG30																									■S □C □N
SEG31																									■S □C □N
SEG32																									■S □C □N
SEG33																									■S □C □N
SEG34																									■S □C □N
SEG35																									■S □C □N
SEG36																									■S □C □N
SEG37																									■S □C □N
SEG38																									■S □C □N
SEG39																									■S □C □N
SEG40																									■S □C □N
SEG41																									■S □C □N
SEG42																									■S □C □N
SEG43																									■S □C □N
SEG44																									■S □C □N
SEG45																									■S □C □N
SEG46																									■S □C □N
SEG47																									■S □C □N
SEG48																									■S □C □N
SEG49																									■S □C □N
SEG50																									■S □C □N
SEG51																									■S □C □N
SEG52																									■S □C □N
SEG53																									■S □C □N
SEG54																									■S □C □N
SEG55																									■S □C □N

<address> H: RAM data high-order address (0–7)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63004)

1. The output specification of SEG0 to SEG19 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG40 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG40 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.
3. Configurations for nonexistent SEG pins (SEG20 to SEG39)
   - Always select "LCD segment output (S)" as the output specification of SEG20 to SEG39.
   - Leave the address cells for SEG20 to SEG39 blank. (Unused addresses will be allocated.)

Table 14.2.3.4 Segment option (S1C63003)

Pin name	Address (F0xxH)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									☐S ☐C ☐N
SEG1																									☐S ☐C ☐N
SEG2																									☐S ☐C ☐N
SEG3																									☐S ☐C ☐N
SEG4																									☐S ☐C ☐N
SEG5																									☐S ☐C ☐N
SEG6																									☐S ☐C ☐N
SEG7																									☐S ☐C ☐N
SEG8																									☐S ☐C ☐N
SEG9																									☐S ☐C ☐N
SEG10																									■S ☐C ☐N
SEG11																									■S ☐C ☐N
SEG12																									■S ☐C ☐N
SEG13																									■S ☐C ☐N
SEG14																									■S ☐C ☐N
SEG15																									■S ☐C ☐N
SEG16																									■S ☐C ☐N
SEG17																									■S ☐C ☐N
SEG18																									■S ☐C ☐N
SEG19																									■S ☐C ☐N
SEG20																									■S ☐C ☐N
SEG21																									■S ☐C ☐N
SEG22																									■S ☐C ☐N
SEG23																									■S ☐C ☐N
SEG24																									■S ☐C ☐N
SEG25																									■S ☐C ☐N
SEG26																									■S ☐C ☐N
SEG27																									■S ☐C ☐N
SEG28																									■S ☐C ☐N
SEG29																									■S ☐C ☐N
SEG30																									■S ☐C ☐N
SEG31																									■S ☐C ☐N
SEG32																									■S ☐C ☐N
SEG33																									■S ☐C ☐N
SEG34																									■S ☐C ☐N
SEG35																									■S ☐C ☐N
SEG36																									■S ☐C ☐N
SEG37																									■S ☐C ☐N
SEG38																									■S ☐C ☐N
SEG39																									■S ☐C ☐N
SEG40																									■S ☐C ☐N
SEG41																									■S ☐C ☐N
SEG42																									■S ☐C ☐N
SEG43																									■S ☐C ☐N
SEG44																									■S ☐C ☐N
SEG45																									■S ☐C ☐N
SEG46																									■S ☐C ☐N
SEG47																									■S ☐C ☐N
SEG48																									■S ☐C ☐N
SEG49																									■S ☐C ☐N
SEG50																									■S ☐C ☐N
SEG51																									■S ☐C ☐N
SEG52																									■S ☐C ☐N
SEG53																									■S ☐C ☐N
SEG54																									■S ☐C ☐N
SEG55																									■S ☐C ☐N

<address> H: RAM data high-order address (0–3)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

Notes for using the segment option generator "winsog" (S1C63003)

1. The output specification of SEG0 to SEG9 can be selected from "LCD segment output (S)," "DC complementary output (C)" and "DC Nch open drain output (N)."
2. Configurations for SEG/GPIO pins (SEG44 to SEG55)
   - Always select "LCD segment output (S)" as the output specification of SEG44 to SEG55.
   - Leave the address cells of the pins for which "1. I/O" is selected with the "SEG/GPIO/RFC selector" option.
   - Enter addresses and data bits to the address cells of the pins for which "2. SEG" is selected with the "SEG/GPIO/RFC selector" option.
3. Configurations for nonexistent SEG pins (SEG10 to SEG43)
   - Always select "LCD segment output (S)" as the output specification of SEG10 to SEG43.
   - Leave the address cells for SEG10 to SEG43 blank. (Unused addresses will be allocated.)
4. Configurations for nonexistent COM pins (COM5 to COM7)
   - Leave the address cells for COM5 to COM7 blank. (Unused addresses will be allocated.)

14.3 LCD Display Control

14.3.1 Selecting Display Mode

In addition to the LPWR register for turning the display on and off, the DSPC[1:0] register is provided to select a display mode. There are three display modes available as shown in Table 14.3.1.1.

Table 14.3.1.1 Display mode

DSPC[1:0]	Display mode
3	All on mode
2	All off mode
1	All on mode
0	Normal mode

Normal mode: The display memory contents are output without being processed.
All on mode: All the LCD segments go on. The SEG terminals output an on waveform. The contents in the display memory are not modified.
All off mode: All the LCD segments go off. The SEG terminals output an off waveform. The contents in the display memory are not modified. (default)

14.3.2 Switching Drive Duty

In the S1C63004/008/016, the drive duty can be selected from six types (1/3 to 1/8) using the LDUTY[2:0] register. In the S1C63003, the drive duty can be selected from three types (1/3 to 1/5).

Table 14.3.2.1 Drive duty settings

LDUTY[2:0]	Drive duty	Common terminals used	Maximum number of segments			
			S1C63016	S1C63008	S1C63004	S1C63003
7	1/8	COM0–COM7	448 (56 × 8)	400 (50 × 8)	288 (36 × 8)	–
6	1/7	COM0–COM6	392 (56 × 7)	350 (50 × 7)	252 (36 × 7)	–
5	1/8	COM0–COM7	448 (56 × 8)	400 (50 × 8)	288 (36 × 8)	–
4	1/7	COM0–COM6	392 (56 × 7)	350 (50 × 7)	252 (36 × 7)	–
3	1/6	COM0–COM5	336 (56 × 6)	300 (50 × 6)	216 (36 × 6)	–
2	1/5	COM0–COM4	280 (56 × 5)	250 (50 × 5)	180 (36 × 5)	110 (22 × 5)
1	1/4	COM0–COM3	224 (56 × 4)	200 (50 × 4)	144 (36 × 4)	88 (22 × 4)
0	1/3	COM0–COM2	168 (56 × 3)	150 (50 × 3)	108 (36 × 3)	66 (22 × 3)

14.3.3 Switching Frame Frequency

The frame frequency is determined by the selected drive duty and the clock supplied from the clock manager. The clock to be supplied (16 Hz, 21.3 Hz, or 32 Hz) can be selected using the FLCKS[1:0] register. Selecting a low frame frequency can reduce current consumption.

Table 14.3.3.1 Frame frequency settings

FLCKS[1:0]	Source clock	1/8 duty	1/7 duty	1/6 duty	1/5 duty	1/4 duty	1/3 duty
3	Prohibited						
2	16.0 Hz	16.0 Hz	18.3 Hz	21.3 Hz	12.8 Hz	16.0 Hz	21.3 Hz
1	21.3 Hz	21.3 Hz	24.4 Hz	28.5 Hz	17.1 Hz	21.3 Hz	28.5 Hz
0	32.0 Hz	32.0 Hz	36.6 Hz	42.7 Hz	25.6 Hz	32.0 Hz	42.7 Hz

(When f_{OSC1} = 32.768 kHz)

Notes:
- Make sure the LCD display is off (LPWR = "0") before setting the frame frequency. If the frame frequency is switched when the LCD display is on (LPWR = "1"), the LCD may not display normally for one frame period after switching.
- The frame frequency affects the display quality. We recommend that the frame frequency should be determined after the display quality is evaluated using the actual LCD panel.

14.3.4 Drive Waveform

The drive waveforms by duty selection are shown in Figures 14.3.4.1 to 14.3.4.6.

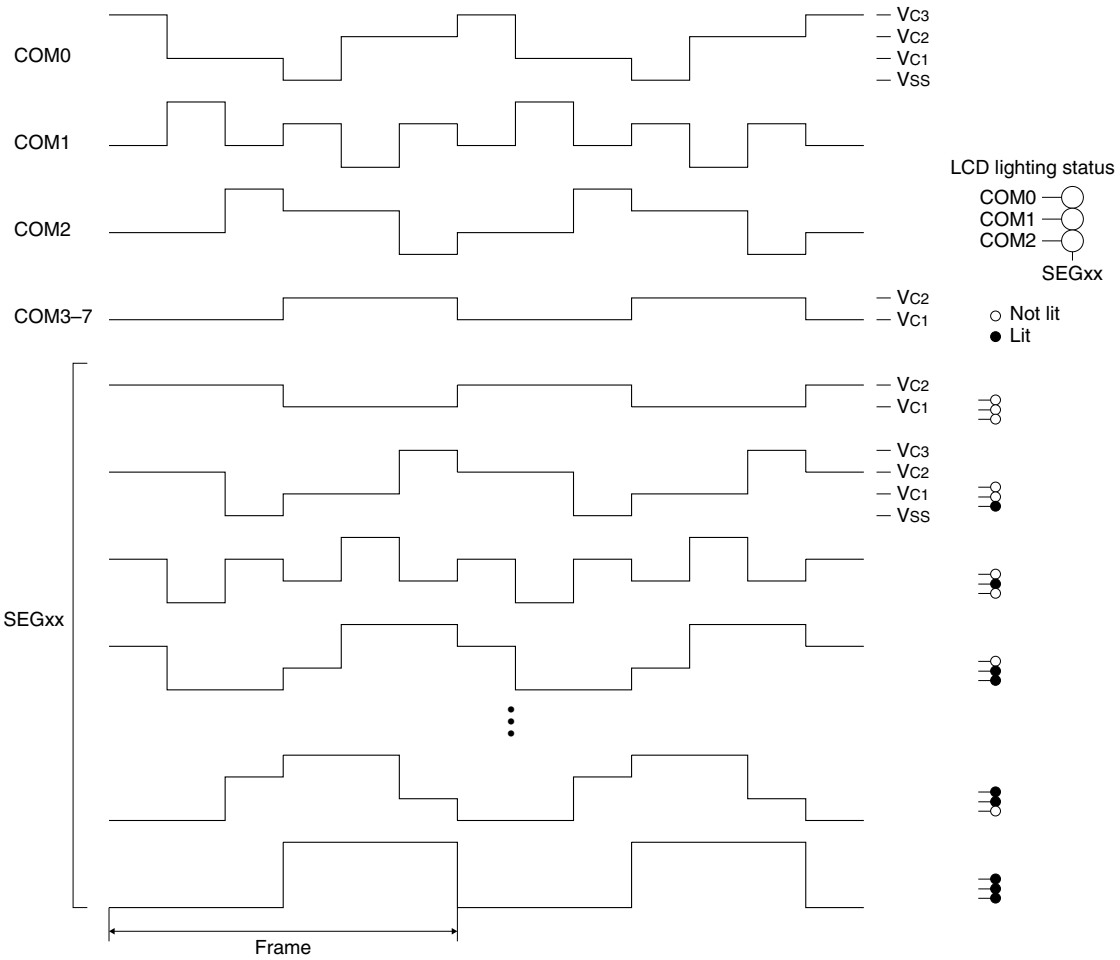


Figure 14.3.4.1 LCD drive waveform for 1/3 duty

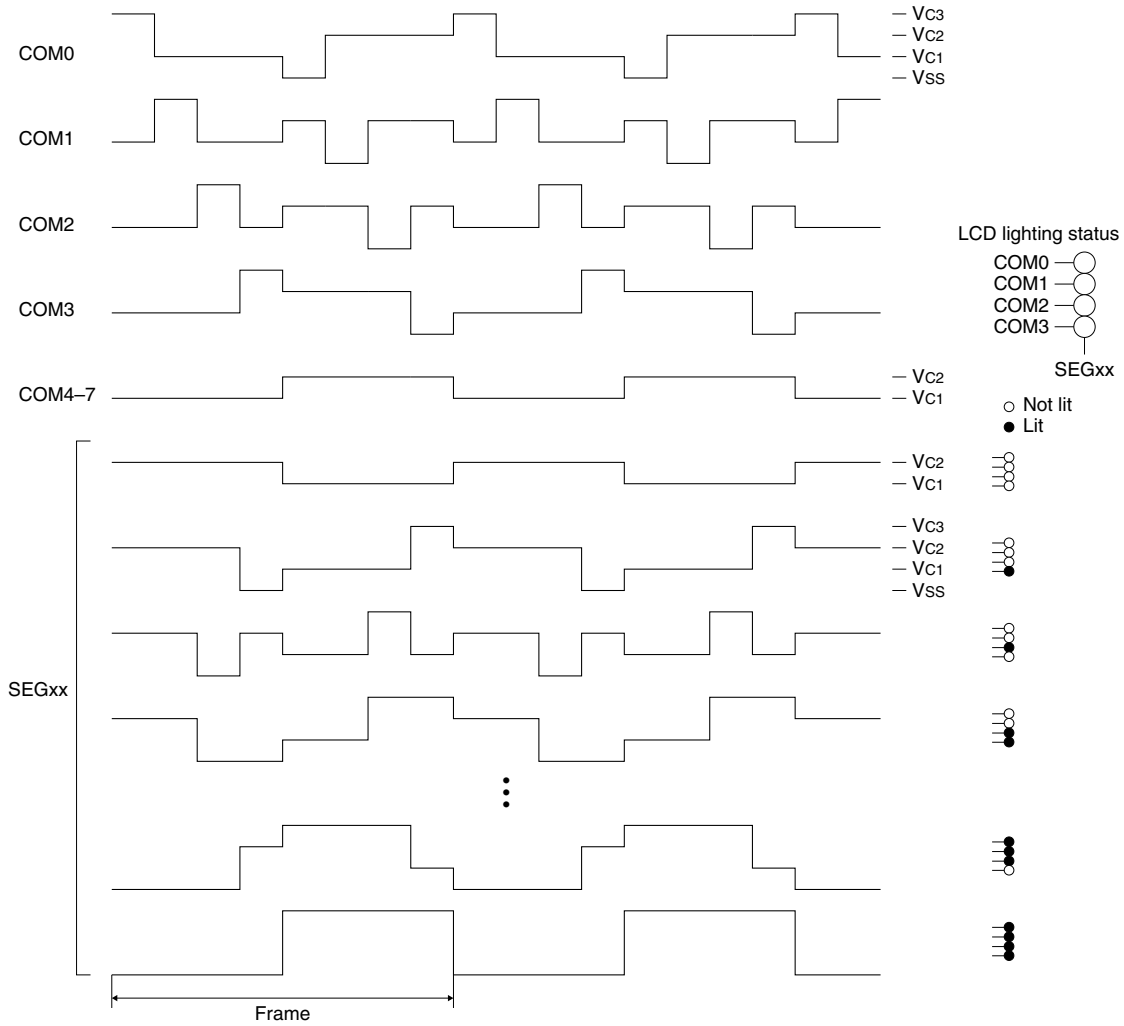


Figure 14.3.4.2 LCD drive waveform for 1/4 duty

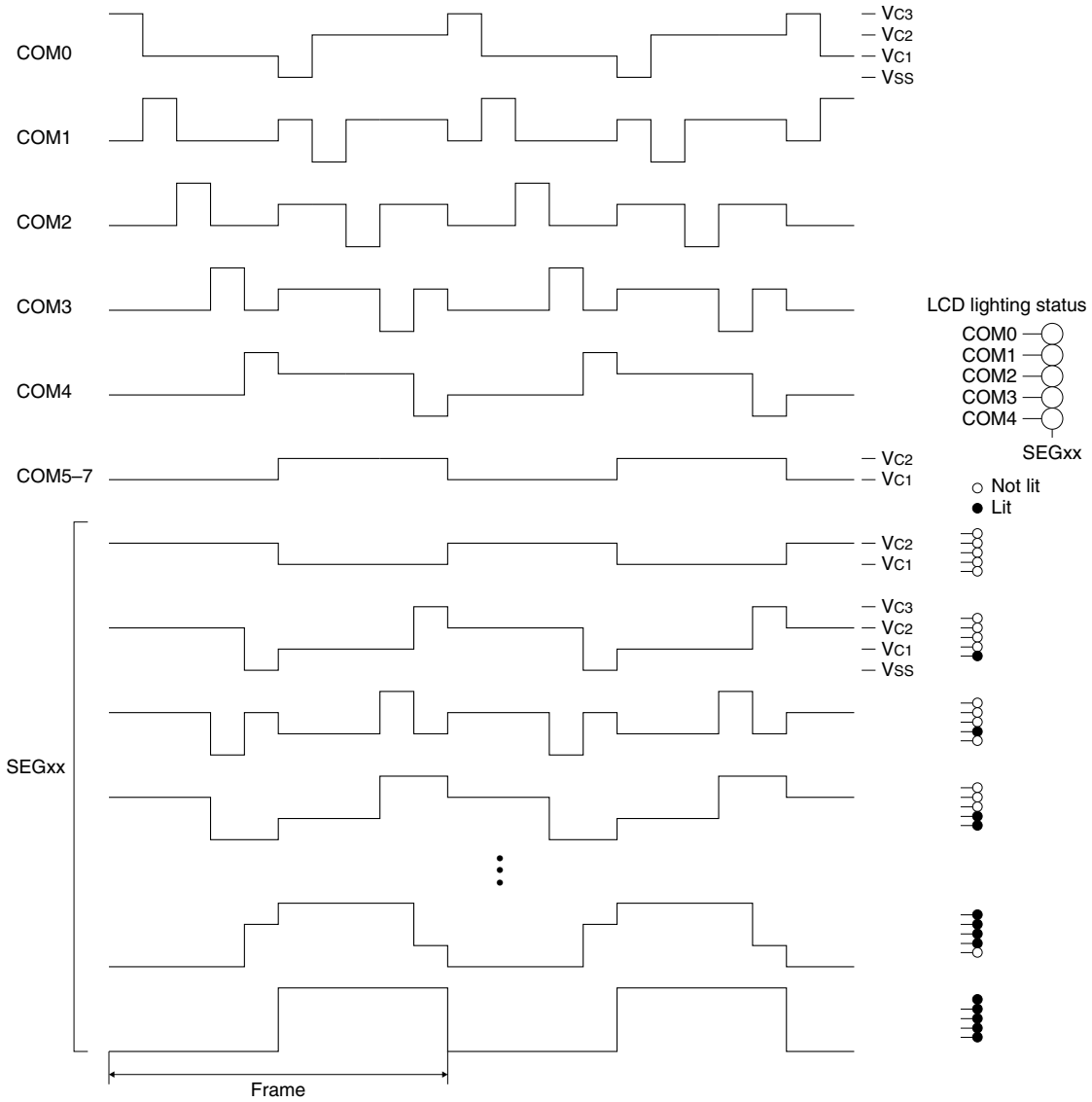


Figure 14.3.4.3 LCD drive waveform for 1/5 duty

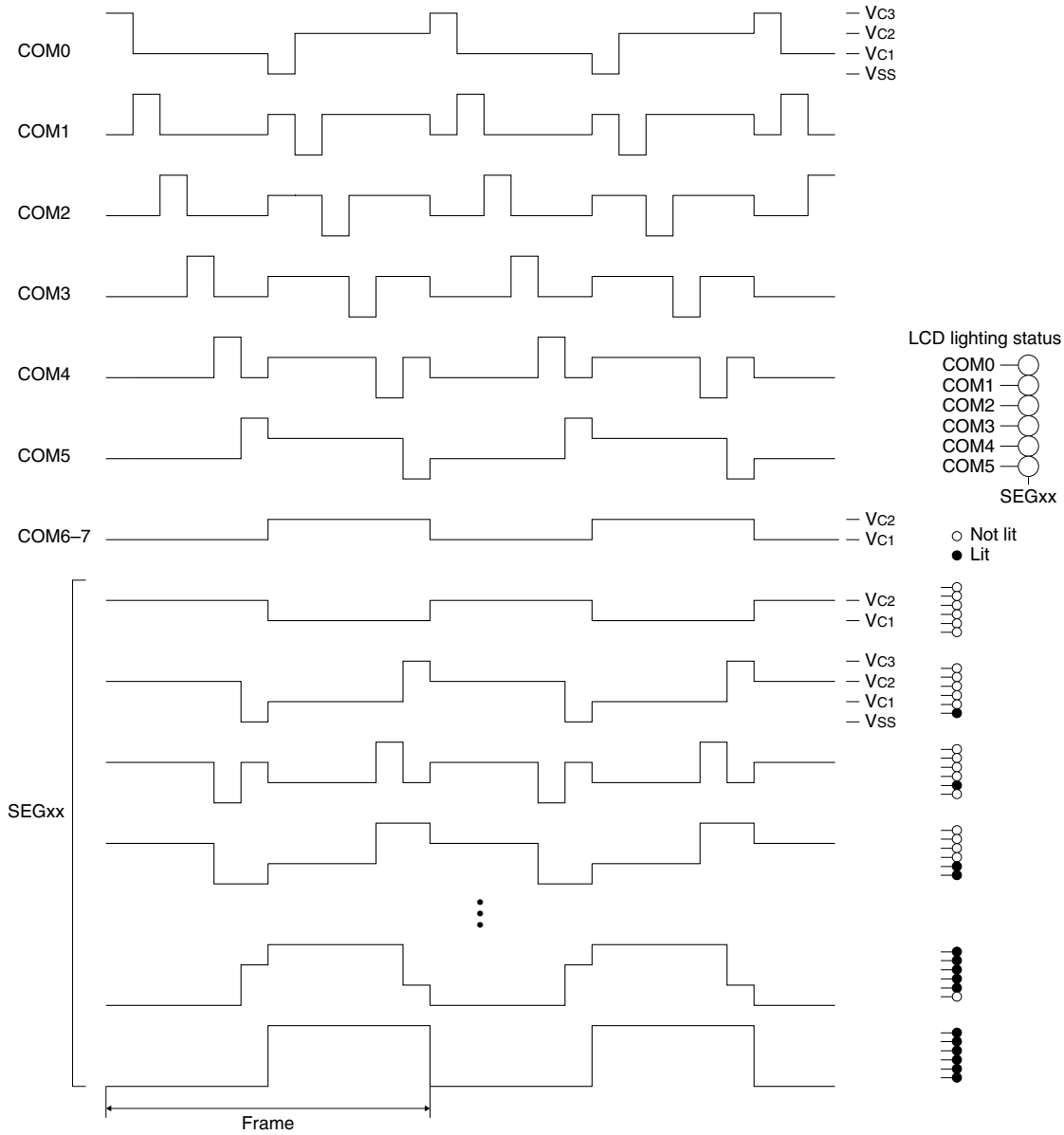


Figure 14.3.4.4 LCD drive waveform for 1/6 duty (S1C63004/008/016)

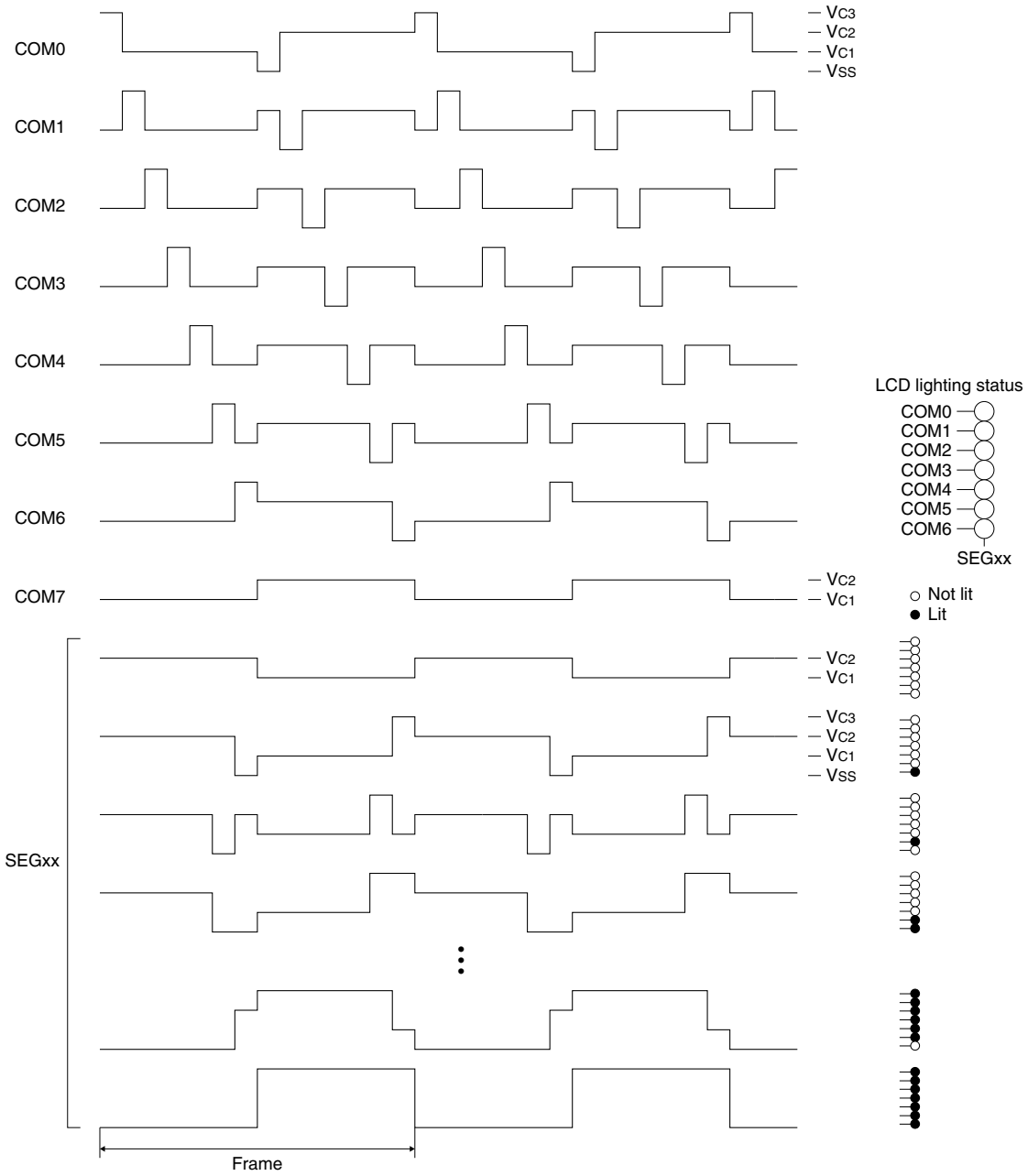


Figure 14.3.4.5 LCD drive waveform for 1/7 duty (S1C63004/008/016)

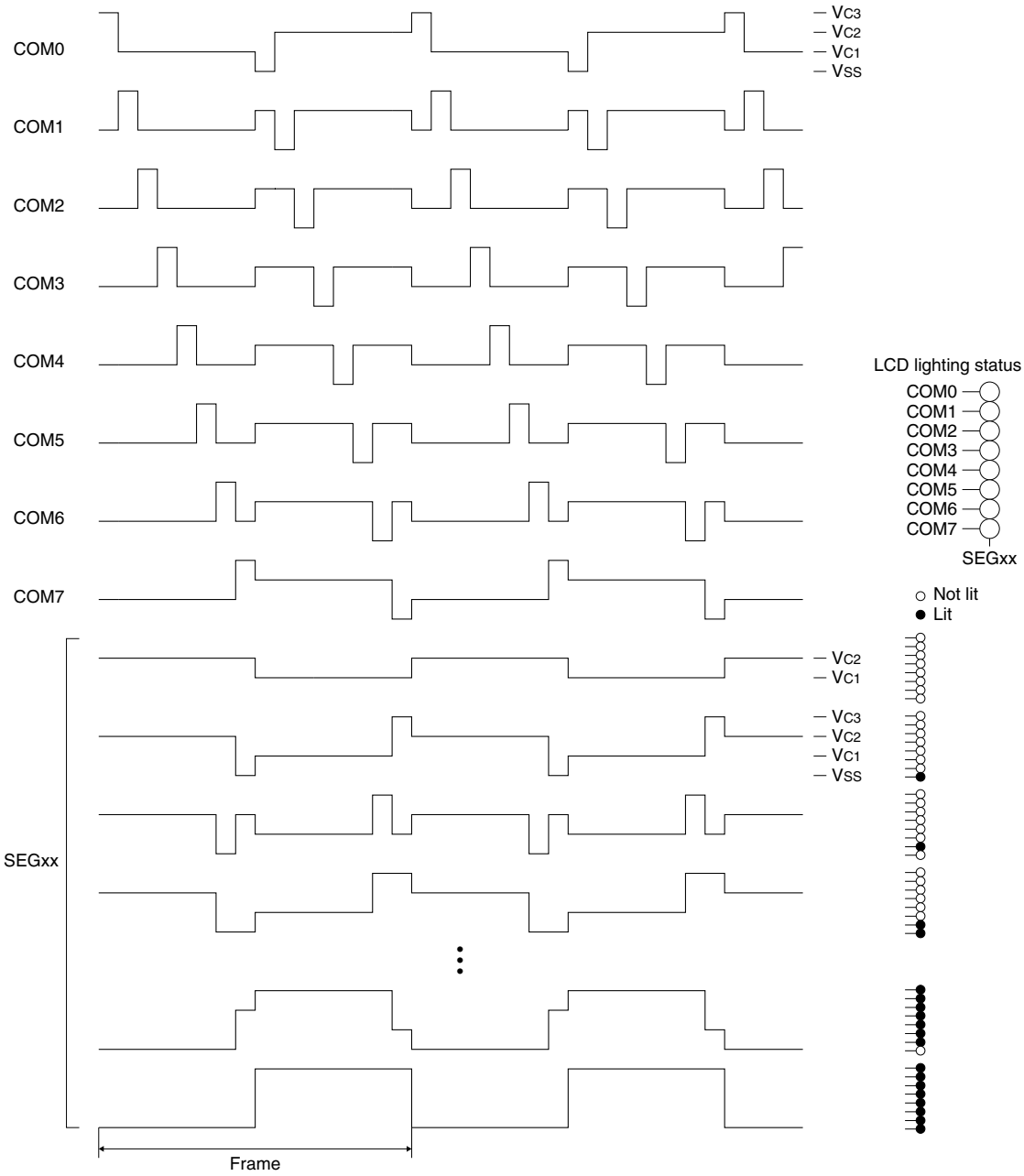


Figure 14.3.4.6 LCD drive waveform for 1/8 duty (S1C63004/008/016)

14.3.5 Static Drive

The LCD driver provides software setting of the static drive.
To set in static drive, write "1" to the STCD register. Then, by writing "1" to COM0 to COM7* (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static on waveform. When all the COM0 to COM7* bits are set to "0," the SEG terminal outputs an off waveform.
Figure 14.3.5.1 shows the static drive waveform.

Note: The static drive function uses all COM outputs (COM0 to COM7*) even if a duty other than 1/8 (1/5 in the S1C63003) is selected. Hence, for static drive, set the same value for all display memory corresponding to COM0 to COM7*.

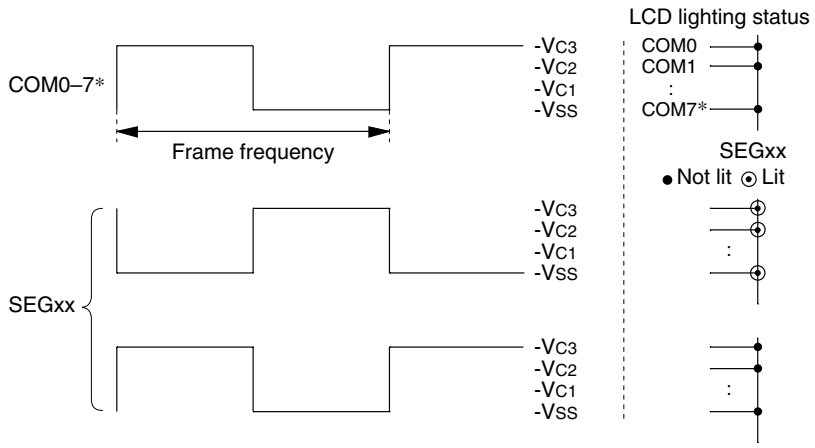


Figure 14.3.5.1 Static drive waveform

* COM0 to COM4 in the S1C63003

14.3.6 LCD Contrast Adjustment [S1C63004/008/016]

The S1C63004/008/016 allows software to adjust the LCD contrast. This function is realized by controlling the voltages V_{C1}, V_{C2} and V_{C3} output from the LCD system voltage regulator. The contrast can be adjusted to 16 levels using the LC[3:0] register as shown in Table 14.3.6.1.

Table 14.3.6.1 LCD contrast

LC[3:0]	Contrast	
FH	Level 15	(dark)
EH	Level 14	↑
DH	Level 13	
CH	Level 12	
BH	Level 11	
AH	Level 10	
9H	Level 9	
8H	Level 8	
7H	Level 7	
6H	Level 6	
5H	Level 5	
4H	Level 4	
3H	Level 3	
2H	Level 2	
1H	Level 1	↓
0H	Level 0	(light)

At initial reset, LC[3:0] is set to "0." The software should initialize the register to set to the desired contrast.
When an external power supply is selected by mask option, the LCD contrast cannot be adjusted using LC[3:0].

14.4 Display Memory

The display memory is located to addresses F000H–F07FH (F000H–F03FH in the S1C63003) in the data memory area and each data bit can be allocated to a segment terminal by mask option.

Table 14.4.1 Display memory

Model	Memory size	SEG terminals
S1C63016	448 bits	56 terminals (SEG0–SEG55)
S1C63008	400 bits	50 terminals (SEG0–SEG29, SEG36–SEG55)
S1C63004	288 bits	36 terminals (SEG0–SEG19, SEG40–SEG55)
S1C63003	110 bits	22 terminals (SEG0–SEG9, SEG44–SEG55)

When a bit in the display memory is set to "1," the corresponding LCD segment goes on, and when it is set to "0," the segment goes off.
At initial reset, the data memory contents become undefined hence, there is need to initialize by software.

Address Low / Base	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000H	S1C63016: 448 bits S1C63008: 400 bits S1C63004: 288 bits R/W															
F010H																
F020H																
F030H																
F040H																
F050H																
F060H																
F070H																

(a) S1C63004/008/016

Address Low / Base	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000H	S1C63003: 110 bits R/W															
F010H																
F020H																
F030H																

(b) S1C63003

Figure 14.4.1 Display memory map

The S1C63004/008/016 includes a 128-word memory (addresses F000H–F07FH) and the S1C63003 includes a 64-word memory (addresses F000H–F03FH). Any address can be allocated for a segment output. Note, however, that the number of bits usable as display memory are limited to the size shown above. The memory bits that are not used for LCD display can be used as general-purpose registers.

14.5 I/O Memory of LCD Driver

Table 14.5.1 shows the I/O addresses and the control bits for the LCD driver.

Table 14.5.1 Control bits of LCD driver

Address		Register name	R/W	Default	Setting/data								Function
FF12H	D3	**FLCKS1**	R/W	0	3	–			1	21.3			Frame frequency (Hz) selection
	D2	**FLCKS0**	R/W	0	2	16.0			0	32.0			
	D1	VCCKS1	R/W	0	3	–			1	2048			V_C boost frequency (Hz) selection
	D0	VCCKS0	R/W	0	2	–			0	Off			
FF50H	D3	0 (*3)	R	– (*2)	–								Unused
	D2	0 (*3)	R	– (*2)	–								Unused
	D1	**DSPC1**	R/W	1	3	All on			1	All on			LCD display mode selection
	D0	**DSPC0**	R/W	0	2	All off			0	Normal			
FF51H	D3	**STCD**	R/W	0	1	Static			0	Dynamic			LCD drive mode switch
	D2	**LDUTY2**	R/W	0	7	1/8 (*6)	4	1/7 (*6)	1	1/4			LCD drive duty selection
	D1	**LDUTY1**	R/W	0	6	1/7 (*6)	3	1/6 (*6)	0	1/3			
	D0	**LDUTY0**	R/W	0	5	1/8 (*6)	2	1/5					

Address		Register name	R/W	Default	Setting/data	Function
FF52H (∗6)	D3	**LC3**	R/W	0	0H(light)–FH(dark)	LCD contrast adjustment
	D2	**LC2**	R/W	0		
	D1	**LC1**	R/W	0		
	D0	**LC0**	R/W	0		

∗1 Initial value at initial reset ∗2 Not set in the circuit ∗3 Constantly "0" when being read
∗4 Unused in the S1C63003/004/008 ∗5 Unused in the S1C63003/004 ∗6 Unused in the S1C63003

FLCKS[1:0]: Frame frequency select register (FF12H•D[3:2])

Selects the frequency of the frame clock supplied from the clock manager.

Table 14.5.2 Frame frequency settings

FLCKS[1:0]	Source clock	1/8 duty	1/7 duty	1/6 duty	1/5 duty	1/4 duty	1/3 duty
3	Prohibited						
2	16.0 Hz	16.0 Hz	18.3 Hz	21.3 Hz	12.8 Hz	16.0 Hz	21.3 Hz
1	21.3 Hz	21.3 Hz	24.4 Hz	28.5 Hz	17.1 Hz	21.3 Hz	28.5 Hz
0	32.0 Hz	32.0 Hz	36.6 Hz	42.7 Hz	25.6 Hz	32.0 Hz	42.7 Hz

(When f_{OSC1} = 32.768 kHz)

At initial reset, this register is set to "0."

Notes:
- Make sure the LCD display is off (LPWR = "0") before setting the frame frequency. If the frame frequency is switched when the LCD display is on (LPWR = "1"), the LCD may not display normally for one frame period after switching.
- The frame frequency affects the display quality. We recommend that the frame frequency should be determined after the display quality is evaluated using the actual LCD panel.

DSPC[1:0]: LCD display mode select register (FF50H•D[1:0])

Sets the display mode.

Table 14.5.3 Display mode

DSPC[1:0]	Display mode
3	All on mode
2	All off mode
1	All on mode
0	Normal mode

Normal mode: The display memory contents are output without being processed.
All on mode: All the LCD segments go on. The SEG terminals output an on waveform. The contents in the display memory are not modified.
All off mode: All the LCD segments go off. The SEG terminals output an off waveform. The contents in the display RAM are not modified. (default)

At initial reset, this register is set to "2."

LDUTY[2:0]: LCD drive duty select register (FF51H•D[2:0])

Selects the LCD drive duty.

Table 14.5.4 Drive duty settings

LDUTY[2:0]	Drive duty	Common terminals used	Maximum number of segments			
			S1C63016	S1C63008	S1C63004	S1C63003
7	1/8	COM0–COM7	448 (56 × 8)	400 (50 × 8)	288 (36 × 8)	–
6	1/7	COM0–COM6	392 (56 × 7)	350 (50 × 7)	252 (36 × 7)	–
5	1/8	COM0–COM7	448 (56 × 8)	400 (50 × 8)	288 (36 × 8)	–
4	1/7	COM0–COM6	392 (56 × 7)	350 (50 × 7)	252 (36 × 7)	–
3	1/6	COM0–COM5	336 (56 × 6)	300 (50 × 6)	216 (36 × 6)	–
2	1/5	COM0–COM4	280 (56 × 5)	250 (50 × 5)	180 (36 × 5)	110 (22 × 5)
1	1/4	COM0–COM3	224 (56 × 4)	200 (50 × 4)	144 (36 × 4)	88 (22 × 4)
0	1/3	COM0–COM2	168 (56 × 3)	150 (50 × 3)	108 (36 × 3)	66 (22 × 3)

At initial reset, this register is set to "0."

STCD: LCD drive switch register (FF51H•D3)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0."

Note: The static drive function uses all COM outputs (COM0 to COM7*) even if a duty other than 1/8 (1/5 in the S1C63003) is selected. Hence, for static drive, set the same value for all display memory corresponding to COM0 to COM7*. (* COM0 to COM4 in the S1C63003)

LC[3:0]: LCD contrast adjustment register (FF52H) – S1C63004/008/016

Adjusts the LCD contrast.

LC[3:0] = 0H light
: :
LC[3:0] = FH dark

When the LCD drive voltage is supplied from outside by mask option selection, this adjustment becomes invalid.
At initial reset, this register is set to 0.

14.6 Precautions

- Make sure the LCD display is off (LPWR = "0") before setting the frame frequency. If the frame frequency is switched when the LCD display is on (LPWR = "1"), the LCD may not display normally for one frame period after switching.
- The frame frequency affects the display quality. We recommend that the frame frequency should be determined after the display quality is evaluated using the actual LCD panel.
- At initial reset, the contents of display memory are undefined and LC[3:0] (LCD contrast) is set to "0," therefore, it is necessary to initialize those contents by software. Also note that the LPWR and DSPC[1:0] registers are set to turn the display off.
- When Pxx (P20 to P53) and R/F converter terminals are used as the segment terminals by selecting mask option, do not alter the Pxx port and R/F converter control registers that affect these terminals from their initial values.

15 Sound Generator

15.1 Configuration of Sound Generator

The S1C63003/004/008/016 has a built-in sound generator for generating a buzzer signal. Hence, the generated buzzer signal can be output from the BZ terminal. Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds. Figure 15.1.1 shows the configuration of the sound generator.

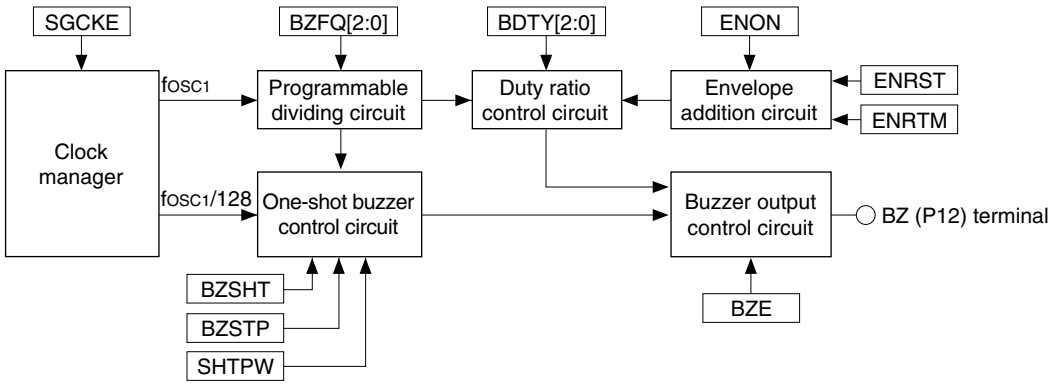


Figure 15.1.1 Configuration of sound generator

Note: If the BZ terminal is used to drive an external component that consumes a large amount of current such as a bipolar transistor, design the pattern of traces on the printed circuit board so that the operation of the external component does not affect the IC power supply. Refer to "Precautions on Mounting" in the Appendix for more information.

15.2 Controlling Operating Clock

To generate the buzzer signal, the clock for the sound generator must be supplied from the clock manager by writing "1" to the SGCKE register in advance.

Table 15.2.1 Controlling sound generator clock

SGCKE	Sound generator clock
1	Programmable dividing circuit input clock: fOSC1 (32 kHz)
	One-shot buzzer control circuit input clock: fOSC1 / 128 (256 Hz)
0	Off

If it is not necessary to run the sound generator, stop the clock supply by setting SGCKE to "0" to reduce current consumption.

15.3 Buzzer Output Control

The BZ signal generated by the sound generator is output from the BZ (P12) terminal by setting "1" for the buzzer output enable register BZE. The I/O control register IOC12 and data register P12 settings are ineffective while the BZ signal is being output. When BZE is set to "0," the P12 port is configured as a general-purpose DC input/output port.

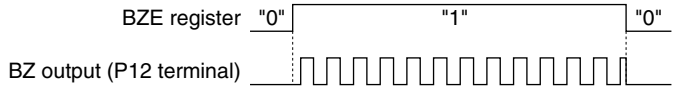


Figure 15.3.1 Buzzer signal output timing chart

Note: Since it generates the buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

15.4 Buzzer Frequency and Sound Level Settings

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency select register BZFQ[2:0] as shown in Table 15.4.1.

Table 15.4.1 Buzzer signal frequency setting

BZFQ[2:0]	Buzzer frequency (Hz)
0	4096.0
1	3276.8
2	2730.7
3	2340.6
4	2048.0
5	1638.4
6	1365.3
7	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.
The duty ratio can be selected from among the 8 types shown in Table 15.4.2 according to the setting of the buzzer duty select register BDTY[2:0].

Table 15.4.2 Duty ratio setting

Level	BDTY[2:0]	Duty ratio by buzzer frequency (Hz)			
		4096.0	3276.8	2730.7	2340.6
		2048.0	1638.4	1365.3	1170.3
Level 1 (Max.)	0	8/16	8/20	12/24	12/28
Level 2	1	7/16	7/20	11/24	11/28
Level 3	2	6/16	6/20	10/24	10/28
Level 4	3	5/16	5/20	9/24	9/28
Level 5	4	4/16	4/20	8/24	8/28
Level 6	5	3/16	3/20	7/24	7/28
Level 7	6	2/16	2/20	6/24	6/28
Level 8 (Min.)	7	1/16	1/20	5/24	5/28

When the high level output time has been made TH and when the low level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes TH/(TH+TL). When BDTY[2:0] has been set to "0H," the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY[2:0] has been set to "7H," the duty ratio becomes minimum and the sound level also becomes minimum. The duty ratio that can be set is different depending on the frequency that has been set, so see Table 15.4.2.

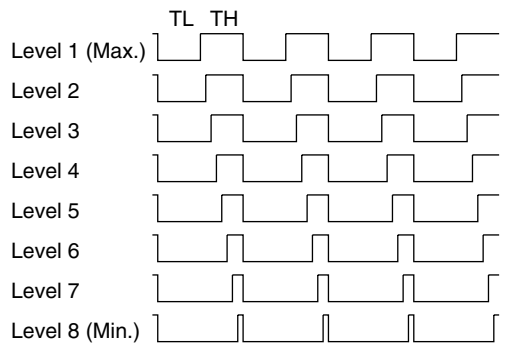


Figure 15.4.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY[2:0] settings will be invalid due to the control of the duty ratio.

15.5 Digital Envelope

A digital envelope for duty control can be added to the buzzer signal.
The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 15.4.2 in the preceding item from level 1 (maximum) to level 8 (minimum). The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.
When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8. When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of an envelope attached buzzer signal.
The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.
Figure 15.5.1 shows the timing chart of the digital envelope.

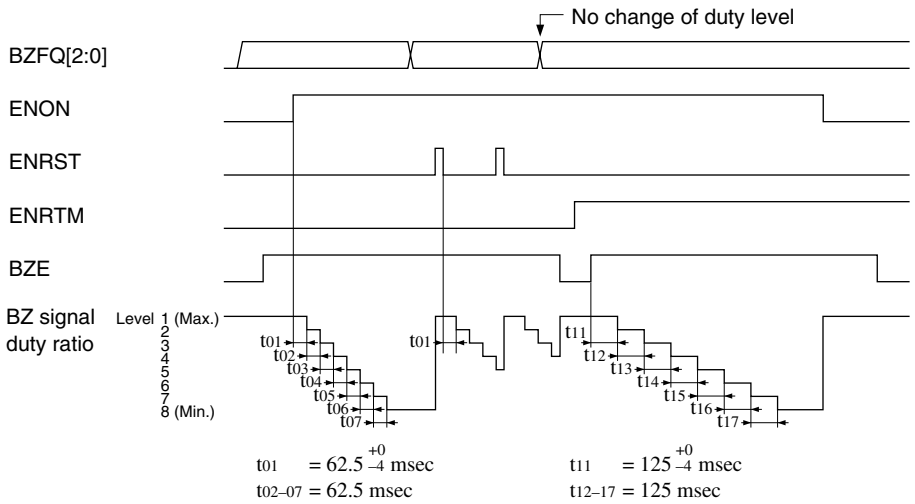


Figure 15.5.1 Timing chart for digital envelope

15.6 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.
The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the buzzer output terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.
The BZSHT also permits reading. When BZSHT is "1," the one-shot output circuit is in operation (during one-shot output) and when it is "0," it shows that the circuit is in the ready to output status.
In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes off in synchronization with the 256 Hz signal.
When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).
The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.
One-shot output is invalid during normal buzzer output (during BZE = "1").
Figure 15.6.1 shows timing chart for one-shot output.

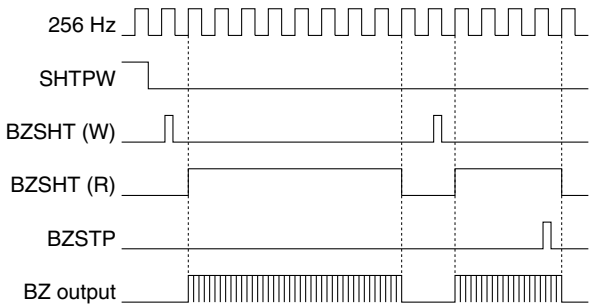


Figure 15.6.1 Timing chart for one-shot output

15.7 I/O Memory of Sound Generator

Table 15.7.1 shows the I/O addresses and the control bits for the sound generator.

Table 15.7.1 Control bits of sound generator

Address		Register name	R/W	Default	Setting/data						Function
FF16H	D3	MDCKE (*5)	R/W	0	1	Enable	0	Disable			Integer multiplier clock enable
	D2	**SGCKE**	R/W	0	1	Enable	0	Disable			Sound generator clock enable
	D1	SWCKE	R/W	0	1	Enable	0	Disable			Stopwatch timer clock enable
	D0	RTCKE	R/W	0	1	Enable	0	Disable			Clock timer clock enable
FF44H	D3	**ENRTM**	R/W	0	1	1 sec	0	0.5 sec			Envelope releasing time selection
	D2	**ENRST** (*3)	W	(Reset)	1	Reset	0	Invalid			Envelope reset (writing)
	D1	**ENON**	R/W	0	1	On	0	Off			Envelope On/Off
	D0	**BZE**	R/W	0	1	Enable	0	Disable			Buzzer output enable
FF45H	D3	0 (*3)	R	– (*2)	–						Unused
	D2	**BZSTP** (*3)	W	0	1	Stop	0	Invalid			1-shot buzzer stop (writing)
	D1	**BZSHT**	R/W	0	1	Trigger (W)	0	Invalid (W)			1-shot buzzer trigger (writing)
						Busy (R)		Ready (R)			1-shot buzzer status (reading)
	D0	**SHTPW**	R/W	0	1	125 msec	0	31.25 msec			1-shot buzzer pulse width setting
FF46H	D3	0 (*3)	R	– (*2)	–						Unused
	D2	**BZFQ2**	R/W	0	7	1170.3	4	2048.0	1	3276.8	Buzzer frequency (Hz) selection
	D1	**BZFQ1**	R/W	0	6	1365.3	3	2340.6	0	4096.0	
	D0	**BZFQ0**	R/W	0	5	1638.4	2	2730.7			
FF47H	D3	0 (*3)	R	– (*2)	–						Unused
	D2	**BDTY2**	R/W	0	7	Level 8	4	Level 5	1	Level 2	Buzzer signal duty ratio selection
	D1	**BDTY1**	R/W	0	6	Level 7	3	Level 4	0	Level 1	
	D0	**BDTY0**	R/W	0	5	Level 6	2	Level 3		(max.)	

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

SGCKE: Sound generator clock enable register (FF16H•D2)

Controls the clock supply to the sound generator.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to SGCKE, the sound generator operating clock is supplied from the clock manager. If it is not necessary to run the sound generator, stop the clock supply by setting SGCKE to "0" to reduce current consumption. At initial reset, this register is set to "0."

BZE: Buzzer output enable register (FF44H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the BZ (P12) terminal. The I/O control register IOC12 and data register P12 settings are ineffective while the BZ signal is being output. When BZE is set to "0," the P12 port is configured as a general-purpose DC input/output port. At initial reset, this register is set to "0."

ENON: Envelope On/Off control register (FF44H•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: On
When "0" is written: Off
Reading: Valid

Writing "1" to ENON causes an envelope to be added during buzzer signal output. When "0" has been written, an envelope is not added. At initial reset, this register is set to "0."

ENRST: Envelope reset (FF44H•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

Writing "1" to ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid. This bit is dedicated for writing, and is always "0" for reading.

ENRTM: Envelope releasing time select register (FF44H•D3)

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio. When "1" is written to ENRTM, it becomes 125 msec (8 Hz) units and when "0" is written, it becomes 62.5 msec (16 Hz) units. At initial reset, this register is set to "0."

SHTPW: One-shot buzzer pulse width setting register (FF45H•D0)

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

Writing "1" to SHTPW causes the one-short output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output. At initial reset, this register is set to "0."

BZSHT: One-shot buzzer trigger/status (FF45H•D1)

Controls the one-shot buzzer output.

When writing

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" to BZSHT causes the one-short output circuit to operate and a buzzer signal to be output. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

When reading

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0."

At initial reset, this bit is set to "0."

BZSTP: One-shot buzzer stop (FF45H•D2)

Stops the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Always "0"

Writing "1" to BZSTP permits the one-shot buzzer output to be turned off prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

BZFQ[2:0]: Buzzer frequency select register (FF46H•D[2:0])

Selects the buzzer signal frequency.

Table 15.7.2 Buzzer signal frequency setting

BZFQ[2:0]	Buzzer frequency (Hz)
0	4096.0
1	3276.8
2	2730.7
3	2340.6
4	2048.0
5	1638.4
6	1365.3
7	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock. At initial reset, this register is set to "0."

BDTY[2:0]: Duty level select register (FF47H•D[2:0])

Selects the duty ratio of the buzzer signal as shown in Table 15.7.3.

Table 15.7.3 Duty ratio setting

Level	BDTY[2:0]	Duty ratio by buzzer frequency (Hz)			
		4096.0	3276.8	2730.7	2340.6
		2048.0	1638.4	1365.3	1170.3
Level 1 (Max.)	0	8/16	8/20	12/24	12/28
Level 2	1	7/16	7/20	11/24	11/28
Level 3	2	6/16	6/20	10/24	10/28
Level 4	3	5/16	5/20	9/24	9/28
Level 5	4	4/16	4/20	8/24	8/28
Level 6	5	3/16	3/20	7/24	7/28
Level 7	6	2/16	2/20	6/24	6/28
Level 8 (Min.)	7	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio. However, when the envelope has been set to on (ENON = "1"), this setting becomes invalid. At initial reset, this register is set to "0."

15.8 Precautions

- Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.
- The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

16 R/F Converter

16.1 Configuration of R/F Converter

The S1C63003/004/008/016 has a built-in CR oscillation type R/F converter that can be used as an A/D converter. Two systems (channel 0 and channel 1) of CR oscillation circuits are built into the R/F converter, so it is possible to compose two types of R/F conversion circuits by connecting different sensors to each CR oscillation circuit. Channel 0 can be used as an R/F (Resistor/Frequency) conversion circuit using a DC bias resistive sensor such as a thermistor, and channel 1 can be used as an R/F conversion circuit the same as channel 0, or for an AC bias resistive sensor such as a humidity sensor. The channel to be used and sensor type for channel 1 are selected with software. Resistance value (relative value to external reference resistance) of the resistive sensor that has been connected to the sensor input terminal is converted into frequency by the CR oscillation circuit and the number of clocks is counted in the built-in measurement counter. By reading the value of the measurement counter, it can obtain the data after digitally-converting the value detected by the sensor. Various sensor circuits such as temperature/humidity measurement circuits can be easily realized using this R/F converter.
The configuration of the R/F converter is shown in Figure 16.1.1.

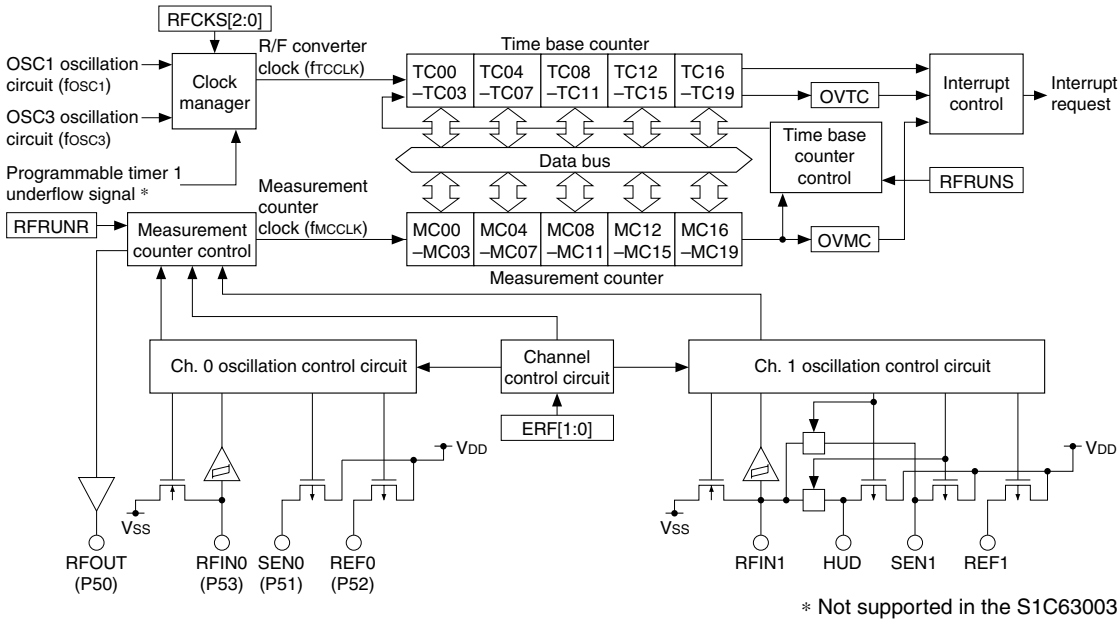


Figure 16.1.1 Configuration of R/F converter

Note: When using R/F converter channel 1, be sure to select all the HUD, SEN1, REF1 and RFIN1 pins by mask options for switching between the R/F converter pins and SEG pins. When the SEG pin is selected, channel 1 may not operate properly even if the HUD pin is not used.

16.2 Controlling Operating Clock

The R/F converter uses the clock supplied from the clock manager as its operating clock and the count clock for the time base counter. The clock manager generates six R/F converter clocks by dividing the OSC1 and OSC3 clocks. In the S1C63003, the R/F converter clock can be selected from the above six clocks. In the S1C63004/008/016, it can be selected from seven types (the above six clocks and the programmable timer 1 output clock). Use the RFCKS[2:0] register to select one of them as shown in Table 16.2.1.

Table 16.2.1 R/F converter clock frequencies

RFCKS[2:0]	RFC clock
7	fosc3 / 4
6	fosc3 / 2
5	fosc3 / 1
4	Programmable timer 1*
3	fosc1 / 4 (8 kHz)
2	fosc1 / 2 (16 kHz)
1	fosc1 / 1 (32 kHz)
0	Off

fosc1: OSC1 oscillation frequency. ( ) indicates the frequency when fosc1 = 32 kHz.
fosc3: OSC3 oscillation frequency

When programmable timer 1* is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the R/F converter clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to the "Programmable Timer" chapter for controlling the programmable timer.
If it is not necessary to run the R/F converter, stop the clock supply by setting RFCKS[2:0] to "0" to reduce current consumption.

* The programmable timer 1 output clock cannot be used in the S1C63003.

16.3 Connection Terminals and CR Oscillation Circuit

The R/F converter channel 0 input/output terminals and the RFOUT output terminal are shared with the I/O port (P50–P53), and the terminal functions must be switched with software when using these terminals for the R/F converter.
By setting the ERF[1:0] register to other than "0," P53, P52 and P51 are configured as the RFIN0, REF0 and SEN0 terminals, respectively.
The RFOUT output through the P50 port is effective when "1" is written to the RFOUT register. When the RFOUT register is "0," P50 is used as an I/O port.
The table below lists the correspondence between the P50 to P53 terminals and the R/F converter input/output.

Table 16.3.1 Setting input/output terminal functions

Terminal name	R/F converter input/output
P50	RFOUT
P51	SEN0
P52	REF0
P53	RFIN0

Note: At initial reset, P50 to P53 are configured as the I/O ports.
When using the R/F converter channel 0, switch the terminal functions (ERF[1:0] = "1," RFOUT = "1") in the initialize routine.

Two systems of CR oscillation circuits, channel 0 and channel 1, are built into the R/F converter and perform CR oscillation with the external resistor and capacitor.
The counter that is used to obtain R/F converted values is shared with channel 0 and channel 1. Therefore, operation for two channels is realized by switching the CR oscillation circuit that performs R/F conversion. The channel to perform R/F conversion and the sensor type should be selected using the ERF[1:0] register in advance.

Table 16.3.2 Selecting channel and sensor type

ERF[1:0]	Channel and sensor type
3	Ch.1 DC
2	Ch.1 AC
1	Ch.0 DC
0	I/O

DC: R/F conversion using a DC bias resistive sensor such as a thermistor
AC: R/F conversion using an AC bias resistive sensor such as a humidity sensor

(1) R/F conversion using a DC bias resistive sensor such as a thermistor

Channel 0 supports this conversion method only, and channel 1 is selected into this method by setting ERF[1:0] to "3." This method should be selected for R/F conversion using a normal resistive sensor (DC bias), such as temperature measurement using a thermistor. At initial reset, channel 1 is set into this conversion method.
Figure 16.3.1 shows the connection diagram of external elements.

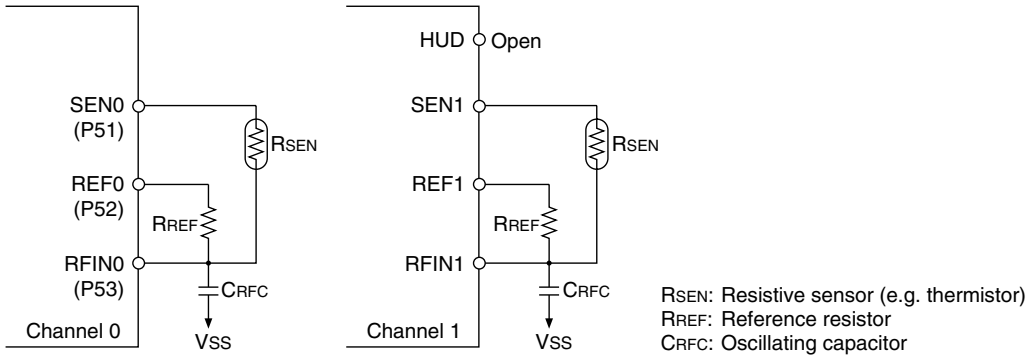


Figure 16.3.1 Connection diagram in case of R/F conversion

CR oscillation waveforms are shaped by the schmitt trigger and sent to the measurement counter. The clock sent to the measurement counter is also output from the RFOUT terminal while the sensor is oscillating. As a result, the oscillation frequency can be measured by an oscilloscope or other equipment. Since this monitor has no effect on oscillation frequency, it can be used to adjust R/F conversion accuracy. Oscillation waveforms and waveforms output from the RFOUT terminal are shown in Figure 16.3.2.

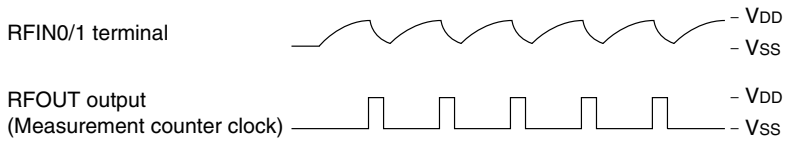


Figure 16.3.2 Oscillation waveform

(2) R/F conversion using an AC bias resistive sensor such as a humidity sensor

This conversion is possible only in channel 1, and this method is selected by setting ERF[1:0] to "2." This is basically the same as the R/F conversion described above (1), but the AC bias circuit works for a sensor (e.g. humidity sensor) to which DC bias cannot be applied for a long time. The oscillating operation by reference resistance is the same as the R/F conversion described above (1). Figure 16.3.3 shows the connection diagram of external devices.

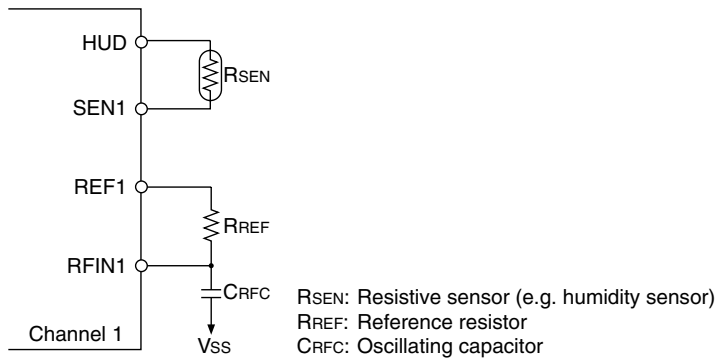


Figure 16.3.3 Connection diagram of resistive humidity sensor

The oscillation waveform is the same as Figure 16.3.2.

16.4 Operation of R/F Conversion

Counter

The R/F converter incorporates two types of counters: measurement counter MC[19:0] and time base counter TC[19:0]. The measurement counter is a 20-bit up counter that counts the CR oscillation clock with the reference resistance or sensor selected by software. The R/F conversion results can be obtained by reading this counter. The time base counter is a 20-bit up/down counter to equal both oscillation times for the reference resistance and the sensor. The time base counter uses the R/F converter clock selected by the RFCKS[2:0] register. Each counter permits reading and writing on a 4-bit basis.

First start an R/F conversion for the reference resistance. The measurement counter starts counting up and the time base counter starts counting down. The counters stop counting when the measurement counter overflows ("FFFFFH" → "00000H"). By resetting the time base counter to "00000H" before starting an R/F conversion for the reference resistance, the reference oscillation time will be obtained from the time base counter.

Then start an R/F conversion for the sensor, the measurement counter starts counting up from "00000H" and the time base counter starts counting up from the counted value. The counters stop counting when the time base counter overflows ("FFFFFH" → "00000H"). The oscillation time in this phase is the same as that of the reference resistance.

Therefore, by converting an appropriate initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from "00000H") and setting it into the measurement counter before starting to count, the number of counts for the sensor oscillation is obtained by reading the measurement counter after the R/F conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result.

The time base counter allows reading of the counter value and presetting of data. By saving the counter value after the reference oscillation has completed into the RAM, the subsequent reference oscillation phase can be omitted. The sensor oscillation can be started after setting the saved value to the time base counter and "00000H" to the measurement counter.

Note: When setting the measurement counter or time base counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H, FF67H → FF68H → FF69H → FF6AH → FF6BH). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used. If data other than low-order 4 bits is written, the counter cannot be set to the desired value.

R/F conversion sequence

An R/F conversion for the reference resistance starts by writing "1" to the RFRUNR register.

However, an initial value must be set to the measurement counter and the time base counter must be cleared to "00000H" before starting the R/F conversion.

When R/F conversion is initiated by the RFRUNR register, oscillation by the reference resistance begins, and the measurement counter starts counting up from the initial value by the oscillation clock. The time base counter also starts counting down by the R/F converter clock.

If the measurement counter becomes "00000H" due to overflow, the oscillation is terminated. At the same time an interrupt occurs and the RFRUNR register is set to "0," and the R/F converter circuit stops operation completely.

The time base counter value should be saved into the RAM for R/F conversion of the sensor.

Figure 16.4.1 shows a timing chart for the reference oscillation.

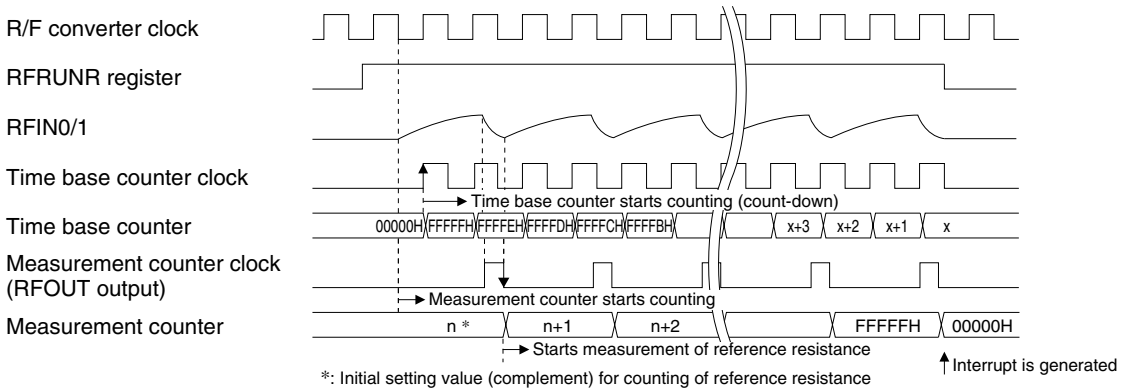


Figure 16.4.1 Reference oscillation timing chart

An R/F conversion for the sensor starts by writing "1" to the RFRUNS register. When performing this sensor oscillation after a reference oscillation has completed, it is not necessary to set initial values to the counters. If converting the sensor resistance independently, the measurement counter must be set to "00000H" and the time base counter must be set to the value measured at the time of a reference oscillation. When R/F conversion is initiated by the RFRUNS register, oscillation by the sensor begins, and the measurement counter starts counting up from "00000H" by the oscillation clock. The time base counter also starts counting up by the R/F converter clock. If the time base counter becomes "00000H," the oscillation is terminated. At the same time an interrupt occurs and the RFRUNS register is set to "0," and the R/F converter circuit stops operation completely.
Figure 16.4.2 shows a timing chart for the sensor oscillation.

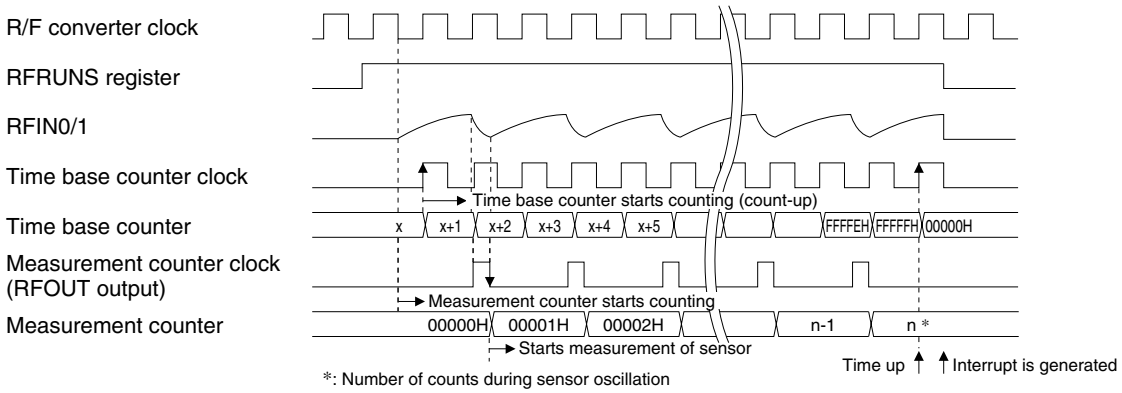


Figure 16.4.2 Sensor oscillation timing chart

By the above operation, the sensor is oscillated for the same period of time as the reference resistance is oscillated. Therefore, the difference in oscillation frequency can be measured from the values counted by the measurement counter.

Since the reference resistance is oscillated until the measurement counter overflows, an appropriate initial value needs to be set before R/F conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. Convert the initial value into a complement (value subtracted from "00000H") before setting it on the measurement counter. Since the data output from the measurement counter after R/F conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 16.4.3.

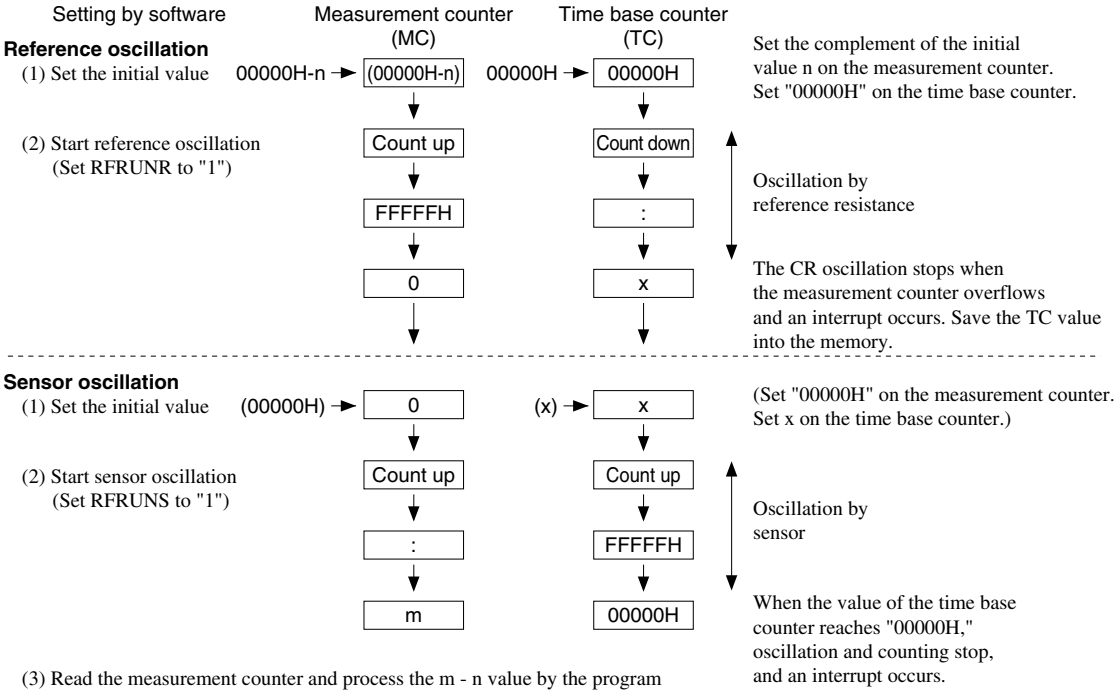


Figure 16.4.3 Sequence of R/F conversion

Note: Set the initial value of the measurement counter taking into account the measurable range and the overflow of counters.

16.5 Interrupt Function

The R/F converter has a function which allows interrupt to occur when an R/F conversion has completed or an error has occurred.

When the measurement counter reaches "00000H" during counting of the reference oscillation, both counters stop counting and RFRUNR is set to "0." At the same time, the interrupt factor flag IRFR is set to "1."

When the time base counter reaches "00000H" during counting of the sensor oscillation, both counters stop counting and RFRUNS is set to "0." At the same time, the interrupt factor flag IRFS is set to "1."

If the measurement counter overflows during counting of the sensor oscillation, both counters stop counting and RFRUNS is set to "0." In this case, the interrupt factor flag IRFE is set to "1." At the same time, the OVMC flag is also set to 1.

If the time base counter overflows during counting of the reference oscillation, both counters stop counting and RFRUNR is set to "0." In this case, the interrupt factor flag IRFE is set to "1." At the same time, the OVTC flag is also set to 1.

These interrupt factors allow masking by the interrupt mask registers EIRFR, EIRFS and EIRFE, and an interrupt is generated to the CPU when these registers are set to "1." When the interrupt mask register is set to "0," an interrupt is not generated to the CPU even if the interrupt factor flag is set to "1." The interrupt factor flag is reset to "0" by writing "1."

Timing of interrupt by the R/F converter is shown in Figures 16.5.1 to 16.5.4.

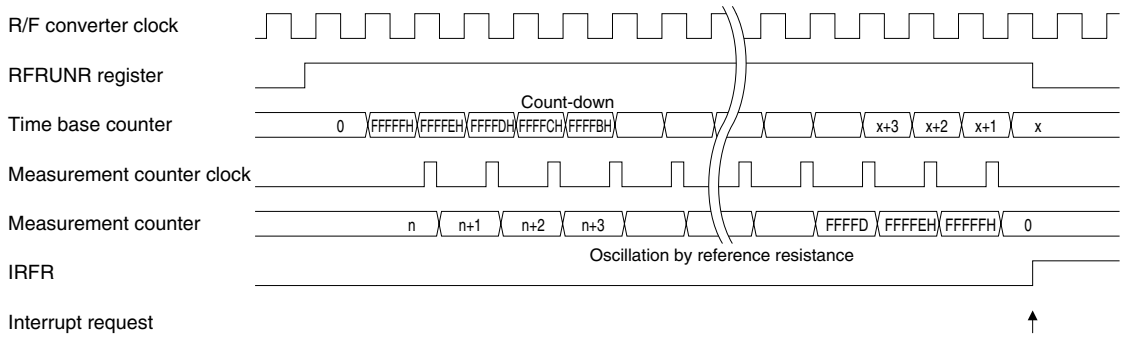


Figure 16.5.1 Reference oscillate completion interrupt

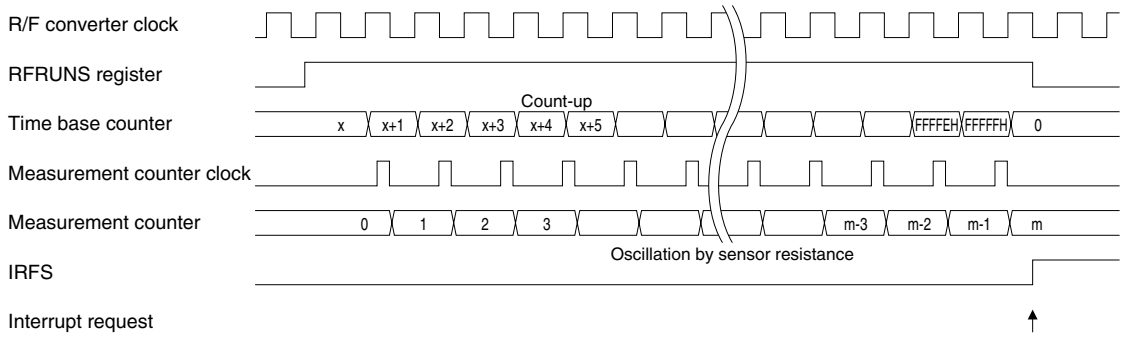


Figure 16.5.2 Sensor oscillate completion interrupt

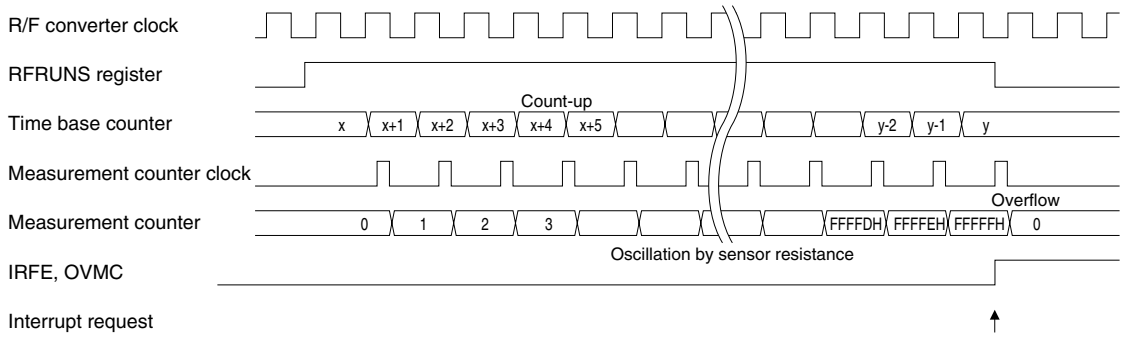


Figure 16.5.3 Error interrupt due to measurement counter overflow

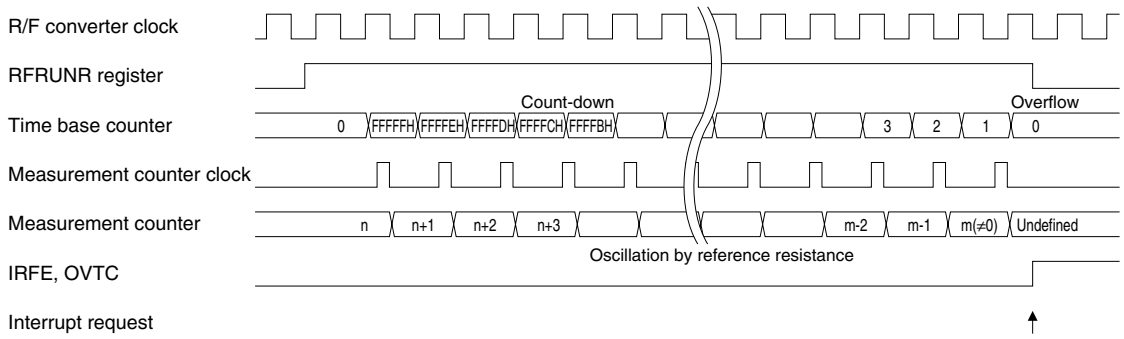


Figure 16.5.4 Error interrupt due to time base counter overflow

Note: When an error interrupt occurs, reset the overflow flag (OVMC or OVTC) by writing "1." The same error interrupt will occur again if the overflow flag is not reset.

16.6 Continuous Oscillation Function

By setting the RFCNT register to "1," the reference oscillation or sensor oscillation can be continued even if the stop condition has been met. This function with RFOUT enabled allows easy measurement of the CR oscillation frequency.

16.7 I/O Memory of R/F Converter

Table 16.7.1 shows the I/O addresses and the control bits for the R/F converter.

Table 16.7.1 Control bits of R/F converter

Address		Register name	R/W	Default	Setting/data	Function
FF15H	D3	0 (*3)	R	– (*2)	–	Unused
	D2	**RFCKS2**	R/W	0	7 $f_3/4$ 4 PT1 (*6) 1 f_1	R/F converter clock frequency selection
	D1	**RFCKS1**	R/W	0	6 $f_3/2$ 3 $f_1/4$ 0 Off	($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D0	**RFCKS0**	R/W	0	5 f_3 2 $f_1/2$	
FF60H	D3	**RFCNT**	R/W	0	1 Continuous 0 Normal	Continuous oscillation enable
	D2	**RFOUT**	R/W	0	1 Enable 0 Disable	RFOUT enable
	D1	**ERF1**	R/W	0	3 Ch.1 DC 1 Ch.0 DC	R/F conversion selection
	D0	**ERF0**	R/W	0	2 Ch.1 AC 0 I/O	
FF61H	D3	**OVTC**	R/W	0	1 Overflow error 0 No error	Time base counter overflow flag
	D2	**OVMC**	R/W	0	1 Overflow error 0 No error	Measurement counter overflow flag
	D1	**RFRUNR**	R/W	0	1 Run 0 Stop	Reference oscillation Run control/status
	D0	**RFRUNS**	R/W	0	1 Run 0 Stop	Sensor oscillation Run control/status
FF62H	D3	**MC3**	R/W	×	0H–FH	Measurement counter MC0–MC3 MC0 = LSB
	D2	**MC2**	R/W	×		
	D1	**MC1**	R/W	×		
	D0	**MC0**	R/W	×		
FF63H	D3	**MC7**	R/W	×	0H–FH	Measurement counter MC4–MC7
	D2	**MC6**	R/W	×		
	D1	**MC5**	R/W	×		
	D0	**MC4**	R/W	×		
FF64H	D3	**MC11**	R/W	×	0H–FH	Measurement counter MC8–MC11
	D2	**MC10**	R/W	×		
	D1	**MC9**	R/W	×		
	D0	**MC8**	R/W	×		
FF65H	D3	**MC15**	R/W	×	0H–FH	Measurement counter MC12–MC15
	D2	**MC14**	R/W	×		
	D1	**MC13**	R/W	×		
	D0	**MC12**	R/W	×		
FF66H	D3	**MC19**	R/W	×	0H–FH	Measurement counter MC16–MC19 MC19 = MSB
	D2	**MC18**	R/W	×		
	D1	**MC17**	R/W	×		
	D0	**MC16**	R/W	×		
FF67H	D3	**TC3**	R/W	×	0H–FH	Time base counter TC0–TC3 TC0 = LSB
	D2	**TC2**	R/W	×		
	D1	**TC1**	R/W	×		
	D0	**TC0**	R/W	×		
FF68H	D3	**TC7**	R/W	×	0H–FH	Time base counter TC4–TC7
	D2	**TC6**	R/W	×		
	D1	**TC5**	R/W	×		
	D0	**TC4**	R/W	×		
FF69H	D3	**TC11**	R/W	×	0H–FH	Time base counter TC8–TC11
	D2	**TC10**	R/W	×		
	D1	**TC9**	R/W	×		
	D0	**TC8**	R/W	×		
FF6AH	D3	**TC15**	R/W	×	0H–FH	Time base counter TC12–TC15
	D2	**TC14**	R/W	×		
	D1	**TC13**	R/W	×		
	D0	**TC12**	R/W	×		
FF6BH	D3	**TC19**	R/W	×	0H–FH	Time base counter TC16–TC19 TC19 = MSB
	D2	**TC18**	R/W	×		
	D1	**TC17**	R/W	×		
	D0	**TC16**	R/W	×		

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

RFCKS[2:0]: R/F converter clock frequency select register (FF15H•D[2:0])

Selects the R/F converter clock frequency.

Table 16.7.2 R/F converter clock frequencies

RFCKS[2:0]	RFC clock
7	fosc3 / 4
6	fosc3 / 2
5	fosc3 / 1
4	Programmable timer 1*
3	fosc1 / 4 (8 kHz)
2	fosc1 / 2 (16 kHz)
1	fosc1 / 1 (32 kHz)
0	Off

fosc1: OSC1 oscillation frequency. ( ) indicates the frequency when fosc1 = 32 kHz.
fosc3: OSC3 oscillation frequency

When programmable timer 1* is selected, the programmable timer 1 underflow signal is divided by 2 before it is used as the R/F converter clock. In this case, the programmable timer must be controlled before operating the R/F converter. Refer to the "Programmable Timer" chapter for controlling the programmable timer.
If it is not necessary to run the R/F converter, stop the clock supply by setting this register to "0" to reduce current consumption. At initial reset, this register is set to "0."

* The programmable timer 1 output clock cannot be used in the S1C63003.

ERF[1:0]: R/F conversion select register (FF60H•D[1:0])

Selects the channel and sensor type to perform R/F conversion.

Table 16.7.3 Selecting channel and sensor type

ERF[1:0]	Channel and sensor type
3	Ch.1 DC
2	Ch.1 AC
1	Ch.0 DC
0	I/O

DC: R/F conversion using a DC bias resistive sensor such as a thermistor
AC: R/F conversion using an AC bias resistive sensor such as a humidity sensor

The R/F converter channel 0 input/output terminals are shared with the I/O port (P51–P53). By setting this register to other than "0," P53, P52 and P51 are configured as the RFIN0, REF0 and SEN0 terminals, respectively. At initial reset, this register is set to "0."

RFOUT: RFOUT enable register (FF60H•D2)

Enables RFOUT output from the P50 port.

When "1" is written: Enabled (RFOUT)
When "0" is written: Disabled (I/O port)
Reading: Valid

When using the RFOUT output, write "1" to RFOUT to set P50 as the RFOUT output port. At initial reset, this register is set to "0."

RFCNT: Continuous oscillation enable register (FF60H•D3)

Enables the R/F converter to oscillate continuously.

When "1" is written: Continuous oscillation
When "0" is written: Normal oscillation
Reading: Valid

By writing "1" to RFCNT, the reference oscillation or sensor oscillation can be continued even if the stop condition has been met. This function with RFOUT enabled allows easy measurement of the CR oscillation frequency. At initial reset, this register is set to "0."

RFRUNS: Sensor oscillation RUN control/status (FF61H•D0)

Starts R/F conversion for the sensor and indicates the operating (RUN/STOP) status.

When "1" is written: R/F conversion starts
When "0" is written: No operation
When "1" is read: RUN status
When "0" is read: STOP status

Writing "1" to RFRUNS starts an R/F conversion for the sensor. The register is held at "1" while the R/F conversion is being processed and is set to "0" when the R/F conversion has completed. Writing "0" during an R/F conversion stops the CR oscillation. When the channel 1 sensor type (AC bias and DC bias) is changed by ERF[1:0] during sensor oscillation, RFRUNS is not reset. In this case, reset RFRUNS by writing "0." If RFRUNS and RFRUNR are set to "1" simultaneously, RFRUNR is effective. At initial reset, this register is set to "0."

RFRUNR: Reference oscillation RUN control/status (FF61H•D1)

Starts R/F conversion for the reference resistance and indicates the operating (RUN/STOP) status.

When "1" is written: R/F conversion starts
When "0" is written: No operation
When "1" is read: RUN status
When "0" is read: STOP status

Writing "1" to RFRUNR starts an R/F conversion for the reference resistance. The register is held at "1" while the R/F conversion is being processed and is set to "0" when the R/F conversion has completed. Writing "0" during an R/F conversion stops the CR oscillation. When the channel 1 sensor type (AC bias and DC bias) is changed by ERF[1:0] during reference oscillation, RFRUNR is not reset. In this case, reset RFRUNR by writing "0." RFRUNR is reset when the channel for R/F conversion is changed. If RFRUNS and RFRUNR are set to "1" simultaneously, RFRUNR is effective. At initial reset, this register is set to "0."

OVMC: Measurement counter overflow flag (FF61H•D2)

Indicates whether the measurement counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred
When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVMC is set to "1" and an error interrupt occurs at the same time. This flag is reset by writing "1" or starting R/F conversion. At initial reset, this flag is set to "0."

OVTC: Time base counter overflow flag (FF61H•D3)

Indicates whether the time base counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred
When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVTC is set to "1" and an error interrupt occurs at the same time. This flag is reset by writing "1" or starting R/F conversion. At initial reset, this flag is set to "0."

MC[19:0]: Measurement counter (FF66H–FF62H)

The measurement counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis. The complement of the number of clocks to be counted by the oscillation of the reference resistance must be entered in this counter prior to reference oscillation. When the counter reaches "00000H" due to overflow, the oscillation of the reference resistance stops. When converting a sensor oscillation, "00000H" must be set in this register (it is unnecessary when it is done immediately after a reference oscillation has completed). The sensor oscillation and measurement counter stop when the time base counter overflows. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program. Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to R/F conversion. At initial reset, this counter is undefined.

TC[19:0]: Time base counter (FF6BH–FF67H)

Writing and reading is possible on a 4-bit basis by the time base counter that is used to adjust the CR oscillation time between the reference resistance and the sensor. The time base counter counts down during oscillation of the reference resistance and counts up to "00000H" during oscillation of the sensor. "00000H" needs to be entered in the counter prior to a reference oscillation in order to adjust the CR oscillating time (number of clocks) of both counts. The counter value after a reference oscillation has completed should be read from this register and save it in the memory. The saved value should be set in this counter before starting a sensor oscillation. At initial reset, this counter is undefined.

16.8 Precautions

- When an error interrupt occurs, reset the overflow flag (OVMC or OVTC) by writing "1." The same error interrupt will occur again if the overflow flag is not reset.
- When setting the measurement counter or time base counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H, FF67H → FF68H → FF69H → FF6AH → FF6BH). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used. If data other than low-order 4 bits is written, the counter cannot be set to the desired value.
- The reference and sensor oscillation frequency IC deviation of the R/F converter may increase due to variations in resistances and capacitances, and board conditions. The 1.5 V low-voltage type is especially sensitive. Take this into consideration and perform evaluations sufficiently when using the R/F converter.
  For the IC deviation, see "Characteristics Curves (RFC reference/sensor oscillation frequency - resistance characteristic)" in Chapter 19, "Electrical Characteristics."

17 SVD (Supply Voltage Detection) Circuit
[S1C63004/008/016]

Note: The S1C63003 has no SVD circuit included.

17.1 Configuration of SVD Circuit

The S1C63004/008/016 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit on/off and the SVD criteria voltage setting can be done with software. Figure 17.1.1 shows the configuration of the SVD circuit.

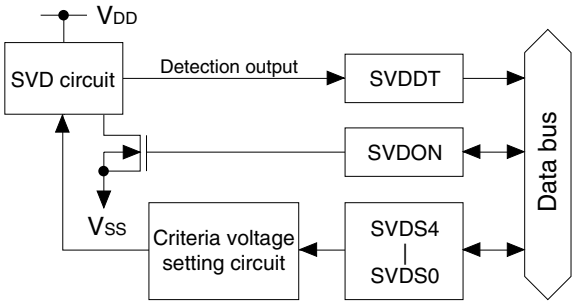


Figure 17.1.1 Configuration of SVD circuit

17.2 SVD Operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD} terminal–V_{SS} terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be selected from 29 types shown in Table 17.2.1 using the SVDS[4:0] register.

Table 17.2.1 Criteria voltage

SVDS[4:0]	Criteria voltage (V)	SVDS[4:0]	Criteria voltage (V)
1FH	3.20	0FH	1.65
1EH	3.10	0EH	1.60
1DH	3.00	0DH	1.55
1CH	2.90	0CH	1.50
1BH	2.80	0BH	1.45
1AH	2.70	0AH	1.40
19H	2.60	09H	1.35
18H	2.50	08H	1.30
17H	2.40	07H	1.25
16H	2.30	06H	1.20
15H	2.20	05H	1.15
14H	2.10	04H	1.10
13H	2.00	03H	1.05
12H	1.90	02H	
11H	1.80	01H	
10H	1.70	00H	

When the SVDON register is set to "1," supply voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0," the result is loaded to the SVDDT latch and the SVD circuit goes off.
To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is on, the IC draws a large current, so keep the SVD circuit off unless it is necessary.

17.3 I/O Memory of SVD Circuit

Table 17.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 17.3.1 Control bits of SVD circuit

Address		Register name	R/W	Default	Setting/data														Function
FF04H (*6)	D3	**SVDS3**	R/W	0	1F	3.20	1A	2.70	15	2.20	10	1.70	B	1.45	6	1.20	1	1.05	SVD criteria voltage (V) setting
	D2	**SVDS2**	R/W	0	1E	3.10	19	2.60	14	2.10	F	1.65	A	1.40	5	1.15	0	1.05	← SVDS[4:0]
	D1	**SVDS1**	R/W	0	1D	3.00	18	2.50	13	2.00	E	1.60	9	1.35	4	1.10			
	D0	**SVDS0**	R/W	0	1C	2.90	17	2.40	12	1.90	D	1.55	8	1.30	3	1.05			
					1B	2.80	16	2.30	11	1.80	C	1.50	7	1.25	2	1.05			
FF05H (*6)	D3	0 (*3)	R	– (*2)	–														Unused
	D2	**SVDS4**	R/W	0	(See FF04H)														SVD criteria voltage (V) setting
	D1	**SVDDT**	R	0	1	Low					0	Normal							SVD evaluation data
	D0	**SVDON**	R/W	0	1	On					0	Off							SVD circuit On/Off

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

SVDS[4:0]: SVD criteria voltage setting register (FF05H•D2, FF04H)

Criteria voltage for SVD is set as shown in Table 17.2.1. At initial reset, this register is set to "0."

SVDON: SVD circuit On/Off register (FF05H•D0)

Turns the SVD circuit on and off.

When "1" is written: SVD circuit On
When "0" is written: SVD circuit Off
Reading: Valid

When SVDON is set to "1," a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0," the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. At initial reset, this register is set to "0."

SVDDT: SVD evaluation data (FF05H•D1)

This is the result of supply voltage detection.

When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch. At initial reset, SVDDT is set to "0."

17.4 Precautions

- To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.
  1. Set SVDON to "1"
  2. Maintain for 500 µsec minimum
  3. Set SVDON to "0"
  4. Read SVDDT
- The SVD circuit should normally be turned off because SVD operation increase current consumption.

18 Integer Multiplier [S1C63008/016]

Note: The S1C63003/004 has no integer multiplier included.

18.1 Configuration of Integer Multiplier

The S1C63008/016 has a built-in unsigned-integer multiplier. This multiplier performs 8 bits × 8 bits of multiplication or 16 bits ÷ 8 bits of division and returns the results and three flag states.
Figure 18.1.1 shows the configuration of the integer multiplier.

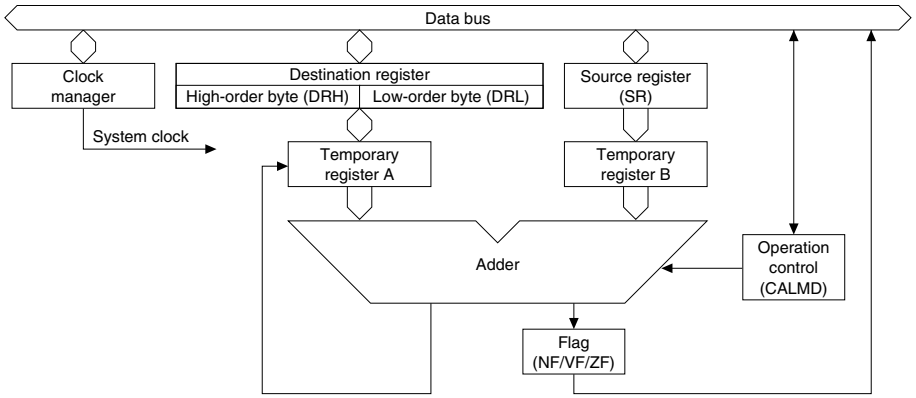


Figure 18.1.1 Configuration of the integer multiplier

18.2 Controlling Clock Manager

The integer multiplier operates with the clock supplied by the clock manager (CPU operating clock selected by OSCC and CLKCHG). Before the integer multiplier can be run, write "1" to the MDCKE register to supply the operating clock to the integer multiplier.

Table 18.2.1 Controlling integer multiplier clock

MDCKE	Integer multiplier clock
1	When CLKCHG = "0": f_{OSC1} (32 kHz) When OSCC = "1," CLKCHG = "1": f_{OSC3}
0	Off

If it is not necessary to run the integer multiplier, stop the clock supply by setting MDCKE to "0" to reduce current consumption.

18.3 Multiplication Mode

To perform a multiplication, set the multiplier to the source register (SR) and the multiplicand to the low-order 8 bits (DRL) of the destination register, then write "0" to the calculation mode select register (CALMD). The multiplication takes 10 CPU clock cycles from writing "0" to CALMD until the 16-bit product is loaded into the destination register (DRH and DRL). At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated. The following shows the conditions that change the operation flag states and examples of multiplication.
N flag: Set when the MSB of DRH is "1" and reset when it is "0."
V flag: Always reset after a multiplication.
Z flag: Set when the 16-bit value in DRH/DRL is 0000H and reset when it is not 0000H.

<Examples of multiplication>

DRL (multiplicand)	SR (multiplier)	DRH/DRL (product)	NF	VF	ZF
00H	64H	0000H	0	0	1
64H	58H	2260H	0	0	0
C8H	58H	44C0H	0	0	0
C8H	A5H	80E8H	1	0	0

18.4 Division Mode

To perform a division, set the divisor to the source register (SR) and the dividend to the destination register (DRH and DRL), then write "1" to the calculation mode select register (CALMD). The division takes 10 CPU clock cycles from writing "1" to CALMD until the quotient is loaded into the low-order 8 bits (DRL) of the destination register and the remainder is loaded into the high-order 8 bits (DRH) of the destination register. At the same time the result is loaded, the operation flags (NF, VF and ZF) are updated. However, when an overflow results (if the quotient exceeds the 8-bit range), the destination register (DRH and DRL) does not change its contents as it maintains the dividend. The following shows the conditions that change the operation flag states and examples of division.
N flag: Set when the MSB of DRL is "1" and reset when it is "0."
V flag: Set when the quotient exceeds the 8-bit range and reset when it is within the 8-bit range.
Z flag: Set when the 8-bit value in DRL is 00H and reset when it is not 00H.

<Examples of division>

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1A16H	64H	42H	4EH	0	0	0
332CH	64H	83H	00H	1	0	0
0000H	58H	00H	00H	0	0	1
2468H	13H	68H	24H	1	1	0

In the example of "2468H" ÷ "13H" shown above, DRH/DRL maintains the dividend because the quotient overflows the 8-bit. To get the correct results when an overflow has occurred, perform the division with two steps as shown below.

1. Divide the high-order 8 bits of the dividend (24H) by the divisor (13H) and then store the quotient (01H) to memory.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
0024H	13H	01H	11H	0	0	0

2. Keep the remainder (11H) in DRH and load the low-order 8 bits of the dividend (68H) to DRL, then perform division again.

DRH/DRL (dividend)	SR (divisor)	DRL (quotient)	DRH (remainder)	NF	VF	ZF
1168H	13H	EAH	0AH	1	0	0

The correct result is obtained as the quotient = 01EAH (the first and second results of DRL are merged into 16 bits) and the remainder = 0AH. However, since the operation flags (NF/VF/ZF) are changed in each step, they cannot indicate the states according to the final operation results.

Note: Make sure that the division results are correct using software as the hardware does not check.

18.5 Execution Cycle

Both the multiplication and division take 10 CPU clock cycles for an operation. Therefore, before the results can be read from the destination register DRH/DRL, wait at least 5 bus cycles after writing to CALMD. The same applies to reading the operation flags NF/VF/ZF. The following shows a sample program.

```
        ldb     %ext, src_data@h
        ldb     %xl, src_data@l      ; Set RAM address for operand
        ldb     %ext, au@h
        ldb     %yl, au@l            ; Set multiplier I/O memory address
;
        ldb     %ba, [%x]+
        ldb     [%y]+, %ba           ; Set data to SR
        ldb     %ba, [%x]+
        ldb     [%y]+, %ba           ; Set data to DRL
        ldb     %ba, [%x]+
        ldb     [%y]+, %ba           ; Set data to DRH
;
        ld      [%y], 0b0001         ; Start operation (select division mode)
;
```

```
        ldb     %ext, rslt_data@h
        ldb     %xl, rslt_data@l    ; Set result store address
        nop
        nop
        nop                         ; Dummy instructions to wait end of operation
;
        bit     [%y], 0b0100
        jrnz    overflow            ; Jump to error routine if VF = "1"
;
        add     %y, -4              ; Set DRL again
;
        ldb     %ba, [%y]+
        ldb     [%x]+, %ba          ; Store result (quotient) into RAM
        ldb     %ba, [%y]+
        ldb     [%x]+, %ba          ; Store result (remainder) into RAM
```

18.6 I/O Memory of Integer Multiplier

Table 18.6.1 shows the I/O addresses and the control bits for the integer multiplier.

Table 18.6.1 Control bits of integer multiplier

Address		Register name	R/W	Default	Setting/data				Function
FF16H	D3	**MDCKE** (*5)	R/W	0	1	Enable	0	Disable	Integer multiplier clock enable
	D2	SGCKE	R/W	0	1	Enable	0	Disable	Sound generator clock enable
	D1	SWCKE	R/W	0	1	Enable	0	Disable	Stopwatch timer clock enable
	D0	RTCKE	R/W	0	1	Enable	0	Disable	Clock timer clock enable
FF70H (*5)	D3	**SR3**	R/W	×	0H–FH				Source register (low-order 4 bits) SR0 = LSB
	D2	**SR2**	R/W	×					
	D1	**SR1**	R/W	×					
	D0	**SR0**	R/W	×					
FF71H (*5)	D3	**SR7**	R/W	×	0H–FH				Source register (high-order 4 bits) SR7 = MSB
	D2	**SR6**	R/W	×					
	D1	**SR5**	R/W	×					
	D0	**SR4**	R/W	×					
FF72H (*5)	D3	**DRL3**	R/W	×	0H–FH				Low-order 8-bit destination register (low-order 4 bits) DRL0 = LSB
	D2	**DRL2**	R/W	×					
	D1	**DRL1**	R/W	×					
	D0	**DRL0**	R/W	×					
FF73H (*5)	D3	**DRL7**	R/W	×	0H–FH				Low-order 8-bit destination register (high-order 4 bits) DRL7 = MSB
	D2	**DRL6**	R/W	×					
	D1	**DRL5**	R/W	×					
	D0	**DRL4**	R/W	×					
FF74H (*5)	D3	**DRH3**	R/W	×	0H–FH				High-order 8-bit destination register (low-order 4 bits) DRH0 = LSB
	D2	**DRH2**	R/W	×					
	D1	**DRH1**	R/W	×					
	D0	**DRH0**	R/W	×					
FF75H (*5)	D3	**DRH7**	R/W	×	0H–FH				High-order 8-bit destination register (high-order 4 bits) DRH7 = MSB
	D2	**DRH6**	R/W	×					
	D1	**DRH5**	R/W	×					
	D0	**DRH4**	R/W	×					
FF76H (*5)	D3	**NF**	R	0	1	Negative	0	Positive	Negative flag
	D2	**VF**	R	0	1	Overflow	0	No	Overflow flag
	D1	**ZF**	R	0	1	Zero	0	No	Zero flag
	D0	**CALMD**	R/W	0	1	Division (W) Run (R)	0	Multiplication (W) Stop (R)	Calculation mode selection (writing) Operation status (reading)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read
*4 Unused in the S1C63003/004/008 *5 Unused in the S1C63003/004 *6 Unused in the S1C63003

MDCKE: Integer multiplier clock enable register (FF16H•D3)

Controls the operating clock supply to the integer multiplier.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to MDCKE, the integer multiplier operating clock (CPU operating clock selected by OSCC and CLKCHG) is supplied from the clock manager. If it is not necessary to run the integer multiplier, stop the clock supply by setting MDCKE to "0" to reduce current consumption. At initial reset, this register is set to "0."

SR[7:0]: Source register (FF71H, FF70H)

Used to set multipliers and divisors.
Set the low-order 4 bits of data to SR[3:0] and the high-order 4 bits to SR[7:4]. This register maintains the latest set value until the next writing, so it is not necessary to set data for each operation if the same multiplier and divisor is used in a series of operations. At initial reset, this register is undefined.

DRL[7:0]: Destination register low-order 8 bits (FF73H, FF72H)

Used to set multiplicands and low-order 8 bits of dividends.
Set the low-order 4 bits of data to DRL[3:0] and the high-order 4 bits to DRL[7:4]. Data written to this register is loaded to the arithmetic circuit when an operation starts (by writing to FF76H•D0), and then a multiplication or a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the low-order 8 bits of the product or the quotient are loaded to this register. However, if an overflow occurs in a division process, the quotient is not loaded and the low-order 8 bits of the dividend remains. At initial reset, this register is undefined.

DRH[7:0]: Destination register high-order 8 bits (FF75H, FF74H)

Used to set high-order 8 bits of dividends.
Set the low-order 4 bits of data to DRH[3:0] and the high-order 4 bits to DRH[7:4].
At the start of a multiplication (by writing "0" to FF76H•D0), the contents in this register are ignored. After 10 CPU clock cycles (5 bus cycles) of multiplication process has finished, the high-order 8 bits of the product are loaded in this register. In a division process, data written to this register is loaded to the arithmetic circuit when an operation starts (by writing "1" to FF76H•D0), and then a division is performed in 10 CPU clock cycles (5 bus cycles). After the operation has finished, the remainder is loaded to this register. However, if an overflow occurs in a division process, the remainder is not loaded and the high-order 8 bits of the dividend remains. At initial reset, this register is undefined.

CALMD: Calculation mode select register/operation status (FF76H•D0)

Selects multiplication or division mode and starts operation.

When "1" is written: Selects/starts division
When "0" is written: Selects/starts multiplication
When "1" is read: Under operating
When "0" is read: Operation has finished

Writing to this register starts the specified operation. After that, this register is set to "1" and returns to "0" when the multiplication or division process has finished.
At initial reset, this register is reset to "0."

ZF: Zero flag (FF76H•D1)

Indicates whether the operation result is zero or not.

When "1" is read: Zero
When "0" is read: Not zero
Writing: Invalid

ZF is a read-only bit, so writing operation is invalid. At initial reset, this flag is set to "0."

VF: Overflow flag (FF76H•D2)

Indicates whether an overflow has occurred or not in a division process.

When "1" is read: Overflow occurred
When "0" is read: Overflow has not occurred
Writing: Invalid

When a multiplication process has finished, this flag is always set to "0." VF is a read-only bit, so writing operation is invalid. At initial reset, this flag is set to "0."

NF: Negative flag (FF76H•D3)

Indicates whether the operation result is a positive value or a negative value.

When "1" is read: Negative value (MSB of the results is "1")
When "0" is read: Positive value (MSB of the results is "0")
Writing: Invalid

NF is a read-only bit, so writing operation is invalid. At initial reset, this flag is set to "0."

18.7 Precautions

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode select register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation is in process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

19 Electrical Characteristics

19.1 Absolute Maximum Rating

3 V normal type

(V_{SS}=0V)

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}		-0.3 to +6.0	V
LCD power supply voltage	V_{C3}		-0.3 to +6.0	V
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V
High level output current	I_{OH}	1 pin	-5	mA
		Total of all pins	-20	mA
Low level output current	I_{OL}	1 pin	5	mA
		Total of all pins	20	mA
Permissible loss *1	P_D		200	mW
Operating temperature	Ta		-40 to 85	°C
Storage temperature	Tstg		-65 to 150	°C
Soldering temperature/time	Tsol		260°C, 10 seconds (lead section)	–

*1 In case of plastic package (QFP12-48pin, QFP14-80pin, QFP15-100pin, TQFP14-100pin)

1.5 V low-voltage type

(V_{SS} = 0V)

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}		-0.3 to +3.0	V
LCD power supply voltage	V_{C3}		-0.3 to +6.0	V
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V
High level output current	I_{OH}	1 pin	-5	mA
		Total of all pins	-20	mA
Low level output current	I_{OL}	1 pin	5	mA
		Total of all pins	20	mA
Permissible loss *1	P_D		200	mW
Operating temperature	Ta		-40 to 85	°C
Storage temperature	Tstg		-65 to 150	°C
Soldering temperature/time	Tsol		260°C, 10 seconds (lead section)	–

*1 In case of plastic package (QFP12-48pin, QFP14-80pin, QFP15-100pin, TQFP14-100pin)

19.2 Recommended Operating Conditions

3 V normal type

(Ta=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}		1.8	–	5.5	V
Operating frequency	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz
	f_{OSC3}	Ceramic oscillation *2	30	–	4,200	kHz
		CR oscillation (external R) *2	30	–	2,200	kHz
Capacitor between CA and CB *1	C_1		–	0.1	–	µF
Capacitor between V_{SS} and V_{C1} *1	C_4		–	0.1	–	µF
Capacitor between V_{SS} and V_{C2} *1	C_5		–	0.1	–	µF
Capacitor between V_{SS} and V_{C3} *1	C_6		–	0.1	–	µF
Capacitor between V_{SS} and V_{D1}	C_2		–	0.1	–	µF
Capacitor between V_{SS} and V_{OSC}	C_3		–	0.1	–	µF

*1 The capacitors are not required when LCD driver is not used. In this case, leave the V_{C1} to V_{C3}, CA and CB pins open.
*2 S1C63004/008/016

1.5 V low-voltage type

(Ta=-40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}		1.1	–	1.7	V
Operating frequency	f_{OSC1}	Crystal oscillation	–	32.768	–	kHz
	f_{OSC3}	Ceramic oscillation *2	30	–	1,000	kHz
		CR oscillation (external R) *2	30	–	500	kHz
Capacitor between CA and CB *1	C_1		–	0.1	–	µF
Capacitor between V_{SS} and V_{C1} *1	C_4		–	0.1	–	µF
Capacitor between V_{SS} and V_{C2} *1	C_5		–	0.1	–	µF
Capacitor between V_{SS} and V_{C3} *1	C_6		–	0.1	–	µF
Capacitor between V_{SS} and V_{D1}	C_2		–	0.1	–	µF
Capacitor between V_{SS} and V_{OSC}	C_3		–	0.1	–	µF

*1 The capacitors are not required when LCD driver is not used. In this case, leave the V_{C1} to V_{C3}, CA and CB pins open.
*2 S1C63004/008/016

19.3 DC Characteristics

3 V normal type

Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		P00–P13 *1	0.8V_{DD}	–	V_{DD}	V
Low level input voltage	V_{IL}		P00–P13 *1	0	–	0.2V_{DD}	V
High level Schmitt input voltage	V_{T+}		RESET, RFIN1, Pxx *2	0.5V_{DD}	–	0.9V_{DD}	V
Low level Schmitt input voltage	V_{T-}		RESET, RFIN1, Pxx *2	0.1V_{DD}	–	0.5V_{DD}	V
High level output current	I_{OH1}	V_{OH1}=0.9V_{DD}	Pxx, REF1, SEN1, HUD	–	–	-0.5	mA
Low level output current	I_{OL1}	V_{OL1}=0.1V_{DD}	Pxx, REF1, SEN1, HUD	0.5	–	–	mA
Input leakage current	I_{LI}		RESET, RFIN1, Pxx	-1	–	1	µA
Output leakage current	I_{LO}		Pxx, REF1, SEN1, HUD	-1	–	1	µA
Input pull-down resistance	R_{IN}		RESET, Pxx	100	–	500	kΩ
Input pin capacitance	C_{IN}	V_{IN}=0V, Ta = 25°C	RESET, RFIN1, Pxx	–	–	15	pF
Common output current	I_{OH2}	V_{OH2}=V_{C3}-0.05V	COM0 to COM7	–	–	-10	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V		10	–	–	µA
Segment output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	SEG0 to SEG55	–	–	-10	µA
(during LCD output)	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10	–	–	µA
Segment output current	I_{OH4}	V_{OH4}=0.8V_{DD}	SEG0 to SEG35	–	–	-330	µA
(during DC output)	I_{OL4}	V_{OL4}=0.2V_{DD}		330	–	–	µA

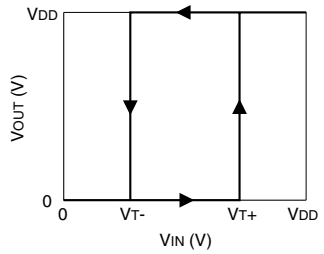
*1 When CMOS level is selected as the input interface
*2 P00–P13 configured as Schmitt input and other P ports

1.5 V low-voltage type

Unless otherwise specified: V_{DD}=1.1 to 1.7V, V_{SS}=0V, Ta=-40 to 85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		P00–P13 *1	0.8V_{DD}	–	V_{DD}	V
Low level input voltage	V_{IL}		P00–P13 *1	0	–	0.2V_{DD}	V
High level Schmitt input voltage	V_{T+}		RESET, RFIN1, Pxx *2	0.45V_{DD}	–	0.9V_{DD}	V
Low level Schmitt input voltage	V_{T-}		RESET, RFIN1, Pxx *2	0.1V_{DD}	–	0.55V_{DD}	V
High level output current	I_{OH1}	V_{OH1}=0.9V_{DD}	Pxx, REF1, SEN1, HUD	–	–	-0.25	mA
Low level output current	I_{OL1}	V_{OL1}=0.1V_{DD}	Pxx, REF1, SEN1, HUD	0.25	–	–	mA
Input leakage current	I_{LI}		RESET, RFIN1, Pxx	-1	–	1	µA
Output leakage current	I_{LO}		Pxx, REF1, SEN1, HUD	-1	–	1	µA
Input pull-down resistance	R_{IN}		RESET, Pxx	100	–	500	kΩ
Input pin capacitance	C_{IN}	V_{IN}=0V, Ta = 25°C	RESET, RFIN1, Pxx	–	–	15	pF
Common output current	I_{OH2}	V_{OH2}=V_{C3}-0.05V	COM0 to COM7	–	–	-10	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V		10	–	–	µA
Segment output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	SEG0 to SEG55	–	–	-10	µA
(during LCD output)	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10	–	–	µA
Segment output current	I_{OH4}	V_{OH4}=0.8V_{DD}	SEG0 to SEG35	–	–	-165	µA
(during DC output)	I_{OL4}	V_{OL4}=0.2V_{DD}		165	–	–	µA

*1 When CMOS level is selected as the input interface
*2 P00–P13 configured as Schmitt input and other P ports



19.4 Analog Circuit Characteristics and Current Consumption

19.4.1 LCD Driver

The typical values in the following LCD driver characteristics varies depending on the panel load (panel size, drive duty, number of display pixels and display contents), so evaluate them by connecting to the actually used LCD panel.

S1C63004/008/016 LCD drive voltage (V_{C1} reference)

Unless otherwise specified: V_{DD}=1.2 to 1.7V (1.5V type) or V_{DD}=1.8 to 5.5V (3V type), V_{SS}=0V, Ta=25°C, C_1–C_6=0.1µF,
When a checker pattern is displayed, No panel load, A 1 MΩ load resistor is connected between V_{SS} and V_{C1}, between V_{SS} and V_{C2}, and between V_{SS} and V_{C3}.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.335 × V_{C3}(typ.)	–	0.363 × V_{C3}(typ.)	V
	V_{C2}		0.646 × V_{C3}(typ.)	–	0.700 × V_{C3}(typ.)	V
	V_{C3}	LC[3:0]=0H		2.75		V
		LC[3:0]=1H		2.84		V
		LC[3:0]=2H		2.92		V
		LC[3:0]=3H		3.00		V
		LC[3:0]=4H		3.08		V
		LC[3:0]=5H		3.17		V
		LC[3:0]=6H		3.25		V
		LC[3:0]=7H	Typ. ×	3.34	Typ. ×	V
		LC[3:0]=8H	0.96	3.42	1.04	V
		LC[3:0]=9H		3.50		V
		LC[3:0]=AH		3.58		V
		LC[3:0]=BH		3.67		V
		LC[3:0]=CH		3.75		V
		LC[3:0]=DH		3.83		V
		LC[3:0]=EH		3.91		V
		LC[3:0]=FH		4.00		V

Notes:
- Depending on the panel load, when V_{DD} is 1.2 V or lower, the LCD drive voltage does not measure up to the specifications above.
- Contrast settings to set "V_{C1} Max. > V_{DD}" are impossible, as the V_{C1} voltage is always lower than V_{DD}. See "LCD drive voltage - supply voltage characteristic (1/3 bias, V_{C1} reference), 1.5 V low-voltage type" in Section 19.8, "Characteristics Curves (reference value)."

S1C63004/008/016 LCD drive voltage (V_{C2} reference)

Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C, C_1–C_6=0.1µF, When a checker pattern is displayed, No panel load
A 1 MΩ load resistor is connected between V_{SS} and V_{C1}, between V_{SS} and V_{C2}, and between V_{SS} and V_{C3}.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.323 × V_{C3}(typ.)	–	0.349 × V_{C3}(typ.)	V
	V_{C2}		0.650 × V_{C3}(typ.)	–	0.704 × V_{C3}(typ.)	V
	V_{C3}	LC[3:0]=0H		2.84		V
		LC[3:0]=1H		2.92		V
		LC[3:0]=2H		3.01		V
		LC[3:0]=3H		3.09		V
		LC[3:0]=4H		3.17		V
		LC[3:0]=5H		3.26		V
		LC[3:0]=6H		3.34		V
		LC[3:0]=7H	Typ. ×	3.43	Typ. ×	V
		LC[3:0]=8H	0.96	3.51	1.04	V
		LC[3:0]=9H		3.60		V
		LC[3:0]=AH		3.68		V
		LC[3:0]=BH		3.77		V
		LC[3:0]=CH		3.85		V
		LC[3:0]=DH		3.94		V
		LC[3:0]=EH		4.02		V
		LC[3:0]=FH		4.11		V

Note: V_{C2} reference cannot be set in the 1.5 V low-voltage type, as the maximum operating voltage is 1.7 V.

S1C63003 LCD drive voltage (V_{C1} reference)

Unless otherwise specified: V_{DD}=1.2 to 1.7V (1.5V type) or V_{DD}=1.8 to 5.5V (3V type), V_{SS}=0V, Ta=25°C, C_1–C_6=0.1µF,
When a checker pattern is displayed, No panel load, A 1 MΩ load resistor is connected between V_{SS} and V_{C1}, between V_{SS} and V_{C2}, and between V_{SS} and V_{C3}.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.347 × V_{C3}(typ.)	–	0.350 × V_{C3}(typ.)	V
	V_{C2}		0.665 × V_{C3}(typ.)	–	0.670 × V_{C3}(typ.)	V
	V_{C3}		Typ. × 0.96	2.947	Typ. × 1.04	V

Note: Depending on the panel load, when V_{DD} is 1.2 V or lower, the LCD drive voltage does not measure up to the specifications above.

S1C63003 LCD drive voltage (V_{C2} reference)

Unless otherwise specified: V_{DD}=2.0 to 5.5V, V_{SS}=0V, Ta=25°C, C_1–C_6=0.1µF, When a checker pattern is displayed, No panel load
A 1 MΩ load resistor is connected between V_{SS} and V_{C1}, between V_{SS} and V_{C2}, and between V_{SS} and V_{C3}.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}		0.329 × V_{C3}(typ.)	–	0.340 × V_{C3}(typ.)	V
	V_{C2}		0.660 × V_{C3}(typ.)	–	0.683 × V_{C3}(typ.)	V
	V_{C3}		Typ. × 0.96	3.022	Typ. × 1.04	V

Notes:
- V_{C2} reference cannot be set in the 1.5 V low-voltage type, as the maximum operating voltage is 1.7 V.
- Depending on the panel load, when V_{DD} is 2.0 V or lower, the LCD drive voltage does not measure up to the specifications above.

19.4.2 SVD circuit [S1C63004/008/016]

Unless otherwise specified: V_{DD}=1.1 to 1.7V (1.5V type) or V_{DD}=1.8 to 5.5V (3V type), V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS[4:0]=00H		1.05		V
		SVDS[4:0]=01H		1.05		V
		SVDS[4:0]=02H		1.05		V
		SVDS[4:0]=03H		1.05		V
		SVDS[4:0]=04H		1.10		V
		SVDS[4:0]=05H		1.15		V
		SVDS[4:0]=06H		1.20		V
		SVDS[4:0]=07H	Typ. ×	1.25	Typ. ×	V
		SVDS[4:0]=08H	0.97	1.30	1.03	V
		SVDS[4:0]=09H		1.35		V
		SVDS[4:0]=0AH		1.40		V
		SVDS[4:0]=0BH		1.45		V
		SVDS[4:0]=0CH		1.50		V
		SVDS[4:0]=0DH		1.55		V
		SVDS[4:0]=0EH		1.60		V
		SVDS[4:0]=0FH		1.65		V
		SVDS[4:0]=10H		1.70		V
		SVDS[4:0]=11H		1.80		V
		SVDS[4:0]=12H		1.90		V
		SVDS[4:0]=13H		2.00		V
		SVDS[4:0]=14H		2.10		V
		SVDS[4:0]=15H		2.20		V
		SVDS[4:0]=16H		2.30		V
		SVDS[4:0]=17H	Typ. ×	2.40	Typ. ×	V
		SVDS[4:0]=18H	0.97	2.50	1.03	V
		SVDS[4:0]=19H		2.60		V
		SVDS[4:0]=1AH		2.70		V
		SVDS[4:0]=1BH		2.80		V
		SVDS[4:0]=1CH		2.90		V
		SVDS[4:0]=1DH		3.00		V
		SVDS[4:0]=1EH		3.10		V
		SVDS[4:0]=1FH		3.20		V
SVD circuit response time	t_{SVD}		–	–	500	µs

Notes:
- SVD voltages higher than SVDS[4:0]=0FH cannot be set in the 1.5 V low-voltage type, as the maximum operating voltage is 1.7 V.
- SVD voltages lower than SVDS[4:0]=10H cannot be set in the 3 V normal type, as the minimum operating voltage is 1.8 V.

19.4.3 R/F converter circuit

3 V normal type

Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference/sensor oscillation frequencies *1	f_{RFCLK}	Ta=-40 to 85°C	1	–	2,000	kHz
Reference/sensor oscillation frequency/IC deviation *2	$\Delta f_{RFCLK}/\Delta IC$		-40	–	40	%
Reference/sensor resistance	R_{REF}/R_{SEN}		10	–	–	kΩ
Reference capacitor and capacitive sensor capacitance *3	C_{RFC}/C_{SEN}		100	–	2,000	pF
Time base counter clock frequency	f_{TCCLK}		–	–	4.2	MHz

*1 The oscillation frequency/IC deviation characteristic value may increase due to variations in oscillation frequency caused by leakage current if the oscillation frequency is 1 kHz or lower.
*2 In these characteristics, unevenness between production lots, and variations in board, resistances and capacitances used in the measurement environment are taken into account (variations in temperature are not included).
*3 The CR oscillation can be performed if the resistance or capacitance is out of the range shown in the table (see characteristic curves), note, however, that the oscillation frequency/IC deviation characteristic value may increase due to parasitic elements on the board and those in the IC.

1.5 V low-voltage type

Unless otherwise specified: V_{DD}=1.1 to 1.7V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference/sensor oscillation frequencies *1	f_{RFCLK}	Ta=-40 to 85°C	1	–	2,000	kHz
Reference/sensor oscillation frequency/IC deviation *2	$\Delta f_{RFCLK}/\Delta IC$		-40	–	40	%
Reference/sensor resistance	R_{REF}/R_{SEN}		10	–	–	kΩ
Reference capacitor and capacitive sensor capacitance *3	C_{RFC}/C_{SEN}		100	–	2,000	pF
Time base counter clock frequency	f_{TCCLK}		–	–	1	MHz

*1 The oscillation frequency/IC deviation characteristic value may increase due to variations in oscillation frequency caused by leakage current if the oscillation frequency is 1 kHz or lower.
*2 In these characteristics, unevenness between production lots, and variations in board, resistances and capacitances used in the measurement environment are taken into account (variations in temperature are not included).
*3 The CR oscillation can be performed if the resistance or capacitance is out of the range shown in the table (see characteristic curves), note, however, that the oscillation frequency/IC deviation characteristic value may increase due to parasitic elements on the board and those in the IC.

19.4.4 Current consumption

3 V normal type

Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C, C_1–C_6=0.1µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in SLEEP	I_{SLP}	When SLP is executed: OSC1=ON, OSC3=OFF	–	0.1	0.5	µA
Current consumption in HALT	I_{HALT1}	OSC1=32kHz Crystal, OSC3=OFF	–	0.5	1.5	µA
	I_{HALT2} *6	OSC1=32kHz Crystal, OSC3=4MHz Ceramic	–	60	120	µA
	I_{HALT3} *6	OSC1=32kHz Crystal, OSC3=2MHz CR (external R)	–	110	220	µA
	I_{HALT4} *6	OSC1=32kHz Crystal, OSC3=500kHz CR (built-in R)	–	25	55	µA
Current consumption during execution	I_{EXE1}	OSC1=32kHz Crystal, OSC3=OFF, CPUclk=OSC1	–	2.3	4.5	µA
	I_{EXE2} *6	OSC1=32kHz Crystal, OSC3=4MHz Ceramic, CPUclk=OSC3	–	220	440	µA
	I_{EXE3} *6	OSC1=32kHz Crystal, OSC3=2MHz CR (external R), CPUclk=OSC3	–	200	400	µA
	I_{EXE4} *6	OSC1=32kHz Crystal, OSC3=500kHz CR (built-in R), CPUclk=OSC3	–	50	100	µA
	I_{EXE5} *7	OSC1=32kHz Crystal, OSC3=550kHz CR (built-in R), CPUclk=OSC3	–	40	60	µA
Current consumption during execution in heavy load protection mode	I_{EXE1H}	OSC1=32kHz Crystal, OSC3=OFF, CPUclk=OSC1 VDHLMOD=1	–	13	25	µA
LCD circuit current (V_{C1} reference)	I_{LCD1}	DSPC[1:0]=All on, LC[3:0]=FH, OSC1=32kHz, V_{DD}=1.8 to 5.5V, VCREF=0 *1	–	0.45 *4	1.2	µA
LCD circuit current in heavy load protection mode (V_{C1} reference)	I_{LCD1H}	DSPC[1:0]=All on, LC[3:0]=FH, OSC1=32kHz, V_{DD}=1.8 to 5.5V, VCREF=0, VCHLMOD=1 *1	–	13	25	µA

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD circuit current (V_{C2} reference)	I_{LCD2}	DSPC[1:0]=All on, LC[3:0]=FH, OSC1=32kHz, V_{DD}=2.8 to 5.5V, VCREF=1 *1	–	0.40 *5	1.0	µA
LCD circuit current in heavy load protection mode (V_{C2} reference)	I_{LCD2H}	DSPC[1:0]=All on, LC[3:0]=FH, OSC1=32kHz, V_{DD}=2.8 to 5.5V, VCREF=1, VCHLMOD=1 *1	–	25	50	µA
SVD circuit current *6	I_{SVD}	V_{DD}=5.5V *2	–	20	35	µA
R/F converter circuit current	I_{RFC}	V_{DD}=5.5V, C_{REF}=C_{SEN}=1000pF, R_{REF}=R_{SEN}=10kΩ *3	–	350	460	µA

*1 This value is added to the current consumption in HALT mode, current consumption during execution, or current consumption during execution in heavy load protection mode when the LCD circuit is active. Current consumption increases according to the display contents and panel load.

*2 This value is added to the current consumption during execution or current consumption during execution in heavy load protection mode when the SVD circuit is active.

*3 This value is added to the current consumption during execution when the R/F converter circuit is active.

*4 The LCD circuit current depends on the number of the segments used.
Examples for reference: S1C63003 - 10 segments × 5 commons 0.25µA
S1C63004 - 20 segments × 8 commons 0.45µA
S1C63008 - 30 segments × 8 commons 0.55µA
S1C63016 - 36 segments × 8 commons 0.60µA

*5 The LCD circuit current depends on the number of the segments used.
Examples for reference: S1C63003 - 10 segments × 5 commons 0.20µA
S1C63004 - 20 segments × 8 commons 0.40µA
S1C63008 - 30 segments × 8 commons 0.45µA
S1C63016 - 36 segments × 8 commons 0.48µA

*6 S1C63004/008/016

*7 S1C63003 only

1.5 V low-voltage type

Unless otherwise specified: V_{DD}=1.1 to 1.7V, V_{SS}=0V, Ta=25°C, C_1–C_6=0.1µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in SLEEP	I_{SLP}	When SLP is executed: OSC1=ON, OSC3=OFF	–	0.1	0.5	µA
Current consumption in HALT	I_{HALT1}	OSC1=32kHz Crystal, OSC3=OFF	–	0.5	1.5	µA
	I_{HALT2} *5	OSC1=32kHz Crystal, OSC3=1MHz Ceramic	–	15	30	µA
	I_{HALT3} *5	OSC1=32kHz Crystal, OSC3=500kHz CR (external R)	–	22	50	µA
	I_{HALT4} *5	OSC1=32kHz Crystal, OSC3=500kHz CR (built-in R)	–	10	22	µA
Current consumption during execution	I_{EXE1}	OSC1=32kHz Crystal, OSC3=OFF, CPUclk=OSC1	–	2.0	4.5	µA
	I_{EXE2} *5	OSC1=32kHz Crystal, OSC3=1MHz Ceramic, CPUclk=OSC3	–	60	120	µA
	I_{EXE3} *5	OSC1=32kHz Crystal, OSC3=500kHz CR (external R), CPUclk=OSC3	–	40	80	µA
	I_{EXE4} *5	OSC1=32kHz Crystal, OSC3=500kHz CR (built-in R), CPUclk=OSC3	–	30	60	µA
	I_{EXE5} *6	OSC1=32kHz Crystal, OSC3=550kHz CR (built-in R), CPUclk=OSC3	–	30	50	µA
Current consumption during execution in heavy load protection mode	I_{EXE1H}	OSC1=32kHz Crystal, OSC3=OFF, CPUclk=OSC1 VDHLMOD=1	–	11	22	µA
LCD circuit current (V_{C1} reference)	I_{LCD1}	DSPC[1:0]=All on, LC[3:0]=FH, OSC1=32kHz, V_{DD}=1.1 to 1.7V, VCREF=0 *1	–	0.45 *4	1.2	µA
LCD circuit current in heavy load protection mode (V_{C1} reference)	I_{LCD1H}	DSPC[1:0]=All on, LC[3:0]=FH, OSC1=32kHz, V_{DD}=1.1 to 1.7V, VCREF=0, VCHLMOD=1 *1	–	13	25	µA
SVD circuit current *5	I_{SVD}	V_{DD}=1.7V *2	–	8	15	µA
R/F converter circuit current	I_{RFC}	V_{DD}=1.7V, C_{REF}=C_{SEN}=1000pF, R_{REF}=R_{SEN}=10kΩ *3	–	120	160	µA

*1 This value is added to the current consumption in HALT mode, current consumption during execution, or current consumption during execution in heavy load protection mode when the LCD circuit is active. Current consumption increases according to the display contents and panel load.

*2 This value is added to the current consumption during execution or current consumption during execution in heavy load protection mode when the SVD circuit is active.

*3 This value is added to the current consumption during execution when the R/F converter circuit is active.

*4 The LCD circuit current depends on the number of the segments used.
Examples for reference: S1C63003 - 10 segments × 5 commons 0.25µA
S1C63004 - 20 segments × 8 commons 0.45µA
S1C63008 - 30 segments × 8 commons 0.55µA
S1C63016 - 36 segments × 8 commons 0.60µA

*5 S1C63004/008/016

*6 S1C63003 only

19.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified: V_{DD}=1.1 to 5.5V, V_{SS}=0V, Ta=25°C, Crystal resonator=C-002RX (R_1=30kΩ Typ., C_L=12.5pF), C_{G1}=25pF (external), C_{D1}=Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}		–	–	3	s
External gate capacitance	C_{G1}	Including the board capacitance	0	–	25	pF
Built-in drain capacitance	C_{D1}	In case of the chip	–	20	–	pF
Frequency/IC deviation	$\Delta f/\Delta IC$	V_{DD}=constant	-10	–	10	ppm
Frequency/voltage deviation	$\Delta f/\Delta V$		–	–	1	ppm/V
Frequency adjustment range	$\Delta f/\Delta C_G$	V_{DD}=constant, C_G=0 to 25pF	25	–	–	ppm

OSC3 ceramic oscillation circuit [S1C63004/008/016]

3 V normal type

Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C, C_{G3}=C_{D3}=30pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}		–	–	1	ms

1.5 V low-voltage type

Unless otherwise specified: V_{DD}=1.1 to 1.7V, V_{SS}=0V, Ta=25°C, C_{G3}=C_{D3}=30pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}		–	–	3	ms

OSC3 CR oscillation circuit (external R type) [S1C63004/008/016]

3 V normal type

Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}		–	–	1	ms
Frequency/IC deviation	$\Delta f/\Delta IC$	R_{CR}=constant	-25	–	25	%

1.5 V low-voltage type

Unless otherwise specified: V_{DD}=1.1 to 1.7V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}		–	–	1	ms
Frequency/IC deviation	$\Delta f/\Delta IC$	R_{CR}=constant	-33	–	33	%

OSC3 CR oscillation circuit (built-in R type) [S1C63004/008/016]

Unless otherwise specified: V_{DD}=1.1 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}		Typ. × 0.75	500	Typ. × 1.25	kHz
Oscillation start time	t_{sta}		–	–	20	µs

OSC3 CR oscillation circuit (built-in R type) [S1C63003]

Unless otherwise specified: V_{DD}=1.1 to 5.5V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}		Typ. × 0.75	550	Typ. × 1.25	kHz
Oscillation start time	t_{sta}		–	–	20	µs

19.6 Serial Interface AC Characteristics [S1C63004/008/016]

Master mode

Unless otherwise specified: V_{DD}=1.5V (1.5V type) or 3.0V (3V type), V_{SS}=0V, Ta=-40 to 85°C, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	t_{SMD}	–	–	200	ns
Receive data input set-up time	t_{SMS}	400	–	–	ns
Receive data input hold time	t_{SMH}	200	–	–	ns

Note that the maximum clock frequency is limited to 1 MHz.

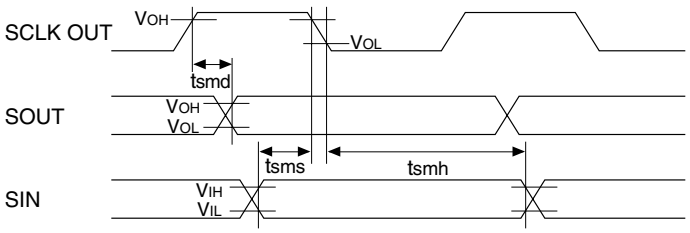
Slave mode

Unless otherwise specified: V_{DD}=1.5V (1.5V type) or 3.0V (3V type), V_{SS}=0V, Ta=-40 to 85°C, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

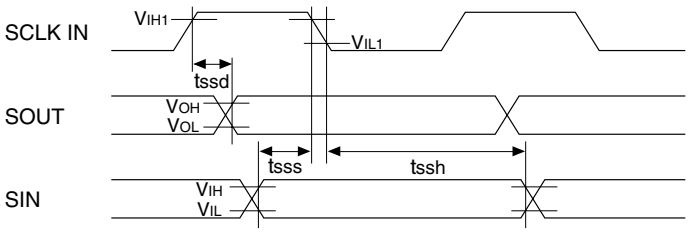
Item	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	t_{SSD}	–	–	200	ns
Receive data input set-up time	t_{SSS}	400	–	–	ns
Receive data input hold time	t_{SSH}	200	–	–	ns

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

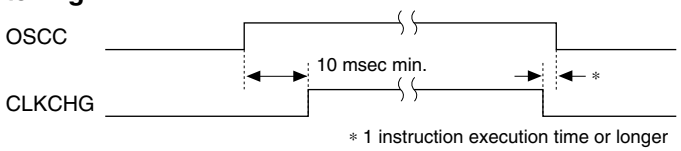


<Slave mode>



19.7 Timing Chart

System clock switching



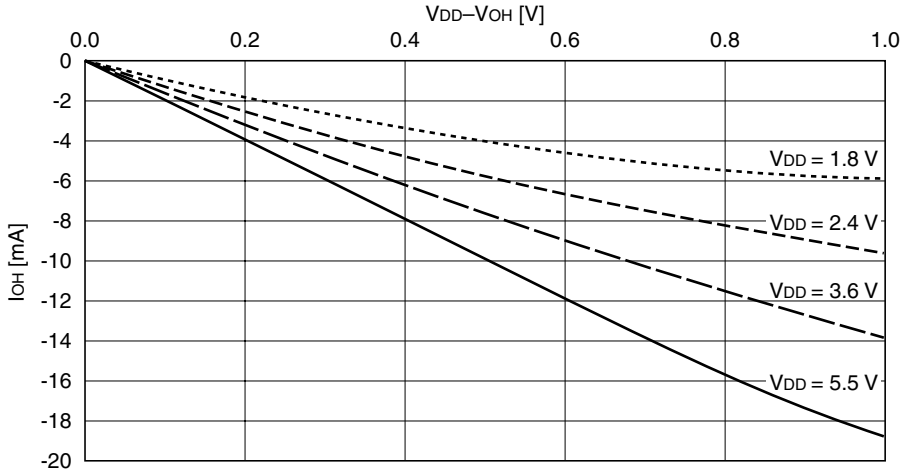
* 1 instruction execution time or longer

19.8 Characteristics Curves (reference value)

High level output current-voltage characteristic

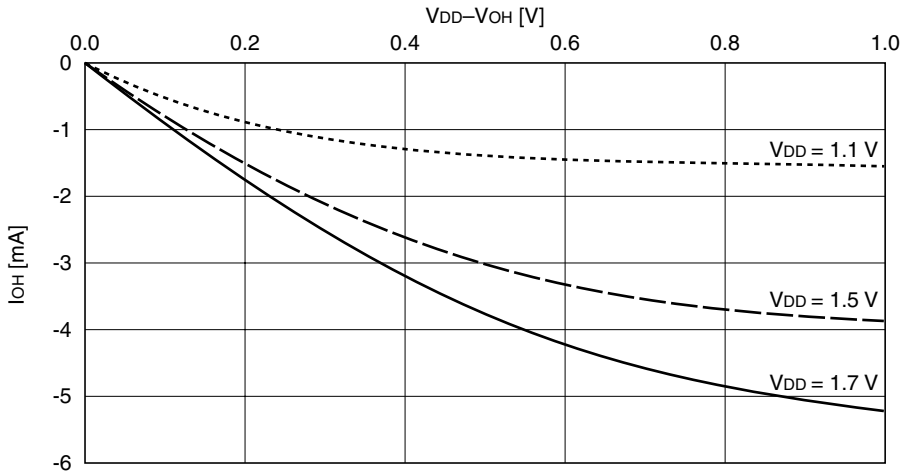
3 V normal type

Ta = 85°C, Max. value



1.5 V low-voltage type

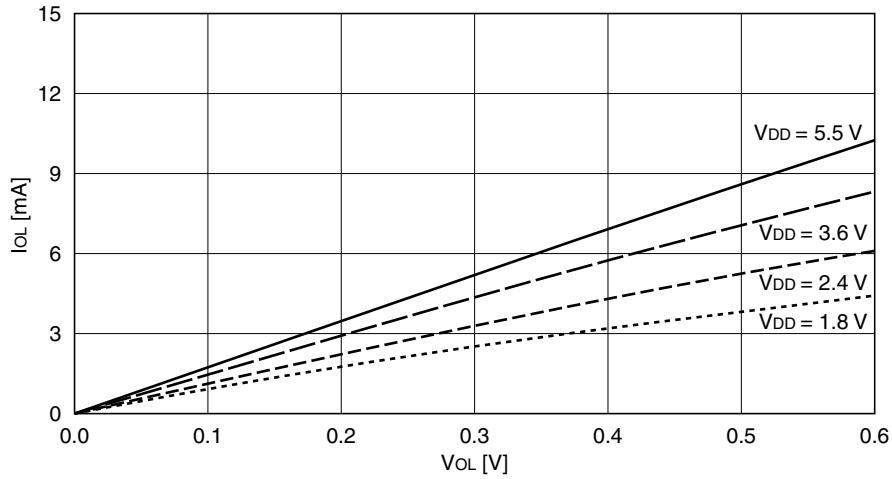
Ta = 85°C, Max. value



Low level output current-voltage characteristic

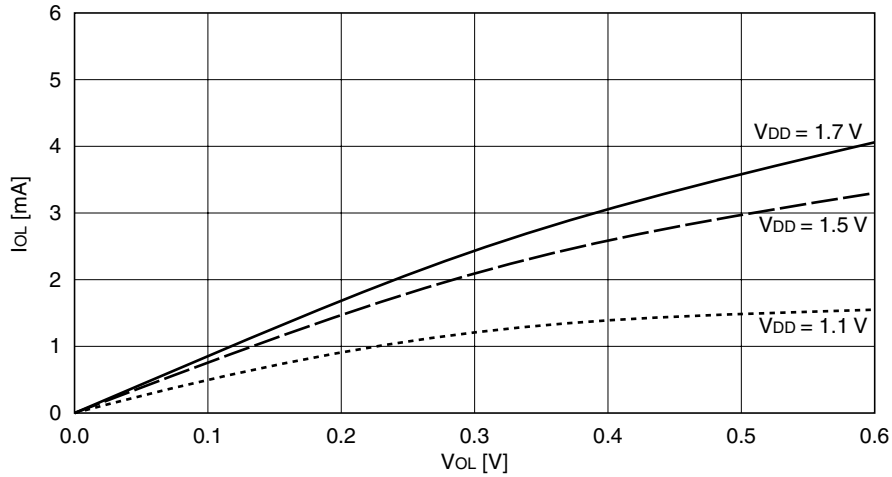
3 V normal type

Ta = 85°C, Min. value



1.5 V low-voltage type

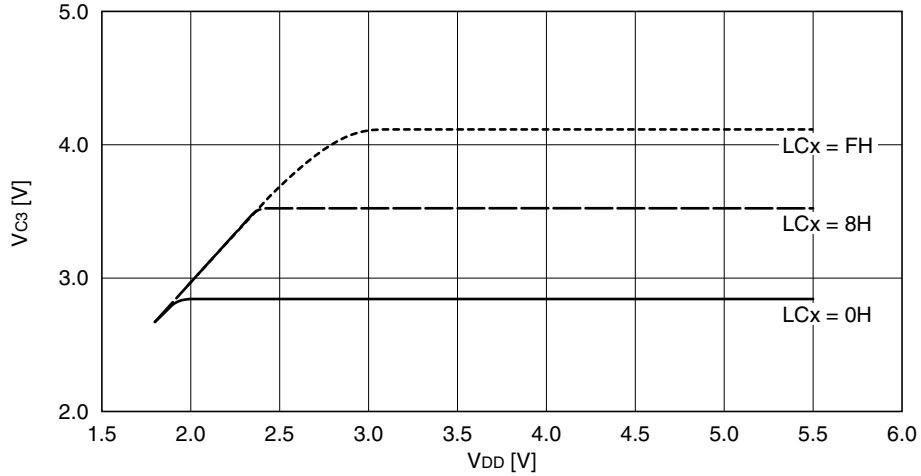
Ta = 85°C, Min. value



LCD drive voltage - supply voltage characteristic (1/3 bias, V_{C2} reference) [S1C63004/008/016]

3 V normal type

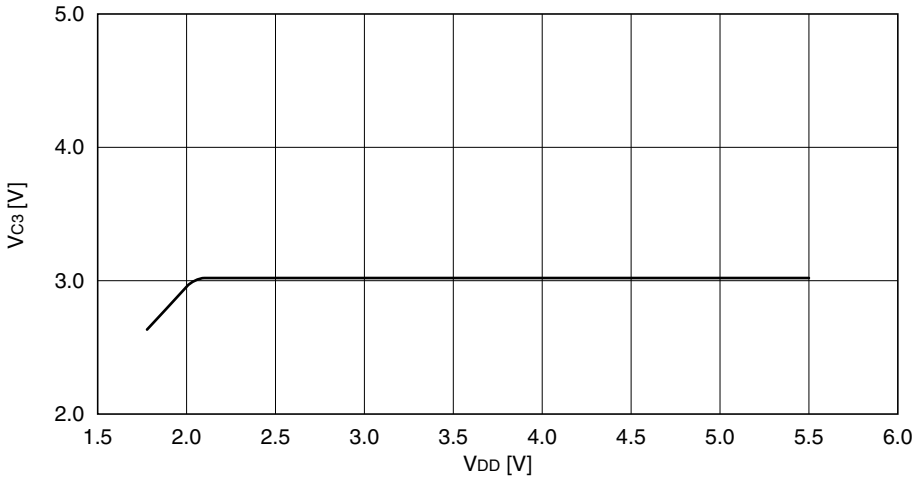
Ta = 25°C, Typ. value



LCD drive voltage - supply voltage characteristic (1/3 bias, V_{C2} reference) [S1C63003]

3 V normal type

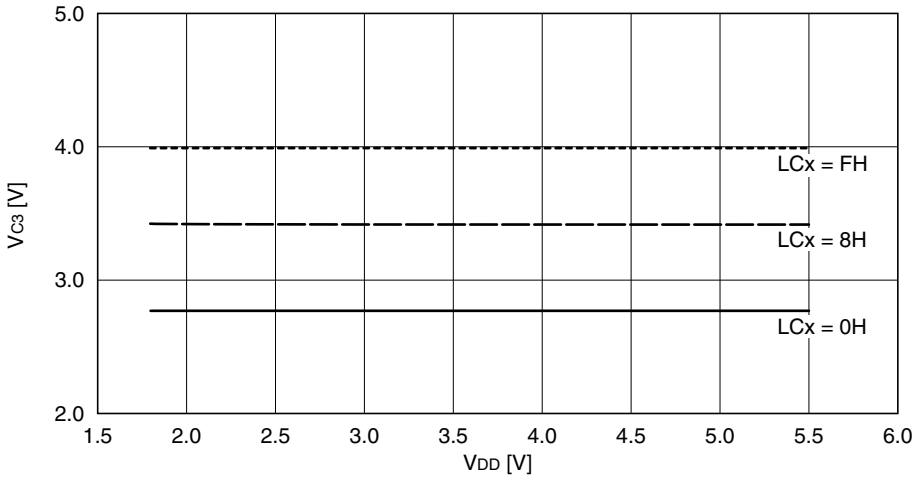
Ta = 25°C, Typ. value



LCD drive voltage - supply voltage characteristic (1/3 bias, V_{C1} reference) [S1C63004/008/016]

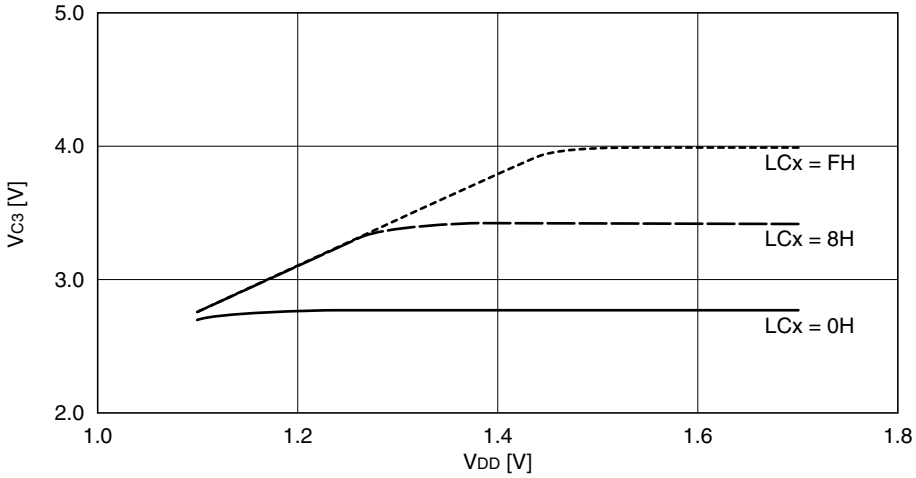
3 V normal type

Ta = 25°C, Typ. value



1.5 V low-voltage type

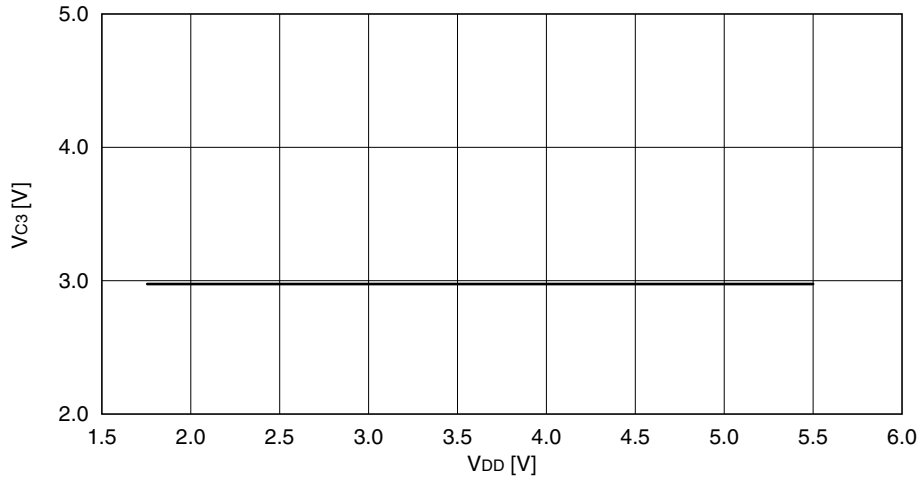
Ta = 25°C, Typ. value



LCD drive voltage - supply voltage characteristic (1/3 bias, V_{C1} reference) [S1C63003]

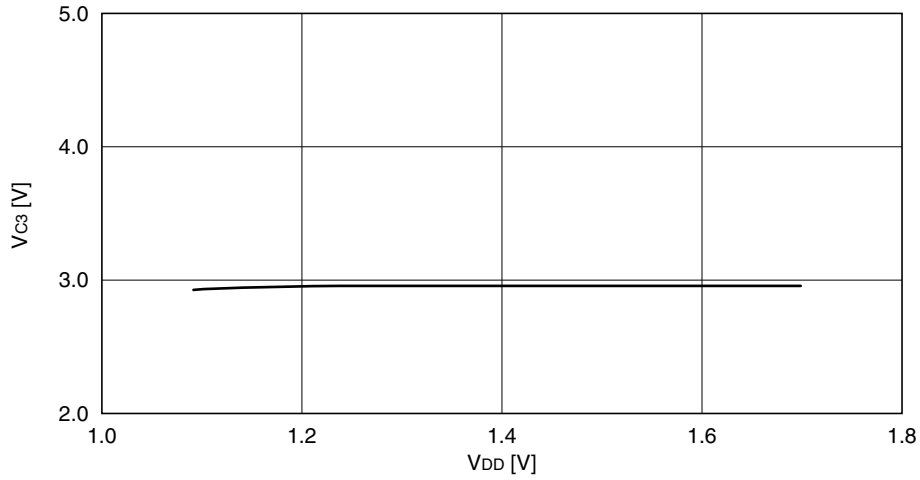
3 V normal type

Ta = 25°C, Typ. value



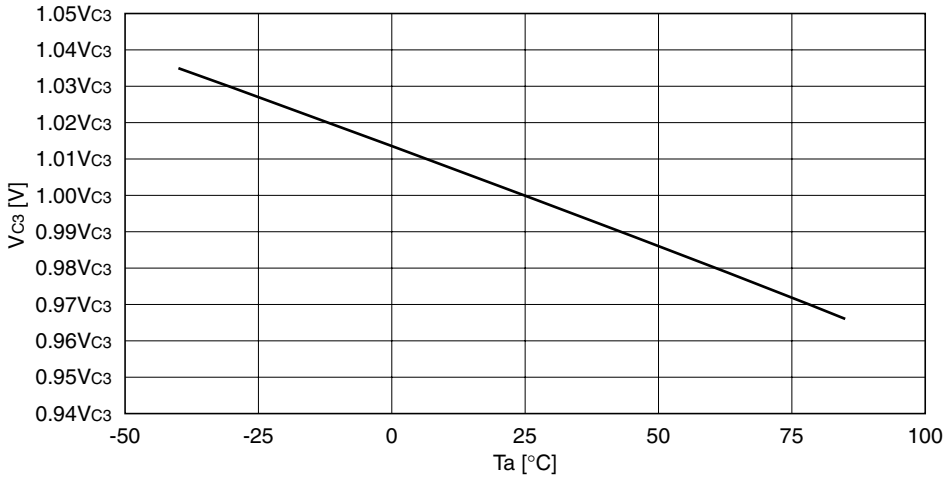
1.5 V low-voltage type

Ta = 25°C, Typ. value



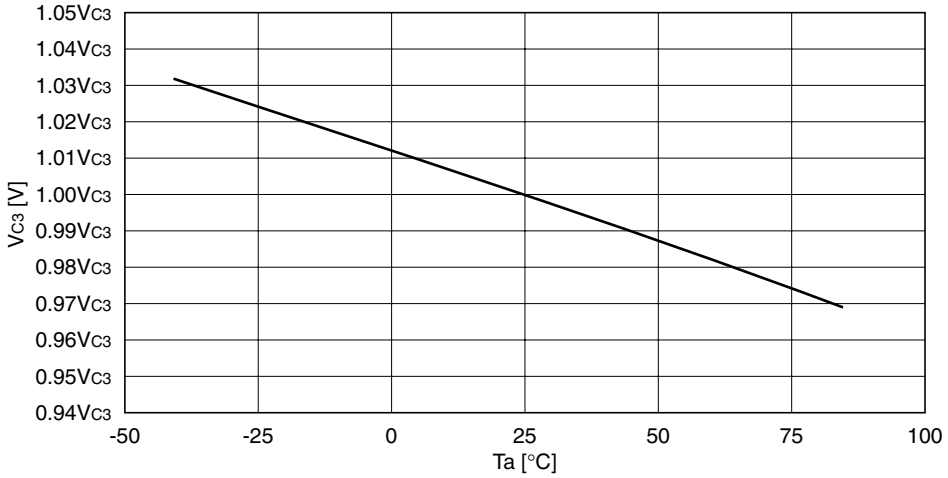
LCD drive voltage - ambient temperature characteristic (1/3 bias, V_{C2}/V_{C1} reference) [S1C63004/008/016]

V_{DD} = 3.0 V, Typ. value



LCD drive voltage - ambient temperature characteristic (1/3 bias, V_{C2}/V_{C1} reference) [S1C63003]

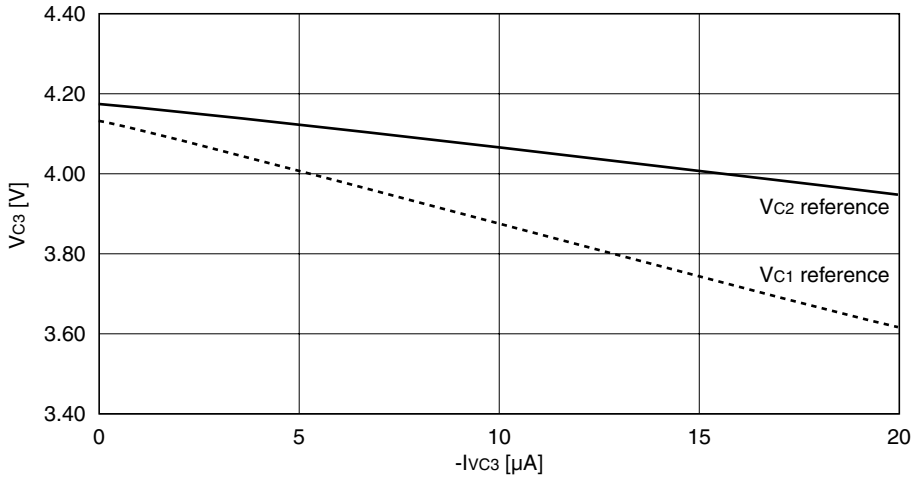
V_{DD} = 3.6 V, Typ. value



LCD drive voltage - load characteristic (1/3 bias) [S1C63004/008/016]

When a load is connected to V_{C3} terminal only

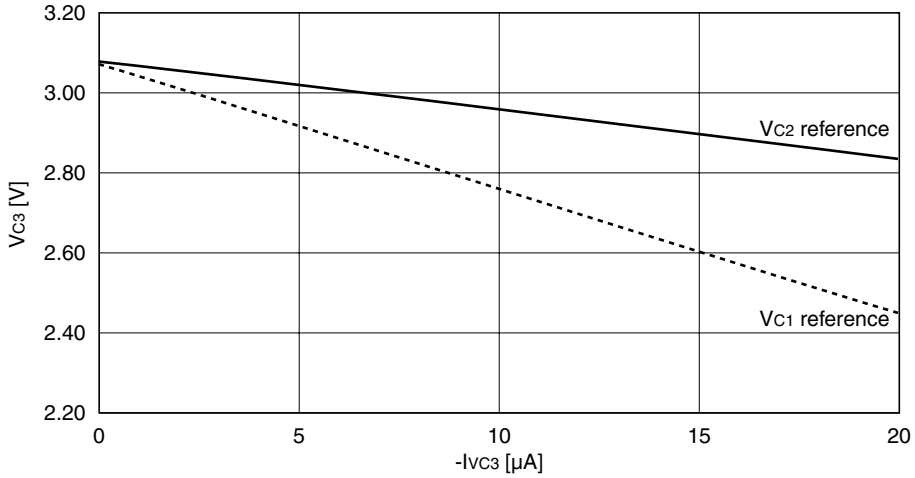
LCx = FH, Ta = 25°C, Typ. value



LCD drive voltage - load characteristic (1/3 bias) [S1C63003]

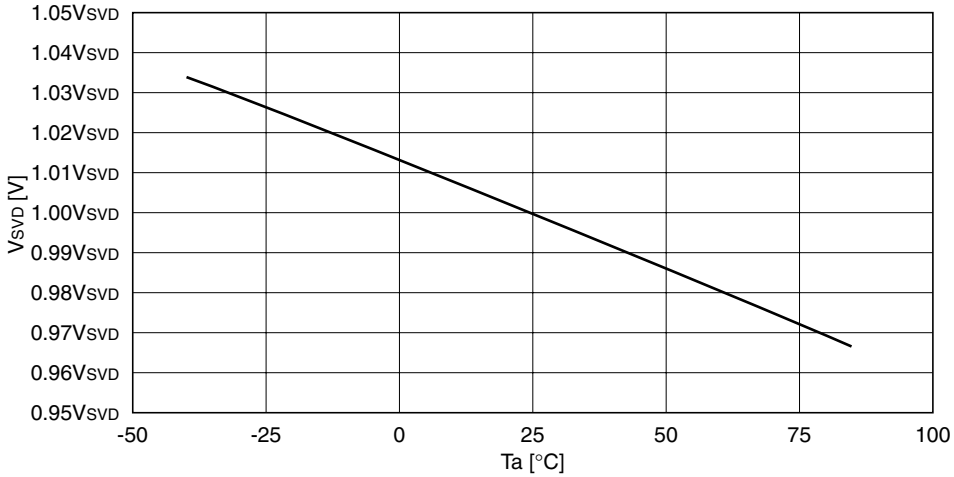
When a load is connected to V_{C3} terminal only

Ta = 25°C, Typ. value



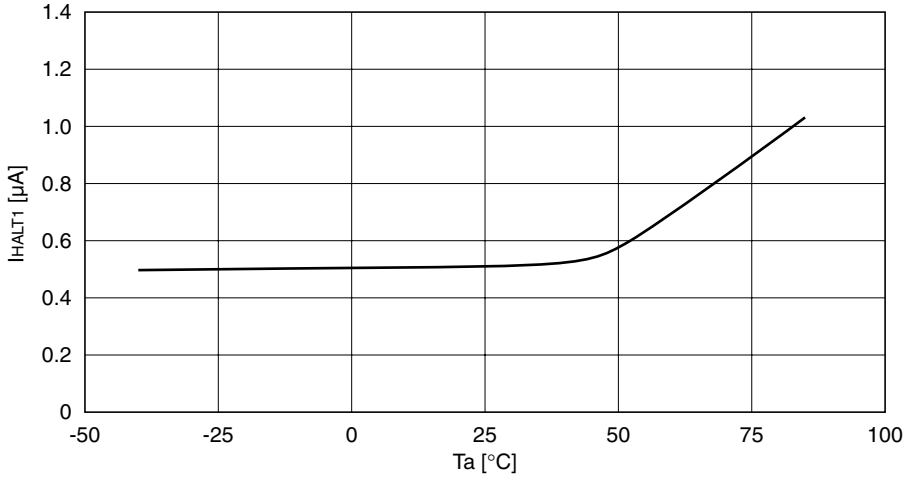
SVD voltage - ambient temperature characteristic [S1C63004/008/016]

SVDSx = FH, Typ. value



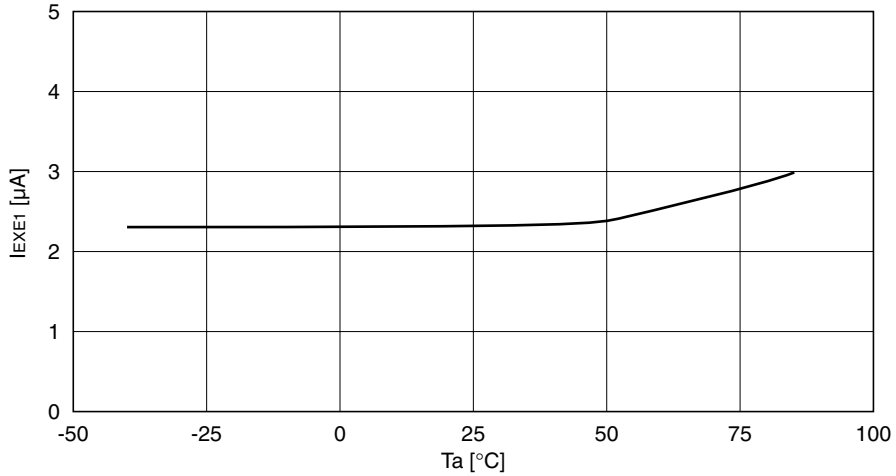
HALT state current consumption - temperature characteristic (during operation with OSC1)

<Crystal oscillation, fosc1 = 32.768 kHz> VDD = 5.5 V, OSC3 = OFF, Clock manager = OFF, Typ. value



RUN state current consumption - temperature characteristic (during operation with OSC1)

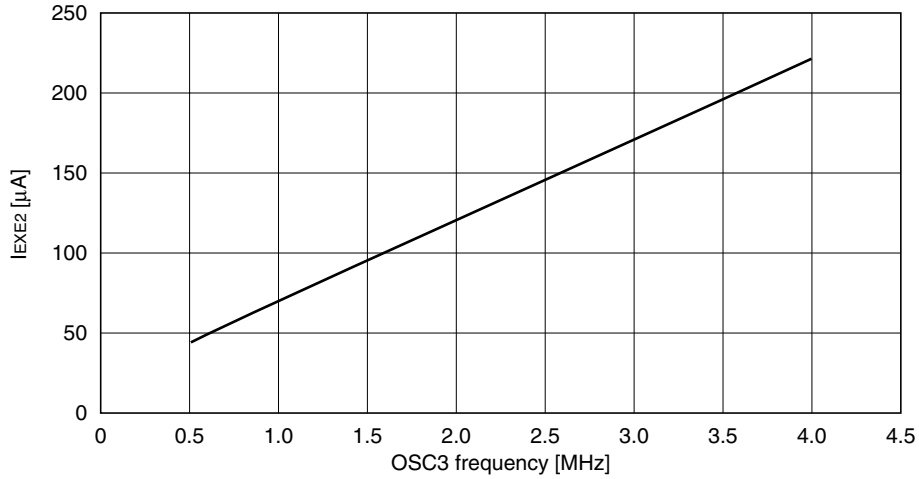
<Crystal oscillation, fosc1 = 32.768 kHz> VDD = 5.5 V, OSC3 = OFF, Clock manager = OFF, Typ. value



RUN state current consumption - frequency characteristic (during operation with OSC3)

<Ceramic oscillation> [S1C63004/008/016]

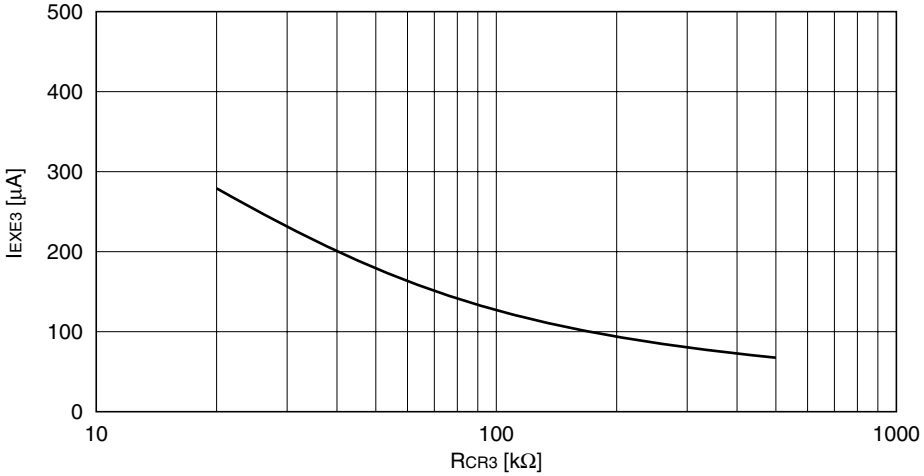
V_{DD} = 5.5 V, Ta = 25°C, Typ. value



RUN state current consumption - resistor characteristic (during operation with OSC3)

<CR oscillation (external R)> [S1C63004/008/016]

V_{DD} = 5.5 V, Ta = 25°C, Typ. value

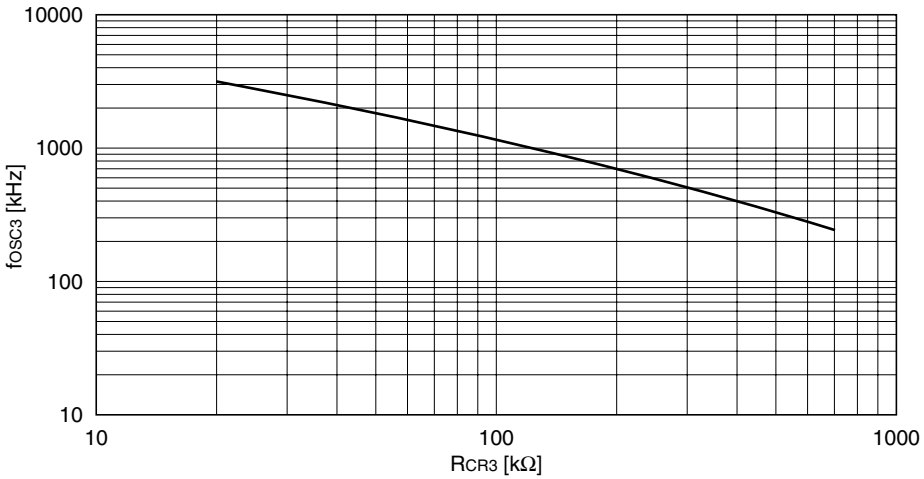


Oscillation frequency - resistor characteristic (OSC3)

<CR oscillation (external R)> [S1C63004/008/016]

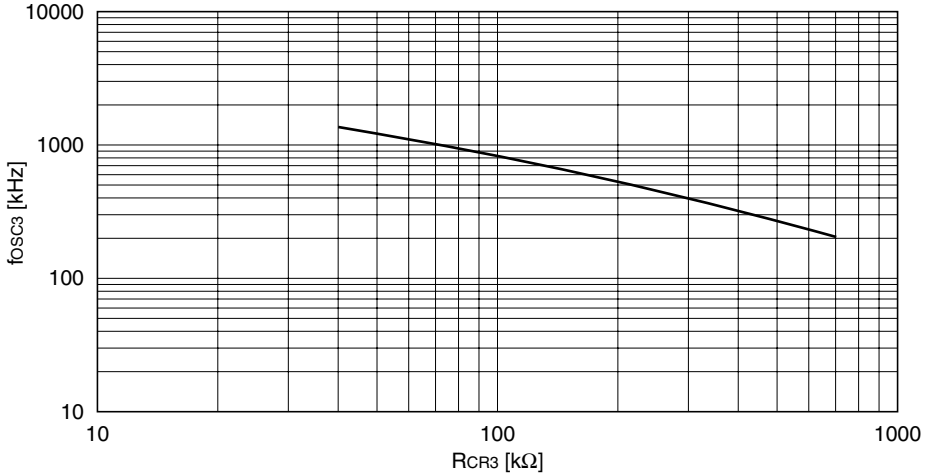
3 V normal type

V_{DD} = 5.5 V, Ta = 25°C, Typ. value



1.5 V low-voltage type

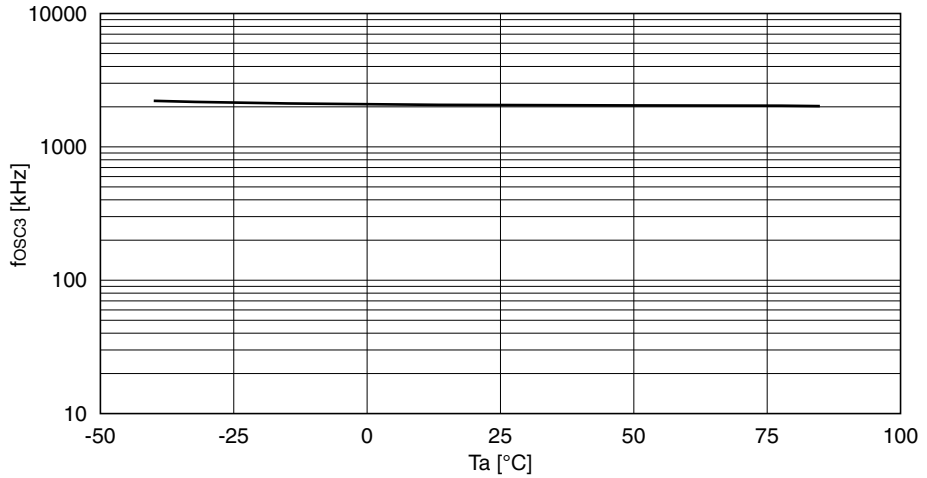
V_{DD} = 1.7 V, Ta = 25°C, Typ. value



Oscillation frequency - temperature characteristic (OSC3)

<CR oscillation (external R)> [S1C63004/008/016]

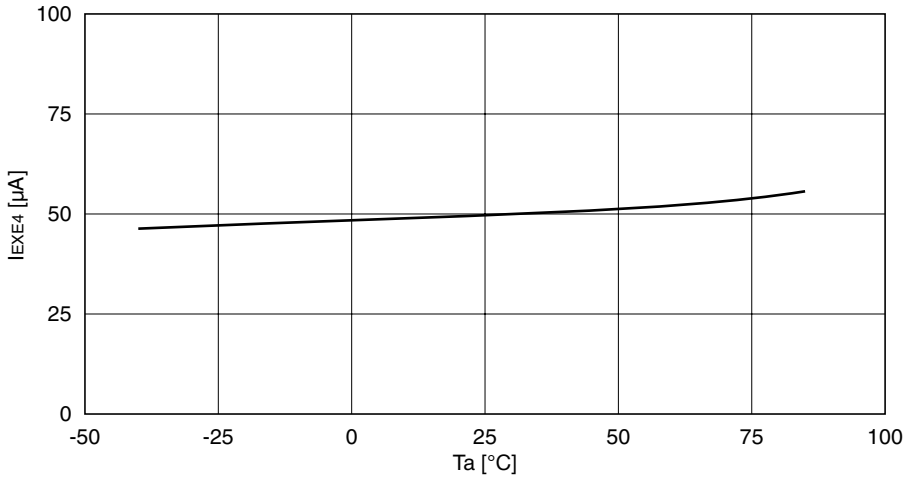
R_{CR3} = 40 kΩ, Typ. value



RUN state current consumption - temperature characteristic (during operation with OSC3)

<CR oscillation (built-in R)> [S1C63004/008/016]

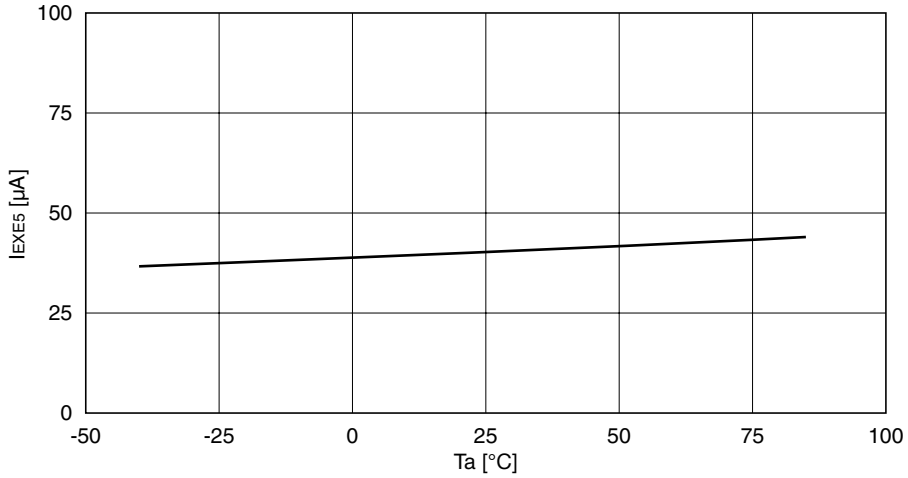
V_{DD} = 5.5 V, Typ. value



RUN state current consumption - temperature characteristic (during operation with OSC3)

<CR oscillation (built-in R)> [S1C63003]

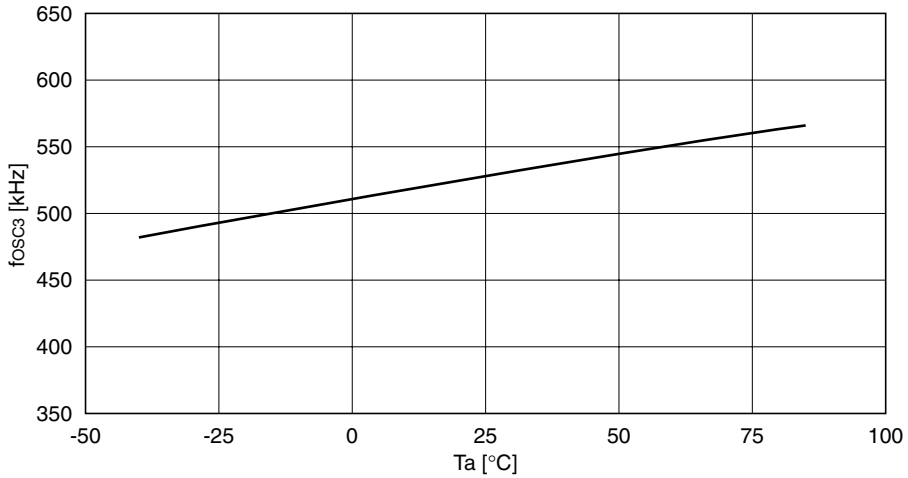
V_{DD} = 5.5 V, Typ. value



Oscillation frequency - temperature characteristic (OSC3)

<CR oscillation (built-in R)> [S1C63004/008/016]

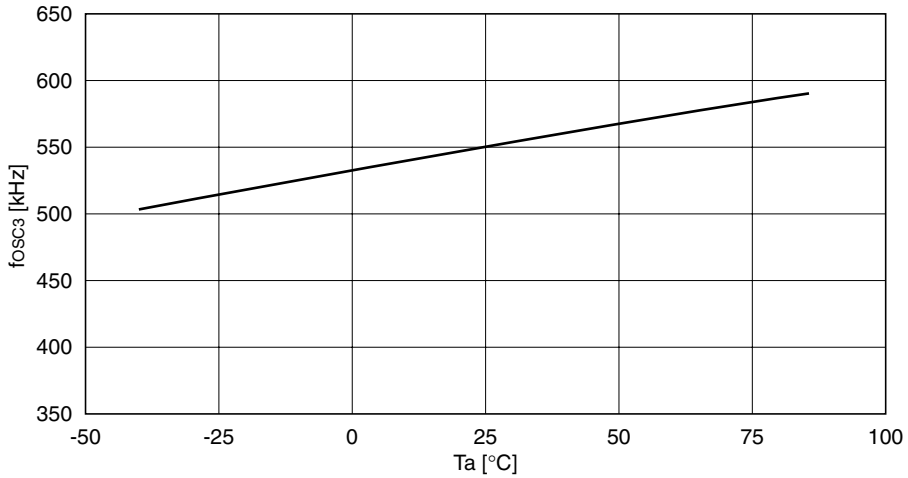
V_{DD} = 5.5 V, Typ. value



Oscillation frequency - temperature characteristic (OSC3)

<CR oscillation (built-in R)> [S1C63003]

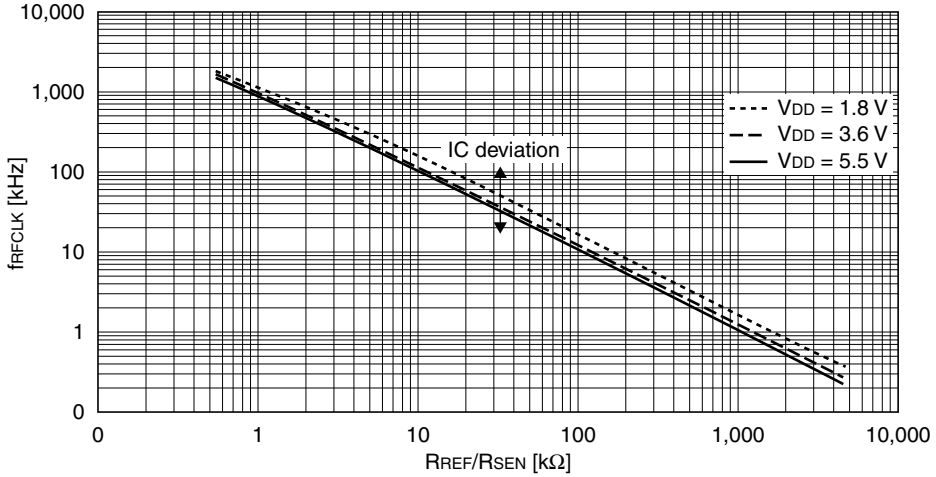
V_{DD} = 5.5 V, Typ. value

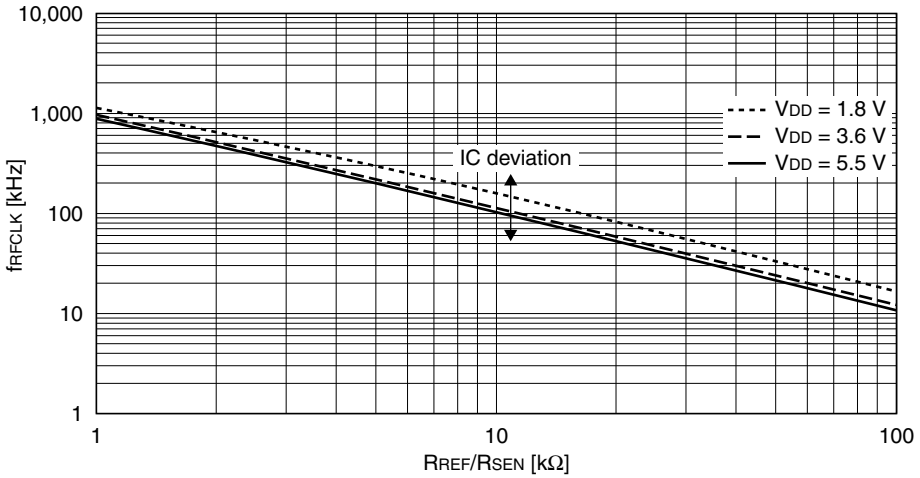


RFC reference/sensor oscillation frequency - resistance characteristic (DC oscillation mode)

3 V normal type

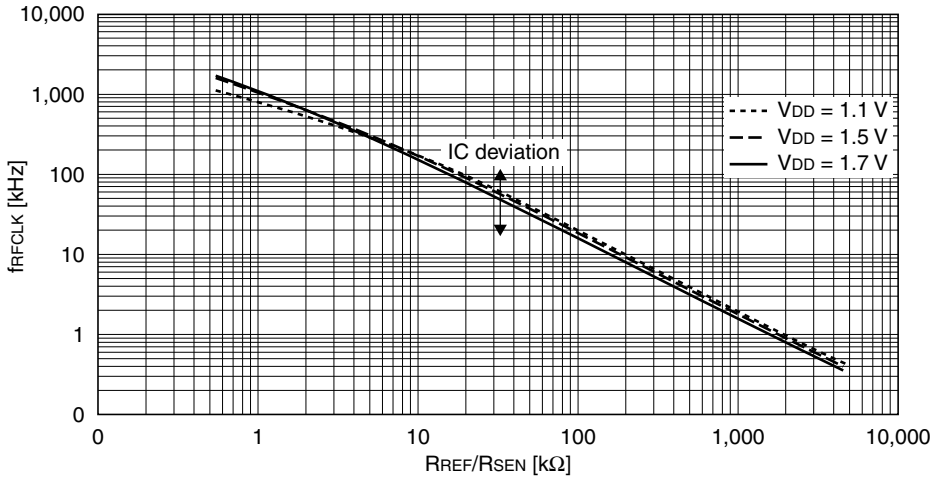
C_{SEN} = 1000 pF, Ta = 25°C, Typ. value

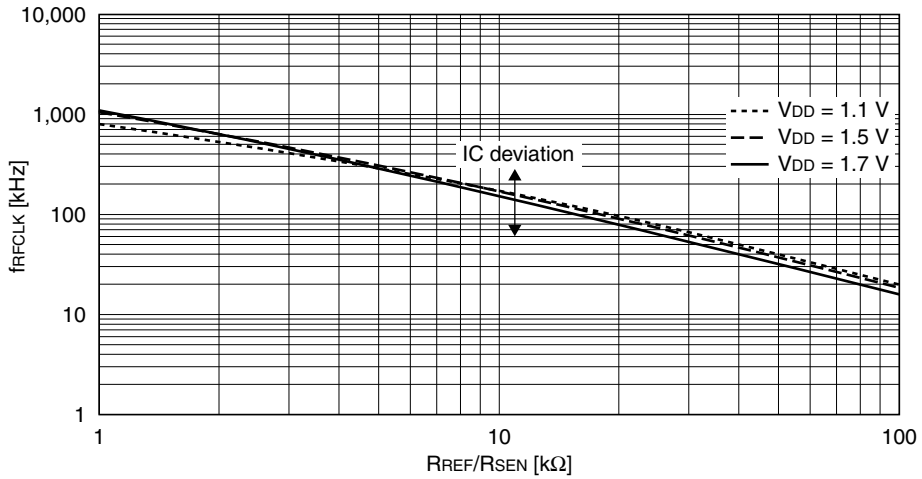




1.5 V low-voltage type

C_{SEN} = 1000 pF, Ta = 25°C, Typ. value

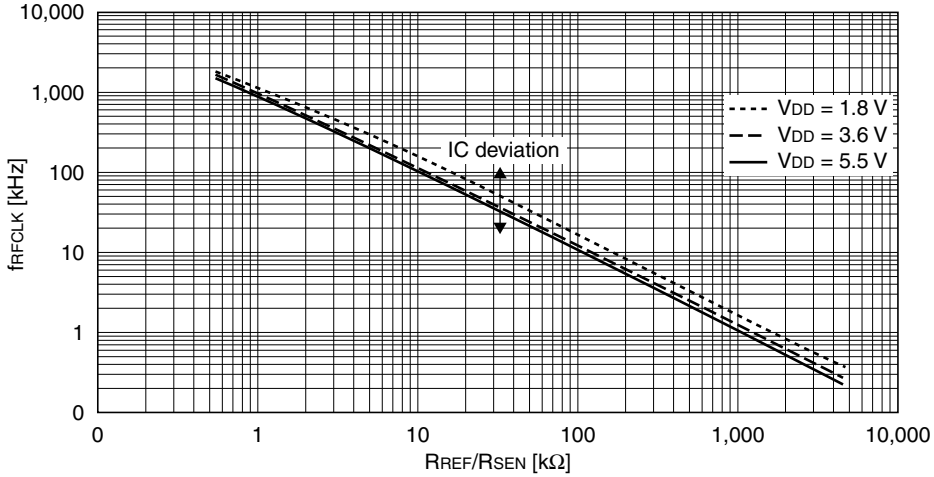


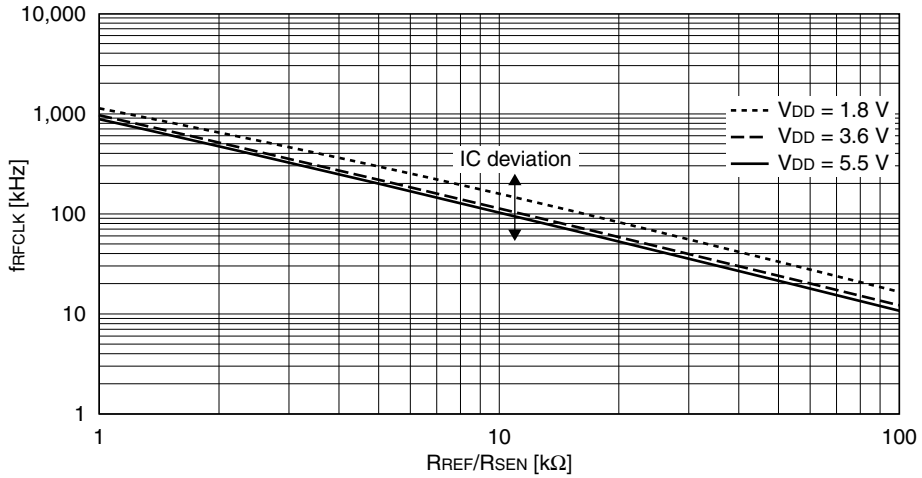


RFC reference/sensor oscillation frequency - resistance characteristic (AC oscillation mode)

3 V normal type

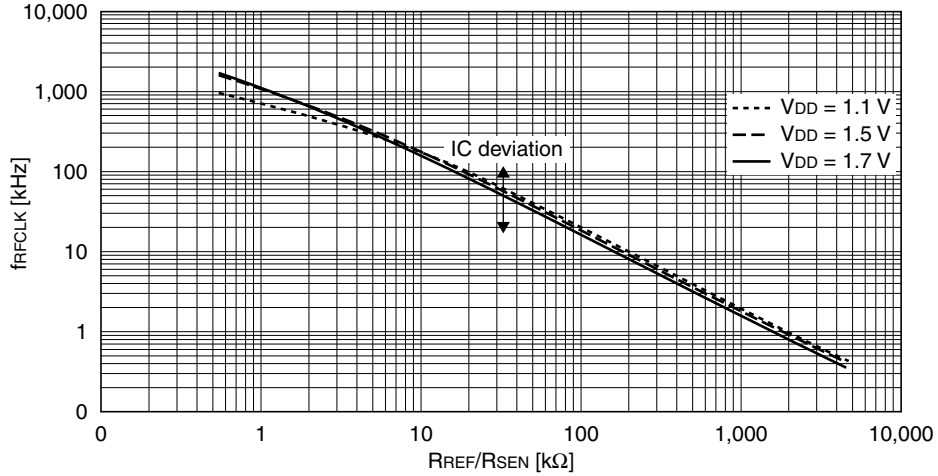
CSEN = 1000 pF, Ta = 25°C, Typ. value

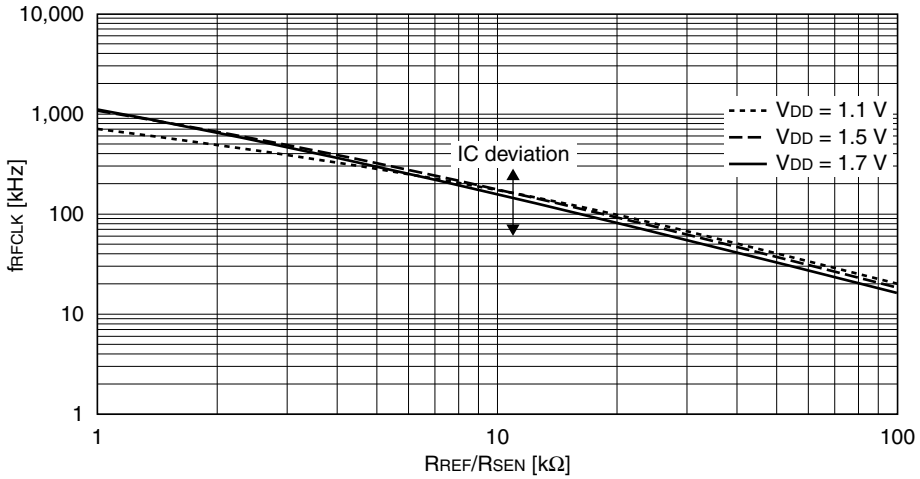




1.5 V low-voltage type

C_{SEN} = 1000 pF, Ta = 25°C, Typ. value

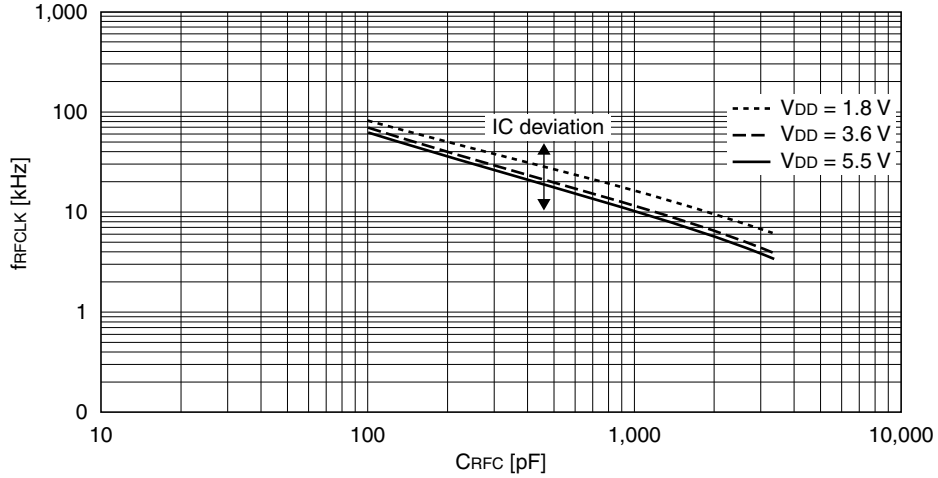




RFC reference/sensor oscillation frequency - capacitance characteristic (DC/AC oscillation mode)

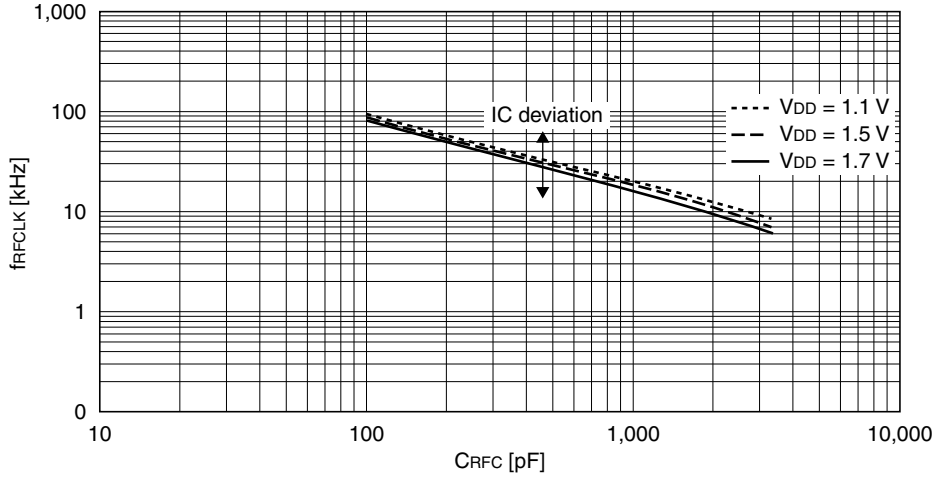
3 V normal type

R_{SEN} = 100 kΩ, Ta = 25°C, Typ. value



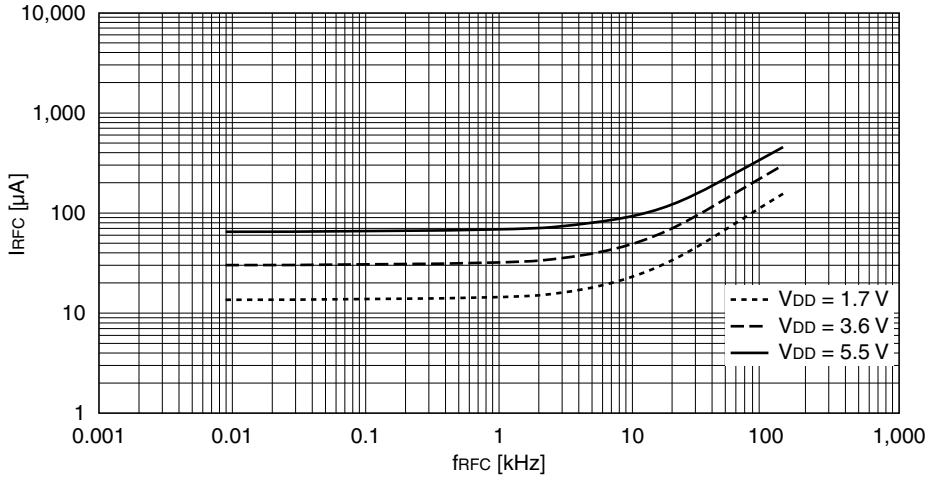
1.5 V low-voltage type

R_{SEN} = 100 kΩ, Ta = 25°C, Typ. value

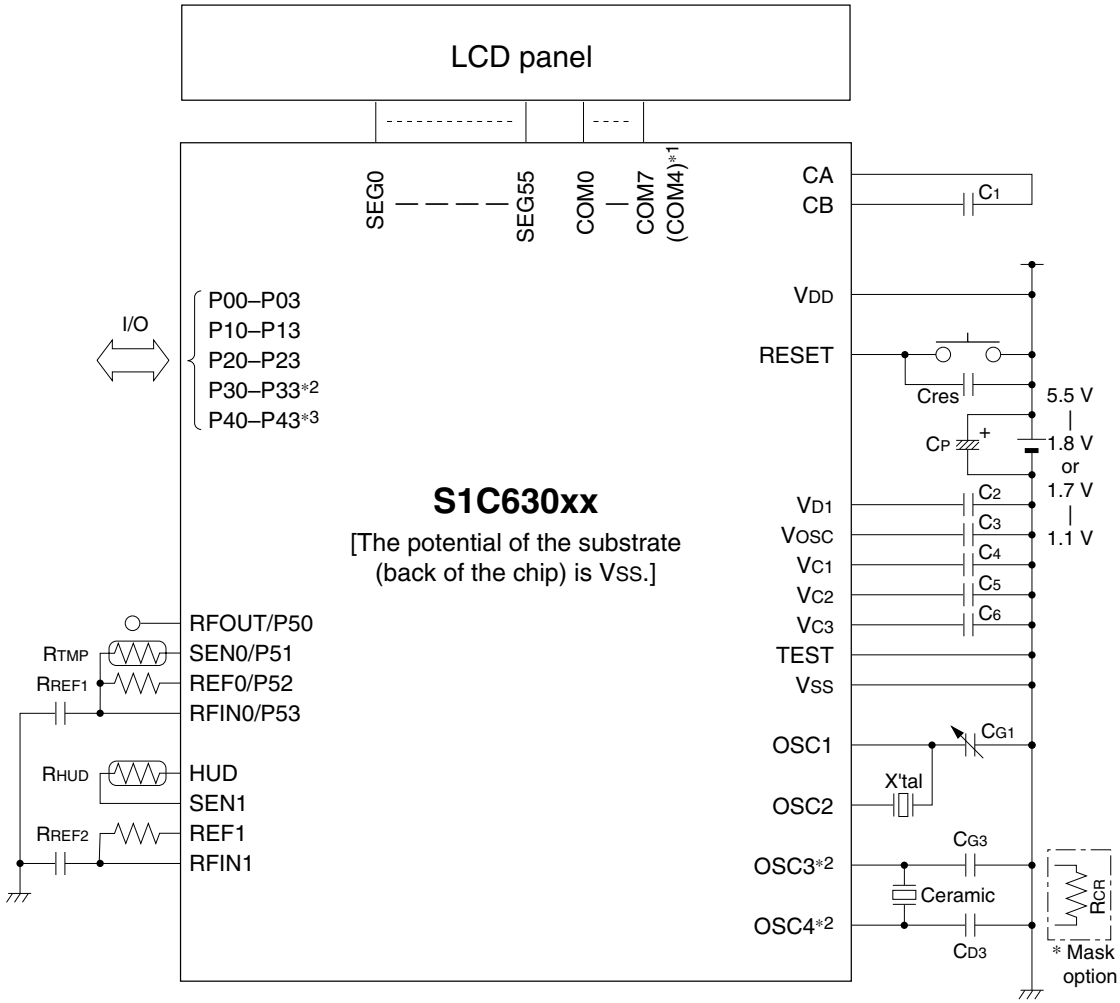


RFC reference/sensor oscillation frequency - current consumption characteristic (DC/AC oscillation mode)

C_{RFC} = 1000 pF, Ta = 25°C, Typ. value



20 Basic External Wiring Diagram



Recommended values for external parts

Symbol	Name	Recommended value
X'tal	Crystal resonator	32.768 kHz
C_{G1}	Trimmer capacitor	0 to 25 pF
Ceramic *4	Ceramic resonator	4 MHz (3 V model) 1 MHz (1.5 V model)
C_{G3}*4	Gate capacitor	30 pF (Ceramic oscillation)
C_{D3}*4	Drain capacitor	30 pF (Ceramic oscillation)
C_1	Booster capacitor	0.1 µF
C_2	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{OSC}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for RESET terminal	0.47 µF

*1: S1C63003
*2: Not available in the S1C63003
*3: Not available in the S1C63003/004
*4: Not used in the S1C63003

Note: The values in the above table are shown only for reference and not guaranteed.

Appendix A List of I/O Registers

∗1 Initial value at initial reset ∗2 Not set in the circuit ∗3 Constantly "0" when being read
∗4 Unused in the S1C63003/004/008 ∗5 Unused in the S1C63003/004 ∗6 Unused in the S1C63003

FF00H Oscillation Circuit

Address		Register name	R/W	Default	Setting/data				Function
FF00H	D3	**CLKCHG**	R/W	0	1	OSC3	0	OSC1	CPU clock switch
	D2	**OSCC**	R/W	0	1	On	0	Off	OSC3 oscillation On/Off
	D1	0 (∗3)	R	– (∗2)	–				Unused
	D0	0 (∗3)	R	– (∗2)	–				Unused

FF01H Watchdog Timer

Address		Register name	R/W	Default	Setting/data				Function
FF01H	D3	0 (∗3)	R	– (∗2)	–				Unused
	D2	0 (∗3)	R	– (∗2)	–				Unused
	D1	**WDEN**	R/W	1	1	Enable	0	Disable	Watchdog timer enable
	D0	**WDRST** (∗3)	W	(Reset)	1	Reset	0	Invalid	Watchdog timer reset (writing)

FF02H–FF03H Power Supply Circuit

Address		Register name	R/W	Default	Setting/data				Function
FF02H	D3	**VDSEL**	R/W	0	1	1	0	0	General-purpose register
	D2	**VCSEL**	R/W	0	1	1	0	0	General-purpose register
	D1	**HLON**	R/W	0	1	1	0	0	General-purpose register
	D0	**DBON**	R/W	0	1	1	0	0	General-purpose register
FF03H	D3	**VCHLMOD**	R/W	0	1	On	0	Off	V_C regulator heavy load protection mode On/Off
	D2	**VDHLMOD**	R/W	0	1	On	0	Off	V_D regulator heavy load protection mode On/Off
	D1	**VCREF** (∗6)	R/W	0	1	V_{C2}	0	V_{C1}	V_C regulator reference voltage selection
	D0	**LPWR**	R/W	0	1	On	0	Off	V_C regulator On/Off

FF04H–FF05H SVD Circuit

Address		Register name	R/W	Default	Setting/data														Function
FF04H (∗6)	D3	**SVDS3**	R/W	0	1F	3.20	1A	2.70	15	2.20	10	1.70	B	1.45	6	1.20	1	1.05	SVD criteria voltage (V) setting ← SVDS[4:0]
	D2	**SVDS2**	R/W	0	1E	3.10	19	2.60	14	2.10	F	1.65	A	1.40	5	1.15	0	1.05	
	D1	**SVDS1**	R/W	0	1D	3.00	18	2.50	13	2.00	E	1.60	9	1.35	4	1.10			
	D0	**SVDS0**	R/W	0	1C	2.90	17	2.40	12	1.90	D	1.55	8	1.30	3	1.05			
					1B	2.80	16	2.30	11	1.80	C	1.50	7	1.25	2	1.05			
FF05H (∗6)	D3	0 (∗3)	R	– (∗2)	–														Unused
	D2	**SVDS4**	R/W	0	(See FF04H)														SVD criteria voltage (V) setting
	D1	**SVDDT**	R	0	1	Low	0	Normal											SVD evaluation data
	D0	**SVDON**	R/W	0	1	On	0	Off											SVD circuit On/Off

FF10H–FF1BH Clock Manager

Address		Register name	R/W	Default	Setting/data								Function
FF10H	D3	**FOUT3**	R/W	0	F	f_3	B	$f_3/16$	7	f_1	3	$f_1/32$	FOUT frequency selection ($f_1 = f_{OSC1}$, $f_3 = f_{OSC3}$)
	D2	**FOUT2**	R/W	0	E	$f_3/2$	A	$f_3/32$	6	$f_1/2$	2	$f_1/64$	
	D1	**FOUT1**	R/W	0	D	$f_3/4$	9	$f_3/64$	5	$f_1/4$	1	$f_1/256$	
	D0	**FOUT0**	R/W	0	C	$f_3/8$	8	$f_3/256$	4	$f_1/16$	0	Off	
FF11H	D3	**NRSP11** (∗6)	R/W	0	3	$f_1/256$			1	$f_1/16$			P1 key input interrupt noise reject frequency selection ($f_1 = f_{OSC1}$)
	D2	**NRSP10** (∗6)	R/W	0	2	$f_1/64$			0	Off			
	D1	**NRSP01**	R/W	0	3	$f_1/256$			1	$f_1/16$			P0 key input interrupt noise reject frequency selection ($f_1 = f_{OSC1}$)
	D0	**NRSP00**	R/W	0	2	$f_1/64$			0	Off			
FF12H	D3	**FLCKS1**	R/W	0	3	–			1	21.3			Frame frequency (Hz) selection
	D2	**FLCKS0**	R/W	0	2	16.0			0	32.0			
	D1	**VCCKS1**	R/W	0	3	–			1	2048			V_C boost frequency (Hz) selection
	D0	**VCCKS0**	R/W	0	2	–			0	Off			

Address		Register name	R/W	Default	Setting/data	Function
FF14H	D3	0 (∗3)	R	– (∗2)	–	Unused
(∗6)	D2	**SIFCKS2**	R/W	0	7 f_3/4 4 PT1 1 f_1	Serial I/F clock frequency selection
	D1	**SIFCKS1**	R/W	0	6 f_3/2 3 f_1/4 0 Off/	(f_1 = $fosc_1$, f_3 = $fosc_3$)
	D0	**SIFCKS0**	R/W	0	5 f_3 2 f_1/2 External	
FF15H	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	**RFCKS2**	R/W	0	7 f_3/4 4 PT1 (∗6) 1 f_1	R/F converter clock frequency selection
	D1	**RFCKS1**	R/W	0	6 f_3/2 3 f_1/4 0 Off	(f_1 = $fosc_1$, f_3 = $fosc_3$)
	D0	**RFCKS0**	R/W	0	5 f_3 2 f_1/2	
FF16H	D3	**MDCKE** (∗5)	R/W	0	1 Enable 0 Disable	Integer multiplier clock enable
	D2	**SGCKE**	R/W	0	1 Enable 0 Disable	Sound generator clock enable
	D1	**SWCKE**	R/W	0	1 Enable 0 Disable	Stopwatch timer clock enable
	D0	**RTCKE**	R/W	0	1 Enable 0 Disable	Clock timer clock enable
FF18H	D3	**PTPS03**	R/W	0	F f_3 B f_3/16 7 f_1 3 f_1/32	Programmable timer 0 count clock frequency
	D2	**PTPS02**	R/W	0	E f_3/2 A f_3/32 6 f_1/2 2 f_1/64	selection (f_1 = $fosc_1$, f_3 = $fosc_3$)
	D1	**PTPS01**	R/W	0	D f_3/4 9 f_3/64 5 f_1/4 1 f_1/256	
	D0	**PTPS00**	R/W	0	C f_3/8 8 f_3/256 4 f_1/16 0 Off	
FF19H	D3	**PTPS13**	R/W	0	F f_3 B f_3/16 7 f_1 3 f_1/32	Programmable timer 1 count clock frequency
(∗6)	D2	**PTPS12**	R/W	0	E f_3/2 A f_3/32 6 f_1/2 2 f_1/64	selection (f_1 = $fosc_1$, f_3 = $fosc_3$)
	D1	**PTPS11**	R/W	0	D f_3/4 9 f_3/64 5 f_1/4 1 f_1/256	
	D0	**PTPS10**	R/W	0	C f_3/8 8 f_3/256 4 f_1/16 0 Off	
FF1AH	D3	**PTPS23**	R/W	0	F f_3 B f_3/16 7 f_1 3 f_1/32	Programmable timer 2 count clock frequency
(∗6)	D2	**PTPS22**	R/W	0	E f_3/2 A f_3/32 6 f_1/2 2 f_1/64	selection (f_1 = $fosc_1$, f_3 = $fosc_3$)
	D1	**PTPS21**	R/W	0	D f_3/4 9 f_3/64 5 f_1/4 1 f_1/256	
	D0	**PTPS20**	R/W	0	C f_3/8 8 f_3/256 4 f_1/16 0 Off	
FF1BH	D3	**PTPS33**	R/W	0	F f_3 B f_3/16 7 f_1 3 f_1/32	Programmable timer 3 count clock frequency
(∗4)	D2	**PTPS32**	R/W	0	E f_3/2 A f_3/32 6 f_1/2 2 f_1/64	selection (f_1 = $fosc_1$, f_3 = $fosc_3$)
	D1	**PTPS31**	R/W	0	D f_3/4 9 f_3/64 5 f_1/4 1 f_1/256	
	D0	**PTPS30**	R/W	0	C f_3/8 8 f_3/256 4 f_1/16 0 Off	

FF20H–FF3FH I/O Ports

Address		Register name	R/W	Default	Setting/data	Function
FF20H	D3	**P03**	R/W	1	1 High 0 Low	P03 I/O port data
	D2	**P02**	R/W	1	1 High 0 Low	P02 I/O port data
	D1	**P01**	R/W	1	1 High 0 Low	P01 I/O port data
	D0	**P00**	R/W	1	1 High 0 Low	P00 I/O port data
FF21H	D3	**IOC03**	R/W	0	1 Output 0 Input	P03 I/O control register
	D2	**IOC02**	R/W	0	1 Output 0 Input	P02 I/O control register
	D1	**IOC01**	R/W	0	1 Output 0 Input	P01 I/O control register
	D0	**IOC00**	R/W	0	1 Output 0 Input	P00 I/O control register
FF22H	D3	**PUL03**	R/W	1	1 Enable 0 Disable	P03 pull-down control register
	D2	**PUL02**	R/W	1	1 Enable 0 Disable	P02 pull-down control register
	D1	**PUL01**	R/W	1	1 Enable 0 Disable	P01 pull-down control register
	D0	**PUL00**	R/W	1	1 Enable 0 Disable	P00 pull-down control register
FF23H	D3	**SMT03**	R/W	1	1 Schmitt 0 CMOS	P03 input I/F level select register
	D2	**SMT02**	R/W	1	1 Schmitt 0 CMOS	P02 input I/F level select register
	D1	**SMT01**	R/W	1	1 Schmitt 0 CMOS	P01 input I/F level select register
	D0	**SMT00**	R/W	1	1 Schmitt 0 CMOS	P00 input I/F level select register
FF24H	D3	**P13**	R/W	1	1 High 0 Low	P13 I/O port data
	D2	**P12**	R/W	1	1 High 0 Low	P12 I/O port data
	D1	**P11**	R/W	1	1 High 0 Low	P11 I/O port data
	D0	**P10**	R/W	1	1 High 0 Low	P10 I/O port data
FF25H	D3	**IOC13**	R/W	0	1 Output 0 Input	P13 I/O control register
	D2	**IOC12**	R/W	0	1 Output 0 Input	P12 I/O control register
	D1	**IOC11**	R/W	0	1 Output 0 Input	P11 I/O control register
	D0	**IOC10**	R/W	0	1 Output 0 Input	P10 I/O control register
FF26H	D3	**PUL13**	R/W	1	1 Enable 0 Disable	P13 pull-down control register
	D2	**PUL12**	R/W	1	1 Enable 0 Disable	P12 pull-down control register
	D1	**PUL11**	R/W	1	1 Enable 0 Disable	P11 pull-down control register
	D0	**PUL10**	R/W	1	1 Enable 0 Disable	P10 pull-down control register
FF27H	D3	**SMT13**	R/W	1	1 Schmitt 0 CMOS	P13 input I/F level select register
	D2	**SMT12**	R/W	1	1 Schmitt 0 CMOS	P12 input I/F level select register
	D1	**SMT11**	R/W	1	1 Schmitt 0 CMOS	P11 input I/F level select register
	D0	**SMT10**	R/W	1	1 Schmitt 0 CMOS	P10 input I/F level select register

Address		Register name	R/W	Default	Setting/data				Function
FF28H	D3	**P23**	R/W	1	1	High	0	Low	P23 I/O port data
	D2	**P22**	R/W	1	1	High	0	Low	P22 I/O port data
	D1	**P21**	R/W	1	1	High	0	Low	P21 I/O port data
	D0	**P20**	R/W	1	1	High	0	Low	P20 I/O port data
FF29H	D3	**IOC23**	R/W	0	1	Output	0	Input	P23 I/O control register
	D2	**IOC22**	R/W	0	1	Output	0	Input	P22 I/O control register
	D1	**IOC21**	R/W	0	1	Output	0	Input	P21 I/O control register
	D0	**IOC20**	R/W	0	1	Output	0	Input	P20 I/O control register
FF2AH	D3	**PUL23**	R/W	1	1	Enable	0	Disable	P23 pull-down control register
	D2	**PUL22**	R/W	1	1	Enable	0	Disable	P22 pull-down control register
	D1	**PUL21**	R/W	1	1	Enable	0	Disable	P21 pull-down control register
	D0	**PUL20**	R/W	1	1	Enable	0	Disable	P20 pull-down control register
FF2CH	D3	**P33**	R/W	1	1	High	0	Low	P33 I/O port data
(*6)	D2	**P32**	R/W	1	1	High	0	Low	P32 I/O port data
	D1	**P31**	R/W	1	1	High	0	Low	P31 I/O port data
	D0	**P30**	R/W	1	1	High	0	Low	P30 I/O port data
FF2DH	D3	**IOC33**	R/W	0	1	Output	0	Input	P33 I/O control register
(*6)	D2	**IOC32**	R/W	0	1	Output	0	Input	P32 I/O control register
	D1	**IOC31**	R/W	0	1	Output	0	Input	P31 I/O control register
	D0	**IOC30**	R/W	0	1	Output	0	Input	P30 I/O control register
FF2EH	D3	**PUL33**	R/W	1	1	Enable	0	Disable	P33 pull-down control register
(*6)	D2	**PUL32**	R/W	1	1	Enable	0	Disable	P32 pull-down control register
	D1	**PUL31**	R/W	1	1	Enable	0	Disable	P31 pull-down control register
	D0	**PUL30**	R/W	1	1	Enable	0	Disable	P30 pull-down control register
FF30H	D3	**P43**	R/W	1	1	High	0	Low	P43 I/O port data
(*5)	D2	**P42**	R/W	1	1	High	0	Low	P42 I/O port data
	D1	**P41**	R/W	1	1	High	0	Low	P41 I/O port data
	D0	**P40**	R/W	1	1	High	0	Low	P40 I/O port data
FF31H	D3	**IOC43**	R/W	0	1	Output	0	Input	P43 I/O control register
(*5)	D2	**IOC42**	R/W	0	1	Output	0	Input	P42 I/O control register
	D1	**IOC41**	R/W	0	1	Output	0	Input	P41 I/O control register
	D0	**IOC40**	R/W	0	1	Output	0	Input	P40 I/O control register
FF32H	D3	**PUL43**	R/W	1	1	Enable	0	Disable	P43 pull-down control register
(*5)	D2	**PUL42**	R/W	1	1	Enable	0	Disable	P42 pull-down control register
	D1	**PUL41**	R/W	1	1	Enable	0	Disable	P41 pull-down control register
	D0	**PUL40**	R/W	1	1	Enable	0	Disable	P40 pull-down control register
FF34H	D3	**P53**	R/W	1	1	High	0	Low	P53 I/O port data
	D2	**P52**	R/W	1	1	High	0	Low	P52 I/O port data
	D1	**P51**	R/W	1	1	High	0	Low	P51 I/O port data
	D0	**P50**	R/W	1	1	High	0	Low	P50 I/O port data
FF35H	D3	**IOC53**	R/W	0	1	Output	0	Input	P53 I/O control register
	D2	**IOC52**	R/W	0	1	Output	0	Input	P52 I/O control register
	D1	**IOC51**	R/W	0	1	Output	0	Input	P51 I/O control register
	D0	**IOC50**	R/W	0	1	Output	0	Input	P50 I/O control register
FF36H	D3	**PUL53**	R/W	1	1	Enable	0	Disable	P53 pull-down control register
	D2	**PUL52**	R/W	1	1	Enable	0	Disable	P52 pull-down control register
	D1	**PUL51**	R/W	1	1	Enable	0	Disable	P51 pull-down control register
	D0	**PUL50**	R/W	1	1	Enable	0	Disable	P50 pull-down control register
FF3CH	D3	**SIP03**	R/W	0	1	Enable	0	Disable	P03 (KEY03) interrupt select register
	D2	**SIP02**	R/W	0	1	Enable	0	Disable	P02 (KEY02) interrupt select register
	D1	**SIP01**	R/W	0	1	Enable	0	Disable	P01 (KEY01) interrupt select register
	D0	**SIP00**	R/W	0	1	Enable	0	Disable	P00 (KEY00) interrupt select register
FF3DH	D3	**PCP03**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P03 (KEY03) interrupt polarity select register
	D2	**PCP02**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P02 (KEY02) interrupt polarity select register
	D1	**PCP01**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P01 (KEY01) interrupt polarity select register
	D0	**PCP00**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P00 (KEY00) interrupt polarity select register
FF3EH	D3	**SIP13**	R/W	0	1	Enable	0	Disable	P13(KEY13) interrupt select register
(*6)	D2	**SIP12**	R/W	0	1	Enable	0	Disable	P12(KEY12) interrupt select register
	D1	**SIP11**	R/W	0	1	Enable	0	Disable	P11(KEY11) interrupt select register
	D0	**SIP10**	R/W	0	1	Enable	0	Disable	P10(KEY10) interrupt select register
FF3FH	D3	**PCP13**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P13(KEY13) interrupt polarity select register
(*6)	D2	**PCP12**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P12(KEY12) interrupt polarity select register
	D1	**PCP11**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P11(KEY11) interrupt polarity select register
	D0	**PCP10**	R/W	1	1	↓ (falling edge)	0	↑ (rising edge)	P10(KEY10) interrupt polarity select register

FF40H–FF42H Clock Timer

Address		Register name	R/W	Default	Setting/data	Function
FF40H	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	0 (∗3)	R	– (∗2)	–	Unused
	D1	**TMRST** (∗3)	W	(Reset)	1 Reset / 0 Invalid	Clock timer reset (writing)
	D0	**TMRUN**	R/W	0	1 Run / 0 Stop	Clock timer Run/Stop
FF41H	D3	**TM3**	R	0	0H–FH	Clock timer data (16 Hz)
	D2	**TM2**	R	0		Clock timer data (32 Hz)
	D1	**TM1**	R	0		Clock timer data (64 Hz)
	D0	**TM0**	R	0		Clock timer data (128 Hz)
FF42H	D3	**TM7**	R	0	0H–FH	Clock timer data (1 Hz)
	D2	**TM6**	R	0		Clock timer data (2 Hz)
	D1	**TM5**	R	0		Clock timer data (4 Hz)
	D0	**TM4**	R	0		Clock timer data (8 Hz)

FF44H–FF47H Sound Generator

Address		Register name	R/W	Default	Setting/data	Function
FF44H	D3	**ENRTM**	R/W	0	1 1 sec / 0 0.5 sec	Envelope releasing time selection
	D2	**ENRST** (∗3)	W	(Reset)	1 Reset / 0 Invalid	Envelope reset (writing)
	D1	**ENON**	R/W	0	1 On / 0 Off	Envelope On/Off
	D0	**BZE**	R/W	0	1 Enable / 0 Disable	Buzzer output enable
FF45H	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	**BZSTP** (∗3)	W	0	1 Stop / 0 Invalid	1-shot buzzer stop (writing)
	D1	**BZSHT**	R/W	0	1 Trigger (W) Busy (R) / 0 Invalid (W) Ready (R)	1-shot buzzer trigger (writing) 1-shot buzzer status (reading)
	D0	**SHTPW**	R/W	0	1 125 msec / 0 31.25 msec	1-shot buzzer pulse width setting
FF46H	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	**BZFQ2**	R/W	0	7 1170.3 / 4 2048.0 / 1 3276.8	Buzzer frequency (Hz) selection
	D1	**BZFQ1**	R/W	0	6 1365.3 / 3 2340.6 / 0 4096.0	
	D0	**BZFQ0**	R/W	0	5 1638.4 / 2 2730.7	
FF47H	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	**BDTY2**	R/W	0	7 Level 8 / 4 Level 5 / 1 Level 2	Buzzer signal duty ratio selection
	D1	**BDTY1**	R/W	0	6 Level 7 / 3 Level 4 / 0 Level 1	
	D0	**BDTY0**	R/W	0	5 Level 6 / 2 Level 3 / (max.)	

FF48H–FF4DH Stopwatch Timer

Address		Register name	R/W	Default	Setting/data	Function
FF48H (∗6)	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	0 (∗3)	R	– (∗2)	–	Unused
	D1	**SWDIR**	R/W	0	1 P00 = Lap, P01 = Run/Stop / 0 P00 = Run/Stop, P01 = Lap	Stopwatch direct input switch
	D0	**EDIR**	R/W	0	1 Enable / 0 Disable	Direct input enable
FF49H (∗6)	D3	0 (∗3)	R	– (∗2)	–	Unused
	D2	**DKM2**	R/W	0	7 P10–13 / 4 P10 / 1 P02	Key mask selection
	D1	**DKM1**	R/W	0	6 P10–12 / 3 P02–03,10 / 0 No mask	
	D0	**DKM0**	R/W	0	5 P10–11 / 2 P02–03	
FF4AH	D3	**LCURF** (∗6)	R	0	1 Request / 0 No	Lap data carry-up request flag
	D2	**CRNWF** (∗6)	R	0	1 Renewal / 0 No	Capture renewal flag
	D1	**SWRUN**	R/W	0	1 Run / 0 Stop	Stopwatch timer Run/Stop
	D0	**SWRST** (∗3)	W	(Reset)	1 Reset / 0 Invalid	Stopwatch timer reset (writing)
FF4BH	D3	**SWD3**	R	0	0–9	Stopwatch timer data BCD (1/1000 sec)
	D2	**SWD2**	R	0		
	D1	**SWD1**	R	0		
	D0	**SWD0**	R	0		
FF4CH	D3	**SWD7**	R	0	0–9	Stopwatch timer data BCD (1/100 sec)
	D2	**SWD6**	R	0		
	D1	**SWD5**	R	0		
	D0	**SWD4**	R	0		
FF4DH	D3	**SWD11**	R	0	0–9	Stopwatch timer data BCD (1/10 sec)
	D2	**SWD10**	R	0		
	D1	**SWD9**	R	0		
	D0	**SWD8**	R	0		

FF50H–FF52H LCD Driver

Address		Register name	R/W	Default	Setting/data	Function
FF50H	D3	0 (*3)	R	– (*2)	–	Unused
	D2	0 (*3)	R	– (*2)	–	Unused
	D1	**DSPC1**	R/W	1	3 All on / 1 All on	LCD display mode selection
	D0	**DSPC0**	R/W	0	2 All off / 0 Normal	
FF51H	D3	**STCD**	R/W	0	1 Static / 0 Dynamic	LCD drive mode switch
	D2	**LDUTY2**	R/W	0	7 1/8 (*6) / 4 1/7 (*6) / 1 1/4	LCD drive duty selection
	D1	**LDUTY1**	R/W	0	6 1/7 (*6) / 3 1/6 (*6) / 0 1/3	
	D0	**LDUTY0**	R/W	0	5 1/8 (*6) / 2 1/5	
FF52H (*6)	D3	**LC3**	R/W	0	0H(light)–FH(dark)	LCD contrast adjustment
	D2	**LC2**	R/W	0		
	D1	**LC1**	R/W	0		
	D0	**LC0**	R/W	0		

FF58H–FF5CH Serial Interface

Address		Register name	R/W	Default	Setting/data	Function
FF58H (*6)	D3	0 (*3)	R	– (*2)	–	Unused
	D2	**ESOUT**	R/W	0	1 Enable / 0 Disable	SOUT enable
	D1	**SCTRG**	R/W	0	1 Trigger (W) Run (R) / 0 Invalid (W) Stop (R)	Serial I/F clock trigger (writing) Serial I/F clock status (reading)
	D0	**ESIF**	R/W	0	1 SIF / 0 I/O	Serial I/F enable (P3 port function selection)
FF59H (*6)	D3	**SCPS1**	R/W	0	3 Negative, ↑ / 1 Positive, ↓	Serial I/F clock format selection
	D2	**SCPS0**	R/W	0	2 Negative, ↓ / 0 Positive, ↑	(polarity, phase)
	D1	**SDP**	R/W	0	1 MSB first / 0 LSB first	Serial I/F data input/output permutation
	D0	**SMOD**	R/W	0	1 Master / 0 Slave	Serial I/F mode selection
FF5AH (*6)	D3	0 (*3)	R	– (*2)	–	Unused
	D2	0 (*3)	R	– (*2)	–	Unused
	D1	**ESREADY**	R/W	0	1 SRDY / 0 $\overline{SS}$	SRDY_SS function selection (ENCS = "1")
	D0	**ENCS**	R/W	0	1 SRDY_SS / 0 P33	SRDY_SS enable (P33 port function selection)
FF5BH (*6)	D3	**SD3**	R/W	×	0H–FH	Serial I/F transmit/receive data (low-order 4 bits) SD0 = LSB
	D2	**SD2**	R/W	×		
	D1	**SD1**	R/W	×		
	D0	**SD0**	R/W	×		
FF5CH (*6)	D3	**SD7**	R/W	×	0H–FH	Serial I/F transmit/receive data (high-order 4 bits) SD7 = MSB
	D2	**SD6**	R/W	×		
	D1	**SD5**	R/W	×		
	D0	**SD4**	R/W	×		

FF60H–FF6BH R/F Converter

Address		Register name	R/W	Default	Setting/data	Function
FF60H	D3	**RFCNT**	R/W	0	1 Continuous / 0 Normal	Continuous oscillation enable
	D2	**RFOUT**	R/W	0	1 Enable / 0 Disable	RFOUT enable
	D1	**ERF1**	R/W	0	3 Ch.1 DC / 1 Ch.0 DC	R/F conversion selection
	D0	**ERF0**	R/W	0	2 Ch.1 AC / 0 I/O	
FF61H	D3	**OVTC**	R/W	0	1 Overflow error / 0 No error	Time base counter overflow flag
	D2	**OVMC**	R/W	0	1 Overflow error / 0 No error	Measurement counter overflow flag
	D1	**RFRUNR**	R/W	0	1 Run / 0 Stop	Reference oscillation Run control/status
	D0	**RFRUNS**	R/W	0	1 Run / 0 Stop	Sensor oscillation Run control/status
FF62H	D3	**MC3**	R/W	×	0H–FH	Measurement counter MC0–MC3 MC0 = LSB
	D2	**MC2**	R/W	×		
	D1	**MC1**	R/W	×		
	D0	**MC0**	R/W	×		
FF63H	D3	**MC7**	R/W	×	0H–FH	Measurement counter MC4–MC7
	D2	**MC6**	R/W	×		
	D1	**MC5**	R/W	×		
	D0	**MC4**	R/W	×		
FF64H	D3	**MC11**	R/W	×	0H–FH	Measurement counter MC8–MC11
	D2	**MC10**	R/W	×		
	D1	**MC9**	R/W	×		
	D0	**MC8**	R/W	×		

Address		Register name	R/W	Default	Setting/data	Function
FF65H	D3	**MC15**	R/W	×	0H–FH	Measurement counter MC12–MC15
	D2	**MC14**	R/W	×		
	D1	**MC13**	R/W	×		
	D0	**MC12**	R/W	×		
FF66H	D3	**MC19**	R/W	×	0H–FH	Measurement counter MC16–MC19 MC19 = MSB
	D2	**MC18**	R/W	×		
	D1	**MC17**	R/W	×		
	D0	**MC16**	R/W	×		
FF67H	D3	**TC3**	R/W	×	0H–FH	Time base counter TC0–TC3 TC0 = LSB
	D2	**TC2**	R/W	×		
	D1	**TC1**	R/W	×		
	D0	**TC0**	R/W	×		
FF68H	D3	**TC7**	R/W	×	0H–FH	Time base counter TC4–TC7
	D2	**TC6**	R/W	×		
	D1	**TC5**	R/W	×		
	D0	**TC4**	R/W	×		
FF69H	D3	**TC11**	R/W	×	0H–FH	Time base counter TC8–TC11
	D2	**TC10**	R/W	×		
	D1	**TC9**	R/W	×		
	D0	**TC8**	R/W	×		
FF6AH	D3	**TC15**	R/W	×	0H–FH	Time base counter TC12–TC15
	D2	**TC14**	R/W	×		
	D1	**TC13**	R/W	×		
	D0	**TC12**	R/W	×		
FF6BH	D3	**TC19**	R/W	×	0H–FH	Time base counter TC16–TC19 TC19 = MSB
	D2	**TC18**	R/W	×		
	D1	**TC17**	R/W	×		
	D0	**TC16**	R/W	×		

FF70H–FF76H Integer Multiplier

Address		Register name	R/W	Default	Setting/data	Function
FF70H (∗5)	D3	**SR3**	R/W	×	0H–FH	Source register (low-order 4 bits) SR0 = LSB
	D2	**SR2**	R/W	×		
	D1	**SR1**	R/W	×		
	D0	**SR0**	R/W	×		
FF71H (∗5)	D3	**SR7**	R/W	×	0H–FH	Source register (high-order 4 bits) SR7 = MSB
	D2	**SR6**	R/W	×		
	D1	**SR5**	R/W	×		
	D0	**SR4**	R/W	×		
FF72H (∗5)	D3	**DRL3**	R/W	×	0H–FH	Low-order 8-bit destination register (low-order 4 bits) DRL0 = LSB
	D2	**DRL2**	R/W	×		
	D1	**DRL1**	R/W	×		
	D0	**DRL0**	R/W	×		
FF73H (∗5)	D3	**DRL7**	R/W	×	0H–FH	Low-order 8-bit destination register (high-order 4 bits) DRL7 = MSB
	D2	**DRL6**	R/W	×		
	D1	**DRL5**	R/W	×		
	D0	**DRL4**	R/W	×		
FF74H (∗5)	D3	**DRH3**	R/W	×	0H–FH	High-order 8-bit destination register (low-order 4 bits) DRH0 = LSB
	D2	**DRH2**	R/W	×		
	D1	**DRH1**	R/W	×		
	D0	**DRH0**	R/W	×		
FF75H (∗5)	D3	**DRH7**	R/W	×	0H–FH	High-order 8-bit destination register (high-order 4 bits) DRH7 = MSB
	D2	**DRH6**	R/W	×		
	D1	**DRH5**	R/W	×		
	D0	**DRH4**	R/W	×		

FF76H (∗5)	D3	**NF**	R	0	1	Negative	0	Positive	Negative flag
	D2	**VF**	R	0	1	Overflow	0	No	Overflow flag
	D1	**ZF**	R	0	1	Zero	0	No	Zero flag
	D0	**CALMD**	R/W	0	1	Division (W) Run (R)	0	Multiplication (W) Stop (R)	Calculation mode selection (writing) Operation status (reading)

FF80H–FF9FH Programmable Timer

Address		Register name	R/W	Default	Setting/data				Function
FF80H	D3	**MOD16_A** (∗6)	R/W	0	1	16 bits	0	8 bits	PTM0–1 16-bit mode selection
	D2	**EVCNT_A**	R/W	0	1	Event counter	0	Timer	PTM0 counter mode selection
	D1	**FCSEL_A**	R/W	0	1	With noise reject	0	No noise reject	PTM0 function selection (for event counter mode)
	D0	**PLPUL_A**	R/W	0	1	↑ (positive)	0	↓ (negative)	PTM0 pulse polarity selection (event counter mode)
FF81H	D3	**PTSEL1** (∗6)	R/W	0	1	PWM	0	Normal	Programmable timer 1 PWM output selection
	D2	**PTSEL0** (∗6)	R/W	0	1	PWM	0	Normal	Programmable timer 0 PWM output selection
	D1	**CHSEL_A** (∗6)	R/W	0	1	Timer 1	0	Timer 0	PTM0–1 TOUT_A output selection
	D0	**PTOUT_A**	R/W	0	1	On	0	Off	PTM0–1 TOUT_A output control
FF82H	D3	**PTRST1** (∗3,∗6)	W	– (∗2)	1	Reset	0	Invalid	Programmable timer 1 reset (reload)
	D2	**PTRUN1** (∗6)	R/W	0	1	Run	0	Stop	Programmable timer 1 Run/Stop
	D1	**PTRST0** (∗3)	W	– (∗2)	1	Reset	0	Invalid	Programmable timer 0 reset (reload)
	D0	**PTRUN0**	R/W	0	1	Run	0	Stop	Programmable timer 0 Run/Stop
FF84H	D3	**RLD03**	R/W	0	0H–FH				Programmable timer 0 reload data (low-order 4 bits) RLD00 = LSB
	D2	**RLD02**	R/W	0					
	D1	**RLD01**	R/W	0					
	D0	**RLD00**	R/W	0					
FF85H	D3	**RLD07**	R/W	0	0H–FH				Programmable timer 0 reload data (high-order 4 bits) RLD07 = MSB
	D2	**RLD06**	R/W	0					
	D1	**RLD05**	R/W	0					
	D0	**RLD04**	R/W	0					
FF86H (∗6)	D3	**RLD13**	R/W	0	0H–FH				Programmable timer 1 reload data (low-order 4 bits) RLD10 = LSB
	D2	**RLD12**	R/W	0					
	D1	**RLD11**	R/W	0					
	D0	**RLD10**	R/W	0					
FF87H (∗6)	D3	**RLD17**	R/W	0	0H–FH				Programmable timer 1 reload data (high-order 4 bits) RLD17 = MSB
	D2	**RLD16**	R/W	0					
	D1	**RLD15**	R/W	0					
	D0	**RLD14**	R/W	0					
FF88H	D3	**PTD03**	R	0	0H–FH				Programmable timer 0 data (low-order 4 bits) PTD00 = LSB
	D2	**PTD02**	R	0					
	D1	**PTD01**	R	0					
	D0	**PTD00**	R	0					
FF89H	D3	**PTD07**	R	0	0H–FH				Programmable timer 0 data (high-order 4 bits) PTD07 = MSB
	D2	**PTD06**	R	0					
	D1	**PTD05**	R	0					
	D0	**PTD04**	R	0					
FF8AH (∗6)	D3	**PTD13**	R	0	0H–FH				Programmable timer 1 data (low-order 4 bits) PTD10 = LSB
	D2	**PTD12**	R	0					
	D1	**PTD11**	R	0					
	D0	**PTD10**	R	0					
FF8BH (∗6)	D3	**PTD17**	R	0	0H–FH				Programmable timer 1 data (high-order 4 bits) PTD17 = MSB
	D2	**PTD16**	R	0					
	D1	**PTD15**	R	0					
	D0	**PTD14**	R	0					
FF8CH (∗6)	D3	**CD03**	R/W	0	0H–FH				Programmable timer 0 compare data (high-order 4 bits) CD00 = LSB
	D2	**CD02**	R/W	0					
	D1	**CD01**	R/W	0					
	D0	**CD00**	R/W	0					
FF8DH (∗6)	D3	**CD07**	R/W	0	0H–FH				Programmable timer 0 compare data (high-order 4 bits) CD07 = MSB
	D2	**CD06**	R/W	0					
	D1	**CD05**	R/W	0					
	D0	**CD04**	R/W	0					
FF8EH (∗6)	D3	**CD13**	R/W	0	0H–FH				Programmable timer 1 compare data (low-order 4 bits) CD10 = LSB
	D2	**CD12**	R/W	0					
	D1	**CD11**	R/W	0					
	D0	**CD10**	R/W	0					
FF8FH (∗6)	D3	**CD17**	R/W	0	0H–FH				Programmable timer 1 compare data (high-order 4 bits) CD17 = MSB
	D2	**CD16**	R/W	0					
	D1	**CD15**	R/W	0					
	D0	**CD14**	R/W	0					

Address		Register name	R/W	Default	Setting/data				Function
FF90H	D3	**MOD16_B** (*4)	R/W	0	1	16 bits	0	8 bits	PTM2–3 16-bit mode selection
(*6)	D2	**EVCNT_B**	R/W	0	1	Event counter	0	Timer	PTM2 counter mode selection
	D1	**FCSEL_B**	R/W	0	1	With noise reject	0	No noise reject	PTM2 function selection (for event counter mode)
	D0	**PLPUL_B**	R/W	0	1	↑ (positive)	0	↓ (negative)	PTM2 pulse polarity selection (event counter mode)
FF91H	D3	**PTSEL3** (*4)	R/W	0	1	PWM	0	Normal	Programmable timer 3 PWM output selection
(*6)	D2	**PTSEL2**	R/W	0	1	PWM	0	Normal	Programmable timer 2 PWM output selection
	D1	**CHSEL_B** (*4)	R/W	0	1	Timer 3	0	Timer 2	PTM2–3 TOUT_B output selection
	D0	**PTOUT_B**	R/W	0	1	On	0	Off	PTM2–3 TOUT_B output control
FF92H	D3	**PTRST3** (*3,*4)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 3 reset (reload)
(*6)	D2	**PTRUN3** (*4)	R/W	0	1	Run	0	Stop	Programmable timer 3 Run/Stop
	D1	**PTRST2** (*3)	W	– (*2)	1	Reset	0	Invalid	Programmable timer 2 reset (reload)
	D0	**PTRUN2**	R/W	0	1	Run	0	Stop	Programmable timer 2 Run/Stop
FF94H	D3	**RLD23**	R/W	0	0H–FH				Programmable timer 2 reload data (low-order 4 bits) RLD20 = LSB
(*6)	D2	**RLD22**	R/W	0					
	D1	**RLD21**	R/W	0					
	D0	**RLD20**	R/W	0					
FF95H	D3	**RLD27**	R/W	0	0H–FH				Programmable timer 2 reload data (high-order 4 bits) RLD27 = MSB
(*6)	D2	**RLD26**	R/W	0					
	D1	**RLD25**	R/W	0					
	D0	**RLD24**	R/W	0					
FF96H	D3	**RLD33**	R/W	0	0H–FH				Programmable timer 3 reload data (low-order 4 bits) RLD30 = LSB
(*4)	D2	**RLD32**	R/W	0					
	D1	**RLD31**	R/W	0					
	D0	**RLD30**	R/W	0					
FF97H	D3	**RLD37**	R/W	0	0H–FH				Programmable timer 3 reload data (high-order 4 bits) RLD37 = MSB
(*4)	D2	**RLD36**	R/W	0					
	D1	**RLD35**	R/W	0					
	D0	**RLD34**	R/W	0					
FF98H	D3	**PTD23**	R	0	0H–FH				Programmable timer 2 data (low-order 4 bits) PTD20 = LSB
(*6)	D2	**PTD22**	R	0					
	D1	**PTD21**	R	0					
	D0	**PTD20**	R	0					
FF99H	D3	**PTD27**	R	0	0H–FH				Programmable timer 2 data (high-order 4 bits) PTD27 = MSB
(*6)	D2	**PTD26**	R	0					
	D1	**PTD25**	R	0					
	D0	**PTD24**	R	0					
FF9AH	D3	**PTD33**	R	0	0H–FH				Programmable timer 3 data (low-order 4 bits) PTD30 = LSB
(*4)	D2	**PTD32**	R	0					
	D1	**PTD31**	R	0					
	D0	**PTD30**	R	0					
FF9BH	D3	**PTD37**	R	0	0H–FH				Programmable timer 3 data (high-order 4 bits) PTD37 =MSB
(*4)	D2	**PTD36**	R	0					
	D1	**PTD35**	R	0					
	D0	**PTD34**	R	0					
FF9CH	D3	**CD23**	R/W	0	0H–FH				Programmable timer 2 compare data (low-order 4 bits) CD20 = LSB
(*6)	D2	**CD22**	R/W	0					
	D1	**CD21**	R/W	0					
	D0	**CD20**	R/W	0					
FF9DH	D3	**CD27**	R/W	0	0H–FH				Programmable timer 2 compare data (high-order 4 bits) CD27 = MSB
(*6)	D2	**CD26**	R/W	0					
	D1	**CD25**	R/W	0					
	D0	**CD24**	R/W	0					
FF9EH	D3	**CD33**	R/W	0	0H–FH				Programmable timer 3 compare data (low-order 4 bits) CD30 = LSB
(*4)	D2	**CD32**	R/W	0					
	D1	**CD31**	R/W	0					
	D0	**CD30**	R/W	0					
FF9FH	D3	**CD37**	R/W	0	0H–FH				Programmable timer 3 compare data (high-order 4 bits) CD37 = MSB
(*4)	D2	**CD36**	R/W	0					
	D1	**CD35**	R/W	0					
	D0	**CD34**	R/W	0					

FFE1H–FFFFH Interrupt Controller

Address		Register name	R/W	Default	Setting/data				Function
FFE1H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	**EIRFE**	R/W	0	1	Enable	0	Mask	Interrupt mask register (RFC error)
	D1	**EIRFR**	R/W	0	1	Enable	0	Mask	Interrupt mask register (RFC REF completion)
	D0	**EIRFS**	R/W	0	1	Enable	0	Mask	Interrupt mask register (RFC SEN completion)
FFE2H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT0**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT0 underflow)
	D0	**EICTC0** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT0 compare match)
FFE3H (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT1**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT1 underflow)
	D0	**EICTC1**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT1 compare match)
FFE4H (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT2**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT2 underflow)
	D0	**EICTC2**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT2 compare match)
FFE5H (*4)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**EIPT3**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT3 underflow)
	D0	**EICTC3**	R/W	0	1	Enable	0	Mask	Interrupt mask register (PT3 compare match)
FFEAH (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	0 (*3)	R	– (*2)	–				Unused
	D0	**EISIF**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Serial I/F)
FFEBH	D3	**EIK03**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY03<P03>)
	D2	**EIK02**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY02<P02>)
	D1	**EIK01**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY01<P01>)
	D0	**EIK00**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY00<P00>)
FFECH (*6)	D3	**EIK13**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY13<P13>)
	D2	**EIK12**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY12<P12>)
	D1	**EIK11**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY11<P11>)
	D0	**EIK10**	R/W	0	1	Enable	0	Mask	Interrupt mask register (KEY10<P10>)
FFEDH	D3	**EIRUN** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (SW direct RUN)
	D2	**EILAP** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (SW direct LAP)
	D1	**EISW1**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Stopwatch 1 Hz)
	D0	**EISW10**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Stopwatch 10 Hz)
FFEEH	D3	**EIT3** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 16 Hz)
	D2	**EIT2**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 32 Hz)
	D1	**EIT1** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 64 Hz)
	D0	**EIT0** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 128 Hz)
FFEFH	D3	**EIT7**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 1 Hz)
	D2	**EIT6**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 2 Hz)
	D1	**EIT5** (*6)	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 4 Hz)
	D0	**EIT4**	R/W	0	1	Enable	0	Mask	Interrupt mask register (Clock timer 8 Hz)
FFF1H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	**IRFE**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (RFC error)
	D1	**IRFR**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (RFC REF completion)
	D0	**IRFS**	R/W	0					Interrupt factor flag (RFC SEN completion)
FFF2H	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**IPT0**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT0 underflow)
	D0	**ICTC0** (*6)	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT0 compare match)
FFF3H (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**IPT1**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT1 underflow)
	D0	**ICTC1**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT1 compare match)
FFF4H (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**IPT2**	R/W	0	1	Occurred (R)	0	Not occurred (R)	Interrupt factor flag (PT2 underflow)
	D0	**ICTC2**	R/W	0		Reset (W)		Invalid (W)	Interrupt factor flag (PT2 compare match)

Address		Register name	R/W	Default	Setting/data				Function
FFF5H (*4)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	**IPT3**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (PT3 underflow)
	D0	**ICTC3**	R/W	0					Interrupt factor flag (PT3 compare match)
FFFAH (*6)	D3	0 (*3)	R	– (*2)	–				Unused
	D2	0 (*3)	R	– (*2)	–				Unused
	D1	0 (*3)	R	– (*2)	–				Unused
	D0	**ISIF**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (Serial I/F)
FFFBH	D3	**IK03**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (KEY03<P03>)
	D2	**IK02**	R/W	0					Interrupt factor flag (KEY02<P02>)
	D1	**IK01**	R/W	0					Interrupt factor flag (KEY01<P01>)
	D0	**IK00**	R/W	0					Interrupt factor flag (KEY00<P00>)
FFFCH (*6)	D3	**IK13**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (KEY13<P13>)
	D2	**IK12**	R/W	0					Interrupt factor flag (KEY12<P12>)
	D1	**IK11**	R/W	0					Interrupt factor flag (KEY11<P11>)
	D0	**IK10**	R/W	0					Interrupt factor flag (KEY10<P10>)
FFFDH	D3	**IRUN** (*6)	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (SW direct RUN)
	D2	**ILAP** (*6)	R/W	0					Interrupt factor flag (SW direct LAP)
	D1	**ISW1**	R/W	0					Interrupt factor flag (Stopwatch 1 Hz)
	D0	**ISW10**	R/W	0					Interrupt factor flag (Stopwatch 10 Hz)
FFFEH	D3	**IT3** (*6)	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (Clock timer 16 Hz)
	D2	**IT2**	R/W	0					Interrupt factor flag (Clock timer 32 Hz)
	D1	**IT1** (*6)	R/W	0					Interrupt factor flag (Clock timer 64 Hz)
	D0	**IT0** (*6)	R/W	0					Interrupt factor flag (Clock timer 128 Hz)
FFFFH	D3	**IT7**	R/W	0	1	Occurred (R) Reset (W)	0	Not occurred (R) Invalid (W)	Interrupt factor flag (Clock timer 1 Hz)
	D2	**IT6**	R/W	0					Interrupt factor flag (Clock timer 2 Hz)
	D1	**IT5** (*6)	R/W	0					Interrupt factor flag (Clock timer 4 Hz)
	D0	**IT4**	R/W	0					Interrupt factor flag (Clock timer 8 Hz)

Appendix B Peripheral Circuit Boards for S1C6F016

Note: The Peripheral Circuit Boards for the S1C6F016 is used for developing S1C63003/004/008/016 applications. Download the S1C6F016 circuit data to the S1C63 Family Peripheral Circuit Board (S5U1C63000P6).

This section describes how to use the Peripheral Circuit Boards for the S1C6F016 (S5U1C63000P6 and S5U1C6F016P2), which provide emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H2/S5U1C63000H6).
This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P6) provided in this document assumes that circuit data for the S1C6F016 has already been downloaded to the board. For information on downloading various circuit data, please see Section B.3. Please refer to the S5U1C63000H manual for detailed information on the ICE functions and method of use.

Note: The S5U1C63000P1 cannot be used for developing the S1C63003/004/008/016 applications.

B.1 Names and Functions of Each Part

B.1.1 S5U1C63000P6

The S5U1C63000P6 board provides peripheral circuit functions of S1C63 Family microcomputers other than the core CPU. The following explains the names and functions of each part of the S5U1C63000P6 board.

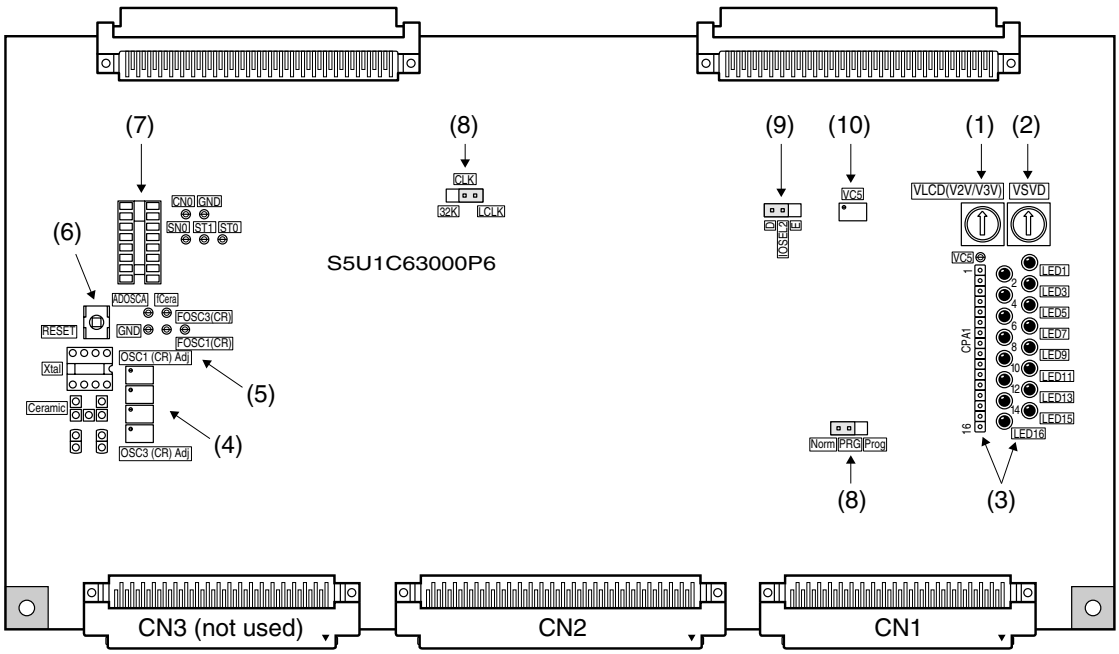


Figure B.1.1.1 S5U1C63000P6

(1) VLCD

This control is used to adjust the LCD drive voltage when an external power supply is selected by mask option for the LCD drive power supply.

(2) VSVD

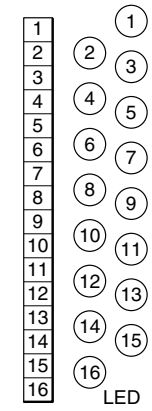
Unused

The switches on the S5U1C6F016P2 board are used to verify the operation of the supply voltage detection function (SVD).

(3) Register monitor LEDs/pins

These LEDs and pins correspond one-to-one to the registers listed below. The LED lights when the register is set to "1" and goes out when the register is set to "0." The monitor pins output a high level when the register is "1" and a low level when the register is "0."

Table B.1.1.1 Register monitor LEDs/pins



No.	pin Name	LED Name	Register = "1"	Register = "0"
1	DONE	–	Initialization of this board has completed normally.	During initialization
2	OSCC		OSC3 oscillation: On	OSC3 oscillation: Off
3	CLKCHG		CPU clock: OSC3	CPU clock: OSC1
4	VCSEL	–	FF02H•D2 = "1" (general-purpose register)	FF02H•D2 = "0" (general-purpose register)
5	DBON	–	FF02H•D0 = "1" (general-purpose register)	FF02H•D0 = "0" (general-purpose register)
6	VCHLMOD		V_C regulator heavy load protection mode: On	V_C regulator heavy load protection mode: Off
7	VDHLMOD		V_D regulator heavy load protection mode: On	V_D regulator heavy load protection mode: Off
8	VCREF		V_C regulator reference voltage: V_{C2}	V_C regulator reference voltage: V_{C1}
9	LPWR		V_C regulator: On	V_C regulator: Off
10	SVDON		SVD circuit: On	SVD circuit: Off
11	SVDS0		SVD criteria voltage level	
12	SVDS1			
13	SVDS2			
14	SVDS3			
15	SVDS4			
16	–	–	–	–

(4) CR oscillation frequency adjusting control

This control is used to adjust the OSC3 oscillation frequency. This function is effective only when CR oscillation is selected for the OSC3 oscillation circuit by mask option. The oscillation frequency can be adjusted in the range of about 100 kHz to 8 MHz. Note that the actual IC may not operate throughout this frequency range. Refer to "Electrical Characteristics" to select the appropriate operating frequency.

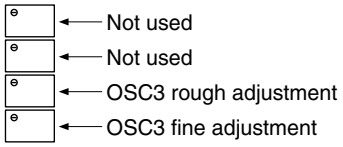


Figure B.1.1.2 CR oscillation frequency adjusting control

When ceramic oscillation is selected for the OSC3 oscillation circuit by mask option, the OSC3 frequency is fixed at 4.1943 MHz in this board .

(5) CR oscillation frequency monitor pins

These pins are used to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that the monitor pin always outputs a clock regardless of whether the oscillation is enabled via software or not.

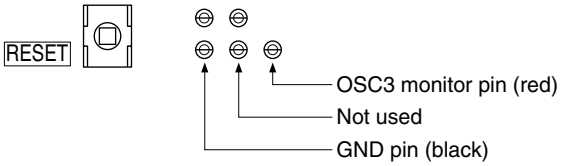


Figure B.1.1.3 CR oscillation frequency monitor pins

(6) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(7) External part connecting socket

Unused

(8) CLK and PRG switches

If power to the ICE is shut down before downloading circuit data is completed, the circuit configuration in this board will remain incomplete and the debugger may not be able to start after the ICE is turned on again.
In this case, temporarily turn the ICE off and set the CLK switch to the 32K position and the PRG switch to the Prog position, then turn the ICE on again. This should allow the debugger to start up, allowing you to download circuit data. After the circuit data has downloaded, temporarily turn the ICE off and reset the CLK and PRG switch to the LCLK and the Norm position, respectively. Then turn the ICE on again.

(9) IOSEL2

When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

(10) VC5

This control allows fine adjustment of the LCD drive voltage when an internal power supply is selected by mask option. Note, however, that the LCD drive voltage of the actual IC must be controlled using the LCD contrast adjustment register.

B.1.2 S5U1C6F016P2

The S5U1C6F016P2 board provides the R/F converter function that supports resistive sensors such as a thermistor and resistive humidity sensors, the SVD function, and the P50–P53 port inputs/outputs.
The following explains the names and functions of each part of the S5U1C6F016P2 board.

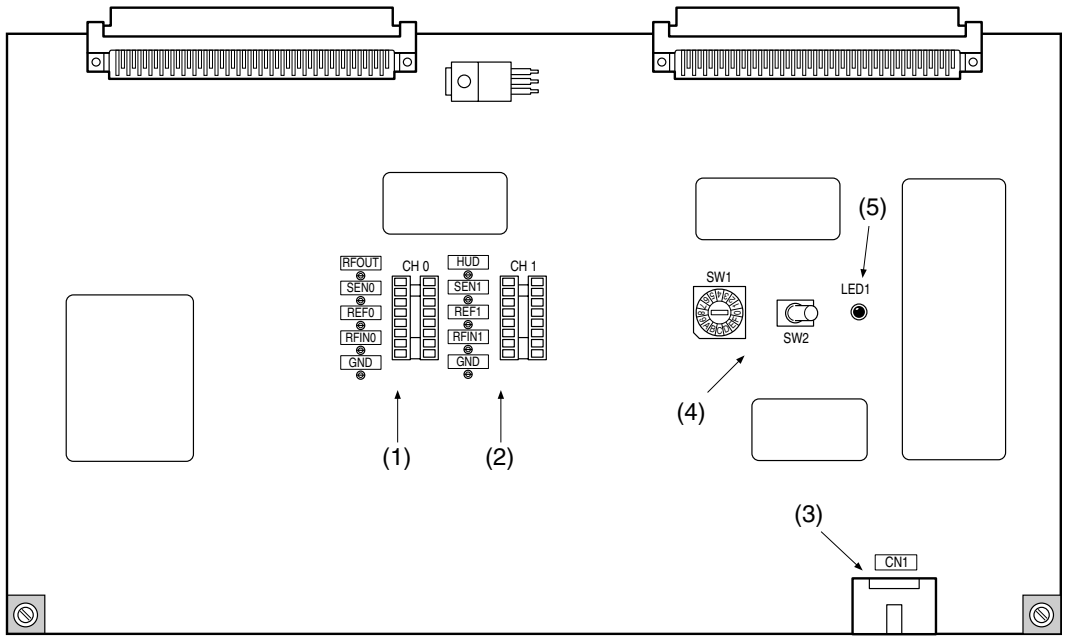


Figure B.1.2.1 S5U1C6F016P2

(1) R/F converter monitor pins and external part connecting socket (Channel 0)

These monitor pins are used to check the operation of R/F converter channel 0. The socket is used to connect external resistors and a capacitor for R/F conversion. Mount resistors and a capacitor on the platform attached with the S5U1C6F016P2 and then connect it to the onboard socket.

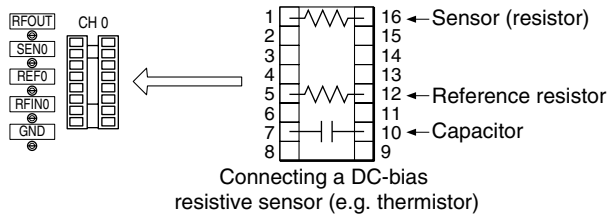
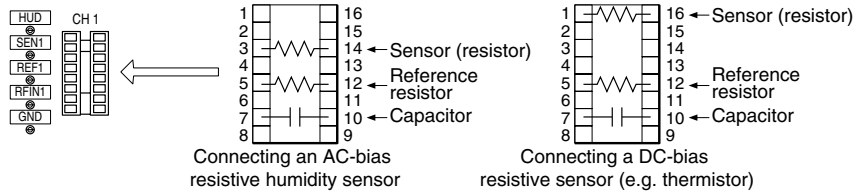


Figure B.1.2.2 R/F converter monitor pins and external part connecting socket (Channel 0)

(2) R/F converter monitor pins and external part connecting socket (Channel 1)

These monitor pins are used to check the operation of R/F converter channel 1. The socket is used to connect external resistors and a capacitor for R/F conversion. Mount resistors and a capacitor on the platform attached with the S5U1C6F016P2 and then connect it to the onboard socket.



The sensor connect position changes according to the sensor type to be used.
Do not mount an AC bias sensor and a DC bias sensor at the same time as it causes a malfunction.

Figure B.1.2.3 R/F converter monitor pins and external part connecting socket (Channel 1)

(3) CN1 (P5 I/O connector)

This is a user connector to input/output the P50 to P53 port signals. The P50 to P53 terminals of the actual IC are shared with the terminals for R/F converter channel 0. The S5U1C6F016P2 board provides this connector separated with the R/F converter socket and monitor pins shown in (1) above. Therefore, be sure to leave this connector open when R/F converter channel 0 is used. Furthermore, do not use this connector when the P50 to P53 ports are switched to SEG outputs by mask option.

(4) Supply voltage level setting switches for SVD (SW1, SW2)

These switches are used to set a supply voltage level for verifying the SVD operation. Table B.1.2.1 shows the relationship between the switch settings and the SVD control register. Note that these switches do not change the actual power supply voltage. These switches are intended to be used only for changing the detection results to debug whether the SVD routine works normally or not.

Table B.1.2.1 Relationship between SW1/SW2 settings and SVDS register

Switch settings		Supply voltage emulation level
SW1	SW2	
0	DETECTION	Voltage level < (SVDS[3:0] = 0)
1	DETECTION	(SVDS[3:0] = 0) ≤ Voltage level < (SVDS[3:0] = 1)
2	DETECTION	(SVDS[3:0] = 1) ≤ Voltage level < (SVDS[3:0] = 2)
3	DETECTION	(SVDS[3:0] = 2) ≤ Voltage level < (SVDS[3:0] = 3)
4	DETECTION	(SVDS[3:0] = 3) ≤ Voltage level < (SVDS[3:0] = 4)
5	DETECTION	(SVDS[3:0] = 4) ≤ Voltage level < (SVDS[3:0] = 5)
6	DETECTION	(SVDS[3:0] = 5) ≤ Voltage level < (SVDS[3:0] = 6)
7	DETECTION	(SVDS[3:0] = 6) ≤ Voltage level < (SVDS[3:0] = 7)
8	DETECTION	(SVDS[3:0] = 7) ≤ Voltage level < (SVDS[3:0] = 8)
9	DETECTION	(SVDS[3:0] = 8) ≤ Voltage level < (SVDS[3:0] = 9)
A	DETECTION	(SVDS[3:0] = 9) ≤ Voltage level < (SVDS[3:0] = 0AH)
B	DETECTION	(SVDS[3:0] = 0AH) ≤ Voltage level < (SVDS[3:0] = 0BH)
C	DETECTION	(SVDS[3:0] = 0BH) ≤ Voltage level < (SVDS[3:0] = 0CH)
D	DETECTION	(SVDS[3:0] = 0CH) ≤ Voltage level < (SVDS[3:0] = 0DH)
E	DETECTION	(SVDS[3:0] = 0DH) ≤ Voltage level < (SVDS[3:0] = 0EH)
F	DETECTION	(SVDS[3:0] = 0EH) ≤ Voltage level < (SVDS[3:0] = 0FH)
–	MAX	(SVDS[3:0] = 0FH) < Voltage level

Notes:
- The S1C63004/008/016 supports 32 detection levels for SVD (SVDS[4:0]). The S5U1C6F016P2 board supports only 16 supply voltage settings corresponding to SVDS[3:0], and cannot set levels including the SVDS4 setting. Use the supply voltage setting function assuming that SVDS4 is set to the same value as the register, and the SVDS4 register setting status should be checked with the register monitor LED/pin 15 (see Table B.1.1.1). To check the SVD operation when SVDS[4:0] = 0H to 0FH, the monitor LED/pin goes off/goes high; to check the SVD operation when SVDS[4:0] = 10H to 1FH, the monitor LED/pin lights/goes low.
- The S1C63003 has no SVD circuit included.

(5) SVD result LED (LED1)

This LED indicates the SVD results according to the SW1 and SW2 settings. The LED lights when the voltage level set using the switches is lower than the level set using the SVDS register (SVDDT = "1").

B.2 Connecting to the Target System

This section explains how to connect the target system.
First insert the S5U1C63000P6 board into the second upper slot of the ICE and the S5U1C6F016P2 board into the top slot. Download the circuit data to the S5U1C63000P6 board before installing the S5U1C6F016P2 board if the S5U1C63000P6 board does not include the correct circuit data. See Section B.3 for downloading circuit data.

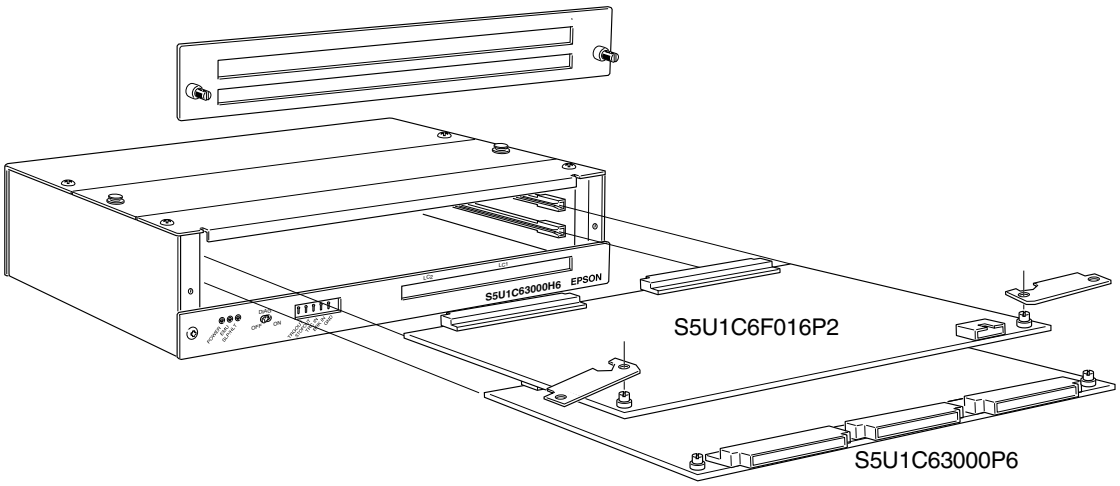


Figure B.2.1 Installing the peripheral circuit boards to the ICE

Installing the S5U1C63000P6/6F016P2 board

Set the jig included with the ICE into position as shown in Figure B.2.2. Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the board has been firmly fitted into the internal slot of the ICE, remove the jig.

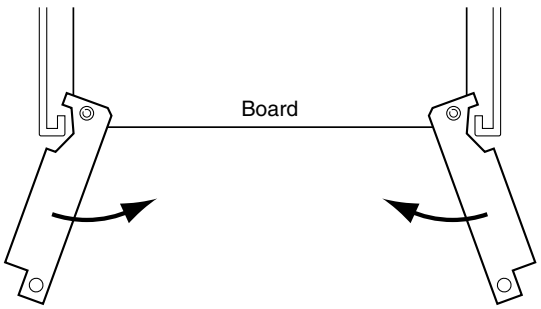


Figure B.2.2 Installing the board

Dismounting the S5U1C63000P6/6F016P2 board

Set the jig included with the ICE into position as shown in Figure B.2.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides. After confirming that the board has been dismounted from the backboard connector, pull the board out of the ICE.

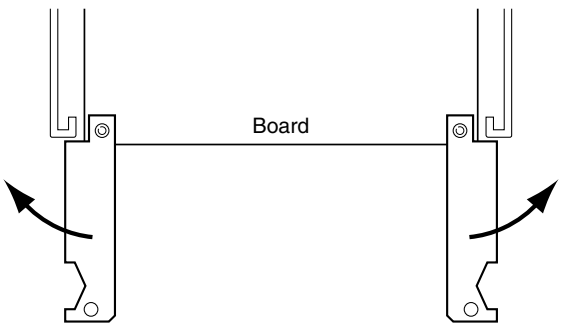


Figure B.2.3 Dismounting the board

To connect the S5U1C63000P6 and S5U1C6F016P2 to the target system, use the I/O connecting cables supplied with these boards. Take care when handling the connectors, since they conduct electrical power (V_{DD} = +3.3 V).

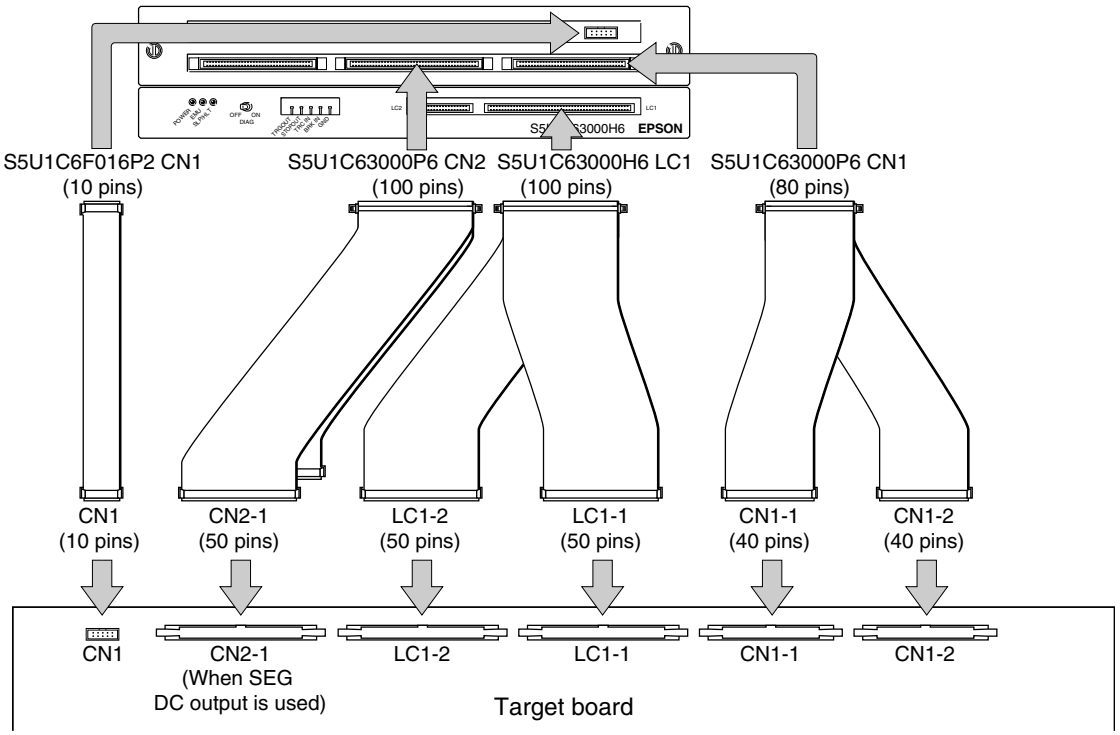


Figure B.2.4 Connecting the S5U1C63000P6 and S5U1C6F016P2 to the target system

Table B.2.1 S5U1C63000P6 CN1 connector pin assignment

40-pin CN1-1 connector			
No.	Pin name	No.	Pin name
1	V_{DD} (= 3.3 V)	21	V_{DD} (= 3.3 V)
2	V_{DD} (= 3.3 V)	22	V_{DD} (= 3.3 V)
3	Cannot be connected	23	P20
4	Cannot be connected	24	P21
5	Cannot be connected	25	P22
6	Cannot be connected	26	P23
7	Cannot be connected	27	P30
8	Cannot be connected	28	P31
9	Cannot be connected	29	P32
10	Cannot be connected	30	P33
11	V_{SS}	31	V_{SS}
12	V_{SS}	32	V_{SS}
13	P00	33	P40
14	P01	34	P41
15	P02	35	P42
16	P03	36	P43
17	P10	37	Cannot be connected
18	P11	38	Cannot be connected
19	P12	39	V_{SS}
20	P13	40	V_{SS}

40-pin CN1-2 connector			
No.	Pin name	No.	Pin name
1	V_{DD} (= 3.3 V)	21	V_{DD} (= 3.3 V)
2	V_{DD} (= 3.3 V)	22	V_{DD} (= 3.3 V)
3	Cannot be connected	23	Cannot be connected
4	Cannot be connected	24	Cannot be connected
5	Cannot be connected	25	Cannot be connected
6	Cannot be connected	26	Cannot be connected
7	Cannot be connected	27	Cannot be connected
8	Cannot be connected	28	Cannot be connected
9	Cannot be connected	29	Cannot be connected
10	Cannot be connected	30	Cannot be connected
11	V_{SS}	31	V_{SS}
12	V_{SS}	32	V_{SS}
13	Cannot be connected	33	Cannot be connected
14	Cannot be connected	34	Cannot be connected
15	Cannot be connected	35	Cannot be connected
16	Cannot be connected	36	Cannot be connected
17	Cannot be connected	37	Cannot be connected
18	Cannot be connected	38	RESET
19	Cannot be connected	39	V_{SS}
20	Cannot be connected	40	V_{SS}

Table B.2.2 S5U1C63000P6 CN2 connector pin assignment

50-pin CN2-1 connector			
No.	Pin name	No.	Pin name
1	V_{DD} (= 3.3 V)	26	SEG19 (DC)
2	V_{DD} (= 3.3 V)	27	SEG20 (DC)
3	SEG0 (DC)	28	SEG21 (DC)
4	SEG1 (DC)	29	SEG22 (DC)
5	SEG2 (DC)	30	SEG23 (DC)
6	SEG3 (DC)	31	V_{SS}
7	SEG4 (DC)	32	V_{SS}
8	SEG5 (DC)	33	SEG24 (DC)
9	SEG6 (DC)	34	SEG25 (DC)
10	SEG7 (DC)	35	SEG26 (DC)
11	V_{SS}	36	SEG27 (DC)
12	V_{SS}	37	SEG28 (DC)
13	SEG8 (DC)	38	SEG29 (DC)
14	SEG9 (DC)	39	SEG30 (DC)
15	SEG10 (DC)	40	SEG31 (DC)
16	SEG11 (DC)	41	V_{DD} (= 3.3 V)
17	SEG12 (DC)	42	V_{DD} (= 3.3 V)
18	SEG13 (DC)	43	SEG32 (DC)
19	SEG14 (DC)	44	SEG33 (DC)
20	SEG15 (DC)	45	SEG34 (DC)
21	V_{DD} (= 3.3 V)	46	SEG35 (DC)
22	V_{DD} (= 3.3 V)	47	Cannot be connected
23	SEG16 (DC)	48	Cannot be connected
24	SEG17 (DC)	49	Cannot be connected
25	SEG18 (DC)	50	Cannot be connected

50-pin CN2-2 connector			
No.	Pin name	No.	Pin name
1	V_{DD} (= 3.3 V)	26	Cannot be connected
2	V_{DD} (= 3.3 V)	27	Cannot be connected
3	Cannot be connected	28	Cannot be connected
4	Cannot be connected	29	Cannot be connected
5	Cannot be connected	30	Cannot be connected
6	Cannot be connected	31	V_{SS}
7	Cannot be connected	32	V_{SS}
8	Cannot be connected	33	Cannot be connected
9	Cannot be connected	34	Cannot be connected
10	Cannot be connected	35	Cannot be connected
11	V_{SS}	36	Cannot be connected
12	V_{SS}	37	Cannot be connected
13	Cannot be connected	38	Cannot be connected
14	Cannot be connected	39	Cannot be connected
15	Cannot be connected	40	Cannot be connected
16	Cannot be connected	41	V_{DD} (= 3.3 V)
17	Cannot be connected	42	V_{DD} (= 3.3 V)
18	Cannot be connected	43	Cannot be connected
19	Cannot be connected	44	Cannot be connected
20	Cannot be connected	45	Cannot be connected
21	V_{DD} (= 3.3 V)	46	Cannot be connected
22	V_{DD} (= 3.3 V)	47	Cannot be connected
23	Cannot be connected	48	Cannot be connected
24	Cannot be connected	49	Cannot be connected
25	Cannot be connected	50	Cannot be connected

* The CN2-1 connector outputs the signals from the SEG pins that have been configured as DC outputs by mask option. Do not connect anything to the SEG pins that have been configured as LCD drive outputs.

Table B.2.3 S5U1C63000H6 LC1 connector pin assignment

50-pin LC1-1 connector			
No.	Pin name	No.	Pin name
1	COM0	26	SEG17
2	COM1	27	SEG18
3	COM2	28	SEG19
4	COM3	29	SEG20
5	COM4	30	SEG21
6	COM5	31	SEG22
7	COM6	32	SEG23
8	COM7	33	SEG24
9	SEG0	34	SEG25
10	SEG1	35	SEG26
11	SEG2	36	SEG27
12	SEG3	37	SEG28
13	SEG4	38	SEG29
14	SEG5	39	SEG30
15	SEG6	40	SEG31
16	SEG7	41	SEG32
17	SEG8	42	SEG33
18	SEG9	43	SEG34
19	SEG10	44	SEG35
20	SEG11	45	SEG36
21	SEG12	46	SEG37
22	SEG13	47	SEG38
23	SEG14	48	SEG39
24	SEG15	49	SEG40
25	SEG16	50	SEG41

50-pin LC1-2 connector			
No.	Pin name	No.	Pin name
1	SEG42	26	Cannot be connected
2	SEG43	27	Cannot be connected
3	SEG44	28	Cannot be connected
4	SEG45	29	Cannot be connected
5	SEG46	30	Cannot be connected
6	SEG47	31	Cannot be connected
7	SEG48	32	Cannot be connected
8	SEG49	33	Cannot be connected
9	SEG50	34	Cannot be connected
10	SEG51	35	Cannot be connected
11	SEG52	36	Cannot be connected
12	SEG53	37	Cannot be connected
13	SEG54	38	Cannot be connected
14	SEG55	39	Cannot be connected
15	Cannot be connected	40	Cannot be connected
16	Cannot be connected	41	Cannot be connected
17	Cannot be connected	42	Cannot be connected
18	Cannot be connected	43	Cannot be connected
19	Cannot be connected	44	Cannot be connected
20	Cannot be connected	45	Cannot be connected
21	Cannot be connected	46	Cannot be connected
22	Cannot be connected	47	Cannot be connected
23	Cannot be connected	48	Cannot be connected
24	Cannot be connected	49	Cannot be connected
25	Cannot be connected	50	Cannot be connected

Table B.2.4 S5U1C6F016P2 CN1 connector pin assignment

10-pin CN1 connector	
No.	Pin name
1	V_{DD} (= 3.3 V)
2	V_{DD} (= 3.3 V)
3	P50
4	P51
5	P52
6	P53
7	Cannot be connected
8	Cannot be connected
9	V_{SS}
10	V_{SS}

Notes: • When developing an S1C63003 application, the connector pins shown below should not be connected to the target board.
40-pin CN1-1: No. 27–30 (P30–P33), No. 33–36 (P40–P43)
50-pin CN2-1: No. 15–20 (SEG10–SEG15), No. 23–30 (SEG16–SEG23), No. 33–40 (SEG24–SEG31), No. 43–46 (SEG32–SEG35)
50-pin LC1-1: No. 19–50 (SEG10–SEG41)
50-pin LC1-2: No. 1–2 (SEG42–SEG43)

• When developing an S1C63004 application, the connector pins shown below should not be connected to the target board.
40-pin CN1-1: No. 33–36 (P40–P43)
50-pin CN2-1: No. 27–30 (SEG20–SEG23), No. 33–40 (SEG24–SEG31), No. 43–46 (SEG32–SEG35)
50-pin LC1-1: No. 29–48 (SEG20–SEG39)

• When developing an S1C63008 application, the connector pins shown below should not be connected to the target board.
50-pin CN2-1: No. 39–40 (SEG30–SEG31), No. 43–46 (SEG32–SEG35)
50-pin LC1-1: No. 39–44 (SEG30–SEG35)

B.3 Downloading to S5U1C63000P6

Note: The S1C630 Series circuit data is available only for the S5U1C63000P6, and it cannot be downloaded to the previous S5U1C63000P1 board.

Downloading Circuit Data – when new ICE (S5U1C63000H2/S5U1C63000H6) is used

The S5U1C63000P6 board comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

(1) Remove the ICE (S5U1C63000H2/S5U1C63000H6) top cover and then set the DIP switch "IOSEL2" on the S5U1C63000P6 board to the "E" position.

(2) Connect the ICE to the host PC. Then turn the host PC and ICE on.

(3) Invoke the debugger included in the assembler package (ver. 5 or later for the S5U1C63000H2, ver. 9 or later for the S5U1C63000H6). For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.

(4) Download the circuit data file (.mot) corresponding to the model by entering the following commands in the command window.

```
>XFER                          (erase all)
>XFWR   <file name>            (download the specified file)*
>XFCP   <file name>            (compare the specified file and downloaded data)
```

* The downloading takes about 15 minutes in the S5U1C63000H2 or about 3 minutes in the S5U1C63000H6.

(5) Terminate the debugger and then turn the ICE off.

(6) Set the DIP switch "IOSEL2" on the S5U1C63000P6 board to the "D" position.

(7) Turn the ICE on and invoke the debugger again. Debugging can be started here.

B.4 Usage Precautions

To ensure correct use of the peripheral circuit board, please observe the following precautions.

B.4.1 Operational precautions

(1) Before inserting or removing cables, turn off power to all pieces of connected equipment.

(2) Do not turn on power or load mask option data if all of the I/O ports (P00–P03) are held high. Doing so may activate the multiple key entry reset function.

(3) Before debugging, always be sure to load mask option data.

B.4.2 Differences with the actual IC

(1) Differences in I/O

<Interface power supply>

This tool and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a circuit such as a level shifter on the target system side to accommodate the required interface voltage.

<Output port drive capability>

The drive capability of each output port on this tool is higher than that of the actual IC. When designing application system and software, refer to "Electrical Characteristics" to confirm each output port's drive capability.

<Port protective diode>

All I/O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between this tool and the target system are set to +3.3 V. Therefore, this tool and the target system cannot be interfaced with voltages exceeding V_{DD} by setting the output ports for open-drain mode.

<Pull-down resistance value>

The pull-down resistance values on this tool are set to 220 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to "Electrical Characteristics."
Note that when using pull-down resistors to pull the input pins low, the input pins may require a certain period to reach a valid low level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since fall delay times on these input ports differ from those of the actual IC.

<Schmitt input>

The P00–P03 and P10–P13 ports of the actual IC can be configured to Schmitt level input interface. The P20–P23, P30–P33, P40–P43, and P50–P53 ports support Schmitt level input interface only. This tool supports CMOS level interface only and does not supports Schmitt inputs.

Note: The P40–P43 ports do not exist in the S1C63004. The P30–P33 and P40–P43 ports do not exist in the S1C63003.

(2) Differences in current consumption

The amount of current consumed by this tool is different significantly from that of the actual IC. Inspecting the LEDs on S5U1C63000P6 may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

<Those which can be verified by LEDs and monitor pins>

(a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
(b) OSC3 oscillation on/off circuit (OSCC)
(c) CPU clock select circuit (CLKCHG)
(d) SVD circuit on/off circuit (SVDON)

<Those that can only be counteracted by system or software>

(e) Current consumed by the internal pull-down resistors
(f) Input ports in a floating state

(3) Functional precautions

<LCD driver>

Use the LC1 connector (max. 56SEG × 8COM) on the ICE (S5U1C63000H2/S5U1C63000H6) to drive an LCD panel. Do not connect anything to the connector pins shown below.

- SEG pins that do not exist on the actual IC) or unused SEG pins
- SEG pins configured for DC output by mask option (Use the S5U1C63000P6 CN2 connector.)
- Pins configured for I/O port or R/F converter (SEG36–SEG55)

For other precautions on LCD drive outputs, refer to the ICE manual.

<SVD circuit>

- The SVD function in this tool sets the detection results by comparing the SVDS[3:0] register value with the settings of the SW1 and SW2 on S5U1C6F016P2 without changing the supply voltage.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. There is no delay in this tool, which differs from that of the actual IC. Refer to "Electrical Characteristics" when setting the appropriate wait time for the actual IC.

Note: The S1C63003 has no SVD circuit included.

<Oscillation circuit>

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. In this tool, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to "Electrical Characteristics" when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If these operations are executed simultaneously with a single instruction, although this tool functions normally, may not function properly in the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts in this tool differs from that of the actual IC.
- This tool includes oscillation circuits for OSC1 and OSC3. Note that the OSC3 oscillation circuit in this tool can generate the OSC3 clock even if no resonator is connected.
- The oscillation frequencies in this tool are as follows:
  - OSC1 oscillation circuit (crystal): Fixed at 32.768 kHz
  - OSC3 oscillation circuit (CR): About 100 kHz to 8 MHz (The OSC3 frequency is adjustable. Set it to the frequency used in the actual product.)

<Access to undefined address space>

If any undefined space in the actual IC's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between this tool and the actual IC. Note that the ICE incorporates the program break function caused by accessing to an undefined address space.

Note: In the S1C63003, no program break occurs when an undefined address space from 0080H to 00FFH is accessed. Therefore, set a data break condition to this area or take other measures when creating the program.

<Reset circuit>

Keep in mind that the operation sequence from when the ICE and the peripheral circuit boards (S5U1C63000P6 and S5U1C6F016P2) are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because S5U1C63000P6 becomes capable of operating as a debugging system after the user program and optional data are downloaded.

When operating the ICE after placing it in free-running mode*, always apply a system reset. A system reset can be performed by pressing the reset switch on S5U1C63000P6, by a reset pin input, or by holding the input ports high simultaneously. (* Free running mode: supported by S5U1C63000H1/2 only)

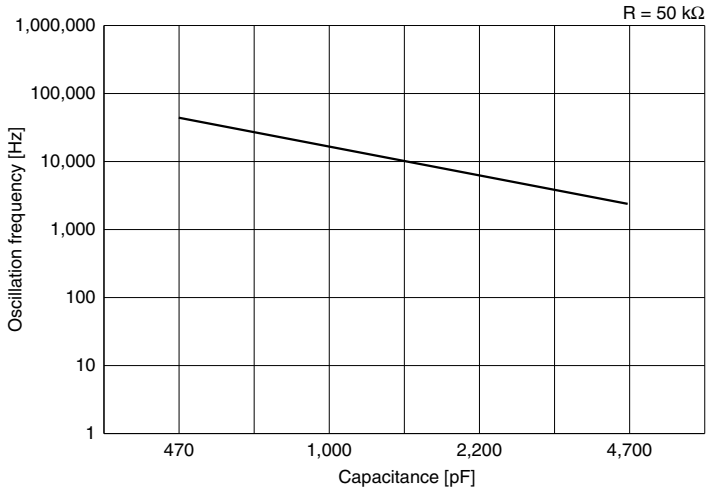
<I/O ports>

Do not set the P0x ports used for multiple key entry reset to output mode as this tool may be reset.

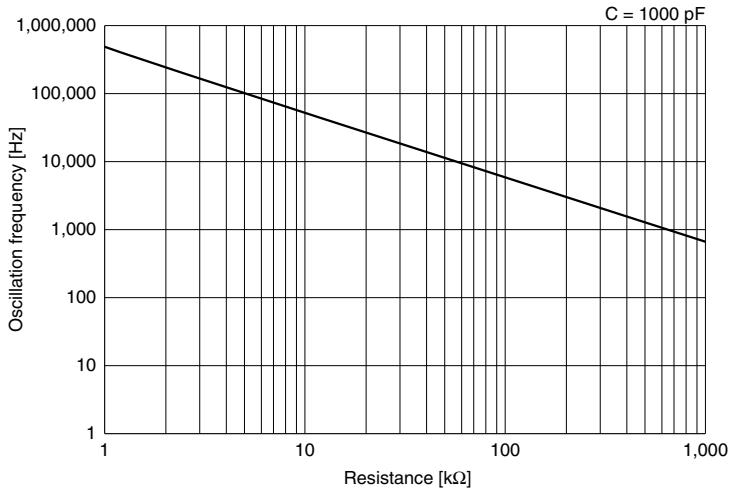
<R/F converter>

- The R/F converter function is implemented using the S1C6F016 chip included in the S5U1C6F016P2 board.
- If the debugger makes program execution to break while the R/F converter is counting the oscillation, the R/F converter does not stop counting. Note that the R/F converter will not able to load a proper result if program execution is resumed from that point.
- The following shows the oscillation characteristics (reference value) of the R/F converter on the S5U1C6F016P2:

R/F converter oscillation frequency - capacitance characteristic (reference value)



R/F converter oscillation frequency - resistance characteristic (reference value)



B.5 Product Specifications

B.5.1 Specifications of S5U1C63000P6

S5U1C63000P6

Dimension:	254 mm (wide) × 144.8 mm (depth) × 16 mm (height) (including screws)
Weight:	Approx. 250 g
Power supply:	DC 5 V ± 5%, less than 1 A (supplied from ICE main unit)

I/O connection cable (80-pin)

S5U1C63000P6 connector:	KEL8830E-080-170L-F
Cable connector (80-pin):	KEL8822E-080-171-F
Cable connector (40-pin):	3M7940-6500SC 1 pair
Cable:	40-conductor flat cable (1 pair)
Interface:	CMOS interface (3.3 V)
Length:	Approx. 40 cm

I/O connection cable (100-pin)

S5U1C63000P6 connector:	KEL8830E-100-170L-F
Cable connector (100-pin):	KEL8822E-100-171-F
Cable connector (50-pin):	3M7950-6500SC 1 pair
Cable:	50-conductor flat cable (1 pair)
Interface:	CMOS interface (3.3 V)
Length:	Approx. 40 cm

Accessories

40-pin connector for connecting to target system: 3M3432-6002LCPL × 2
50-pin connector for connecting to target system: 3M3433-6002LCPL × 2

B.5.2 Specifications of S5U1C6F016P2

S5U1C6F016P2

Dimension:	254 mm (width) × 144.8 mm (depth) × 13 mm (height) (including screws)
Weight:	Approx. 170 g
Power supply:	DC 5 V ± 5%, less than 50 mA (supplied from ICE main unit and converted into 3.3 V by the onboard regulator)

I/O connection cable (10-pin)

S5U1C6F016P2 connector:	3M3654-5002-PL
Cable connector (10-pin):	3M7910-6500SC
Cable:	10-conductor flat cable
Interface:	CMOS interface (3.3 V)
Length:	Approx. 40 cm

Accessories

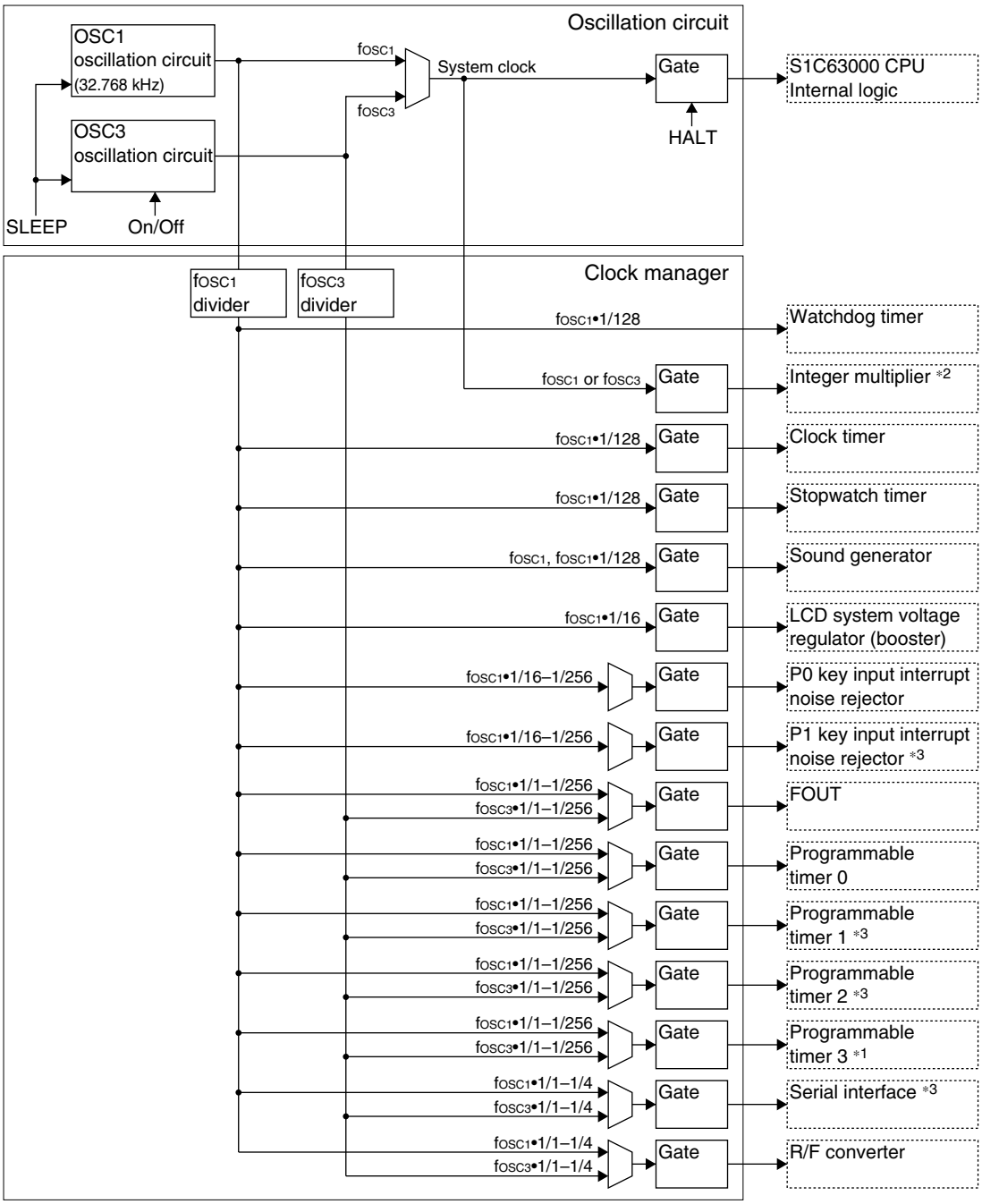
10-pin connector for connecting to target system: 3M3662-6002LCPL × 1
Discreet platform (for mounting external resistors and capacitors of the R/F converter): DIS12-016-403 (KEL) × 2

Appendix C Power Saving

Current consumption will vary dramatically, depending on CPU operating mode, operation clock frequency, and the peripheral circuits being operated. Listed below are the control methods for saving power.

C.1 Power Saving by Clock Control

Figure C.1.1 illustrates the S1C63003/004/008/016 clock system.



*1 S1C63016 only *2 S1C63008/016 only *3 S1C63004/008/016 only

Figure C.1.1 Clock system

This section describes clock systems that can be controlled via software and power-saving control details. For more information on control registers and control methods, refer to the respective peripheral circuit sections.

System SLEEP (All clocks stopped)

- Execute the SLP instruction (CPU)
  Execute the SLP instruction when the entire system can be stopped. The CPU enters SLEEP mode and the OSC1 and OSC3 oscillation circuits stop. This also stops all peripheral circuits using clocks. Starting up the CPU from SLEEP mode is therefore limited to startup using a port (described later).

System clock

- Clock source selection (oscillation circuit)
  Select between OSC3 and OSC1 for the system clock source. Reduce current consumption by selecting the OSC1 clock when low-speed processing is possible.
  Control register: CLKCHG
  Default setting: CLKCHG = "0" (operated with the OSC1 clock)

- OSC3 oscillator circuit stop (oscillation circuit)
  Operate the oscillation circuit comprising the system clock source. Where possible, stop the other oscillation circuit. You can reduce current consumption by using OSC1 as the system clock and stopping the OSC3 oscillation circuit.
  Control register: OSCC
  Default setting: OSCC = "0" (OSC3 oscillation off)

CPU clock

- Execute the HALT instruction (CPU)
  Execute the HALT instruction when program execution by the CPU is not required—for example, when only the display is required or for interrupt standby. The CPU enters HALT mode and suspends operations, but the peripheral circuits maintain the status in place at the time of the HALT instruction, enabling use of peripheral circuits for timers and interrupts. You can reduce power consumption even further by suspending unnecessary oscillation circuit and peripheral circuits before executing the HALT instruction. The CPU is started from HALT mode by an interrupt from a port or the peripheral circuit operating in HALT mode.

Peripheral circuit clocks

- Stop clock supply to the peripheral circuits (clock manager)
  The S1C63003/004/008/016 incorporates a clock manager to control the clock supply to the peripheral circuits. Stop the clock supply to the unused peripheral circuits to reduce current consumption.
  The table below lists the peripheral circuits of which the operating clock can be stopped.

Table C.1.1 Peripheral circuits with clock control

Peripheral circuit/function	Stop control	Frequency selection	Clock control register
FOUT output	Possible	Possible	FOUT[3:0]
Key input interrupt noise rejector (P00 to P03)	Possible	Possible	NRSP0[1:0]
Key input interrupt noise rejector (P10 to P13) *3	Possible	Possible	NRSP1[1:0]
LCD system voltage regulator (booster clock)	Possible	–	VCCKS[1:0]
Serial interface *3	Possible	Possible	SIFCKS[2:0]
R/F converter	Possible	Possible	RFCKS[2:0]
Programmable timer 0	Possible	Possible	PTPS0[3:0]
Programmable timer 1 *3	Possible	Possible	PTPS1[3:0]
Programmable timer 2 *3	Possible	Possible	PTPS2[3:0]
Programmable timer 3 *1	Possible	Possible	PTPS3[3:0]
Clock timer	Possible	–	RTCKE
Stopwatch timer	Possible	–	SWCKE
Sound generator	Possible	–	SGCKE
Integer multiplier *2	Possible	–	MDCKE

*1 S1C63016 only *2 S1C63008/016 only *3 S1C63004/008/016 only

- Use low-speed clocks (clock manager)
  Reduce current consumption by setting the clock for the peripheral circuit that supports clock frequency selection as low as possible.

Table C.1.2 shows a list of methods for clock control and starting/stopping the CPU.

Table C.1.2 Clock control list

Current consumption	OSC1	OSC3	CPU clock	Peripheral (OSC3)	Peripheral (OSC1)	CPU stop method	CPU startup method
↑ Low	Stop	Stop	Stop	Stop	Stop	Execute SLP instruction	1
	Oscillation (system CLK)	Stop	Stop	Stop	Run	Execute HALT instruction	1, 2
	Oscillation (system CLK)	Stop	Stop	Run	Run	Execute HALT instruction	1, 2, 3
	Oscillation (system CLK)	Stop	Run	Run	Run		
	Oscillation	Oscillation (system CLK)	Stop	Run	Run	Execute HALT instruction	1, 2, 3
High ↓	Oscillation	Oscillation (system CLK)	Run	Run	Run		

HALT and SLEEP mode cancelation methods (CPU startup method)

1. Startup by a port
   Started up by a key input interrupt.
2. Startup by a peripheral circuit being operated with the OSC1 clock
   Started up by an interrupt from the clock timer, stopwatch timer, watchdog timer or a peripheral circuit being operated with an OSC1 dividing clock.
3. Startup by a peripheral circuit
   Started up by a peripheral circuit interrupt.

C.2 Power Saving by Power Supply Control

The available power supply controls are listed below.

Internal operating voltage regulator

- Note that turning on internal operating voltage regulator heavy load protection will increase current consumption. Turn off heavy load protection for normal operations. Turn on only if operations are unstable.

LCD system voltage regulator

- Turning on the LCD system voltage regulator heavy load protection will increase current consumption. Turn off heavy load protection for normal operations. Turn on only if the display is unstable.
- If no LCD display is being used, turn off the LCD system voltage regulator.

Supply voltage detection (SVD) circuit [S1C63004/008/016]

- Operating the SVD circuit will increase current consumption. Turn off power supply voltage detection unless it is required.

Appendix D Mask Data Creation Procedure

This chapter shows a procedure to create an S1C630 Series (S1C63003/004/008/016) mask data file (PA*x*) for submission to Seiko Epson. Use the appropriate device information definition file according to the model to be used.

Note: Before creating the mask data file, get the latest device information definition file package listed below from our website. *1
S1C63003 device information definition file version 5.0 or later
S1C63004 device information definition file version 6.0 or later
S1C63008 device information definition file version 4.0 or later
S1C63016 device information definition file version 1.0 or later

D.1 Mask Data Creation Flowchart

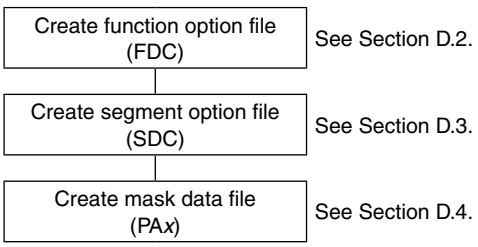


Figure D.1.1 Mask data creation flowchart

D.2 Function Option File Creation Procedure

The following shows a procedure to create a function option file:

1. Launch the function option generator (winfog.exe).
2. Load the device information definition file (INI).
   Select "Device INI select" from the "Tool (T)" menu or click the "Device INI select" button.
   When the dialog box appears, select the folder and file (INI) for the target model.
   - Folder: 630*xx* *2
   - File: 630*xx*.INI *2
3. Set up information such as the output folder/file name.
   Select "Setup (S)" from the "Tool (T)" menu or click the "Setup" button.
   Enter the information required through the dialog box appeared.
4. Select options to be used.
5. Generate the function option files (FDC, FSA).
   Select "Generate (G)" from the "Tool (T)" menu or click the "Generate" button.
   The function option files will be generated.

D.3 Segment Option File Creation Procedure

The following shows a procedure to create a segment option file:

1. Launch the segment option generator (winsog.exe).
2. Load the device information definition file (INI).
   Select "Device INI select" from the "Tool (T)" menu or click the "Device INI select" button.
   When the dialog box appears, select the folder and file (INI) for the target model.
   - Folder: 630*xx* *2
   - File: 630*xx*.INI *2

3. Set up information such as the output folder/file name.
   Select "Setup (S)" from the "Tool (T)" menu or click the "Setup" button.
   Enter the information required through the dialog box appeared.
4. Load a segment assignment data file (SAD).
   Select "Record (R) → Load (L)" from the "Fie (F)" menu or click the "Load" button.
   When the dialog box appears, select the folder and file (SAD) for the target model.
   - Folder: 630*xx* *2
   - File: 630*xx*.SAD *2

Note: The area that allows configuration of segment assignment and output specification is restricted as shown in Figure D.3.1. Assignment must be performed within the assignable area only.

Area that cannot be assigned (unavailable SEG terminals)
Fixed specification area

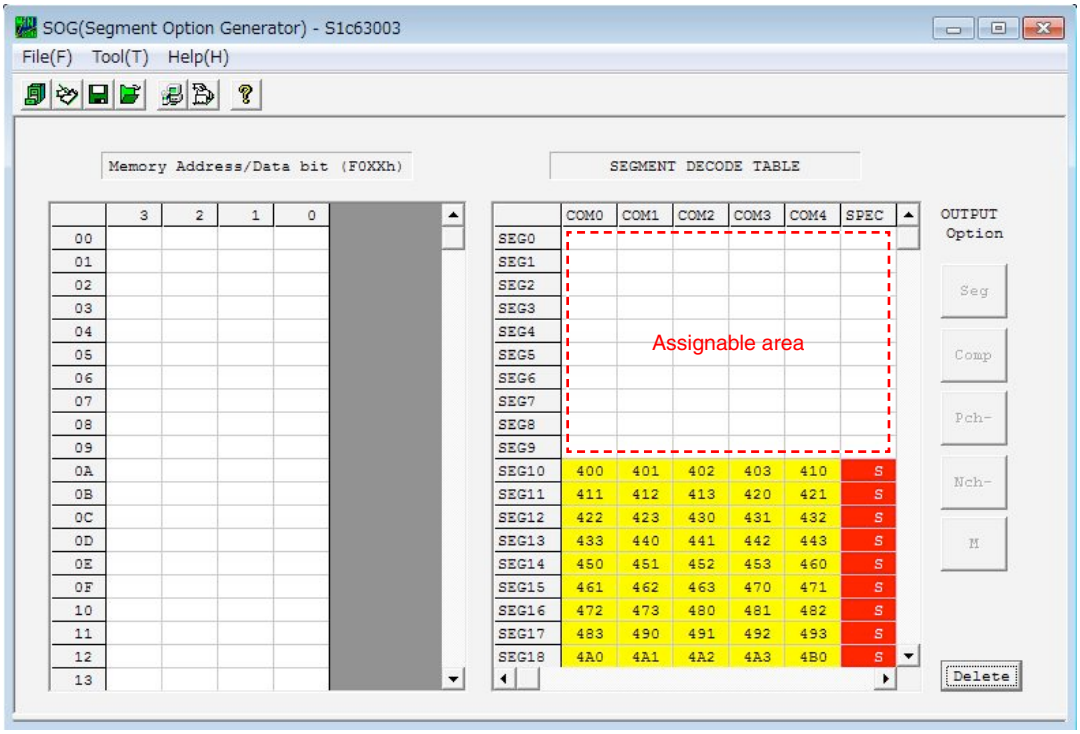


Figure D.3.1 Sample segment assignment area

5. Segment assignment
   Assign addresses/data bits to the assignable area according to the system design.
6. Generate the segment option files (SDC, SSA).
   Select "Generate (G)" from the "Tool (T)" menu or click the "Generate" button.
   The segment option files will be generated.

D.4 Mask Data File Creation Procedure

The following shows a procedure to create a mask data file:

1. Launch the mask data checker (winmdc.exe).
2. Load the device information definition file (INI).
   Select "Device INI select" from the "Tool (T)" menu or click the "Device INI select" button.
   When the dialog box appears, select the folder and file for the target model.
   - Folder: 630*xx* *2
   - File: 630*xx*.INI *2

3. Select ROM data files and option document files.
   Select "Pack (P)" from the "Tool (T)" menu or click the "Pack" button on the toolbar.
   When the dialog box appears, select the files required for generating the mask data file.
   - Folder: 630*xx* *2
     or another folder in which the files listed below are stored
   - File: *zzzzzzzz*.HSA created by the user
     zzzzzzzz.LSA created by the user
     zzzzzzzz.CSA created by the user
     zzzzzzzz.FDC created by the user
     zzzzzzzz.SDC created by the user
4. Generate the mask data file (PAx).
   Click the "Pack" button in the dialog box that appears in Step 3.
   The mask data file will be generated.

For details of the function option generator, segment option generator, and mask data checker, refer to the "S5U1C63000A Manual."

∗1 When mask data has already been created using an earlier version of device information definition file
Refer to the segment option for each model described in this manual and check that there is no assignment setting as below in the segment option file.
- An available area is assigned to the SEG terminals that do not exist.
- An unavailable area is assigned to the SEG terminals to be used.

If there is a such assignment as above, create the segment option file and mask data with the correct assignment once again using the latest device information definition file.

∗2 Included in the device information definition file package downloaded.

Appendix E Summary of Notes

E.1 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

- Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed.
- Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.
- The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1). 16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH, 0100H to 017FH in the S1C63003). Memory accesses except for stack operations by SP1 are 4-bit data access.
  The stack address management requires caution as the stack pointers may be set to an address out of the RAM address range.
  After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Power control

- When a 3.0 V LCD drive voltage is supplied to the V_{C3} or V_{C2} terminal in the 1.5 V low-voltage type, use separated power sources for V_{DD} and V_{C3}/V_{C2} and supply a voltage within 1.1 V to 1.7 V to the V_{DD} terminal.
- Do not use the V_{D1}, V_{OSC} and V_{C1} to V_{C3} terminal output voltages to drive external circuits.
- The LCD system voltage regulator takes about 100 msec for stabilizing the LCD drive voltages after writing "1" to LPWR.
- Do not select the reference voltage V_{C2} for the S1C63003 1.5 V low-voltage type.
- Current consumption increases in heavy load protection mode, therefore do not set heavy load protection mode with software if unnecessary.

Interrupt

- The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0."
- After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.
- The interrupt handler routine must be located within the range from "Interrupt vector address (100H–10FH)" -7FH to +80H. If it is difficult, make a relay point within that range as the destination of the vector jump and branch the program to the interrupt handler from there.
- Both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

Oscillation circuit

- When high speed CPU operations are not necessary, you should operate the peripheral circuits with the setting shown below.
  - CPU operating clock: OSC1
  - OSC3 oscillation circuit: Off (When the OSC3 clock is not necessary for peripheral circuits.)
  - Clock manager: Disable the clock supply to unnecessary peripheral circuits.
- Since several tens of μsec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit on. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes on. The oscillation start time will vary somewhat depending on the resonator and externally attached parts. Refer to the oscillation start time example indicated in the "Electrical Characteristics" chapter.
- When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation off with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.
- Both the OSC1 and OSC3 oscillation circuits stop oscillating when the CPU enters SLEEP mode. To prevent the CPU from a malfunction when it resumes operating from SLEEP mode, switch the CPU clock to OSC1 before placing the CPU into SLEEP mode.

Watchdog timer

- When the watchdog timer is being used, the software must reset it within 3-second cycles.
- Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Clock timer

- Be sure to read timer data in the order of low-order data (TM[3:0]) then high-order data (TM[7:4]).
- The clock timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the clock timer count data should be read by one of the procedures shown below.
  - Read the count data twice and verify if there is any difference between them.
  - Temporarily stop the clock timer when the counter data is read to obtain proper data.
- When resetting the clock timer (TMRST = "1"), do not start the clock timer (TMRUN = "1") simultaneously. If both control bits are set to "1," the clock timer may not reset properly.

Stopwatch timer

- The interrupt factor flag should be reset after resetting the stopwatch timer.
- Be sure to data reading in the order of SWD[3:0] → SWD[7:4] → SWD[11:8].
- When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD[11:8] and check whether the data has been renewed or not. (S1C63004/008/016)
- When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not. (S1C63004/008/016)

Programmable timer

- When reading counter data, be sure to read the low-order 4 bits (PTDx[3:0]) first. The high-order 4 bits (PTDx[7:4]) are latched when the low-order 4 bits are read and they are held until the next reading of the low-order 4 bits. In 16-bit timer mode, the high-order 12 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first. When the CPU is running with the OSC1 clock and the programmable timer is running with the OSC3 clock, stop the timer before reading the counter data to read the proper data.
- The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.

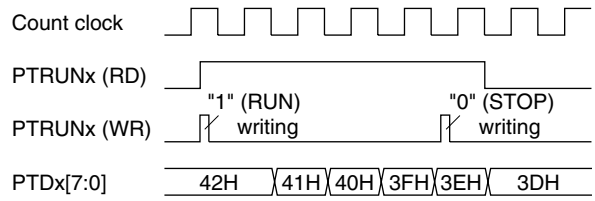


Figure E.1.1 Timing chart for RUN/STOP control (timer mode)

In event counter mode, the timer starts counting at the first event clock.

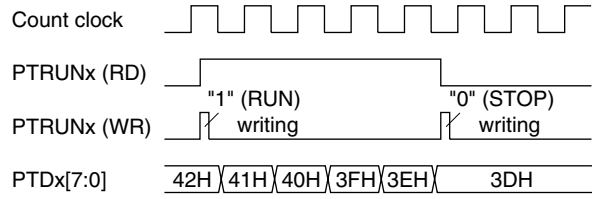


Figure E.1.2 Timing chart for RUN/STOP control (event counter mode)

- Since the TOUT_A/TOUT_B signal is generated asynchronously from the PTOUT_A/PTOUT_B register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
- When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation on, prior to using the programmable timer. However the OSC3 oscillation circuit requires several tens of μsec to several tens of msec after turning the circuit on until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit on to starting the programmable timer. Refer to the "Oscillation Circuit and Clock Control" chapter, for the control and notes of the OSC3 oscillation circuit.
  At initial reset, the OSC3 oscillation circuit is set in off state.
- For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
  The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

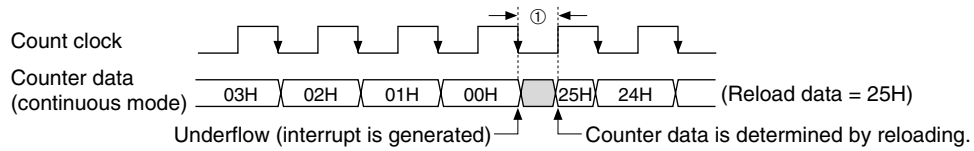


Figure E.1.3 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

- The programmable timer count clock does not synch with the CPU clock. Therefore, the correct value may not be obtained depending on the count data read and count-up timings. To avoid this problem, the programmable timer count data should be read by one of the procedures shown below.
  - Read the count data twice and verify if there is any difference between them.
  - Temporarily stop the programmable timer when the counter data is read to obtain proper data.

I/O port

- When an I/O ports in input mode is changed from high to low by the pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
  Particular care needs to be taken of the key scan during key matrix configuration.
  Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 15 pF + parasitic capacitance ? pF
R: pull-down resistance 500 kΩ (Max.)

- Be sure to turn the noise rejector off before executing the SLP instruction.
- Reactivating from SLEEP status can only be done by generation of a key input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt select register (SIPxx = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the key input interrupt using the corresponding interrupt mask register (EIKxx = "1") before executing the SLP instruction to run key input interrupt handler routine after SLEEP status is released.
- Before the port function is configured, the circuit that uses the port (e.g. input interrupt, multiple key entry reset, serial interface, R/F converter, event counter input, direct RUN/LAP input for stopwatch) must be disabled.

Serial interface (S1C63004/008/016)

- Perform data writing/reading to the data registers SD[7:0] only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).
- As a trigger condition, it is required that data writing or reading on data registers SD[7:0] be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD[7:0].) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
  Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.
- Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD[7:0].
- Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when the programmable timer is used as the clock source or the serial interface is used in slave mode.

LCD driver

- Make sure the LCD display is off (LPWR = "0") before setting the frame frequency. If the frame frequency is switched when the LCD display is on (LPWR = "1"), the LCD may not display normally for one frame period after switching.
- The frame frequency affects the display quality. We recommend that the frame frequency should be determined after the display quality is evaluated using the actual LCD panel.
- At initial reset, the contents of display memory are undefined and LC[3:0] (LCD contrast) is set to "0," therefore, it is necessary to initialize those contents by software. Also note that the LPWR and DSPC[1:0] registers are set to turn the display off.
- When Pxx (P20 to P53) and R/F converter terminals are used as the segment terminals by selecting mask option, do not alter the Pxx port and R/F converter control registers that affect these terminals from their initial values.

Sound generator

- Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.
- The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

R/F converter

- When an error interrupt occurs, reset the overflow flag (OVMC or OVTC) by writing "1." The same error interrupt will occur again if the overflow flag is not reset.

- When setting the measurement counter or time base counter, always write 5 words of data continuously in order from the lower address (FF62H → FF63H → FF64H → FF65H → FF66H, FF67H → FF68H → FF69H → FF6AH → FF6BH). Furthermore, an LD instruction should be used for writing data to the measurement counter and a read-modify-write instruction (AND, OR, ADD, SUB, etc.) cannot be used. If data other than low-order 4 bits is written, the counter cannot be set to the desired value.
- The reference and sensor oscillation frequency IC deviation of the R/F converter may increase due to variations in resistances and capacitances, and board conditions. The 1.5 V low-voltage type is especially sensitive. Take this into consideration and perform evaluations sufficiently when using the R/F converter.
  For the IC deviation, see "Characteristics Curves (RFC reference/sensor oscillation frequency - resistance characteristic)" in Chapter 19, "Electrical Characteristics."

SVD circuit (S1C63004/008/016)

- To obtain a stable detection result, the SVD circuit must be on for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.
  1. Set SVDON to "1"
  2. Maintain for 500 µsec minimum
  3. Set SVDON to "0"
  4. Read SVDDT
- The SVD circuit should normally be turned off because SVD operation increase current consumption.

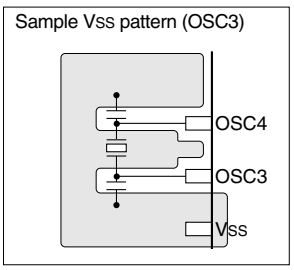
Integer multiplier (S1C63008/016)

An operation process takes 10 CPU clock cycles (5 bus cycles) after writing to the calculation mode select register CALMD until the operation result is set to the destination register DRH/DRL and the operation flags. While this operation is in process, do not read/write from/to the destination register DRH/DRL and do not read NF/VF/ZF.

E.2 Precautions on Mounting

Oscillation circuit

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:
  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.
  (2) As shown in the right hand figure, make a Vss pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this Vss pattern for any purpose other than the oscillation system.



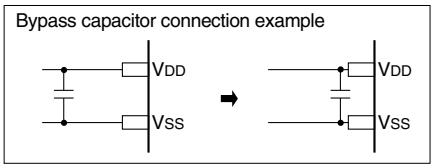
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

Reset circuit

- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.). Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When using the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

Power supply circuit

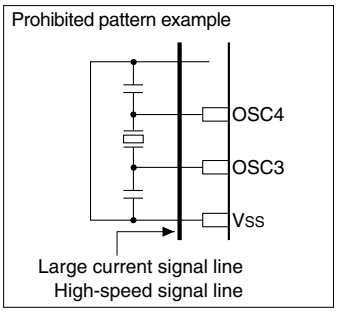
- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:
  (1) The power supply should be connected to the VDD and VSS terminals with patterns as short and large as possible.
  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1, VOSC and VC1–VC3 terminals, such as capacitors, should be connected in the shortest line. In particular, the VC1–VC3 voltages affect the display quality.
- Do not connect anything to the VC1–VC3 terminals when the LCD driver is not used.

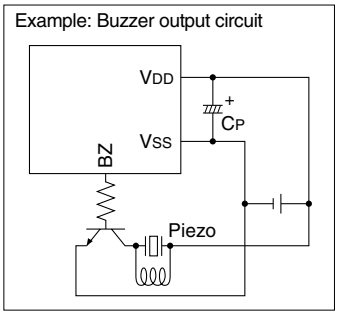
Arrangement of signal lines

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



Output terminals

- When an output terminal is used to drive an external component that consumes a large amount of current, the operation of the external component affects the built-in power supply circuit of this IC and the output voltage may vary. When driving a bipolar transistor by a periodic signal such as the BZ or timer output in particular, it may cause variations in the voltage output from the LCD system voltage circuit that affects the contrast of the LCD display. To prevent this, separate the traces on the printed circuit board. Put one between the power supply and the IC's VDD and VSS terminals, and another between the power supply and the external component that consumes the large amount of current. Furthermore, use an external component with as low a current consumption as possible.



Precautions for Visible Radiation (when bare chip is mounted)

- Visible radiation causes semiconductor devices to change electrical characteristics. It may cause the IC to malfunction. When developing products, consider the following precautions to prevent malfunctions caused by visible radiation.
  (1) Design the product and bond the IC on the board so that it is shielded from visible radiation in actual use.
  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
  (3) Shield not only the face of the IC but the back and side as well.
  (4) After the shielded package has been opened, the IC chip should be bonded on the board within one week. If the IC chip must be stored after the package has been opened, be sure to shield the IC from visible radiation.

Revision History

Code No.	Page	Contents
412158900	All	New establishment
412158901a	14-2	Segment allocation (Old) Note: Refer to "Generating S1C63003 Mask Data" in the Appendix when generating an application using the S1C63003. (New) Note: Refer to Appendix D, "Mask Data Creation Procedure," for mask data creation including segment allocation and precautions.
	AP-D-1 to 3	Appendix D Mask Data Creation Procedure Replaced all the contents.

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