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S1R77022F00B000
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

NOTICE

Table of Contents

1. OVERVIEW

This is an analog front-end (AFE) IC to allow high-speed reading operation. Also, this IC incorporates six 10-bit resolution A/D converters to easily develop a high-speed scanner system.

2. FEATURES

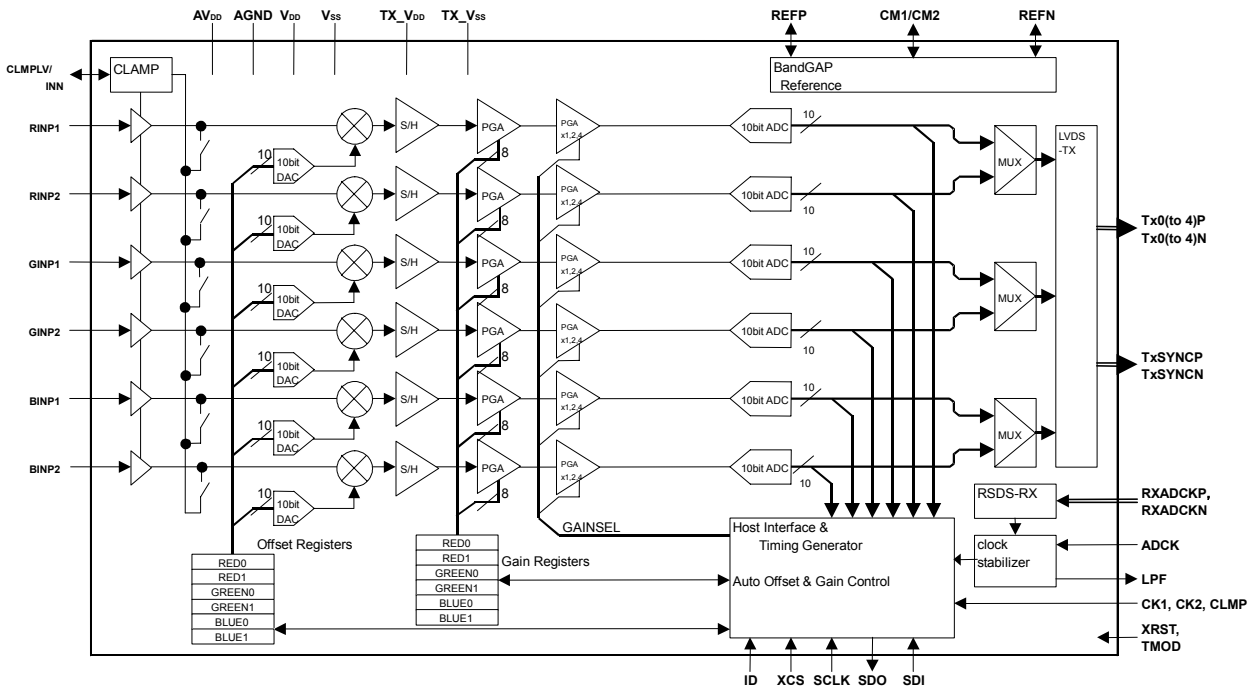
Common section
- -0.5 mm pitch, QFP80-pin package
- 3.3V single power supply
- Built-in input clock waveform shaper function

Host Interface Section
- Serial interface
- LVDS image data output (Transfer rate: 10-80 MHz)
- Selectable image output sequence during multiplexed image output
  From odd to even channel, or from even to odd channel
- Point sequential output mode (2 LVDS output channels for image data output)
  Transfer rate in 2-channel mode: 4 to 20 MHz
  Transfer rate in 6-channel mode: 2 to 13 MHz

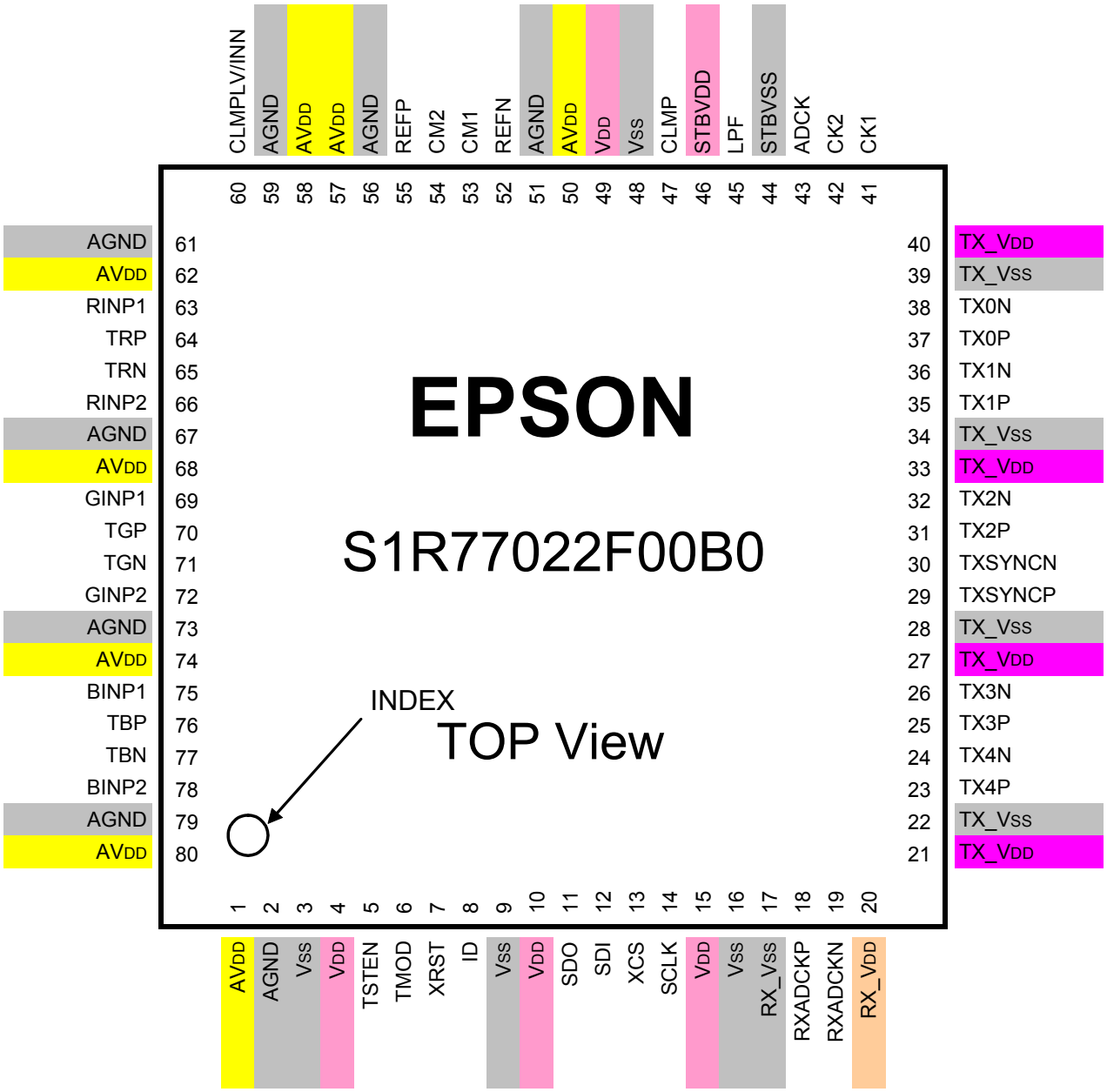
Analog Front End (AFE) Section
- Six built-in, 10-bit A/D converters
- Maximum conversion rate per channel (AFE transfer clocks): 40MHz
- Operation mode: CDS or S/H mode
- Number of operating channels: Selectable from 1, 2, 3, 4 and 6 channels
- Analog signal input range: 2.2 Vp-p
- Full-scale input range to A/D converter: 1.2 Vp-p
- Programmable gain amp (PGA) control range: The gain characteristics can be selected using registers
  From -6.9 dB (0.45 times) to +12.0 dB (4.0 times) (in 128-bit resolution steps)
  From -0.9 dB (0.9 times) to +18.0 dB (8.0 times) (in 128-bit resolution steps)
  From +5.1 dB (1.8 times) to +24.1 dB (16.0 times) (in 128-bit resolution steps)
- Offset control range: ±300 mV (in 1024-bit resolution steps)
- Built-in automatic offset and gain control functions
- Built-in pixel level monitor function during automatic offset and gain control
- Built-in automatic black level compensation function
- Built-in automatic sampling signal generation function (in S/H mode only)
- Built-in, two-pixel averaging function (when odd and even channels are simultaneously used)

* Radiation shield not included.

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



PRECAUTIONS

It is recommended separate the power line systems from each other. When the separation like above is not available due to the limited space on the actual board, it is strongly advised to separate at least AVDD-AGND system from other power line systems. In this case, however, please note that the best characteristics may not be available.

5. PIN DESCRIPTION

No.	Pin	Pin Name	I/O	Reset	Pin Functions	Remarks	Drive Capacity
Analog signal pins							
1	55	REFP	A	—	High potential reference		Analog
2	53	CM1	A	—	In-phase mode voltage 1		Analog
3	54	CM2	A	—	In-phase mode voltage 2		Analog
4	52	REFN	A	—	Low potential reference		Analog
5	63	RINP1	A	—	R-channel analog input (ODD)		Analog
6	66	RINP2	A	—	R-channel analog input (EVEN)		Analog
7	69	GINP1	A	—	G-channel analog input (ODD)		Analog
8	72	GINP2	A	—	G-channel analog input (EVEN)		Analog
9	75	BINP1	A	—	B-channel analog input (ODD)		Analog
10	78	BINP2	A	—	B-channel analog input (EVEN)		Analog
11	60	CLMPLV/INN	A	—	Clamp level monitor/reference level input		Analog
12	64	TRP	A	—	R-channel A/D converter high-potential input (for test)		Analog
13	65	TRN	A	—	R-channel A/D converter low-potential input (for test)		Analog
14	70	TGP	A	—	G-channel A/D converter high-potential input (for test)		Analog
15	71	TGN	A	—	G-channel A/D converter low-potential input (for test)		Analog
16	76	TBP	A	—	B-channel A/D converter high-potential input (for test)		Analog
17	77	TBN	A	—	B-channel A/D converter low-potential input (for test)		Analog
18	1	AV_{DD}	P	—	+3.3V analog power supply		—
19	50	AV_{DD}	P	—			
20	57	AV_{DD}	P	—			
21	58	AV_{DD}	P	—			
22	62	AV_{DD}	P	—			
23	68	AV_{DD}	P	—			
24	74	AV_{DD}	P	—			
25	80	AV_{DD}	P	—			
26	2	AGND	P	—	Analog ground		—
27	51	AGND	P	—			
28	56	AGND	P	—			
29	59	AGND	P	—			
30	61	AGND	P	—			
31	67	AGND	P	—			
32	73	AGND	P	—			
33	79	AGND	P	—			
Control signals							
34	7	XRST	I	—	Reset signal	SMT, PD	—
35	43	ADCK	I5	—	A/D conversion clock		—
36	18	RXADCKP	A	—	A/D conversion clock (RSDS input)		Analog
37	19	RXADCKN	A	—	A/D conversion clock (RSDS input)		Analog
38	41	CK1	I5	—	Sampling clock 1	PD	—
39	42	CK2	I5	—	Sampling clock 2	PD	—
40	47	CLMP	I5	—	Clamp timing	PD	—
41	45	LPF	A	—	Input clock waveform shaping filter connection pin		Analog

Symbols in I/O columns
A: Analog signal pin
I: Input pin
I5: Input pin (5V tolerant input)
O: Output pin
B: Bi-directional pin
P: Power supply pin

Symbols in Reset (in the initial state) columns
HI-Z: High-impedance state

Symbols in Remarks columns
PU: Pulled up
PD: Pulled down
SMT: Schmidt input

No.	Pin	Pin Name	I/O	Reset	Pin Functions	Remarks	Drive Capacity
Serial interface							
42	8	ID	I	—	Chip ID selection	PD	—
43	6	TMOD	I	—	Serial interface access cycle selection	PD	—
44	13	XCS	I5	—	Chip select	SMT	—
45	14	SCLK	I5	—	Serial data I/O synchronous clock	SMT, PD	—
46	12	SDI	I5	—	Serial data input	SMT, PD	—
47	11	SDO	O	Hi-Z	Serial data output		2mA
Image data output (LVDS)							
48	37	TX0P	A	—	Image data output		Analog
49	38	TX0N	A	—			
50	35	TX1P	A	—			
51	36	TX1N	A	—			
52	31	TX2P	A	—			
53	32	TX2N	A	—			
54	25	TX3P	A	—			
55	26	TX3N	A	—			
56	23	TX4P	A	—			
57	24	TX4N	A	—			
58	29	TXSYNCP	A	—			
59	30	TXSYNCN	A	—			
Test pin							
60	5	TSTEN	I	—	Test pin	PD	—
Power supply pins							
61	4	V_{DD}	P	—	3.3V logic power supply pin		—
62	10	V_{DD}	P	—			
63	15	V_{DD}	P	—			
64	49	V_{DD}	P	—			
65	21	TX_V_{DD}	P	—	LVDS-TX power supply pin (3.3V)		—
66	27	TX_V_{DD}	P	—			
67	33	TX_V_{DD}	P	—			
68	40	TX_V_{DD}	P	—			
69	20	RX_V_{DD}	P	—	RSDS-RX power supply pin (3.3V)		—
70	46	STBV$_{DD}$	P	—	Waveform shaper function power supply pin (3.3V)		—
71	3	V_{SS}	P	—	Logic ground		—
72	9	V_{SS}	P	—			
73	16	V_{SS}	P	—			
74	48	V_{SS}	P	—			
75	22	TX_V_{SS}	P	—	LVDS-TX ground		—
76	28	TX_V_{SS}	P	—			
77	34	TX_V_{SS}	P	—			
78	39	TX_V_{SS}	P	—			
79	17	RX_V_{SS}	P	—	RSDS-RX ground		—
80	44	STBV$_{SS}$	P	—	Waveform shaper function ground		—

Symbols in I/O columns
A: Analog signal pin
I: Input pin
I5: Input pin (5V tolerant input)
O: Output pin
B: Bi-directional pin
P: Power supply pins

Symbols in Reset (in the initial state) columns
HI-Z: High-impedance state

Symbols in Remarks columns
PU: Pulled up
PD: Pulled down
SMT: Schmidt input

6. FUNCTIONAL DESCRIPTION

The functions of each circuit block are explained below.

6.1 Host Interface Section

6.1.1 Serial interface

Four types of serial interface signals can be handled. They are: Chip Select (XCS) signal, Serial Data I/O Sync Clock (SCLK) signal, Serial Data Input (SDI) signal, and Serial Data Output (SDO) signal. When this IC is in the active state (when the XCS signal is Low), data is sent or received synchronously with the SCLK signal. The access occurs in 17 or 16 cycles depending on the presence or absence of Chip ID Select bit. Cycle count is set according to TMOD and ID signals as defined in Table 6.1.

Table 6.1 Setting of Access Cycles

Access cycle	TMOD signal	ID signal
17 cycles	LOW	Chip ID selection
16 cycles	HIGH	LOW

To access to the register, first write the identification (ID) bit that indicates the write or read access. When the ID bit is low, the write access occurs. When it is high, the read access occurs. After writing the ID bit, write the ID Select bit (in 17-cycle operation only) and the 5-bit register ID number. Then, write or read the data. During 17-cycle operation, an access to this IC is made valid only when the input level of Chip ID Select bit has the same logic as the ID signal (for Chip ID selection setting).

All of Chip ID Select bit, register ID number, and data are sent at the rising edge of clocks, and they are sent beginning with the MSB.

This IC has a built-in counter for serial-to-parallel (or parallel-to-serial) data conversion, and it is reset when the XCS signal goes high. Therefore, the XCS signal must be negated (that is, the XCS signal must go high) at the end of each access cycle for register writing or reading.

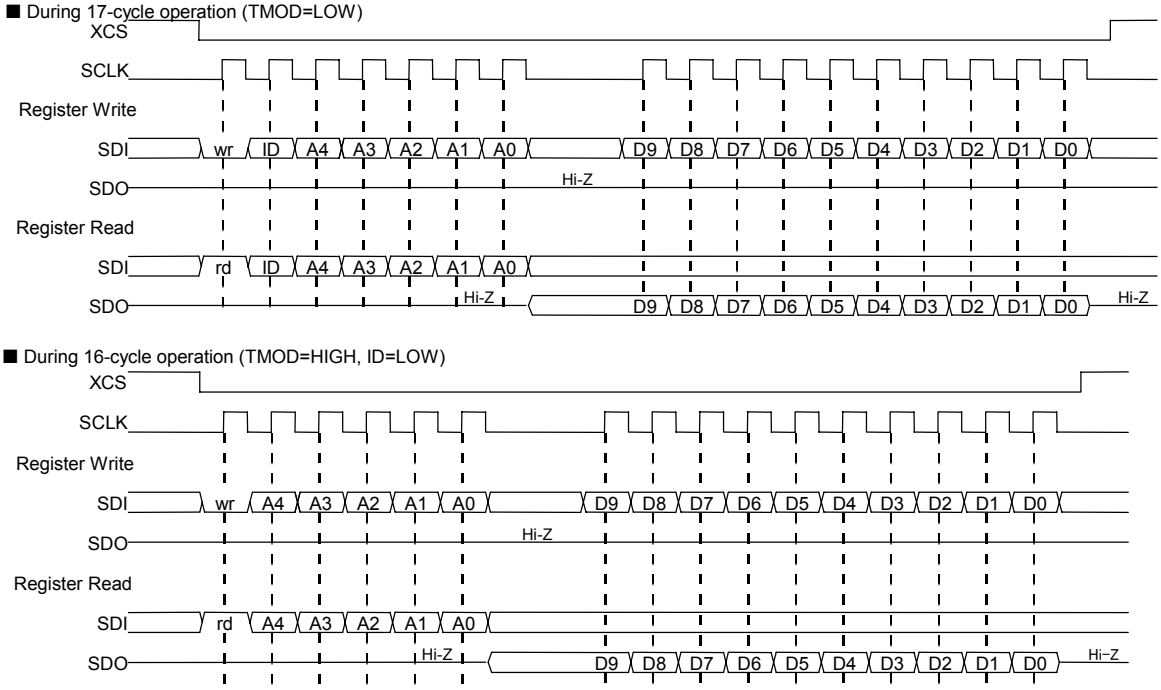


Fig.6.1 Serial Inter Access Timing

PRECAUTIONS

Note that a writing error can result if the pulse number of SCLK signal is excessive or deficient in an access cycle operation for writing to the register.

If the pulse number of SCLK signal was less than the followings, you can cancel writing to the register by setting XSC signal to high.

During 17-cycle operation: 15 pulses or less
During 16-cycle operation: 14 pulses or less

If the pulse number of SCLK signal was excessive, you can end the register write normally by setting, after writing to the register is completed, XSC signal to high while the pulse number is within the following range.

During 17-cycle operation: 18 - 25 pulses (+1 to +18 pulses)
During 16-cycle operation: 17 - 24 pulses (+1 to +18 pulses)

An writing error results if the above pulse number is exceeded (the error starts from 26th pulse (+9th pulse) in 17-cycle operation).

In the register read, on the other hand, excessive or deficient pulse number in SCLK signal does not affect the contents of the register.

6.1.2 Image data output

(1) Output sequence

An image data is output in synchronous with an externally entered A/D Conversion Clock (ADCK) signal. 10-bit image data is output at a time for each channel. If the MUXMD bit of DATACTL register (No. 0x03) is set to 1, the odd and even analog input signals are multiplexed and output as the analog-to-digitally converted image data. However, if the MUXMD bit is set to 0, either the odd or even analog input signal is converted from analog into digital form and output as the image data. Also, if the XOER, XOEG and XOEB bits of DATACTL register (No. 0x03) are set to 1, the corresponding channel outputs become null codes (0x000).

During multiplexed signal output, its sequence can be set by the MUXSQ bit of DATACTL register (No. 0x03). If the MUXSQ bit is set to 0, the odd-to-even signal output sequence is set. If it is set to 1, the even-to-odd signal output sequence is set.

(2) Two-pixel averaging function

If the AVEMD bit of DATACTL register (No. 0x03) is set to 1, the analog-to-digitally converted odd and even signal image data can be averaged in each color and output.

Table 6.2 shows the relationship between respective register settings and the resulting image data outputs and Fig.6.2 illustrates the operation examples. And Fig.6.3 shows an operation timing chart when the two-pixel averaging function is active.

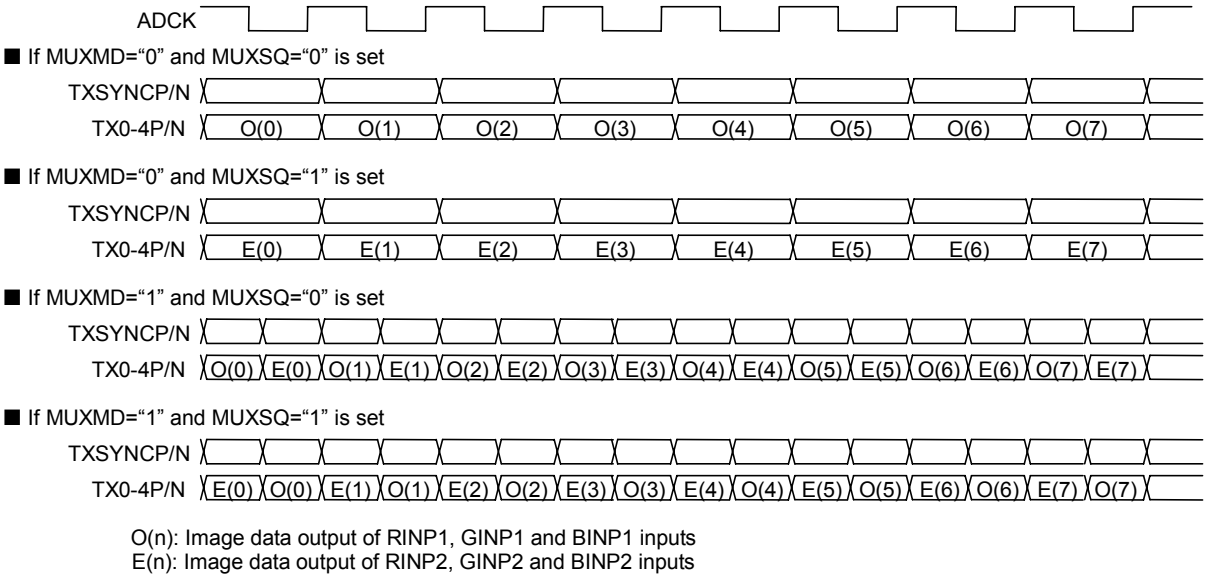
Table 6.2 Image Data Output

Register setting						Input	Image data output		
XOEB	**XOEG**	**XOER**	**MUXSQ**	**AVEMD**	**MUXMD**	**ADCK**	**B-channel**	**G-channel**	**R-channel**
“1”	“1”	“1”	X	X	X	X	null	null	null
“0”	“0”	“1”	“0”	“0”	“0”	X	BINP1	GINP1	null
“0”	“1”	“0”	“0”	“0”	“0”	X	BINP1	null	RINP1
“1”	“0”	“0”	“0”	“0”	“0”	X	null	GINP1	RINP1
“0”	“0”	“0”	“0”	“0”	“0”	X	BINP1	GINP1	RINP1
“0”	“0”	“0”	X	“1”	“0”	X	$\frac{BINP1+BINP2}{2}$	$\frac{GINP1+GINP2}{2}$	$\frac{RINP1+RINP2}{2}$
“0”	“0”	“0”	“1”	“0”	“0”	X	BINP2	GINP2	RINP2
“0”	“0”	“0”	“0”	“0”	“1”	HIGH	BINP1	GINP1	RINP1
						LOW	BINP2	GINP2	RINP2
“0”	“0”	“0”	“1”	“0”	“1”	HIGH	BINP2	GINP2	RINP2
						LOW	BINP1	GINP1	RINP1

0: Set the register to 0. L: LOW-level input
1: Set the register to 1. H: HIGH-level input
X: Don’t care.

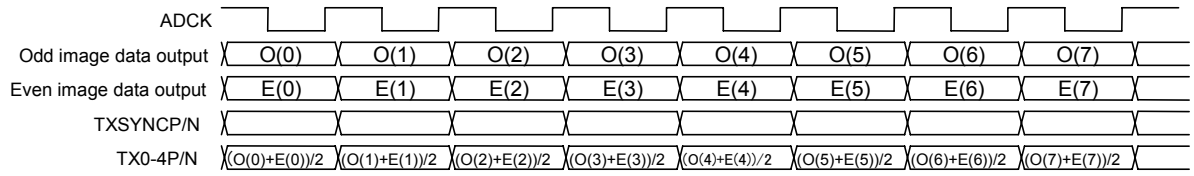
Restriction

Before changing the MUXMD and AVEMD bit state, be sure to set the PDLVDS and PDSTB bits of POWERDOWN register (No. 0x00) to 1.



O(n): Image data output of RINP1, GINP1 and BINP1 inputs
E(n): Image data output of RINP2, GINP2 and BINP2 inputs

Fig.6.2 Image Data Output Operation Example



O(n): Image data of RINP1, GINP1 and BINP1 inputs
E(n): Image data of RINP2, GINP2 and BINP2 inputs

Fig.6.3 Operating Timing of Two-Pixel Averaging Function

(3) Line Monitor function

This function counts the number of pixels of an image data and monitors the attributes of image data in each pixel position. These attributes are as follows. The image data and their attributes are output with together.

wh: White-based pixels (or effective pixel data)
dm: Black dummy pixels
ob: Black-based pixels (OB pixels)

The Line Monitor function is made valid only when an appropriate number of pixels is set in each of BKWHST register (No.0x04), BKNUM register (No.0x05) and WHNUM registers (No.0x06 to 0x07) and when the INSTGO bit of DATACTL register (No.0x03) is set to "1". An external signal input is required for line monitoring. For details, see Paragraph 6.5.11 "Automatic Offset and Gain Control Functions."

6.1.3 Test mode

The image data output test mode is selected if the TSTMD [1:0] bit of DATACTL register (No.0x03) is set. The fixed value or increment data can be output and tested. Output of increment data becomes available by setting an appropriate number of pixels on each of BKWHST register (No. 0x04), BKNUM register (No. 0x05) and WHNUM registers (No. 0x06 and 0x07), and also setting 1 for the INSTGO bit of DATACTL register (No. 0x03). Two types of increment data can be output, and either of them is selected by using or not using the color channel ID code. The following gives an example of R-channel multiplexed signal output with no use of color channel ID code.

Rodd	**R**even	**R**odd	**R**even	···	**R**odd	**R**even	**R**odd	**R**even	**R**odd	···
0xXXX	0xXXX	0x002	0x003	···	0x0FE	0x0FF	0x000	0x001	0x002	…

Table 6.3 defines its data format.

Table 6.3 Data Format during Increment Data Output

■ If TSTMD [1:0]= “10” is set

9	8	7	6	5	4	3	2	1	0
CNT[8:0]									ch

CNT[8:0] Pixel counter
ch: ODD or EVEN channel ID
0: ODD-numbered (xINP1) channel
1: EVEN-numbered (xINP2) channel

■ If TSTMD [1:0]= “01” is set

9	8	7	6	5	4	3	2	1	0
CL[1:0]		CNT[6:0]							ch

CL[1:0] Color channel ID
00: R-channel
01: G-channel
10: B-channel
CNT[8:0] Pixel counter
ch: ODD or even channel ID
0: ODD-numbered (xINP1) channel
1: EVEN-numbered (xINP2) channel

If the TSTMD [1:0] bits are set to “11”, the fixed data is output. The fixed data is used as the offset register value of each channel. Table 6.4 shows its data format.

Table 6.4 Data Format during Fixed Data Output

■ If TSTMD [1:0]= “11” is set

9	8	7	6	5	4	3	2	1	0
OFS[9:0]									

PRECAUTIONS
An invalid pixel data is first output during increment data output.

6.2 LVDS Section

The image data is output by the LVDS (low-voltage differential signaling) circuits). The LVDS section has 5 channels for image data output and 1 channel for Sync clock output.Fig.6.4 illustrates the LVDS peripheral connections.

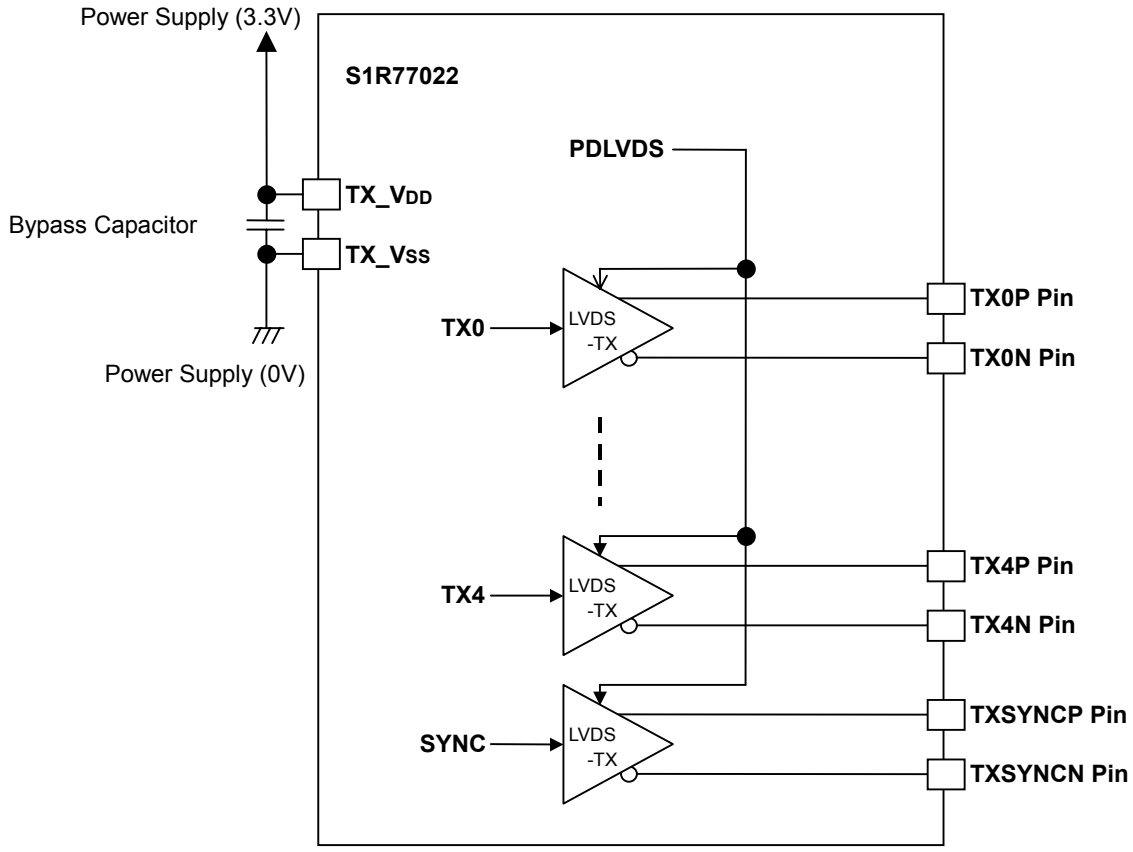


Fig.6.4 LVDS Peripheral Connections

(1) Power-Down function

The LVDS section provides the Power-down function that is controlled by the PDLVDS bit of POWERDOWN register (No.0x00). If the PDLVDS bit is set to "1", the LVDS section enters in the Power-down mode and it stops image data transmission. If the PDLVDS bit is set to "0", the Power-Down mode is released and the LVDS section restarts image data transmission. After release of the Power-Down mode, however, up to 10 milliseconds are required for the LVDS section to start the stable image data transmission.

Restriction

Before changing the state of VCOSEL [1:0] bits of AFECTL register (No. 0x0B) and MUXMD, AVEMD and PIXSQMD bits of DATACTL register (No. 0x03), be sure to set the PDLVDS and PDSTB bits of POWERDOWN register (No. 0x00) to 1.

(2) Termination resistor

The LVDS output must be terminated with 100Ω at a position close to an input pin of the receiving device.

Restriction

We recommend to use an external resistor having the ±1.0% or less tolerance. Also, this IC and connectors must be mounted on the same side (component side) of the board without passing the leads through holes.

(3) Image data output format

Fig.6.5 shows the format of image data to be output by the LVDS circuit. Each empty bit of image data is assigned with a code that indicates its internal operation state. Meaning of each bit showin in Fig.6.5 is follows.

R9 to 0: R-channel image data output
G9 to 0: G-channel image data output
B9 to 0: B-channel image data output
wh: White-based pixels (or effective pixel data)
dm: Black dummy pixels
ob: Black-based pixels (OB pixels)
ck2: CK2 pin monitor
clmp: CLMP pin monitor

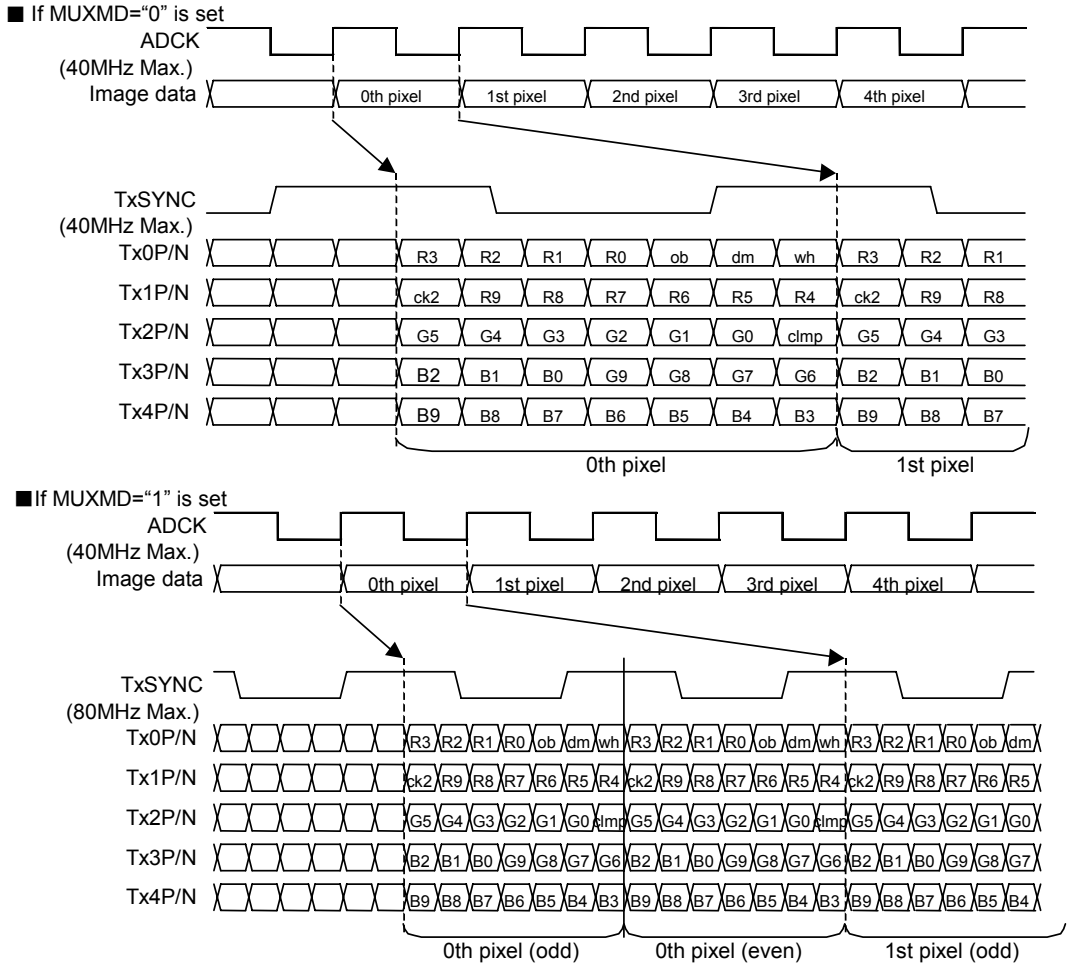


Fig.6.5 LVDS Image Data Output

Restriction

Frequency range of ADCK signal in the normal output mode is as shown below.

■ If MUXMD=0

10 MHz ≤ ADCK signal frequency ≤ 40 MHz

■ If MUXMD=1

5 MHz ≤ ADCK signal frequency ≤ 40 MHz

The point sequential output mode is selected if the PIXSQMD bit of DATACTL register (No. 0x03) is set to 1. In the point sequential output mode, two pairs of image data sets can be output simultaneously by the LVDS circuit.

Fig.6.6 shows an example of the capture operation.

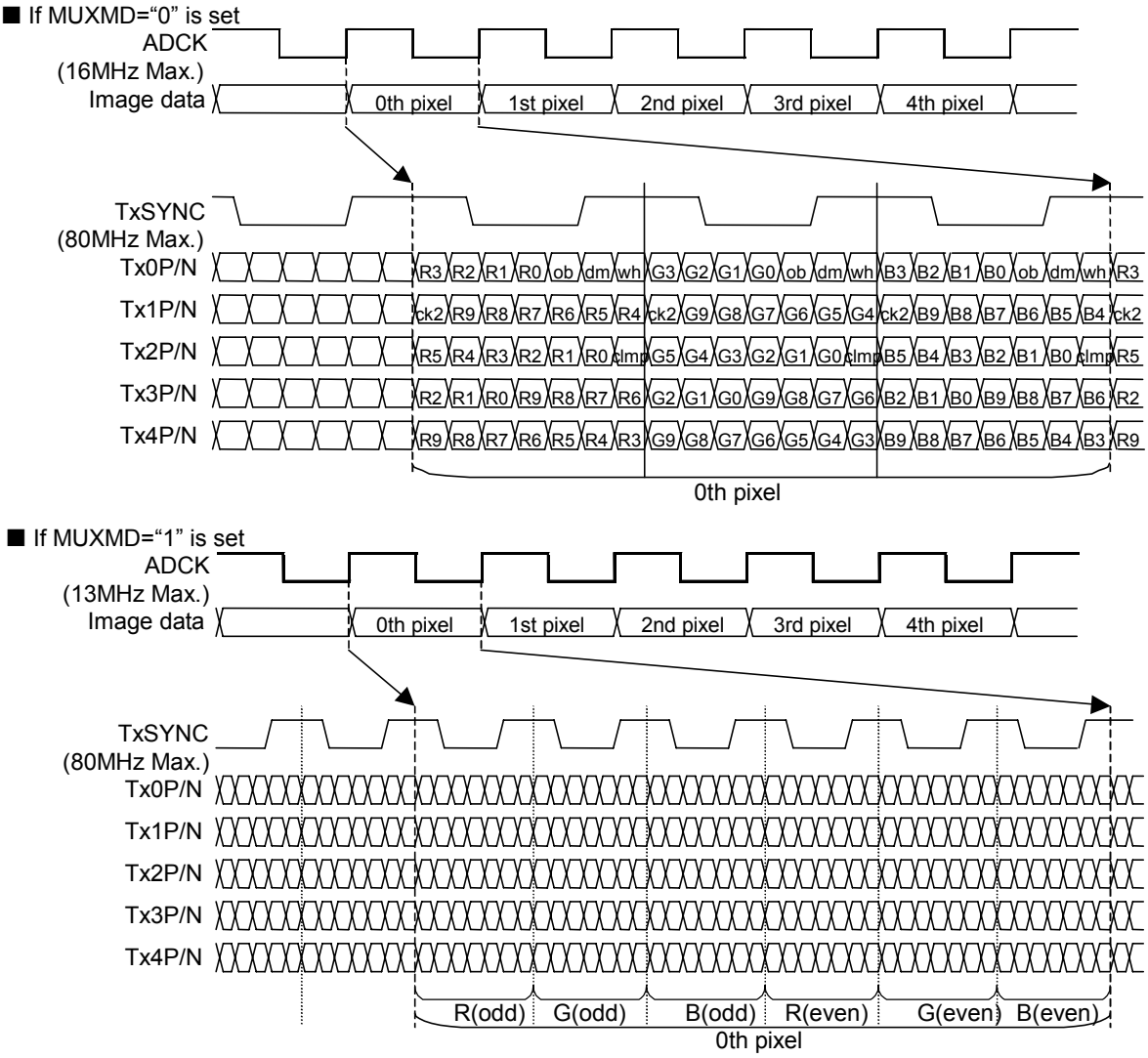


Fig.6.6 LVDS Image Data Output in Point Sequential Output Mode

Restriction 1

The point sequential output mode can be used only if the ADCK signal has the following frequency only.

- If MUXMD=0
  3.33 MHz ≤ ADCK signal frequency ≤ 16.6 MHz
- If MUXMD=1
  1.66 MHz ≤ ADCK signal frequency ≤ 13.3 MHz

Restriction 2

Before changing the PIXSQMD bit state, be sure to set the PDLVDS and PDSTB bits of POWERDOWN register (No. 0x00) to 1.

(4) Pre-emphasis function

The pre-emphasis function allows stable data transmission by flowing the large switching current of internal circuits if data transmission is unstable due to the high LVDS transmission frequency or others. If the PE bit of LVDSCTL register (No. 0x16) is set to 1, the pre-emphasis function flows the large switching current. Usually, the PE bit must be set to 0.

(5) Channel output enabling function

It is possible to enable or disagle the LVDS output on a channel basis. Use the TX0EN - TX4EN bits of LVDSCTL register (No. 0x16) for the setting. When the output is disabled, zero it out.

(6) Test code output function

Use the Test Code Output function for the LVDS transmission test. If the LVDSDT bit of LVDSCTL register (No. 0x16) is set to 1, each channel data is output in the format defined.Table6.5.

Table 6.5 Format of Data output by Test Code Output Function

Output channel	6	5	4	3	2	1	0
Tx0P/N	RD1OFS[6:0]						
Tx1P/N	RD2OFS[6:0]						
Tx2P/N	GR1OFS[6:0]						
Tx3P/N	GR2OFS[6:0]						
Tx4P/N	BL1OFS[6:0]						

6.3 RSDS Section

An ADCK signal can be entered via the RSDS (Reduced Swing Differential Signaling) circuit. Fig.6.7 illustrates the RSDS peripheral connections.

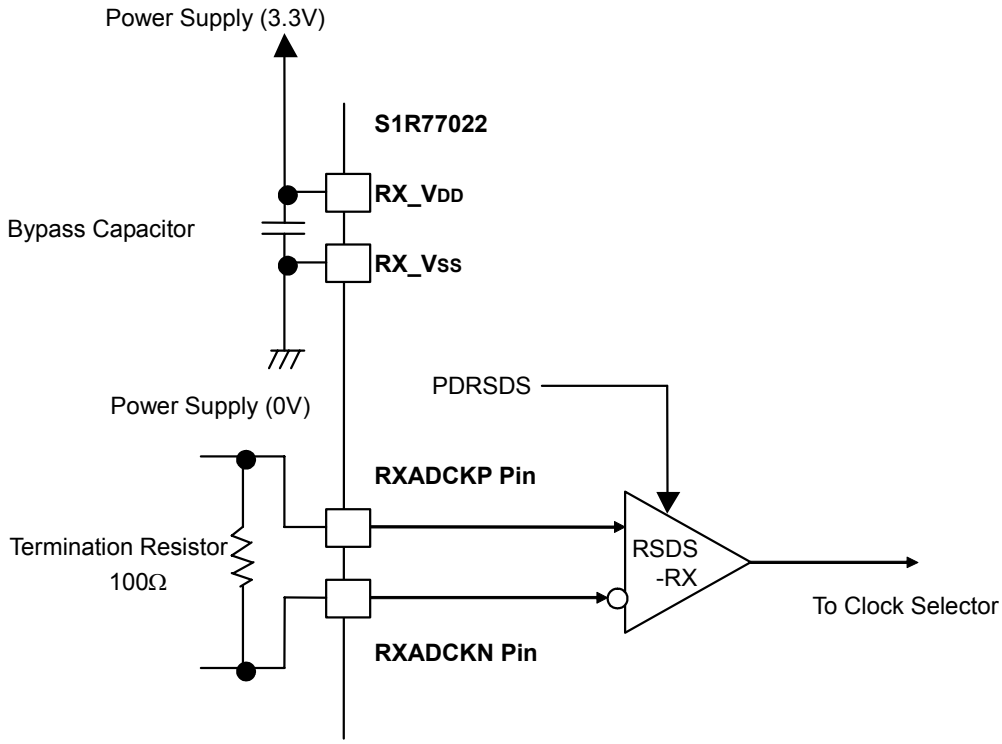


Fig.6.7 RSDS Connection Diagram

(1) Power-Down Function

The RSDS section provides the Power-Down function that is controlled by the PDRSDS bit of POWERDOWN register (No. 0x00). If the PDRSDS bit is set to 1, the RSDS section enters in the Power-Down mode and it stops ADCK signal input. If the PDRSDS bit is set to 0, the Power-Down mode is released and the RSDS section restarts ADCK signal input. After release of the Power-Down mode, however, up to 10 milliseconds are required for the RSDS section to start its stable operation.

(2) Termination resistor

Connect a 100Ω termination resistor to a point close to the RSDS input pin.

Restriction

We recommend to use an external resistor having the ±1.0% or less tolerance. Also, this IC and connectors must be mounted on the same side (component side) of the board without passing the leads through holes.

(3) Processing of empty pins

If ADCK signal is NOT entered via the RSDS circuit, the RXCLKP signal must be fixed to low and the RXCLKN signal must be fixed to high.

6.4 Input Clock Waveform Shaper Function Section

This IC has the Input Clock Waveform Shaper function to shape the ADCK signal waveforms (with 50% duty). Fig.6.8 illustrates the peripheral connections of the Input Clock Waveform Shaper function.

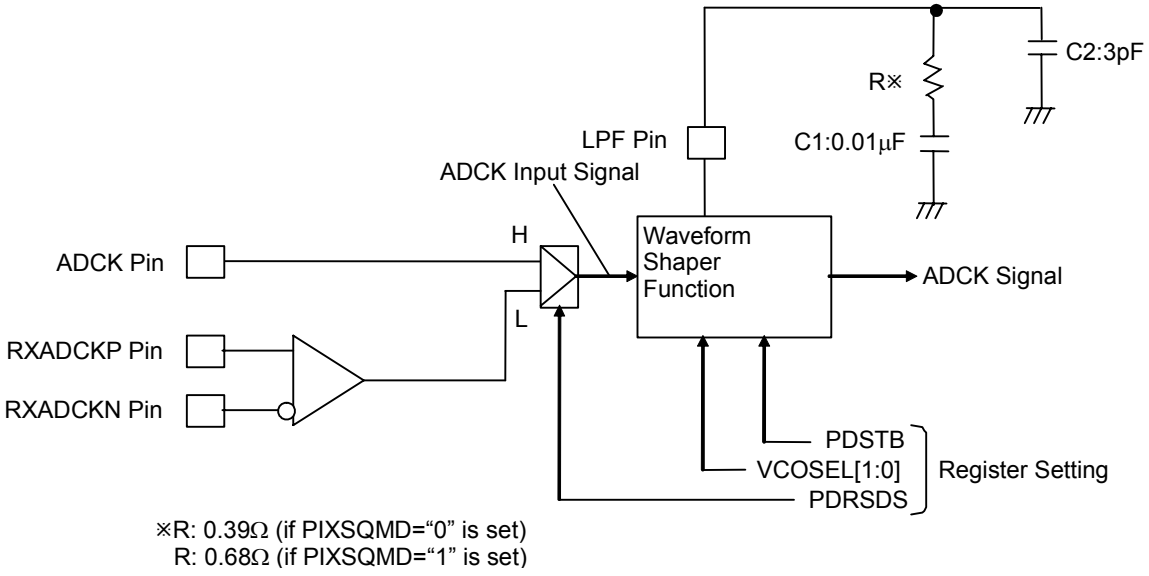


Fig.6.8 Input Clock Waveform Shaper Function

Restriction

To operate this IC in the stable state, keep the Input Clock Waveform Shaper function active (in the operating state).

(1) Power-Down Function

The power-down function of the Input Clock Waveform Shaper function can be controlled by the PDSTB bit of POWERDOWN register (No. 0x00). If the PDSTB bit is set to 1, the Input Clock Waveform Shaper function enters the Power-Down mode and the function stops. If it is set to 0, the Power-Down mode is released and the analog section returns to the normal operation. After release of the Power-Down mode, however, up to 10 milliseconds are required to start the stable function operation.

(2) ADCK Signal Input Method Selection

As defined in Table.6.6, an input of ADCK signal from an external pin can be selected as either the clock pulse input or RSDS input.

Table 6.6 Selection of ADCK Signal Input

Input method	Register setting	Pin processing		
	PDRSDS	CLKIN	RXCLKP	RXCLKN
Clock pulse input	"1"	Clock input	LOW	HIGH
RSDS input	"0"	LOW	Clock input	

0: Set the register to "0". L: LOW-level input
1: Set the register to "1". H: HIGH-level input

(3) ADCK Signal Input Frequency Setting

The VCOSEL [1:0] bits of AFECTL register (No. 0x0B) must be set according to the ADCK signal frequency as defined in Table 6.7

Table 6.7 Setting of VCOSEL [1:0] Bits

ADCK signal frequency		Setting of VCOSEL [1:0] bits
PIXSQMD="0"	PIXSQMD="1"	
25.0 to 40.0MHz	8.3 to 13.3MHz	"11"
20.0 to 25.0MHz	6.6 to 8.3MHz	"10"
12.5 to 20.0MHz	4.1 to 6.6MHz	"01"
10.0 to 12.5MHz	3.3 to 4.1MHz	"00"

Restriction

Before changing the state of VCOSEL [1:0] bits of AFECTL register (No. 0x0B) and MUXMD, AVEMD and PIXSQMD bits of DATACTL register (No. 0x03), be sure to set the PDLVDS and PDSTB bits of POWERDOWN register (No. 0x00) to 1.

(4) External Parts

To allow stable operation of Input Clock Waveform Shaper function, an external resistor and an external capacitor must be connected to the LPF pin. Connect the external resistor and capacitor having the following constants to the LPF pin. Note that constant R varies depending on the setting of PIXSQMD bit of DATACTL register (No. 0x03).

R: 0.39Ω (if PIXSQMD=0)
0.68KΩ (if PIXSQMD=1)
C1:0.01μF
C2:3pF

6.5 Analog Section

6.5.1 Overview

The analog section is a functional block that converts an analog image data, output from the Charge Coupled Device (CCD), into digital data. This block is basically comprised of a Correlated Double Sampling (CDS) section, an offset control section, a Programmable Gain Amp (PGA), and a 10-bit A/D converter.

- Six built-in, 10-bit A/D converters
- Maximum conversion rate: 40 Msps per channel
- Operation mode: CDS mode or Sample/Hold (S/H) mode
- Number of operating channels: Selectable from 1, 2, 3, 4 or 6 channels
- Full-scale input range to A/D converter: 1.2 Vp-p
- Programmable Gain Amp (PGA) control range: The gain characteristics can be selected using registers as follows:
  From -6.9 dB (0.45 time) to +12.0 dB (4.0 times)
  From -0.9 dB (0.9 time) to +18.0 dB (8.0 times)
  From +5.1 dB (1.8 times) to +24.1 dB (16.0 times)
- Offset adjustable range: ±300 mV
- Built-in automatic offset and gain control functions
- Built-in automatic black level compensation function
- Built-in automatic sampling signal generation function (in S/H mode only)

6.5.2 Specification

Table 6.8 Specifications of Analog Section

Item		Specifications		
		Min.	Typ.	Max.
Internal reference voltage level				
Low potential reference (REFN)		1.10V	1.20V	1.30V
Common mode voltage (CM1)		1.40V	1.50V	1.60V
High potential reference (REFP)		1.70V	1.80V	1.90V
Conversion Characteristics				
Maximum conversion rate (per channel)				40Msps
Resolution			10bits	
Analog input				
External differential input range				2.6Vp-p
A/D converter input range				1.2Vp-p
input voltage		AGND		AV_{DD}
Effective range of analog input *1		0V		1.5V
Minimum gain control *2			-6.9 dB (0.45 times), -0.9 dB (0.9 times), +5.1 dB (1.8 times)	
Maximum gain control *2			+12.0 dB (4.0 times), +18.0 dB (8.0 times), +24.1 dB (16.0 times)	
Gain resolution			128 steps	
Gain error			±1dB	
Offset control range			±300mV	
Offset resolution			1024 steps	
Offset error			±20mV	
Clamp level		Register selection (16 steps)		
Dynamic characteristics of A/D converter (in 20MHz ADCK frequency)				
Integral non-linearity (INL)	30 [MHz] or less		±1.0	
	30 to 35 [MHz] or less		±1.1	
	35 to 40 [MHz]		±4.7	
Integral non-linearity (DNL)	30 [MHz] or less		±0.6	
	30 to 35 [MHz] or less		±0.9	
	35 to 40 [MHz]		+4.5/-1.0	
No missing code		Guarantee		
Power supply conditions				
Power supply voltage (AV_{DD})		+3.135V	+3.3V	+3.465V

* 1 A/D-convertible input range only in S/H mode (line clamp)
(Excluding ineffective analog components such as reset noises of CCD)

*2 Switched by register setting

*3 When 35 MHz or less

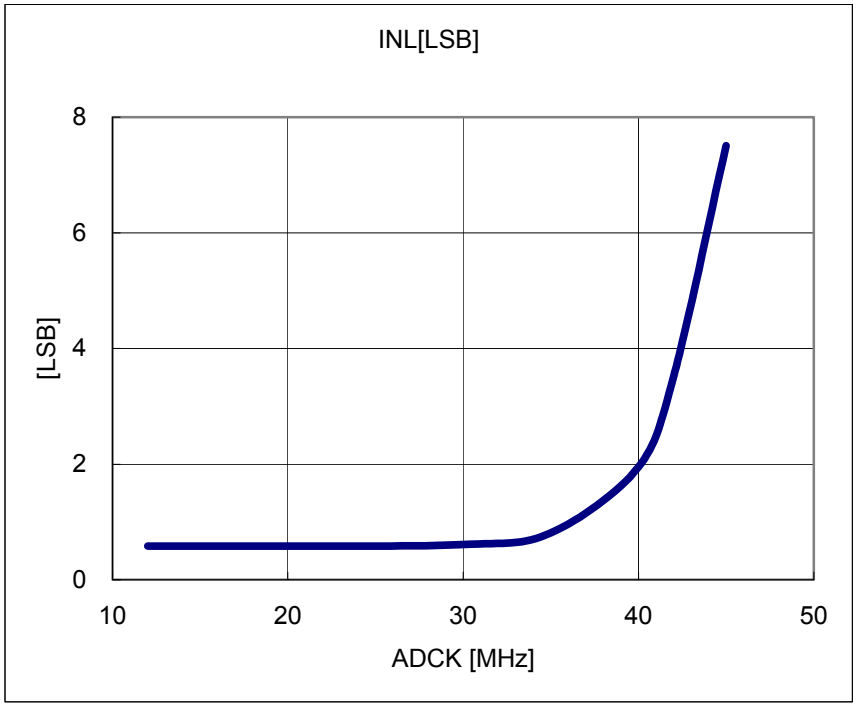


Fig.6.9 Integral nonlinearity (INL) of A/D converter

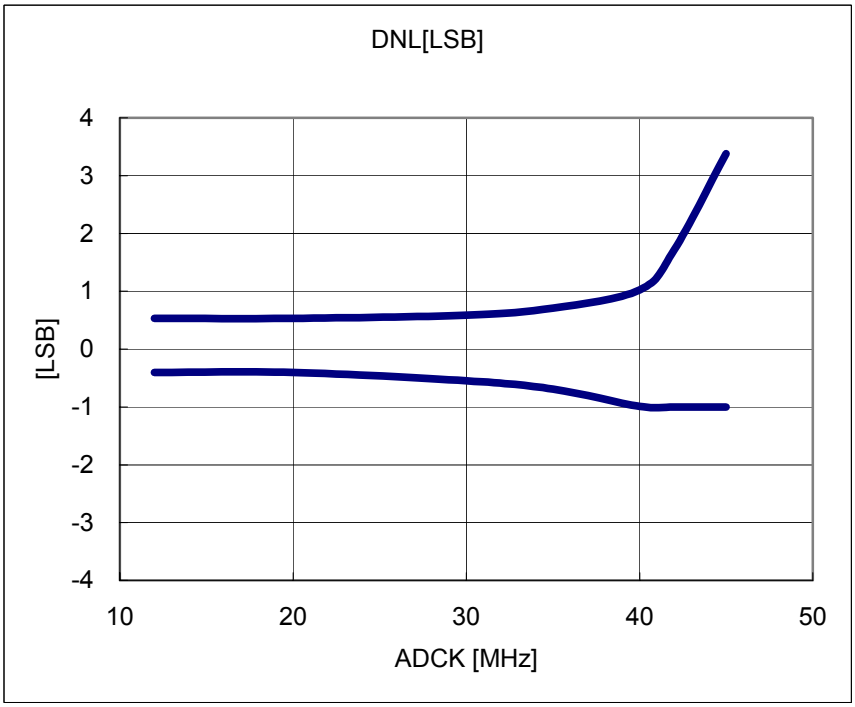


Fig.6.10 Differential nonlinearity (DNL) of A/D converter

6.5.3 Internal Block Configuration

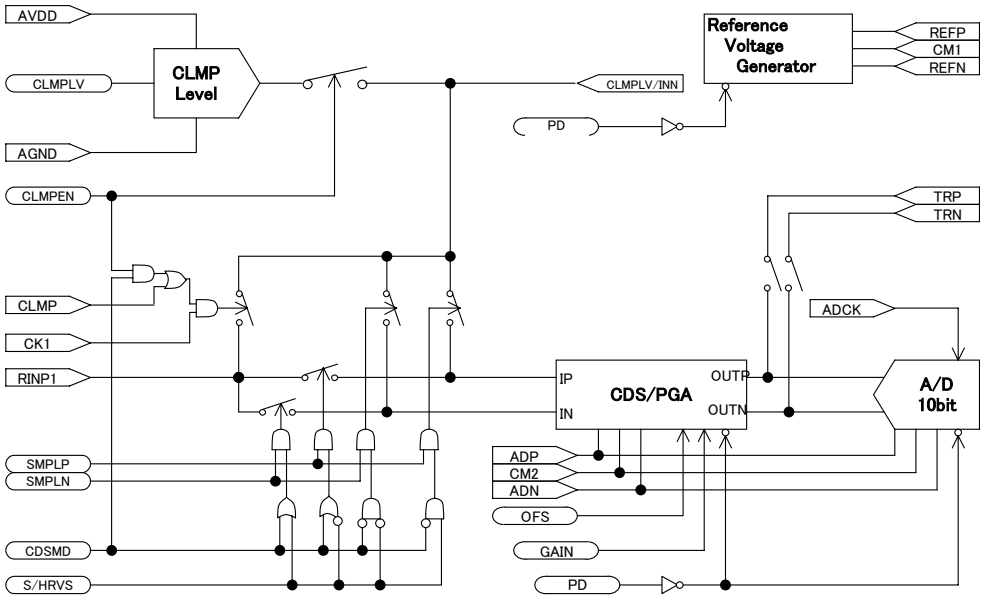


Fig.6.11 Analog Section Block Diagram (R-Channel [ODD])

Table 6.9 Pin Description of Analog Section pins

Pin name	Pin description	Connected to
External connection		
AV_{DD}	+3.3V analog power supply	External connection
AGND	Analog ground	External connection
REFN	Low potential reference 1 (1.2V)	External connection
ADN	Low potential reference 2 (1.2V)	External connection
CM1	Common mode voltage 1 (1.5V)	External connection
CM2	Common mode voltage 2 (1.5V)	External connection
REFP	High potential reference 1 (1.8V)	External connection
ADP	High potential reference 2 (1.8V)	External connection
RINP1	Analog input	External connection
CLMPLV/INN	Clamp level monitor/reference level input	External connection
TRP1	A/D Converter high-potential input (ODD)	External connection
TRN1	A/D Converter low-potential input (ODD)	External connection
ADCK	A/D conversion clock	External input
CK1	Clock signal 1	External input
CLMP	Clamp signal	External input
Internal connection		
PD	Power down	Register output
SMPLP	High-potential input level sampling signal	Internally generated (or generated from CK1 in specific operation mode)
SMPLN	Low-potential input level sampling signal	Internally generated (or generated from CK1 or CK2 in specific operation mode)
CDSMD	Sampling mode setting	Register output
S/HRVS	S/H mode differential voltage polarity setting	Register output
OFS	Offset setting	Register output
GAIN	Gain setting	Register output
CLMPEN	Clamp enable setting	Register output
CLMPLV	Clamp level setting	Register output

6.5.4 Power-Down Function

The Power-Down function of the analog section can be controlled by the PD bit of POWERDOWN register (No. 0x00). If the PD bit is set to 1, the Power-Down mode is selected. If it is set to 0, the Power-Down mode is released and the analog section returns to the normal operation. Note that the analog section of a non-operating channel is automatically set to the Power-Down mode.

6.5.5 Reference Voltage Generator

The analog section operates based on the reference voltage that has been generated by the reference voltage generator. The internal reference voltage can be monitored at the CM1 and REFN pins.

6.5.6 Clamping Circuit

To eliminate DC components from CCD analog output signals, the clamping circuit enters analog input signals using the AC coupling capacitor and clamps signals to the appropriate voltage using the internal bias circuit.

Signals can be clamped by “bit clamping” that operates for each pixel in the CLMP signal input timing (or clamp timing) or by “line clamping” that operates for the specified range of images. Signals are clamped when both the CLMP (clamp timing) signal and CK1 (sampling clock 1) signal go high. The logical polarity of CLMP signal can be inverted by the CLMPPOL bit of AFEMD register (No. 0x02).

The clamp level signal can be generated internally or can be entered from an external device. To enter it from an external device, set the CLMPEN bit of AFEMD register (No. 0x02) to 0 and enter the signal having the voltage within the limit range from the CLMPLV/INN pin. To internally generate the signal, set the CLMPEN bit to 1. The voltage of internally generated clamp level signal can be set by CLMPLV [3:0] bits of AFEMD register (No. 0x02) as described below. Also, its voltage level can be monitored at the CLMPLF/INN pin.

$$\text{Clamp voltage (V)} \fallingdotseq AV_{DD} \times \frac{\text{Register set value (0 to 15)}}{16}$$

6.5.7 CDS/PGA

This IC converts analog image data output from the CCD into digital data. The analog image data can be sampled either in the CDS mode or in the S/H mode. These modes can be switched by the CDSMD bit of AFEMD register (No. 0x02). Set the CDSMD bit to 1 to select the CDS mode, and set it to 0 to select the S/H mode.

Also, in the S/H mode alone, if the CKGEN bit of AFECTL register (No. 0x0B) is set to 1, a sampling signal is generated automatically even if the CK1 (sampling clock 1) signal is not entered from an external device. The sampling signal is created based on the externally entered ADCK signal and the sampling point is set at the negative going edge of the ADCK signal. It is possible to cut its puse duration short (delaying the rising edge by approximately 2 - 7 ns) by setting 1 for the CKGENMD bit of CKGENMD register (No. 0x0C).

(1) CDS mode function

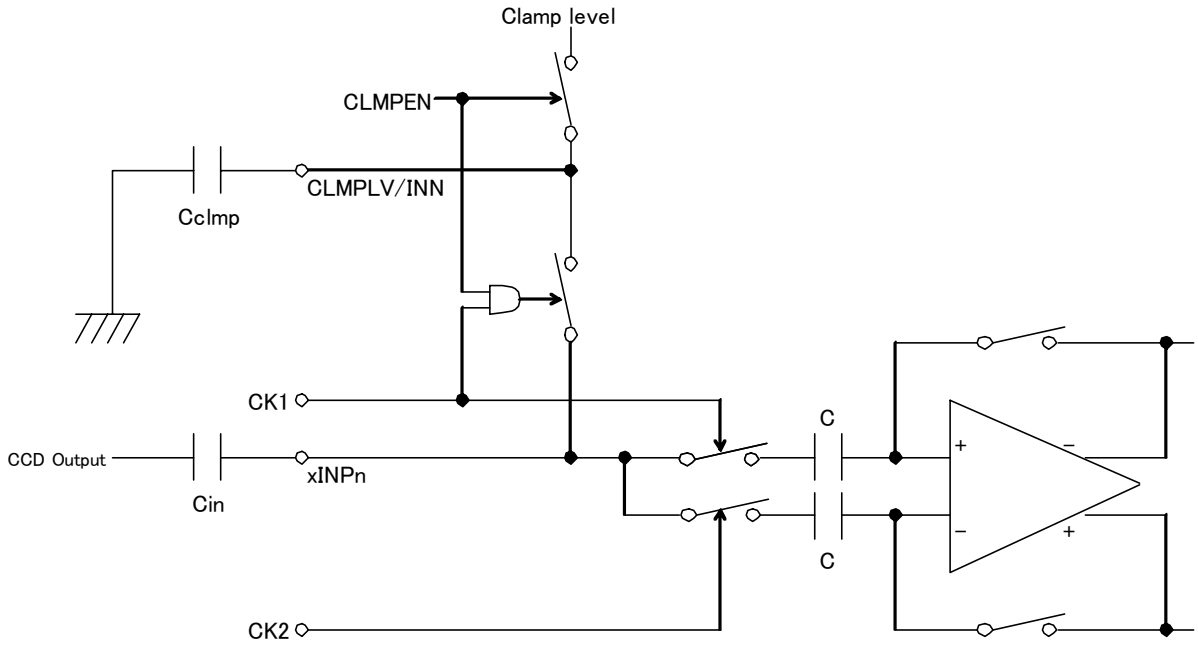


Fig.6.12 Internal Configuration Diagram in CDS Mode

Set the CDSMD bit of AFEMD register (No.0x02) to "1" to select the CDS mode. If the CLMPEN bit of AFEMD register (No.0x02) is set to "1", each bit of the corresponding pixel can be clamped.

In the CDS mode, the CCD output signals are sampled when the CK1 (sampling clock 1) signal is clamped and the CK2 (sampling clock 2) signal is HIGH. The logical polarity of CK1 and CK2 signals can be inverted by the CKPOL bit of AFEMD register (No.0x02).

Fig.6.12 shows the internal configuration in the CDS mode.

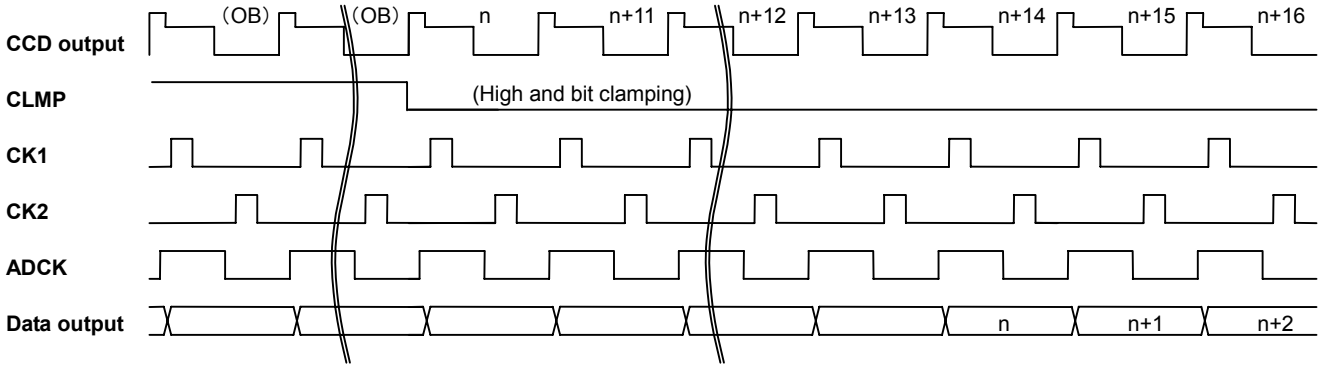


Fig.6.13 Operation Timing Example in CDS mode CDS

Fig.6.13 shows the operation timing example in the CDS mode. Also, the following gives the operation setting example.

AFEMD register (No.0x02):XX XX01 0001(2) Note) X can be any depending on the given reference voltage level.

(2) S/H mode function (Differential voltage input)

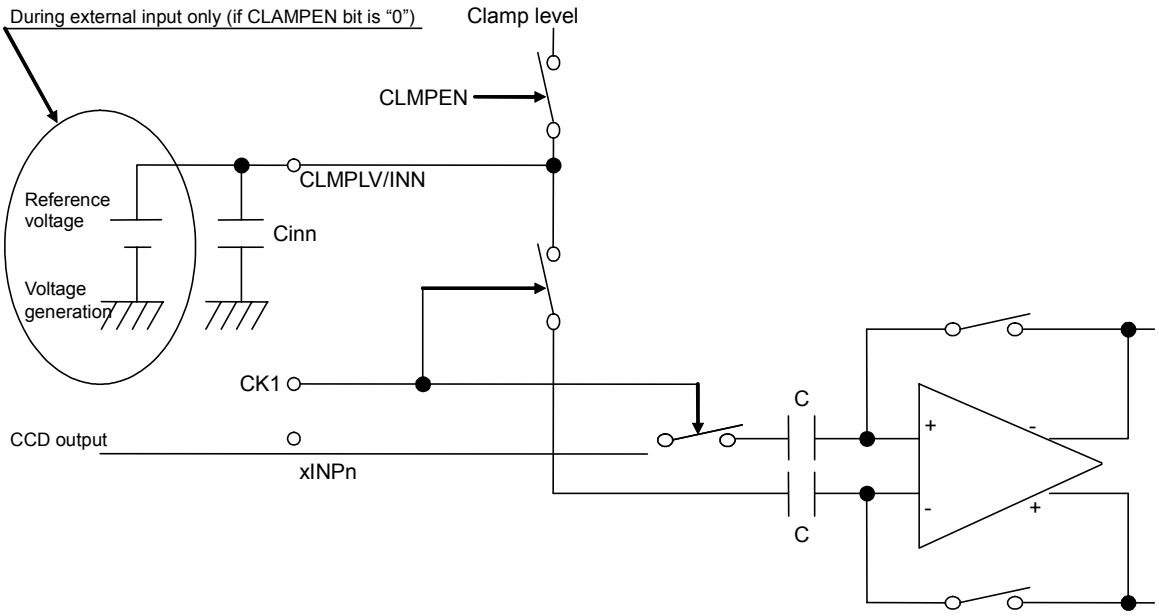


Fig.6.14 Internal Configuration in S/H Mode (Differential voltage input)

If the CDSMD bit of AFEMD register (No. 0x02) is set to 0, the S/H mode is selected. In the S/H mode, the reference voltage level signals can be entered in the CLMPLV/INN pin, and the differential voltage between the reference voltage level and the image data signal level can be entered. Both the reference voltage level signals and the CCD output level signals are sampled simultaneously when the CK1 (sampling clock) signal goes high. To enter the reference voltage level signals in the CLMPLV/INN pin, set the CLMPEN bit of AFEMD register (No. 0x02) to 0.

However, if the CLMPEN bit is set to 1, the bit clamp level signal can be generated internally at the reference voltage level. This voltage level can be monitored at the CLMPLV/INN pin. Do not apply an external voltage during voltage level monitoring.

Fig.6.14 shows the internal configuration in the S/H mode (differential voltage input).

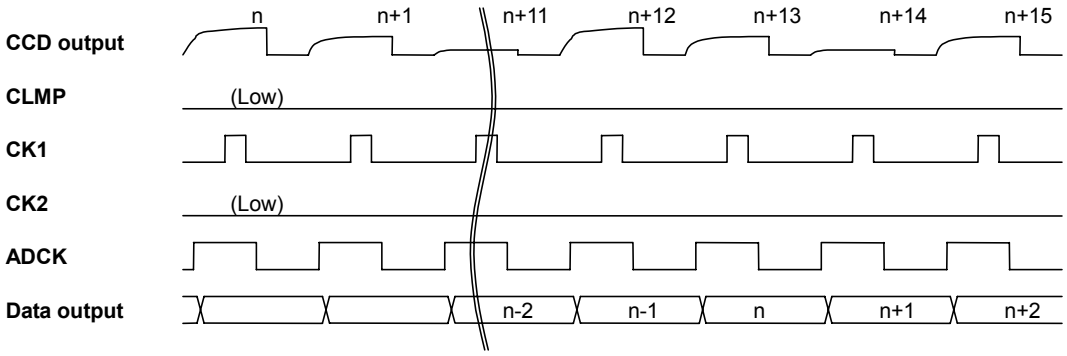


Fig.6.15 Example of S/H Mode (Differential Voltage Input) Operation Timing

Fig.6.15 gives an example of system operation timing when the S/H (differential voltage input) mode is selected and when the reference voltage is externally entered. Also, the following gives the operation setting example.

AFEMD register (No. 0x02): 00 0000 0000(2)

(3) S/H mode function (Line clamp)

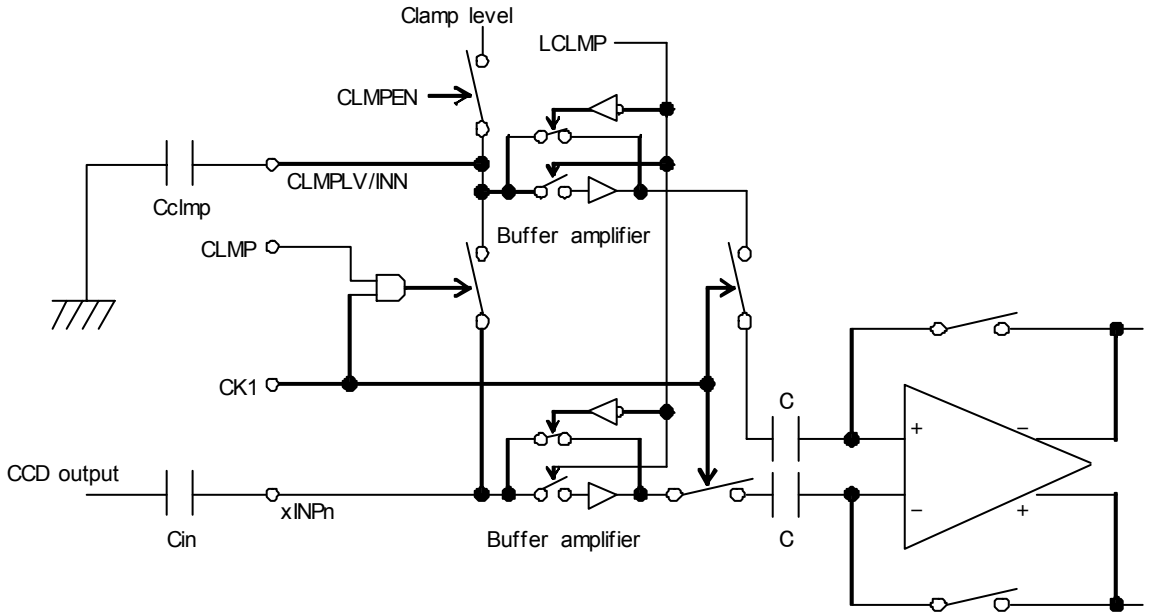


Fig.6.16 Internal Configuration in S/H Mode (Line clamp)

If both the S/HRVS bit and CLMPEN bit of AFEMD register (No. 0x02) are set to 1 in the S/H mode, the input polarity of reference voltage level and image data signal level is reversed and the line can be clamped. During line clamp, the CLMP signal goes high in the OB (Optical Black) pixel timing of the CCD output. When the effective pixel data is entered, the CLMP signal goes low and the differential voltage between the clamp level and the CCD output level is sampled. Both the clamp level signal and the CCD output level signal are sampled simultaneously when the CK1 (sampling clock) signal goes high. Setting the LCLMP bit of INCLT register (No. 0x0D) enables the buffer amplifier function and, thus, the analog input level (xINPn pin) being locked to the clamp level is stabilized. Setting of the buffer amplifier capacity is available with the BL bit [1:0] of ADCMD register (No. 0x0F).

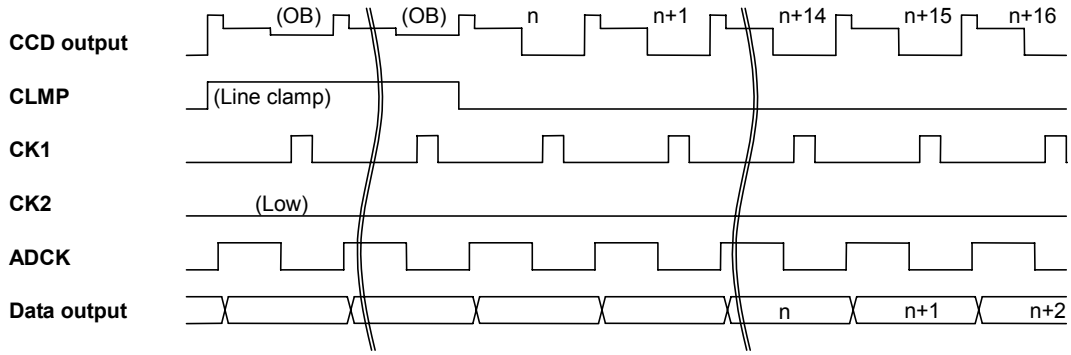


Fig.6.17 Example of S/H Mode (Line Clamp) Operation Timing

Fig.6.17 gives an example of system operation timing when the S/H (line clamp) mode is selected and when the reference voltage is externally entered. Also, the following gives the operation setting example.

AFEMD register (No.0x02):XX XX01 0010(2) Note) X can be any depending on the given reference voltage level.

6.5.8 A/D Converter

A high-speed, 10-bit A/D converter is used. It can convert a single pixel data from analog into digital form within a single ADCK signal cycle. The logical polarity of ADCK signal can be inverted by the ADCKPOL bit of AFEMD register (No. 0x02).

6.5.9 Offset Control

This IC can control a signal offset from the input signal level.

The 1024-step offset control register is used for signal offset control. The offset is controlled by this register setting. Each channel is assigned a register, and the signal offset can be controlled separately by each register setting.

The signal offset can be controlled within the range of -300 mV to +300 mV. If the register is set to "0x000", the range is set to -300 mV. If the register is set to "0x3FF", the range is set to +300 mV.

Fig.6.18 shows the offset control register and resulting offset values.

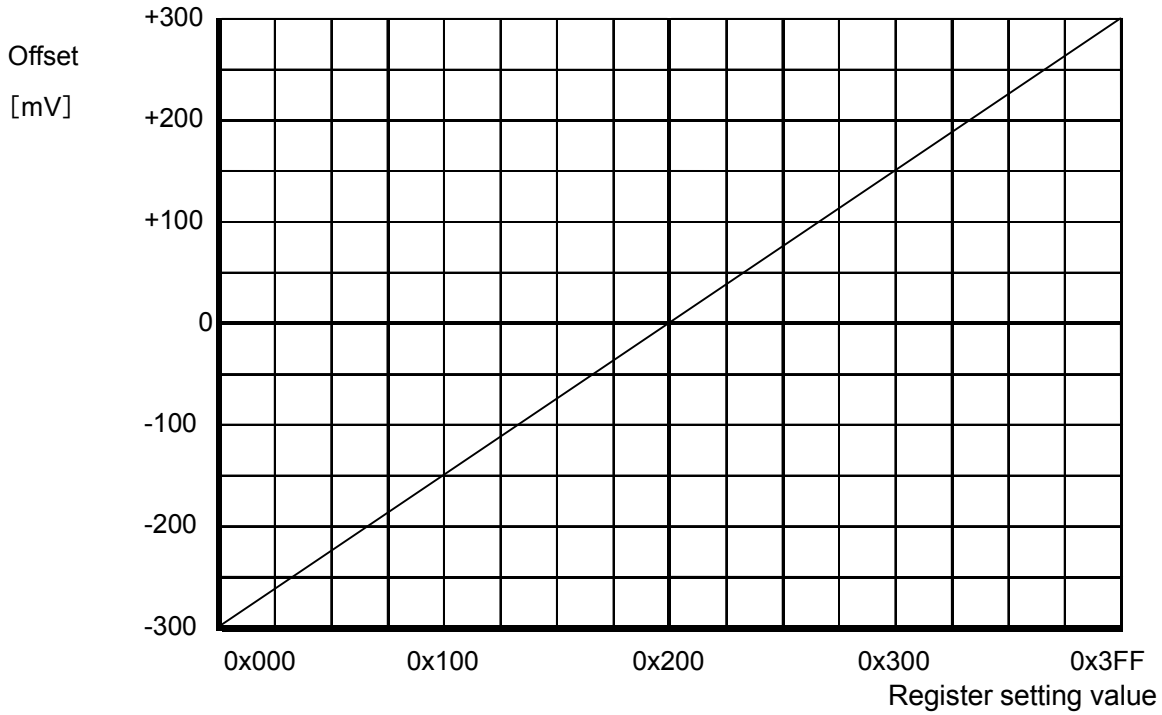


Fig.6.18 Offset Control Characteristics

6.5.10 Programmable Gain Amp (PGA)

This IC incorporates a programmable gain amp (PGA).

The PGA has an 128-step gain control register, and the signal gain can be controlled by this register setting. Each channel is assigned a register, and the signal gain can be controlled separately by each register setting.

The signal gain can be set within the range of -6.9 dB (0.45 time) to +12.0 dB (4 times). If the register is set to "0x00", the minimum gain is set. If the register is set to "0xFE", the maximum gain is set. Also, if the GAINSEL [1:0] bits are set to 01, the signal gain can be set within the range of -0.9 dB (0.9 time) to +18.0 dB (8.0 times). If the GAINSEL [1:0] bits are set to 11, the signal gain can be set within the range of -5.1 dB (1.8 times) to +24.1 dB (16.0 times). Control these signal gains, and set their values to match with the S/D converter input range (1.2 V).

Fig.6.19 shows the gain control register and resulting gain values. Also, the register setting value and the obtained signal gain can be approximately calculated by the following expression.

$$\text{Gain (magnification)} \fallingdotseq \frac{128}{32 + (255 - \text{Register setting value})}$$

Note) If GAINSEL [1:0] bits are set to 00, the gain is equal to the above gain (magnification).
If GAINSEL [1:0] bits are set to 01, the gain is 2 times higher than the above gain (magnification).
If GAINSEL [1:0] bits are set to 11, the gain is 4 times higher than the above gain (magnification).

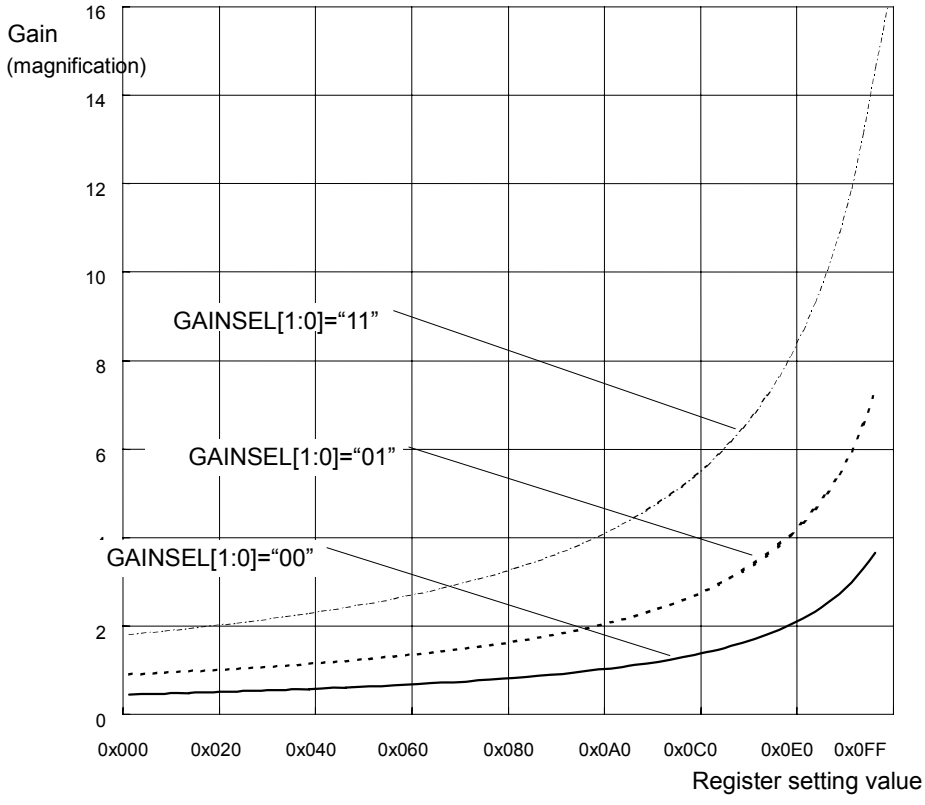


Fig.6.19 Gain Characteristics (Magnification)

Restrictions

PGA characteristics

Setting of 128 steps of gray scales is available from the programmable gain amplifier (PGA) of this IC.

Be sure to use the upper 7 bits for the register setting and set zero for the least significant bit. Refer to Fig.6.19 for the relationship between the register setting and the resulting gain characteristics.

Fig.6.20 shows the relationship between the register setting and output value [LSB] when 0.05 V is entered as the input differential voltage. And it is possible to approximate Fig.6.20 by use of the following expression.

Output value [LSB] ≒ {Input differential voltage × (Gain [magnification]) + err}
err is 0 [LSB] when the register setting (steps) is within the range of 0 and 64.
err is 2.2 [LSB] when the register setting (steps) is within the range of 65 and 127.

However, when the register setting is fixed to a certain value, linearity of the output value to the input differential voltage is secured.

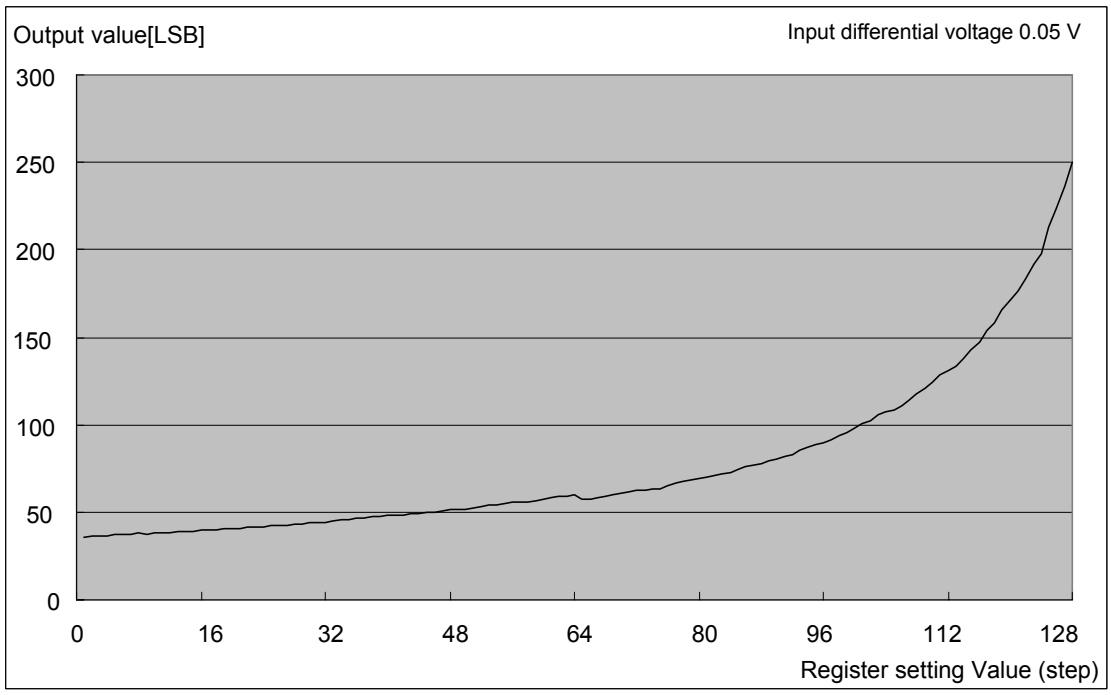


Fig.6.20 Example of Gain Characteristics (Output value [LSB])

6.5.11 Automatic Offset and Gain Control Functions

The automatic offset and gain control functions automatically set a signal offset and control the signal gain before reading an image. The image can be read quickly and easily by this function. These functions automatically control the offset and gain register so that the black level after the A/D conversion of the black-based or black dummy pixel and the white level after A/D conversion of the white-based pixel reaches the value set in the register.

The automatic offset control function or the automatic gain control function is made effective if the AOEN bit and AGEN bit of the AUTOOFSGAIN register (No. 0x0A) are set to "1". These functions can be operated independently from each other. If both bits are set to "1" simultaneously, the both functions are made effective.

The automatic offset and gain control functions operate by analyzing the level of their reference pixel data. Therefore, the input timing of each pixel must be specified. The automatic offset control function requires for 11 lines of data in order to complete the signal offset control. While the automatic gain control function requires for 9 lines of data to complete the signal gain control. If both the automatic offset and gain control functions are activated simultaneously, the automatic gain control function operates only after the automatic signal offset control has completed. In this case, 45 lines of data are required for automatic offset and gain control. After the automatic offset and gain control have completed, both the AOEN bit and AGEN bit of AUTOOFSGAIN register (No. 0x0A) are set to 0 automatically. Also, if the AOGCMPOUT bit of CALCTL register (No. 0x01) is set to 1, its operation status signal can be output to the SD0 pin. After the operation of the control function has completed, the signal goes high. If the automatic offset and gain control functions are activated simultaneously, their state signals are output when the operation of these functions has completed.

Regarding the black level set on BKLEVEL register (No. 0x09) as the lower limit, the automatic offset control function automamtically controls the offset signal closer toward that lower limit value. While, the the automatic gain control function automatically controls the gain signal closer toward toward the white level set on WHLEVEL register (No. 0x08) regarding it as the upper limit. The respective analyses are done on the averaged value of the number of pixels that are present within the specified range and being set for the WHAVE [2:0] bit or BKAVE bit [2:-] of CALCTL register (No. 0x01)

After completion of this signal control, the output pixel level can be monitored by setting the AOGMON bit of CALCTL register (No. 0x01) to 1. Note, as indicated in Table 6.10, that the monitor register is used for other purposes, too.

Table 6.10 List of Monitor Registers

Input channel	Black level monitor	White level monitor
R-channel (Odd)	RD10FS register (No. 0x10)	RD1GAIN register (No. 0x18)
R-channel (Even)	RD20FS register (No. 0x11)	RD2GAIN register (No. 0x19)
G-channel (Odd)	GR10FS register (No. 0x12)	GR1GAIN register (No. 0x1A)
G-channel (Even)	GR20FS register (No. 0x13)	GR2GAIN register (No. 0x1B)
B-channel (Odd)	BL10FS register (No. 0x14)	BL1GAIN register (No. 0x1C)
B-channel (Even)	BL20FS register (No. 0x15)	BL2GAIN register (No. 0x1D)

(1) In CDS mode

The automatic offset control function sets the A/D conversion result of black-based pixels (OB pixels) of the CCD to the black level, and controls the signal offset automatically. Also, the automatic gain control function sets the A/D conversion result of pixels, that are within the range being specified by WHST [3:0] bits of BKWHST register (No. 0x04) and the WHNUM registers (No. 0x06 and 0x07), as the white level to carry out the automatic signal gain control. When specifying the black-based pixel position, set the CLMP pin to high at the same time as the black-based pixel is input. Fig.6.21 shows the operation timing examples.

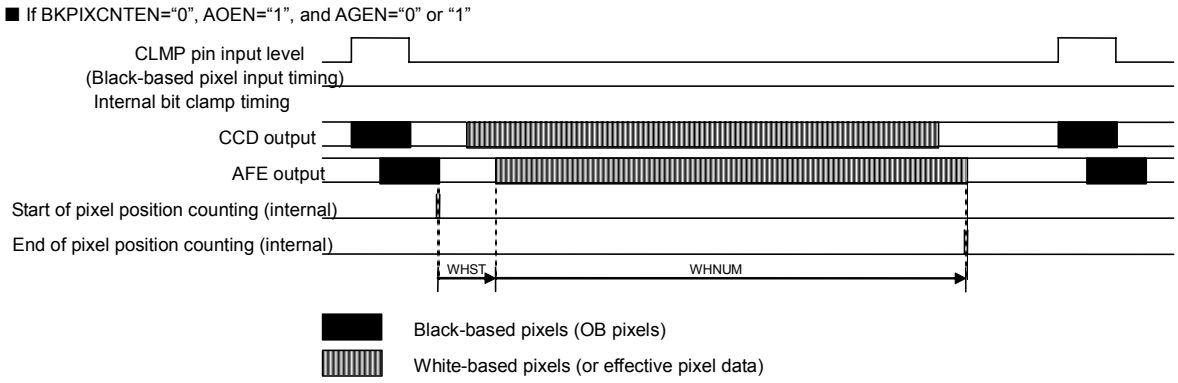


Fig.6.21 Example of Automatic Offset and Gain Control Timings in CDS Mode

(2) In S/H mode

The automatic offset control function sets the A/D conversion result of black dummy pixels of the CCD to the black level as the black level, and controls the signal offset automatically. Like in CDS mode, the automatic gain control function sets the A/D conversion result of pixels, that are within the range specified by the WHST [3:0] bits of BKWHST register (No. 0x04) and the WHNUM registers (No. 0x06 and 0x07), as the white level to carry out automatic control of the signal gain.

The black dummy pixel position can be specified either by the external signal input or by the use of internal pixel position counter. When utilizing the external signal, set the BKPIXCNTEN bit of AUTOOFGAIN register (No. 0x0A) to 0 and then set the CK2 pin signal to logical high at the same time as the black dummy pixel is input. When using the internal pixel position counter, however, set the BKPIXCNTEN bit of BKMNUM register (No. 0x05) to 1, set the black dummy pixel start position for the BKST [5:0] bits of BKWHST register (No. 0x04), and set the number of black dummy pixels for the BKNUM register (No. 0x05) Fig.6.22 shows the operation timing examples.

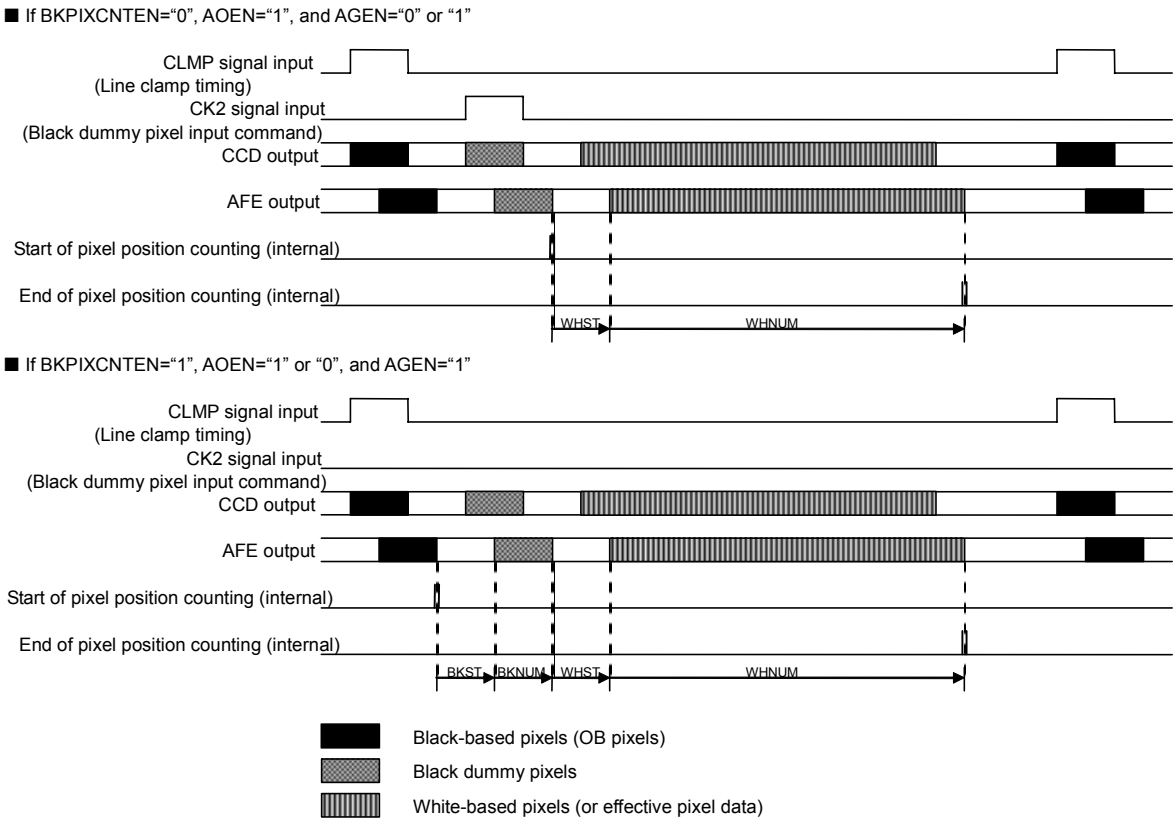


Fig.6.22 Automatic Offset and Gain Control Timing in S/H Mode

6.5.12 Automatic Black Level Compensation Function

If the ABKADJ bit of AUTOOFSGAIN register (No. 0x0A) is set to 1, the automatic black level compensation function is activated. This function absorbs the variation in the black level of the CCD or the variation in the voltage level locking to the clamp level by automatically compensating the offset settings when the document is read by the scanner system.

The automatic black level compensation function analyzes the black level for each line, automatically updates offset setting, and compensates the black level. In the same way as for the automatic offset control function, the black level analysis function analyzes the average of the number of pixels specified in the BKAVE[2:0] bit of the CALCTL register (No. 0x01). After the black level has been analyzed, the offset setting update timing can be switched as shown in Fig.6.23 by setting the HTIM bit of CALCTL register (No. 0x01). For the analysis and adjustment methods, the operation mode can be selected by setting ABKMD bits 0 to 5 of AUTOOFSGAIN register (No. 0x0A).

The specification of black-based pixels in CDS mode or black dummy pixels in S/H mode is the same as for the automatic offset and gain control functions. In such case, set the WHST [3:0] bits of BKWHST register (No. 0x04) and the WHNUM registers (No. 0x06 and 0x07) to appropriate values. Fig.6.20 shows the operation timing examples.

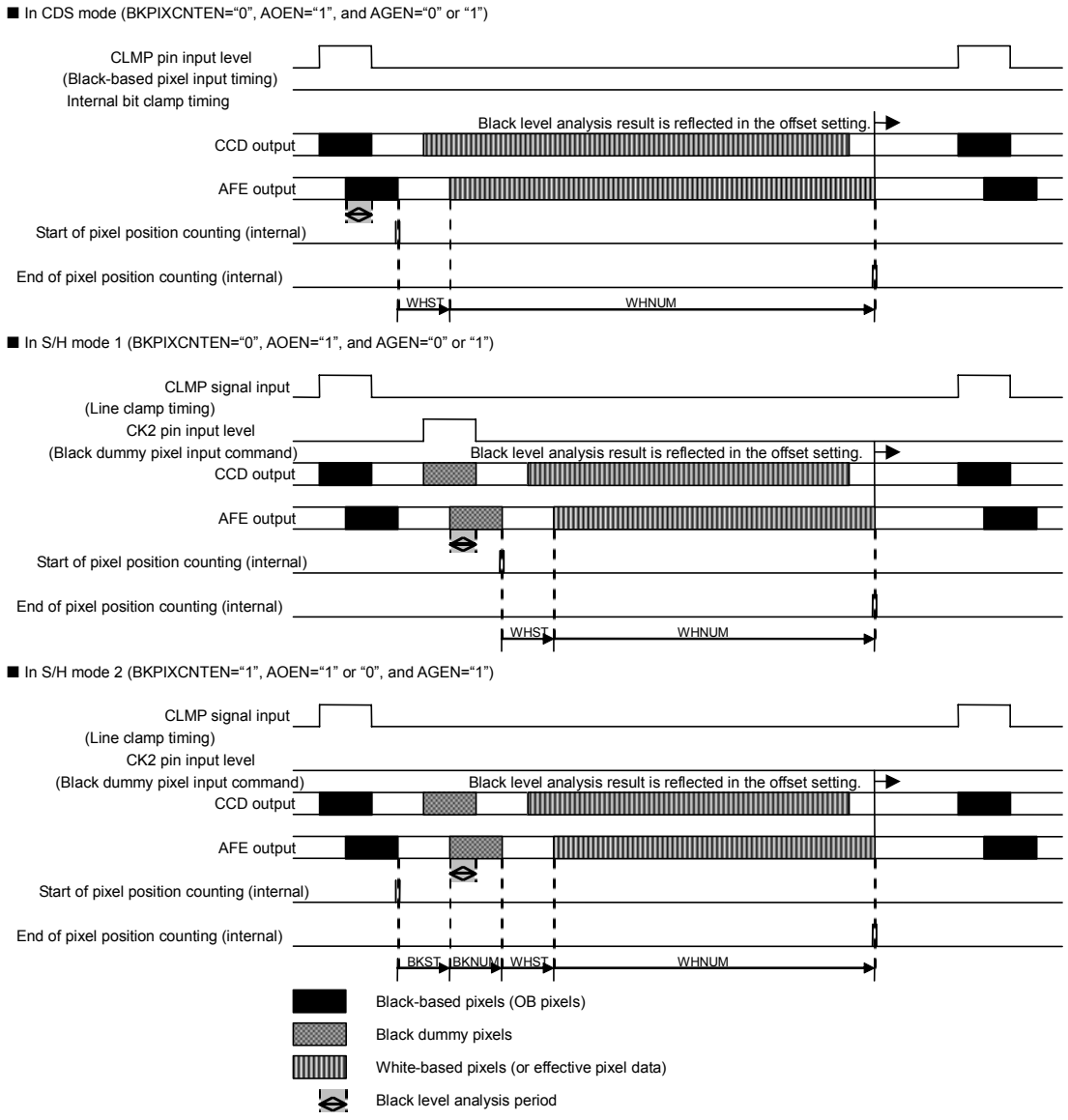


Fig.6.23 Operation Timing Example of Automatic Black Level Compensation Function

(1) Detection of black level variation

The variation of the black level is detected about the avarage of the number of pixels (in the black level analysis period shown in Fig.6.23 which is specified in the BKAVE [2:0] bit of CALCTL register (No. 0x01). The average is analyzed based on the setting of the BKLEVEL register (No. 0x09).

The method of detecting the variation of the black level can be selected by setting the ABKMD4, ABKMD1, or ABKMD0 bit in the AUTOOFSAGIN register (No. 0x0A). The optimum method varies depending on the environment of the application used; therefore, the ABKMD bit must be set to enable the optimum image to be captured.

- Specifying the number of lines to be detected (ABKMD4 bit)

Setting the ABKMD4 bit of the AUTOOFSGAIN register (No. 0x0A) to "0" updates and compensates offset setting when the variation of the black level is detected on two successive lines in the same direction. Setting the ABKMD4 bit to "1" updates and compensates offset setting when the variation of the black level is detected for each line. If the variation of the black level is smaller like in the CDS or S/H mode (differential voltage input), set the ABKMD4 bit to "0" to reduce the compensation level.

- Specifying the detection range (ABKMD1 bit)

The range for detecting the variation of the black level can be specified by setting the ABKMD1 bit of the AUTOOFSGAIN register (No. 0x0A). This range is as shown in Fig.6.24 When the average black level is as shown in Fig.6.24, the black level goes off the set value of the BKLEVEL register (No. 0x09) when the ABKMD1 bit is set to "1". In this case, detect the variation and update offset setting. When the ABKMD1 bit is set to "0", the variation within the range of BKLEVEL register (No. 0x09)+/-n is not sensed. Offset setting is not therefore updated without detecting the variation. The n value in the range of variation, which is equivalent to the 1LSB variation of offset setting in the A/D conversion result, varies depending on gain settings. While, when the gain setting is less than 2 times, this function is carried out on the assumption that 2 = 1.

Example: n value when the gain setting is 4 times

$$\text{Detection range } n = \frac{0.586 \text{ mv (equivalent to 1LSB variation of offset setting)} \times 4 \text{ (gain setting)} \times 1023}{1.2 \text{ Vp-p (Range of A/D conversion)}} = 2$$

Note) Decimals shall be truncated.

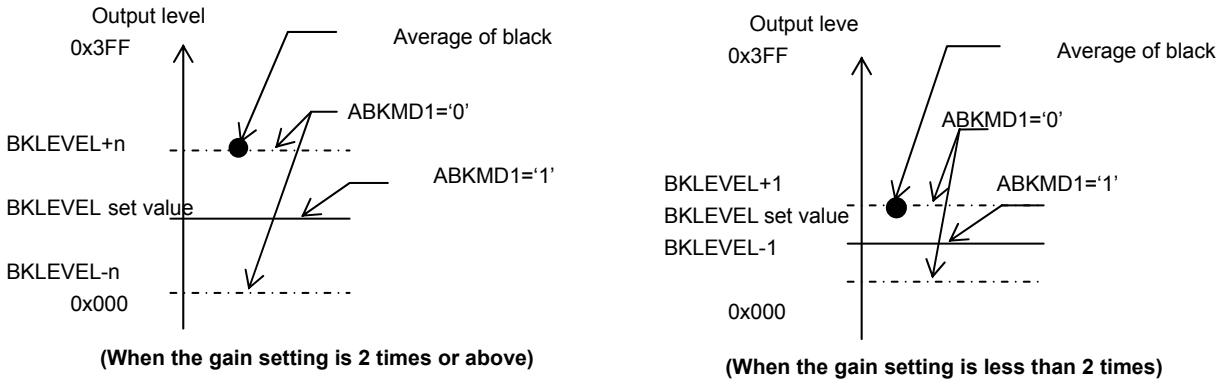


Fig.6.24 Black Level Variation Detection Range

-When the dead zone setting doubled (ABKMD0 bit)

The black level variation detection range can be doubled depending on the setting of the ABDMD0 bit of AUTOFSGAIN register (No. 0x0A) compared with the one obtainable from the setting of ABKMD1 bit. This range is as shown in Fig.6.25 When the average black level is as shown in Fig.6.25, the black level goes off the set value of the BKLEVEL register (No. 0x09) when the ABKMD0 bit is set to "0". In this case, detect the variation and update offset setting. When the ABKMD0 bit is set to "1", the variation within the range of BKLEVEL register (No. 0x09)+/-n x 2 is not sensed. Offset setting is not therefore updated without detecting the variation. The n value in the range of variation, which is equivalent to the 1LSB variation of offset setting in the A/D conversion result, varies depending on gain settings. While, when the gain setting is less than the double, this function is carried out on the assumption that 2 = 1.

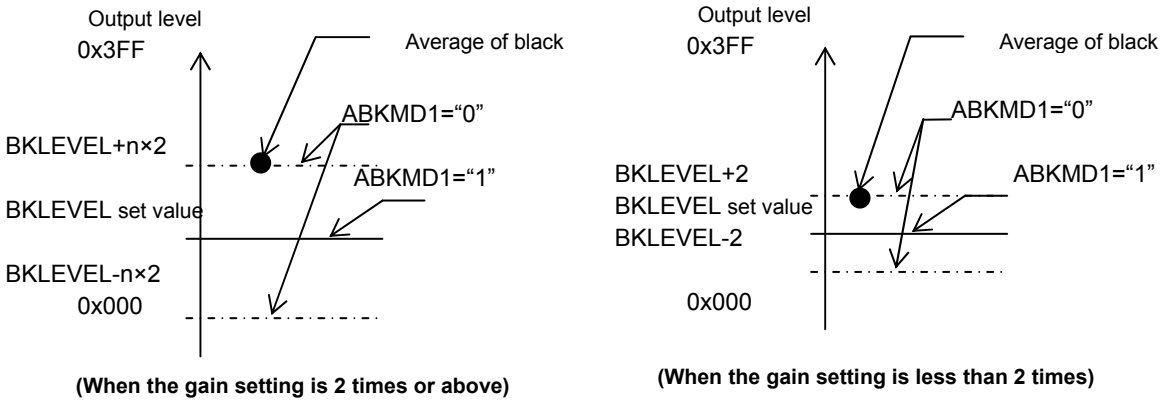


Fig.6.25 Black Level Variation Detection Range (When dead zone is doubled)

(2) Compensation of black level

The method of compensating the detected black-level variation can be selected by setting the ABKMD2, ABKMD3, or ABKMD5 bit in the AUTOOFGAIN register (No. 0x0A). The optimum method varies depending on the environment of the application used; therefore, the ABKMD bit must be set to enable the optimum image to be captured.

-Specifying the target compensation value (ABKMD2 bit)

Set the ABKMD2 bit of the AUTOOFSGAIN register (No. 0x0A) to detect the variation of the black level and define the target compensation value. Setting the ABKMD2 bit to "0" enables you to compensate the set value of the BKLEVEL register (No. 0x09) to the target. Setting the ABKMD2 bit to "1" enables you to compensate the set value of "BKLEVEL register (No. 0x09) + $\overline{n}$" to the target.

Fig.6.26 shows an operation example.

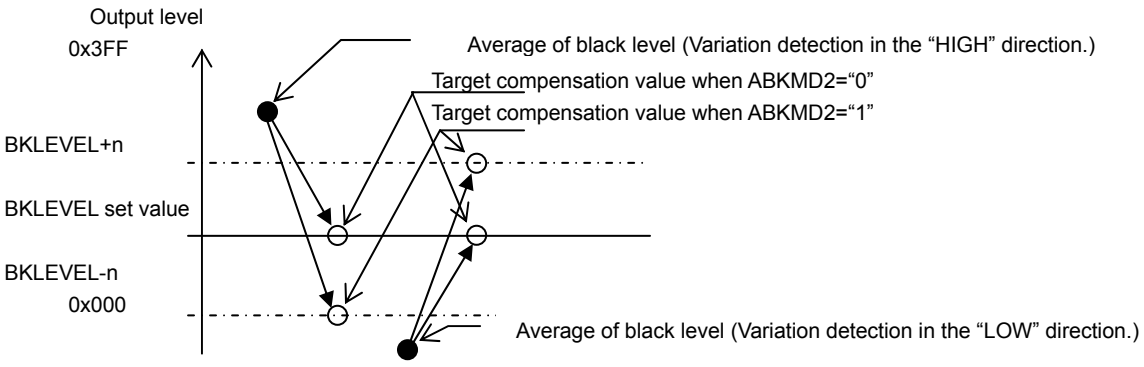


Fig.6.26 Example of Compensation-to-Target Operation

-Specifying the over-compensation value (ABKMD3 bit)

Setting the ABKMD3 bit of the AUTOOFSGAIN register (No. 0x0A) to "1" doubles the compensation value. Setting the ABKMD3 bit to "0" enables you to compensate the target value with the optimum one.

Fig.6.27 shows an operation example.

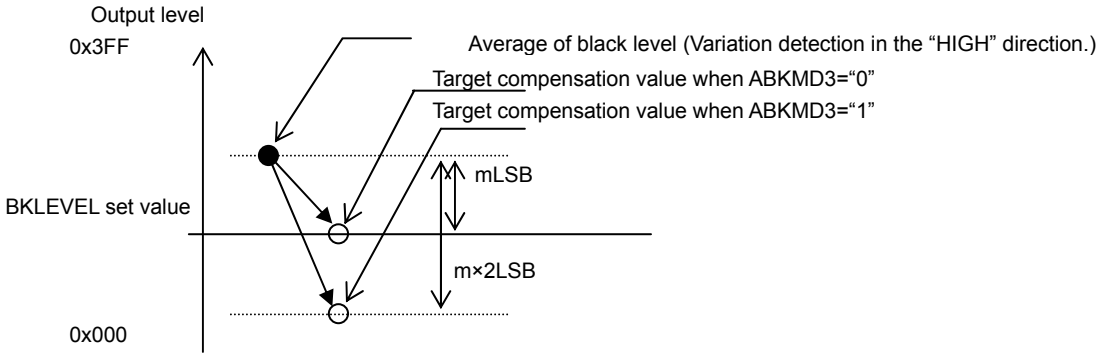


Fig.6.27 Example of Over Compensation Operation

-Specifying the compensation value (ABKMD5 bit)

Setting the ABKMD5 bit of the AUTOOFSGAIN register (No. 0x0A) to "1" will result in the compensation value being set to the target when the variation of the black level has been detected. Setting the ABKMD5 bit to "0" enables you to compensate offset 1LSB when the gain is above double. Setting the gain below double will result in the system conducting the compensation equivalent to 1LSB by A/D conversion.

-Specifying an under-compensation value (ABKMD6 bit)

Setting the ABKMD6 bit of the AUTOOFSGAIN register (No. 0x0A) to "1" halves the compensation value. Setting the ABKMD3 bit to "0" enables you to compensate the target value with the optimum one.

Fig.6.28 shows an operation example.

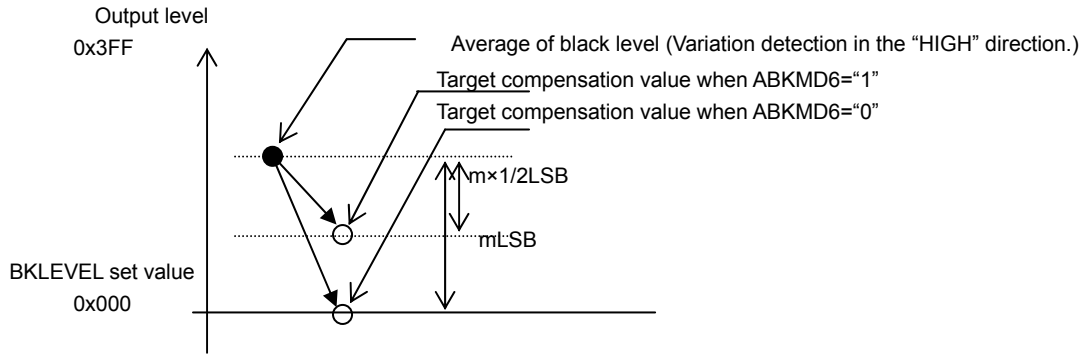


Fig.6.28 Example of Under Compensation Operation

6.5.13 Register Setting Sequence Example

Fig.6.29 shows an example of a register setting sequence ranging from when the power has been turned on or the system has been recovered from the standby state up to image capture. The sequence shown in Fig.6.29 shows a case where "LOW" is input to the XRST pin in the standby state or in the duration ranging from a time when the power has been turned on to a time when the voltage becomes stable. Register setting in each stage (part enclosed in a square) may be in random order.

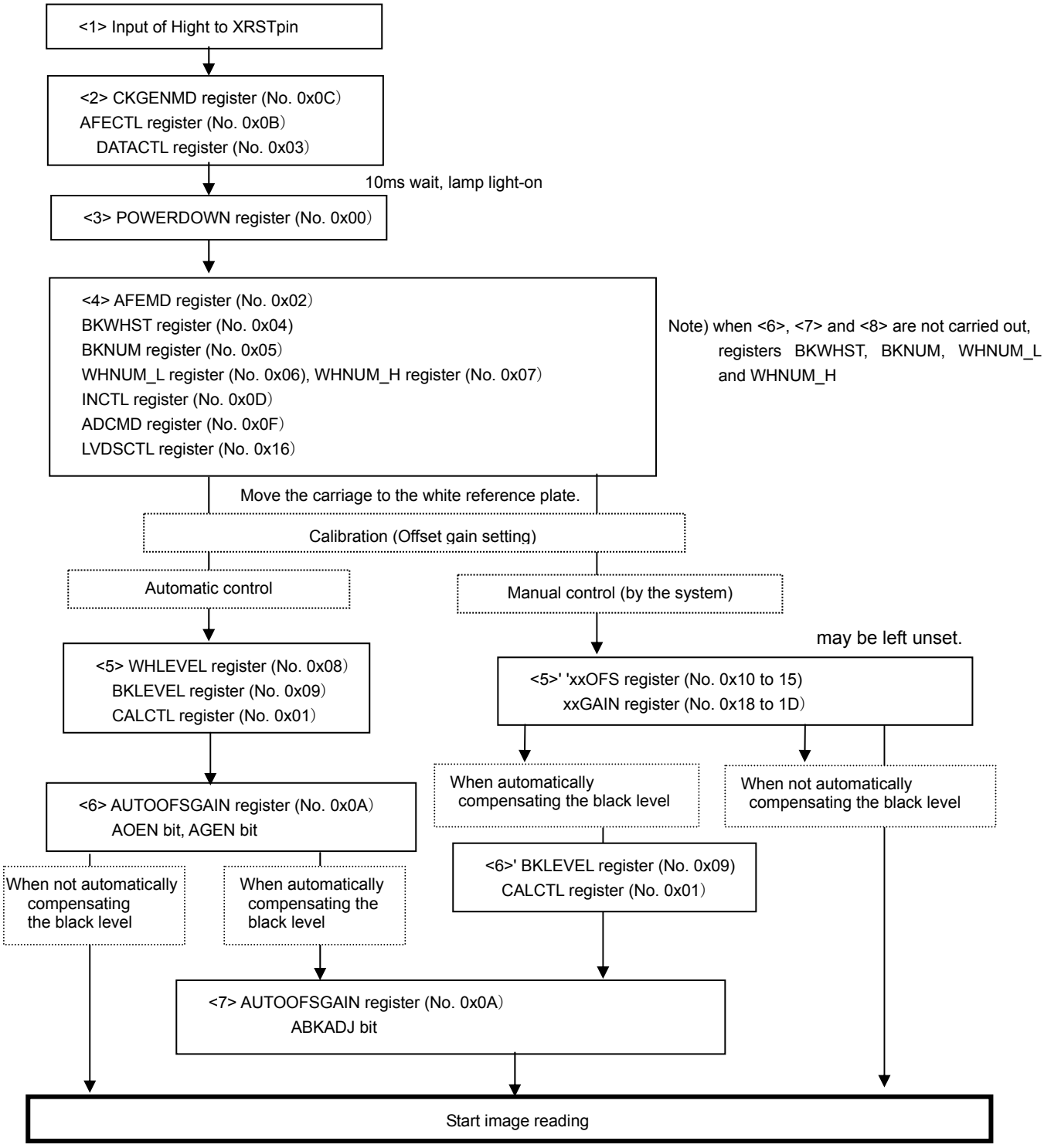


Fig.6.29 Register Setting Sequence Example

7. REGISTERS

7.1 Register Map

No.	Register Name	R/W	Function
0x00	POWERDOWN	R/W	Power down register
0x01	CALCTL	R/W	Image analysis function control register
0x02	AFEMD	R/W	AFE operation mode setting register
0x03	DATACTL	R/W	Data output control register
0x04	BKWHST	R/W	Black and white-based pixel start position setting register
0x05	BKNUM	R/W	Black-based pixel number setting register
0x06	WHNUM_L	R/W	Black-based pixel number setting register (Low level)
0x07	WHNUM_H	R/W	White-based pixel number setting register (High level)
0x08	WHLEVEL	R/W	White-based pixel output level setting register
0x09	BKLEVEL	R/W	Black-based pixel output level setting register
0x0A	AUTOOFSGAIN	R/W	Automatic offset and gain adjustment function setting register
0x0B	AFECTL	R/W	AFE control register
0x0C	CKGENMD	R/W	Sampling signal control register
0x0D	INCTL	R/W	Image control register
0x0E	(Reserved)		
0x0F	ADCMD	R/W	A/D converter operation mode setting register
0x10	RD1OFS	R/W	R-channel (ODD) offset register
0x11	RD2OFS	R/W	R-channel (EVEN) offset register
0x12	GR1OFS	R/W	G-channel (ODD) offset register
0x13	GR2OFS	R/W	G-channel (EVEN) offset register
0x14	BL1OFS	R/W	B-channel (ODD) offset register
0x15	BL2OFS	R/W	B-channel (EVEN) offset register
0x16	LVDSCTL	R/W	LVDS setting register
0x17	(Reserved)		
0x18	RD1GAIN	R/W	R-channel (ODD) gain register
0x19	RD2GAIN	R/W	R-channel (EVEN) gain register
0x1A	GR1GAIN	R/W	G-channel (ODD) gain registe
0x1B	GR2GAIN	R/W	G-channel (EVEN) gain register
0x1C	BL1GAIN	R/W	B-channel (ODD) gain register
0x1D	BL2GAIN	R/W	B-channel (EVEN) gain register
0x1E	(Reserved)		
0x1F	(Reserved)		

7.2 Bit Map

No.	Register Name	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	POWERDOWN							PDLVDS	PDRSDS	PDSTB	PD
0x01	CALCTL	AOGMON	OFSCHTIM		WHAVE[2:0]			AOGCMPOUT	BKAVE[2:0]		
0x02	AFEMD	CLMPLV[3:0]				CLMPPOL	CLMPEN	ADCKPOL	CKPOL	S/HRVS	CDSMD
0x03	DATACTL	TSTMD[1:0]		INSTGO	XOEB	XOEG	XOER	PIXSQMD	MUXSQ	AVEMD	MUXMD
0x04	BKWHST	WHST[3:0]				BKST[5:0]					
0x05	BKNUM	BKPIXCNTEN		BKNUM[7:0]							
0x06	WHNUM_L	WHNUM[9:0]									
0x07	WHNUM_H					WHNUM[15:10]					
0x08	WHLEVEL	WHLEVEL[9:0]									
0x09	BKLEVEL	BKLEVEL[9:0]									
0x0A	AUTOOFSGAIN	ABKMD5	ABKMD4	ABKMD3	ABKMD2	ABKMD1	ABKMD0	AOEN	AGEN	ABKMD6	ABKADJ
0x0B	AFECTL	CKGEN	VCOSEL[1:0]								
0x0C	CKGENMD	CKGENMD									
0x0D	INCTL		LCLMP								
0x0E	(Reserved)										
0x0F	ADCMD			BL[1:0]				BIAS[3:0]			
0x10	RD1OFS	RD1OFS[9:0]									
0x11	RD2OFS	RD2OFS[9:0]									
0x12	GR1OFS	GR1OFS[9:0]									
0x13	GR2OFS	GR2OFS[9:0]									
0x14	BL1OFS	BL1OFS[9:0]									
0x15	BL2OFS	BL2OFS[9:0]									
0x16	LVDSCTL		TX4EN	TX3EN	TX2EN	TX1EN	TX0EN		LVDSDT		PE
0x17	(Reserved)										
0x18	RD1GAIN	RD1GAINSEL[1:0]		RD1GAIN[7:0]							
0x19	RD2GAIN	RD2GAINSEL[1:0]		RD2GAIN[7:0]							
0x1A	GR1GAIN	GR1GAINSEL[1:0]		GR1GAIN[7:0]							
0x1B	GR2GAIN	GR1GAINSEL[1:0]		GR2GAIN[7:0]							
0x1C	BL1GAIN	BL1GAINSEL[1:0]		BL1GAIN[7:0]							
0x1D	BL2GAIN	BL1GAINSEL[1:0]		BL2GAIN[7:0]							
0x1E	(Reserved)										
0x1F	(Reserved)										

7.3 Detailed Description of Registers

7.3.1 0x00 Power-Down Register (POWERDOWN)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x00	POWERDOWN		9:			0x00F
			8:			
			7:			
			6:			
			5:			
			4:			
		R/W	3: PDLVDS	0: Normal	1: power down	
			2: PDRSDS	0: Normal	1: power down	
			1: PDSTB	0: Normal	1: power down	
			0: PD	0: Normal	1: power down	

Bits 9 to 4 Reserved

Bit 3 PDLVDS
This is a power-down register of LVDS section.

Bit 2 PDRSDS
A power-down register of RSDS section

Bit 1 PDSTB
A power-down register of input clock waveform shaper function

Bit 0 PD
A power-down register of analog section

7.3.2 0x01 Pixel Analysis Function Control Register (CALCTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x01	CALCTL	R/W	9: AOGMON	0: Disable	1: Enable	0x000
			8: OFSCHTIM	0: after WHNUM	1: after BKNUM	
			7:			
			6: WHAVE[2]	White-based pixel number setting register		
			5: WHAVE[1]			
			4: WHAVE[0]			
			3: AOGCMPOUT	0: Disable	1: Enable	
			2: BKAVE [2]	Black-based pixel number setting register		
			1: BKAVE [1]			
			0: BKAVE [0]			

Bit 9 AOGMON

If this bit is set to 1, the output pixel level can be monitored after completion of automatic offset and gain control functions.

Bit 8 OFSCHTIM

Sets the offset register update timing when the automatic black level compensation function is effective.

Bit 7 Reserved

Bit 6 to 4 WHAVE [2:0]

Specify the number of pixels that are to be averaged to detect white-based pixels during running of the automatic gain control function.

WHAVE[2:0]: Average number of pixels

000: 1 pixel
001: 2 pixels
010: 4 pixels
011: 8 pixels
100: 16 pixels
101: 32 pixels
110: 64 pixels
111: 128 pixels

Bit 3 AOGCMPOUT

This register outputs the operation state to the SDO pin when the automatic offset and gain control functions or the compensation value detection function are active.

Bit 2 to 0 BKAVE [2:0]

Specify the number of pixels that are to be averaged to detect black-based pixels or black dummy pixels when the automatic offset control and automatic black level compensation functions are effective.

AVENUM [2:0]: Number of pixels detected

000: 1 pixel
001: 2 pixels
010: 4 pixels
011: 8 pixels
100: 16 pixels
101: 32 pixels
110: 64 pixels
111: 128 pixels

7.3.3 0x02 AFE Operation Mode Setting Register (AFEMD)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x02	AFEMD	R/W	9: CLMPLV [3]	Sets a clamp level.		0x000
			8: CLMPLV [2]			
			7: CLMPLV [1]			
			6: CLMPLV [0]			
			5: CLMPPOL	0: Normal	1: Invert	
			4: CLMPEN	0: Disable	1: Enable	
			3: ADCKPOL	0: Normal	1: Invert	
			2: CKPOL	0: Normal	1: Invert	
			1: S/HRVS	0: Normal	1: Reverse	
			0: CDSMD	0: S/H mode	1: CDS mode	

Bits 9 and 6 CLMPLV [3:0]
Sets a clamp level.

Bit 5 CLMPOL
If this bit is set to 1, the logic of CLMP signal is inverted.

Bit 4 CLMPEN
If this bit is set to 1, a clamp level is internally generated. Also, if this bit is set to 1 in the CDS mode, a bit clamp occurs automatically.

Bit 3 ADCKPOL
If this bit is set to 1, the logic of ADCK signal is inverted.

Bit 2 CKPOL
If this bit is set to 1, the logic of CK1 and CK2 signals is inverted.

Bit 1 S/HRVS
In the S/H mode, set this bit according to the polarity of differential voltage between the CLMPLV/INN pin signal level and the signal level of analog inputs (RINP, GINP and BINP).
"0":CLMPLV/INN < RINP (GINP, BINP)
"1":CLMPLV/INN > RINP (GINP, BINP)
This register setting is ineffective in the CDS mode.

Bit 0 CDSMD
Selects one of the following AFE sampling methods.
0: S/H mode
1: CDS mode

7.3.4 0x03 Data Output Control Register (DATACTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x03	DATACTL	R/W	9: TSTMD [1]	Test mode setting register		0x070
			8: TSTMD [0]			
			7: INSTGO	0: Disable	1: Enable	
			6: XOEB	0: Enable	1: Disable	
			5: XOEG	0: Enable	1: Disable	
			4: XOER	0: Enable	1: Disable	
			3: PIXSQMD	0: Normal	1: pixel sequence	
			2: MUXSQ	0: Normal	1: Reverse	
			1: AVEMD	0: Normal	1: average mode	
			0: MUXMD	0: Normal	1: multiplex mode	

Bits 9 and 8 TSTMD [1:0]
Select the test mode.

Bit 7 INSTGO
If this bit is set to 1, the monitoring function is activated.

Bit 6 XOEB
0: Makes the B-channel output effective.
1: Inhibits the B-channel output (to cause zero output).

Bit 5 XOEG
0: Makes the G-channel output effective.
1: Inhibits the G-channel output (to cause zero output).

Bit 4 XOER
0: Makes the R-channel output effective.
1: Inhibits the R-channel output (to cause zero output).

Bit 3 PIXSQMD
0: Selects the normal output mode.
1: Selects the point sequential output mode.

Bit 2 MUXSQ
Allows to select the multiplexed output sequence as follows.
0: From odd to even
1: From even to odd
Also, this bit can set the output channel during normal output (not multiplexed output) as follows.
0: Odd
1: Even

Bit 1 AVEMD
If this bit is set to 1, the two-pixel averaging function is activated.

Bit 0 MUXMD
Selects the image data output mode as follows.
0: Odd or even in normal mode
1: Odd and even in multiplexed mode

Restriction
Before setting MUXMD, AVEMD, and PIXSQMD bits, set PDLVDS and PDSTB bits of POWERDOWN register (No. 0x00) PDLVDS to “1”.

7.3.5 0x04 Black Dummy Pixel and White-Based Pixel Start Position Setting Register (BKWHST)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x04	BKWHST	R/W	9: WHST [3]	White-based pixel start position setting register	0x000
			8: WHST [2]		
			7: WHST [1]		
			6: WHST [0]		
			5: BKST [5]	Black dummy pixle start position setting register	
			4: BKST [4]		
			3: BKST [3]		
			2: BKST [2]		
			1: BKST [1]		
			0: BKST [0]		

This register is used for setting the black dummy pixel and white-based pixel start position. Set this register value for each pixel.

Restriction

Before changing this register value, be sure to set the INSTGO bit of DATACTL register (No. 0x03) and the AOEN, AGEN, ABKST and ABKADJ bits of AUTOOFGAIN register (No. 0x0A) to 0.

7.3.6 0x05 Black Dummy Pixel Number Setting Register (BKNUM)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x05	BKNUM	R/W	9: BKPIXCNTEN	0: Disable	1: Enable	0x000
			8:			
		R/W	7: BKNUM [7]	Black-based pixel number setting register		
			6: BKNUM [6]			
			5: BKNUM [5]			
			4: BKNUM [4]			
			3: BKNUM [3]			
			2: BKNUM [2]			
			1: BKNUM [1]			
			0: BKNUM [0]			

Bit 9 BKPIXCNTEN
Activate the pixel position count function when detecting the black dummy pixel position.

Bit 8 Reserved

Bit 7 to 0 BKNUM[7:0]
This register is used for stting the number of black dummy pixels. Set this register value for each pixel.

Restriction

Before changing this register value, be sure to set the INSTGO bit of DATACTL register (No. 0x03) and the AOEN, AGEN, ABKST and ABKADJ bits of AUTOOFGAIN register (No. 0x0A) to 0.

And when using CDS mode, set this register to 0x000.

7.3.7 0x06 to 0x07 White-Based Pixel Number Setting Registers (WHNUM)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x07	WHNUM_H		9:		0x000
			8:		
			7:		
			6:		
		R/W	5: WHNUM [15]	White-based pixel number setting register	
			4: WHNUM [14]		
			3: WHNUM [13]		
			2: WHNUM [12]		
			1: WHNUM [11]		
			0: WHNUM [10]		
0x06	WHNUM_L		9: WHNUM [9]		0x001
			8: WHNUM [8]		
			7: WHNUM [7]		
			6: WHNUM [6]		
			5: WHNUM [5]		
			4: WHNUM [4]		
			3: WHNUM [3]		
			2: WHNUM [2]		
			1: WHNUM [1]		
			0: WHNUM [0]		

This is a white-based pixel number setting register. Set this register value for each pixel.

Restriction 1

Before changing this register value, be sure to set the INSTGO bit of DATACTL register (No. 0x03) and the AOEN, AGEN, ABKST and ABKADJ bits of AUTOOFGAIN register (No. 0x0A) to 0.

Restriction 2

Set the WHNUM bits within the following range: WHNUM ≥ 1

7.3.8 0x08 White Pixel Output Level Setting Register (WHLEVEL)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x08	WHLEVEL	R/W	9: WHLEVEL [9]	Sets a white pixel output level.	0x000
			8: WHLEVEL [8]		
			7: WHLEVEL [7]		
			6: WHLEVEL [6]		
			5: WHLEVEL [5]		
			4: WHLEVEL [4]		
			3: WHLEVEL [3]		
			2: WHLEVEL [2]		
			1: WHLEVEL [1]		
			0: WHLEVEL [0]		

This register sets the upper limit of white level when the automatic gain control function is effective.

7.3.9 0x09 Black Pixel Output Level Setting Register (BKLEVEL)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x09	BKLEVEL	R/W	9: BKLEVEL [9]	Sets a black pixel output level.	0x000
			8: BKLEVEL [8]		
			7: BKLEVEL [7]		
			6: BKLEVEL [6]		
			5: BKLEVEL [5]		
			4: BKLEVEL [4]		
			3: BKLEVEL [3]		
			2: BKLEVEL [2]		
			1: BKLEVEL [1]		
			0: BKLEVEL [0]		

This register sets a black-based pixel output level when the automatic offset control function or automatic black level compensation function is effective.

7.3.10 0x0A Automatic Offset and Gain Control Function Setting Register (AUTOOFSGAIN)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x0A	AUTOOFSGAIN	R/W	9: ABKMD5	0: static adjustment	1: dynamic adjustment	0x000
			8: ABKMD4	0: 1 line filter	1: filter disable	
			7: ABKMD3	0: moderate adjustment	1: extreme adjustment	
			6: ABKMD2	0: normal correction	1: over correction	
			5: ABKMD1	0: low sensitivity	1: high sensitivity	
			4: ABKMD0	0: low sensitivity	1:very low sensitivity	
			3: AOEN	0: Disable	1: Enable	
			2: AGEN	0: Disable	1: Enable	
			1: ABKMD6	0: Disable	1: Enable	
			0: ABKADJ	0: Disable	1: Enable	

Bit 9 ABKMD5

Sets the amount of compensation required to update the offset register.
"0": Amount of compensation in a single unit on a line basis
"1": Amount of compensation of corresponding to the variation in black-level

Bit 8 ABKMD4

Sets the number of lines that were detected in the variation of the black level.
"0": Compensated when the variation of the black level has been detected on two successive lines.
"1": Compensated when the variation in the black level has been detected on every line.

Bit 7 ABKMD3

Sets the amount of compensation required to update the offset register.
"0": Amount of compensation of corresponding to the variation in black-level
"1": Doubles the amount of compensation.

Bit 6 ABKMD2

Sets the target amount of compensation after the variation of the black level has been detected.
"0": Compensates BKLEVEL[9:0] setting to the target.
"1": An amount of compensation corresponding to the offset setting+/-1LSB is done beyond BKLEVEL [9:0].

Bit 5 ABKMD1

Sets the threshold when the variation of the black level has been detected.
"0": Performs compensation when a variation in the black level has exceeded offset setting+/-1LSB.
"1": Performs compensation when the black level has deviated from BKLEVEL [9:0] setting.

Bit 4 ABKMD0

Doubles the dead zone when "0" is set for ABKMD1 bit.
"0": Performs compensation when the variation of the black level has exceeded the range of BKLEVEL [9:0]+/-1LSB.
"1": Performs compensation when a variation in black level beyond the range of BKLEVEL [9:0]+/-1LSB is detected.

Bit 3 AOEN

Set "1" when starting the automatic offset control function. This bit is automatically reset to 0 after the function has been completed.

Bit 2 AGEN

Set "1" when starting the automatic gain control function. This bit is automatically reset to 0 after the function has been completed.

Bit 1 ABKMD6

Sets the amount of compensation required to update the offset register.
"0": Amount of compensation of corresponding to the variation in black-level
"1": Halves the amount of compensation.

Bit 0 ABKADJ

If this bit is set to 1, the automatic black level compensation function is made effective.

Restriction 1

This register can be accessed only when an ADCK signal is entered (during normal operation).

Restriction 2

After the automatic offset and gain control functions or the compensation value detection function have been activated (by setting the AOEN or AGEN bit to “1”), any access to other registers is inhibited until the current operation is completed.

Restriction 3

If the automatic offset and gain control functions or the compensation value detection function are effective (by setting the AOEN or AGEN bit to “1”), set both the AOEN and AGEN bits to 0 simultaneously to cancel the current operation.

7.3.11 0x0B AFE Control Register (AFECTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x0B	AFECTL	R/W	9: CKGEN	0: Disable	1: Enable	0x000
			8: VCOSEL[1]	ADCK signal frequency setting register		
			7: VCOSEL[0]			
			6:			
			5:			
			4:			
			3:			
			2:			
			1:			
			0:			

Bit 9 CKGEN

If this bit is set to 1, a sampling timing signal of external input is automatically and internally generated in the S/H mode.

Bit8 to 7 VCOSEL [1:0]

Set these bits according to the frequency of ADCK signal, that is entered in the input clock waveform shaper function, as follows.

VCOSEL [1:0]: Set the ADCK signal frequency.

	If PIXSQMD=0	If PIXSQMD=1
11:	25 - 40 MHz	8.3 - 13.3 MHz
10:	20 - 25 MHz	6.6 - 8.3 MHz
01:	12.5 - 20 MHz	4.1 - 6.6 MHz
00:	5.0 - 12.5 MHz	1.66 - 4.1 MHz

Bits 6 to 0 Reserved

Restriction

Before setting the VCOSEL [1:0] bits, be sure to set the PDLVDS and PDSTB bits of POWERDOWN register (No. 0x00) to 1.

7.3.12 0x0C Sampling Signal Control Register(CKGENMD)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x0C	CKGENMD	R/W	9: CKGENMD	0: Normal	1: delay rising edge	0x000
			8:			
			7:			
			6:			
			5:			
			4:			
			3:			
			2:			
			1:			
			0:			

Bit 9 Reserved

Bit 8 CKGENMD
When sampling signal is automatically generated, this register allows cutting the pulse duration shot by delaying (approximately 2 - 7 ns) the rising edge of the internally generated timing sampling signal.

Bit 7 to 0 Reserved

7.3.13 0x0D Input Control Register (INCTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x0D	INCTL		9:			0x000
		R/W	8: LCLMP	0: Normal	1: line clamp mode	
			7:			
			6:			
			5:			
			4:			
			3:			
			2:			
			1:			
			0:			

Bit 9 Reserved

Bit 8 LCLMP
This register controls the buffer amplifier function on the analog input section. Normally “1” is set when its function is turned on in the S/Hmode (line clamp).

Bit 7 to 0 Reserved

7.3.14 0x0F A/D Converter Operation Mode Setting Register (ADCMD)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x0F	ADCMD		9:		0x049
			8:		
		R/W	7: BL [1]	Buffer amp capacity setting	
			6: BL [0]		
			5:		
			4:		
		R/W	3: BIAS [3]	Sets A/D converter bias current.	
			2: BIAS [2]		
			1: BIAS [1]		
			0: BIAS [0]		

Bit 9 to 8 Reserved

Bit 7 to 6 BL[1:0]

This register controls processing capability of the buffer amp function by controlling bias current conducted to the buffer amp. Normally, the default value "1" is set for use.

BL[1:0]: Buffer amp capacity setting

11: 1.7 times
10: 1.4 times
01: 1 time (Default value)
00: 0.5 times

Bit 5 to 8 Reserved

Bit 3 to 0 BIAS [1:0]

This is a bias current control register. Bias current can be controlled to have a better image quality.Fig.7.1 shows the bias currenct characteristics.

Reference setting example

ADCK signal frequency	Set value (Reference)	Bias current [Magnification]
10 to 20 MHz	0x9	1.0
20 to 30 MHz	0xB	1.2
30 to 40 MHz	0xD	1.5

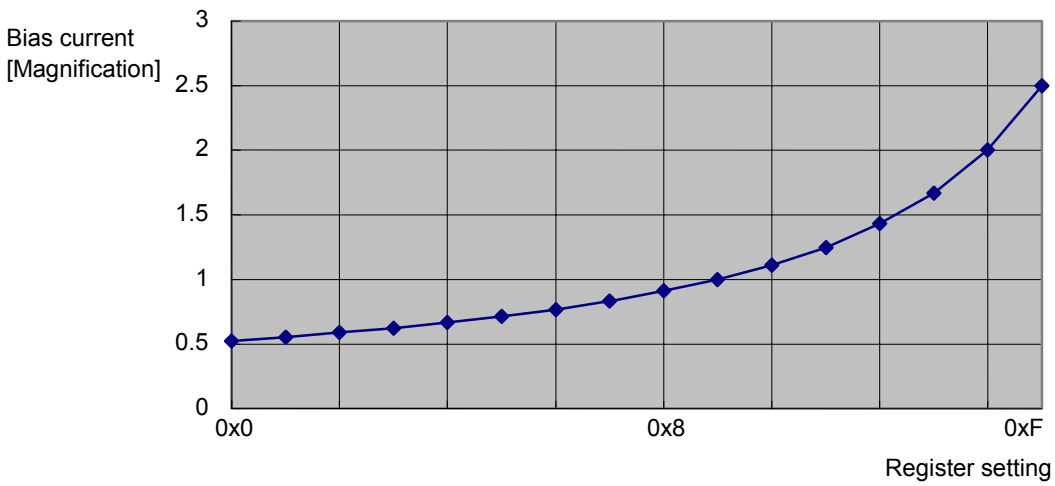


Fig.7.1 Bias Setting

7.3.15 0x10 R-Channel (Odd) Offset Register (RD1OFS)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x10	RD1OFS	R/W	9: RD1OFS [9]	R-channel (odd) offset register	0x200
			8: RD1OFS [8]		
			7: RD1OFS [7]		
			6: RD1OFS [6]		
			5: RD1OFS [5]		
			4: RD1OFS [4]		
			3: RD1OFS [3]		
			2: RD1OFS [2]		
			1: RD1OFS [1]		
			0: RD1OFS [0]		

This is an R-channel (odd) offset setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).

7.3.16 0x11 R-Channel (Even) Offset Register (RD2OFS)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x11	RD2OFS	R/W	9: RD2OFS[9]	R-channel (even) offset register	0x200
			8: RD2OFS[8]		
			7: RD2OFS[7]		
			6: RD2OFS[6]		
			5: RD2OFS[5]		
			4: RD2OFS[4]		
			3: RD2OFS[3]		
			2: RD2OFS[2]		
			1: RD2OFS[1]		
			0: RD2OFS[0]		

This is an R-channel (even) offset setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).

7.3.17 0x12 G-Channel (Odd) Offset Register (GR1OFS)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x12	GR1OFS	R/W	9: GR1OFS[9]	G-channel (odd) offset register	0x200
			8: GR1OFS[8]		
			7: GR1OFS[7]		
			6: GR1OFS[6]		
			5: GR1OFS[5]		
			4: GR1OFS[4]		
			3: GR1OFS[3]		
			2: GR1OFS[2]		
			1: GR1OFS[1]		
			0: GR1OFS[0]		

This is a G-channel (odd) offset setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).

7.3.18 0x13 G-Channel (Even) Offset Register (GR2OFS)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x13	GR2OFS	R/W	9: GR2OFS[9]	G-channel (even) offset register	0x200
			8: GR2OFS[8]		
			7: GR2OFS[7]		
			6: GR2OFS[6]		
			5: GR2OFS[5]		
			4: GR2OFS[4]		
			3: GR2OFS[3]		
			2: GR2OFS[2]		
			1: GR2OFS[1]		
			0: GR2OFS[0]		

This is a G-channel (even) offset setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).

7.3.19 0x14 B-Channel (Odd) Offset Register (BL1OFS)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x14	BL1OFS	R/W	9: BL1OFS[9]	B-channel (odd) offset register	0x200
			8: BL1OFS[8]		
			7: BL1OFS[7]		
			6: BL1OFS[6]		
			5: BL1OFS[5]		
			4: BL1OFS[4]		
			3: BL1OFS[3]		
			2: BL1OFS[2]		
			1: BL1OFS[1]		
			0: BL1OFS[0]		

This is a B-channel (odd) offset setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).

7.3.20 0x15 B-Channel (Even) Offset Register (BL2OFS)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x15	BL2OFS	R/W	9: BL2OFS[9]	B-channel (even) offset register	0x200
			8: BL2OFS[8]		
			7: BL2OFS[7]		
			6: BL2OFS[6]		
			5: BL2OFS[5]		
			4: BL2OFS[4]		
			3: BL2OFS[3]		
			2: BL2OFS[2]		
			1: BL2OFS[1]		
			0: BL2OFS[0]		

This is a B-channel (even) offset setting register.

Restriction
This register can be accessed only when an ADCK signal is entered (during normal operation).

7.3.21 0x16 LVDS Setting Register (LVDSCTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x16	LVDSCTL		9:			0x1F0
		R/W	8: TX4EN	0: Disable	1: Enable	
			7: TX3EN	0: Disable	1: Enable	
			6: TX2EN	0: Disable	1: Enable	
			5: TX1EN	0: Disable	1: Enable	
			4: TX0EN	0: Disable	1: Enable	
			3:			
		R/W	2: LVDSDT	0: Disable	1: Enable	
			1:			
		R/W	0: PE	0: Disable	1: Enable	

Bit 9 Reserved

Bit 8 TX4EN
0: Disables Tx4P/N output (causes zero output).
1: Enables Tx4P/N output

Bit 7 TX3EN
0: Inhibits Tx3P/N output (causes zero output).
1: Enables Tx3P/N output

Bit 6 TX2EN
0: Disable Tx2P/N output (causes zero output).
1: Enables Tx2P/N output

Bit 5 TX1EN
0: Disables Tx2P/N output (causes zero output).
1: Enables Tx1P/N output

Bit 4 TX0EN
0: Disables Tx0P/N output (causes zero output).
1: Enables Tx0P/N output

Bit 3 Reserved

Bit 2 LVDSDT
If this bit is set to 1, the Test Code Output function is activated.

Bit 1 Reserved

Bit 0 PE
If this bit is set to 1, more switching current is flown by the pre-emphasis function.

7.3.22 0x18 R-Channel (Odd) Gain Register (RD1GAIN)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x18	RD1GAIN	R/W	9: RD1GAINSEL[1]	R-channel (odd) gain control range switching register	0x09F
			8: RD1GAINSEL[0]		
			7: RD1GAIN[7]	R-channel (odd) gain register	
			6: RD1GAIN[6]		
			5: RD1GAIN[5]		
			4: RD1GAIN[4]		
			3: RD1GAIN[3]		
			2: RD1GAIN[2]		
			1: RD1GAIN[1]		
			0: RD1GAIN[0]		

This is an R-channel (odd) gain setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).
Zero must always be set for the least significant bit (bit 0).

7.3.23 0x19 R-Channel (Even) Gain Register (RD2GAIN)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x19	RD2GAIN	R/W	9: RD2GAINSEL[1]	R-channel (even) gain control range switching register	0x09F
			8: RD2GAINSEL[0]		
			7: RD2GAIN[7]	R-channel (even) gain register	
			6: RD2GAIN[6]		
			5: RD2GAIN[5]		
			4: RD2GAIN[4]		
			3: RD2GAIN[3]		
			2: RD2GAIN[2]		
			1: RD2GAIN[1]		
			0: RD2GAIN[0]		

This is an R-channel (even) gain setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).
Zero must always be set for the least significant bit (bit 0).

7.3.24 0x1A G-Channel (Odd) Gain Register (GR1GAIN)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x1A	GR1GAIN	R/W	9: GR1GAINSEL[1]	G-channel (odd) gain control range switching register	0x09F
			8: GR1GAINSEL[0]		
			7: GR1GAIN[7]	G-channel (odd) gain register	
			6: GR1GAIN[6]		
			5: GR1GAIN[5]		
			4: GR1GAIN[4]		
			3: GR1GAIN[3]		
			2: GR1GAIN[2]		
			1: GR1GAIN[1]		
			0: GR1GAIN[0]		

This is a G-channel (odd) gain setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).
Zero must always be set for the least significant bit (bit 0).

7.3.25 0x1B G-Channel (Even) Gain Register (GR2GAIN)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x1B	GR2GAIN	R/W	9: GR2GAINSEL[1]	G-channel (even) gain control range switching register	0x09F
			8: GR2GAINSEL[0]		
			7: GR2GAIN[7]	G-channel (even) gain register	
			6: GR2GAIN[6]		
			5: GR2GAIN[5]		
			4: GR2GAIN[4]		
			3: GR2GAIN[3]		
			2: GR2GAIN[2]		
			1: GR2GAIN[1]		
			0: GR2GAIN[0]		

This is a G-channel (even) gain setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).
Zero must always be set for the least significant bit (bit 0).

7.3.26 0x1C B-Channel (Odd) Gain Register (BL1GAIN)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x1C	BL1GAIN	R/W	9: BL1GAINSEL[1]	B-channel (odd) gain control range switching register	0x09F
			8: BL1GAINSEL[0]		
			7: BL1GAIN[7]	B-channel (odd) gain register	
			6: BL1GAIN[6]		
			5: BL1GAIN[5]		
			4: BL1GAIN[4]		
			3: BL1GAIN[3]		
			2: BL1GAIN[2]		
			1: BL1GAIN[1]		
			0: BL1GAIN[0]		

This is a B-channel (odd) gain setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).
Zero must always be set for the least significant bit (bit 0).

7.3.27 0x1D B-Channel (Even) Gain Register (BL2GAIN)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x1D	BL2GAIN	R/W	9: BL2GAINSEL[1]	B-channel (even) gain control range switching register	0x09F
			8: BL2GAINSEL[0]		
			7: BL2GAIN[7]	B-channel (even) gain register	
			6: BL2GAIN[6]		
			5: BL2GAIN[5]		
			4: BL2GAIN[4]		
			3: BL2GAIN[3]		
			2: BL2GAIN[2]		
			1: BL2GAIN[1]		
			0: BL2GAIN[0]		

This is a B-channel (even) gain setting register.

Restriction

This register can be accessed only when an ADCK signal is entered (during normal operation).
Zero must always be set for the least significant bit (bit 0).

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}*1	-0.3 to +4.0	V
	AV_{DD}*1	-0.3 to +4.0	V
	TX_V_{DD}*	-0.3 to +4.0	V
	RX_V_{DD}*	-0.3 to +4.0	V
Input voltage	VI	-0.3 to V_{DD}+0.5 (-0.3V to +7.0V at 5V tolerant input pin)	V
	AVI	-0.3 to AV_{DD}+0.5	V
	RXVI	-0.3 to RXV_{DD}+0.5	V
Output voltage	VO	-0.3 to V_{DD}+0.5	V
	AVO	-0.3 to AV_{DD}+0.5	V
	TXVO	-0.3 to TXV_{DD}+0.5	V
Output current/pin	IOUT	±30	mA
Storage temperature	Tstg	-65 to 150	°C
Package thermal resistance*2	θj-a	44	°C/W
	θj-c	6	°C/W

*1 V_{DD} = AV_{DD} = TX_V_{DD} = RX_V_{DD} V_{SS}=0V, AGND=0V, TX_V_{SS}=0V, RX_V_{SS} =0V

*2 When equipped with JEDEC STD board (114.3×76.2×1.6 mm, 4 layers) and under dead calm condition

8.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.135	3.300	3.465	V
	AV_{DD}	3.135	3.300	3.465	V
	TX_V_{DD}	3.135	3.300	3.465	V
	RX_V_{DD}	3.135	3.300	3.465	V
Input voltage	VI	V_{SS}	—	V_{DD}	V
	AVI	AGND	—	AV_{DD}	V
	RXVI	RXV_{SS}	—	RXV_{DD}	V
Ambient temperature	Ta	0	25	70	°C
Surface temperature of the package	Ts	—	—	100	°C
Rising edge of input (normal input)	tri*	—	—	50	ns
Input fall (normal output)	tfa*	—	—	50	ns
Rising edge of input (Schmidt input)	tri*	—	—	5	ms
Falling edge of input (Schmidt input)	tfa*	—	—	5	ms

* Time required for V_{DD} to change from 10% to 90% V_{SS}=0V, AGND=0V

8.3 DC Characteristics

(1) Input/output characteristics in DC state

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static current	I_{DDS}	V_{DD}=3.3V±5%, 25°C	—	—	10	μA
	AI_{DDS}	AV_{DD}=3.3V±5%, 25°C	—	—	10	μA
	TXI_{DDS}	TX_V_{DD}=3.3V±5%, 25°C	—	—	10	μA
	RXI_{DDS}	RX_V_{DD}=3.3V±5%, 25°C	—	—	10	μA
Current consumption	I_{DD} *	V_{DD}=3.3V±5%	—	66	—	mA
	AI_{DD}	AV_{DD}=3.3V±5%	—	179	—	mA
	TXI_{DD}	TX_V_{DD}=3.3V±5%	—	38	—	mA
	RXI_{DD}	RX_V_{DD}=3.3V±5%	—	9	—	mA
Input leak current	I_{LI}	V_{DD}=3.3V, V_{IH}=V_{DD}, V_{IL}=V_{SS}	-5	—	5	μA
Off-state leak current	I_{OZ}	—	-5	—	5	μA

* At no-load to external pins

(2) Input characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	LVTTL, V_{DD}=Max.	2.0	—	—	V
Low-level input voltage	V_{IL}	LVTTL, V_{DD}=Min.	—	—	0.8	V
Positive trigger voltage	V_{T+}	LVTTL Schmidt	1.1	—	2.4	V
Positive trigger voltage	V_{T-}	LVTTL Schmidt	0.6	—	1.8	V
Hysteresis voltage	V_H	LVTTL Schmidt	0.1	—	—	V

(3) Input pull-down characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Pull-down resistance	R_{PD}	V_I=V_{DD}	20	50	100	KΩ

(4) Input pull-up characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Pull-up resistance	R_{PU}	V_I=0V	20	50	100	KΩ

(5) Output characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH}	V_{DD}=Min., I_{OH}=-6mA	V_{DD}-0.4	—	—	V
Low-level output voltage	V_{OL}	V_{DD}=Min., I_{OL}=6mA	—	—	0.4	V

(6) RSDS-RX characteristics

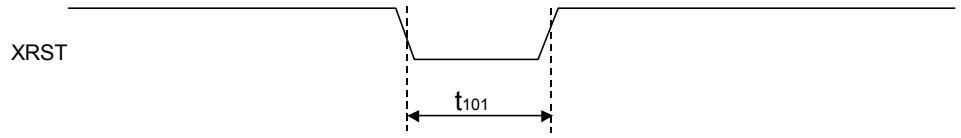
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Terminating resistor	R_{trm}	RXV_{DD}=3.3V	99	100	101	Ω
Differential input voltage	V_{id}	RXV_{DD}=3.3V	140	200	280	|mV|
Input common mode voltage	V_{os}	RXV_{DD}=3.3V	1.1	1.3	1.5	V

(7) LVDS-TX characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Differential output voltage	V_{od}	TXV_{DD}=3.3V	250	325	450	|mV|
Output common mode voltage	V_{os}	TXV_{DD}=3.3V	1.10	1.25	1.40	V

8.4 AC Characteristics

8.4.1 System reset

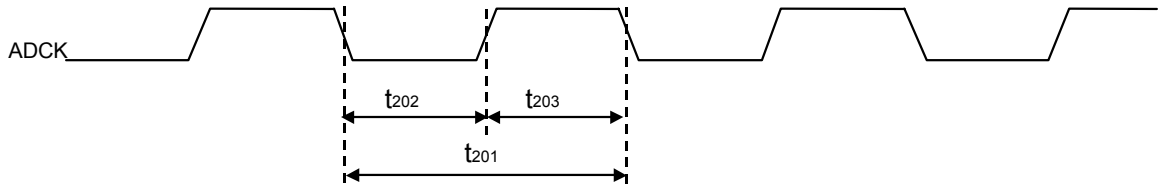


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{101}	XRST low-level pulse width	10	—	—	ms

* To avoid an operation error, the XRST signal entered must have a pulse width longer than the above minimum value.

8.4.2 Clock Timing

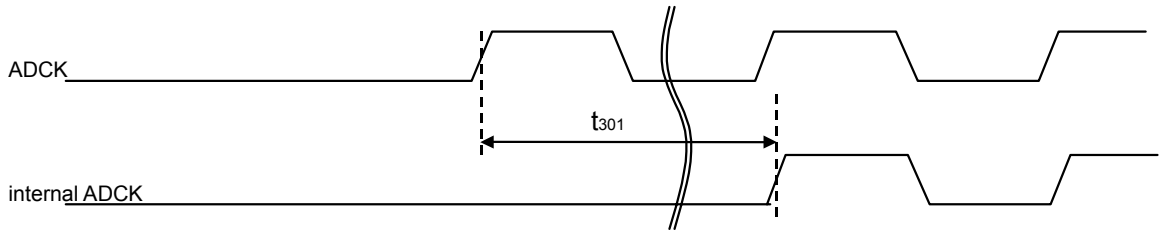


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{201}	ADCK cycle	-100ppm	1/(1 to 40M)	+100ppm	s
t_{202}	ADCK low-level pulse width	10.0	—	—	ns
t_{203}	ADCK high-level pulse width	10.0	—	—	ns

* t_{201} is the cycle of ADCK pin input clock.

8.4.3 Operation Timing of Input Clock Waveform Shaper Function

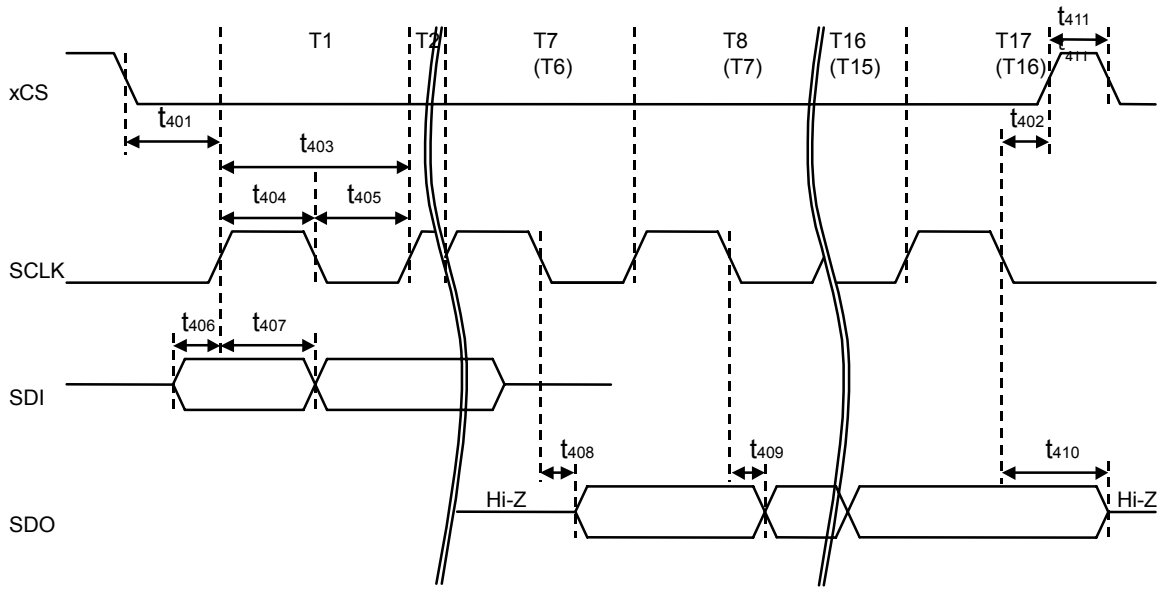


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{301}	Lock time	10	—	—	ms

8.4.4 Serial Interface Timing

"Txx" is valid in 16-cycle operation.

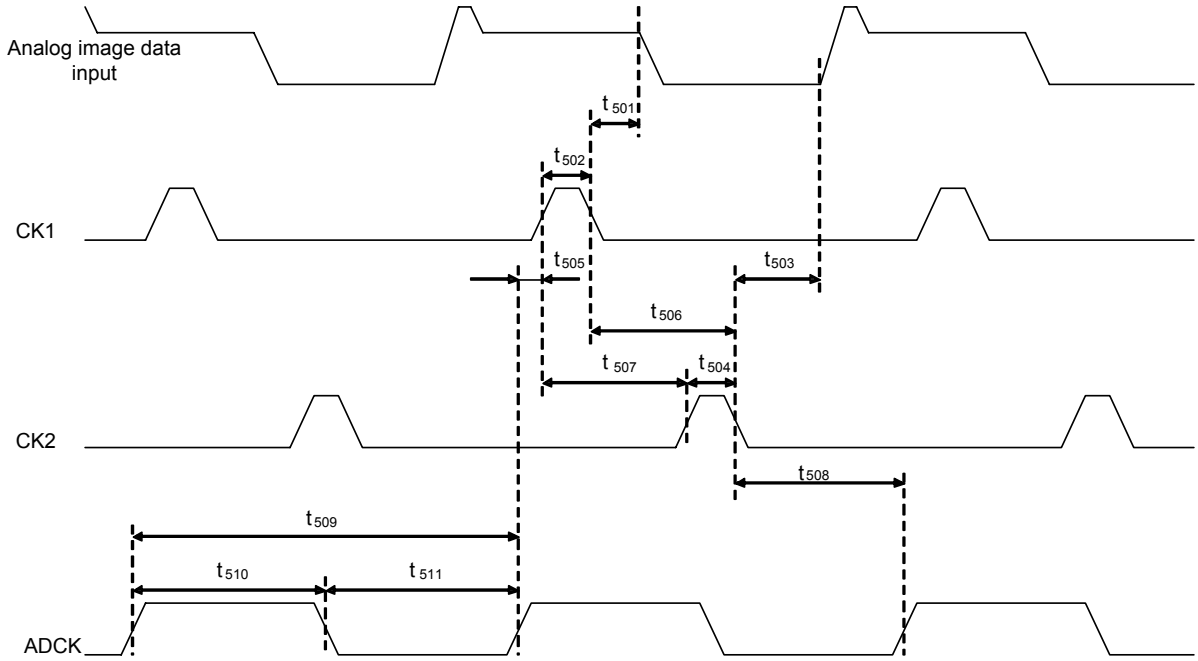


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{401}	Serial interface access start setup time	100	—	—	ns
t_{402}	Serial interface access end hold time	10	—	—	ns
t_{403}	SCLK cycle	100	—	—	ns
t_{404}	SCLK high-level pulse width	40	—	—	ns
t_{405}	SCLK low-level pulse width	40	—	—	ns
t_{406}	SDI setup time	20	—	—	ns
t_{407}	SDI hold time	20	—	—	ns
t_{408}	SDO read delay time	5	—	—	ns
t_{409}	SDO switching delay time	—	—	20	ns
t_{410}	SDO holding time	—	—	20	ns
t_{411}	Serial interface access cycle wait time	100	—	—	ns

* t_{403} is the cycle of SCLK pin input clock.

8.4.5 CDS Mode Sampling Timing

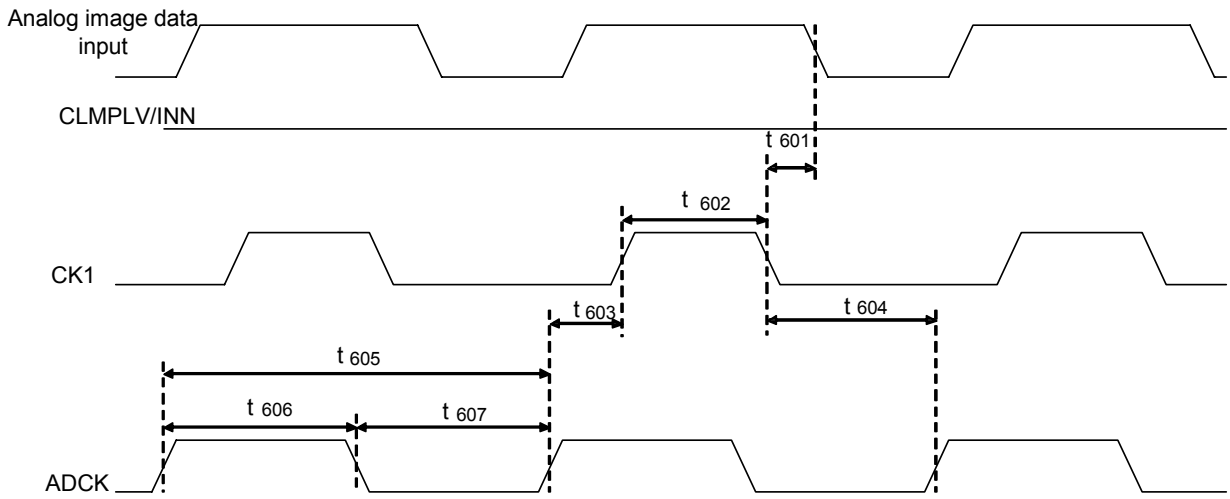


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{501}	CK1 hold time	—	7.0	—	ns
t_{502}	CK1 high-level pulse width	6.0	—	—	ns
t_{503}	CK2 sampling time	—	7.0	—	ns
t_{504}	CK2 high-level pulse width	6.0	—	—	ns
t_{505}	ADCK rise → CK1 rise time	2.0	—	—	ns
t_{506}	CK1 fall → CK2 fall time	0	—	—	ns
t_{507}	CK2 rise → CK2 rise time	0	—	—	ns
t_{508}	Ck2 fall → ADCK rise time	10.0	—	—	ns
t_{509}	ADCK cycle	25.0	—	—	ns
t_{511}	ADCK high-level pulse width	10.0	—	—	ns
t_{512}	ADCK low-level pulse width	10.0	—	—	ns

* The timing must be adjusted more closely by referring to the above timing chart so that the best quality of images can be obtained.

8.4.6 S/H Mode (Differential Voltage Input) Sampling Timing

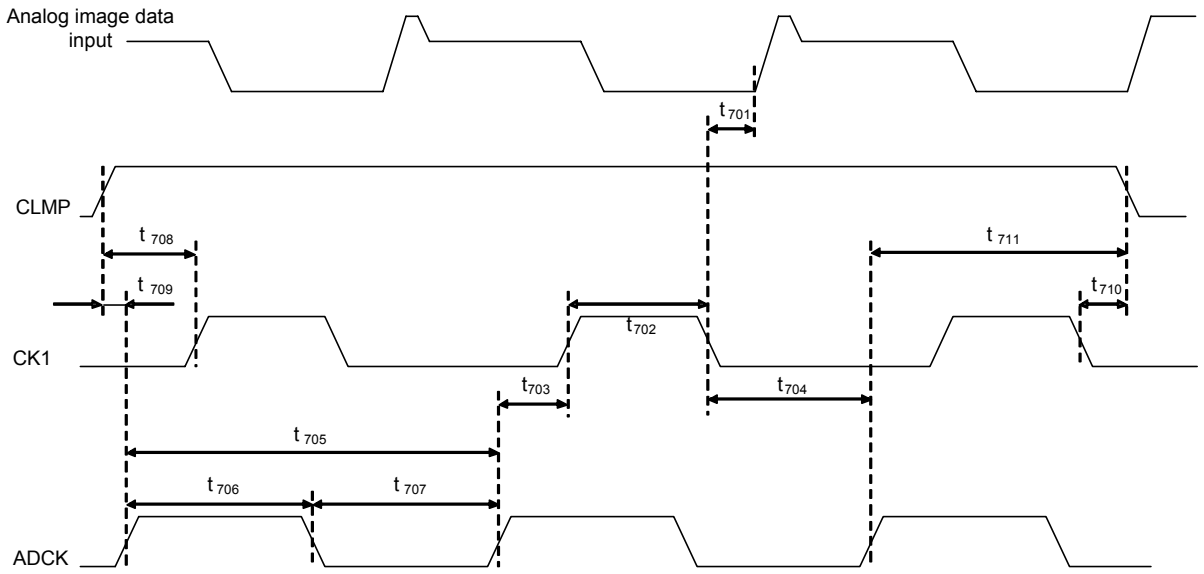


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{601}	CK1 hold time	—	7.0	—	ns
t_{602}	CK1 high-level pulse width	6.0	—	—	ns
t_{603}	ADCK rise → CK1 rise time	2.0	—	—	ns
t_{604}	CK1 fall → ADCK rise time	10.0	—	—	ns
t_{605}	ADCK cycle	25.0	—	—	ns
t_{606}	ADCK high-level pulse width	10.0	—	—	ns
t_{607}	ADCK low-level pulse width	10.0	—	—	ns

* The timing must be adjusted more closely by referring to the above timing chart so that the best quality of images can be obtained.

8.4.7 S/H Mode (Line Clamp) Sampling Timing

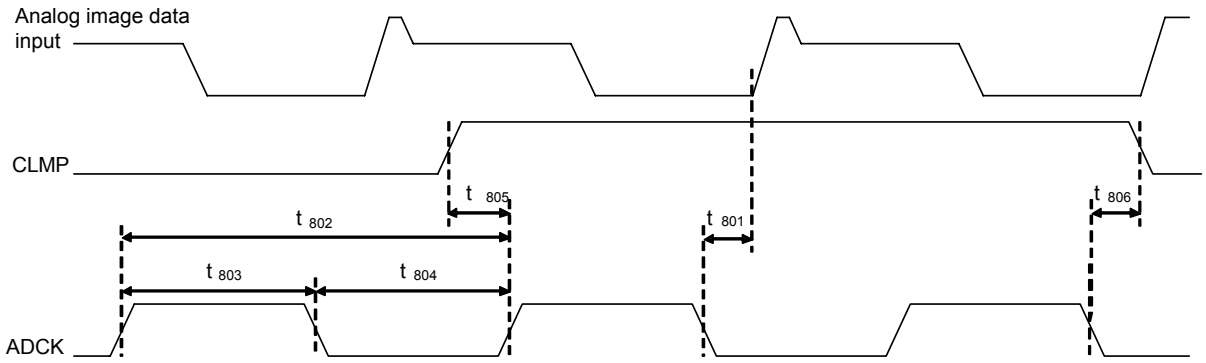


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{701}	CK1 hold time	—	7.0	—	ns
t_{702}	CK1 high-level pulse width	6.0	—	—	ns
t_{703}	ADCK rise → CK1 rise time	0	—	—	ns
t_{704}	CK1 fall → ADCK rise time	10.0	—	—	ns
t_{705}	ADCK cycle	25.0	—	—	ns
t_{706}	ADCK high-level pulse width	10.0	—	—	ns
t_{707}	ADCK low-level pulse width	10.0	—	—	ns
t_{708}	CLMP rise → CK1 rise time	1.0	—	—	ns
t_{709}	CLMP rise → ADCK rise time	5.0	—	—	ns
t_{710}	CK1 fall → CLMP fall time	1.0	—	—	ns
t_{711}	CLMP rise → ADCK rise time	5.0	—	—	ns

* The timing must be adjusted more closely by referring to the above timing chart so that the best quality of images can be obtained.

8.4.8 S/H Mode Sampling Timing (during Automatic Sampling Clock Generation)

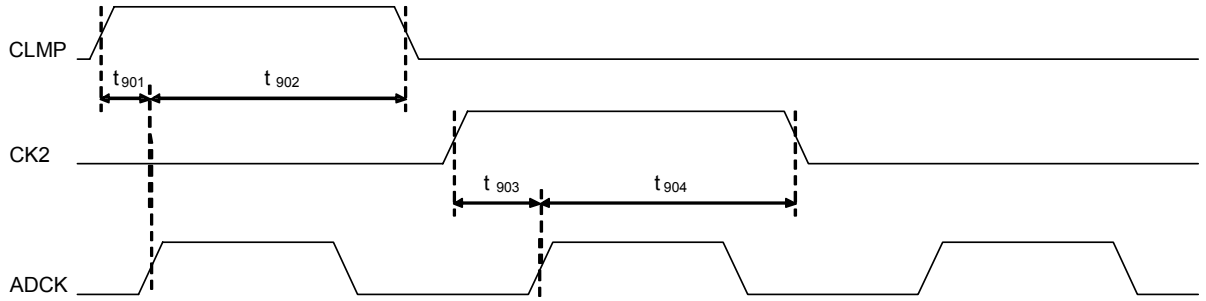


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{801}	ADCK hold time	—	7.0	—	ns
t_{802}	ADCK cycle	25.0	—	—	ns
t_{803}	ADCK high-level pulse width	10.0	—	—	ns
t_{804}	ADCK low-level pulse width	10.0	—	—	ns
t_{805}	CLMP rise → ADCK rise time	5.0	—	—	ns
t_{806}	ADCK fall → CLMP fall time	5.0	—	—	ns

* The timing must be adjusted more closely by referring to the above timing chart so that the best quality of images can be obtained.

8.4.9 Pixel Input Instruction Timing



Symbol	Item	Min.	Typ.	Max.	Unit
t_{901}	CLMP rise → ADCK rise time	5.0	—	—	ns
t_{902}	ADCK rise → CLMP fall time	5.0	—	—	ns
t_{903}	CK2 rise → ADCK rise time	5.0	—	—	ns
t_{904}	ADCK rise → CK2 fall time	5.0	—	—	ns

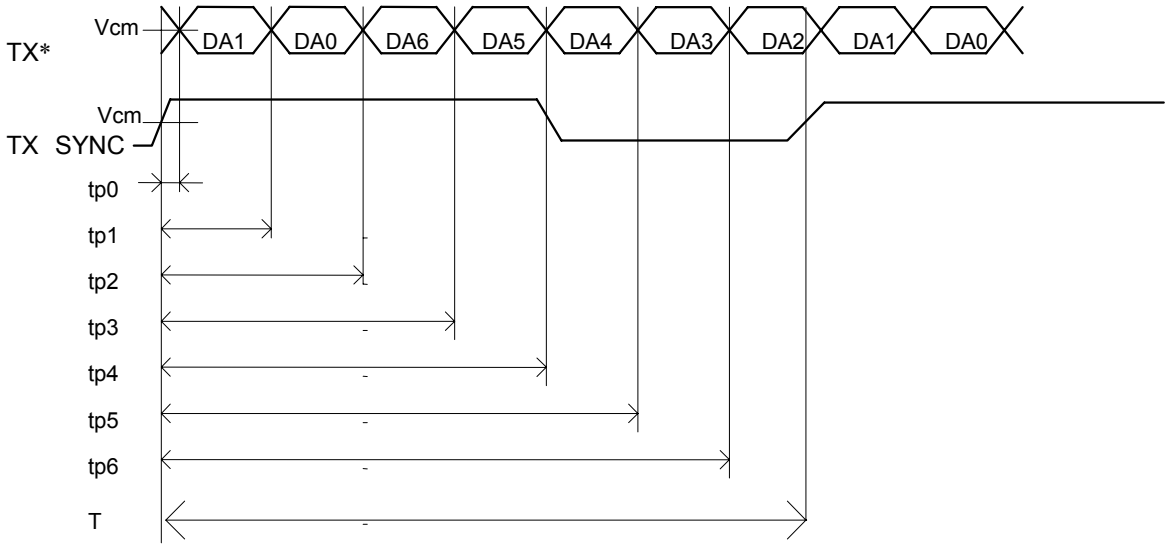
* The timing must be adjusted more closely by referring to the above timing chart so that the best quality of images can be obtained.

Above timings apply when CLMP signal and CK2 signal are used for specifying the black-based pixel input timing and black dummy pixel input timing, respectively.

CLMP: For specifying black-based pixel input timing

CK2: For specifying black dummy pixel input timing

8.4.10 LVDS Output Timing

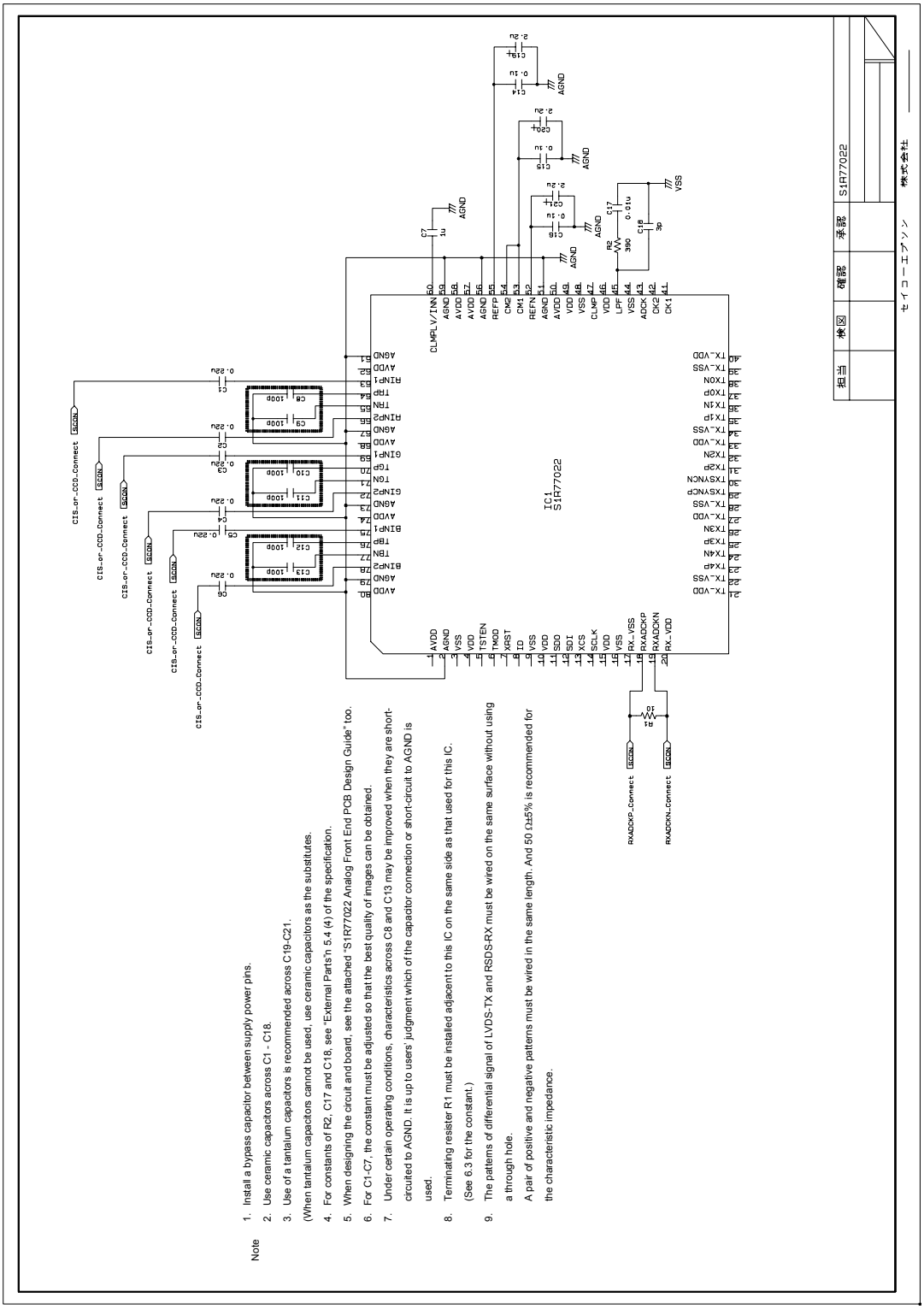


T=TXSYNC clock period

Item	Symbol	Conditions	min	typ	max	Unit
Pulse position at Bit-0	tp0	f=80 MHz (T=12.5 ns)	-0.25	0	0.25	ns
Pulse position at Bit-1	tp1		T/7-0.25	T/7	T/7+0.25	″
Pulse position at Bit-2	tp2		2*T/7-0.25	2*T/7	2*T/7+0.25	″
Pulse position at Bit-3	tp3		3*T/7-0.25	3*T/7	3*T/7+0.25	″
Pulse position at Bit-4	tp4		4*T/7-0.25	4*T/7	4*T/7+0.25	″
Pulse position at Bit-5	tp5		5*T/7-0.25	5*T/7	5*T/7+0.25	″
Pulse position at Bit-6	tp6		6*T/7-0.25	6*T/7	6*T/7+0.25	″
Power Down delay	tpd	Output goes HiZ from PDLVDS=0			100	ns

9. APPLICATION CONNECTION EXAMPLES

(TBD)



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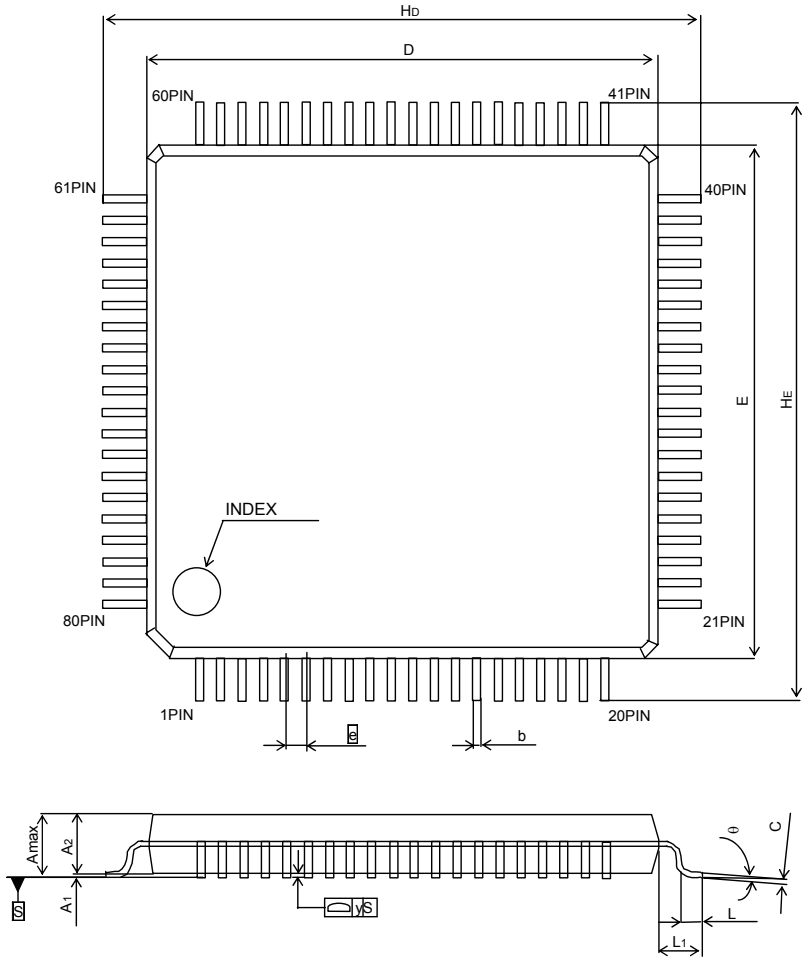
10. EXTERNAL DIMENSIONS

QFP14-80 Package



Symbol	Dimension in Millimters		
	Min.	Nom.	Max.
E	—	12	—
D	—	12	—
Amax	—	—	1.7
A1	—	0.1	—
A2	—	1.4	—
e	—	0.5	—
b	0.13	—	0.27
c	0.09	—	0.2
Θ	0°	—	10°
L	0.3	—	0.75
L1	—	1	—
HE	—	14	—
HD	—	14	—
y	—	—	0.08

1=1mm

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