EPSON
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RSDS Transmitter / Receiver

S1R77081 Series
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.1

NOTICE

Table of Contents

1. OVERVIEW

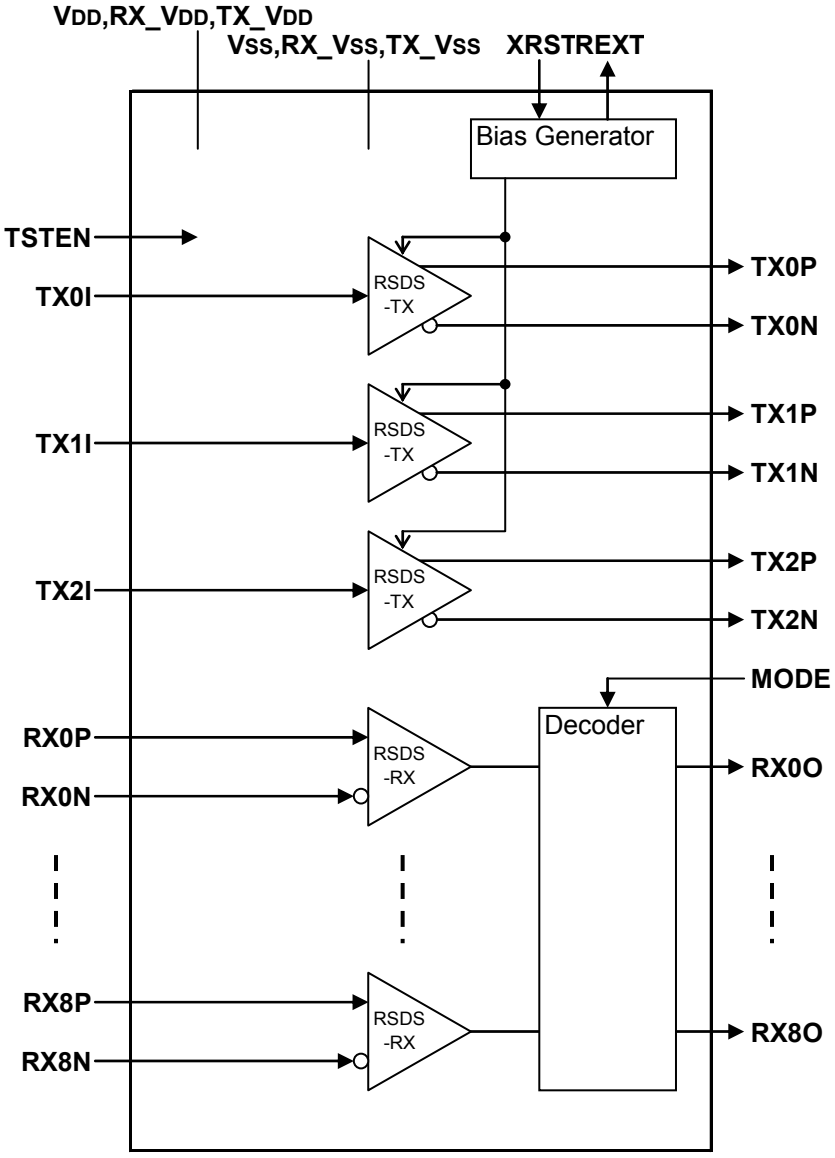
The IC stipulated herein is the RSDS transmitter/receiver IC. When used in combination with an analog front-end incorporating a CCD drive clock, the IC helps facilitate the realization of a high-speed scanner system with superior EMI characteristics.

2. FEATURES

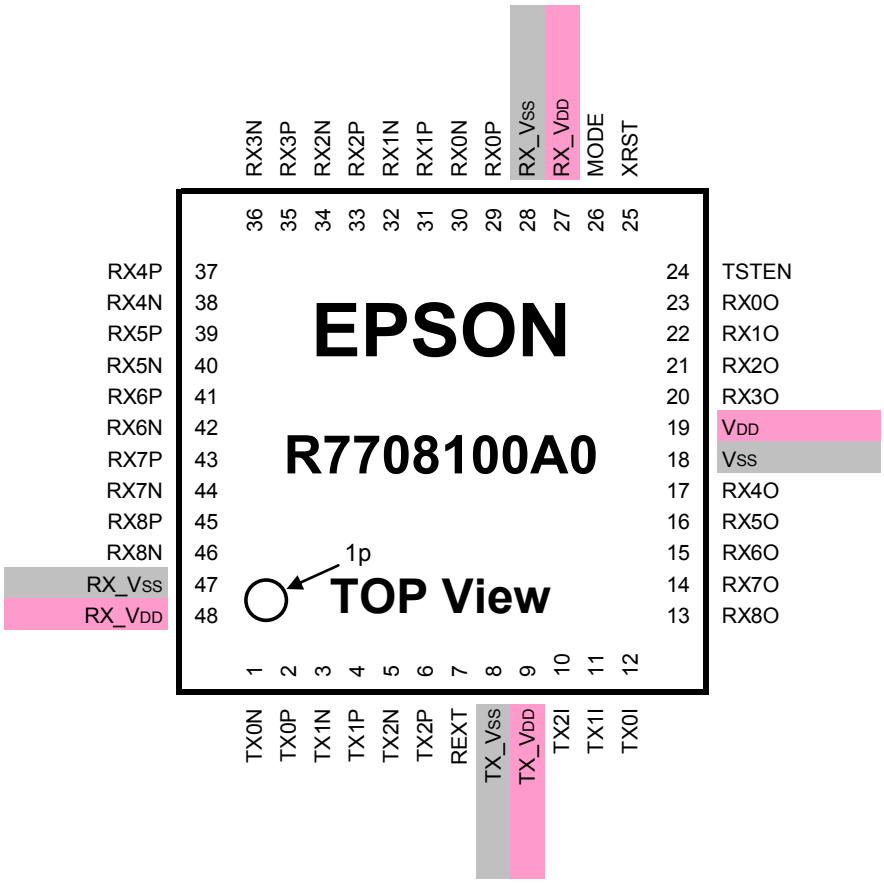
- 0.5-mm pitch, 48-pin QFP package
- 3.3 V single power supply
- Transmit channel × 3
- Receive channel × 9
- Output current adjustable by an external resistor
- Maximum transfer rate 100Mbps (per 1-channel)

* This product is not designed to resist radiation.

3. BLOCK DIAGRAM



4. PIN LAYOUT DIAGRAM



5. PIN DESCRIPTION

No.	pin	Pin Name	I/O	Reset	Pin Function	Remark	Drive Capacity
Differential input/output							
1	2	TX0P	A	—	Transmit data (differential output)		Analog
2	1	TX0N	A	—			
3	4	TX1P	A	—			
4	3	TX1N	A	—			
5	6	TX2P	A	—			
6	5	TX2N	A	—			
7	29	RX0P	A	—	Received data (differential input)		Analog
8	30	RX0N	A	—			
9	31	RX1P	A	—			
10	32	RX1N	A	—			
11	33	RX2P	A	—			
12	34	RX2N	A	—			
13	35	RX3P	A	—			
14	36	RX3N	A	—			
15	37	RX4P	A	—			
16	38	RX4N	A	—			
17	39	RX5P	A	—			
18	40	RX5N	A	—			
19	41	RX6P	A	—			
20	42	RX6N	A	—			
21	43	RX7P	A	—			
22	44	RX7N	A	—			
23	45	RX8P	A	—			
24	46	RX8N	A	—			
25	7	REXT	A	—	Connects the external resistor used to adjust output current		Analog
Digital input/output							
26	12	TX0I	I	—	Transmit data (digital input)	PD	—
27	11	TX1I	I	—		PD	—
28	10	TX2I	I	—		PD	—
29	23	RX0O	O	Lo	Received data (digital input)		2mA
30	22	RX1O	O	Lo			
31	21	RX2O	O	Lo			
32	20	RX3O	O	Lo			
33	17	RX4O	O	Lo			
34	16	RX5O	O	Lo			
35	15	RX6O	O	Lo			
36	14	RX7O	O	Lo			
37	13	RX8O	O	Lo			
Test pins and system signals							
38	24	TSTEN	I	—	Test pin (normally fixed low)	PD	—
39	25	XRST	I	—	Reset signal	SMT, PD	—
40	26	MODE	I	—	Mode select	PD	—
Power supply pins							
41	19	V_{DD}	P	—	3.3 V power supply pin		—
42	9	TX_V_{DD}	P	—	RSDS-TX power supply pin (3.3 V)		—
43	27	RX_V_{DD}	P	—	RSDS-RX power supply pin (3.3 V)		—
44	48	RX_V_{DD}	P	—			
45	18	V_{SS}	P	—	Ground		—
46	8	TX_V_{SS}	P	—	RSDS-TX ground		—
47	28	RX_V_{SS}	P	—	RSDS-RX ground		—
48	47	RX_V_{SS}	P	—			

I/O column legend:
- A: Analog pin
- I: Input pin
- O: Output pin
- P: Power supply pin

Reset (initial state) column legend:
- HI-Z: Hi-Z: High-impedance state
- Lo: LOW output

Remark column legend:
- PD: Pulldown
- SMT: Schmitt

6. FUNCTIONAL DESCRIPTION

This section describes the function of each block.

6.1 RSDS

The IC is comprised of 3 transmit channels and 9 receive channels.
Fig.6.1 shows the pin connections of the IC in the periphery of the RSDS unit.

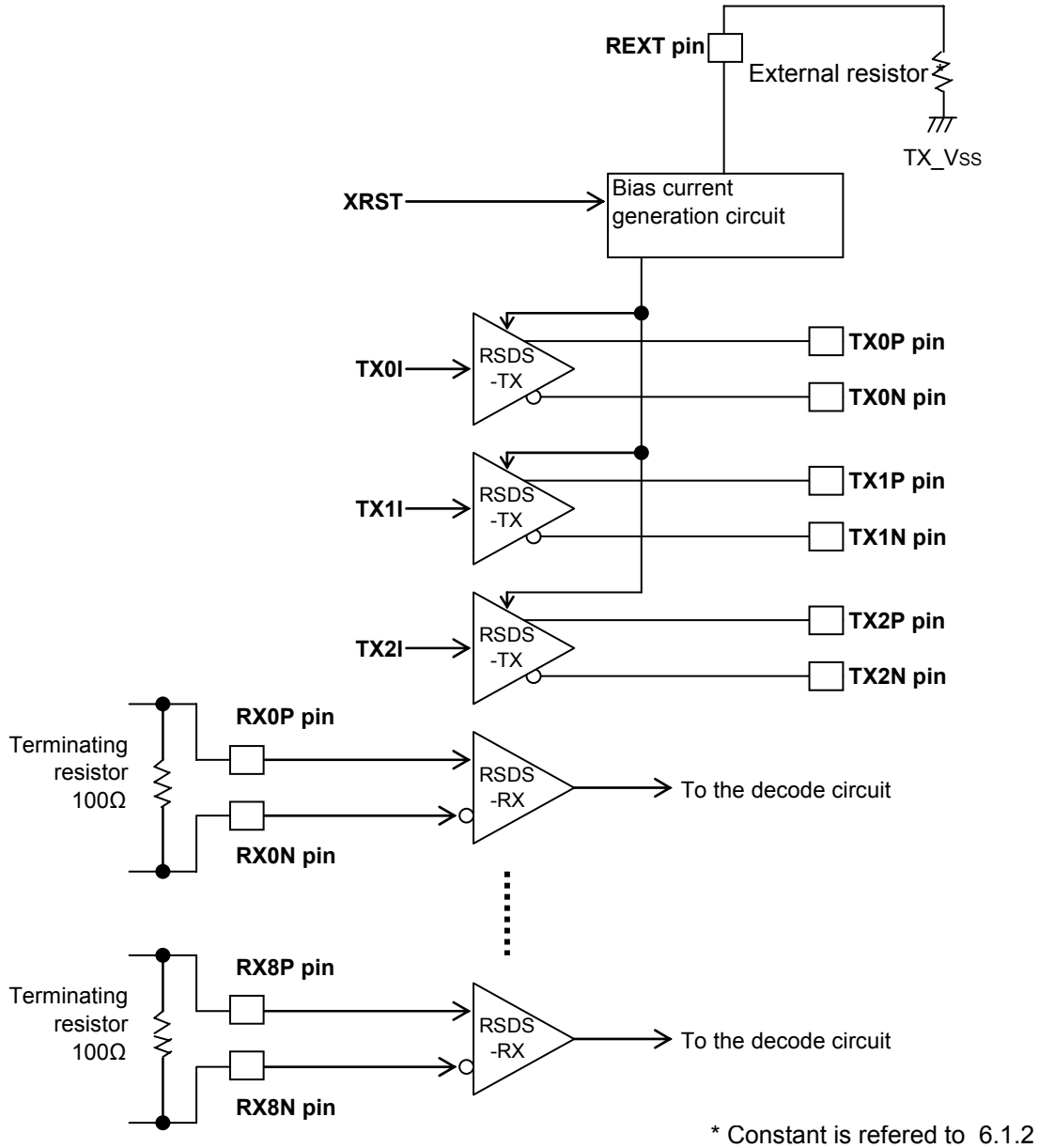


Fig.6.1 RSDS connection diagram

6.1.1 Power-down Function

The transmit channels each have a power-down function, which can be controlled by the XRST pin. Pulling the XRST pin low shifts the transmit channel into power-down mode, causing it to stop sending data. Conversely, driving the XRST pin high shifts the transmit channel out of power-down mode, allowing it to start sending data. The transmit channel requires 10 ms at maximum before it can safely send data after exiting power-down mode.

6.1.2 Bias Current Generation Function

The output current of the transmit channel is controlled by the IC's built-in bias current generation function. Furthermore, the output current of the transmit channel can be adjusted by an external resistor connected to the REXT pin.

Table 6.1 Transmit Channel Output Current Characteristics

External resistor constant	Min.	Typ.	Max.
26 KΩ	0.7 mA	1.0 mA	1.4 mA
13 KΩ	1.4 mA	2.0 mA	2.8 mA
6.5 KΩ	2.8 mA	4.0 mA	5.6 mA
4.3 KΩ	4.0 mA	6.0 mA	8.0 mA

CAUTION:
It is recommended that external resistor is common difference under ±1.0%.

6.1.3 Terminating Resistor

Connect a 100 Ω terminating resistor to the nearest vicinity of external pin of each receive channel.
Also make sure the transmit channel too is terminated with 100Ω at the input pin of the receive device as close to it as possible.

CAUTION:
It is recommended that terminating resistor is common difference under ±1.0%.
In mounting on board, mount it without through-hold to the same face with this IC.

6.1.4 Processing of Free Pins

(1) Transmit channels
If any transmit channel is not used, fix the digital input (TXnI) of the channel either low or high. On the other hand, leave the differential output (TXnP/N) of the channel open.

(2) Receive channels
Although the receive channels each have an internal pulldown resistor, the digital output (RXn0) of an unused receive channel is indeterminate. Therefore, fix the polarities of differential input (RXnP/n) of the channel to the opposite phases so that the digital output of the channel will always be high or low. For example, if the positive polarity (RXnP pin) is fixed low and the negative polarity (RXnN pin) is fixed high, the digital output (RXn0) will always be low.
On the other hand, leave the digital output (RXn0) of the channel open.

6.2 Decode Function Unit

Depending on the MODE pin state, the received data can be decoded before being output. If the MODE pin is fixed low, the received differential data is output 1 for 1 in digital. Conversely, if the MODE pin is fixed high, the decode function is enabled.

The decode function has two selectable modes that can be switched by receive channel pins according to the purpose of use. Table 6.2 shows the relationship between external pin settings and the selected decode mode.

Table 6.2 External Pin Settings and Decode Modes

Decode mode	External pin									
	MODE	RX8P/N	RX7P/N	RX6P/N	RX5P/N	RX4P/N	RX3P/N	RX2P/N	RX1P/N	RX0P/N
Normal operation (1 to 1 reception)	Low	D	D	D	D	D	D	D	D	D
4-channel mode	High	C	D	D	D	D	0	0	0	0
2-channel mode	High	C	D	D	0	X	X	Other than "000"		

0: Fix RXnP and RXnN low and high, respectively.
1: Fix RXnP and RXnN high and low, respectively.
X: Set to 0 or 1.
C: Sync clock receive channel
D: Data receive channel

Table 6.3 shows the relationship of receive channel input/output pins corresponding to decode modes.

Table 6.3 Receive Channel Input/Output

External pin	Differential input pin									Digital output								
MODE	RX8P/N	RX7P/N	RX6P/N	RX5P/N	RX4P/N	RX3P/N	RX2P/N	RX1P/N	RX0P/N	RX8O	RX7O	RX6O	RX5O	RX4O	RX3O	RX2O	RX1O	RX0O
Low	D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0
High	↑	D7	D6	D5	D4	0	0	0	0	H	D7	D6	D5	D4	D3	D2	D1	D0
	↓	D3	D2	D1	D0	0	0	0	0	L								
	↑	DH	DL	0	0	0	SYNCNUM[2:0] Other than "000" *			H	D15	D14	D13	D12	D11	D10	D9	D8
	↓	DH	DL	0		/1				/L	/D7	/D6	/D5	/D4	/D3	/D2	/D1	/D0
	↓	DH	DL	0	1	0				H	D15	D14	D13	D12	D11	D10	D9	D8
	↑	DH	DL	0		/1				/L	/D7	/D6	/D5	/D4	/D3	/D2	/D1	/D0

0: Fix RXnP and RXnN low and high, respectively.
1: Fix RXnP and RXnN high and low, respectively.
DH: Data receive (D15 to 8)
DL: Data receive (D7 to 0)
* Refer to Section 6.2.3.

6.2.1 Normal Operation (1 to 1 Reception)

Fig.6.2 shows a timing example during normal operation (1 to 1 reception).

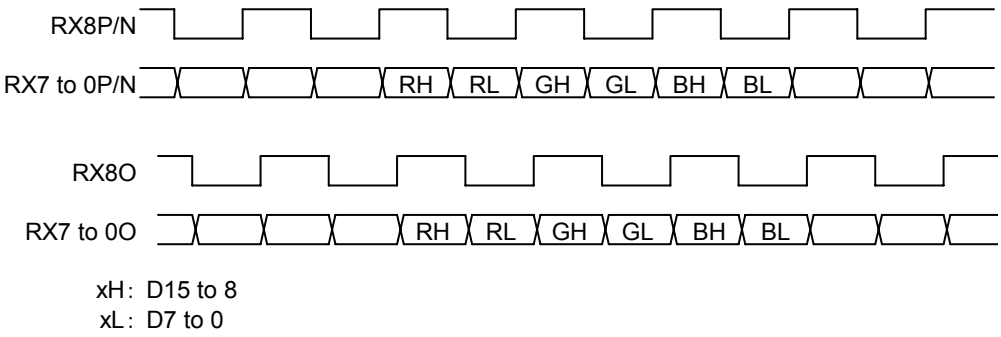


Fig.6.2 Timing Example of Normal Operation

6.2.2 4-channel Mode

In 4-channel mode, input at the RX8P/N pin is the sync clock and the received data fed into the RX7–4P/N pins are latched on both rising and falling edges of the sync clock. The received data latched on the rising edge of the sync clock comprises the 4 high-order bits, and the received data latched on the falling edge of the sync clock comprises the 4 low-order bits, which are forwarded together to the RX7-0O pins. The sync clock for the output data is forwarded as digital output to the RX8O pin.

Fig.6.3 shows an operation example of the decode function whose decode mode is set to 4-channel mode.

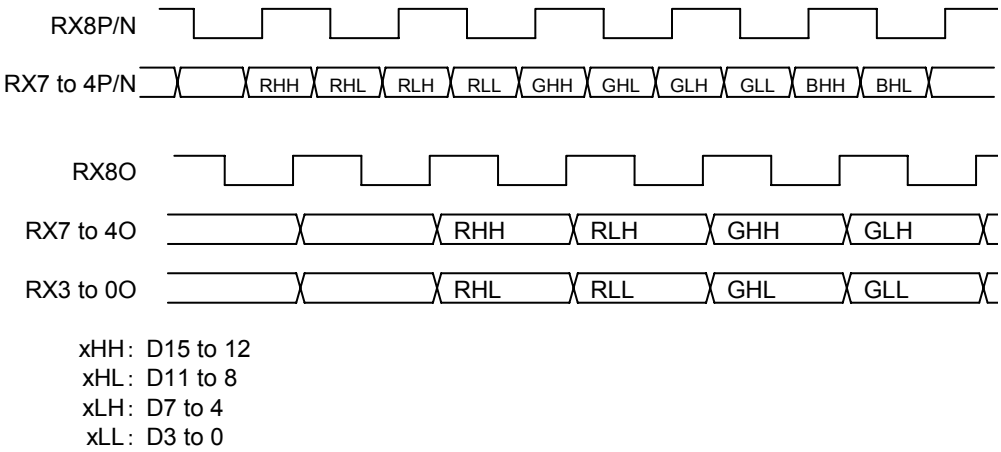
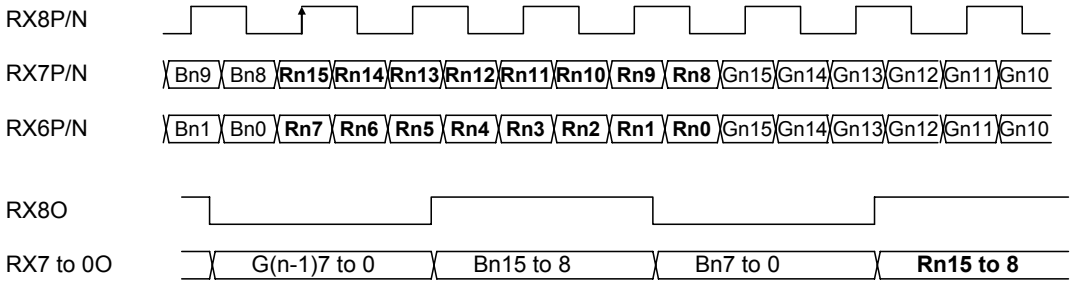


Fig.6.3 Example of an operation timing in 4-channel mode

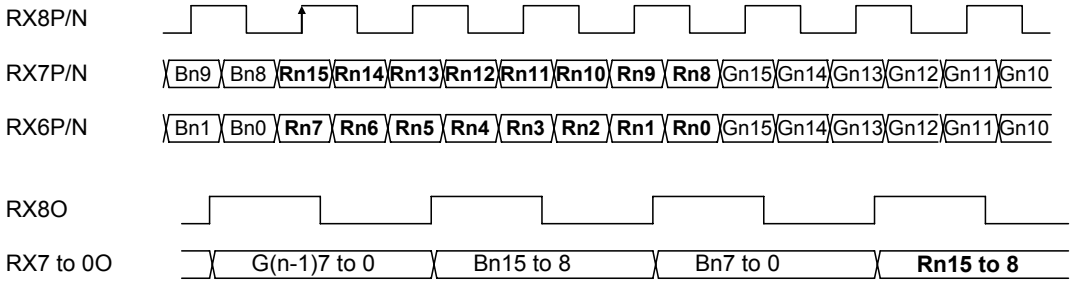
6.2.3 2-channel Mode

In 2-channel mode, input at the RX8P/N pin is the sync clock and the received data fed into the RX7–6P/N pins are latched on both rising and falling edges of the sync clock. The 16 bits of received data that are fed in on two channels are aligned after being latched and then forwarded in 8-bit units as digital output in order of the high and the low bytes. At this time, the digital output is delayed by a finite time equal to 1 sync clock cycle before being output. Furthermore, the RX3P/N and RX4P/N pins, depending on their set state, change the active edge of the received sync clock and the output cycle of the output sync clock. Fig.6.4 shows an operation example of the decode function whose decode mode is set to 2-channel mode.

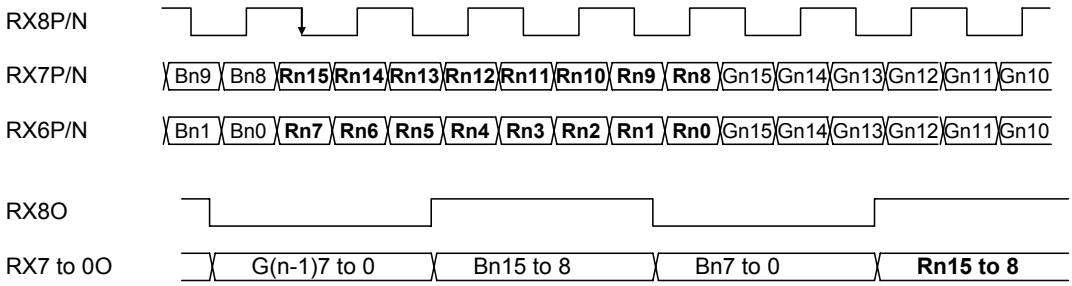
■ Latched on positive sync clock edge, output sync clock word output (RX4P/N = "0", RX3P/N = "0")



■ Latched on positive sync clock edge, output sync clock byte output (RX4P/N = "0", RX3P/N = "1")



■ Latched on negative sync clock edge, output sync clock word output (RX4P/N = "1", RX3P/N = "0")



■ Latched on negative sync clock edge, output sync clock byte output (RX4P/N = "1", RX3P/N = "1")

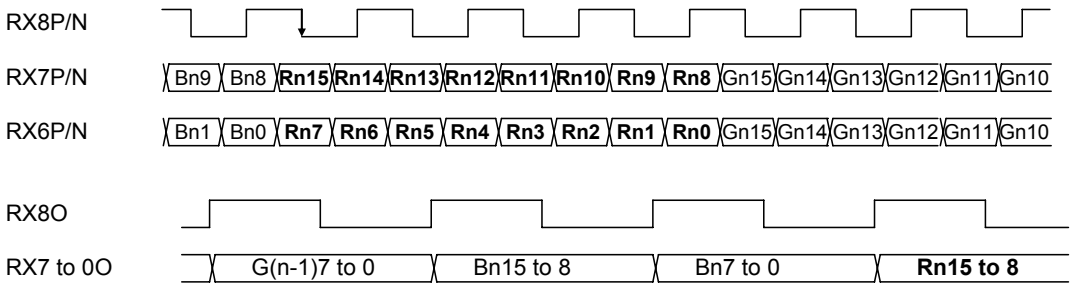


Fig.6.4 Example of an operation timing in 2-channel mode

In 2-channel mode, furthermore, since the received data needs to be aligned, the decode block has a facility to detect the first bit of the 16-bit received data. More specifically, the first bit is detected by means of the fixed data (0xA15E) that is successively received every 2 words. The two words received between the fixed data are not the objects to be detected and can therefore be an indeterminate value. The number of occurrences of the fixed data necessary to detect the first bit is determined by the code that is set on the RX2-0P/N pins (SYNCNUM[2:0]), i.e., the set value + 1 determines the number of occurrences. This is illustrated by operation examples in Fig.6.5.

CAUTION:

In first bit detect function, detect by means of the fix data that is successively received. If input data is the same as the fixed data accidentally, it detects the first bit in the wrong. Accordingly, it is recommended that SYNCNUM[2:0] is set to over 5 (“101”) to lower the probability of wrong detection.

In the case that SYNCNUM[2:0] is 5, there is the possibility that detects the first bit in the wrong at probability of about 1 time in 124 years. (CCD clock: 3.3MHz, Operating rate: 2.4 hour /day)

■ When SYNCNUM = 001

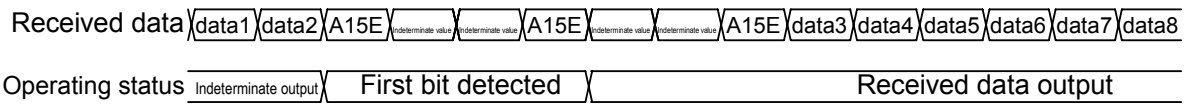


Fig.6.5 Operation example for first bit detection in 2-channel mode

CAUTION:

If the IC is used in 2-channel mode in combination with the S1R77013, be sure to use the “image data fixed value output setting” of the S1R77013. Resistor setting of S1R77013 is as follows.

CCAEMODE resistor (No.0x68) INDEX bit: “1”
TESTMODE resistor (No.0x77) ADTD_DT[7:0] bit: “0xA1”
AFEMODE resistor (No.0x7E) SIMGOUTADJ[1:0] bit: “10”

In pulse length of shift-pulse-trigger signal (TGCK signal) that inputs from external to S1R77013, make necessary time to detect the first bit.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 to +4.0	V
	TXV_{DD} *	-0.3 to +4.0	V
	RXV_{DD} *	-0.3 to +4.0	V
Input voltage	V_I	-0.3 to V_{DD}+0.5	V
	RXV_I	-0.3 to RXV_{DD}+0.5	V
Output voltage	V_O	-0.3 to V_{DD}+0.5	V
	TXV_O	-0.3 to TXV_{DD}+0.5	V
Output current per pin	I_{OUT}	±30	mA
Storage temperature	T_{stg}	-65 to +150	°C

* TXV_{DD}=RXV_{DD}(In mounting on board, supply from the same power supply) V_{SS}=0V, TXV_{SS}=0V, RXV_{SS}=0V

7.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.135	3.300	3.465	V
	TXV_{DD}	3.135	3.300	3.465	V
	RXV_{DD}	3.135	3.300	3.465	V
Input voltage	V_I	V_{SS}	—	V_{DD}	V
	RXV_I	RXV_{SS}	—	RXV_{DD}	V
Ambient temperature	Ta	0	25	70	°C
Input rise (normal input)	t_{ri} *	—	—	50	ns
Input fall (normal output)	t_{fa} *	—	—	50	ns
Input rise (Schmitt input)	t_{ri} *	—	—	5	ms
Input fall (Schmitt input)	t_{fa} *	—	—	5	ms

* Indicates the 10% to 90% change time of V_{DD}. V_{SS}=0V, TXV_{SS}=0V, RXV_{SS}=0V

7.3 DC Characteristics

(1) Input/output characteristics in the DC state

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Quiescent current	I_{DDS}	V_{DD}=3.3V±5%	—	—	10	μA
Current consumption	I_{DD} *	V_{DD}=3.3V±5%	—	—	32	mA
	RSI_{DD} *	TXV_{DD}=RXV_{DD}=3.3V±5%	—	—	46	mA
Input leakage current	I_{LI}	V_{DD}=3.3V, V_{IH}=V_{DD},V_{IL}=V_{SS}	-5	—	5	μA
Off-state leakage current	I_{OZ}	—	-5	—	5	μA

* When external pins are nonloaded

(2) Input characteristics

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	LVTTL,V_{DD}=Max	2.0	—	—	V
Low level input voltage	V_{IL}	LVTTL,V_{DD}=Min	—	—	0.8	V
Positive trigger voltage	V_{T+}	LVTTL Schmitt	1.1	—	2.4	V
Negative trigger voltage	V_{T-}	LVTTL Schmitt	0.6	—	1.8	V
Hysteresis voltage	V_H	LVTTL Schmitt	0.1	—	—	V

(3) Input pulldown characteristics

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Pulldown resistance value	R_{PD}	V_I=V_{DD}	20	50	100	KΩ

(4) Output characteristics

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	V_{DD}=Min,I_{OH}=-6mA	V_{DD}-0.4	—	—	V
Low level output voltage	V_{OL}	V_{DD}=Min,I_{OL}=6mA	—	—	0.4	V

(5) RSDS-RX characteristics

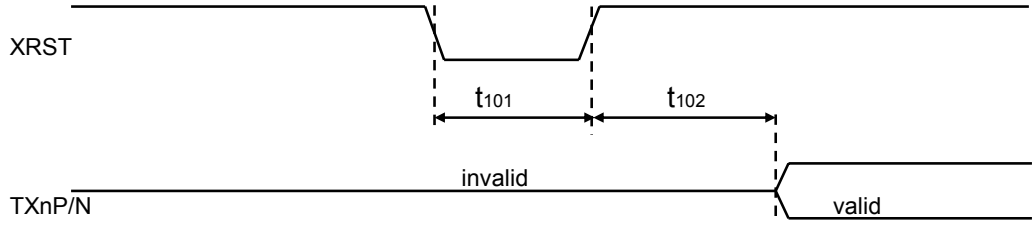
Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Terminating resistance	R_{trm}	RXV_{DD}=3.3V	99	100	101	Ω
Differential input voltage	V_{id}	RXV_{DD}=3.3V	140	200	280	|mV|
Input common mode voltage	V_{os}	RXV_{DD}=3.3V	1.1	1.3	1.5	V

(6) RSDS-TX characteristics

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
External resistance	R_{ext}	TXV_{DD}=3.3V	4.3	13	30	KΩ
Differential output voltage	V_{od}	TXV_{DD}=3.3V,R_{ext}=13KΩ	140	200	280	|mV|
Output common mode voltage	V_{os}	TXV_{DD}=3.3V	1.1	1.3	1.5	V
Output current	I_{OH2}	TXV_{DD}=3.3V,R_{ext}=13KΩ	1.4	2.0	2.8	mA

7.4 AC Characteristics

7.4.1 System Reset

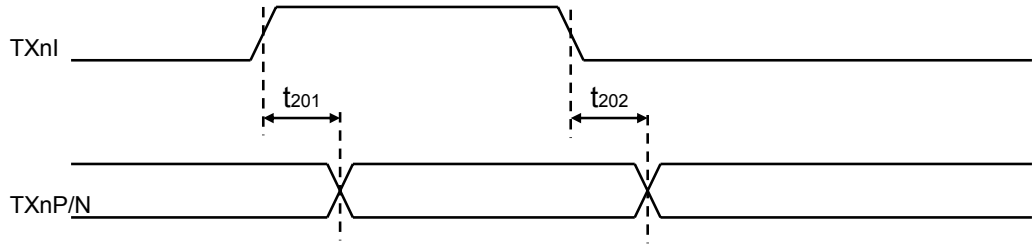


(Under recommended operating conditions)

Symbol	parameter	Min.	Typ.	Max.	Unit
t_{101}	XRST low level pulse width	10	—	—	ms
t_{102}	Transmit channel rise time	—	—	10	ms

* To ensure the IC will not operate erratically, make sure the XRST input signal is asserted for more than the above-rated minimum value.

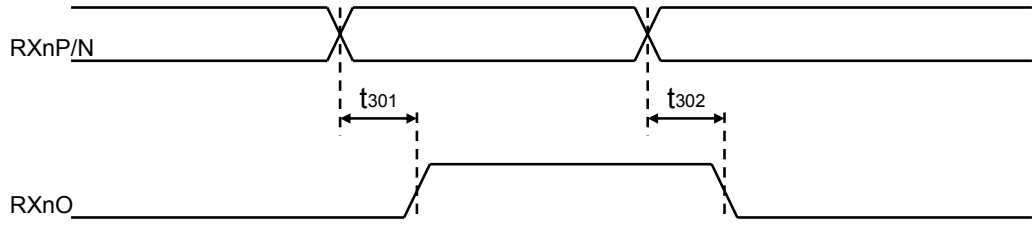
7.4.2 Transmit Channel Delay Time



(Under recommended operating conditions)

Symbol	parameter	Min.	Typ.	Max.	Unit
t_{201}	Transmit channel logic 0 to logic 1 delay time	1.5	2.8	6.0	ns
t_{202}	Transmit channel logic 1 to logic 0 delay time	1.5	2.8	6.0	ns

7.4.3 Receive Channel Delay Time

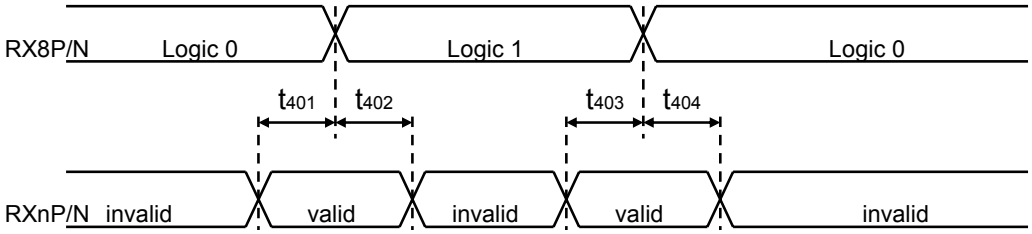


(Under recommended operating conditions)

Symbol	parameter	Min.	Typ.	Max.	Unit
t_{301}	Receive channel logic 0 to logic 1 delay time	1.5	2.8	6.0	ns
	Receive channel logic 0 to logic 1 delay time *	3.0	5.3	9.1	ns
t_{302}	Receive channel logic 1 to logic 0 delay time	1.5	2.8	6.0	ns
	Receive channel logic 1 to logic 0 delay time *	3.0	5.3	9.5	ns

* RX8P/N to RX8O delay time during 4-channel mode
RX8P/N to RX8O delay time during 2-channel mode (However, logic differs with operation setting.)

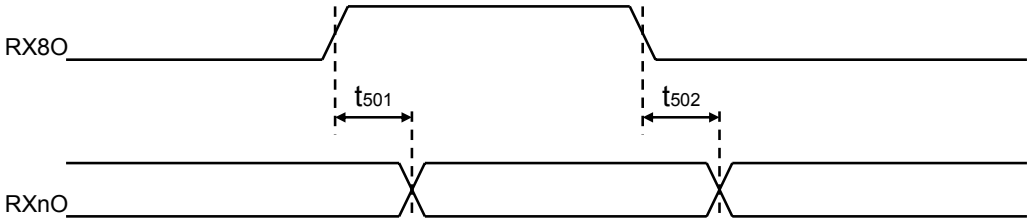
7.4.4 Receive Channel Decode Function Timing



(Under recommended operating conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{401}	Sync clock (RX8P/N) rise to RXnP/N setup time	1.5	—	—	ns
t_{402}	Sync clock (RX8P/N) rise to RXnP/N hold time	4.5	—	—	ns
t_{403}	Sync clock (RX8P/N) fall to RXnP/N setup time	1.5	—	—	ns
t_{404}	Sync clock (RX8P/N) fall to RXnP/N hold time	3.9	—	—	ns

7.4.5 4-channel Mode / 2-channel Mode Output Timing

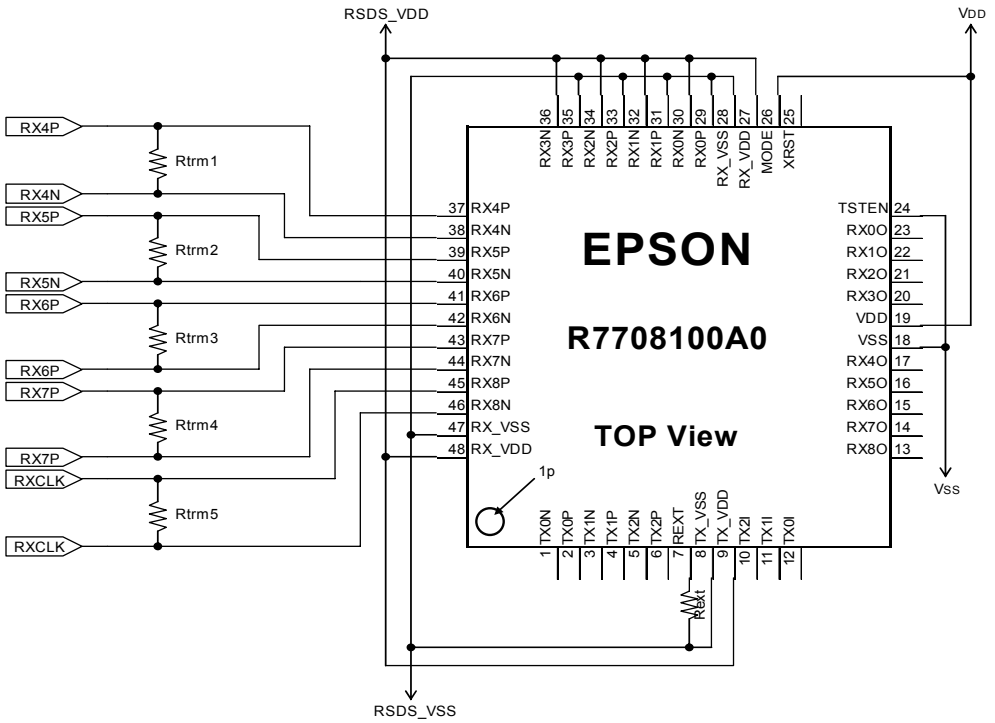


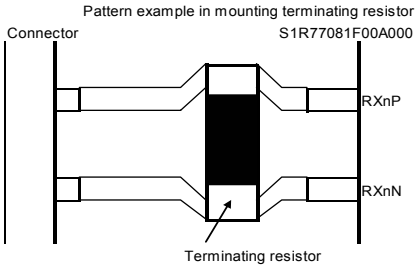
(Under recommended operating conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{501}	Output sync clock (RX8O) rise to RxnO output delay time	-2.0	—	2.0	ns
t_{502}	Output sync clock (RX8O) rise to RxnO output delay time *	-2.0	—	2.0	ns

* Applies for only 2-channel mode where the output sync clock is set to be output in words.

8. CONNECTION EXAMPLES FOR APPLICATION

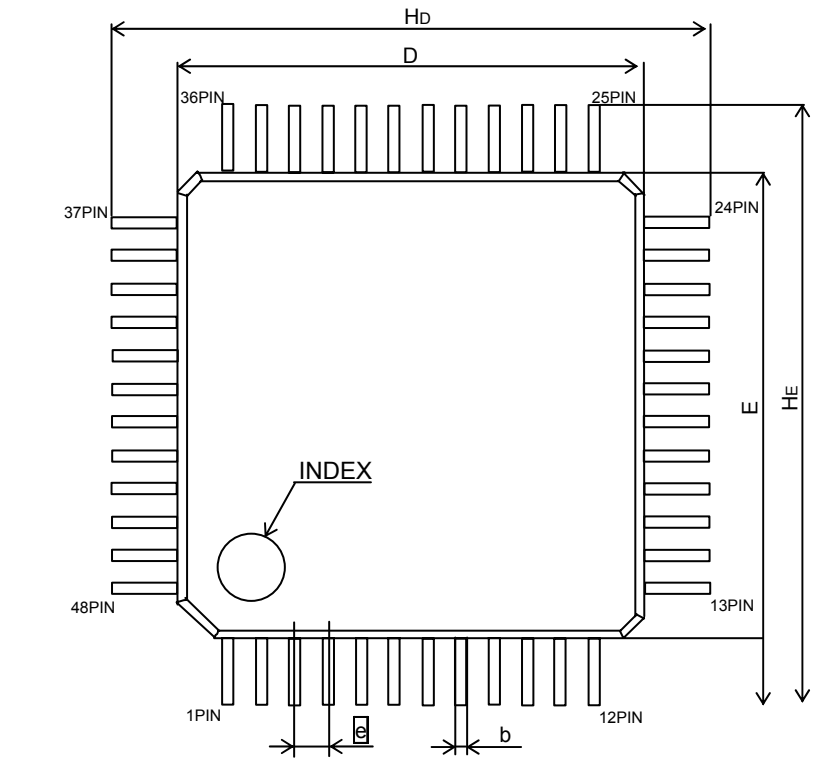


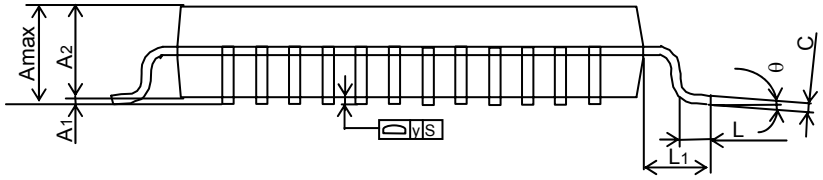


Note1) This connection example shows the selected 4-channel mode.
Note2) Mount the bypass capacitor between each power supply pin.
Note3) Terminating resistor (Rtrm1 to 5) is same face with this IC and place nearly.
(Constant is refer to 6.1.3)
Note4) It is recommended that mount external resistor (Rext) to the same face with this IC.
(Constant is refer to 6.1.2)
Note5) In differential signal pattern of RSDS-Tx and RSDS-RX, it is recommended that connect to same face without through-hold. In respective polarities pattern, connect same length and characteristic impedance with 50Ω±10%.

Subject to change without prior notice.

9. DIMENSIONAL OUTLINE DRAWING





Symbol	Dimension in Millimters		
	Min.	Nom.	Max.
E	—	7	—
D	—	7	—
A_{max}	—	—	1.7
A_1	—	0.1	—
A_2	—	1.4	—
e	—	0.5	—
b	0 13	—	0 27
c	0.09	—	0.2
θ	0°	—	10°
L	0.3	—	0.7
L_1	—	1	—
H_E	—	9	—
H_D	—	9	—
y	—	—	0.08

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