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S2R72A0x/4x Series
Application Note

SEIKO EPSON CORPORATION

Rev.1.10

NOTICE

Table of Contents

1. Overview

This document is an application note applying to all of the following Hub controller LSIs supporting USB 2.0.

S2R72A04 / S2R72A44 (with 4 downstream ports)

S2R72A03 / S2R72A43 (with 3 downstream ports)

S2R72A02 / S2R72A42 (with 2 downstream ports)

This document describes the mode settings, system configuration, circuit examples, and PCB design precautions. For hardware information on this LSI, refer to the data sheet.

2. Mode Description

This LSI includes Mode [4-0] pins, enabling the operation mode to be set to suit the hub system configuration.

2.1 Mode [4-3]: Downstream port enabling setting

This specifies which downstream port is enabled. Note that different available and unavailable settings exist for individual controller LSI model numbers. Note also that settings cannot be changed dynamically.

Table 2.1 Mode [4-3] settings

MODE4	MODE3	Downstream port				LSI setting availability		
		D1	D2	D3	D4	S2R72A44 S2R72A04	S2R72A43 S2R72A03	S2R72A42 S2R72A02
L	L	Enabled	Enabled	Disabled	Disabled	Yes	Yes	Yes
L	H	Enabled	Enabled	Enabled	Disabled	Yes	Yes	No
H	H	Enabled	Enabled	Enabled	Enabled	Yes	No	No
H	L	Disabled				No		

Note that the following pins should be left open for disabled ports.

- Dn_DP
- Dn_DM
- Dn_VBUSEN
- Dn_VBUSFLG

(n = 3, 4 when Mode [4-3] = 00b, and n = 4 when Mode [4-3] = 01b)

2.2 Mode [2-1]: VBUS power supply mode settings

The VBUS power supply fed to the downstream port can be switched on and off using a VBUS switching IC or similar. This enables the system to be protected by switching off the VBUS supply when an overcurrent exceeding the stipulated rating is detected in the downstream. This function can be achieved by connecting the VBUS switching IC to the Dn_VBUSEN and Dn_VBUSFLG pins on this LSI. The following control modes can be selected for this LSI.

Table 2.2 Mode [2-1] settings

MODE2	MODE1	VBUS supply mode
H	H	Individual mode
L	H	Gang mode
H/L	L	Non-control mode

Note that the individual pin logic is as shown below in either Individual or Gang modes.

Dn_VBUSEN pin: Positive logic (VBUS output on for H)

Dn_VBUSFLG pin: Negative logic (Overcurrent detection for L)

If the Dn_VBUSFLG pin receives a Low input, it will be treated as overcurrent detection by the LSI, and the Dn_VBUSEN pin operates to give a Low output within 6 ms to stop the VBUS supply. At the same time, those downstream port's VBUS status change causes the HUB_OVER_CURRENT status bit of the Hub Status (when Gang mode) or PORT_OVER_CURRENT status bit of the Port Status (when Individual mode) on. Those statuses are reported on replies for GetHubStatus() request or GetPortStatus() request. Notification of those changes in the status is given to the USB host via the interrupt pipe on the hub.

Individual mode

This mode allows overcurrent detection and VBUS supply on/off switching for each individual downstream port. VBUS switching ICs are required corresponding to the number of ports, but overcurrent detected in one port does not affect the VBUS supply to other ports.

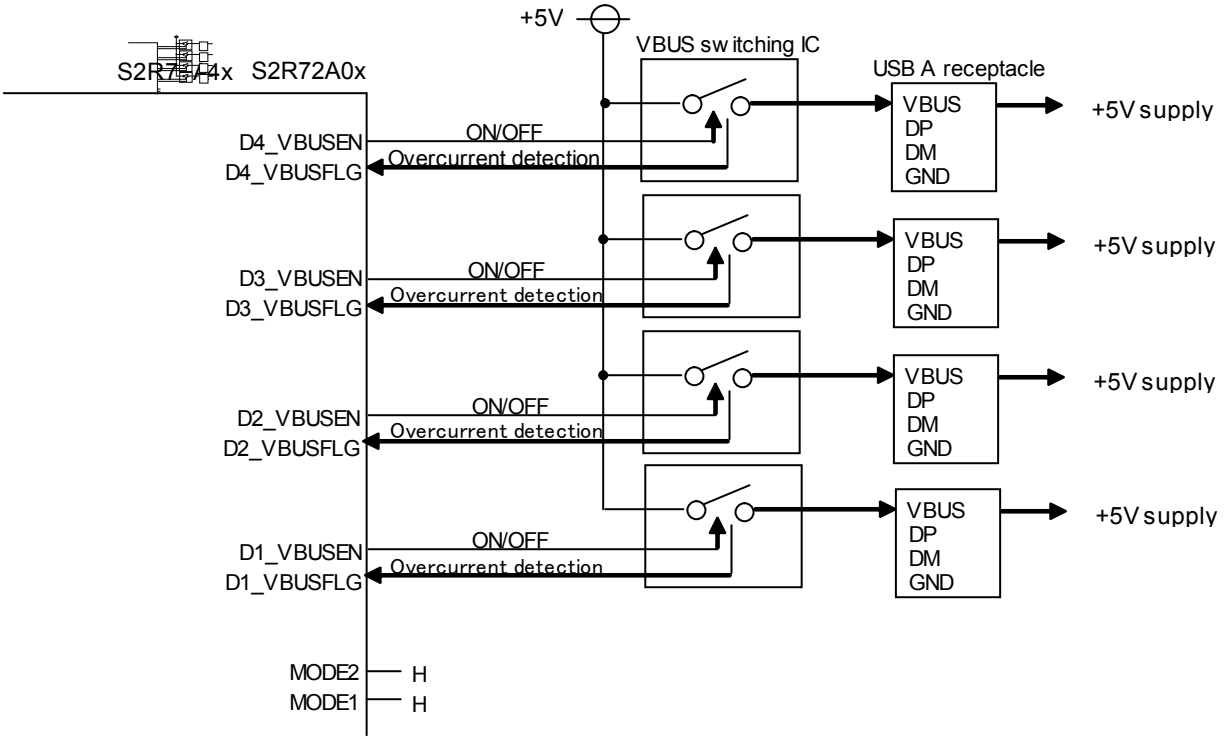


Figure 2.1 Individual mode

Gang mode

This mode achieves combined overcurrent detection and VBUS supply on/off switching of all downstream ports by using port1 pins(D1_VBUSEN and D1_VBUSFLG pins). This requires only one switching unit, but means that overcurrent detection affects the VBUS supply to all ports.

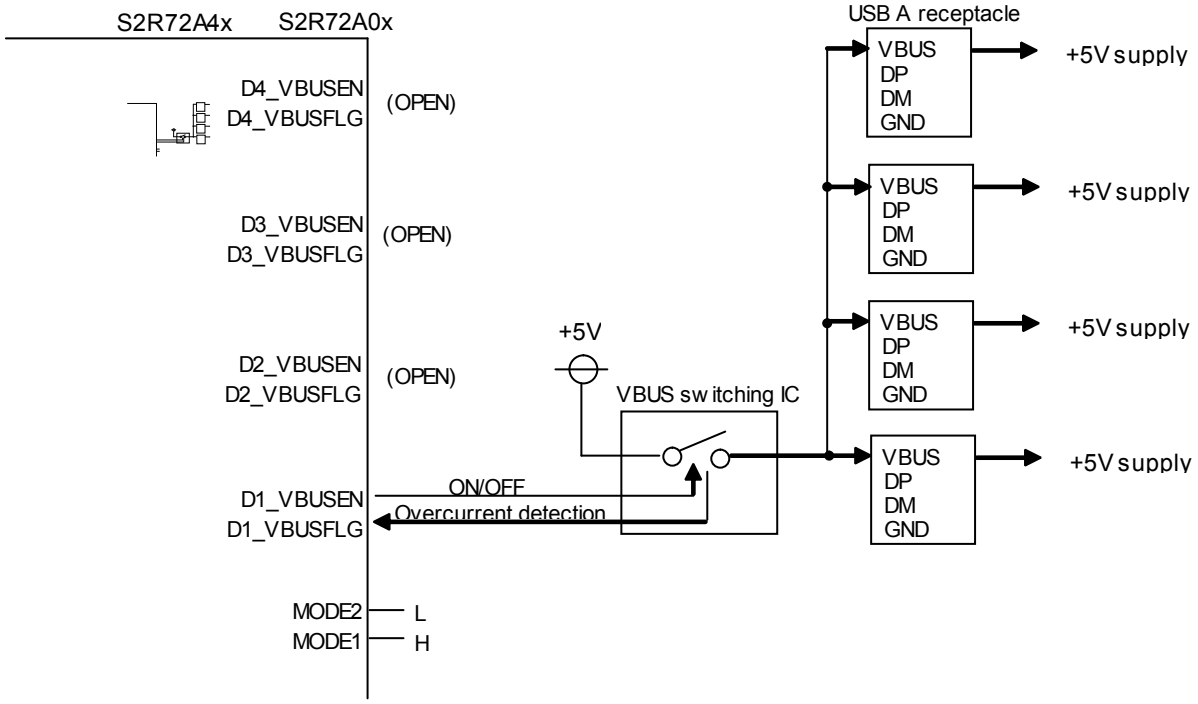


Figure 2.2 Gang mode

Non-control mode

In this mode, the LSI is not involved with VBUS supply. In other words, overcurrent detection status of the VBUS supply to downstream cannot be reported to the USB host. From a safety viewpoint, a protective device of some sort should ideally be included at an appropriate position. Note that the Dn_VBUSEN and Dn_VBUSFLG pins should be left open in this mode.

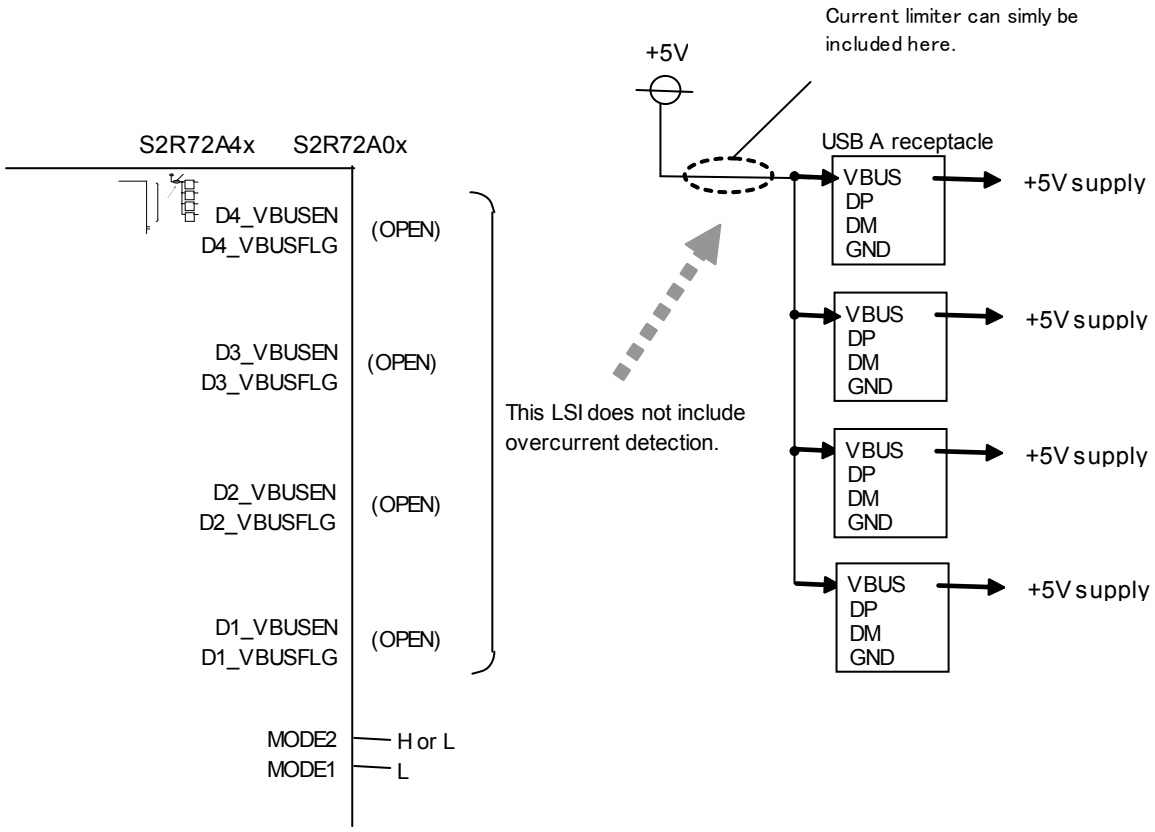


Figure 2.3 Non-control mode

2.3 Mode [0]: Upstream port USB speed settings

The Mode[0] sets the USB speed for the upstream port.

Table 2.3 Mode [0] settings

MODE0	Upstream port speed setting
L	HS/FS automatic detection (USB 2.0)
H	FS fixed (USB 1.1)

3. PCB Design Guide

3.1 Power supply configuration

There are two main hub device power supply configurations, as shown below, but this LSI does not support the bus-powered configuration. The self-powered configuration should be considered for use.

Self-powered configuration

In this configuration, the hub device operates equipped with its own local power supply. The power supply to each downstream port is required to have a capacity of up to 500 mA for each port.

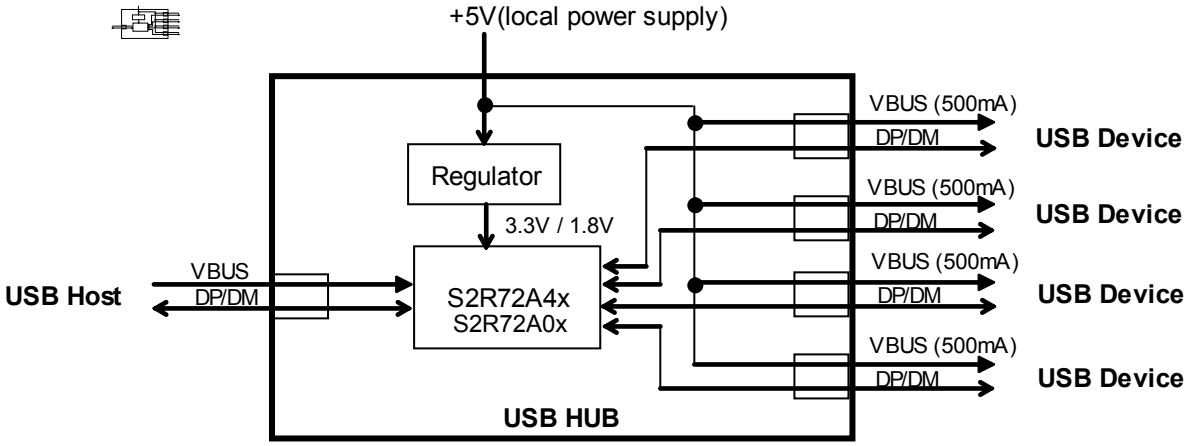


Figure 3.1 Self-powered configuration

Bus-powered configuration (not supported)

In this configuration, the hub device operates using the VBUS power supply from the upstream port. The power supply to each downstream port is required to have a capacity of up to 100 mA for each port. However, this LSI does not support this power supply configuration, as the bmAttributes value in the Configulation descriptor returned to the host by the LSI is "SelfPowered" and also the bMaxPower value is 0x32 (max 100 mA).

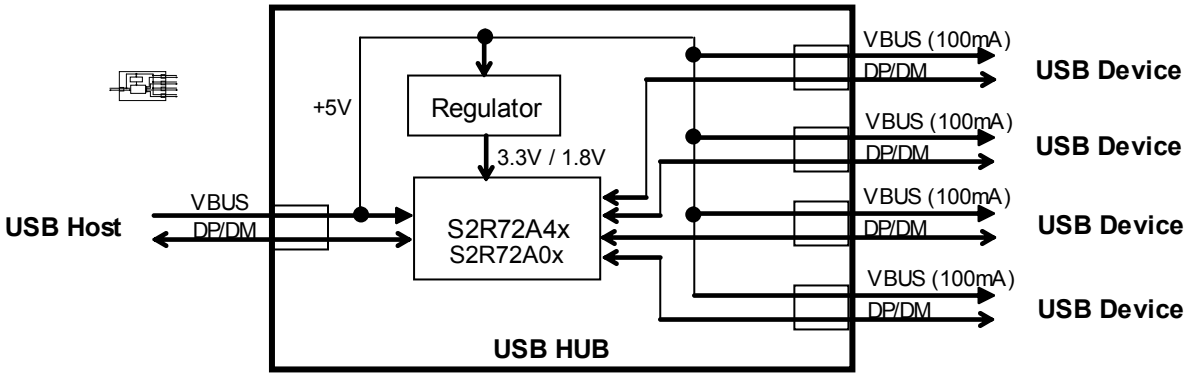


Figure 3.2 Bus-powered configuration (not supported)

3.2 Power supply and resetting

This section describes the power supply fed to the LSI.

Power supply on/off sequence

The power supply fed to this LSI consists of an HVDD power supply (3.3 V) and LVDD power supply (1.8 V), and the on/off sequence and timing specifications should be as shown below. For more information, refer to the Data Sheet.

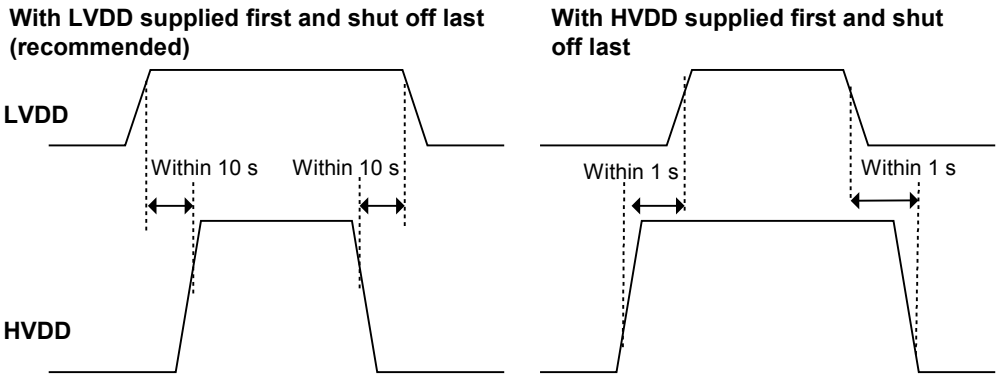


Figure 3.3 Power supply on/off sequence

Note that connecting the USB host to the upstream port while the LSI is not fed with a power supply does not harm the LSI. A current of approximately 40 μA is consumed by the USB host, however, due to the pull-down resistance of 125 kΩ (min 100 kΩ, max 165 kΩ) in the U0_VBUS pin.

Noise

Noise on the power supply may affect the USB waveform quality and cause USB communication problems. Care must be taken when designing the power supply to avoid external noise or ripple noise due to irregular series regulator oscillation or if the switching regulator circuit constants are inappropriate.

Resetting

Once the power supply to the LSI has been turned on, perform reset cancellation by setting the XRESET pin from Low to High. Note that oscillation starts once reset cancellation has been performed and the U0_VBUS pin is subjected to a High level voltage. It is therefore not necessary to perform reset cancellation sequences after oscillation stabilization.

Power supply design

Peak current which appears momentary while there is bus traffic should be considered in power supply design. For example, current consumption on HVDD increases approximately 18mA per hub's transmitting port as compared with the bus is in the idle state, when this LSI is working on the HS mode. It is because of the LSI's power save feature which saves HS transmitter current while it is not transmitting. Power source capacity must cover those current increases.
Below example is showing a current wave form captured with Seiko Epson S5U2R72A04F0100 evaluation board and how it is taken.

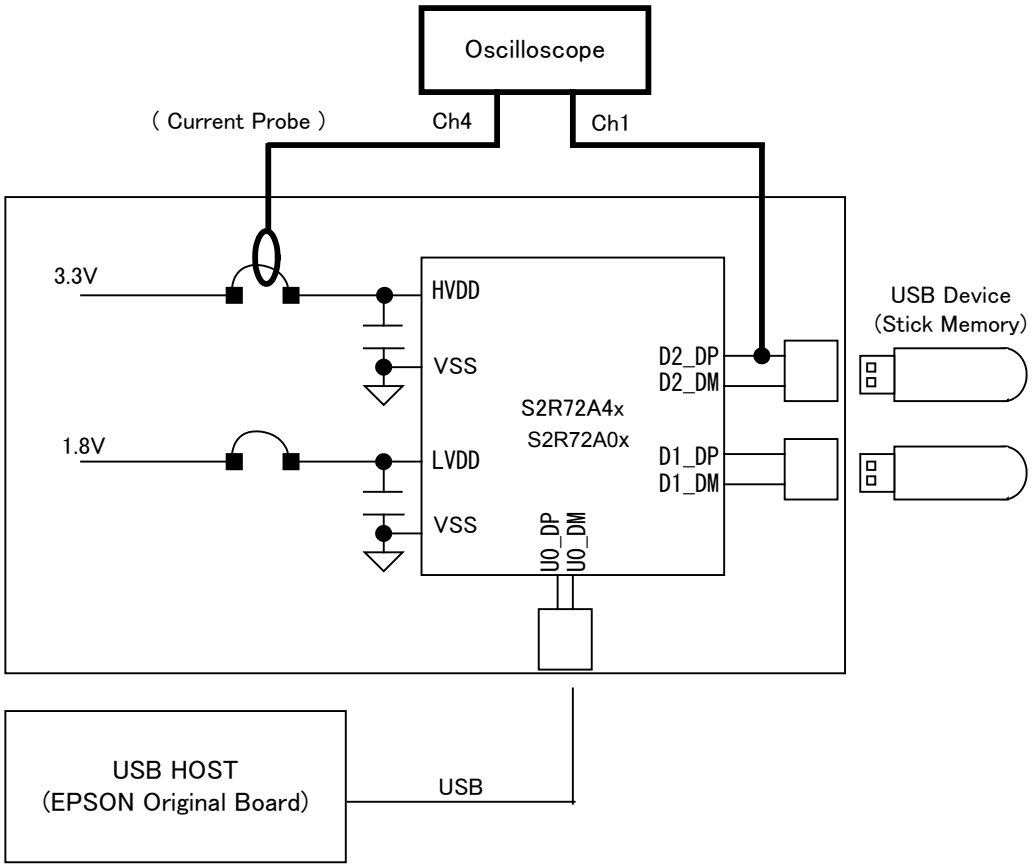


Figure 3.4 Measurement environment

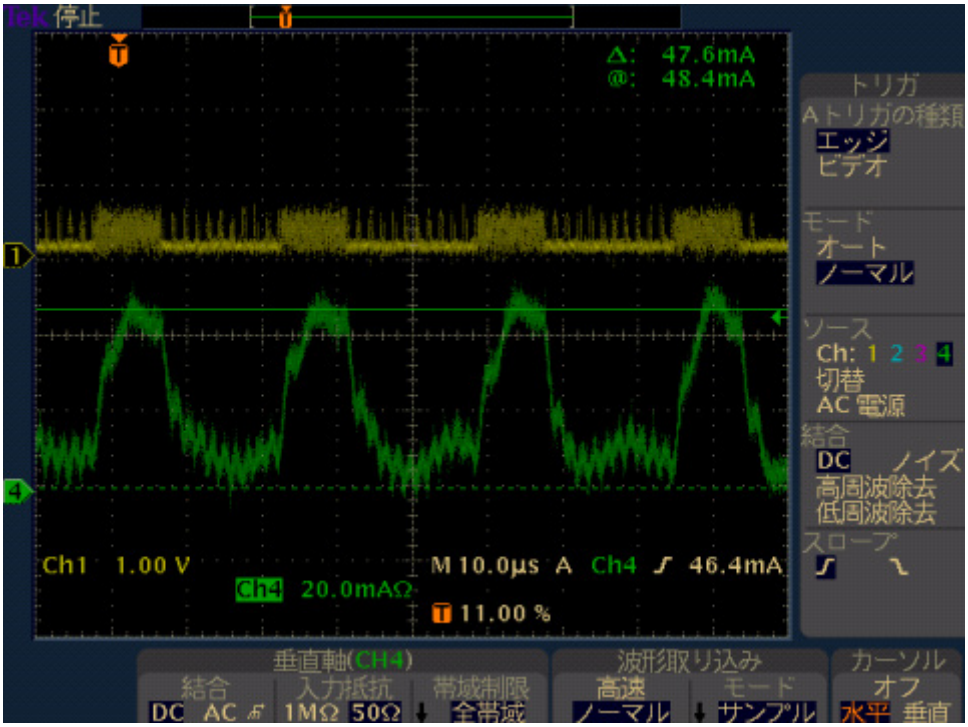


Figure 3.5 Current wave form example

Ch1(yellow line) : DP line on the bus
Ch4(green line) : Current on HVDD

Note that such measured values depend on power source conditions such as regulator characteristics, power line impedance, circuit structure, temperature etc.

3.3 DP/DM signal line

3.3.1 Circuit board wiring

The following points should be taken into consideration for the DP/DM signal wiring to ensure impedance matching and prevent reflection. Refer to the practical examples given in the Appendix.

- The differential impedance in the DP/DM signal line must be 90 Ω.
- Sufficient attention must be paid to impedance matching if other connectors and cables are inserted between the LSI and the USB receptacle.
- The lining layer directly below the signal line must be a non-separated GND plane.
- Signal lines that are considered noise sources (e.g. clock, high-speed bus line) must be kept away from the DP/DM line.
- A pair of DP/DM signal lines should be parallel and of equal length, and should be kept as short as possible. Branches should be minimized, and curved lines should be subject to curved wire treatment.

Note that USB standards stipulate respective transmission delay times for signals within devices, and the following conditions must be satisfied. The signal line lengths to comply with these stipulations will vary depending on parameters such as the dielectric constant, εr, of the board used.

Between the LSI pins (D1 to D4) and receptacle A pins: Within 3 ns

Between the LSI pin (U0) and receptacle B pins: Within 1 ns

3.3.2 Additional components

Common mode choke coil

The common mode choke coil prevents the occurrence of common mode noise by inhibiting current flowing in the same direction in the differential signal line. Use on the DP/DM signal line can be effective in improving skew and in reducing unwanted radiated noise. It is not directly involved in improving Eye-pattern opening. Typical components used for USB High-speed are listed below. Note that components should preferably be installed linearly with respect to the signal line to ensure signal quality.

- TDK ACM2012-900-2P
- Murata DLW21SN900SQ2
- Toko 985BH－1007

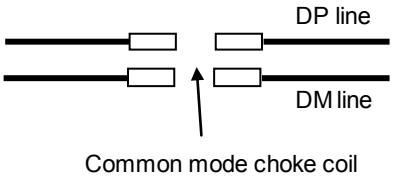


Figure 3.6 Typical common mode choke coil wiring

Chip varistor

Use on the DP/DM signal line can be effective in protecting the LSI DP/DM pins from static electricity and surges. Typical components used for USB High-speed are listed below. Note that components should preferably be installed with shortest possible branches from the signal line to ensure signal quality. The chip varistor mounting position is generally considered more effective in the vicinity of the connectors, but this should be determined after consulting with the respective manufacturers.

- TDK AVR Series
- Panasonic Electronic Devices EZJZ Series

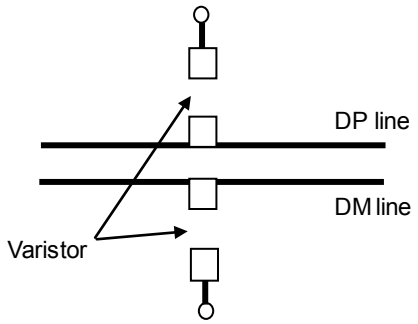


Figure 3.7 Typical varistor wiring

Connector

The DP/DM signal quality may deteriorate if a non-USB certified connector is used. It is recommended that USB-certified connectors be used. The same applies to the cables used.

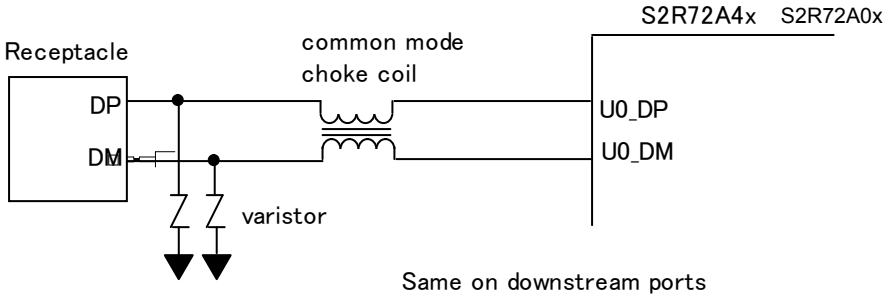


Figure 3.8 DP/DM wiring example

Note: Capacity components

Adding parts with capacity components such as chip varistors on the DP/DM signal line will relax the rising and falling (Tr/Tf) characteristics of the USB high-speed transmission waveform. Care is necessary when selecting parts, as an excessively large capacity component may cause the Tr/Tf characteristics or Eye-pattern to fail the USB compliance test.

3.3.3 Terminations

Since this LSI has cable terminations which are defined in the USB2.0 standard on it's silicon inside the pins as shown in figure 3.9, none of those resisters are required to be assembled on PCB.

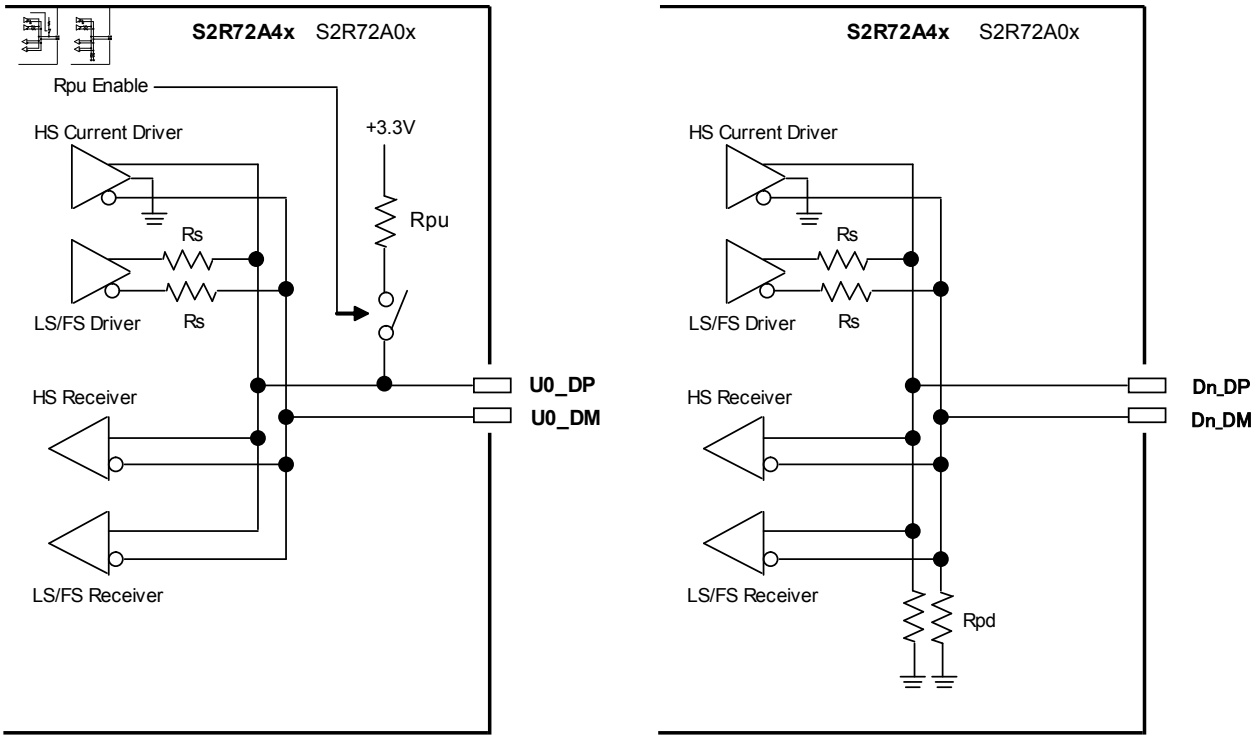


Figure 3.9 Internal termination resisters

3.4 U0_VBUS pin protection circuit (upstream port side)

The U0_VBUS pin may be subjected to a voltage exceeding the VBUS rated voltage (5 V) transiently when connected by the USB cable, depending on the USB host connected to the upstream port. The following protection circuit must be included, as the voltage could exceed the absolute maximum rating of the U0_VBUS pin and damage the LSI. The protection circuit is not required if there is no concern of voltages exceeding the ratings, such as in the case of internal connections that do not involve cable connection or disconnection. The following points must be noted if the circuit constant is altered, and not only in this case.

- The voltage applied to the VBUS pin must not exceed the absolute maximum rating (6 V).
- The U0_VBUS pin input level due to the voltage ratio with the external resistance must not be less than the "H" level trigger voltage, as the VBUS pin is subjected to a 125 kΩ (min 100 kΩ, max 165 kΩ) pull-down inside the IC.

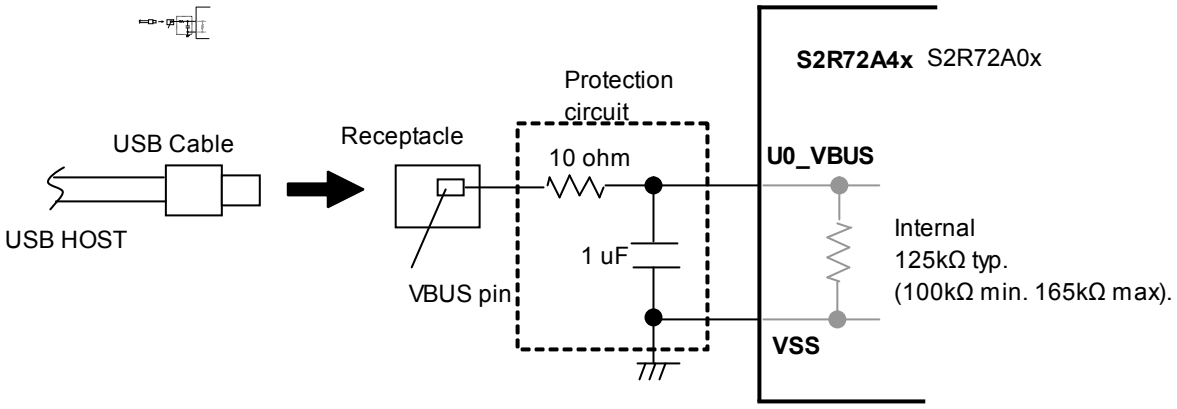
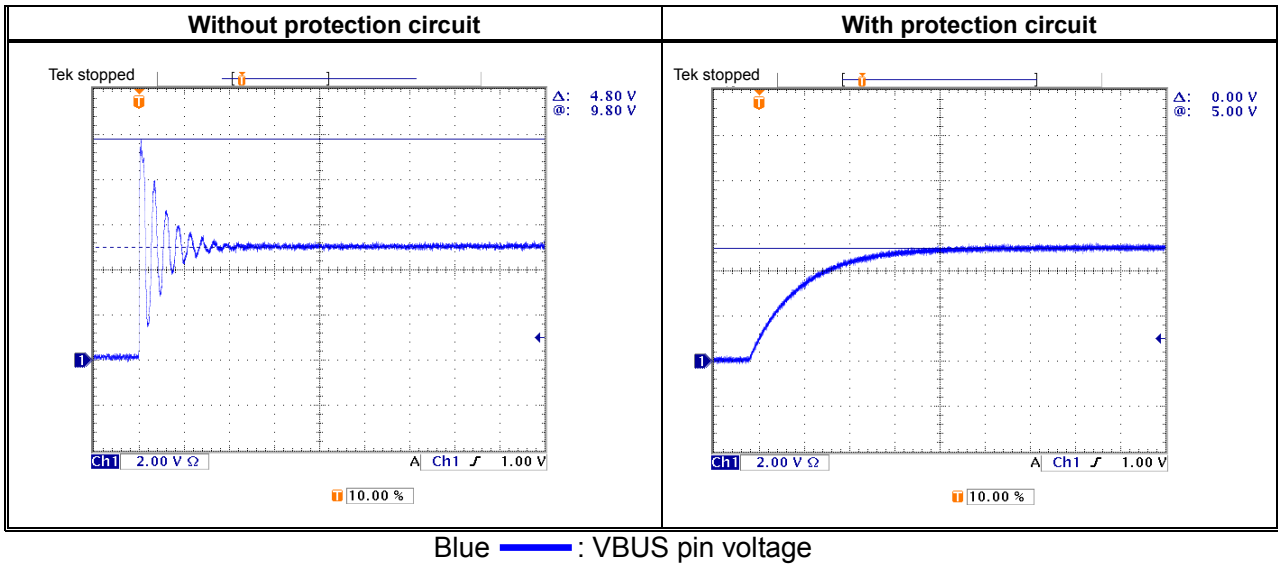


Figure 3.10 U0_VBUS pin protection circuit



Blue ——: VBUS pin voltage

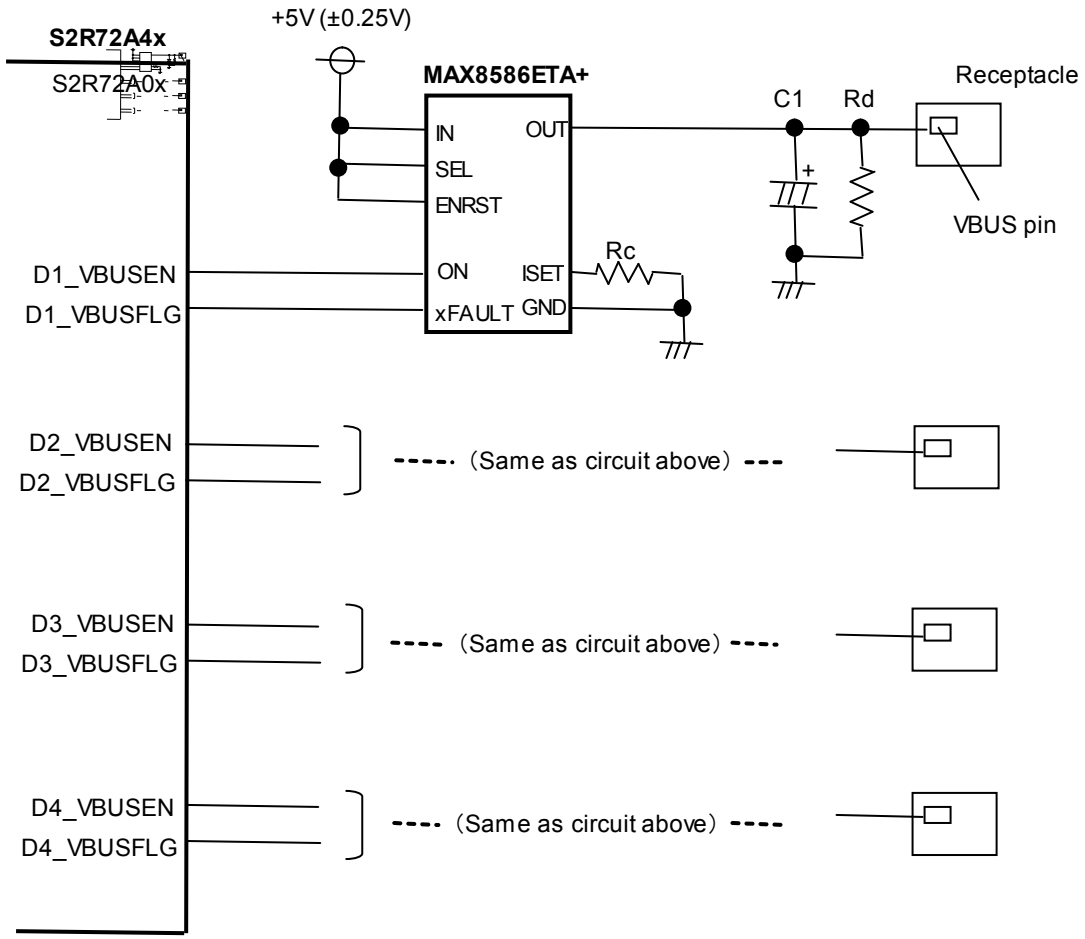
Figure 3.11 U0_VBUS pin applied voltage leading edge waveform

For hub's down-ports, there is no notice like that because no device is expected to give electric charge on VBUS.

3.5 VBUS supply circuit (downstream port side)

This section describes a typical control circuit to feed the VBUS power supply (+5 V) to the downstream port. The circuit configuration will vary depending on the control mode (Individual/Gang). Here, connection examples are shown for both modes using Maxim MAX8586ETA+ USB power switching ICs with overcurrent detection function.

Individual mode



C1: Stipulated as capacitance of at least 120uF in USB 2.0 standards, section 7.2.4. (220uF for Seiko Epson evaluation board S4U2R72A04F0100)
R1: Load discharge resistance for when the VBUS switching IC output is shut off with C1 charged and no USB device connected to the receptacle. (100kΩ for Seiko Epson evaluation board S5U2R72A04F0100)
R2: Resistance for determining the overcurrent detection value. For more information, refer to the MAX8586ETA+ specifications.

Figure 3.12 Individual mode circuit example

Gang mode

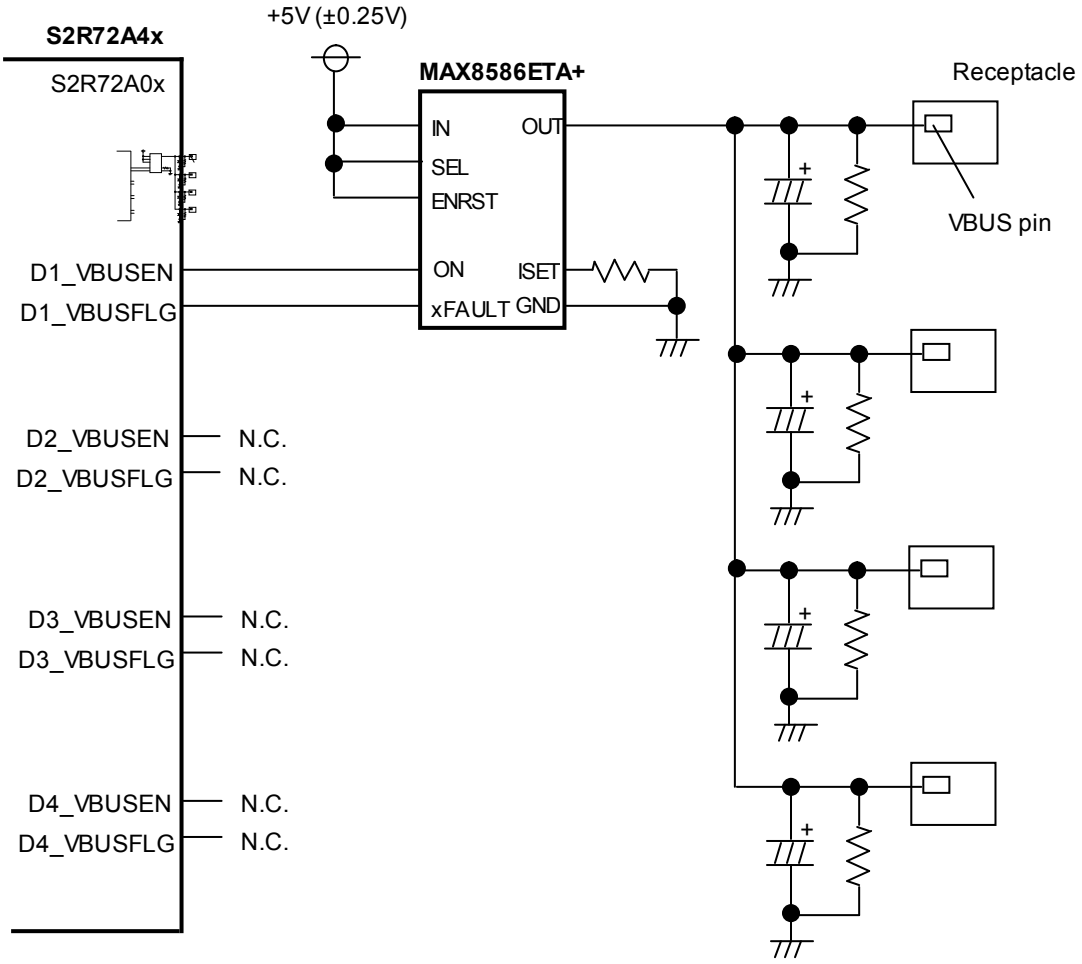


Figure 3.13 Gang mode circuit example

Note: Switch IC consideration

Logic level of VBUS controlling pins of this LSI is fixed as below.
Dn_VBUSEN pin: Active High (Enables VBUS by High)
Dn_VBUSFLG pin: Active Low (Indicates over-current by Low)
So, the VBUS switch IC having different specifications should be fitted to it with some external circuit.

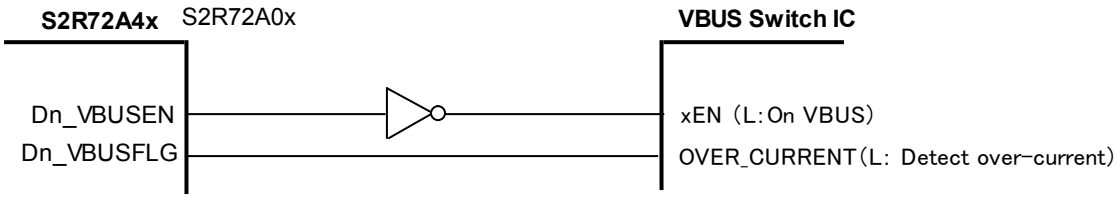
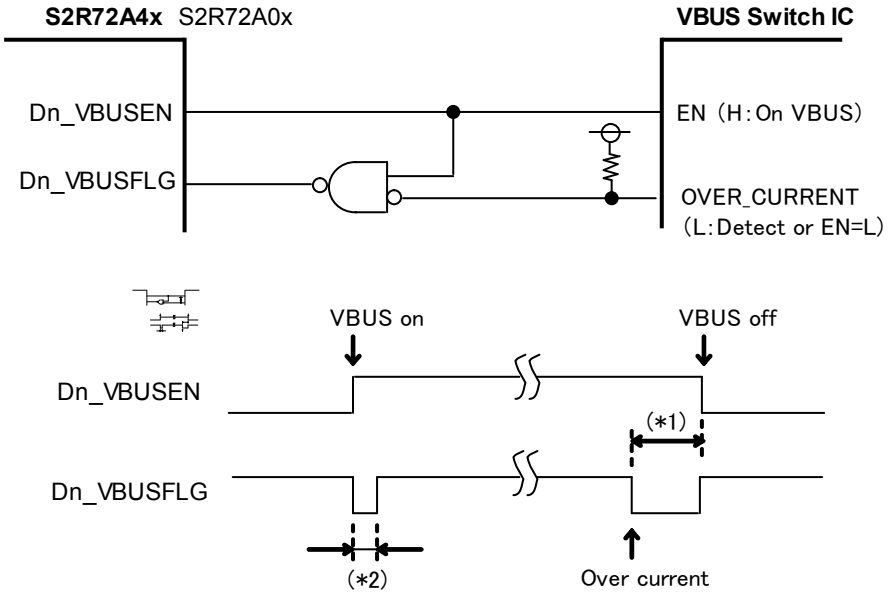


Figure 3.14 Logic converting circuit example

It should be also considered that this LSI does not assert Dn_VBUSEN pin high while Dn_VBUSFLG pin is kept low. Note that some VBUS switch IC are designed as it asserts over-current detection output while it is disenabled. Combination of this kind of VBUS switch IC and this LSI require a special consideration for external circuit to activate. Below is just an example of such external circuit.



(*1) This LSI asserts Dn_VBUSEN low in 6ms after Dn_VBUSFLG is asseted low.
(*2) This LSI ignores Dn_VBUSFLG pulse narrower than 4ms.

Figure 3.15 Adaptor circuit example

3.6 Oscillator circuit

Using a crystal oscillator

A 12 MHz crystal oscillator should be used connected as shown below. The USB high-speed data rate tolerance is ±500 ppm, but the crystal oscillator frequency accuracy should preferably be within ±100 ppm to ensure satisfactory waveform quality. On the other hand, the USB full-speed data rate tolerance is less strict, so the crystal oscillator frequency accuracy can be within ±200 ppm if the LSI is configured as USB1.1 mode (refer to 2.3).

Note that oscillation starts once the LSI has been reset cancelled and the U0_VBUS pin is subjected to a High level voltage. U0_DP is also pulled up immediately (FS termination) when oscillation starts. Oscillation must be stable until a bus reset is subsequently received from the USB host, and this interval is stipulated as being at least 100 ms by the USB standards. There will therefore be no problem if the oscillation stabilization time is within a few ms.

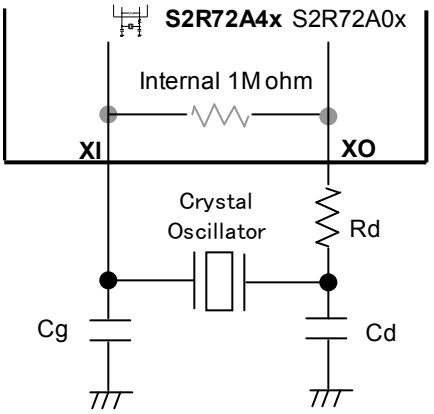


Figure 3.16 Typical crystal oscillator connection circuit

Recommended device (for vehicle mounting): Epson Toyocom FA-238A (C_L = 7pF)

Typical constants for Seiko Epson evaluation board: Cg = 6 pF, Cd = 6 pF, Rd = 0 Ω

Note that our evaluation board is using FA-23A which is previous product.

Using a clock signal

When inputting an external clock signal without using a crystal oscillator, it should be input to the XI pin when power is provided to the LSI. The XO pin should be left open. The clock input can be fed to the XI pin when the U0_VBUS pin input status is either H or L. The clock signal duty ratio is 45% to 55%, and the amplitude is the same as for the LVDD voltage level. The tolerances are the same as for the crystal oscillator.

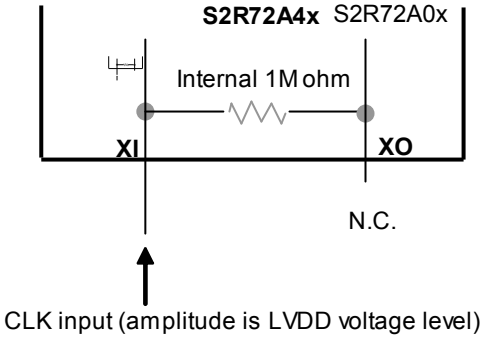


Figure 3.17 External clock input

3.7 Other precautions

Resistance connected to R1 pin

A 12 kΩ ±1% resistance should be positioned as close as possible to the R1 pin. This is used to generate the standard reference current which determines the USB analog circuit characteristics, so the analog characteristics will be affected if the tolerances are overly large. A resistance with the specified accuracy must always be used.

HVDD and LVDD pins

Bypass capacitors should be positioned as close as possible to the HVDD and LVDD pins. The capacitances on Seiko Epson evaluation boards are as shown below, but they will vary depending on the regulator characteristics. It is recommended that they be installed for each power supply pin, to ensure LSI operation stability.

HVDD pins: 0.1 μF (15pin, 31pin), 0.1 μF + 2.2 μF (4pin, 9pin, 42pin)

LVDD pins: 0.01 μF (3pin, 8pin, 16pin, 29pin, 43pin), 0.01 μF + 10 μF (46pin)

VSS pins

The VSS pins must be connected to a non-separated GND plane (see examples in Appendix) via a low impedance.

4. Port USB Connection Speeds

The upstream port U0 connected to the USB host can be set to either a mode automatically detecting HS/FS (USB 2.0) or a mode fixed at FS (USB 1.1) depending on the MODE0 pin setting.

The downstream ports D1 to D4 connected to the USB devices are divided into ports supporting HS/FS/LS and ports supporting FS/LS. These are shown in the table below for the respective LSI model numbers.

Table 4.1 USB speeds for each port

LSI model	Port	USB speeds supported
S2R72A44	U0	HS/FS (MODE0=L) or FS only (MODE0=H)
	D1	HS/FS/LS(U0=HS) or FS/LS(U0=FS)
	D2	HS/FS/LS(U0=HS) or FS/LS(U0=FS)
	D3	FS/LS
	D4	FS/LS
S2R72A43	U0	HS/FS (MODE0=L) or FS only (MODE0=H)
	D1	HS/FS/LS(U0=HS) or FS/LS(U0=FS)
	D2	HS/FS/LS(U0=HS) or FS/LS(U0=FS)
	D3	FS/LS
S2R72A42	U0	HS/FS (MODE0=L) or FS only (MODE0=H)
	D1	HS/FS/LS(U0=HS) or FS/LS(U0=FS)
	D2	HS/FS/LS(U0=HS) or FS/LS(U0=FS)
S2R72A0x	U0	FS
	Dn	FS/LS

Examples of the speed of the USB connected to the downstream ports are shown below for the S2R72A44 with the upstream ports divided into HS and FS respectively. The same applies to A43 and A42, apart from the lack or presence of ports.

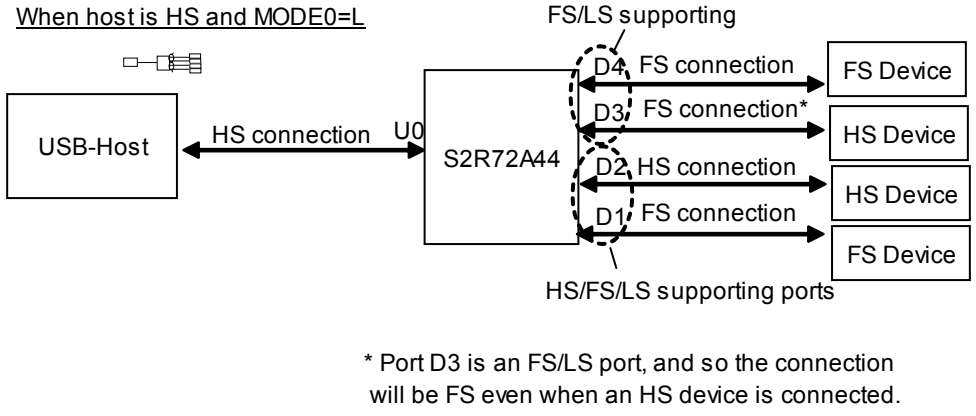


Figure 4.1 Example with upstream HS connection

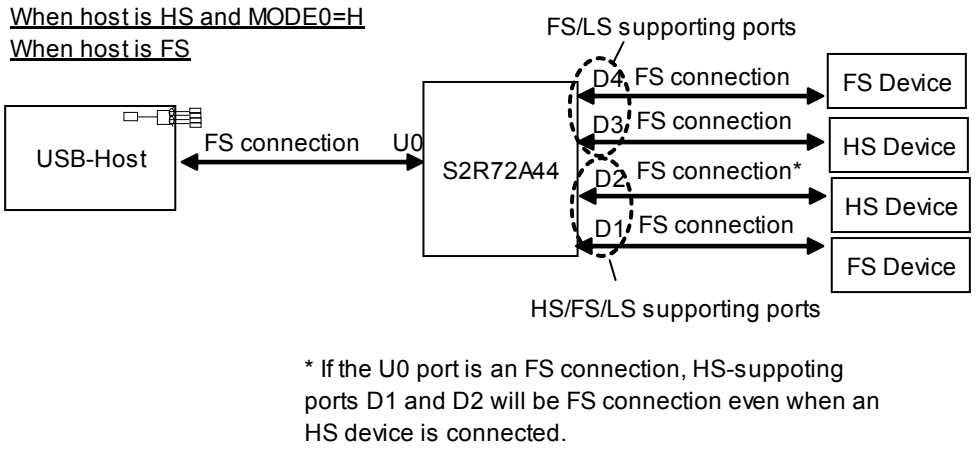


Figure 4.2 Example with upstream FS connection

Note that the USB host is able to know the operating speed of devices connected to the downstream side of the LSI using the status acquired from the LSI (hub). The Port Status Field returned when a GetPortStatus request is issued is as shown below depending on the operating speed.

For HS: PORT_LOW_SPEED=0, PORT_HIGH_SPEED=1

For FS: PORT_LOW_SPEED=0, PORT_HIGH_SPEED=0

For LS: PORT_LOW_SPEED=1, PORT_HIGH_SPEED=0

5. Appendix

5.1 DP/DM circuit board wiring examples

Examples are given below showing DP/DM signal wiring between the LSI and the USB receptacle. Note that components added to the DP/DM signal are omitted here. The dimensions are based on manufacturing data for Seiko Epson evaluation boards (manufactured by Kyoden).

Upstream port side

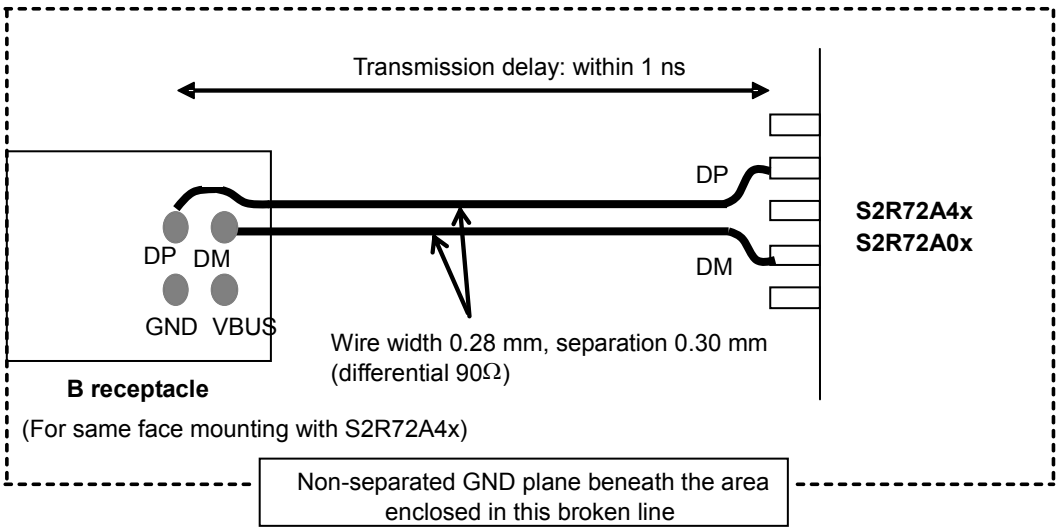


Figure 5.1 B receptacle (through-hole type) example with same-face mounting

Downstream port side

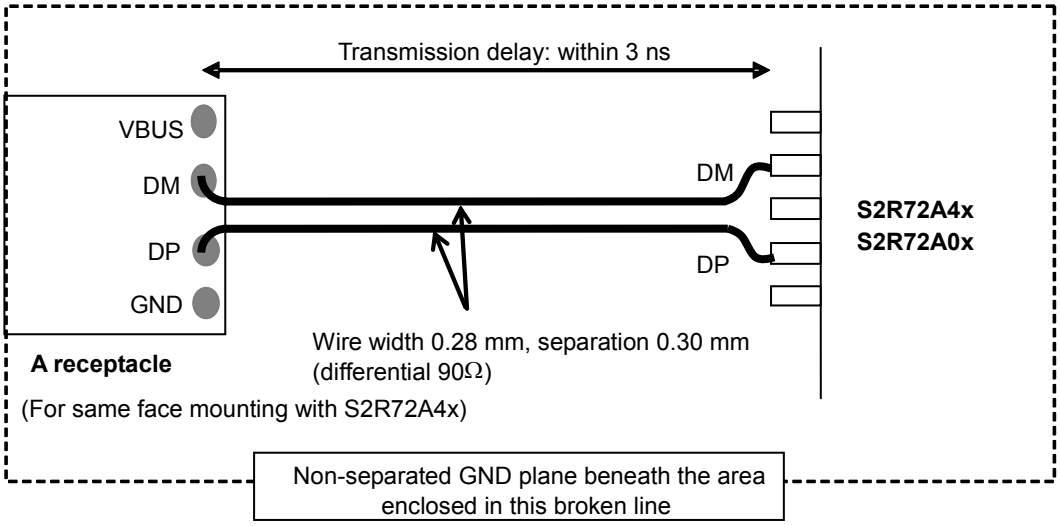


Figure 5.2 A receptacle (through-hole type) example with same-face mounting

5.2 Upstream port connection example

The sequence from HS connection to the upstream port until the downstream port is enabled is described below using the diagram below as an example. This example is for an HS host and MODE0 = L.

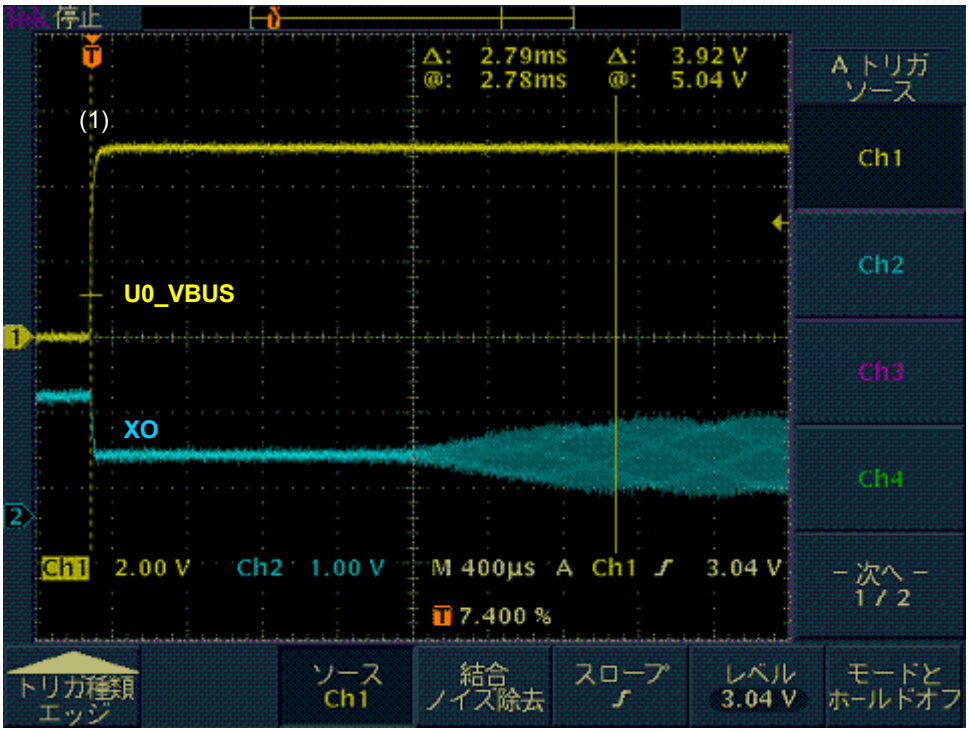


Figure 5.3 Oscillation waveform example

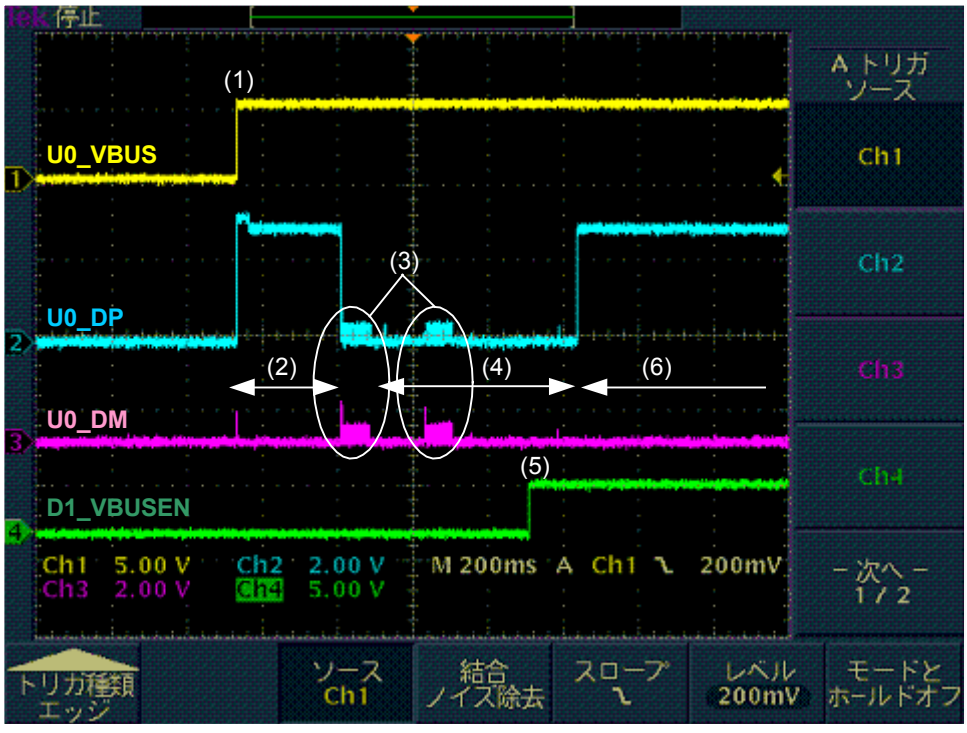


Figure 5.4 Upstream port connection example

(1) U0_VBUS High detection and OSC oscillation

Connecting to a USB host via a cable causes the U0_VBUS pin to switch to High. This triggers the LSI to start internal oscillation.

(2) DP pull-up

After detecting the U0_VBUS pin High level, the LSI pulls up the U0_DP pin using the internal resistance.

(3) Bus resetting and chirping

The LSI returns a Chirp K on receiving a bus reset from the USB host shortly after the U0_DP pin is pulled up. A host chirp is issued from the host in response to this. The speed negotiation is thus completed as High Speed.

(4) Enumeration

The LSI responds to the various requests issued from the host. (The packet waveform is not shown sufficiently in the diagram above.)

(5) Downstream port VBUS enabling

The Dn_VBUSEN pin switched to High in step (4) described above. (x = 1 to 4) This is performed on receiving a SetPortFeature (PORT_POWER) request from the host. The VBUS supply to the downstream port is started using this signal.

(6) Suspended state

In this example, the U0 port enters suspended state once the processing in (4) and (5) above ends. This is because no USB device is connected to the downstream port and no packet is transmitted in this example, and so the upstream port enters suspended state. If a USB device is connected, connection processing with the device starts and the U0 port does not enter suspended state.

5.3 Downstream port overcurrent detection example

The diagram below shows the sequence from detection of an overcurrent in the VBUS power supply fed to the downstream port until the VBUS supply stops. The example below is for Individual mode. The requests used will differ in Gang mode, but the sequence is the same.

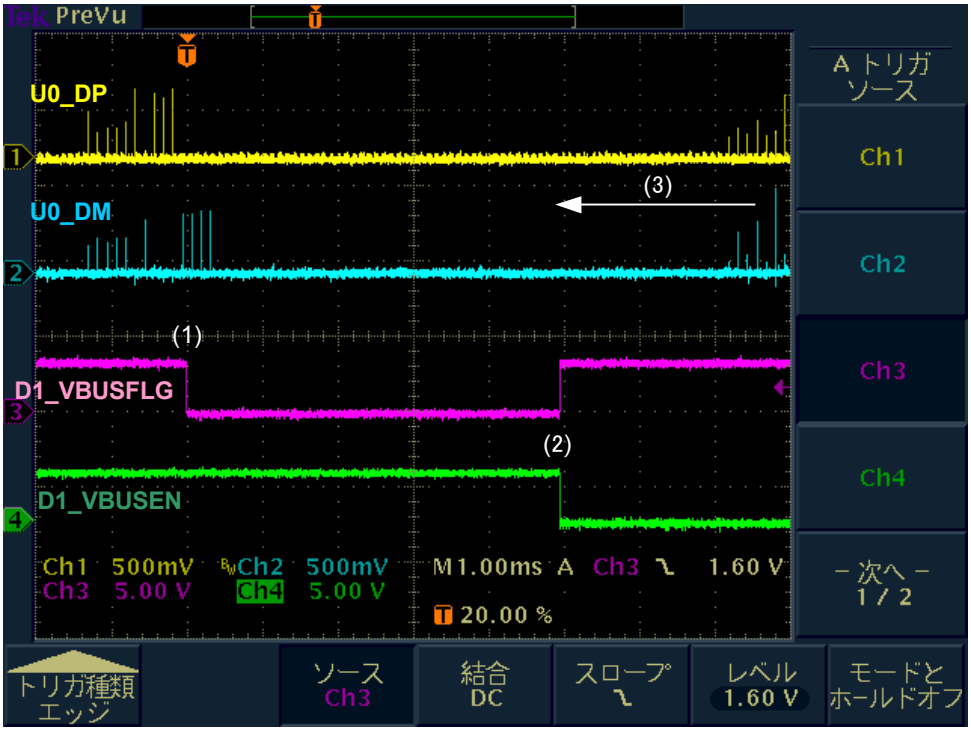


Figure 5.5 Overcurrent detection example

(1) Overcurrent detection

Overcurrent occurrence is detected when a Low level signal is input to the D1_VBUSFLG pin from the external VBUS switching IC, etc. The condition corresponding to overcurrent depends on the VBUS switching IC's specifications and settings.

(2) Downstream port VBUS disabling

The D1_VBUSEN pin outputs a Low signal within 6 ms after (1) above. The VBUS supply to the downstream port is stopped using this signal. In this example, the signal input to the D1_VBUSFLG pin returns to High level at the same time. This is because the external VBUS switching IC no longer detects overcurrent.

(3) Status change notification and request response

The host detects that the overcurrent status has changed in the VBUS port of the LSI's downstream side using the following sequence.

1. The host detects that StatusChange bit has been set for the port in which the overcurrent field changed using Interrupt-IN transfer.
2. The host issues a GetStatus request, and the LSI notifies by setting the PortChangeBits C_PORT_OVER_CURRENT bit. (Note 1)
3. The host issues a ClearFeature (C_PORT_OVER_CURRENT) request.

Note 1: The PortStatusBits PORT_OVER_CURRENT bit is not normally set, as the VBUS supply is stopped and the overcurrent status clears when this request response is issued.

If the host subsequently issues the SetFeature (PORT_POWER) request, the D1_VBUSEN pin outputs High, and the VBUS supply is resumed to this downstream port. However, whether or not the SetFeature request is issued depends on the host specifications, as the process described above will be repeated if the fundamental cause of the overcurrent occurrence remains unchanged.

5.4 Device malfunction detection and recovey

Though a hub is not expected to detect device's malfunction because it has no mechanism to do that other than detach and over-current, it still has an ability to recover a system from devices' temporary failure conditions. For example, followings are possible recovering procedures which hub can serve.

1. VBUS negation
   Off the VBUS by ClearPortFeature(PORT_POWER) request to hub's corresponding port.
   On the VBUS again by SetPortFeature(PORT_POWER) request.
2. Bus reset
   Force hub's down-port bus reset by SetPortFeature(PORT_RESET) request to hub's corresponding port.
   Note that bus reset is not an almighty method to recover a device while hard reset is, because it is a kind of bus protocol handled by a device's usb controller which might be malfunction.

Revision History

Date	Revision details			
	Rev. No.	Page	Category	Details
06/19/2009	0.79	All	New	Newly established
08/03/2009	0.90	18, 22, 23	Add Amend	Added methods for host detecting device connection speed. Amended diagram for overcurrent detection example, and added explanation.
02/28/2011	1.00	All	Add	Added products' name as subjects of this document.
		3	Amend	Amended explanations for over current notification method in clause 2.2.
		5	Fix	Fixed a typo in Gang section in clause 2.2.
		7	Clarify	Clarified a sentence in clause 2.3.
		8	Supplement	Supplemented explanations in Bus-powered section in clause 3.1.
		10, 11	Add	Added "Power supply design" section in clause 3.2.
		13	Add	Added figure 3.8 in clause 3.3.2.
		14	Add	Added clause 3.3.3.
		18	Add	Added Note for switch IC in 3.5.
		19	Amend	Added relieved requirement for crystal part for FS purpose in 3.6.
		20	Amend	Amended recommended capacitance values in 3.7.
		21	Amend	Amended description for supported speed in Table 4.1.
		28	Add	Added 5.4.
10/01/2015	1.10	19	Amend	Amended recommended crystal oscillator from FA-23A to FA-238A and parts values of circumstance of crystal oscillator.

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Document Code: 411812102
First Issue June 2009
Revised October 2015 in JAPAN