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S2S65A30
Data Sheet

SEIKO EPSON CORPORATION

Rev.1.0

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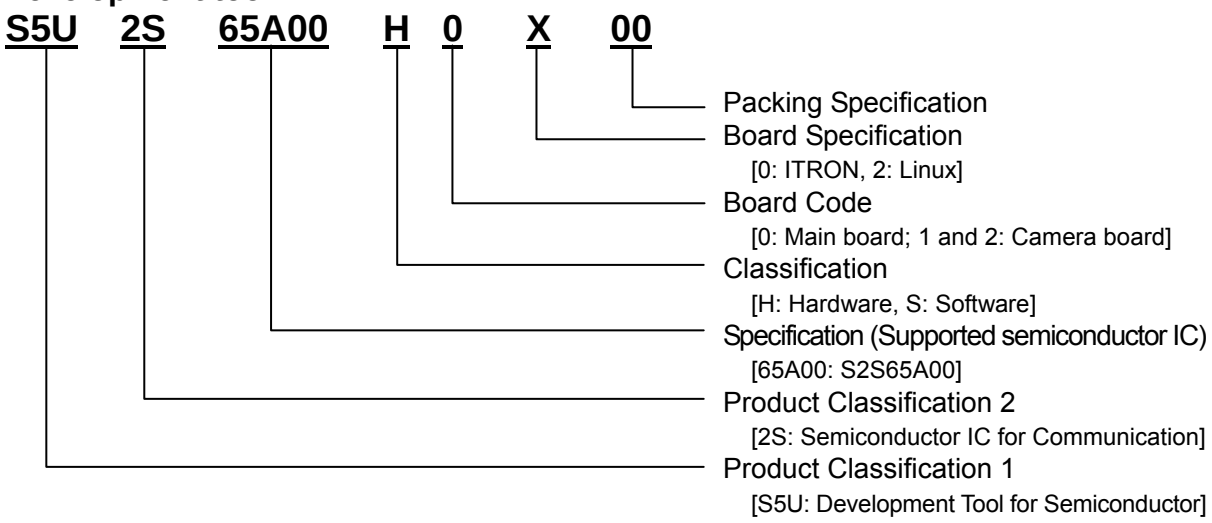
Configuration of product number

● **Device**

● **Development tool**



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1. DESCRIPTION

The S2S65A30 is an image controller IC with additional convenient features and enhanced functions compared to the conventional IC S2S65A00. In addition to these conventional functions, it has an input image-correction function achieved by real-time image processing, an Interlace/Progressive conversion function that allows easy interlace camera connection, a replay function of recorded images and a high-speed write function to a SD card. The operating-temperature accuracy guarantees -40°C to +85°C. Compatible with conventional IC pins, the software is also upper-compatible with the S2S65A00. It is an optimum controller IC for image recording drive recorders.

1.1 Features

- One-chip solution, which can reduce system cost.
- Provides JPEG encoding by using 30 fps @VGA hardware (ISO 10918 compliant).
- Up to two camera modules can be connected.
- Each camera module has two hardware JPEG encoders.
- Provides moving-object detection function to support motion detection.
- Supports I^2S for voice data.
- Has a CompactFlash interface for a CF memory card or a wireless LAN interface (802.11b).
- An SD memory interface for SD memory card connection.
- ARM720T 50MHz operation.
- USB 2.0 device (High-Speed) function support, which enables connection to a PC.
- Supports 8-ch ADC for connection with various analog sensors.
- Contains event counter timers.
- Memory bus: 2 ports (6bit-Bus: FROM/SRAM, 16/32bit-Bus: SDRAM).
- Interlaced/Progressive converion
- JPEG decoding
- Image light and shade correction

1.2 Built-In Functions

CPU:

- 32-bit RISC ARM720T (maximum of 56MHz).
- 32-bit long command codes and 16-bit long command codes called Efficient Thumb Code can be used by switching them.
- 32-bit general purpose register (×31).
- A multiplier is included in the CPU.

RAM:

- 56 KB Built-in RAM for CPU/JPEG Work (CPU Work: 32KB Max.).

Standby Function

- A HALT function to stop the CPU clock when any CPU operation is not required.
- An I/O clock stop function to stop each clock of the main I/O blocks.

Camera Input/JPEG Encoder:

- 8-bit parallel interface × 2 ports
- 2 camera modules can be connected.
- Up to 640×480 resolution (VGA, QVGA, CIF, QCIF).
- Hardware JPEG encoder × 2
- Throughput greater than 30 fps @VGA (when 1 camera module connected).
- YUV4-2-2 progressive (both ports)
- Pixel clock frequency for inputting camera data is less than 2/3 of CPU clock frequency.
- Support of Interlaced signal by Interlace/Progressive conversion(Camera I/F 2ch)

Image light and shade correction :
- Correction function of light and shade part

JPEG:
- Hardware JPEG encoder
- Resize function (screen can be cut off)
- Dedicated line buffer
- Variable volume FIFO built in the JPEG encoder output.
- An enhanced DMA is included in the network.
- Hardware JPEG decoder

USB2.0 Device:
- Supports HS (480Mbps) and FS (12Mbps) transfer.
- Has built-in FS/HS Termination function (external circuit not required).
- VBUS 5V Interface (external protection circuit required).
- Supports control bulk and interrupt transfer.
- Supports 8 end points shared by control (End Point 0) and bulk/interrupt
- Has a 16-bit or 8-bit width general purpose CPU interface.
- Littler Endian is supported.
- Addition to and deletion form the register table is performed based on the HS-Device section of S1R72V05.
- 12MHz or 24MHz crystal oscillator input is supported as clock input for USB.
- As internal clock use, the following frequencies are available based on the clock for the input USB.
- Clock for input USB: 12MHz or 24MHz.
- Clock for internal USB: 60MHz (via PLL for built-in USB).

Memory Controller:
- AHB bus interface memory controller.
- Supports up to four SRAM timing devices.
- Supports up to two SDRAMs.
- Refresh interval of SDRAM auto-refresh can be adjusted to the device.
- SDRAM burst refresh support.
- Supports SDRAM self-refresh.

CF Card Interface:
- Complies with CF+ Specification Rev.1.4.
- Can be used as the interface of wireless LAN, PHS card, etc.
- Supports the True IDE mode.

SD Memory Interface:
- Complies with SD Memory Card Physical Layer Spec. ver.2.0.
- 1-bit/4-bit interface support

Interrupt Controller:
- Supports 32 IRQs and 2 FIQs.

Serial interface:
- UART: Compatible with 16550 software × 3 channel
- SPI: Clock synchronous type × 1 channel
- I^2C master interface (camera interface and multipurpose use)
- I^2S interface (voice/audio data supported, I^2S compliant)

Timer A:
- 16-bit timer × 3-channel timer
- Re-load/cyclic or one shot operation mode
- Supports toggle outputs resulted from underflow output or port outputs.

Timer B: for Event Counter
- 16-bit upcount timer
- Four COMMON registers are implemented, each of which can be configured as an output register or an input capture register.

Watchdog Timer
- Interrupt output or re-settable watchdog timer.

Real Time Clock
- Supports year, month, day, hour, minute and second.
- The internal timer tap from 1/128 to 1/2 can be used as the interrupt source as well.
- Supports alarm function and interrupt.

GPIO:
- General-purpose I/O port (up to 82)
- Programmable setting of directions is possible for all ports.
- Partly selects other I/O functions.

Power Supply:
- 3.3V (I/O power supply)
- 3.3V (USB)
- 1.8V (core power supply)
- 2.4 to 3.6V (Camera 1/2 I/O power supply)
- 2.7 to 3.6V (SDRAM I/O power supply)
- 3.3V (A/D power supply)
- 1.8V (USB/PLL/RTC)

Package:
- PFBGA 280 Pin (PFBGA16UX280) 16 × 16 × 1.2 mm, 0.8 mm ball pitch

2. BLOCK DIAGRAM

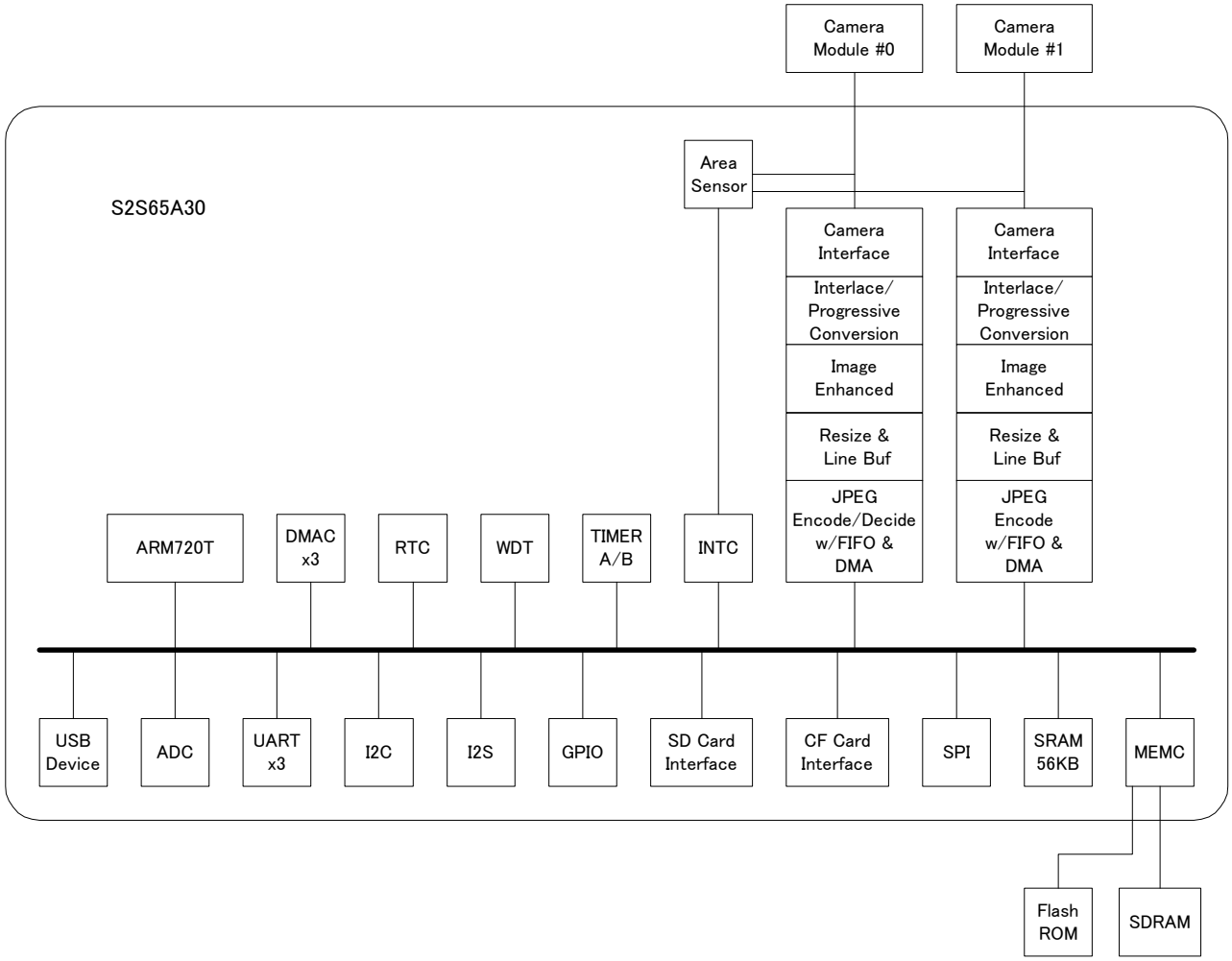


Figure 2.1 S2S65A30 Internal Block Diagram

3. PIN

3.1 Pin Assignment

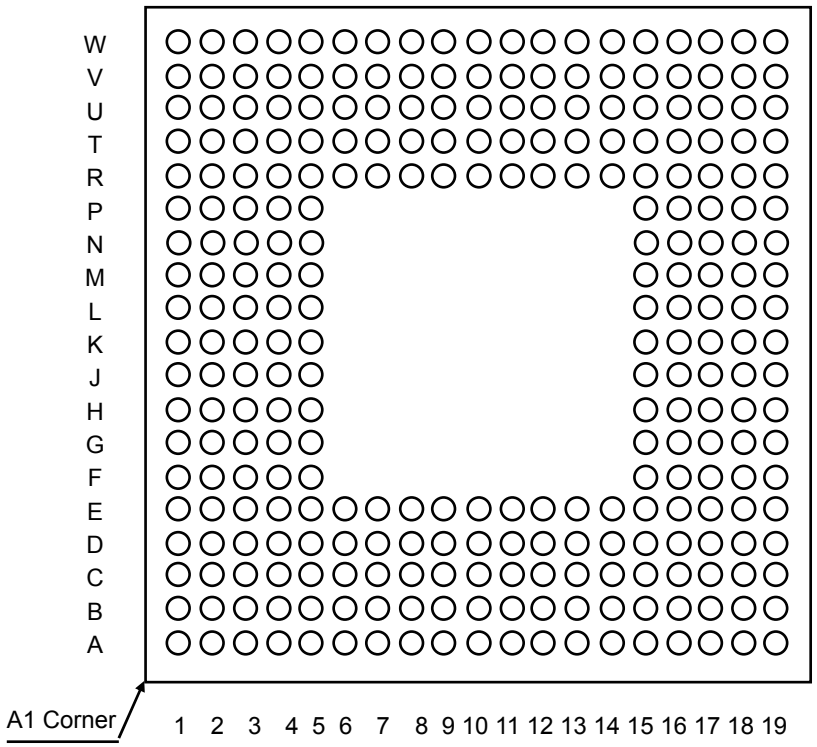


Figure 3.1 Pin Assignment (Bottom View)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	NC	D14	HVDD	K15	LVDD	T7	CM2DATA2
A2	CM1CLKIN	D15	GPIOA2	K16	CFDEN#	T8	GPIOD2
A3	CM1CLKOUT	D16	GPIOA4	K17	CFDDIR	T9	GPIOD1
A4	C1VDD	D17	GPIOA0	K18	LVDD	T10	MA17
A5	SYS_OSCO	D18	LVDD	K19	CFSTSCHG#	T11	MA15
A6	SYS_OSCI	D19	GPIOA1	L1	Vss	T12	MA11
A7	RTCVDD	E1	LVDD	L2	GPIOJ6	T13	MA7
A8	PLLVSS	E2	Vss	L3	GPIOJ3	T14	Vss
A9	SYSVCP	E3	SDA6	L4	GPIOJ5	T15	MA2
A10	SYSCLKI	E4	VSS	L5	LVDD	T16	MCS1#
A11	LVDD	E5	SDA0	L15	HVDD	T17	MD13
A12	Vss	E6	GPIOK5	L16	CFWAIT#	T18	MD12
A13	UXVDD	E7	GPIOK4	L17	CFRST	T19	MD10
A14	DP	E8	Vss	L18	Vss	U1	SDD0
A15	DM	E9	CM1DATA0	L19	CFIRQ	U2	SDDQM1#
A16	UVDD3	E10	TESTEN1	M1	GPIOJ0	U3	CM2HREF
A17	R1	E11	Vss	M2	GPIOJ2	U4	Vss
A18	UPVDD	E12	LVDD	M3	GPIOJ1	U5	CM2DATA4
A19	NC	E13	TDI	M4	SDD15	U6	AVSS
B1	SDA13	E14	GPIOB3	M5	Vss	U7	CM2DATA5
B2	SDA14	E15	GPIOB1	M15	CFCE2#	U8	CM2DATA7
B3	CM1HREF	E16	GPIOB0	M16	MD3	U9	GPIOD3

3. PIN

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
B4	Vss	E17	GPIOA3	M17	CFCE1#	U10	GPIOD0
B5	CM1DATA3	E18	HVDD	M18	CFIORD#	U11	MA16
B6	CM1DATA6	E19	GPIOA5	M19	CFIOWR#	U12	MA12
B7	Vss	F1	SDA1	N1	SDD11	U13	MA8
B8	BUP#	F2	SDVDD	N2	Vss	U14	MA4
B9	PLLVDD	F3	SDA5	N3	SDD13	U15	MA1
B10	SYSCKSEL	F4	SDA2	N4	SDD14	U16	Vss
B11	TRST#	F5	GPIOK1	N5	SDD12	U17	MBEL#
B12	TESTCK	F15	LVDD	N15	MD5	U18	MD14
B13	XVSS	F16	GPIOB2	N16	MD1	U19	MD15
B14	UVDD3	F17	GPIOA6	N17	Vss	V1	GPIOD6
B15	UVSS	F18	LVDD	N18	MD2	V2	Vss
B16	Vss	F19	GPIOA7	N19	MD0	V3	CM2VREF
B17	UVSS	G1	GPIOK7	P1	SDVDD	V4	CM2DATA0
B18	PVSS	G2	GPIOK6	P2	SDD10	V5	AVDD
B19	USBOSCO	G3	GPIOK3	P3	SDD9	V6	ADIN7
C1	SDA11	G4	GPIOK0	P4	SDD8	V7	ADIN5
C2	Vss	G5	Vss	P5	Vss	V8	ADIN3
C3	SDVDD	G15	GPIOC1	P15	MD9	V9	ADIN1
C4	SDA12	G16	HVDD	P16	MD8	V10	AVSS
C5	CM1VREF	G17	GPIOB5	P17	MD6	V11	MA19
C6	CM1DATA5	G18	Vss	P18	MD4	V12	MA14
C7	CM1DATA7	G19	GPIOB4	P19	LVDD	V13	Vss
C8	Vss	H1	LVDD	R1	SDD6	V14	MA3
C9	HVDD	H2	Vss	R2	SDD5	V15	GPIOD5
C10	Vss	H3	GPIOK2	R3	SDD4	V16	MCS0#
C11	TESTEN0	H4	SDWE#	R4	SDD7	V17	MWE#
C12	TDO	H5	SDCAS#	R5	SDD3	V18	LVDD
C13	Vss	H15	GPIOC6	R6	SD2	V19	Vss
C14	VBUS	H16	GPIOC0	R7	CM2DATA1	W1	NC
C15	Vss	H17	GPIOB6	R8	CM2DATA6	W2	CM2CLKIN
C16	HVDD	H18	HVDD	R9	Vss	W3	CM2CLKOUT
C17	Vss	H19	GPIOB7	R10	HVDD	W4	C2VDD
C18	Vss	J1	SDCS1#	R11	MA13	W5	AVDD
C19	USBOSCI	J2	SDCS0#	R12	MA9	W6	ADIN6
D1	SDA8	J3	SDRAS#	R13	MA6	W7	ADIN4
D2	SDA9	J4	GPIOJ7	R14	MA5	W8	ADIN2
D3	SDA7	J5	GPIOJ4	R15	HVDD	W9	ADIN0
D4	SDA10	J15	GPIOC7	R16	GPIOD4	W10	AVDD
D5	SDA4	J16	GPIOC5	R17	MD11	W11	MA18
D6	SDA3	J17	GPIOC4	R18	Vss	W12	HVDD
D7	CM1DATA1	J18	GPIOC3	R19	MD7	W13	MA10
D8	CM1DATA2	J19	GPIOC2	T1	Vss	W14	LVDD
D9	CM1DATA4	K1	SDCLK	T2	LVDD	W15	HVDD
D10	LVDD	K2	SDCLKEN	T3	SDD1	W16	MA0
D11	TCK	K3	SDVDD	T4	GPIOD7	W17	MOE#
D12	TMS	K4	SDVDD	T5	SDDQM0#	W18	MBEH#
D13	RESET#	K5	Vss	T6	CM2DATA3	W19	NC

Note: # at the right end of pin name indicates to be an active low signal.

3.2 Pin Description

＃ : # at the right end of pin name indicates to be an active low signal.
I : Input pin
O : Output pin
IO : Bi-directional pin
P : Power supply

Table 3.1 Cell Type Description

Cell Type	Description	Example of Pin being Used
ICS	LVCMOS Schmitt input	TCK, CLKI, RESET#
ICD1	LVCMOS input with pull-down resistor (50kΩ@3.3V)	TESTEN
ICU1	LVCMOS input with pull-up resistor (50kΩ@3.3V)	TMS, TDI
ICSU1	LVCMOS Schmitt input with pull-up resistor (50kΩ@3.3V)	TRST#
ICSD1	LVCMOS Schmitt input with pull-down resistor (50kΩ@3.3V)	SYSCKSEL
ILTR	Low Voltage Transparent Input	SYS_CSCI, USB_OSCI
IHTR	High Voltage Transparent Input	ADIN[7:0]
BLNC4	Low noise LVCMOS IO buffer (±4mA)	GPIOA[7:0], GPIOB[7:0]
BLNC4U1	Low noise LVCMOS IO buffer with pull-up resistor (50kΩ@3.3V) (±4mA)	CF Interface
BLNC4D2	Low noise LVCMOS IO buffer with pull-down resistor (100kΩ@3.3V) (±4mA)	MD [15:0]
BLNS4	Low noise LVCMOS Schmitt IO buffer (±4mA)	GPIOA, GPIOB, GPIOD [1:0]
BLNS4D1	Low noise LVCMOS Schmitt IO buffer with pull-down resistor (50kΩ@3.3V) (±4mA)	Camera Interface
OLN4	Low noise output buffer (±4mA)	MEMC Interface (excluding MD)
OTLN4	Low noise Tri-state output buffer (±4mA)	TDO
OLTR	Low Voltage Transparent Output	VCP

Table 3.2 Pin Description

Pin Name	Type	Cell Type	Pin No.	Description
(MA [23:20])	(I/O)	(BLNS4)		For information on these pins, see the description of **GPIOD [3:0]**.
MA [19:12]	O	OLN4	V11,W11, T10,U11, T11,V12, R11,U12	**Address Output Signal for Flash-ROM/SRAM [19:12]**
MA 11	O	OLN4	T12	This pin has the following functions: • **MA11: Address output signal for Flash-ROM/SRAM [11]** (Pin function right after reset) • **CFREG# Output Signal** When the compact flash (CF) interface is in operation, this signal functions as the REG signal selecting attribute of the CF interface and I/O space.
MA [10:0]	O	OLN4	W13,R12, U13,T13, R13,R14, U14,V14, T15,U15, W16	These pins have the following functions: • **MA [10:0]: Address output signal for Flash-ROM/SRAM [10:0]** (Pin function right after reset) • **CFADDR [10:0] Output signal** When the CF interface is in operation, this signal becomes the CF interface address signal [10:0].
MBEL#	I/O	OLN4	U17	Data bus low byte enable output for **Flash-ROM/SRAM**
MBEH#	I/O	OLN4	W18	Data bus high byte enable output for **Flash-ROM/SRAM**

Pin Name	Type	Cell Type	Pin No.	Description
MD [15:0]	I/O	BLNC4D2	U19,U18, T17,T18, R17,T19, P15,P16, R19,P17, N15,P18, M16,N18, N16,N19	These pins have the following functions: • **16-bit data bus for Flash-ROM/SRAM** (Pin function right after reset) • **When the CF interface is in operation, this pin becomes good for 16-bit data.** • **MODESEL[15:0]** Sampled to determine the internal operation mode, at power-on resetting (RESET# transition from Low to High). For details, see section "4.1 System Configuration". Here, to determine the operation mode, a pull-up resistance may be required externally. (Resistance in the range from 4.7 to 10kΩ)
MCS [3:2]#	O	(BLNS4)	V15,R16	For information on these pins, see the description of **GPIOD [5:4]**.
MCS [1:0]#	O	OLN4	T16,V16	**Chip select signal for Flash-ROM/SRAM [1:0]** (Active low signal)
MOE#	O	OLN4	W17	This pin has the following functions: (Active low signal) • **MOE#: Strobe signal for Flash-ROM/SRAM** (Pin function right after reset) • **CFOE# output signal** When the CF interface is in operation, this signal becomes the output enable signal of CF interface memory and attribute spaces.
MWE#	O	OLN4	V17	This pin has the following functions: (Active low signal) • **MWE#: Write enable signal for Flash-ROM/SRAM** (for static memory) (Pin function right after reset) • **CFWE# output signal** When the CF interface is in operation, this signal becomes the write enable signal of CF interface memory and attribute spaces.
SDA [14:0]	O	OLN4	B2,B1, C4,C1, D4,D2, D1,D3, E3,F3, D5,D6, F4,F1, E5	**Address output for SDRAM [14:0]**
SDD[31:16]	(I/O)	(BLNC4D2)		For information on these pins, see the descriptions of **GPIOK [7:0] and GPIOJ [7:0]**.
SDD [15:0]	I/O	BLNC4D2	M4,N4, N3,N5, N1,P2, P3,P4, R4,R1, R2,R3, R5,R6, T3,U1	**Data I/O for SDRAM [15:0]**
SDWE#	O	OLN4	H4	**Write enable signal for SDRAM**
SDCLK	O	OLN4	K1	**Outputting clock for SDRAM** The same frequency as internal operation frequency (CPUCLK) is output.
SDCLKEN	O	OLN4	K2	**Clock enable signal for SDRAM**
SDRAS#	O	OLN4	J3	**RAS signal for SDRAM** (Active low signal)
SDCAS#	O	OLN4	H5	**CAS signal for SDRAM** (Active low signal)
SDCS[1:0]#	O	OLN4	J1,J2	**Chip select signal for SDRAM** (Active low signal)

Pin Name	Type	Cell Type	Pin No.	Description
SDDQM[3:2]#	(I/O)	(BLNS4)		For information on these pins, see the description of **GPIOD [7:6]**.
SDDQM[1:0]#	O	OLN4	U2,T5	**DQM signal for SDRAM** (Active low signal) SDDQM0# corresponds to the lower bytes; SDDQM1#, to the higher bytes.
CM1DATA[7:0]	I/O	BLNS4D1	C7,B6, C6,D9, B5,D8, D7,E9	These pins have the following functions: • **CM1DATA [7:0]: Camera 1YUV data input** This pin, when reset, becomes good for inputting GPIOE [7:0]. To use as the CM1DATA [7:0] pin, set bits [15:0] of the GPIOE pin function register to "Function 1 other than GPIO." • **IPC1DATA [7:0]: Interlace Camera 1YUV data input** This pin, when reset, becomes good for inputting GPIOE [7:0]. To use as the IPCM1DATA [7:0] pin, set bits [15:0] of the GPIOE pin function register to "Function 2 other than GPIO." • **GPIOE [7:0] I/O** (Pin function right after reset)
CM1VREF	I/O	BLNS4D1	C5	This pin has the following functions: • **CM1VREF: Vertical sync input at Progressive camera 1 data input** This pin, when reset, becomes good for inputting GPIOF0. To use as the CM1VREF pin, set bits [1:0] of the GPIOF pin function register to "Function 1 of other than GPIO." • **IPC1VREF: Vertical sync input at Interlaced camera 1 data input** This pin, when reset, becomes good for inputting GPIOF0. To use as the IPC1VREF pin, set bits [1:0] of the GPIOF pin function register to "Function 2 of other than GPIO." • **GPIOF0 I/O** (Pin function right after reset)
CM1HREF	I/O	BLNS4D1	B3	This pin has the following functions: • **CM1HREF: Horizontal sync input at Progressive camera 1 data input** This pin, when reset, becomes good for inputting GPIOF1. To use as the CM1HREF pin, set bits [3:2] of the GPIOF pin function register to "Function 1 of other than GPIO." • **IPC1HREF: Horizontal sync input at Interlaced camera 1 data input** This pin, when reset, becomes good for inputting GPIOF1. To use as the IPC1HREF pin, set bits [3:2] of the GPIOF pin function register to "Function 2 of other than GPIO." • **GPIOF1 I/O** (Pin function right after reset)

Pin Name	Type	Cell Type	Pin No.	Description
CM1CLKOUT	I/O	BLNS4D1	A3	This pin has the following functions: • **CM1CLKOUT: Basic clock output for Progressive camera 1** This pin, when reset, becomes good for inputting GPIOF2. To use as the CM1CLKOUT pin, set bits [5:4] of the GPIOF pin function register to "Function 1 of other than GPIO." • **IPC1FIELD: Field identification signal for Interlaced camera 1** This pin, when reset, becomes good for inputting GPIOF2. To use as the IPC1FIELD pin, set bits [5:4] of the GPIOF pin function register to "Function 2 of other than GPIO." • **GPIOF2 I/O** (Pin function right after reset)
CM1CLKIN	I/O	BLNS4D1	A2	This pin has the following functions: • **CM1CLKIN: Pixel clock for inputting Progressive camera 1 data** This pin, when reset, becomes good for inputting GPIOF3. To use as the CM1CLKIN pin, set bits [7:6] of the GPIOF pin function register to "Function 1 of other than GPIO." • **IPC1CLKIN: Pixel clock for inputting Interlaced camera 1 data** This pin, when reset, becomes good for inputting GPIOF3. To use as the IPC1CLKIN pin, set bits [7:6] of the GPIOF pin function register to "Function 2 of other than GPIO." • **GPIOF3 I/O** (Pin function right after reset)
CM2DATA[7:0]	I/O	BLNS4D1	U8,R8 U7,U5 T6,T7, R7,V4	These pins have the following functions: • **CM2DATA [7:0]: Camera 2YUV data input** This pin, when reset, becomes good for inputting GPIOG [7:0]. To use as the CM2DATA [7:0] pin, set bits [15:0] of the GPIOG pin function register to "Function 1 other than GPIO." • **IPC2DATA [7:0]: Interlace Camera 2YUV data input** This pin, when reset, becomes good for inputting GPIOG [7:0]. To use as the IPCM2DATA [7:0] pin, set bits [15:0] of the GPIOG pin function register to "Function 2 other than GPIO." • **GPIOG [7:0] I/O** (Pin function right after reset)
CM2VREF	I/O	BLNS4D1	V3	This pin has the following functions: • **CM2VREF: Vertical sync input at camera 2 data input** This pin, when reset, becomes good for inputting GPIOF4. To use as the CM2VREF pin, set bits [9:8] of the GPIOF pin function register to "Function 1 of other than GPIO." • **IPC2VREF: Vertical sync input at Interlaced camera 2 data input** This pin, when reset, becomes good for inputting GPIOF4. To use as the IPC2VREF pin, set bits [1:0] of the GPIOF pin function register to "Function 2 of other than GPIO." • **GPIOF4 I/O** (Pin function right after reset)

Pin Name	Type	Cell Type	Pin No.	Description
CM2HREF	I/O	BLNS4D1	U3	This pin has the following functions: • **CM2HREF: Horizontal sync input at camera 2 data input** This pin, when reset, becomes good for inputting GPIOF5. To use as the CM2HREF pin, set bits [11:10] of the GPIOF pin function register to “Function 1 other than GPIO.” • **IPC2HREF: Horizontal sync input at Interlaced camera 2 data input** This pin, when reset, becomes good for inputting GPIOF5. To use as the IPC2HREF pin, set bits [3:2] of the GPIOF pin function register to “Function 2 of other than GPIO.” • **GPIOF5 I/O** (Pin function right after reset)
CM2CLKOUT	I/O	BLNS4D1	W3	This pin has the following functions: • **CM2CLKOUT: Basic clock output for camera 2** This pin, when reset, becomes good for inputting GPIOF6. To use as the CM2CLKOUT pin, set bits [13:12] of the GPIOF pin function register to “Function 1 other than GPIO.” • **IPC2FIELD: Field identification signal for Interlaced camera 2** This pin, when reset, becomes good for inputting GPIOF6. To use as the IPC2FIELD pin, set bits [5:4] of the GPIOF pin function register to “Function 2 of other than GPIO.” • **GPIOF6 I/O** (Pin function right after reset)
CM2CLKIN	I/O	BLNS4D1	W2	This pin has the following functions: • **CM2CLKIN: Pixel clock for inputting camera 2 data** This pin, when reset, becomes good for inputting GPIOF7. To use as the CM2CLKIN pin, set bits [15:14] of the GPIOF pin function register to “Function 1 other than GPIO.” • **IPC2CLKIN: Pixel clock for inputting Interlaced camera 2 data** This pin, when reset, becomes good for inputting GPIOF7. To use as the IPC2CLKIN pin, set bits [7:6] of the GPIOF pin function register to “Function 2 of other than GPIO.” • **GPIOF7 I/O** (Pin function right after reset)
CFCE2#	I/O	BLNC4U1	M15	This pin has the following functions: • **CFCE2#: Card enable 2 (CE2#) output** (active low signal) **for Compact Flash Memory Interface (hereafter referred to as CF)** This pin, when reset, becomes good for inputting GPIOH0. To use as the CFCE2# pin, set bits [1:0] of the GPIOH pin function register to “Function 1 of other than GPIO.” • **GPIOH0 I/O** (Pin function right after reset) • **SDMDATA0: Data I/O 0 for SD card** (Pin Function 2 of other than GPIO)

Pin Name	Type	Cell Type	Pin No.	Description
CFCE1#	I/O	BLNC4U1	M17	This pin has the following functions: • **CFCE1#: Card Enable 1 (CE1#) Output for CF** (Active low signal) This pin, when reset, becomes good for inputting GPIOH1. To use as the CFCE1# pin, set bits [3:2] of the GPIOH pin function register to “Function 1 of other than GPIO.” • **GPIOH1 I/O** (Pin function right after reset) • **SDMDATA1: Data I/O 1 for SD card** (Pin Function 2 of other than GPIO)
CFIORD#	I/O	BLNC4U1	M18	This pin has the following functions: • **CFIORD#: IO read strobe output for CF** (Active low signal) This pin, when reset, becomes good for inputting GPIOH2. To use as the CFIORD# pin, set bits [5:4] of the GPIOH pin function register to “Function 1 other than GPIO.” • **GPIOH2 I/O** (Pin function right after reset) • **SDMDATA2: Data I/O 2 for SD card** (Pin Function 2 of other than GPIO)
CFIOWR#	I/O	BLNC4U1	M19	This pin has the following functions: (Active low signal) • **CFIOWR#: IO write strobe output for CF** This pin, when reset, becomes good for inputting GPIOH3. To use as the CFIOWR# pin, set bits [7:6] of the GPIOH pin function register to “Function 1 other than GPIO.” • **GPIOH3 I/O** (Pin function right after reset) • **SDMDATA3: Data I/O 3 for SD card** (Pin Function 2 of other than GPIO)
CFWAIT#	I/O	BLNC4U1	L16	This pin has the following functions: • **CFWAIT#: Wait request input for CF** (active low signal) This pin, when reset, becomes good for inputting GPIOH4. To use as the CFWAIT# pin, set bits [9:8] of the GPIOH pin function register to “Function 1 other than GPIO.” • **GPIOH4 I/O** (Pin function right after reset) • **SDMCMD: Command I/O for SD card** (Function 2 of other than GPIO)
CFRST	I/O	BLNC4U1	L17	This pin has the following functions: • **CFRST: Reset signal to CF card** The signal is HIGH when the card is reset and LOW when the card is under normal operation. This pin, when reset, becomes good for inputting GPIOH5. To use as the CFRST pin, set bits [11:10] of the GPIOH pin function register to “Function 1 other than GPIO.” • **GPIOH5 I/O** (Pin function right after reset) • **SDMCLK: Clock output for SD card** (Function 2 of other than GPIO)

Pin Name	Type	Cell Type	Pin No.	Description
CFIRQ	I/O	BLNC4U1	L19	This pin has the following functions: • **CFIRQ: Interrupt request signal from CF card** This pin, when reset, becomes good for inputting GPIOH6. To use as the CFIREQ pin, set bits [13:12] of the GPIOH pin function register to "Function 1 other than GPIO." • **GPIOH6 I/O** (Pin function right after reset) • **SDMCD#: Card detect input for SD card** (Function 2 of other than GPIO)
CFSTSCHG#	I/O	BLNC4U1	K19	This pin has the following functions: • **CFSTSCHG#: Status change signal from CF card** (active low signal) This pin, when reset, becomes good for inputting GPIOH7. To use as the CFSTSCHG# pin, set bits [15:14] of the GPIOH pin function register to "Function 1 other than GPIO." • **GPIOH7 I/O** (Pin function right after reset) • **SDMWP: Write protect input for SD card** (Function 2 of other than GPIO)
CFDEN#	I/O	BLNC4U1	K16	This pin has the following functions: • **CFDEN#: Data bus enable signal for external buffer of CF card** (active low signal) This pin, when reset, becomes good for inputting GPIOI0. To use as the CFDEN# pin, set bits [1:0] of the GPIOI pin function register to "Function 1 other than GPIO." • **GPIOI0 I/O pin** (Pin function right after reset) • **SDMGPO: General-purpose output for SD card** (Function 2 of other than GPIO)
CFDDIR	I/O	BLNC4U1	K17	This pin has the following functions: • **CFDDIR: Data bus directional instruction output for CF** When CF data is read, this pin becomes Low. Also, this pin, when reset, becomes good for inputting GPIOI1. To use as the CFDDIR pin, set bits [3:2] of the GPIOI pin function register to "Function 1 other than GPIO." • **GPIOI1 I/O** (Pin function right after reset)
R1	I	LLIN	A17	USB Device internal operation setting pin
DM	I/O	USBDM	A15	USB Device D- I/O
DP	I/O	USBDP	A14	USB Device D+ I/O
VBUS	I	USBVBUS	C14	USB Device VBUS input
ADIN[7:0]	I	HLIN	V6,W6, V7,W7, V8,W8, V9,W9	Analog signal input
GPIOA0	I/O	BLNS4	D17	This pin has the following functions: • **GPIOA0 I/O** (Pin function right after reset) • **TXD1: UART1 transmit data output** (Function 1 of other than GPIO)
GPIOA1	I/O	BLNS4	D19	This pin has the following functions: • **GPIOA1 I/O** (Pin function right after reset) • **RXD1: UART1 receive data input** (Function 1 of other than GPIO)
GPIOA2	I/O	BLNS4	D15	This pin has the following functions: • **GPIOA2 I/O** (Pin function right after reset) • **RTS1: UART1 request to send output** (Function 1 of other than GPIO)

Pin Name	Type	Cell Type	Pin No.	Description
GPIOA3	I/O	BLNS4	E17	This pin has the following functions: • **GPIOA3 I/O** (Pin function right after reset) • **CTS1: UART1 clear to send input** (Function 1 of other than GPIO)
GPIOA4	I/O	BLNS4	D16	This pin has the following functions: • **GPIOA4 I/O** (Pin function right after reset) • **TXD2: UART2 transmit data output** (Function 1 of other than GPIO)
GPIOA5	I/O	BLNS4	E19	This pin has the following functions: • **GPIOA5 I/O** (Pin function right after reset) • **RXD2: UART2 receive data input** (Function 1 of other than GPIO)
GPIOA6	I/O	BLNS4	F17	This pin has the following functions: • **GPIOA6 I/O** (Pin function right after reset) • **RTS2: UART2 request to send output** (Function 1 of other than GPIO) • **SCL: I^2C clock I/O** (Function 2 of other than GPIO)
GPIOA7	I/O	BLNS4	F19	This pin has the following functions: • **GPIOA7 I/O** (Pin function right after reset) • **CTS2: UART2 clear to receive input** (Function 1 of other than GPIO) • **SDA: I^2C data I/O** (Function 2 of other than GPIO)
GPIOB0	I/O	BLNS4	E16	This pin has the following functions: • **GPIOB0 I/O** (Pin function right after reset) • **INT0 input** • **I^2S_WS: Word select for I^2S** (Function 1 of other than GPIO)
GPIOB1	I/O	BLNS4	E15	This pin has the following functions: • **GPIOB1 I/O** (Pin function right after reset) • **INT1 input** • **I^2S_SCK: Serial clock for I^2S** (Function 1 of other than GPIO)
GPIOB2	I/O	BLNS4	F16	This pin has the following functions: • **GPIOB2 I/O** (Pin function right after reset) • **INT2 input** • **I^2S_SDO: Serial data output for I^2S** (Function 1 of other than GPIO)
GPIOB3	I/O	BLNS4	E14	This pin has the following functions: • **GPIOB3 I/O** (Pin function right after reset) • **INT3 input** • **I^2S_SDI: Serial data input for I^2S** (Function 1 of other than GPIO)
GPIOB4	I/O	BLNS4	G19	This pin has the following functions: • **GPIOB4 I/O** (Pin function right after reset) • **INT4 input** • **TimerA0Out** (Function 1 other than GPIO)
GPIOB5	I/O	BLNS4	G17	This pin has the following functions: • **GPIOB5 I/O** (Pin function right after reset) • **INT5 input** • **TimerA1Out** (Function 1 other than GPIO) • **DREQ#** (Function 2 other than GPIO)
GPIOB6	I/O	BLNS4	H17	This pin has the following functions: • **GPIOB6 I/O** (Pin function right after reset) • **INT6 input** • **TimerA2Out** (Function 1 other than GPIO)

Pin Name	Type	Cell Type	Pin No.	Description
GPIOB7	I/O	BLNS4	H19	This pin has the following functions: • **GPIOB7 I/O** (Pin function right after reset) • **INT7 input** • **TimerBIn** (Function 1 other than GPIO)
GPIOC0	I/O	BLNS4	H16	This pin has the following functions: • **GPIOC0 I/O** (Pin function right after reset) • **TimerB0IO** (Function 1 other than GPIO)
GPIOC1	I/O	BLNS4	G15	This pin has the following functions: • **GPIOC1 I/O** (Pin function right after reset) • **TimerB1IO** (Function 1 other than GPIO) • **DACK#** (Function 2 other than GPIO)
GPIOC2	I/O	BLNS4	J19	This pin has the following functions: • **GPIOC2 I/O** (Pin function right after reset) • **TimerB2IO** (Function 1 other than GPIO) • **CFRST#** (Function 2 other than GPIO)
GPIOC3	I/O	BLNS4	J18	This pin has the following functions: • **GPIOC3 I/O** (Pin function right after reset) • **TimerB3IO** (Function 1 other than GPIO) • **UART3_CLK** (Function 2 of other than GPIO)
GPIOC4	I/O	BLNS4	J17	This pin has the following functions: • **GPIOC4 I/O** (Pin function right after reset) • **SPI_SS: Chip select for SPI** (Function 1 of other than GPIO) • **TXD3: UART3 transmit data output** (Function 2 of other than GPIO)
GPIOC5	I/O	BLNS4	J16	This pin has the following functions: • **GPIOC5 I/O** (Pin function right after reset) • **SPI_SCLK: Serial clock for SPI** (Function 1 of other than GPIO) • **RXD3: UART3 receive data input** (Function 2 of other than GPIO)
GPIOC6	I/O	BLNS4	H15	This pin has the following functions: • **GPIOC6 I/O** (Pin function right after reset) • **SPI_MISO: Serial data master input/slave output for SPI** (Function 1 of other than GPIO) • **RTS3: UART3 request to send output** (Function 2 of other than GPIO)
GPIOC7	I/O	BLNS4	J15	This pin has the following functions: • **GPIOC6 I/O** (Pin function right after reset) • **SPI_MOSI: Serial data master output/slave input for SPI** (Function 1 of other than GPIO) • **CTS3: UART3 clear to receive input** (Function 2 of other than GPIO)
GPIOD[3:0]	I/O	BLNS4	U9,T8, T9,U10	This pin has the following functions: • **GPIOD [3:0] I/O** (Pin function right after reset) • **MA [23:20]: Address output signal [23:20]** (Function 1 of other than GPIO)
GPIOD[5:4]	I/O	BLNS4	V15,R16	This pin has the following functions: • **GPIOD [5:4] I/O** (Pin function right after reset) • **MCS [3:2]#: Chip select output signal for memory** (Function 1 of other than GPIO)
GPIOD6	I/O	BLNS4	V1	This pin has the following functions: • **GPIOD6 I/O** (Pin function right after reset) • **DQM2# signal for SDRAM** (active low signal) • **SDDQM2#: Corresponds to the lower byte of the higher 16 bits of SDRAM 32-bit data width** (Function 1 of other than GPIO)

Pin Name	Type	Cell Type	Pin No.	Description
GPIOD7	I/O	BLNS4	T4	This pin has the following functions: • **GPIOD7 I/O** (Pin function right after reset) • **DQM3# signal for SDRAM** (active low signal) • **SDDQM3##: Corresponds to the higher byte of the higher 16 bits of SDRAM 32-bit data width** (Function 1 of other than GPIO)
GPIOJ[7:0]	I/O	BLNS4	J4,L2, L4,J5, L3,M2, M3,M1	This pin has the following functions: • **GPIOJ [7]0] I/O** (Pin function right after reset) • **SDD [23:16]: Data I/O for SDRAM** (Function 1 of other than GPIO)
GPIOK[7:0]	I/O	BLNS4	G1,G2, E6,E7, G3,H3, F5,G4	This pin has the following functions: • **GPIOK [7]0] I/O** (Pin function right after reset) • **SDD [31:24]: Data I/O for SDRAM** (Function 1 of other than GPIO)
SYSCLKI	I	BLNS4	A10	**32kHz system clock input** Basic clock input when SYSCKSEL is “HIGH”. 1/8 of 32KHz or system clock becomes output when SYSCKSEL is “LOW”.
SYS_OSCI	I	LLIN	A6	**Connection pin for crystal transducer** This is an operation clock oscillator pin. It connects a 32kHz crystal transducer.
SYS_OSCO	O	LLOT	A5	**Connection pin for crystal transducer** This is an operation clock oscillator pin. It connects a 32kHz crystal transducer.
SYSVCP	O	LLOT	A9	**System test pin for built-in PLL** This pin is used to monitor outputs of the PLL at the time of system test. Make the pin open at the time of normal operation.
SYSCKSEL	I	ICSD1	B10	**32kHz system clock input crystal transducer/oscillator select signal** Crystal oscillator is used when SYSCKSEL is “HIGH”. Crystal transducer is used when SYSCKSEL is “LOW”.
USBCK_OSCI	I	LLIN	C19	**Connection pin for crystal oscillator** This is an operation clock oscillator pin specifically for USB. It connects a 12/24MHz crystal transducer.
USBCK_OSCO	O	LLOT	B19	**Connection pin for crystal transducer** This is an operation clock oscillator pin specifically for USB. It connects a 12/24MHz crystal transducer.
TRST#	I	ICSU1	B11	**Resetting for JTAG Interface** (active low signal) This signal is to be input with a Schmitt trigger with pull-up resistor.
TCK	I	ICSU1	D11	**Clock Input Pin for JTAG Interface** This clock is to be input with a Schmitt trigger.
TMS	I	ICU1	D12	**TMS Pin for JTAG Interface** This pin has a built-in pull-up resistor.
TDI	I	ICU1	E13	**Serial Data Input Pin for JTAG Interface** This pin has a built-in pull-up resistor.
TDO	O	OTLN4	C12	**Serial Data Output Pin for JTAG Interface**
TESTEN0	I	ICD1	C11	**Test enable 0 (active high signal)** This pin has a built-in pull-down resistor. Connect this pin to Vss or make it open at the time of normal operation.
TESTEN1	I	ICD1	E10	**Test enable 1** (active high signal) This pin has a built-in pull-down resistor. Connect this pin to Vss or make it open at the time of normal operation.
TESTCK	I	ICD1	B12	**Test clock?**

Pin Name	Type	Cell Type	Pin No.	Description
RESET#	I	ICSU1	D13	**System reset signal** (active low signal) Even after HVDD1 and LVDD become stable, keep RESET# active (LOW) for 100ms.
BUP#	I	ICS	B8	**Backup signal** (active low signal) 1.8V I/O
HVDD	P	P	C9,C16, D14,E18, G16,H18, L15,R10, R15,W12, W15	**Power supply for I/O cell :** 3.3V (Typical) 3.0V (Min.) - 3.6V (Max.)
C1VDD	P	P	A4	**Power supply for camera 1 interface:** 3.0 (Typical) 2.4V (Min.) - 3.6V (Max.)
C2VDD	P	P	W4	**Power supply for camera 2 interface:** 3.0 (Typical) 2.4V (Min.) - 3.6V (Max.)
SDVDD	P	P	C3,F2, K3,K4, P1	**Power supply for SDRAM:** 3.3V (Typical) 2.7V (Min.) - 3.6V (Max.)
AVDD	P	P	V5,W5, W10	**Power supply for A/D C:** 3.3V (Typical) 3.0V (Min.) - 3.6V (Max.)
UVDD3	P	P	A16,B14	**Power supply for USB:** 3.3V (Typical) 3.0V (Min.) - 3.6V (Max.)
LVDD	P	P	A11,D10, D18,E1, E12,F15, F18,H1, K15,K18, L5,P19, T2,V18, W14	**Power supply for core (internal):** 1.8V (Typical) 1.65V (Min.) - 1.95V (Max.)
UPVDD	P	P	A18	**Power supply for USB:** 1.8V (Typical) 1.65V (Min.) - 1.95V (Max.)
UXVDD	P	P	A13	**Power supply for USB:** 1.8V (Typical) 1.65V (Min.) - 1.95V (Max.)
PLLVDD	P	P	B9	**Power supply for analog (PLL):** 1.8V (Typical) 1.65V (Min.) - 1.95V (Max.) Handling as an analog power supply is required. Supply stable power that generates less noise.
RTCVDD	P	P	A7	**Power supply for RTC:** 1.8V (Typical) 1.65V (Min) – 1.95V (Max)
UVSS	P	P	B15,B17	**Ground for USB**
PVSS	P	P	B18	**Ground for USB**
XVSS	P	P	B13	**Ground for USB**
AVSS	P	P	U6,V10	**Ground for A/D C**
PLLVSS	P	P	A8	**Ground for analog (PLL)** Handling as an analog power supply is required. Supply stable ground that generates less noise.

Pin Name	Type	Cell Type	Pin No.	Description
Vss	P	P	A12,B4, B7,B16, C2,C8, C10,C13, C15,C17, C18,E2, E4,E8, E11,G5, G18,H2, K5,L1, L18,M5, N2,N17, P5,R9, R18,T1, T14,U4, U16,V2, V13,V19	**Ground common to I/O cell, camera interface, and core power supplies**

3.3 Multiplex Pin Function of GPIO Pins, Pin Function Right after Reset

S2S65A30 Signal name	Fuction after reset	FlashROM/ SAM (enhancing)	SDRAM (enhancing)	UART	I2C/ I2S/ SPI	Timer	Progressivec camera I/F	Interlace camera I/F	CF card	SD card
GPIOA0	GPIOA0			TXD1						
GPIOA1	GPIOA1			RXD1						
GPIOA2	GPIOA2			RTS1	I2S1_WS					
GPIOA3	GPIOA3			CTS1	I2S1_SCK					
GPIOA4	GPIOA4			TXD2						
GPIOA5	GPIOA5			RXD2						
GPIOA6	GPIOA6			RTS2	SCL					
GPIOA7	GPIOA7			CTS2	SDA					
GPIOB0	GPIOB0				I2S0_WS					
GPIOB1	GPIOB1				I2S0_SCK					
GPIOB2	GPIOB2				I2S0_SD					
GPIOB3	GPIOB3				I2S1_SD					
GPIOB4	GPIOB4					TimerA0out				
GPIOB5	GPIOB5	DREQ#				TimerA1out				
GPIOB6	GPIOB6					TimerA2out				
GPIOB7	GPIOB7					TimerBIN				
GPIOC0	GPIOC0					TimerB0IO				
GPIOC1	GPIOC1	DACK#				TimerB1IO				
GPIOC2	GPIOC2					TimerB2IO			CFRST	
GPIOC3	GPIOC3			UART3_CLK		TimerB3IO				
GPIOC4	GPIOC4			TXD3	SPI_SS					
GPIOC5	GPIOC5			RXD3	SPI_SCLK					
GPIOC6	GPIOC6			RTS3	SPI_MISO					
GPIOC7	GPIOC7			CTS3	SPI_MOSI					
GPIOD0	GPIOD0	MA20								
GPIOD1	GPIOD1	MA21								
GPIOD2	GPIOD2	MA22								
GPIOD3	GPIOD3	MA23								
GPIOD4	GPIOD4	MCS2#								
GPIOD5	GPIOD5	MCS3#								
GPIOD6	GPIOD6		SDDQM2#							
GPIOD7	GPIOD7		SDDQM3#							
CM1DATA0	GPIOE0						CM1DATA0	IPC1DATA0		
CM1DATA1	GPIOE1						CM1DATA1	CM1DATA1		
CM1DATA2	GPIOE2						CM1DATA2	IPC1DATA2		
CM1DATA3	GPIOE3						CM1DATA3	IPC1DATA3		
CM1DATA4	GPIOE4						CM1DATA4	IPC1DATA4		
CM1DATA5	GPIOE5						CM1DATA5	IPC1DATA5		
CM1DATA6	GPIOE6						CM1DATA6	IPC1DATA6		
CM1DATA7	GPIOE7						CM1DATA7	IPC1DATA7		
CM1VREF	GPIOF0						CM1VREF	IPC1VREF		
CM1HREF	GPIOF1						CM1HREF	IPC1HREF		
CM1CLKOUT	GPIOF2						CM1CLKOUT	IPC1FIELD		
CM1CLKIN	GPIOF3						CM1CLKIN	IPC1CLKIN		
CM2VREF	GPIOF4						CM2VREF	IPC2VREF		
CM2HREF	GPIOF5						CM2HREF	IPC2HREF		
CM2CLKOUT	GPIOF6						CM2CLKOUT	IPC2FIELD		
CM2CLKIN	GPIOF7						CM2CLKIN	IPC2CLKIN		
CM2DATA0	GPIOG0						CM2DATA0	IPC2DATA0		
CM2DATA1	GPIOG1						CM2DATA1	IPC2DATA1		
CM2DATA2	GPIOG2						CM2DATA2	IPC2DATA2		
CM2DATA3	GPIOG3						CM2DATA3	IPC2DATA3		
CM2DATA4	GPIOG4						CM2DATA4	IPC2DATA4		
CM2DATA5	GPIOG5						CM2DATA5	IPC2DATA5		
CM2DATA6	GPIOG6						CM2DATA6	IPC2DATA6		
CM2DATA7	GPIOG7						CM2DATA7	IPC2DATA7		

S2S65A30 Signal name	Fuction after reset	FlashROM/ SAM (enhancing)	SDRAM (enhancing)	UART	I2C/ I2S/ SPI	Timer	Progressivec camera I/F	Interlace camera I/F	CF card	SD card
CFCE2#	GPIOH0								CFCE2#	SDMDATA0
CFCE1#	GPIOH1								CFCE1#	SDMDATA1
CFIORD#	GPIOH2								CFIORD#	SDMDATA2
CFIOWR#	GPIOH3								CFIOWR#	SDMDATA3
CFWAIT#	GPIOH4								CFWAIT#	SDMCMD
CFRST	GPIOH5								CFRST	SDMCLK
CFIRQ	GPIOH6								CFIRQ	SDMCD#
CFSTSCHG#	GPIOH7								CFSTSCHG#	SDMWP
CFDEN#	GPIOI0								CFDEN#	SDMGPO
CFDDIR	GPIOI1								CFDDIR	
GPIOJ0	GPIOJ0		SDD16							
GPIOJ1	GPIOJ1		SDD17							
GPIOJ2	GPIOJ2		SDD18							
GPIOJ3	GPIOJ3		SDD19							
GPIOJ4	GPIOJ4		SDD20							
GPIOJ5	GPIOJ5		SDD21							
GPIOJ6	GPIOJ6		SDD22							
GPIOJ7	GPIOJ7		SDD23							
GPIOK0	GPIOK0		SDD24							
GPIOK1	GPIOK1		SDD25							
GPIOK2	GPIOK2		SDD26							
GPIOK3	GPIOK3		SDD27							
GPIOK4	GPIOK4		SDD28							
GPIOK5	GPIOK5		SDD29							
GPIOK6	GPIOK6		SDD30							
GPIOK7	GPIOK7		SDD31							

Function 1 : Function 1 Function 2 : Function 2

3.4 Pin Status during/after Reset

Pin Name	Direction during RESET	Value during RESET	Value after RESET	Presence of Internal Resistor	Description
MA[19:0]	Output	Low	—	No	
MD[15:0]	Input	Low	Low	Yes, Pull-down resistor	100kΩ
MCS[2:0]#	Output	High	—	No	
MBEL#	Output	High	—	No	
MBEH#	Output	High	—	No	
MOE#	Output	High	—	No	
MWE#	Output	High	—	No	
SDA[14:0]	Output	Low	—	No	
SDD[15:0]	Input	Low	—	Yes, Pull-down resistor	100kΩ
SDCS[1:0]#	Output	High	—	No	
SDWE#	Output	High	—	No	
SDCLK	Output	Low	—	No	
SDLKEN	Output	Low	—	No	
SDRAS#	Output	High	—	No	
SDCAS#	Output	High	—	No	
SDDQM[1:0]#	Output	Low	—	No	
CM1DATA[7:0]	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM1VREF	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM1HREF	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM1CLKOUT	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM1CLKIN	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM2DATA[7:0]	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM2VREF	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM2HREF	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM2CLKOUT	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CM2CLKIN	Input	Low	Low	Yes, Pull-down resistor	50kΩ
CFCE2#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFCE1#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFIORD#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFIOWR#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFWAIT#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFRST	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFIREQ	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFSTSCHG#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFDEN#	Input	High	High	Yes, Pull-Up resistor	50kΩ
CFDDIR	Input	High	High	Yes, Pull-Up resistor	50kΩ
GPIOA[7:0]	Input	High-Z	High-Z	No	Depends on the external circuits
GPIOB[7:0]	Input	High-Z	High-Z	No	Depends on the external circuits
GPIOC[7:0]	Input	High-Z	High-Z	No	Depends on the external circuits
GPIOD[7:0]	Input	High-Z	High-Z	No	Depends on the external circuits
GPIOJ[7:0]	Input	High-Z	High-Z	Yes, Pull-down resistor	100kΩ
GPIOK[7:0]	Input	High-Z	High-Z	Yes, Pull-down resistor	100kΩ
SYSCLKI	Input	High-Z	High-Z	No	
SYSVCP	Output	High-Z	High-Z	No	Leave this pin Open when it is used
SYSCKSEL	Input	Low	Low	Yes, Pull-down resistor	50kΩ
TRST#	Input	High	High	Yes, Pull-Up resistor	50kΩ
TCK	Input	High-Z	High-Z	Yes, Pull-Up resistor	50kΩ
TMS	Input	High	High	Yes, Pull-Up resistor	50kΩ
TDI	Input	High	High	Yes, Pull-Up resistor	50kΩ
TDO	Output	High-Z	High-Z	No	
TESTEN0	Input	Low	Low	Yes, Pull-down resistor	50kΩ
TESTEN1	Input	Low	Low	Yes, Pull-down resistor	50kΩ
TESTCK	Input	Low	Low	Yes, Pull-down resistor	50kΩ
RESET#	Input	Low	High	No	

4. ABSOLUTE MAXIMUM RATINGS

4.1 Absolute Maximum Ratings

(VSS = 0 [V])

Item	Symbol	Rated Value	Unit
Power voltage	HVDD*	-0.3 to 4.0	V
	LVDD*	-0.3 to 2.5	V
Input voltage	HVI	-0.3 to HVDD+0.5	V
	LVI	-0.3 to LVDD+0.5	V
Output voltage	HVO	-0.3 to HVDD+0.5	V
	LVO	-0.3 to LVDD+0.5	V
Output current/pin	I_{OUT}	± 10	mA
Storage temperature	T_{stg}	-65 to 150	°C

*: HVDD ≥ LVDD

4.2 Recommended Operating Conditions (Dual Power Supplies, 3.3V I/O Buffers)

(VSS = PLLVSS = 0 [V])

Item		Symbol	Min.	Typ.	Max.	Unit
Power voltage (High-voltage)	I/O cell power supply	HVDD	3.00	3.30	3.60	V
	USB power supply	UVDD3	3.00	3.30	3.60	V
	Camera-1 I/F power supply	C1VDD	2.40	3.00	3.60	V
	Camera-2 I/F power supply	C2VDD	2.40	3.00	3.60	V
	SDRAM I/F power supply	SDVDD	2.70	3.00	3.60	V
	A/D converter power supply	AVDD	3.00	3.30	3.60	V
Power voltage (Low-voltage)	(Internal) core power supply	LVDD	1.65	1.80	1.95	V
	USB power supply	UPVDD	1.65	1.80	1.95	V
	USB power supply	UXVDD	1.65	1.80	1.95	V
	Analog (PLL) power supply	PLLVDD	1.65	1.80	1.95	V
	RTC power supply	RTCVDD	1.65	1.80	1.95	V
Input voltage	I/O cell power supply	HV_I	VSS	—	HVDD	V
	USB power supply	$UV3_I$	UVSS	—	UVDD3	
	Camera-1 I/F power supply	$C1V_I$	VSS	—	C1VDD	V
	Camera-2 I/F power supply	$C2V_I$	VSS	—	C2VDD	V
	SDRAM I/F power supply	SDV_I	VSS	—	SDVDD	V
	A/D converter power supply	AV_I	AVSS	—	AVDD	V
	(Internal) core power supply	LV_I	VSS	—	LVDD	V
	USB power supply	UPV_I	PVSS	—	UPVDD	V
	USB power supply	UXV_I	XVSS	—	UXVDD	V
	Analog (PLL) power supply	$PLLV_I$	PLLVSS	—	PLLVDD	V
	RTC power supply	$RTCV_I$	VSS		RTCVDD	V
Ambient temperature		Ta	-40	25	85*	°C
Input rise time (normal input)		t_{ri}	—	—	50	ns
Input fall time (normal input)		t_{fa}	—	—	50	ns
Input rise time (Schmitt input)		t_{ri}	—	—	5	ms
Input fall time (Schmitt input)		t_{fa}	—	—	5	ms

*: This temperature range is the recommended ambient temperature range if Tj=-40 to 125°C.

4.3 Power-ON Timing

The 3.3V power supply (HVDD1) and 1.8V power supply (LVDD) must be turned On in the following sequence.

(1) Turn on the power supply of the remainder within one second after turning on the power supply in one side. This interval is recommended to be shortened as much as possible.
(2) After the HVDD1 and LVDD signals have become stable, keep the RESET# signal in logical Low more than the 32kHz oscillation start time.

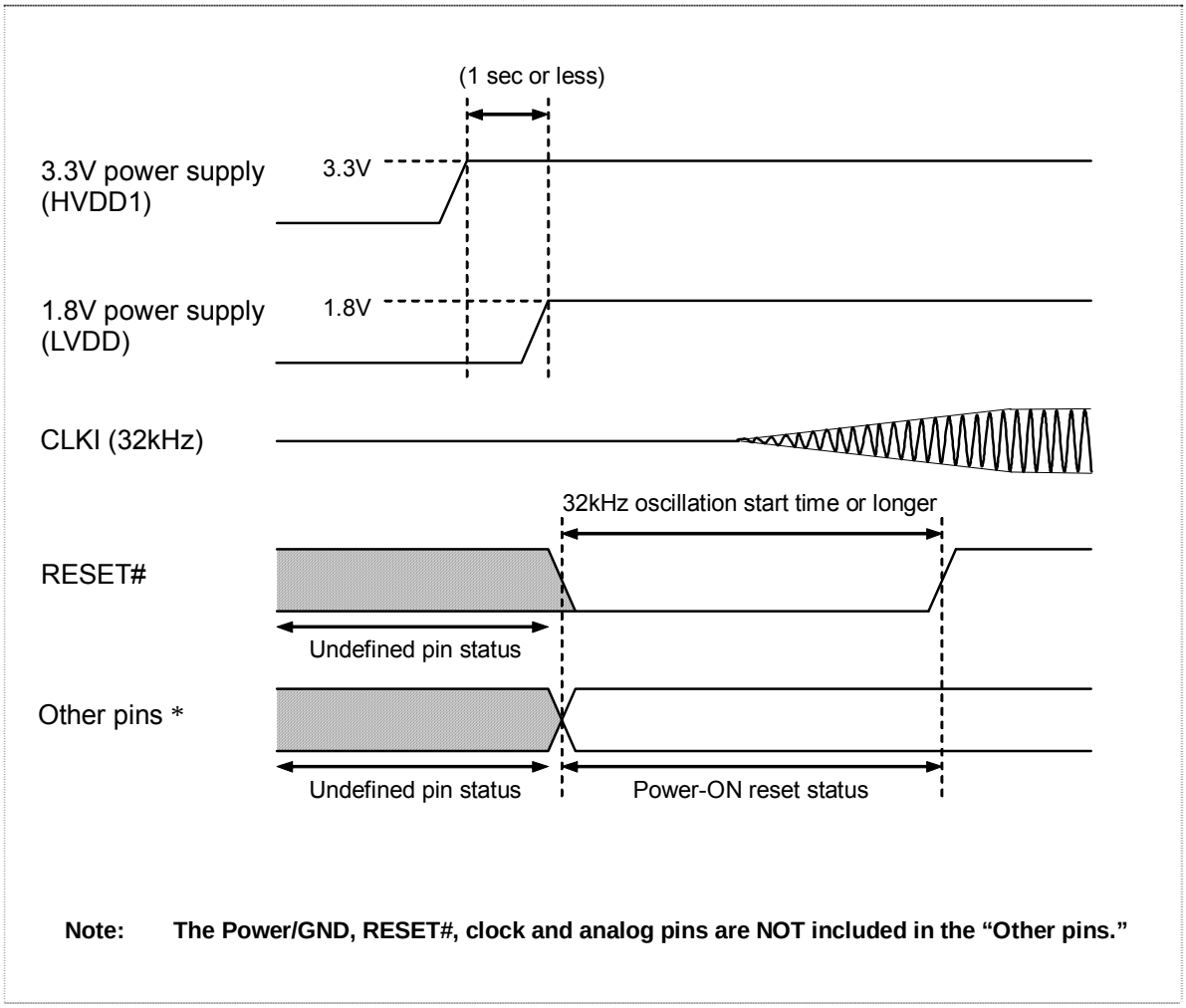


Figure 4.1 Power-ON Timing

4.4 Power-OFF Timing

The 3.3V power supply (HVDD1) and 1.8V power supply (LVDD) must be turned Off in the following sequence.

(1) Turn off the power supply of the remainder within one second after cutting the power supply in one side. This interval is recommended to be shortened as much as possible.
(2) If the 1.8V power supply is only turned Off, the pin status is unstable. You must design the system to avoid the system malfunction due to this unstable pin status.

5. ELECTRICAL CHARACTERISTICS

5.1 DC Characteristics

Table 5.1 DC Characteristics(3.3V)

(HVDD = 3.3V ± 0.3V, VSS = 0V, Ta= -40～85℃)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leak current	I_{LI}	—		-5	—	5	μA
Off-state leak current	I_{OZ}	—		-5	—	5	μA
High-level output voltage (*1)	V_{OH}	I_{OH} = -4mA HVDD=Min.		HVDD -0.4	—	—	V
Low-level output voltage (*1)	V_{OL}	I_{OL} = 4mA HVDD=Min.		—	—	0.4	V
High-level input voltage	V_{IH1}	LVCMOS level, HVDD=Max.		2.2	—	—	V
Low-level input voltage	V_{IL1}	LVCMOS level, HVDD=Min.		—	—	0.8	V
High-level input voltage	V_{T1+}	LVCMOS Schmitt input		1.4	—	2.7	V
Low-level input voltage	V_{T1-}	LVCMOS Schmitt input		0.6	—	1.8	V
Hysteresis voltage	V_{H1}	LVCMOS Schmitt input		0.3	—	—	V
High-level input voltage	V_{IH2}	LVTTL level, HVDD=Max.		2.0	—	—	V
Low-level input voltage	V_{IL2}	LVTTL level, HVDD=Min.		—	—	0.8	V
Pull-up resistance	P_{PU}	VI=0V		25	50	120	kΩ
Pull-down resistance	P_{PD}	VI=HVDD	Other pins *2	25	50	120	kΩ
			MD[15:0] pin	50	100	240	
Input pin capacity	C_I	f=1MHz, HVDD = 0V		—	—	8	pF
Output pin capacity	C_O	f=1MHz, HVDD = 0V		—	—	8	pF
Input and output pin capacity	C_{IO}	f=1MHz, HVDD = 0V		—	—	8	pF

*1: Applied to all output and I/O pins.
*2: The pin has pull-down resistance except for MD[15:0] pin.

Table 5.2 DC Characteristics(1.8V)

(RTCVDD = 1.8V ± 0.15V, VSS = 0V, Ta= -40～85℃)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leak current	I_{LI}	—	-5	—	5	μA
Off-state leak current	I_{OZ}	—	-5	—	5	μA
High-level input voltage	V_{T1+}	LVCMOS Schmitt input	0.6	—	1.4	V
Low-level input voltage	V_{T1-}	LVCMOS Schmitt input	0.3	—	1.1	V
Hysteresis voltage	V_{H1}	LVCMOS Schmitt input	0.02	—	—	V
Input pin capacity	C_I	f=1MHz, HVDD = 0V	—	—	8	pF

Table 5.3 USBVBUS Judgment voltage

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level triggrer voltage	VB_{TH}	UVDD3 = 3.6V	1.86	—	2.85	V
Low-level triggrer voltage	VB_{TL}	UVDD3 = 3.0V	1.48	—	2.23	V
Hysteresis voltage	VB_H	UVDD3 = 3.0V	0.31	—	0.64	V

Table 5.4 current consumption

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (LVDD)	I_{LOW}	Low-speed mode*1	—	180	—	µA
	I_{LOWh}	Low-speed HALT mode*2	—	155	—	µA
	I_{FO1}	High-speed mode 1*3	—	120	—	mA
	I_{FO2}	High-speed mode 2*4	—	95	—	mA
	I_{FO3}	High-speed mode 3*5	—	145	—	mA
Power consumption (PTCVDD)	I_{RTCO}	RTC Stand-alone Operations (BUP#=LOW)*6	—	1	—	µA
	I_{RTCH}	RTC Normal Operations (BUP#=HIGH)*7	—	450	—	µA
Current Consumption (PLLVDD)	I_{DDPLL}	PLL Frequency = 50.00MHz	—	1.8	—	µA
	I_{DDPD}	During PLL Power-down	—	1	—	µA

*1: When system is operated at 32KHz
*2: When the system is operated at 32KHz and the internal bus clock is stopped
*3: When two camera is connected and executed IP conversion and JPEG encode (30fps@VGA) and recorded on a SD memory
*4: When A JPEG file stored in an external SDRAM is being recorded on a SD memory with the camera interfaces and the JPEG controller being stopped.
*5: When two cameras are connected, and IP conversion and JPEG encoding (30fps@VGA) are executed and images are being displayed on a PC via a USB cable.
*6: Timekeeping on the RTC is active and other power supplies are shut down (Battery backup mode)
*7: The current consumption of RTC portion when the system is operated at 50 MHz.

6. EXTERNAL CONNECTION EXAMPLES (REFERENCE)

6.1 analog camera Connection Examples(Bt.656 mode)

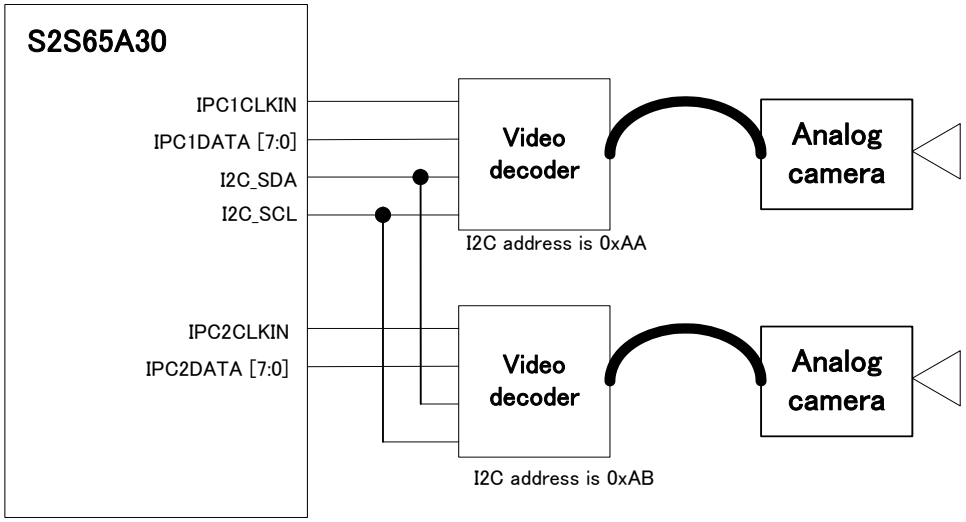


Figure 6.1 Analog camera connection example

6.2 Memory Connection Examples

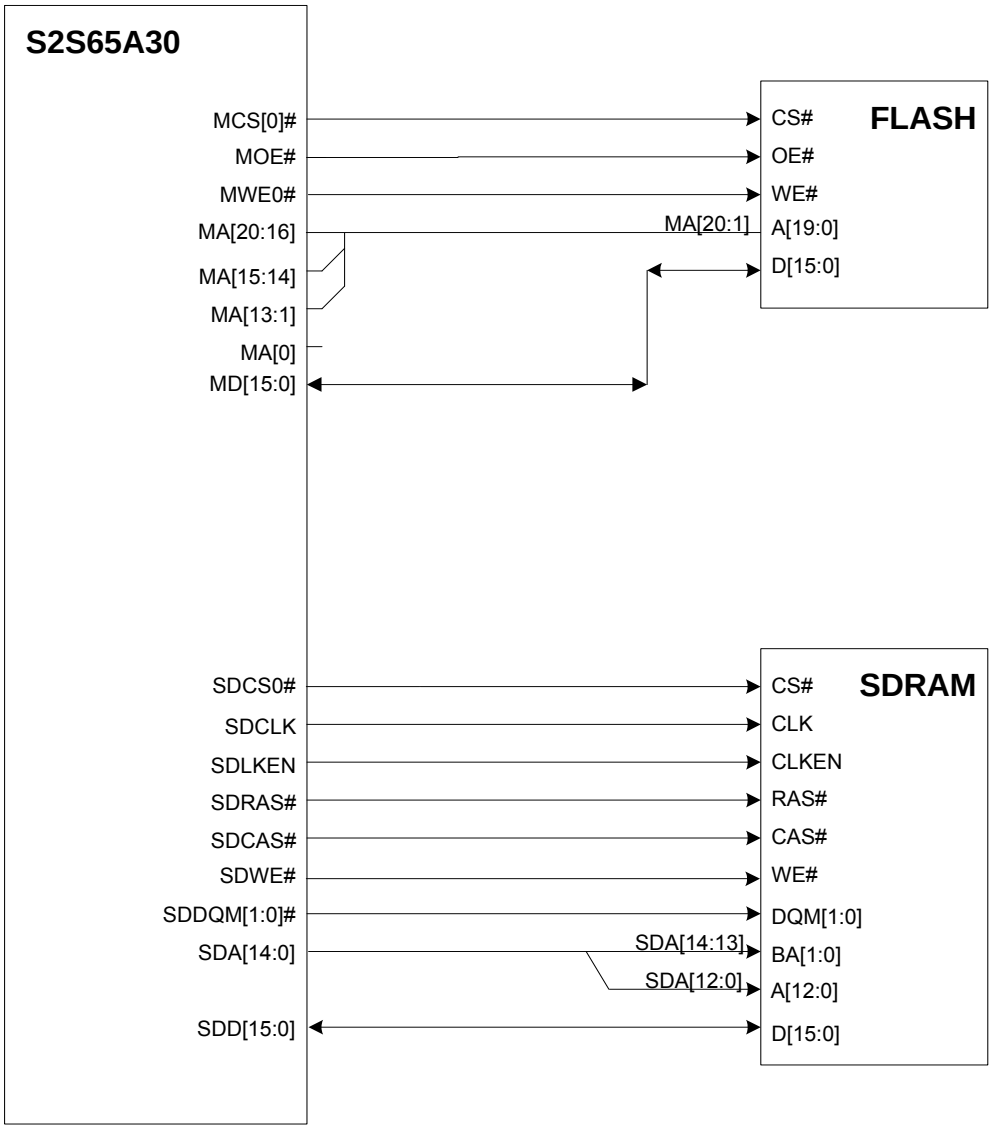


Figure 6.2 Memory Connection Example (1)

Note: Connect SDMA[14:13] to the SDRAM bank address (BA[1:0]).

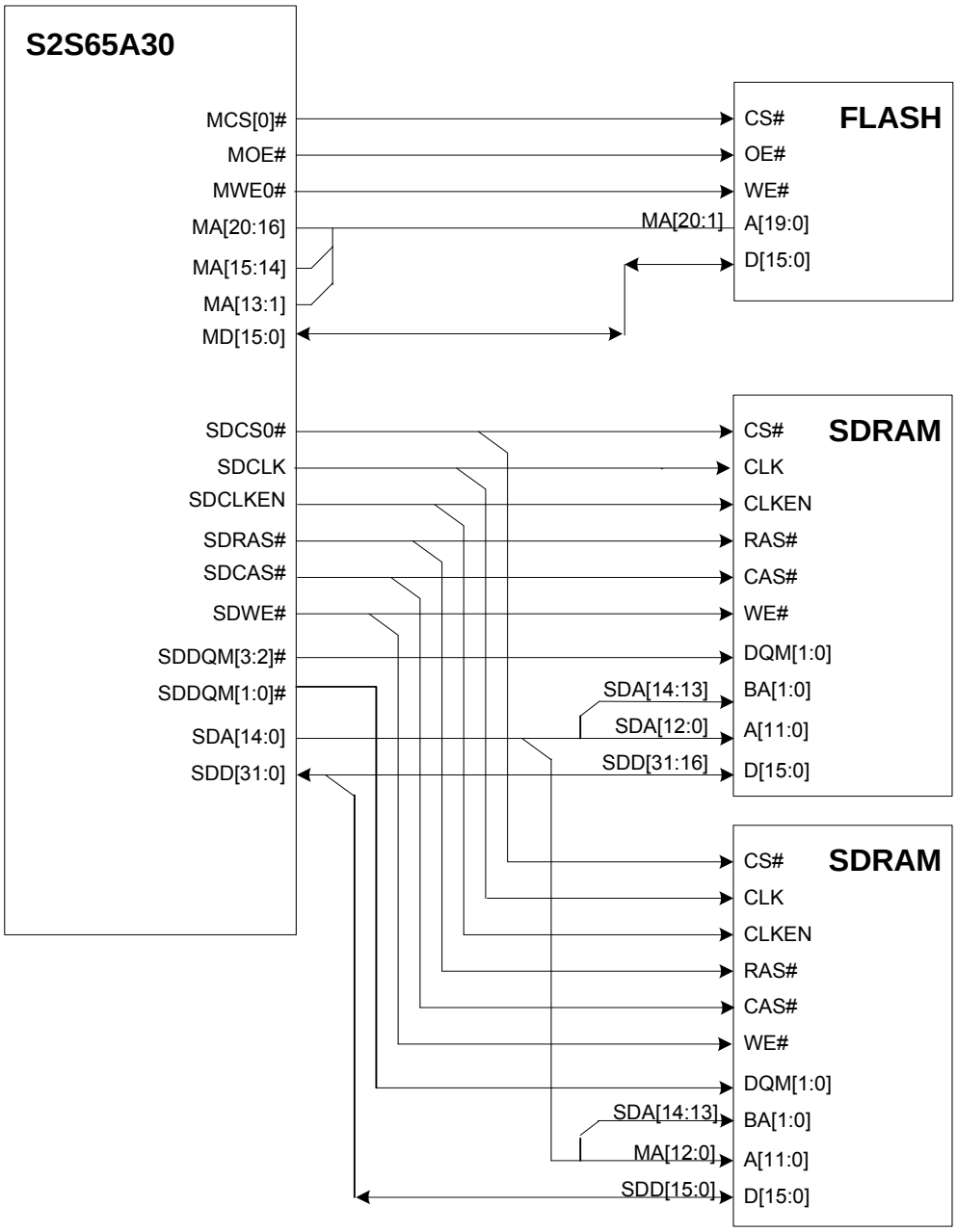


Figure 6.3 Memory Connection Example (2)

Note: Connect SDA[14:13] to the SDRAM bank address (BA[1:0]).

6.3 Compact Flash Memory Connection Example (for 16-Bit Bus Support Model)

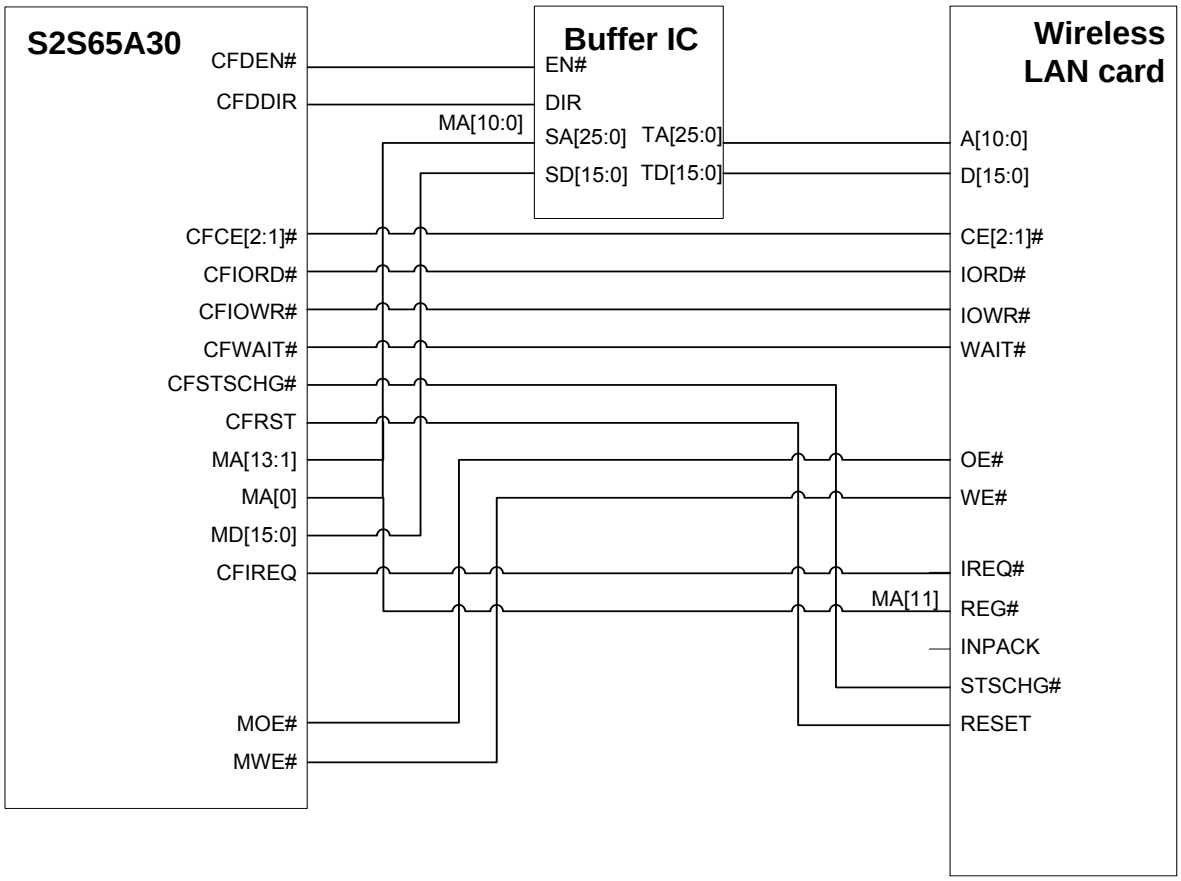
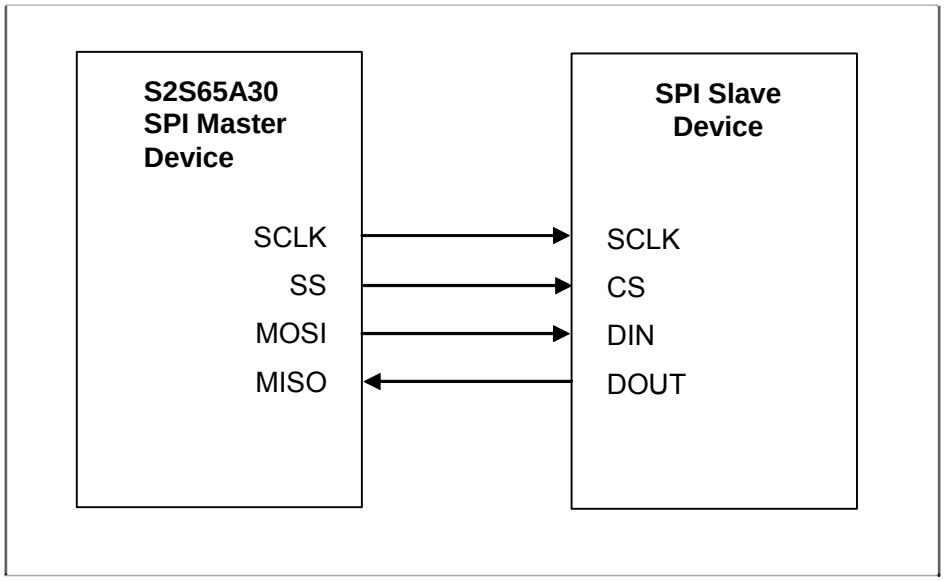


Figure 6.4 Compact Flash Memory I/F Connection Example

6.4 Serial Peripheral Device Interface (SPI) Connection Examples

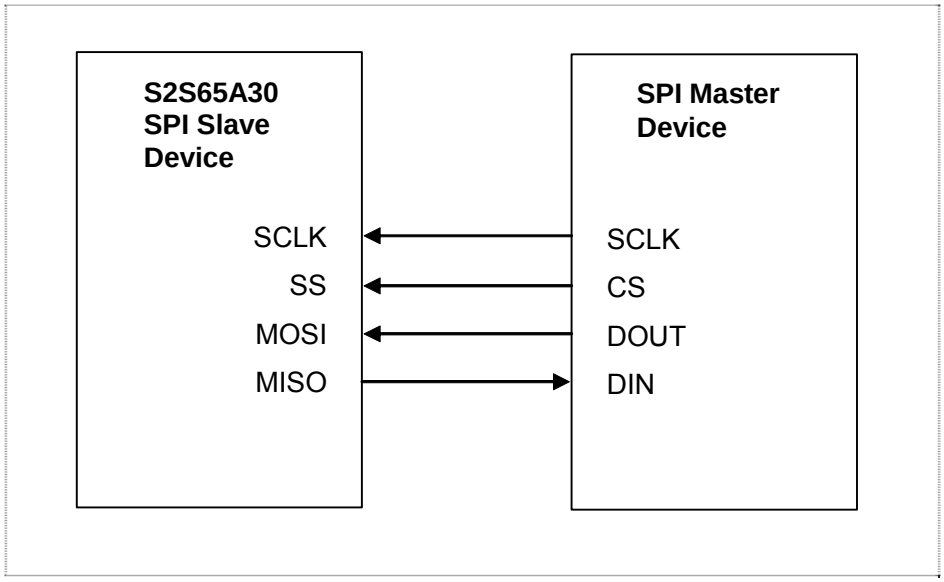
6.4.1 Master Mode

A connection example if S2S65A30 is used as master device



6.4.2 Slave Mode

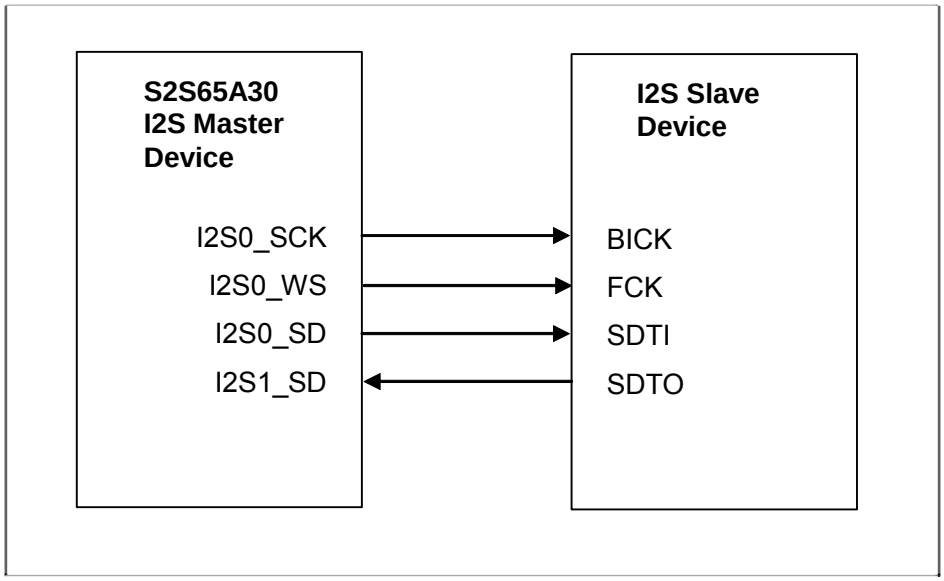
A connection example if S2S65A30 is used as slave device



6.5 I^2S Connection Examples

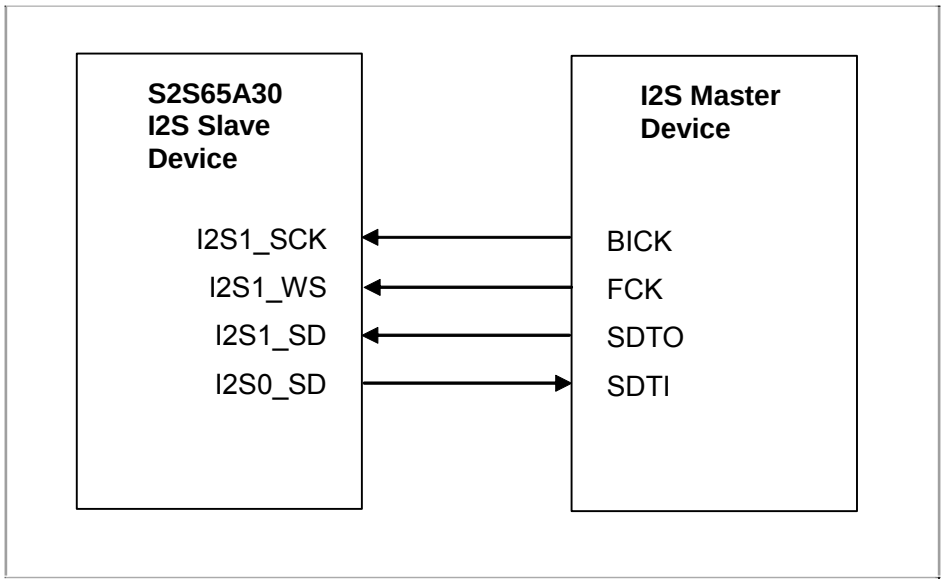
6.5.1 Master Mode

A connection example if S2S65A30 is used as master device



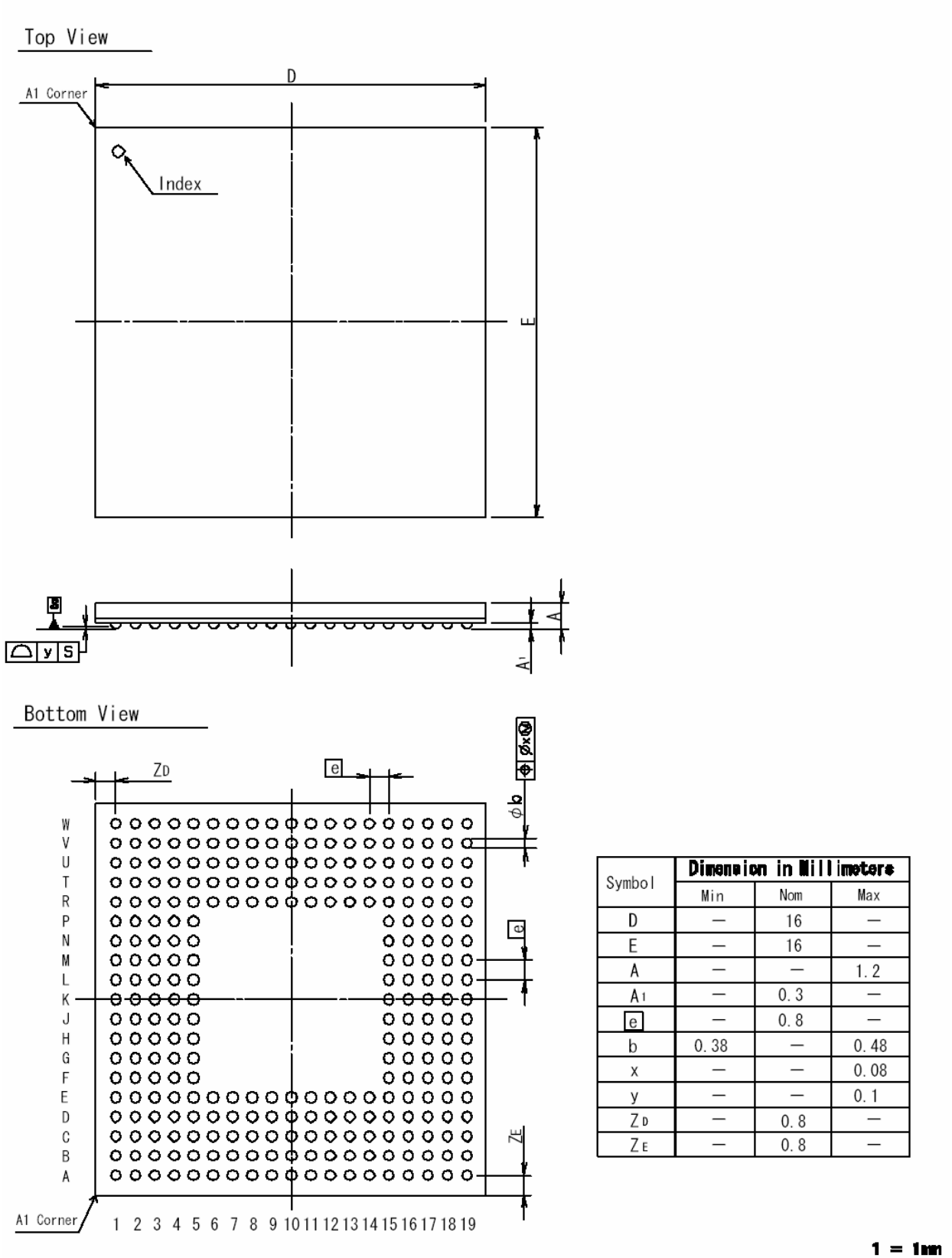
6.5.2 Slave Mode

A connection example if S2S65A30 is used as slave device



7. EXTERNAL DIMENSIONS

7.1 Plastic TFBGA 280pin Body size 16x16x1.2mm (PFBGA16U-280)



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	16	—
E	—	16	—
A	—	—	1.2
A_1	—	0.3	—
e	—	0.8	—
b	0.38	—	0.48
x	—	—	0.08
y	—	—	0.1
Z_D	—	0.8	—
Z_E	—	0.8	—

1 = 1mm

Figure 7.1 Package Dimensions (PFBGA16U-280PIN)

REVISION HISTORY

Revision	Date of Issue	Description		
		Revision data	Before revision	After revision
0.9	2009/06/01	First edition		
1.0	2009/08/26	Release		

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway,
San Jose, CA 95131, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, Block B, Hi-Tech Bldg., 900 Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road,
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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