S1C33L19

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CMOS 32-bit Application Specific Controller

- 32-bit RISC CPU-Core Optimized for SoC (EPSON S1C33 PE)
- Dual AMBA Bus System for CPU and LCDC
- Built-in PLL (Multiplication rate: ×1 to ×16)
- Advanced CPU Instruction Queue Buffer
- Built-in 8KB RAM + Built-in VRAM/RAM (12KB)
- SDRAM Controller with Burst Control
- Generic DMA Controller (HSDMA/IDMA)
- 4-ch. PWM Control Timer/Counter
- Supports Several Interfaces
  SIO with FIFO (IrDA1.0, ISO7816-3), SPI, I2S and USB
- 5-ch. ADC for Analog Input
- Built-in LCD Controller with 12KB IVRAM
  Supports Up to QVGA (320 × 240) Display in 1 bpp Mode (black and white) by Single Chip
  Supports VGA (640 × 480) and 64K Color
- Built-in JPEG decoder/encoder
- Built-in USB controller (Device) Full speed (12Mbps)
- Supports I^2S interface (In/Out)
- NAND Flash Interface

■ DESCRIPTIONS

The S1C33L19 is a cost-effective, high-performance 32-bit RISC controller designed specifically for graphic display applications. It incorporates LCD display functions and JPEG image processing for electronic devices requiring LCD display of images, such as photo viewers and other compact image display units, home intercoms and other home electronic devices, as well as operating panels incorporated into various office equipment.

The JPEG image processing function uses an internal hardware accelerator for high-load JPEG processing to achieve faster processing than software processing alone. It is provided as an easy-to-use JPEG decoder/encoder API with complex controls handled internally, allowing easy interfacing with applications for easy, high-speed enlargement and compression of JPEG image data, including photographs, improved application display capabilities, and smaller data sizes.

Peripheral circuits and pin layout are completely forward-compatible with the S1C33L17, enabling use with applications that rely on ADC functions and a wide range of serial interfaces, including numerous general-purpose input/output ports, powerful PWM timer/counter, and USB-FS device controller.

The S1C33L19 consists of a 32-bit RISC CPU core, JPEG decoder/encoder, general-purpose DMA controller, USB-FS device controller, PWM control timer/counter, several interfaces (IrDA1.0, SIO including ISO7816-3 protocol, SPI and I2S), ADC, RAM, general-purpose RAM shared IVRAM, RTC, and NAND Flash interface implemented by EPSON SoC design technology using a 0.18 µm fine-pattern CMOS process.

■ FEATURES

●Technology

- 0.18 µm AL-4-Layers mixed analog low power CMOS process technology

●CPU

- EPSON original C33 PE 32-bit RISC CPU-Core with AMBA bus optimized for SoC
- Max. 66 MHz operation
- Internal 2-stage pipeline and 4 instruction queues
- Instruction set: 128 instructions (16-bit fixed length)
- Basic instructions are compatible with the S1C33 32-bit RISC Cores.
- Dual AMBA bus system for CPU and LCDC

●Internal Memories
- 8K-byte RAM
- 12K-byte IVRAM (used as general-purpose RAM or VRAM)
- 2K-byte DST RAM (used as general-purpose RAM or IDMA descriptor table RAM can be used to store multiplicand when the build in MAC and API is used.)

●Oscillator Circuit / PLL

OSC3 Oscillator Circuit
- Crystal oscillation: 5 MHz min. to 48 MHz max.
- Ceramic oscillation: 5 MHz min. to 48 MHz max.
- External clock input: 5 MHz min. to 48 MHz max.
- A 48 MHz clock source with 0.25% of accuracy should be connected for using the USB function.
- Before using a ceramic resonator, please be sure to contact Murata Manufacturing Co., Ltd. for further information on conditions of use for ceramic resonators.

PLL
- PLL input frequency: 5 MHz min. to 50 MHz max. (OSC3 ×1, ×1/2, ×1/3 ... ×1/9, ×1/10)
- PLL output frequency: 20 MHz min. to 90 MHz max.
- Multiplication rate: ×1, ×2, ×3, ... ×15, ×16

OSC1 Oscillator Circuit
- Crystal oscillation: 32.768 kHz typ.
- External clock input: 32.768 kHz typ.

●Hardware accelerator module

JPEG decoder/encoder
- High-speed processing using internal hardware accelerator
- JPEG-baseline (ITU-T T.82 and JIS X4081 compliant)
- Supported markers: SOI, DQT, DHT, SOF0, DRI, SOS, EOI
- JPEG image formats: YUV444, YUV422, YUV420, YUV411, Grayscale
- Bitmap formats: RGB 24/16/8-bit, Grayscale 4/2/1-bit
- High-speed reduction function: 1/1, 1/2, 1/4, 1/8 Shrink mode
- Split decoding/encoding is possible to reduce memory usage
- Supported image data size: Unlimited (dependent on available memory size)
- API list
  JPEG header analysis (JpegAnalyze)
  JJPEG decoding (JpegDecode)
  JPEG encoding (JpegEncode)
- Decoding time:
  VGA (640x480): 1012 [msec] (typ.)
  QVGA (320x240): 287 [msec] (typ.)
  QQVGA (160x120): 86 [msec] (typ.)
  * Operating at 66 MHz, VRAM: Color 16-bit, Q value = 75, YUV420 format
- Encoding time:
  VGA (640x480): 1572 [msec] (typ.)
  QVGA (320x240): 415 [msec] (typ.)
  QQVGA (160x120): 116 [msec] (typ.)
  * Operating at 66 MHz, VRAM: Color 16-bit

Hardware calculation module

Allows high-speed processing using internal hardware accelerator.
- 4/8/16-element product-sum calculation (MAC)
- 2/3/4-order matrix calculation (Matrix)
- 2/3-order affine conversion (Affine)
- Butterfly calculation (Butterfly)

Supports the following calculation modes as numerical equations.
- Signed/unsigned 32-bit integer
- Q13/14 16-bit fixed decimal point value (FLOAT16_Q13/FLOAT16_Q14)

Supports saturation processing to prevent numerical overflows. (16-bit fixed decimal point value only)

●High Speed Bus (HB) Modules

SRAMC (SRAM Controller)

- 25-bit address lines and 8/16-bit selectable data bus
- UP to a 512M-byte (A[24:0]) address space is provided for each chip enable signal.
- Max. 8 chip enable signals are available to connect external devices.
- Programmable bus wait cycle (0 to 7 cycles)
- Supports external wait signals.
- 4GB physical address space is available.
  - The physical address space is divided into 23 areas: Area 0 to Area 22.
  - Areas 0 to 4 and Area 6 are system reserved.
- Supports only Little-Endian access to each area.
- Memory mapped I/O
- Supports both A0 and BS (Bus Strobe) access type external devices.
- SRAM, ROM, and Flash ROM direct access interfaces are built in.

SDRAMC (SDRAM Controller with SDRAM APP and AHB Local Bus Arbiter)

- Supports SDRAM direct interface.
- Supports only SDRAM devices with 16-bit data bus.
  Minimum configuration: 16M bits (2MB), 16-bit SDRAM × 1
  Maximum configuration: 512M bits (64MB), 16-bit SDRAM × 1
- CAS latency: 1, 2 or 3 programmable
- Supports burst and single read/write.
- Supports DQM (byte write) function.
- Supports max. 4 SDRAM banks and bank active mode.
- Incorporates a 12-bit auto-refresh counter.
- Intelligent self-refresh function for low power operation
- 2-stage × 32-bit data buffer and 8-stage × 16-bit × 2-slot instruction buffer built-in
- Supports up to 90 MHz SDRAM clock.
  - When the CPU clock is 48 MHz, the SDRAM clock can be set to 48 MHz.
  - When the CPU clock is 45 MHz, the SDRAM clock can be set to 90 MHz using the PLL.
- Arbitrates ownership of the external bus between the CPU, DMAC, LCDC and SRAMC.

DMAC (Direct Memory Access Controller)

- 4-ch. high speed hardware DMA
- 128-ch. intelligent DMA (variable data transfer controller) with specific control table

IVRAMARB (Internal Video RAM Arbiter)

- Contains a 12KB SRAM (3,072 words × 16 bits × 2).
- Arbitrates accesses from the LCDC and CPU.
- Allows the CPU and LCDC to access IVRAM in minimum 2 cycles by 32-bit access.
- Supports UMA (Unified Memory Access) for display.
- IVRAM is configurable as a 12KB general-purpose RAM in Area 0 using a control register if it is not used as a video RAM.

●Peripheral Bus (SAPB) Modules

TCU (timer/Counter Unit with PWM Outputs)

- 4-ch. 16-bit timer/counter
- Supports PWM outputs with DA16 (Digital D/A) mode.
- Contains a prescaler, which can divide the peripheral clock by 1 to 4,096, to generate the operating clock for each channel.
- Possible to invoke DMA transfer.

WDT (Watchdog Timer)

- 30-bit watchdog timer to generate an NMI interrupt
- The watchdog timer overflow cycle (NMI interrupt cycle) is programmable.
- The watchdog timer overflow signal can be output outside the IC.

ADC (A/D Converter)

- 5-ch. 10-bit A/D converter
- Upper/lower limit interrupt is available.
- Each ADC channel includes a data buffer.
- Contains a prescaler, which can divide the peripheral clock by 2 to 256, to generate the operating clock for ADC.

ITC (Interrupt Controller)

- Possible to invoke DMA transfer
- DMA controller interrupt: 5 types
- Input interrupt: 18 types
- TCU interrupt: 8 types
- EFSIO interrupt: 9 types
- ADC interrupt: 2 types
- RTC interrupt: 1 type
- SPI interrupt: 3 types
- USB interrupt: 2 types
- I^2S interrupt: 2 types
- LCDC interrupt: 1 type

GPIO (General-Purpose I/O Ports)

- Max. 82 ports in the TQFP24-144pin model.
  * The S1C33L19 GPIO ports are shared with other peripheral function pins (EFSIO, PWM etc.). Therefore, the number of GPIO ports depends on the peripheral functions used.

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- Supports USB2.0 full speed (12M bps) mode.
- Supports auto negotiation function.
- Supports control, bulk, isochronous and interrupt transfers.
- Supports 4 general-purpose end points and end point 0 (control).
- Embedded 1K-byte programmable FIFO
- Supports 8-bit local bus DMA port.
- Possible to invoke DMA transfer.
- Supports Async. DMA transfer.
- Supports DMA slave mode.
- Fixed 48 MHz clock for USB-FS.
- Supports snooze mode.

RTC (Real Time Clock)

- Contains time counters (seconds, minutes, and hours) and calendar counters (days, days of the week, months, and year).
- BCD data can be read from and written to both counters.
- Capable of controlling the starting and stopping of time clocks.
- 24-hour or 12-hour mode can be selected.
- A 30-second correction function can be implemented in software.
- Periodic interrupts are possible.

CARD (Serial Input/Output with Direction Control)

- Provides SmartMedia I/F signals (#SMRE, #SMWE).
- Provides 8-bit NAND Flash I/F signals.
- Hardware Reed-Solomon CODEC for either MLC or SLC Nand error detection.
- Supports NAND Flash booting function.

EFSIO (Extended Serial Interface with FIFO Buffer)

- 2-ch. clock sync./async. serial interface
- Contains FIFO data buffers (4 receive data buffer and 2 transmit data buffer are available for each channel).
- Supports IrDA1.0 interface.
- Contains a baud-rate generator (12-bit programmable timer).
- Supports ISO7816 mode (Ch.1 only).
  - Alternative MSB or LSB
  - Memory card interface compatible with ISO7816-3 T=0 & T=1 protocol
  - Programmable baud-rate and guard-time generation
  - ISO7816 acknowledge and automatically repeat transmission
- Possible to invoke DMA transfer.

UART

- Async. only Serial Interface (UART) with 1 byte Transmit data buffer and 2 bytes Receive data buffer (Ch.2).
- Built-in programmable 12-bit timer is available for baud-rate generators.
- Possible to invoke DMA Transfer.

SPI (Serial Peripheral Interface)

- 1 ch. SPI that operates in either master or slave mode

- Supports 1- to 32-bit data transfer.
- Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
- A 1 to 65,536 clocks of delay can be inserted between transfers.
- Generates transmit data register empty and receive data register full interrupts.
- Support both MMC & SD Card capabilities.
- Possible to invoke DMA transfer.
- Max. Bit Rate in Master mode is MCLK/2.

EGPIO (Extended GPIO)

- Max. 17 configurable GPIO ports are available in addition to the standard GPIO ports. In die form, Max. 91 ports are available.
  * The EGPIO ports are shared with other peripheral function pins.
    Therefore, the number of EGPIO ports depends on the peripheral functions used.
- Most ports have a pull-up resistor that can be enabled/disabled with the control register.
- Possible to drive the ports low.

CMU (Extended Clock Management Unit)

- Controls clock supply to each peripheral module (static).
- Manages reset and NMI inputs.
- Switches the system clock source (MCLK, SDRAM_CLK, or RTC_CLK).
- Controls the MCLK and RTC_CLK oscillator circuits.
- Turns on/off and controls frequency multiplication rate of the PLL.
- Controls clocks according to the standby mode (SLEEP and HALT).
- Controls divide ratios of the LCDC clock.
- Manages the external bus clock.

MISC (Misc. Setting Register)

- USB/RTC wait configuration registers
- Debug port function select register
- Boot mode configuration register

I^2S (Inter-IC Sound Bus Interface)

- Supports universal audio I2S Bus Interface.
- Support 16 bit or 24 bit data format for both input channel and output channel.
- Generate the bit clock, word-select signal, data and master clock.
- Master clock can be generated internally, or input from external.
- Generate 2 I^2S interrupt signals.
- Generate 4 I^2S HSDMA trigger signals.

LCDC (STN/TFT LCD Controller with AMBA Bus)

VRAM:

- Built-in a 12KB RAM usable as a display buffer or general-purpose RAM (register selectable)
- Supports the UMA method allowing LCDC to access SDRAM (external VRAM) or IVRAM (internal VRAM).
- The external VRAM map (SDRAM) is configurable.
- The sub-window area can be located in IVRAM or external VRAM regardless of whether it contains the main window area or not.

Display Support:

- 4- or 8-bit monochrome LCD interface
- 4- or 8-bit color LCD interface
- Single-panel, single-drive passive displays
- 12 or 16-bit Generic HR-TFT interface
  - 320 × 240-dot Sharp HR-TFT panel, SII liquid TFT panel, or some other TFT panels
- Typical resolutions
  - 320 × 240 (8-bpp mode, external VRAM is required) bpp = bits per pixel
  - 320 × 240 (1-bpp mode)

    * Note that the panel width must be a multiple of 16 ÷ bits per pixel.

Display Modes:

- Due to frame rate modulation, grayscale display is possible in up to 16 shades of gray when a monochrome passive LCD panel is used.
  - Two-shade display in 1-bpp mode
  - Four-shade display in 2-bpp mode
  - 16-shade display in 4-bpp mode

- A maximum of 64K colors can be simultaneously displayed on a color passive LCD panel.
  - 256-color display in 8-bpp mode
  - 4K-color display in 12-bpp mode
  - 64K-color display in 16-bpp mode
- A maximum of 65536 colors can be simultaneously displayed on a TFT panel.
  - Two-color display in 1-bpp mode
  - Four-color display in 2-bpp mode
  - 16-color display in 4-bpp mode
  - 256-color display in 8-bpp mode
  - 4K-color display in 12-bpp mode
  - 64K-color display in 16-bpp mode
- A look-up table, which consists of 6 bits × 16 entries × 3 colors, is provided.
  - In monochrome 1/2/4-bpp or color 8/12-bpp mode, the look-up table can be used or bypassed.
  - In color 1/2/4/16-bpp mode, the look-up table cannot be used (must be bypassed).

Display Features:

- Picture-in-Picture Plus (PIP+)

  Picture-in-Picture Plus enables a secondary window (or sub-window) within the main display window. The sub-window may be positioned anywhere within the main window and is controlled through registers. The sub-window retains the same color depth as the main window.
  The speed of generating a sub-window by hardware is faster than software. By using this PIP+ function, it can greatly speed the GUI performance and CPU can have more performance to assign other processing.
  (e.g. Voice etc.)
- 12 or 16-bit Generic HR-TFT interface

  The 12 or 16-bit Generic HR-TFT interface can support 320 × 240 Sharp HR-TFT panel, SII TFT panel or some other TFT panels. Because the timing of FPFRAM, FPLINE, FPSHIFT and TFT_CTL0–3 are not fixed for TFT panels, they can be controlled by register setting. By different register settings, you can get your specified TFT I/F signal timing.
- Clock source

  The LCDC clock can be internally divided 48 MHz by 1 to 16. The clock division register is located in CMU part.

●Operating Voltage

- VDD (Core): 1.70 to 1.90 V (typ. 1.8 V) when a ceramic resonator is used
- VDD (Core): 1.65 to 1.95 V (typ. 1.8 V) when a crystal is used or an external clock is input
- PLVDD: 1.65 to 1.95 V (typ. 1.8 V)
- VDDH (I/O): 2.70 to 3.60 V when the USB is not used (5-V tolerant I/O not supported)
- VDDH (I/O): 3.00 to 3.60 V (typ. 3.3 V) when the USB is used (5-V tolerant I/O not supported)

●Operating Frequency

- CPU: 66 MHz max.
- USB: 48 MHz fixed.
- SDRAMC: 90 MHz max.
- LCDC: 66 MHz max.
- Other peripheral circuits: 66 MHz max.

●Operating Temperatures

- -40 to 85°C

  (0 to 70°C when a ceramic resonator is used)

●Current Consumption

- During SLEEP: 0.3 µA typ. (Operation clock = 48 MHz)
- During HALT: 3.2 mA typ. (Operation clock = 48 MHz)
- During execution:

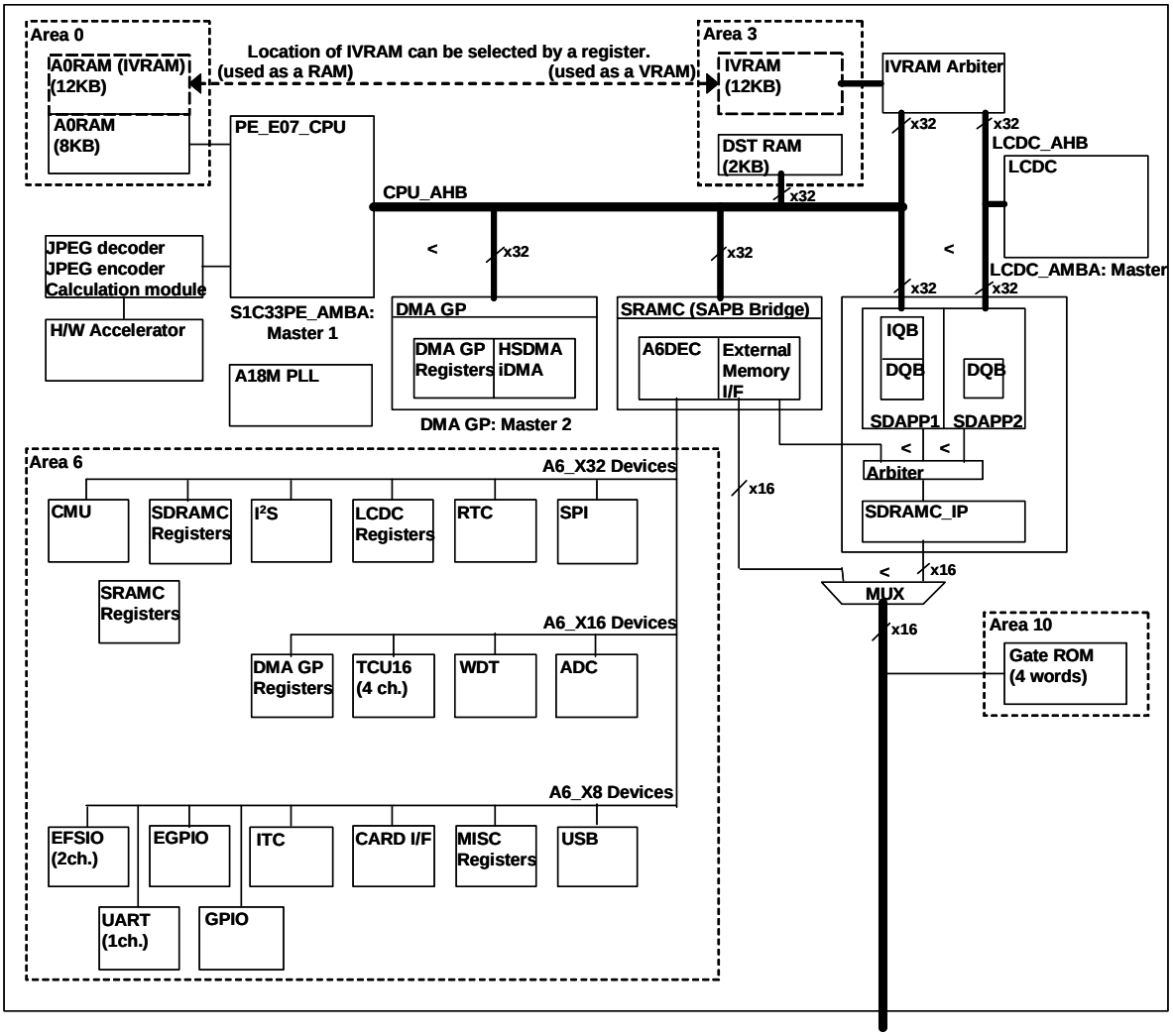
  Core 22.0 mA typ. (operation clock = 48 MHz)
  SRAMC 3.6 mA typ. (operation clock = 48 MHz, idle state with the clock supplied)
  SDRAMC 5.6 mA typ. (operation clock = 48 MHz, idle state with the clock supplied)
  DMA 4.1 mA typ. (operation clock = 48 MHz, idle state with the clock supplied)
  LCDC 5.6 mA typ. (operation clock = 48 MHz, idle state with the clock supplied)
  USB 10.0 mA typ. (operation clock = 48 MHz, idle state with the clock supplied)

ADC 260.0 µA typ. (idle state when ADC is enabled)
JPEG 25.0 mA Typ. (with 48 MHz operating clock, JPEG decoder/encoder operation)
* By controlling the CPU clock through the Clock-Gear (CMU), current consumption can be reduced.

●Shipping Form

- Package: TQFP24-144pin (16 mm × 16 mm × 1.0 mm and 0.4 mm pin pitch)
  PFBGA-180pin (12 mm × 12 mm × 1.2 mm and 0.8 mm ball pitch)
- Die form: 168 pads with pad pitch 90 µm

■ Block Diagram



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