EPSON
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S1R77009
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

NOTICE

Table of Contents

1. OVERVIEW

This IC is a line-sensor drive clock generation ID that provides high-speed read operation.

2. FEATURES

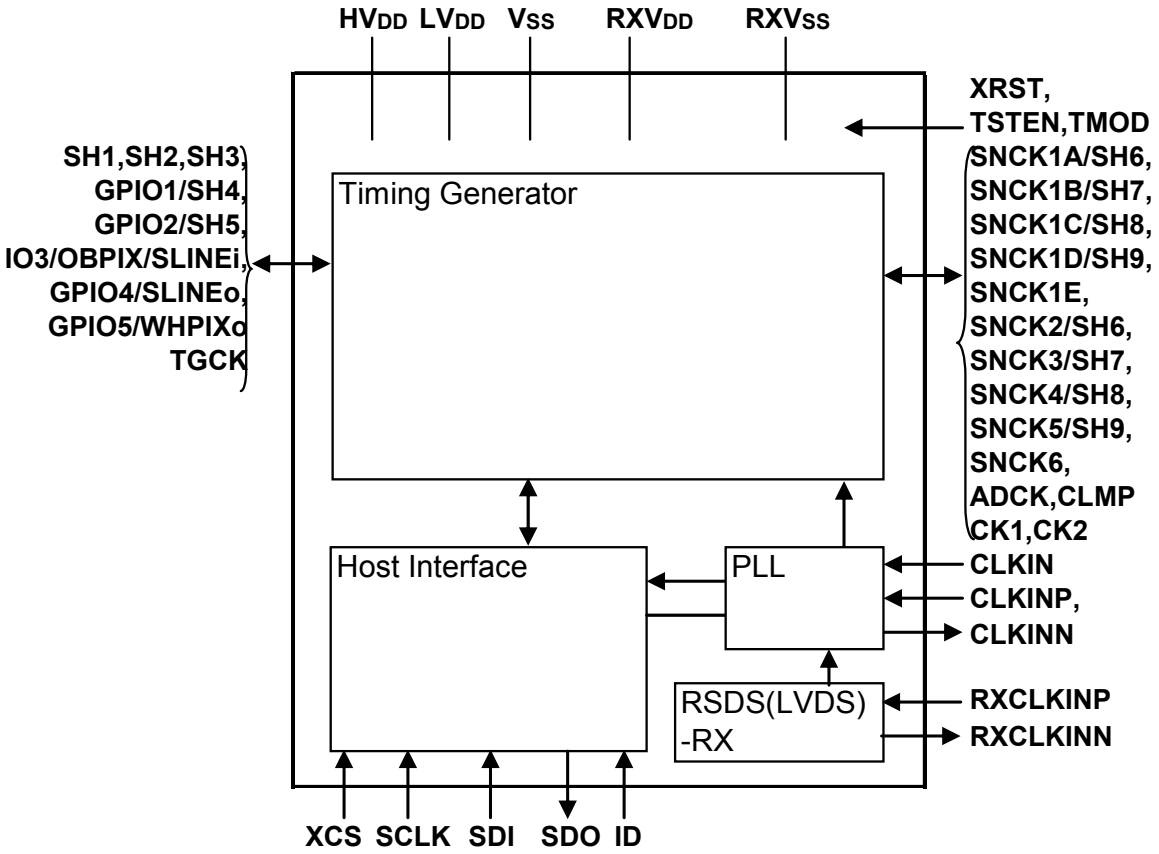
Common section
- 0.5 mm pitch, QFP48-pin package
- Two power supplies of 3.3V and 5V
- This IC, which contains PLL, generates internal reference clocks by multiplying the input of the CLK input signal by 3 or 6 times.
- Internal reference clock frequency: 60MHz ≤ Internal reference clock frequency ≤ 150MHz

Host Interface Section
- Serial interface

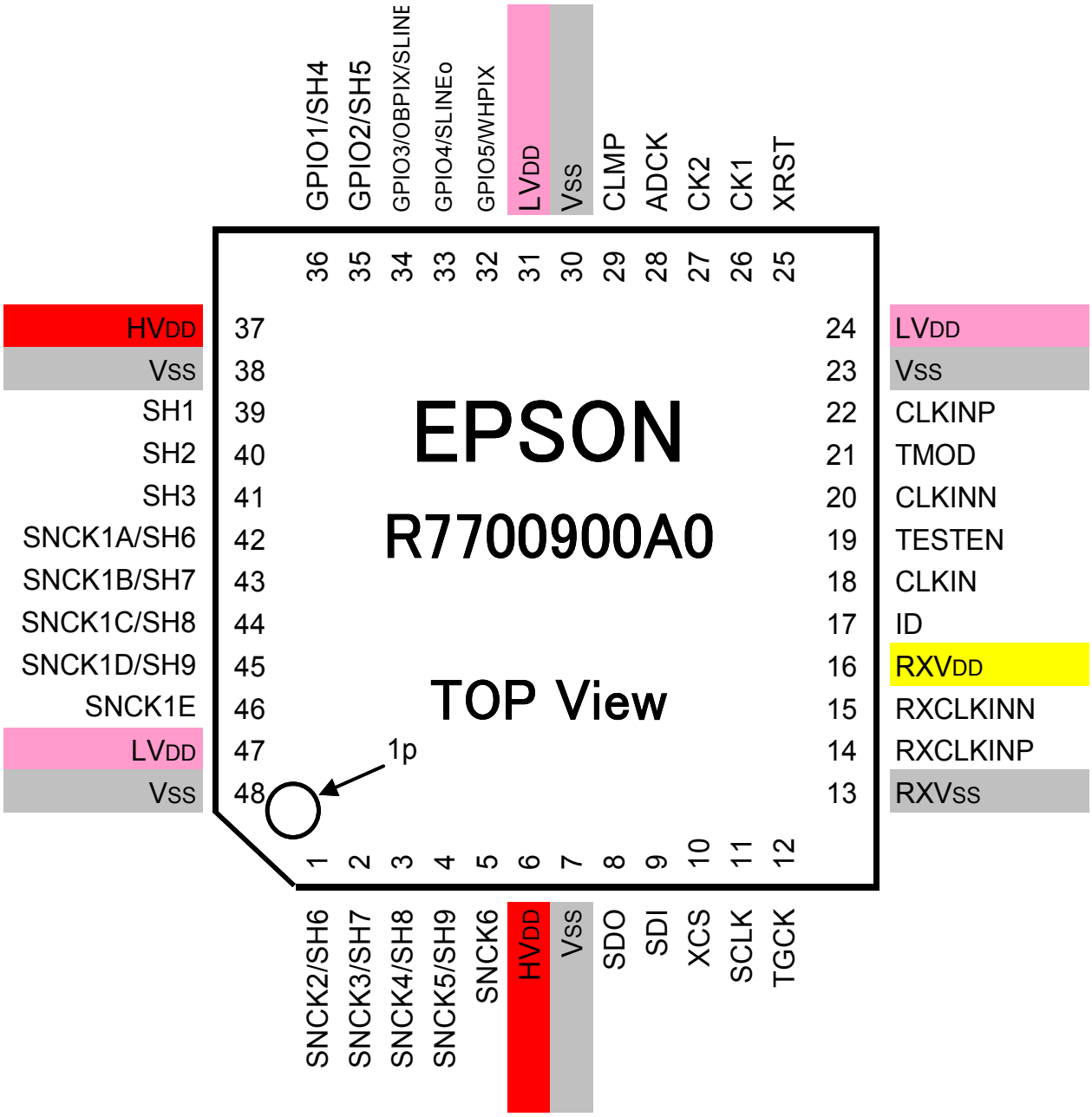
Drive clock signal generation section
- Generates the following shift and clock signals required for driving the line sensor and AFE.
  ADCK, SH1, SH2, SH3, SH4, SH5, SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E, SNCK2, SNCK3, SNCK4, SNCK5, SNCK6, CK1, CK2, CLMP
- Built-in memory for generating clock signal drive patterns
- The clock signal drive pattern during image reading and dummy pixel output is freely programmable.
- Select the drive pattern resolution per cycle for the ADCK signal from 3 and 6.
- Support of line sensor
- 5.0V drive clock output

※ Radiation shield is not included.

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



5. PIN DESCRIPTION

No.	Pin	Pin Name	I/O	Reset	Pin Function	Remarks	Drive Capacity
Line Sensor Drive Clocks							
1	39	SH1	B5	PD	Line Sensor shift 1	PD	12mA*
2	40	SH2	B5	PD	Line Sensor shift 2	PD	12mA*
3	41	SH3	B5	PD	Line Sensor shift 3	PD	12mA*
4	42	SNCK1A/SH6	B5	PD	Line Sensor clock 1A/SH6	PD	12mA*/24mA*
5	43	SNCK1B/SH7	B5	PD	Line Sensor clock 1B/SH7	PD	12mA*/24mA*
6	44	SNCK1C/SH8	B5	PD	Line Sensor clock 1C/SH8	PD	12mA*/24mA*
7	45	SNCK1D/SH9	B5	PD	Line Sensor clock 1D/SH9	PD	12mA*/24mA*
8	46	SNCK1E	B5	PD	Line Sensor clock 1E	PD	12mA*/24mA*
9	1	SNCK2/SH6	B5	PD	Line Sensor clock 2/SH6	PD	12mA*/24mA*
10	2	SNCK3/SH7	B5	PD	Line Sensor clock 3/SH7	PD	12mA*/24mA*
11	3	SNCK4/SH8	B5	PD	Line Sensor clock 4/SH8	PD	12mA*/24mA*
12	4	SNCK5/SH9	B5	PD	Line Sensor clock 5/SH9	PD	12mA*/24mA*
13	5	SNCK6	B5	PD	Line Sensor clock 6	PD	12mA*/24mA*
Host Interface							
14	36	GPIO1/SH4	B	PD	General Purpose1/SH4	PD	12mA*
15	35	GPIO2/SH5	B	PD	General Purpose2/SH5	PD	12mA*
16	34	GPIO3/SLINEi/OBPIX	B	PD	General Purpose3/SLINEi/OBPIX	PD	12mA*
17	33	GPIO4/SLINEo	O	Hi-Z	General Purpose4/SLINEo		12mA*
18	32	GPIO5/WHPIX	O	Hi-Z	General Purpose5/WHPIX		12mA*
19	12	TGCK	B5T	Hi-Z	Line Sensor shift signal trigger	SMT	12mA*
20	10	XCS	I5T	—	Chip select	SMT	—
21	11	SCLK	I5T	—	Serial clock	SMT	
22	9	SDI	I5T	—	Serial data input	SMT	
23	8	SDO	O	Hi-Z	Serial data output		2mA
24	17	ID	I	—	Chip ID select	PD	—

Symbols in the I/O section
A: Analog pin
I: Input pin (3.3V input)
I5T: Input pin (5.0V tolerant input)
O: Output pin (3.3V output)
B: Bi-directional pin (3.3V input/output)
B5: Bi-directional pin (5.0V input/output)
B5T: Bi-directional pin (5.0V tolerant input/output)
P: Power supply pin
Symbols in the Reset (in the initial state) section
HI-Z: High impedance state
PD: In the input state, potential is Low due to pull-down register
Symbols in the Remarks section
PU: Pull-up
PD: Pull-down
SMT: Schmitt input
* Low Noise type output

No.	Pin	Pin Name	I/O	Reset	Pin Function	Remarks	Drive Capacity
AFE Interface							
25	28	ADCK	B	PD	A/D Converter clock	PD	12mA*
26	26	CK1	B	PD	Sampling clock 1	PD	12mA*
27	27	CK2	B	PD	Sampling clock 2	PD	12mA*
28	29	CLMP	B	PD	Clamp timing	PD	12mA*
System Signal							
29	25	XRST	I	—	Reset signal	SMT	—
30	18	CLKIN	I	—	Reference clock	PD	—
31	22	CLKINP	A	—	Reference clock (Positive) [OSC input]		Analog
32	20	CLKINN	A	—	Reference clock (Negative) [OSC input]		Analog
33	14	RXCLKINP	A	—	Differential clock (Positive) [RSDS (LVDS) input]		Analog
34	15	RXCLKINN	A	—	Differential clock (Negative) [RSDS (LVDS) input]		Analog
35	19	TESTEN	I	—	Test pin	PD	—
36	21	TMOD	I	—	Test pin	PD	—
Power Supply							
37	6	HV_{DD}	P	—	5.0V logic power supply		—
38	37	HV_{DD}					
39	24	LV_{DD}	P	—	3.3V logic power supply		—
40	31	LV_{DD}	P	—			
41	47	LV_{DD}	P	—			
42	16	RXV_{DD}	P	—	RSDS (LVDS) -RX power supply +3.3V		—
43	7	V_{SS}	P	—	Logic ground		—
44	23	V_{SS}	P	—			
45	30	V_{SS}	P	—			
46	38	V_{SS}	P	—			
47	48	V_{SS}	P	—			
48	13	RXV_{SS}	P	—	RSDS (LVDS) -RX ground		—

Symbols in the I/O section
A: Analog pin
I: Input pin (3.3V input)
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SMT: Schmitt input
* Low Noise type output

6. FUNCTIONAL DESCRIPTION

The functions of each circuit block are explained below.

6.1 Host Interface Section

6.1.1 Serial interface

Four types of serial interface signals can be handled. They are: Chip Select (XCS) signal, Serial Data I/O Sync Clock (SCLK) signal, Serial Data Input (SDI) signal, and Serial Data Output (SDO) signal. When this IC is in the active state (when the XCS signal is Low), data is sent or received synchronously with the SCLK signal. The access occurs in the 16-bit register access mode (25 or 24 cycles) or 8-bit register access mode (16 cycles) based on the combination of TMOD and ID signals. Cycle count is set according to TMOD and ID signals as defined in Table 6.1.

Table 6.1 Setting of Access Cycles

Access cycle	TMOD	ID
25 cycles	LOW	Chip ID selection
24 cycles	HIGH	LOW
16 cycles	HIGH	HIGH

This IC has a built-in counter for serial-to-parallel (or parallel-to-serial) data conversion, and it is reset when the XCS signal goes high. Therefore, the XCS signal must be negated (that is, the XCS signal must go high) at the end of each cycle for register writing or reading.
In the 16-bit register access mode, first write the identification (ID) bit that indicates the write or read access. When the ID bit is low, the write access occurs. When it is high, the read access occurs.After writing the ID bit, write the ID Select bit (in 25-cycle operation only) and the 7-bit register ID number. Then, write or read the data.During 25-cycle operation, an access to this IC is made valid only when the input level of Chip ID Select bit has the same logic as the ID signal (for Chip ID selection setting).
All of Chip ID Select bit, register ID number, and data are sent at the rising edge of clocks, and they are sent beginning with the MSB. Figure 6.1 and 6.2 show the timing chart of each access, and Figure 4.2 shows the access sequence.

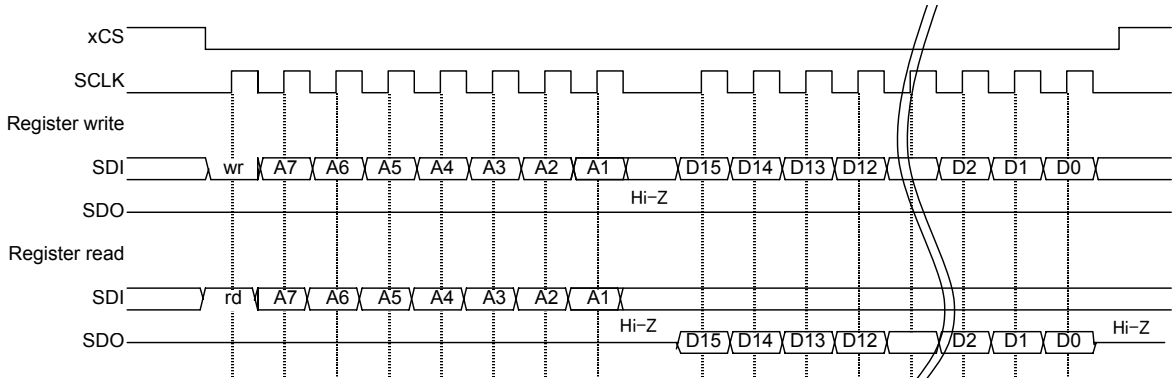


Figure 6.1 Serial interface access timing of register access mode without 16-bit ID

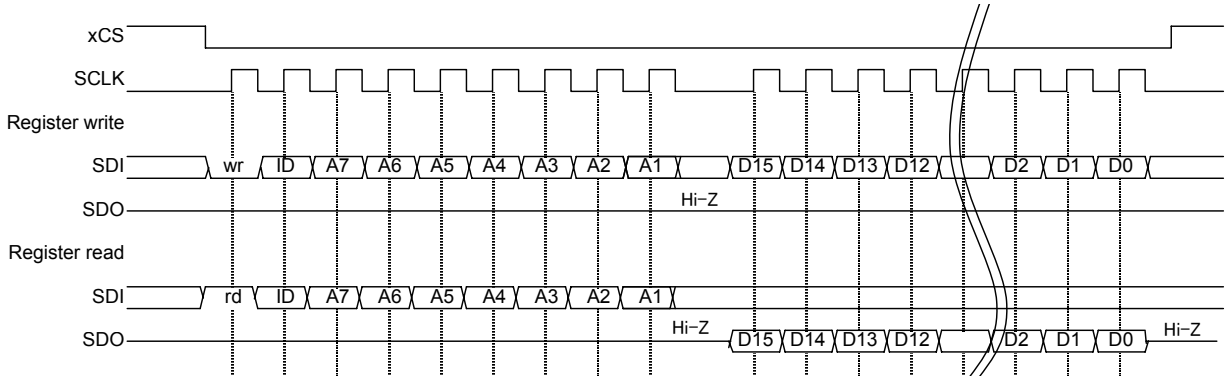


Figure 6.2 Serial interface access timing of register access mode with 16-bit ID

In the 8-bit register access mode, first write the data format specification bit during the read operation. If MD[1:0] = “00”, 8-bit data is output with “00” set for the high-order 2 bits. If MD[1:0] = “00”, 8-bit data is output with “00” set for the high-order 2 bits. Following the data format specification bit, write the identification (ID) bit that indicates the write or read access. When the ID bit is low, the write access occurs. When it is high, the read access occurs. Following the identification bit, 3-bit register identification number is written and the data writing or reading follows.During this register access, 8-bit low data or high data must be accessed for each address. Also, the register address must not be specified directly.
To access, specify the address to be accessed in the address register, set the write data in the data low register, and set the write data to the data high register. Then the register access is complete. Table 6.2 shows the address, the register address for data L and data H.

Table 6.2 Setting of Access Cycles

Address A [3:1]	Register name
001	Address setting register
010	Data low setting register
100	Data high setting register

Both register identification number and data transfer synchronizes with the clock rise and transfer takes place in sequence from MSB. Figure 6.3 shows the timing chart of each access, and Figure 6.4 shows the access sequence.

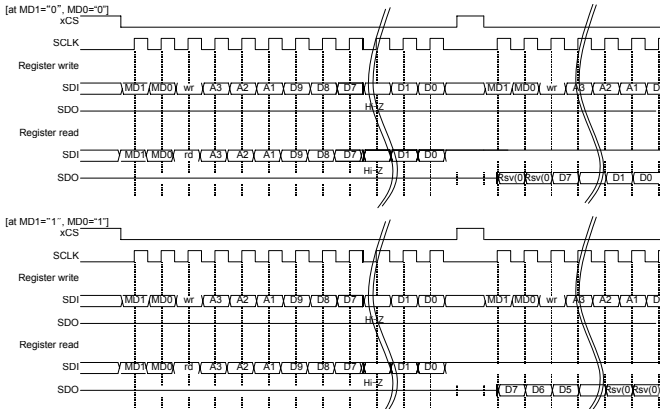


Figure 6.3 8-bit Register Access Mode Serial Interface Access Timing

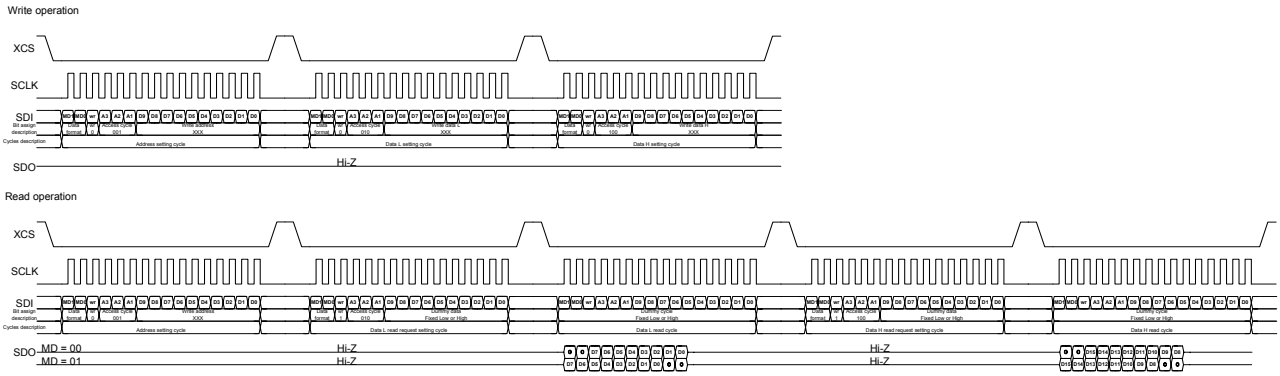


Figure 6.4 Serial interface access sequence of 8-bit register access mode

6.2 RSDS (LVDS) Section

An input clock signal can be entered via the RSDS (LVDS) circuit. Figure 6.5 illustrates the RSDS (LVDS) peripheral connections.

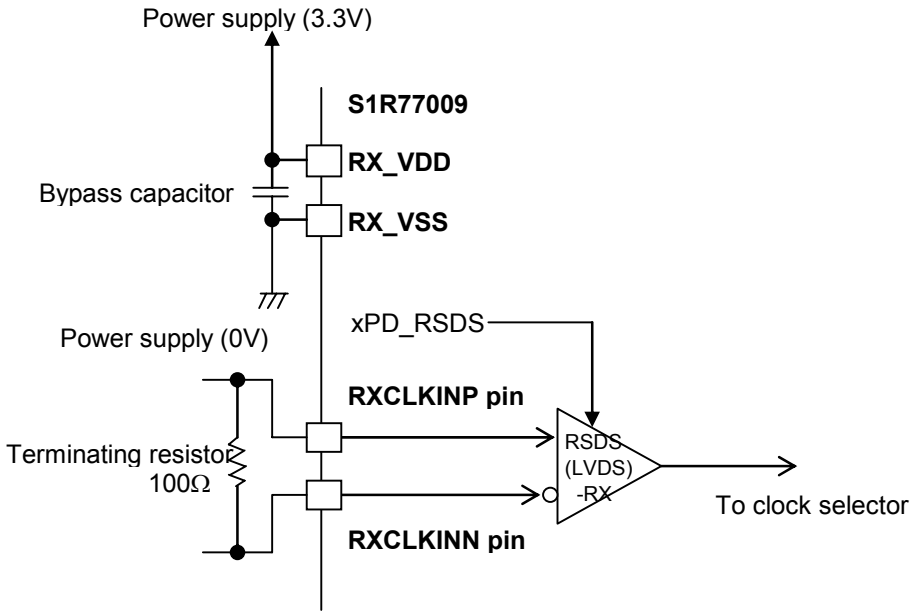


Figure 6.5 RSDS (LVDS) Connection Diagram

(1) Power-down function

The RSDS (LVDS) section provides the Power-Down function that is controlled by the xPD_RSDS bit of the ANA_RESET register (No.0x70). If the xPD_RSDS bit is set to "0", the RSDS (LVDS) section enters in the power-down mode and it stops output of input signal. Also, setting "1" cancels the power-down mode and starts output of input signal. After release of the power-down mode, however, up to 10 milliseconds are required for the RSDS (LVDS) section to start its stable operation.

(2) Terminating resistor

Connect a 100Ω termination resistor to a point close to the RSDS (LVDS) input pin.

Restriction

We recommend to use an external resistor having the (1.0% or less tolerance. Also, this IC and connectors must be mounted on the same side (component side) of the board without passing the leads through holes.

(3) Processing of empty pins

If the clock input signal is NOT entered via the RSDS (LVDS) circuit, the RXCLKINP signal must be fixed to low and the RXCLKINN signal must be fixed to high.

6.3 Built-in PLL Section

This IC enables the built-in PLL to multiply the external input clock, CLK input signal, by 3 or 6 times and generates the internal reference clock. The internal reference clock generates the internal state required for processing per pixel. 1T (one state) is equivalent to one cycle of internal reference clock.
Figure 6.6 illustrates the built-in PLL peripheral connections.

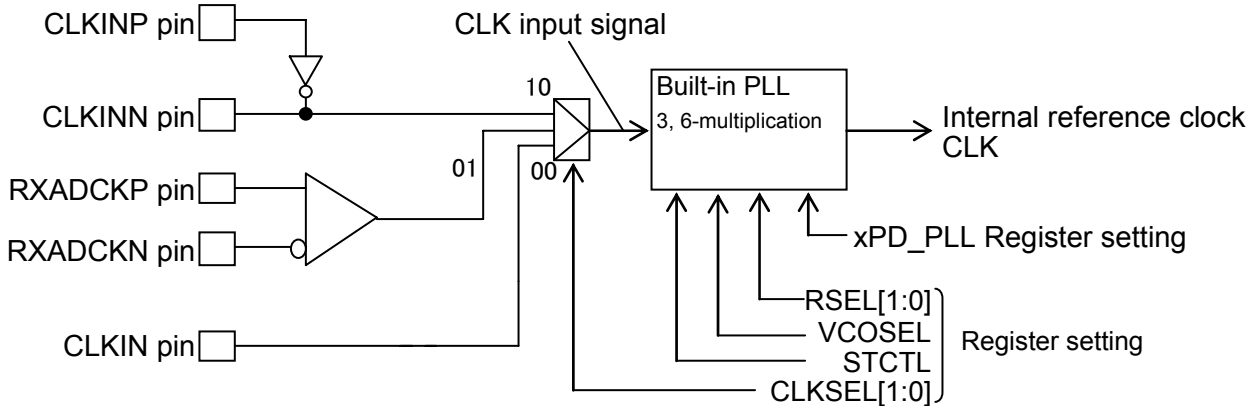


Figure 6.6 Built-in PLL

Restriction

Be sure to set "0" for the xPD_PLL bit in the ANA_RESET register (No.0x70) and stop oscillation of the built-in PLL before changing the setting of the following bits in the PLL_IMGSIG_CTL register (No.0x7F).

VCOSEL, CLKSEL[1:0], RSEL[1:0]

(1) Power-down function

The power-down function of the built-in PLL can be controlled by the XPD_PLL bit in the ANA_RESET register (No.0x70). Setting "0" for the xPD_PLL bit places the built-in PLL in power-down mode and stops oscillation. Setting "1" releases the power-down mode and starts oscillation. After releasing the PLL power-down mode, a maximum of 10 ms is required until stable oscillation output is achieved.

(2) External clock selection

This IC enables input by selecting clock pulse input, RSDS (LVDS) differential input or oscillation circuit input for the external clock as shown in Table 6.3. Also, you need to set the CLKSEL bit in the PLL_IMGSIG_CTL register (No.0x7F) in accordance with the input method.

Table 6.3 CLKSEL Setting

External clock input	Register setting	Pin processing				
	CLKSEL[1:0]	CLKIN	RXCLKINP	RXCLKINN	CLKINP	CLKINN
Clock pulse	00	Clock input	Predefind at LOW	Predefind at HIGH	Predefind at LOW	Unconnected
RSDS (LVDS) differential	01	Predefind at LOW	Clock input		Predefind at LOW	Unconnected
Oscillation Circuit	10	Predefind at LOW	Predefind at LOW	Predefind at HIGH	X'tal connection	

(3) Internal reference clock frequency setting

For the internal reference clock frequency setting, set the VCOSEL bit in the PLL_IMGSIG_CTL register (No.0x7F) in accordance with the frequency and multiple number of CLKIN input signal in compliance with Table 6.4.

Table 6.4 VCOSEL Setting

Internal reference clock (internal clock frequency (f_{CLKIN} MHz) × multiple number)	VCOSEL bit setting
60MHz ≤ f_{CLKIN} × (multiplication setting) ≤ 100 MHz	0
60MHz ≤ f_{CLKIN} × (multiplication setting) ≤ 150 MHz	1

Restriction

For the internal reference clock frequency (fclk), set by taking care of the following:

60MHz ≤ Internal reference clock frequency (f_{CLKIN}) ≤ 150MHz

(4) Multiplication setting

Set the built-in PLL multiplication with the STNUM bit of the STCTL register (No.0x52). Also set the reference multiplication to 3 or 6 using the STNUM bit.

6.4 Controls

6.4.1 Overview

The controller generates control signals that are compatible with the internal AFE and line sensor.
- Support of line sensor
- Programmable support of the control signal for line sensor and internal AFE.
- Programmable support of the drive clock pulse pattern output of line sensor.
- Programmable support of the AFE clock pulse pattern output.
- Support of output control for each clock and control signal.

6.4.2 Image Capture Operation

This IC operation includes two states: standby and image capture. To put the operation into standby, the TGSTART bit must be set to "0" in the TGCTL register (No.0x50). To put the operation into image capture state, set "1" for the TGSTART bit, similarly. Setting "1" for the TGSTART bit triggers the image capture operation.

Figure 6.7 Standby and Image Capture State

Restriction
Change of register setting other than the TGSTART bit is not allowed during image capturing. If other than the TGSTART bit is changed, when the image data is being captured, normal operation may not be performed.

Restriction 2
Setting the TGSTART bit to "1" is not allowed when the ADCKEN bit is "0". If "1" is set for the TGSTART bit when the ADCKEN bit is "0", normal operation may not be performed.

6.4.3 Pixel Process

(1) Internal state and drive pattern resolution setting
All the processing operations per pixel of this IC are based on the internal state. The internal signal "ADCKREF" is used as the base point of the internal state, and its cycle depends on drive pattern resolution setting. A one-element process is performed in ADCKREF1 cycles.
The number of states of the internal state, which depends on drive pattern resolution setting, is set with the STNUM bit in the STCTL register (No.0x52). For example, at 6-dividing setting, the resolution is set to 6, and ADCKREF generates one cycle in six states. Table 6.5 shows the relationships between the drive pattern resolution setting and total number of states.

Table 6.5 Internal State Number

Drive pattern resolution setting		Range of states	Total number of states
Set value (STNUM)	Dividing		
"1"	6	0 to 5	6T
"0"	3	0 to 2	3T

Figure 6.8 shows the relationships between the internal state and ADCKREF signal when the drive pattern resolution is set to six dividings. In this figure, "T" indicates a 1-state time in the internal state to process one pixel in 0 to 5 states (6T in all). The figure provides an example when 0 to 2 of the ADCKREF signal are set to high in the pattern RAM and 3 to 5 are set to low.

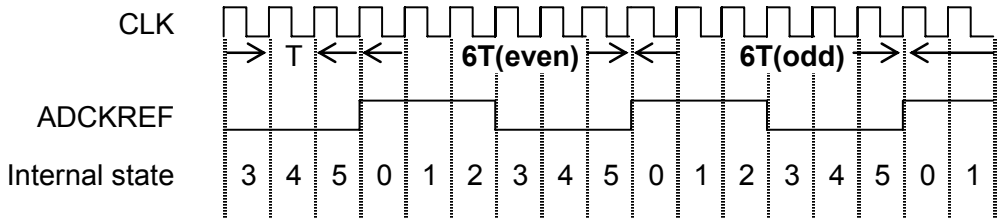


Figure 6.8 Relationship between the Internal State and the ADCKREF Signal (at 6-dividing setting)

(2) Synchronization mode

This IC has a function to phase-adjust (synchronize) the internal state with the CLK input signal. You can select the method of synchronization by setting the SYNCMD [1:0] bit in the STCTL register (No.0x52).

If "00" is set to the SYNCMD [1:0] bit, the internal state is always reset in synchronization with the rising edge of the CLK input signal. If "10" is set, synchronization of the internal state takes place only on the rising edge of the next CLK input signal after the rising edge of the shift pulse trigger signal (TGCK) that indicates the start of 1-line process has been detected. If "11" is set, no synchronization takes place. The internal state is reset only when the internal counter full is detected. Figure 6.9 shows an example of operation when different values are set.

To filter in this IC, the TGCK signal externally input delays in the internal reference clock by about 2 clocks as shown in Figure 6.9. Based on the rising edge of this delayed signal [TGCK (rising edge) in the figure below] synchronization of the internal state takes place. During external input of the TGCK signal, the TGCK signal can be input in negative logic by setting the TGCKINV bit to "1" in the TGMD register (No.0x51).

For details of 1-line process, see 6.4.4.

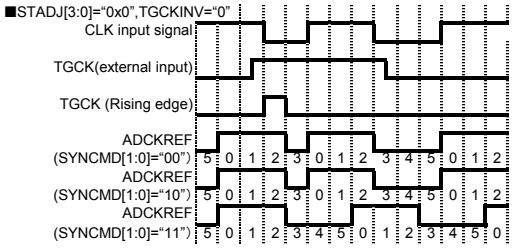


Figure 6.9 Example of Setting Synchronization Mode (1)

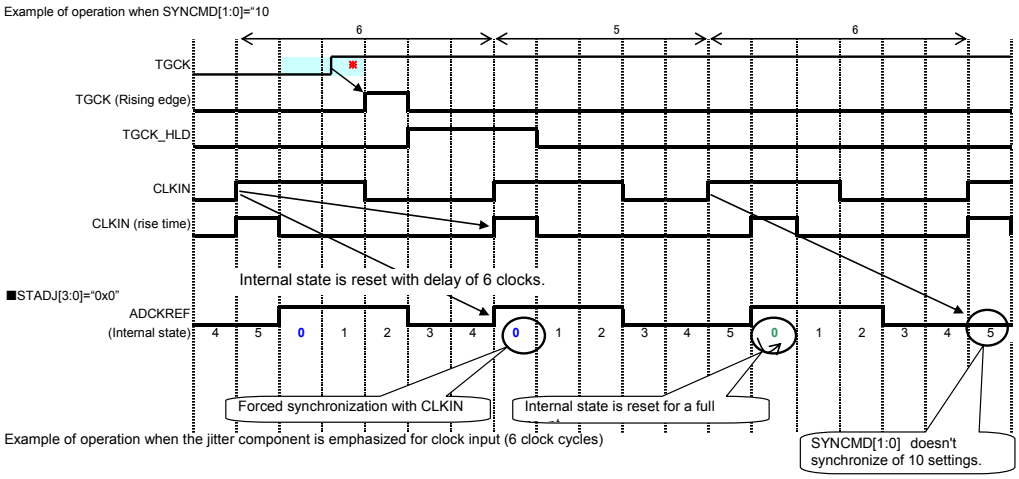


Figure 6.10 Example of Synchronization Mode Internal Operation

Restriction

To prevent the detection of TGCK rising from delaying one cycle of ADCKREF, the ADCKREF signal should not synchronize with the point of change of TGCK (internal TGCK rising). TGCK must therefore be input by avoiding one state after the rising edge of the CLK input signal.

Figure 6.10 shows an internal operation example.

When the internal state synchronizes with the CLK input signal, the phase difference can be set with the STADJ [3:0] bit in the STCTL register (No.0x52). Figure 6.11 shows an operation example. If no amount of adjustment (STADJ[3:0] = "0x0") is specified for setting the phase difference as shown in Figure 6.11, the phase difference between the CLK input signal and internal state is 0 in the internal clock.

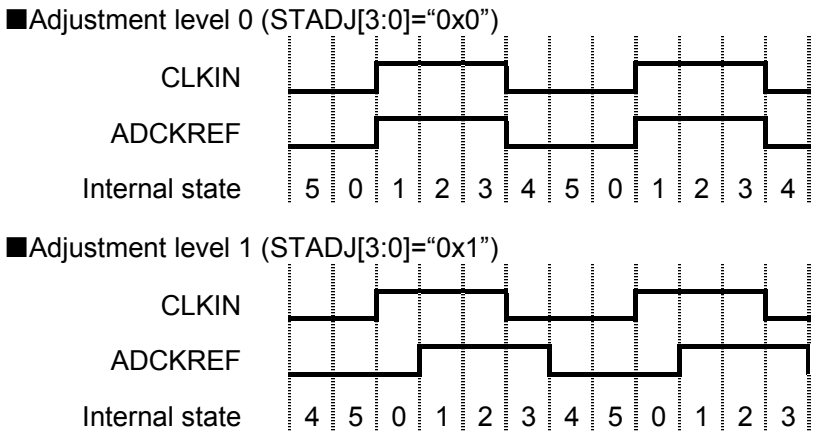


Figure 6.11 Internal-state synchronization adjustment example

Restriction 1

At 6-multiplication operation, the set value must be within STADJ[3:0] multiplication value (0x05). In the same way, at 3-multiplication setting, the set value must be within the 0x02 value.
For 6-multiplication operation, set 0x0 to synchronize reference clock.
For 3-multiplication operation, set 0x0 to synchronize reference clock.

6.4.4 Line Process

1-line operation

One-line process is done based on the TGCK signal (or trigger signal). The TGCK signal indicates the start of one-line process. This IC starts the process of one line after detecting active TGCK signal. The cycle of the TGCK signal is referred to as the line cycle.
Figure 6.12 shows an example of 1-line process operation.

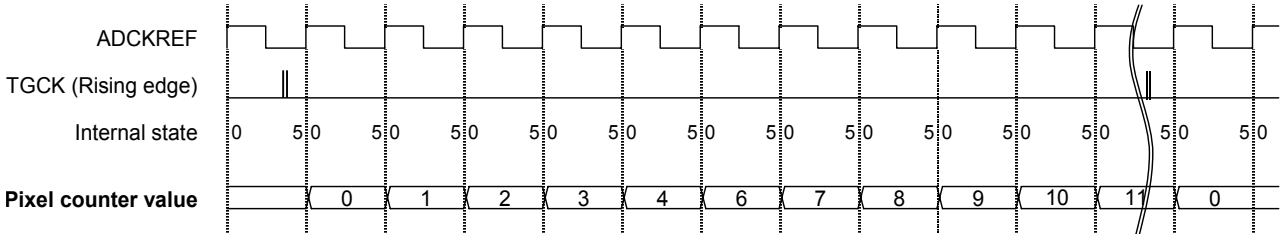


Figure 6.12 Example of One-line Processing Operation

This IC generates each timing with the counters below to perform capture process of 1 line.

- Pixel counter
  - ・Counts the number of pixels of the image data transferred from AFE.
  - ・Starts counting the internal state from the first "state 0" after detecting the rising edge of the TGCK signal.

6.4.5 Shift Signal and Clock Pulse Output Timings

(1) Setting of Timing

Shift signal and clock pulse output timings, as well as black-base pixel and white pixel locations, are specified with event patterns (PAT00 to 7F registers), using the change of the respective states as an event.
Each event pattern is set in 2-word units as shown in Table 6.6. You can therefore specify up to 64 events (0x40 events). Each event, which is set in pixels, generates an event of the set bit when the pixel counter is equal to the set value of the PIXNUM [15:0] bit. Once an event is generated, the desired bit is set to "1", and the state of the timing changes. To prevent any event from being changed, "0" should be set.
When setting "1" for the INTGCK bit of TGMD register (No.0x51) to operate as the TGCK internal generation mode, set "1" for all bits of from SH1 to WHPIX in the last line of the event setting, and set the pattern in which the pixel counter value of the desired timing is set to generate the TGCK signal.
PAT00 to PAT7F registers (No.0x00 to 3F) consist of 2 banks. Be sure to set the EVENTPAT0EN bit in the PATEN register (No.0x53) to "1" to access to PAT00 to PAT3F registers (No.0x00 to 3F) which is the 0th bank. After completing access, set "0" for the EVENTPAT0EN bit. In the same manner, set the EVENTPAT0EN bit in the PATEN register (No.0x53) to access to PAT40 to 7F registers (No.0x00 to 3F) which is the 1st bank. An unnecessary event pattern setting register should be set to 0xFFFF.

Table 6.6 Register for Setting Output Timing of Each Signal

Registers	Bit	Symbol	Description
PAT00, PAT02…	0 to 15	PIXNUM[15:0]	Specifies a pixel location to generate an event. (Comparison with pixel counter)
PAT01, PAT03…	0	SH1	SH1 signal timing
	1	SH2	SH2 signal timing
	2	SH3	SH3 signal timing
	3	SH4	GPIO1/SH4 signal timing
	4	SH5	GPIO2/SH5 signal timing
	5	SH6	SNCK1A/SNCK2/SH6 signal timing
	6	SH7	SNCK1B/SNCK3/SH7 signal timing
	7	SH8	SNCK1C/SNCK4/SH8 signal timing
	8	SH9	SNCK1D/SNCK5/SH9 signal timing
	9	SLINE_RISE	GPIO4/SLINEo signal timing
	10	SLINE_FALL	GPIO4/SLINEo signal timing
	11	CLMP	Clamp timing
	12 to 13	SNCKCTL[1:0]	Clock pattern output timing 00: (Unchanged) 01: Pattern 1 output 10: Pattern 2 output 11: Fixed value output, switching of fixed value output*
	14	OBPIX	Specifies a black-base pixel location.
	15	WHPIX	Specifies a white pixel location.

* During fixed value output setting, if an event set by "11" occurs, the fixed value output is switched.
(SNCKxxLV1 setting level output ←→ SNCKxxLV2 setting level output)

Restriction 1
If a PIXNUM event occurs, the maximum set value is set to 0xFFFE.
The minimum set value is set to 0x0001.
0xFFFF must be specified at a portion without event setting.

Restriction 2
It is recommended to set the last clock pattern output timing of one line cycle to the fixed value output.

(2) Operation example
Figure 6.13 Operation example in single-channel mode shows an operation example where event patterns are set as shown Table 6.7 in the single-channel mode.

Table 6.7 Timing Setting Example

No.	WHPIX 15	OBPIX 14	SNCKCTL[1:0] 13 to12	CLMP 11	SLINE_FALL 10	SLINE_RISE 9	SH9 8	SH8 7	SH7 6	SH6 5	SH5 4	SH4 3	SH3 2	SH2 1	SH1 0	PIXNUM[15:0] 15 to 0	bit
0x00	0	0	11	1	0	0	0	0	0	0	0	0	0	0	0	0x00001	
0x02	0	0	01	0	0	0	0	1	0	1	0	1	0	0	1	0x00002	
0x04	0	0	10	0	0	0	0	0	0	0	0	0	0	0	1	0x00003	
0x06	0	0	00	0	0	0	0	0	0	0	1	1	0	1	0	0x00004	
0x08	1	1	01	0	0	0	0	0	0	1	0	0	0	1	1	0x00005	
0x0A	0	0	00	0	0	0	1	1	0	0	1	1	1	0	1	0x00006	
0x0C	1	1	00	0	0	0	0	0	0	0	0	0	1	1	0	0x00007	
0x0E	0	0	11	0	0	0	0	0	1	0	1	1	0	1	0	0x00008	
0x10	0	0	11	0	0	0	0	0	0	0	0	0	1	0	0	0x00009	
0x12	0	0	11	1	0	0	1	0	0	0	1	0	1	0	0	0x0000A	
0x14	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF *	
0x16	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x18	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x1A	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x1C	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x1E	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x20	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x22	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x24	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x26	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x28	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x2A	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
:																:	
:																:	
0x7C	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	
0x7E	1	1	11	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF	

SH1POL = 0 SH2POL = 0 SH3POL = 0 SH4POL = 0
SH5POL = 1 SH6POL = 0 SH7POL = 0 SH8POL = 0
SH9POL = 0
GPIO3POL = 0 GPIO4POL = 0
GPIO5POL = 1
INSLINE = 0
SNCK1AxSH6 = 1 SNCK1BxSH7 = 1 SNCK1CxSH8 = 0 SNCK1DxSH9 = 0
SNCK2xSH6 = 0 SNCK3xSH7 = 0 SNCK4xSH8 = 1 SNCK5xSH9 = 1

* In the TGCK input mode, set the event signal field to 0xFFFF, and set the PIXNUM field to a pixel counter value of the timing you want to generate TGCK.

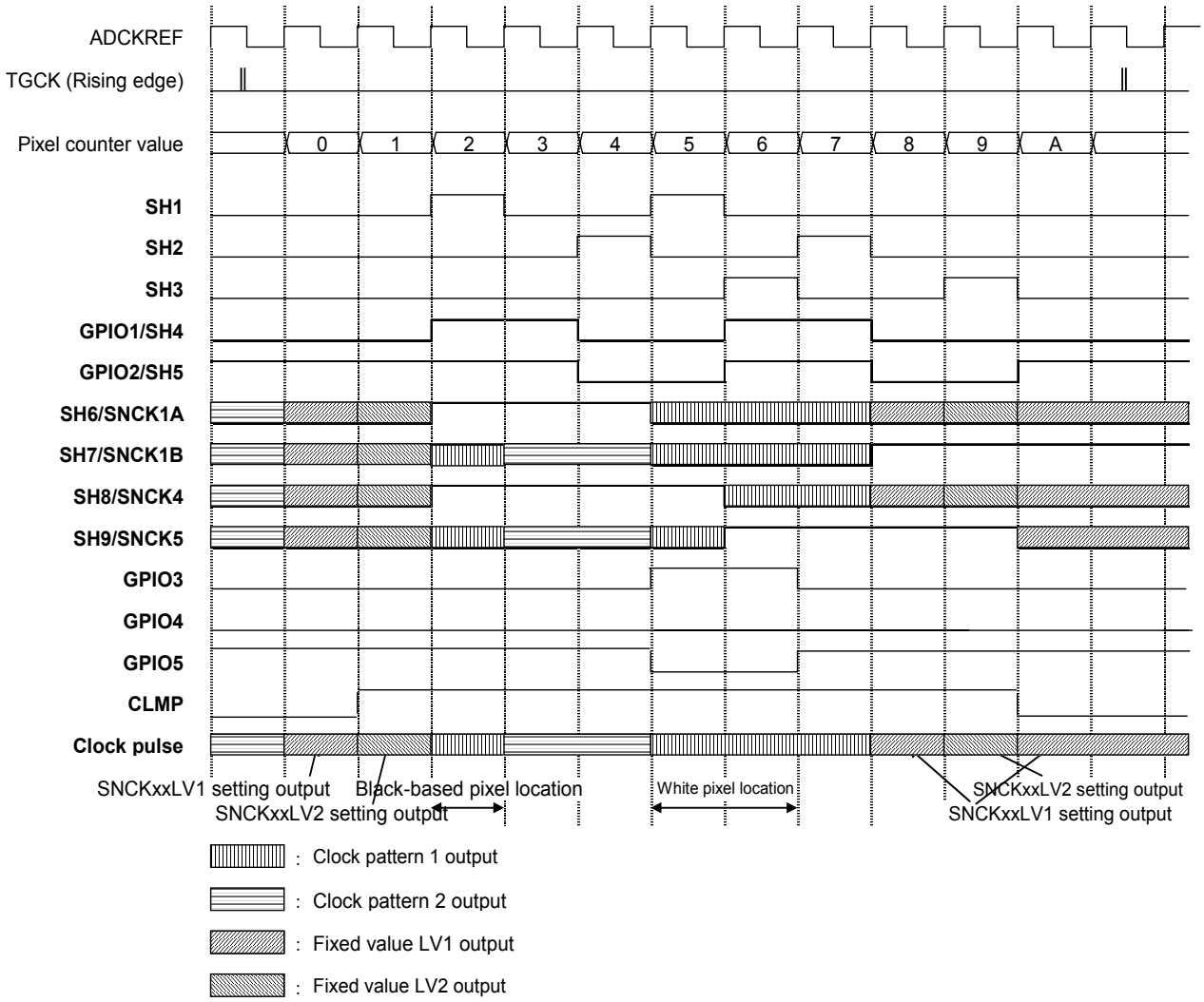


Figure 6.13 Operation example in single-channel mode

6.4.6 Clock Pulse Pattern Output

The pattern output of clock pulse signals (SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E, SNCK2, SNCK3, SNCK4, SNCK5, SNCK6, CK1, CK2, ADCK) outputs any pattern of signals specified by registers.
The clock pulses can be classified into line-sensor drive clock pulses and AFE clock pulses as follows.

- Line-sensor drive clock pulse
  - ・SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E, SNCK2, SNCK3, SNCK4, SNCK5, SNCK6
- AFE clock pulse
  - ・CK1, CK2, ADCK

Table 6.8 shows the pattern cycle, which varies depending on each clock pulse.

Table 6.8 Pattern cycle

Clock pulse	Pattern cycle	
	1/3 divider	1/6 divider
SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E	6T	12T
SNCK2, SNCK3, SNCK4, SNCK5, SNCK6	3T	6T
CK1, CK2, ADCK	6T(3T)	12T(6T)

(1) Clock pulse pattern output setting

The clock pulse pattern setting registers are listed on Table 6.9.

Table 6.9 Pattern setting register

Clock pulse	Pattern setting register	
	At pattern 1 output	At pattern 2 output
SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E, CK1, CK2, ADCK	SNCK1APAT00 (No.0x00) to ADCKPAT00 (No.0x07)	SNCK1APAT10 (No.0x08) to ADCKPAT10 (No.0x0F)
SNCK2, SNCK3, SNCK4, SNCK5, SNCK6,	SNCK2PAT00 (No.0x10) to SNCK6PAT00 (No.0x14)	SNCK2PAT00 (No.0x18) to SNCK6PAT00 (No.0x1C)

Be sure to set the SNCKPATEN bit in the PATEN register (No.0x53) to “1” before reading or writing PAT00 to PAT1F registers (No.0x00 to 0x1F). After reading or writing of registers has been completed, reset the SNCKPATEN bit to “0”. Set null codes (0x0000) in the line-sensor drive clock pulse pattern setting registers if not used.
Also set the output level in the fixed-value output period with the SNCK1ALV1 to SNCK6LV1 and SNCK1ALV2 to SNCK6LV2 bits in the SNCKCTL registers (No.0x55 to 56). Two types of fixed-value output settings, SNCK1ALV1 to SNCK6LV1 bits and SNCK1ALV2 to SNC6LV2 bits, are provided for each signal, and they are switched depending on the respective set values each time an event occurs.

(2) Line-sensor drive clock pulse pattern output at pattern 1 output

The following gives an example setup of line-sensor drive clock pulse pattern setting registers for single-channel and 12 dividing outputs and an example of output waveforms.

Table 6.10 Pattern 1 Setting Example in Single-Channel Mode

Bit / Register No.	Even cycle						ODD cycle						Reserved			
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
0x00 SNCK1APAT00	0	0	0	0	0	0	1	1	1	1	1	1	x	x	x	x
0x01 SNCK1BPAT00	1	1	1	1	1	1	0	0	0	0	0	0	x	x	x	x
0x05 CK1PAT00	0	0	0	1	0	0	0	0	0	1	0	0	x	x	x	x
0x06 CK2PAT00	0	0	0	0	0	1	0	0	0	0	0	1	x	x	x	x
0x07 ADCKPAT00	1	1	1	0	0	0	1	1	1	0	0	0	x	x	x	x
0x10 SNCK2PAT00	1	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
0x11 SNCK3PAT00	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: don't care

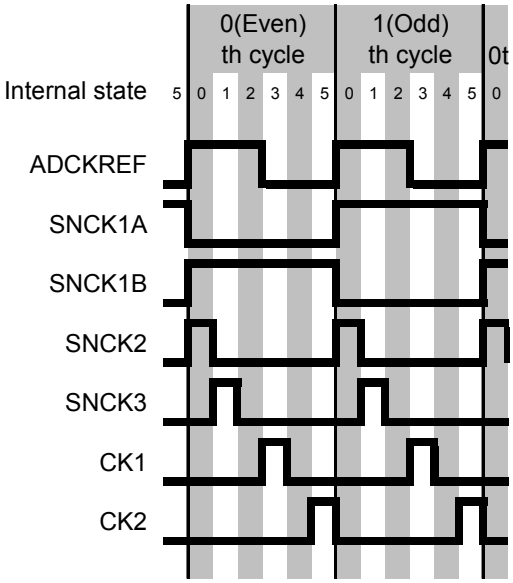


Figure 6.14 Example of Pattern 1 Output Waveforms in Single-channel Mode

(3) Line-sensor drive clock pulse pattern output at pattern 2 output
At pattern 2 output, use a state number other than the internal state number for pattern 1 output.
The output pattern is output in the same way as for pattern 1 as shown in Table 6.11.

Table 6.11 Output Pattern of Pattern 2 Output

Bit / Register No.	Even cycle						ODD cycle						Reserved			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0x08 SNCK1APAT10	0	0	0	0	0	0	1	1	1	1	1	1	x	x	x	x
0x09 SNCK1BPAT10	1	1	1	1	1	1	0	0	0	0	0	0	x	x	x	x
0x0D CK1PAT10	0	0	0	1	0	0	0	0	0	1	0	0	x	x	x	x
0x0E CK2PAT10	0	0	0	0	0	1	0	0	0	0	0	1	x	x	x	x
0x0F ADCKPAT10	1	1	1	0	0	0	1	1	1	0	0	0	x	x	x	x
0x18 SNCK2PAT10	1	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
0x19 SNCK3PAT10	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x

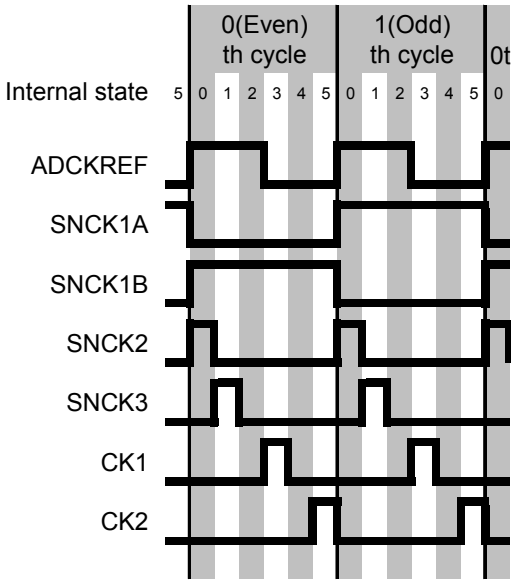


Figure 6.15 Example of Pattern 2 Output Waveforms in Single-channel Mode

(4) Function of switching the clock pulse pattern outputs of AFE clock pulses
The ADCK, CK1 and CK2 signals of AFE clock pulses can be output by switching pattern cycles. The output, usually set to EVEN/ODD cycles (6T/12T), can be set to EVEN cycle (3T/12T) only by setting the AFEDISOE bit of the TGCTL register (No.0x50) to "1".
As is the case with the SNCK signal, the AFE clock pulses stops ticking during the LV output of the event pattern register. By setting the AFECKOUT bit of the TGCTL register (No. 0x50) to "1", however, the clock can continue output the pattern 1 while the ADCKEN bit is turned "1". Use this setting when you cannot stop the clock of an AFE IC because of mounted PLL, etc.

6.4.7 SLINE Output Process

After the image capture enable signal (TGSTART bit) became active, the output process is performed by the external input of SLINE or register setting.
External input or internal generation of the SLINE signal can be selected by setting the INSLINE or MUXSLINE bit of the TGMD register (No.0x51). Setting the INSLINE bit to "0" internally generates the SLINE signal. Setting the INSLINE bit to "1" and the MUXSLINE bit to "1" assigns the rising edge to the external input and the falling edge to the internal generation. Setting the INSLINE bit to "1" and MUXSLINE bit to "0" generates the SLINE signal at the timing that was externally input by SLINEi. Table 6.12 shows the operation when the INSLINE and MUXSLINE bits are combined.
If the SLINE signal is internally generated or the rising edge is set to the external input and the falling edge to the internal generation, the number of lines in the sub operation direction is counted based on the TGCK signal after the TGSTART bit has became active, Start the output of the SLINE signal from the set value of the SLINEST register (No.0x40) and the setting portion of the SLINE_RISE bit of the event pattern setting registers (No.0x00 to 0x3F), and end the output of the SLINE signal from the set value of the SLINEEND register (No.0x41) and the setting portion of the event pattern setting registers (No.0x00 to 0x3F).
When externally generating the SLINE signal, synchronize the SLINE signal input at TGCK rising after the TGSTART bit has became active.
Figure 6.16 shows an operation example when the SLINE signal is internally generated with SLINEST=2 and SLINEEND=6. Figure 6.17 shows an operation example when the SLINE signal is internally generated.

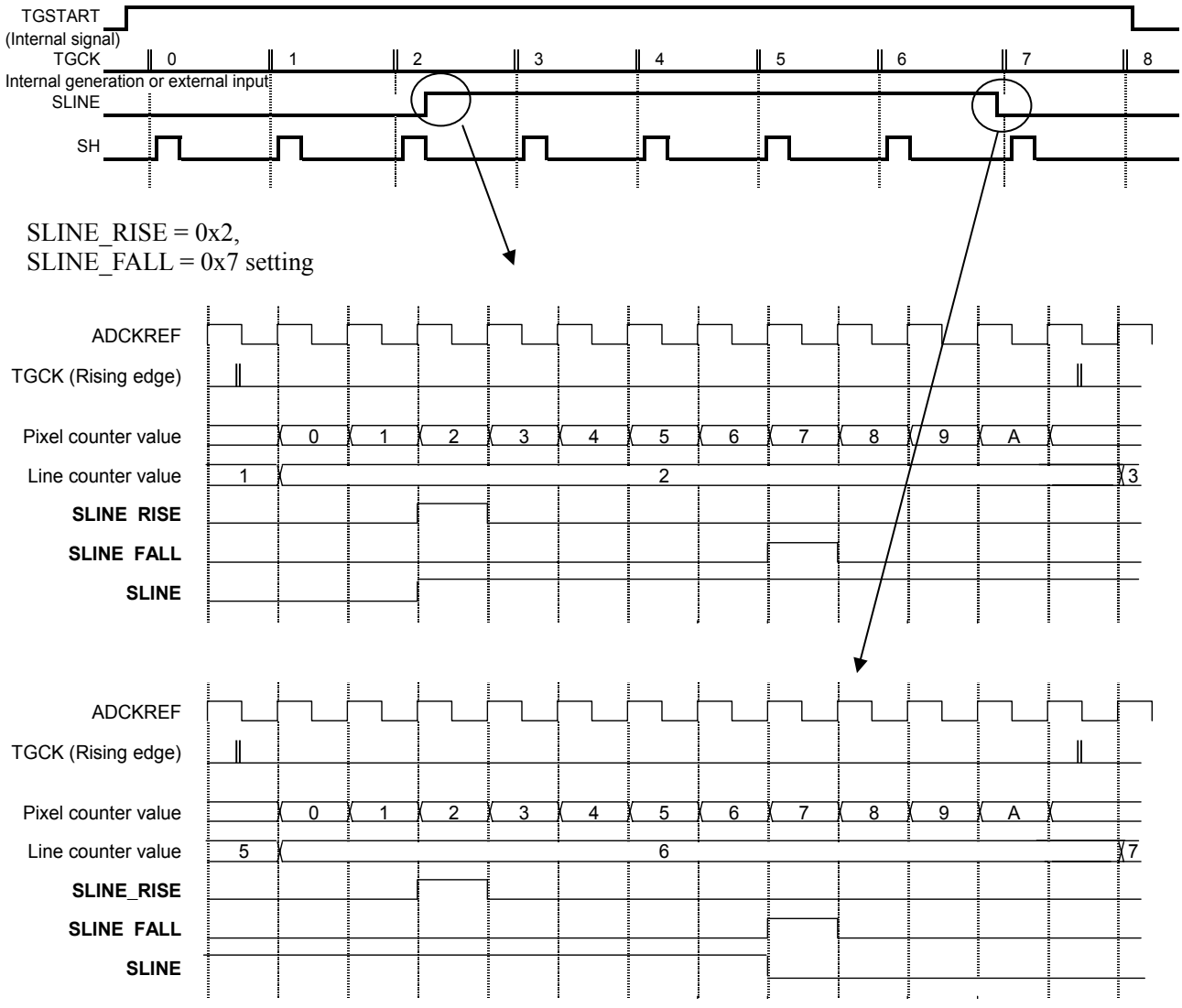


Figure 6.16 Example of internal generation of SLINE signal

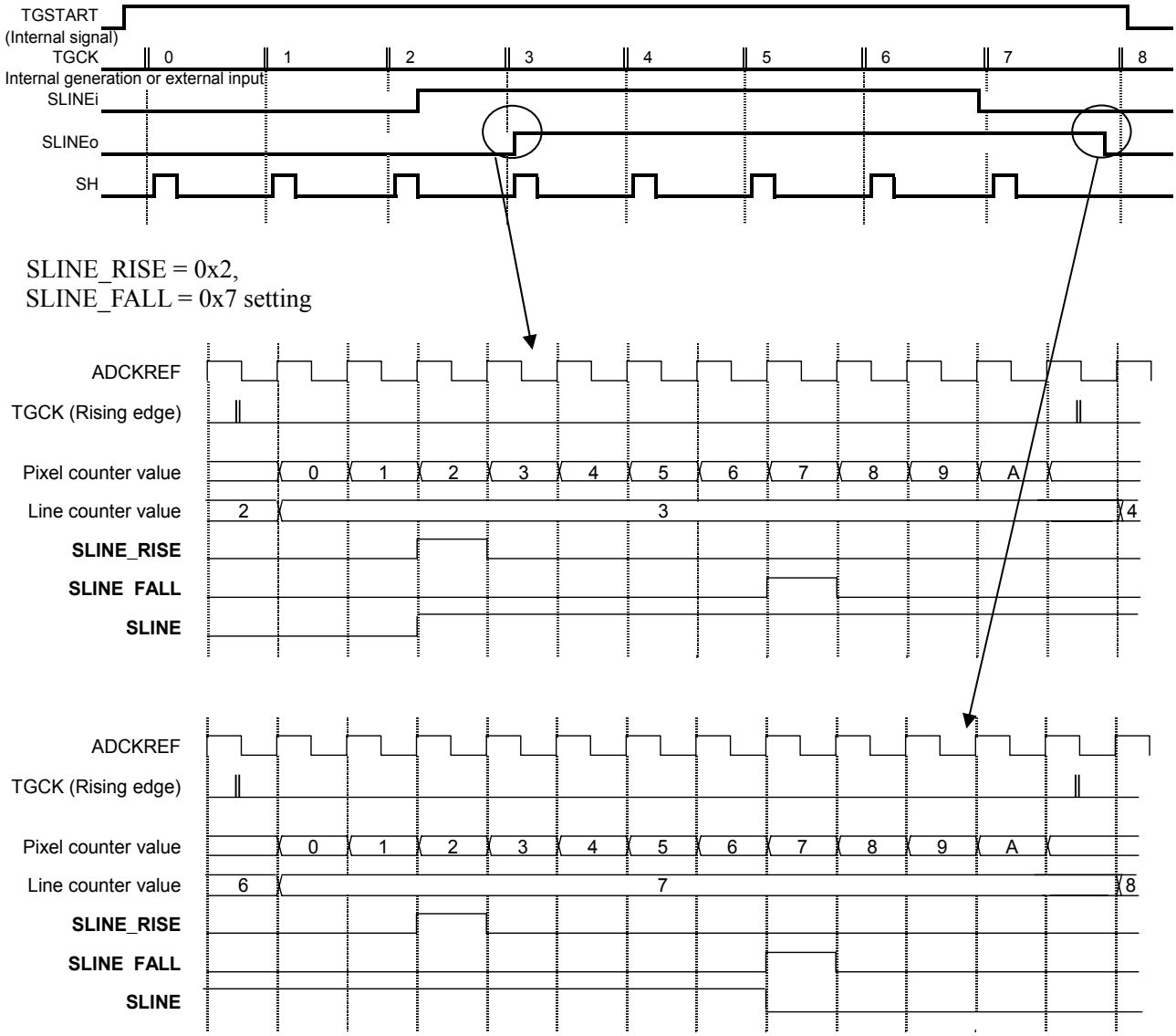


Figure 6.17 Example of external input of SLINE signal

Table 6.12 shows the operation when the INSLINE and MUXSLINE bits are combined

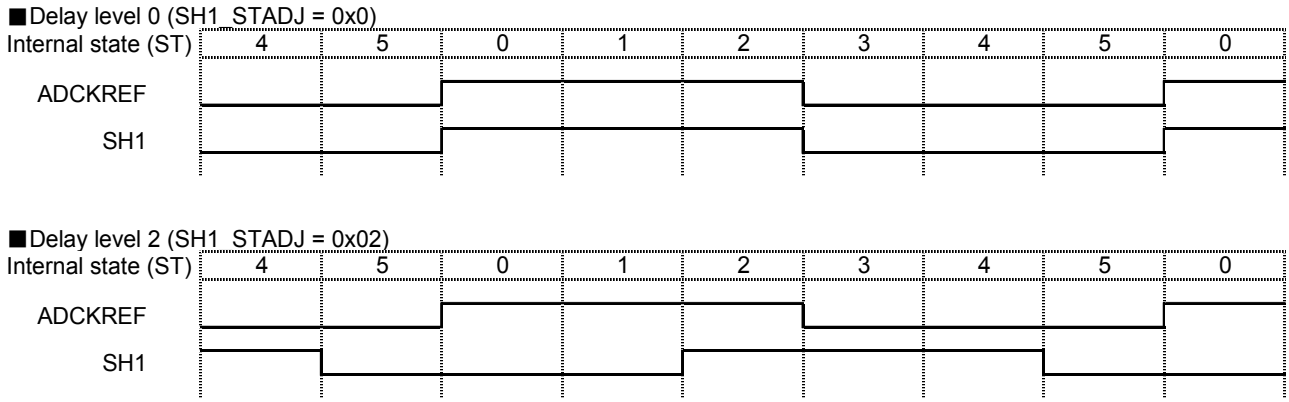
	Combination of INSLINE/MUXSLINE			
	"0/0"	**"0/1"**	**"1/0"**	**"1/1"**
SLINE_RISE generation method	Line counter input Timing + Pixel counter Delay output	Setting disabled	SLINEi input Timing + Pixel counter delay output	SLINEi input Timing + Pixel counter delay output
SLINE_FALL generation method	Line counter input Timing + Pixel counter delay output	Setting disabled	SLINEi input Timing + Pixel counter delay output	Line counter input Timing + Pixel counter delay output

6.4.8 Control Signal Output Delay Setting

(1) Delay in shift signal output

Set the delay amount in change timing of the SH1 to SH9 and CLMP to WHPIX signals by setting each bit of the SH_ADJ1 register (No.0x42) to SH_ADJ4 register (No.0x45). Based on the set value, the rise or fall timing of the SH1 to SH9 and CLMP to WHPIX signals is delayed by the set value × time T.

Figure 6.18 provides an example of output delay of the SH1 signal. Also, the same operation is performed for the SH2 to 9 and CLMP to WHPIX signals.



Pulse width: 1 pixel

Figure 6.18 Example of SH1 Signal Output Delay Amount Setting Operation

(2) Clock pulse output delay setting

Output of the clock pulse can be delayed. You can combine 3 types of delay settings individually for states 0 to 5. Combining register settings enables you to change the pulse width. The output delay can be specified with a T/10 phase clock for each state. Also, whether to output in normal mode or inversion mode can be selected. In this case, set the bit of the output clock, which is made effective based on Table 6.13, to "1".

Table 6.13 Correspondence between register bits and SNCK clocks

Correspondence between registers and SNCK clocks					
Bit name (No.0x49 to 0x4B)	**Corresponding clock**	**Bit name (No.0x4C to 0x4E)**	**Corresponding clock**	**Bit name (No.0x4C to 0x4E)**	**Corresponding State**
SNCK_CLKADJ*[9]	Phase clock 9 output enable	SNCK_INV*[9]	Phase clock 9 output enable in inversion mode	ADJ*_STATE[5]	State 5 output enable
SNCK_CLKADJ*[8]	Phase clock 8 output enable	SNCK_INV*[8]	Phase clock 8 output enable in inversion mode	ADJ*_STATE[4]	State 4 output enable
SNCK_CLKADJ*[7]	Phase clock 7 output enable	SNCK_INV*[7]	Phase clock 7 output enable in inversion mode	ADJ*_STATE[3]	State 3 output enable
SNCK_CLKADJ*[6]	Phase clock 6 output enable	SNCK_INV*[6]	Phase clock 6 output enable in inversion mode	ADJ*_STATE[2]	State 2 output enable
SNCK_CLKADJ*[5]	Phase clock 5 output enable	SNCK_INV*[5]	Phase clock 5 output enable in inversion mode	ADJ*_STATE[1]	State 1 output enable
SNCK_CLKADJ*[4]	Phase clock 4 output enable	SNCK_INV*[4]	Phase clock 4 output enable in inversion mode	ADJ*_STATE[0]	State 0 output enable
SNCK_CLKADJ*[3]	Phase clock 3 output enable	SNCK_INV*[3]	Phase clock 3 output enable in inversion mode		
SNCK_CLKADJ*[2]	Phase clock 2 output enable	SNCK_INV*[2]	Phase clock 2 output enable in inversion mode		
SNCK_CLKADJ*[1]	Phase clock 1 output enable	SNCK_INV*[1]	Phase clock 1 output enable in inversion mode		
SNCK_CLKADJ*[0]	Phase clock 0 output enable				

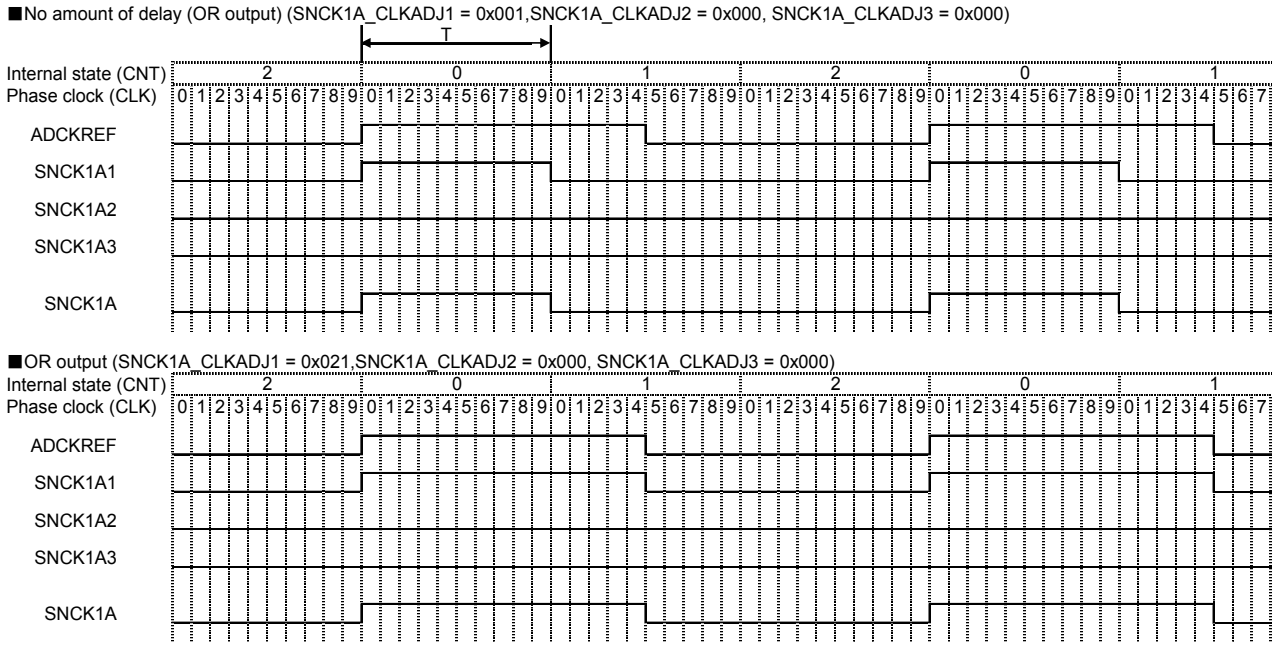


Figure 6.19 Example of SNCK1A signal OR output delay amount setting

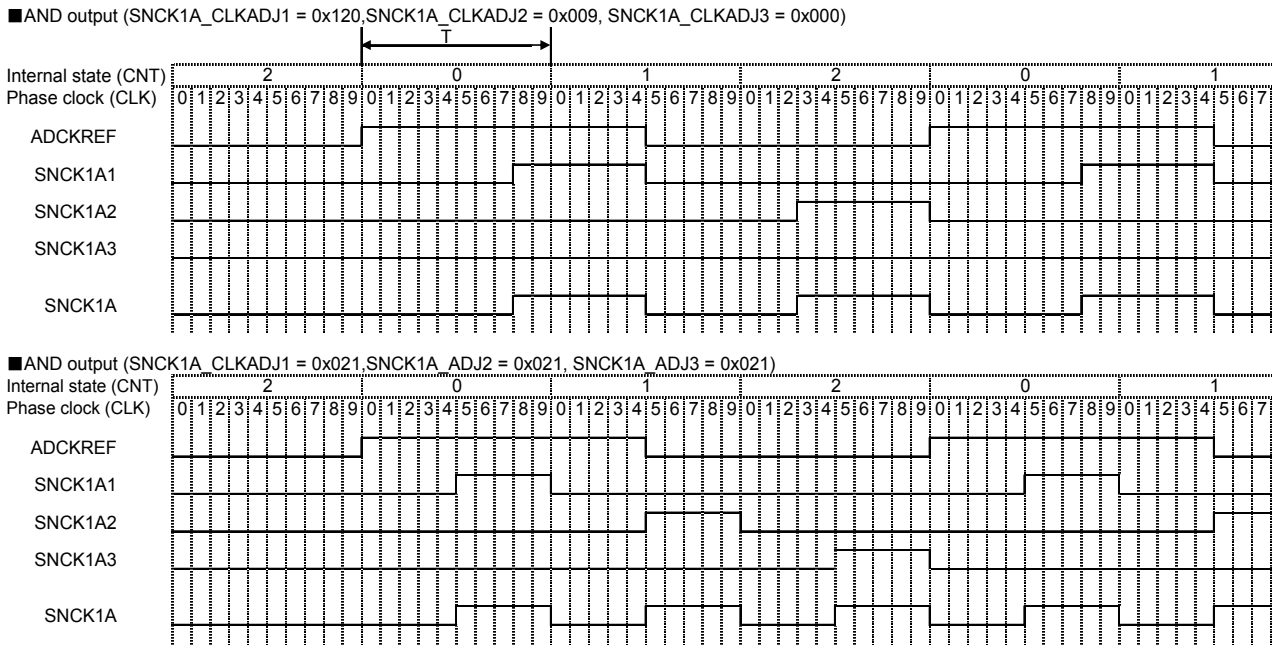


Figure 6.20 Example of SNCK1A signal AND output delay amount setting

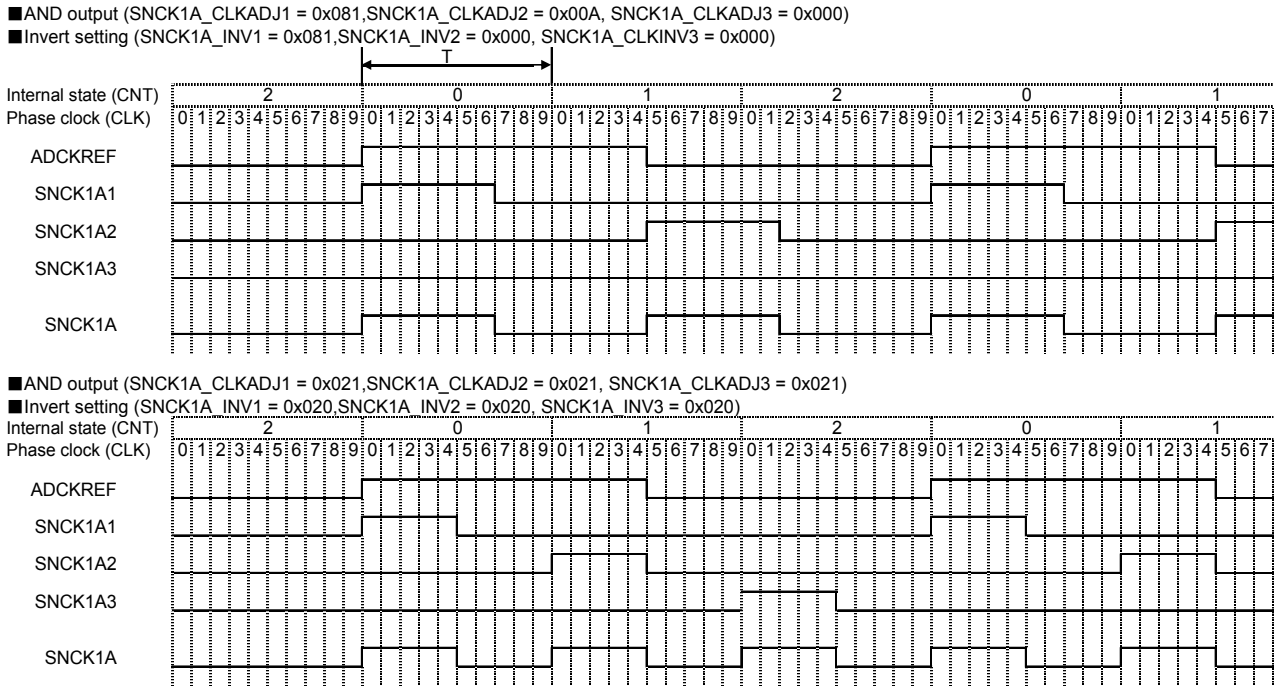


Figure 6.21 Example of SNCK1A signal AND inverted output delay amount setting

Before setting a delay setting register, set the SNCK_ADJ_PAGESEL register (No.0x48) and the register setting page must be switched.
Table 6.14 shows the register for setting the amount of delay of each signal and the page setting register.

Table 6.14 Clock pulse delay amount setting register

Signal Name	Setting of amount of delay				
	Page setting	Registers	Delay setting	AND/OR switching	Output logic invert switching
SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E	0x0	SNCK1A_CLKADJ/ SNCK1A_INV	SNCK1A_CLKADJ[9:0]	ANDxOR1A	SNCK1A_INV[9:1]
	0x1	SNCK1B_CLKADJ/ SNCK1B_INV	SNCK1B_CLKADJ[9:0]	ANDxOR1B	SNCK1B_INV[9:1]
	0x2	SNCK1C_CLKADJ/ SNCK1C_INV	SNCK1C_CLKADJ[9:0]	ANDxOR1C	SNCK1C_INV[9:1]
	0x3	SNCK1D_CLKADJ/ SNCK1D_INV	SNCK1D_CLKADJ[9:0]	ANDxOR1D	SNCK1D_INV[9:1]
	0x4	SNCK1E_CLKADJ/ SNCK1E_INV	SNCK1E_CLKADJ[9:0]	ANDxOR1E	SNCK1E_INV[9:1]
SNCK2, SNCK3, SNCK4, SNCK5, SNCK6	0x5	SNCK2_CLKADJ/ SNCK2_INV	SNCK2_CLKADJ[9:0]	ANDxOR2	SNCK2_INV[9:1]
	0x6	SNCK3_CLKADJ/ SNCK3_INV	SNCK3_CLKADJ[9:0]	ANDxOR3	SNCK3_INV[9:1]
	0x7	SNCK4_CLKADJ/ SNCK4_INV	SNCK4_CLKADJ[9:0]	ANDxOR4	SNCK4_INV[9:1]
	0x8	SNCK5_CLKADJ/ SNCK5_INV	SNCK5_CLKADJ[9:0]	ANDxOR5	SNCK5_INV[9:1]
	0x9	SNCK6_CLKADJ/ SNCK6_INV	SNCK6_CLKADJ[9:0]	ANDxOR6	SNCK6_INV[9:1]
CK1	0xA	CK1_CLKADJ/ CK1_INV	CK1_CLKADJ[9:0]	ANDxORCK1	CK1_INV[9:1]
CK2	0xB	CK2_CLKADJ/ CK2_INV	CK2_CLKADJ[9:0]	ANDxORCK2	CK2_INV[9:1]
ADCK	0xC	ADCK_CLKADJ/ ADCK_INV	ADCK_CLKADJ[9:0]	ANDxORA	ADCK_INV[9:1]

By setting “1” for the SNCKXXxSHX SNCKxSHCTL register (No.0x57), the SNCK signal is logically ORed with the SH signal.
Figure 6.22 shows the configuration diagram of the output delay circuit.

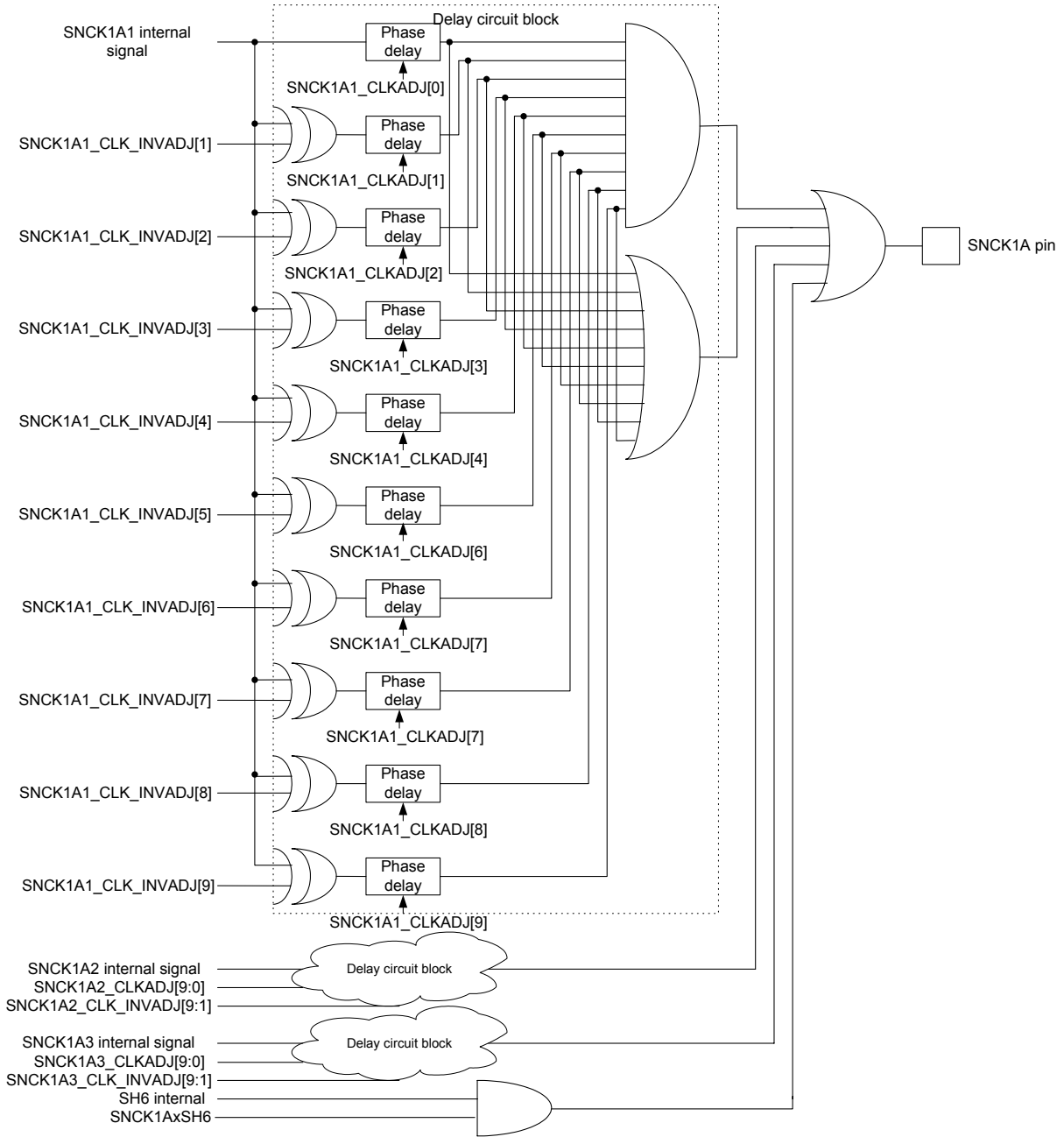


Figure 6.22 Output Delay Circuit

6.4.9 Control Signal Output Polarity Setting

Table 6.15 shows the register for setting polarities of the AFE transfer clock, some of the line-sensor drive clock pulses and shift signals.

Table 6.15 Control Signal Output Polarity Setting Register

Signal	Signal Name	Polarity setting	
		Registers	Bit
AFE transfer clock signal	CLMP	POLCTL(No.0x58)	CLMPPOL
Shift signal	SH1		SH1POL
	SH2		SH2POL
	SH3		SH3POL
	SH4		GPIO1POL
	SH5		GPIO2POL
	SH6		SH6POL
	SH7		SH7POL
	SH8		SH8POL
	SH9		SH9POL
	OBPIX		GPIO3POL
	SLINE		GPIO4POL
	WHPIX		GPIO5POL
Line sensor drive clock signal	SNCK1A	SNCKINV(No.0x54)	SNCK1AINV
	SNCK1B		SNCK1BINV
	SNCK1C		SNCK1CINV
	SNCK1D		SNCK1DINV
	SNCK1E		SNCK1EINV
	SNCK2		SNCK2INV
	SNCK3		SNCK3INV
	SNCK4		SNCK4INV
	SNCK5		SNCK5INV
	SNCK6		SNCK6INV

Restriction

If the SH6 to SH9 signals are used as the SNCK signal, the SNCK signal and the SH signal are logically ORed. Therefore, set SH6POL to SH9POL so that signal output logics are mutually exclusive.

6.4.10 Shared General-purpose Ports

Table 6.16 shows general-purpose ports shared with each control signal.
Effective setting of the general-purpose port function is controlled by the GPIOEN1/GPIOEN2 registers (No.0x59 to 5A). Setting "0" enables the pin that corresponds to the register bit to output the functional signal of the appropriate pin. Setting "1" enables the function of the general-purpose I/O port of the corresponding pin. Since the general-purpose port is set ("1" setting) for all signals at the time of initialization, set "0" for the appropriate bit of the GPIOEN1/GPIOEN2 registers (No.0x59 to 5A) when outputting a functional signal.
The general-purpose port configuration of the SNCK pin varies from the SH1 to 3/GPIO1 to 4 pins. For this reason, if the SNCK pin is used as the general-purpose port, set "0" for all of the output clock select bits of the SNCK_CLKADJ1 to 3/SNCK_INV1 to 3 registers (No.0x48 to 4E), and set "0" for the ANDxOR bit.
I/O switching of the general-purpose port is controlled by the GPIODIR1/GPIODIR2/GPIODIR3 registers (No.0x5B to 5D).
If the GPIODIR1/GPIODIR2 registers are set to "00", the pins corresponding to the registers turn to input ports. If the registers are set to "01" or "10", the pins turn to output ports. If you want to output functional signals, the registers must be set to "01" or "10" to turn the pins to the output state.
During the "01" setting, output current is set to 12 mA drive, and during the "10" setting, it is set to 24 mA drive. Thus settings can be changed according to output load.
If the GPIODIR3 register is set to "0", the pin corresponding to the register turns to an input port. If it is set to "1", the pin turns to an output port. If you want to output a functional signal, the register must be set to "1" to turn the pin to the output state.
If output is set for the appropriate pin, the signal output to the general-purpose port produces the value set in the register when the GPIOST1/GPIOST2 register (No.0x5E to 5F) is written. If you read the GPIOST1/GPIOST2 registers (No.0x5E to 5F), you can read the state of the corresponding pin regardless of the setting of the general-purpose port.

Table 6.16 General-purpose Port

<table>
<tr><th rowspan="2">Signal pin name</th><th colspan="4">General-purpose port control register</th></tr>
<tr><th>Enabling general-purpose port function</th><th>Switching general-purpose port I/O</th><th>General-purpose port output</th><th>General-purpose port input</th></tr>
<tr><td>SNCK1A/SH6</td><td rowspan="10">GPIOEN1(No.0x59)</td><td rowspan="10">GPIODIR1/GPIODIR2 (No.0x5B to 5C)</td><td rowspan="10">GPIOST1(No.0x5E)</td><td rowspan="10">GPIOST1(No.0x5E)</td></tr>
<tr><td>SNCK1B/SH7</td></tr>
<tr><td>SNCK1C/SH8</td></tr>
<tr><td>SNCK1D/SH9</td></tr>
<tr><td>SNCK1E</td></tr>
<tr><td>SNCK2/SH6</td></tr>
<tr><td>SNCK3/SH7</td></tr>
<tr><td>SNCK4/SH8</td></tr>
<tr><td>SNCK5/SH9</td></tr>
<tr><td>SNCK6</td></tr>
<tr><td>SH1</td><td rowspan="9">GPIOEN2(No.0x5A)</td><td rowspan="8">GPIODIR3(No.0x5D)</td><td rowspan="9">GPIOST2(No.0x5F)</td><td rowspan="9">GPIOST2(No.0x5F)</td></tr>
<tr><td>SH2</td></tr>
<tr><td>SH3</td></tr>
<tr><td>GPIO1/SH4</td></tr>
<tr><td>GPIO2/SH5</td></tr>
<tr><td>GPIO3</td></tr>
<tr><td>GPIO4</td></tr>
<tr><td>GPIO5</td><td></td></tr>
</table>

Figure 6.23 shows the internal connection for the general-purpose port of the SH1 signal. Similar connection is applied to the SH2, SH3, GPIO1, GPIO2, GPIO3 and GPIO4 pins.
Figure 6.24 shows the internal connection for the general-purpose port of the SNCK1A signal.
Similar connection is applied to the SNCK1B, SNCK1C, SNCK1D, SNCK1E, SNCK2, SNCK3, SNCK4, SNCK5 and SNCK6 pins.

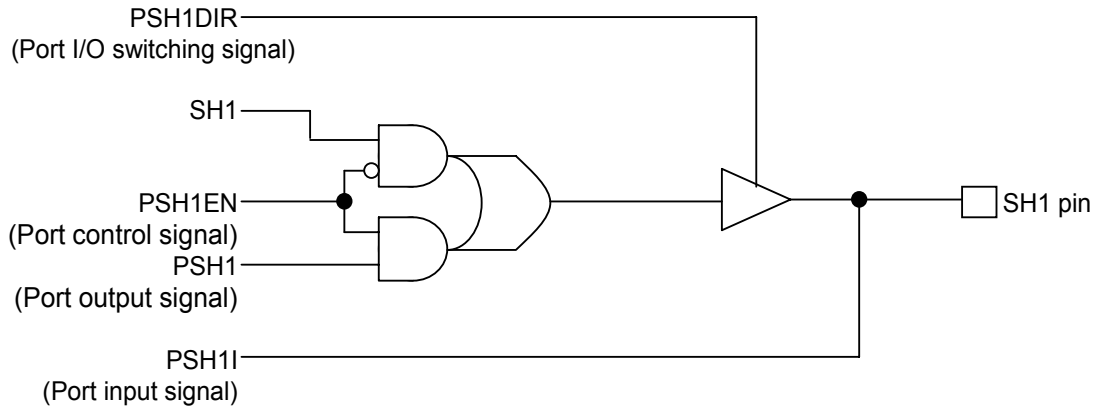


Figure 6.23 SH/GPIO General-purpose Port Internal Connection

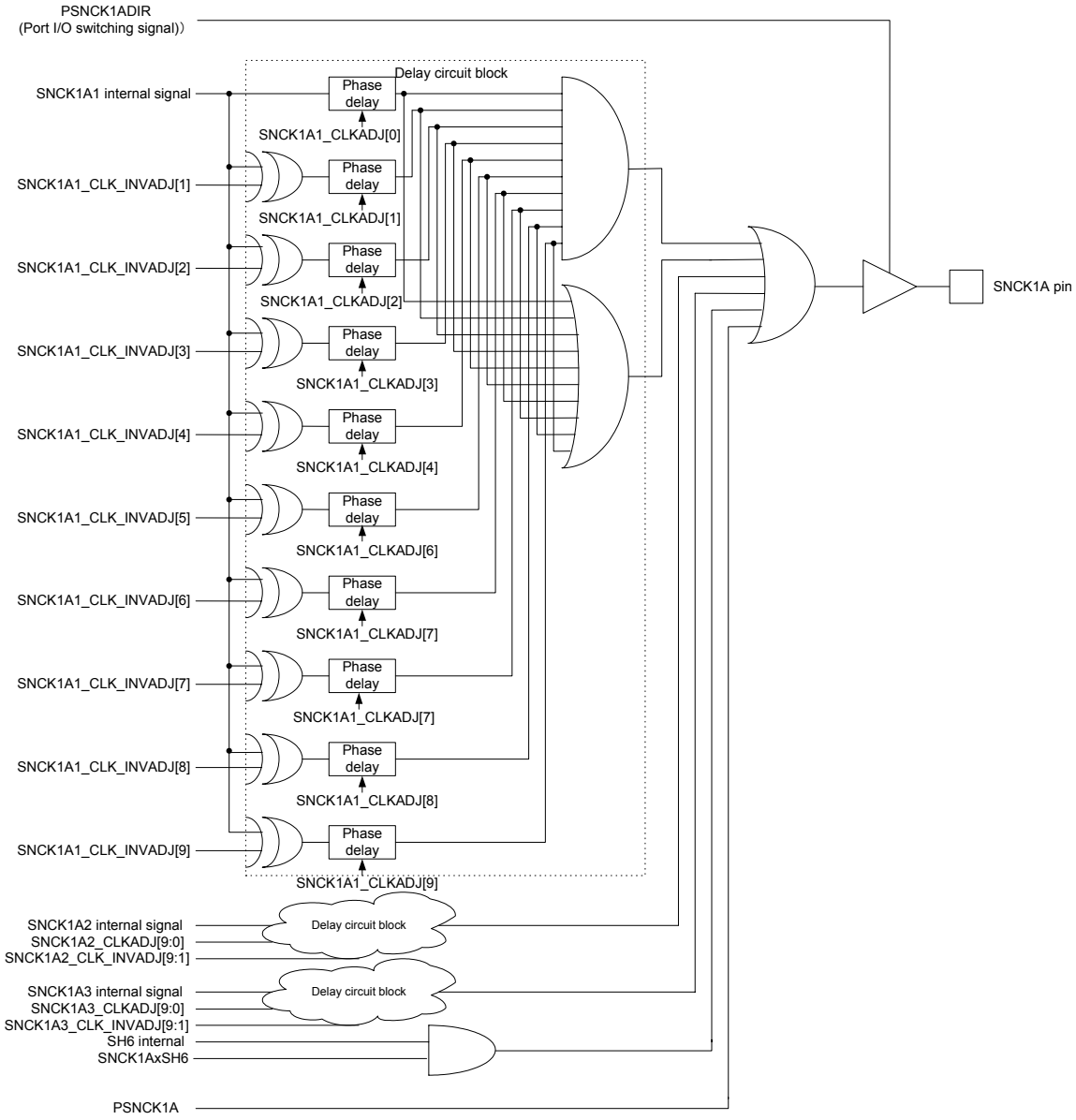


Figure 6.24 SNCK1A General-purpose Port Internal Connection

7. REGISTERS

7.1 Memory Map

No.	Address	Description			Size	Access Size
0x00	0x00	SNCK Pattern Registers (No.0x00 to 0x1F)	EVENT Pattern1 Registers (No.0x00 to 0x3F)	EVENT Pattern2 Registers (No.0x40 to 0x7F)	128B	16-bit
0x3F	0x7F	Reserved				
0x40	0x80	Timing Parameter Registers			32B	
0x4F	0x9F					
0x50	0xA0	Control Registers			32B	
0x5F	0xBF					
0x60	0xC0	Reserved			32B	
0x6F	0xDF					
0x70	0xE0	AFE & External Interface Registers			32B	
0x7F	0xFF					

7.2 Register Map

No.	Address	Register Name	R/W	Function
SNCK/Event Pattern Registers				
0x00	0x00	PAT00	R/W	Pattern setting register No.00
:	:	:	R/W	:
0x3F	0x7E	PAT3F	R/W	Pattern setting register No.3F
Timing Parameter Registers				
0x40	0x80	SLINEST	R/W	SLINE starting line setting register
0x41	0x82	SLINEEND	R/W	SLINE ending line setting refister
0x42	0x84	SH_ADJ1	R/W	Shift pulse signal output delay setting register 1
0x43	0x86	SH_ADJ2	R/W	Shift pulse signal output delay setting register 2
0x44	0x88	SH_ADJ3	R/W	Clock pulse signal output delay setting register 1
0x45	0x8A	SH_ADJ4	R/W	Clock pulse signal output delay setting register 2
0x46	0x8C	(Reserved)		
0x47	0x8E	(Reserved)		
0x48	0x90	SNCK_ADJ_PAGESE	R/W	Clock pulse delay setting page select register
0x49	0x92	SNCK_CLKADJ1	R/W	Clock pulse signal output delay setting register 1
0x4A	0x94	SNCK_CLKADJ2	R/W	Clock pulse signal output delay setting register 2
0x4B	0x96	SNCK_CLKADJ3	R/W	Clock pulse signal output delay setting register 3
0x4C	0x98	SNCK_INV1	R/W	Clock pulse inversion output delay setting register 1
0x4D	0x9A	SNCK_INV2	R/W	Clock pulse inversion output delay setting register 2
0x4E	0x9C	SNCK_INV3	R/W	Clock pulse inversion output delay setting register 3
0x4F	0x9E	(Reserved)		
Control Registers				
0x50	0xA0	TGCTL	R/W	Timing generation functional control register
0x51	0xA2	TGMD	R/W	Timing generation functional setting register
0x52	0xA4	STCTL	R/W	Internal state control register
0x53	0xA6	PATEN	R/W	Pattern setting control register
0x54	0xA8	SNCKINV	R/W	Line-sensor drive clock pulse polarity setting register
0x55	0xAA	SNCK1CTL	R/W	Line-sensor drive clock pulse pattern setting register 1
0x56	0xAC	SNCK2CTL	R/W	Line-sensor drive clock pulse pattern setting register 2
0x57	0xAE	SNCKxSHCTL	R/W	Line-sensor drive clock pulse output setting register
0x58	0xB0	POLCTL	R/W	Polarity control register
0x59	0xB2	GPIOEN1	R/W	General-purpose port control register 1
0x5A	0xB4	GPIOEN2	R/W	General-purpose port control register 2
0x5B	0xB6	GPIODIR1	R/W	General-purpose port I/O switching register 1
0x5C	0xB8	GPIODIR2	R/W	General-purpose port I/O switching register 2
0x5D	0xBA	GPIODIR3	R/W	General-purpose port I/O switching register 3
0x5E	0xBC	GPIOST1	R/W	General-purpose port register 1
0x5F	0xBE	GPIOST2	R/W	General-purpose port register 2
0x60	0xC0	(Reserved)		
0x61	0xC2	(Reserved)		
0x62	0xC4	(Reserved)		
0x63	0xC6	(Reserved)		
0x64	0xC8	(Reserved)		
0x65	0xCA	(Reserved)		
0x66	0xCC	(Reserved)		
0x67	0xCE	(Reserved)		
0x68	0xD0	(Reserved)		
0x69	0xD2	(Reserved)		
0x6A	0xD4	(Reserved)		
0x6B	0xD6	(Reserved)		
0x6C	0xD8	(Reserved)		
0x6D	0xDA	(Reserved)		
0x6E	0xDC	(Reserved)		
0x6F	0xDE	(Reserved)		
AFE & External Interface Registers				
0x70	0xE0	ANA_RESET	R/W	Analog module reset register
0x71	0xE2	(Reserved)		
0x72	0xE4	(Reserved)		
0x73	0xE6	(Reserved)		
0x76	0xE8	(Reserved)		
0x77	0xEA	(Reserved)		
0x76	0xEC	(Reserved)		
0x77	0xEE	(Reserved)		
0x78	0xF0	(Reserved)		
0x79	0xF2	(Reserved)		
0x7A	0xF4	(Reserved)		
0x7B	0xF6	(Reserved)		
0x7C	0xF8	(Reserved)		
0x7D	0xFA	(Reserved)		
0x7E	0xFC	(Reserved)		
0x7F	0xFE	PLL_IMGSIG_CTL	R/W	PLL/image output signal control register

7.3 Bit Map

No.	Address	Register Name	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SNCK/Event Pattern Registers																		
0x00	0x00	SNCK1APAT00					SNCK1A1PAT0B	SNCK1A1PAT0A	SNCK1A1PAT09	SNCK1A1PAT08	SNCK1A1PAT07	SNCK1A1PAT06	SNCK1A1PAT05	SNCK1A1PAT04	SNCK1A1PAT03	SNCK1A1PAT02	SNCK1A1PAT01	SNCK1A1PAT00
0x01	0x02	SNCK1BPAT00					SNCK1B1PAT0B	SNCK1B1PAT0A	SNCK1B1PAT09	SNCK1B1PAT08	SNCK1B1PAT07	SNCK1B1PAT06	SNCK1B1PAT05	SNCK1B1PAT04	SNCK1B1PAT03	SNCK1B1PAT02	SNCK1B1PAT01	SNCK1B1PAT00
0x02	0x04	SNCK1CPAT00					SNCK1C1PAT0B	SNCK1C1PAT0A	SNCK1C1PAT09	SNCK1C1PAT08	SNCK1C1PAT07	SNCK1C1PAT06	SNCK1C1PAT05	SNCK1C1PAT04	SNCK1C1PAT03	SNCK1C1PAT02	SNCK1C1PAT01	SNCK1C1PAT00
0x03	0x06	SNCK1DPAT00					SNCK1D1PAT0B	SNCK1D1PAT0A	SNCK1D1PAT09	SNCK1D1PAT08	SNCK1D1PAT07	SNCK1D1PAT06	SNCK1D1PAT05	SNCK1D1PAT04	SNCK1D1PAT03	SNCK1D1PAT02	SNCK1D1PAT01	SNCK1D1PAT00
0x04	0x08	SNCK1EPAT00					SNCK1E1PAT0B	SNCK1E1PAT0A	SNCK1E1PAT09	SNCK1E1PAT08	SNCK1E1PAT07	SNCK1E1PAT06	SNCK1E1PAT05	SNCK1E1PAT04	SNCK1E1PAT03	SNCK1E1PAT02	SNCK1E1PAT01	SNCK1E1PAT00
0x05	0x0A	CK1PAT00					CK11PAT0B	CK11PAT0A	CK11PAT09	CK11PAT08	CK11PAT07	CK11PAT06	CK11PAT05	CK11PAT04	CK11PAT03	CK11PAT02	CK11PAT01	CK11PAT00
0x06	0x0C	CK2PAT00					CK21PAT0B	CK21PAT0A	CK21PAT09	CK21PAT08	CK21PAT07	CK21PAT06	CK21PAT05	CK21PAT04	CK21PAT03	CK21PAT02	CK21PAT01	CK21PAT00
0x07	0x0E	ADCKPAT00					ADCK1PAT0B	ADCK1PAT0A	ADCK1PAT09	ADCK1PAT08	ADCK1PAT07	ADCK1PAT06	ADCK1PAT05	ADCK1PAT04	ADCK1PAT03	ADCK1PAT02	ADCK1PAT01	ADCK1PAT00
0x08	0x10	SNCK1APAT10					SNCK1A1PAT1B	SNCK1A1PAT1A	SNCK1A1PAT19	SNCK1A1PAT18	SNCK1A1PAT17	SNCK1A1PAT16	SNCK1A1PAT15	SNCK1A1PAT14	SNCK1A1PAT13	SNCK1A1PAT12	SNCK1A1PAT11	SNCK1A1PAT10
0x09	0x12	SNCK1BPAT10					SNCK1B1PAT1B	SNCK1B1PAT1A	SNCK1B1PAT19	SNCK1B1PAT18	SNCK1B1PAT17	SNCK1B1PAT16	SNCK1B1PAT15	SNCK1B1PAT14	SNCK1B1PAT13	SNCK1B1PAT12	SNCK1B1PAT11	SNCK1B1PAT10
0x0A	0x14	SNCK1CPAT10					SNCK1C1PAT1B	SNCK1C1PAT1A	SNCK1C1PAT19	SNCK1C1PAT18	SNCK1C1PAT17	SNCK1C1PAT16	SNCK1C1PAT15	SNCK1C1PAT14	SNCK1C1PAT13	SNCK1C1PAT12	SNCK1C1PAT11	SNCK1C1PAT10
0x0B	0x16	SNCK1DPAT10					SNCK1D1PAT1B	SNCK1D1PAT1A	SNCK1D1PAT19	SNCK1D1PAT18	SNCK1D1PAT17	SNCK1D1PAT16	SNCK1D1PAT15	SNCK1D1PAT14	SNCK1D1PAT13	SNCK1D1PAT12	SNCK1D1PAT11	SNCK1D1PAT10
0x0C	0x18	SNCK1EPAT10					SNCK1E1PAT1B	SNCK1E1PAT1A	SNCK1E1PAT19	SNCK1E1PAT18	SNCK1E1PAT17	SNCK1E1PAT16	SNCK1E1PAT15	SNCK1E1PAT14	SNCK1E1PAT13	SNCK1E1PAT12	SNCK1E1PAT11	SNCK1E1PAT10
0x0D	0x1A	CK1PAT10					CK11PAT1B	CK11PAT1A	CK11PAT19	CK11PAT18	CK11PAT17	CK11PAT16	CK11PAT15	CK11PAT14	CK11PAT13	CK11PAT12	CK11PAT11	CK11PAT10
0x0E	0x1C	CK2PAT10					CK21PAT1B	CK21PAT1A	CK21PAT19	CK21PAT18	CK21PAT17	CK21PAT16	CK21PAT15	CK21PAT14	CK21PAT13	CK21PAT12	CK21PAT11	CK21PAT10
0x0F	0x1E	ADCKPAT10					ADCK1PAT1B	ADCK1PAT1A	ADCK1PAT19	ADCK1PAT18	ADCK1PAT17	ADCK1PAT16	ADCK1PAT15	ADCK1PAT14	ADCK1PAT13	ADCK1PAT12	ADCK1PAT11	ADCK1PAT10
0x10	0x20	SNCK20PAT											SNCK21PAT05	SNCK21PAT04	SNCK21PAT03	SNCK21PAT02	SNCK21PAT01	SNCK21PAT00
0x11	0x22	SNCK30PAT											SNCK31PAT05	SNCK31PAT04	SNCK31PAT03	SNCK31PAT02	SNCK31PAT01	SNCK31PAT00
0x12	0x24	SNCK40PAT											SNCK41PAT05	SNCK41PAT04	SNCK41PAT03	SNCK41PAT02	SNCK41PAT01	SNCK41PAT00
0x13	0x26	SNCK50PAT											SNCK51PAT05	SNCK51PAT04	SNCK51PAT03	SNCK51PAT02	SNCK51PAT01	SNCK51PAT00
0x14	0x28	SNCK60PAT											SNCK61PAT05	SNCK61PAT04	SNCK61PAT03	SNCK61PAT02	SNCK61PAT01	SNCK61PAT00
0x15	0x2A	(Reserved)																
0x16	0x2C	(Reserved)																
0x17	0x2E	(Reserved)																
0x18	0x30	SNCK21PAT											SNCK21PAT15	SNCK21PAT14	SNCK21PAT13	SNCK21PAT12	SNCK21PAT11	SNCK21PAT10
0x19	0x32	SNCK31PAT											SNCK31PAT15	SNCK31PAT14	SNCK31PAT13	SNCK31PAT12	SNCK31PAT11	SNCK31PAT10
0x1A	0x34	SNCK41PAT											SNCK41PAT15	SNCK41PAT14	SNCK41PAT13	SNCK41PAT12	SNCK41PAT11	SNCK41PAT10
0x1B	0x36	SNCK51PAT											SNCK51PAT15	SNCK51PAT14	SNCK51PAT13	SNCK51PAT12	SNCK51PAT11	SNCK51PAT10
0x1C	0x38	SNCK61PAT											SNCK61PAT15	SNCK61PAT14	SNCK61PAT13	SNCK61PAT12	SNCK61PAT11	SNCK61PAT10
0x1D	0x3A	(Reserved)																
0x1E	0x3C	(Reserved)																
0x1F	0x3E	(Reserved)																
0x20	0x40	(Reserved)																
0x21	0x42	(Reserved)																
0x22	0x44	(Reserved)																
0x23	0x46	(Reserved)																
0x24	0x48	(Reserved)																
0x25	0x4A	(Reserved)																
0x26	0x4C	(Reserved)																
0x27	0x4E	(Reserved)																
0x28	0x50	(Reserved)																
0x29	0x52	(Reserved)																
0x2A	0x54	(Reserved)																
0x2B	0x56	(Reserved)																
0x2C	0x58	(Reserved)																
0x2D	0x5A	(Reserved)																
0x2E	0x5C	(Reserved)																
0x2F	0x5E	(Reserved)																
0x30	0x60	(Reserved)																
0x31	0x62	(Reserved)																
0x32	0x64	(Reserved)																
0x33	0x66	(Reserved)																
0x34	0x68	(Reserved)																
0x35	0x6A	(Reserved)																
0x36	0x6C	(Reserved)																
0x37	0x6E	(Reserved)																
0x38	0x70	(Reserved)																
0x39	0x72	(Reserved)																
0x3A	0x74	(Reserved)																
0x3B	0x76	(Reserved)																
0x3C	0x78	(Reserved)																
0x3D	0x7A	(Reserved)																
0x3E	0x7C	(Reserved)																
0x3F	0x7E	(Reserved)																
Timing Parameter Registers																		
0x40	0x80	SLINEST	SLINEST[15:0]															
0x41	0x82	SLINEEND	SLINEEND[15:0]															
0x42	0x84	SH_ADJ1		SH4_STADJ[2:0]				SH3_STADJ[2:0]				SH2_STADJ[2:0]				SH1_STADJ[2:0]		
0x43	0x86	SH_ADJ2		SH8_STADJ[2:0]				SH7_STADJ[2:0]				SH6_STADJ[2:0]				SH5_STADJ[2:0]		
0x44	0x88	SH_ADJ3														SH9_STADJ[2:0]		
0x45	0x8A	SH_ADJ4		WHPIX_STADJ[2:0]				OBPIX_STADJ[2:0]				SLINE_STADJ[2:0]				CLMP_STADJ[2:0]		
0x46	0x8C	(Reserved)																
0x47	0x8E	(Reserved)																
0x48	0x90	SNCK_ADJ_PAGESEL														SNCK_ADJ_PAGESEL		
0x49	0x92	SNCK_CLKADJ1	ANDxOR1						SNCK_CLKADJ1[9:0]									
0x4A	0x94	SNCK_CLKADJ2	ANDxOR2						SNCK_CLKADJ2[9:0]									
0x4B	0x96	SNCK_CLKADJ3	ANDxOR3						SNCK_CLKADJ3[9:0]									
0x4C	0x98	SNCK_INV1	ADJ1_STATE[5:0]										SNCK_INV1[9:1]					
0x4D	0x9A	SNCK_INV2	ADJ2_STATE[5:0]										SNCK_INV2[9:1]					
0x4E	0x9C	SNCK_INV3	ADJ3_STATE[5:0]										SNCK_INV3[9:1]					
0x4F	0x9E	(Reserved)																
Control Registers																		
0x50	0xA0	TGCTL							AFEDISOE	AFECKOUT	ADCKEN							TGSTART
0x51	0xA2	TGMD		TGCKWIDTH[2:0]		TGCKINV			MUXSLINE	INSLINE		INTGCK				TGCK_ADJ[2:0]		
0x52	0xA4	STCTL								STNUM		SYNCMD[1:0]					STADJ[3:0]	
0x53	0xA6	PATEN														EVENTPAT1EN	EVENTPAT0EN	SNCKPAT0EN
0x54	0xA8	SNCKINV				SNCK6INV	SNCK5INV	SNCK4INV	SNCK3INV	SNCK2INV				SNCK1EINV	SNCK1DINV	SNCK1CINV	SNCK1BINV	SNCK1AINV
0x55	0xAA	SNCK1CTL				SNCK1ELV2	SNCK1DLV2	SNCK1CLV2	SNCK1BLV2	SNCK1ALV2				SNCK1ELV1	SNCK1DLV1	SNCK1CLV1	SNCK1BLV1	SNCK1ALV1
0x56	0xAC	SNCK2CTL				SNCK6LV2	SNCK5LV2	SNCK4LV2	SNCK3LV2	SNCK2LV2				SNCK6LV1	SNCK5LV1	SNCK4LV1	SNCK3LV1	SNCK2LV1
0x57	0xAE	SNCKxSHCTL					SNCK5xSH9	SNCK4xSH8	SNCK3xSH7	SNCK2xSH6					SNCK1DxSH9	SNCK1CxSH8	SNCK1BxSH7	SNCK1AxSH6
0x58	0xB0	POLCTL	CLMPPOL	GPIO5POL	GPIO4POL	GPIO3POL				SH9POL	SH8POL	SH7POL	SH6POL	SH5POL	SH4POL	SH3POL	SH2POL	SH1POL
0x59	0xB2	GPIOEN1				PSNCK6EN	PSNCK5EN	PSNCK4EN	PSNCK3EN	PSNCK2EN				PSNCK1EEN	PSNCK1DEN	PSNCK1CEN	PSNCK1BEN	PSNCK1AEN
0x5A	0xB4	GPIOEN2	PCLMPEN	PADCKEN	PCK2EN	PCK1EN					PGPIO5EN	PGPIO4EN	PGPIO3EN	PGPIO2EN	PGPIO1EN	PSH3EN	PSH2EN	PSH1EN
0x5B	0xB6	GPIODIR1							PSNCK1EDIR		PSNCK1DDIR		PSNCK1CDIR		PSNCK1BDIR		PSNCK1ADIR	
0x5C	0xB8	GPIODIR2							PSNCK6DIR		PSNCK5DIR		PSNCK4DIR		PSNCK3DIR		PSNCK2DIR	
0x5D	0xBA	GPIODIR3	PCLMPDIR	PADCKDIR	PCK2DIR	PCK1DIR							PGPIO3DIR	PGPIO2DIR	PGPIO1DIR	PSH3DIR	PSH2DIR	PSH1DIR
0x5E	0xBC	GPIOST1				PSNCK6	PSNCK5	PSNCK4	PSNCK3	PSNCK2				PSNCK1E	PSNCK1D	PSNCK1C	PSNCK1B	PSNCK1A
0x5F	0xBE	GPIOST2	PCLMP	PADCK	PCK2	PCK1					PGPIO5	PGPIO4	PGPIO3	PGPIO2	PGPIO1	PSH3	PSH2	PSH1
0x60	0xC0	(Reserved)																
0x61	0xC2	(Reserved)																
0x62	0xC4	(Reserved)																
0x63	0xC6	(Reserved)																
0x64	0xC8	(Reserved)																
0x65	0xCA	(Reserved)																
0x66	0xCC	(Reserved)																
0x67	0xCE	(Reserved)																
0x68	0xD0	(Reserved)																
0x69	0xD2	(Reserved)																
0x6A	0xD4	(Reserved)																
0x6B	0xD6	(Reserved)																
0x6C	0xD8	(Reserved)																
0x6D	0xDA	(Reserved)																
0x6E	0xDC	(Reserved)																
0x6F	0xDE	(Reserved)																
AFE & External Interface Registers																		
0x70	0xE0	ANA_RESET				xPD_RSDS				xPD_PLL								
0x71	0xE2	(Reserved)																
0x72	0xE4	(Reserved)																
0x73	0xE6	(Reserved)																
0x74	0xE8	(Reserved)																
0x75	0xEA	(Reserved)																
0x76	0xEC	(Reserved)																
0x77	0xEE	(Reserved)																
0x78	0xF0	(Reserved)																
0x79	0xF2	(Reserved)																
0x7A	0xF4	(Reserved)																
0x7B	0xF6	(Reserved)																
0x7C	0xF8	(Reserved)																
0x7D	0xFA	(Reserved)																
0x7E	0xFC	(Reserved)														TESTMD		
0x7F	0xFE	PLL_IMGSIG_CTL	VCOSEL		RSEL1	RSEL0	CLKSEL[1:0]											

7.4 Detailed Description of Registers

7.4.1 0x00 to 0x3F Pattern Setting Registers No.00 to No.3F (PAT00 to PAT3F)

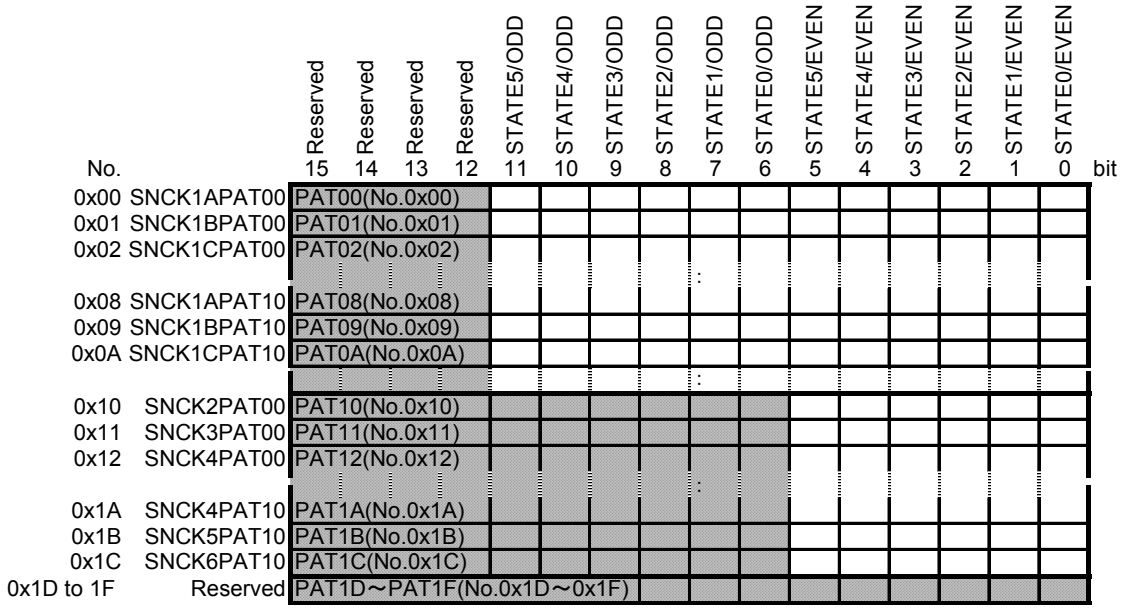
No.	Register Name	R/W	Bit Symbol	Description	Reset
0x00	PAT00	R/W	PAT00[15:0]	Pattern setting No.00	0xXXXX
0x01	PAT01		PAT01[15:0]	Pattern setting No.01	0xXXXX
:	:		:	:	:
0x3E	PAT3E		PAT3E[15:0]	Pattern setting No.3E	0xXXXX
0x3F	PAT3F		PAT3F[15:0]	Pattern setting No.3F	0xXXXX

These registers are used to set the line-sensor drive clock pulse pattern or event pattern. Each can be set by switching the SNCKPATEN, EVENTPAT0EN or EVENTPAT1EN bit to "1" in the PATEN register (No.0x53). If the SNCKPATEN bit is set to "1", the line sensor drive clock pulse pattern setting is made effective. If the EVENTPAT0PAT bit is set to "1", the event pattern setting (0 bank) is made effective. If the EVENTPAT1EN bit is set to "1", the event pattern setting (1 bank) is made effective.

(1) Line-sensor drive clock pulse pattern setting

(SNCKPATEN="1", EVENTPAT0EN="0", EVENTPAT1EN="0")

Sets the following line sensor drive clock pulse waveform patterns.
SNCK1A, SNCK1B, SNCK1C, SNCK1D, SNCK1E, SNCK2, SNCK3, SNCK4, SNCK5, SNCK6, CK1, CK2, ADCK
Bit array of the registers is shown below.



Restriction 1

Be sure to set the TGSTART bit to "0" in the TGCTL register (No.0x50) and set the SNCKPATEN bit to "1" in the PATEN register (No.0x53) before accessing these registers. Also, always reset the SNCKPATEN bit to "0" after you have completed to access the registers.

Restriction 2

If the TGSTART bit is set to "1" in the TGCTL register (No.0x50), setting the SNCKPATEN bit to "1" in the PATEN register (No.0x53) is not allowed.

Restriction 3

Setting all of the SNCKPATEN, EVENTPAT0EN and EVENTPAT1EN bits simultaneously to "1" in the PATEN register (No.0x53) is not allowed. Make sure only single bank is effective at a time.

(2) Event pattern setting (SNCKPATEN= “0”, EVENTPAT0EN or EVENTPAT1EN = “1”)
Sets various event generation timing. Bit array of the registers is shown below.

BANK0(EVENTPAT0EN=“1”, EVENTPAT1EN=“0”)

No.	15 WHPIX	14 OBPIX	13 SNCKCTL[1]	12 SNCKCTL[0]	11 CLMP	10 SLINE_FALL	9 SLINE_RISE	8 SH9	7 SH8	6 SH7	5 SH6	4 SH5	3 SH4	SH3	... SH2	0 SH1	15 PIXNUM[15]	...	0 PIXNUM[0]	bit
0x00							PAT01(No.0x01)										PAT00(No.0x00)			
0x02							PAT03(No.0x03)										PAT02(No.0x02)			
:							:										:			
0x3C							PAT3D(No.3D)										PAT3C(No.0x3C)			
0x3E							PAT3F(No.3F)										PAT3E(No.0x3E)			

BANK1(EVENTPAT0EN=“0”, EVENTPAT1EN=“1”)

No.	15 WHPIX	14 OBPIX	13 SNCKCTL[1]	12 SNCKCTL[0]	11 CLMP	10 SLINE_FALL	9 SLINE_RISE	8 SH9	7 SH8	6 SH7	5 SH6	4 SH5	3 SH4	SH3	... SH2	0 SH1	15 PIXNUM[15]	...	0 PIXNUM[0]	bit
0x00							PAT41(No.0x41)										PAT40(No.0x40)			
0x02							PAT43(No.0x43)										PAT42(No.0x42)			
:							:										:			
0x3C							PAT7D(No.7D)										PAT7C(No.0x7C)			
0x3E							PAT7F(No.7F)										PAT7E(No.0x7E)			

Restriction 1
Be sure to set the TGSTART bit to “0” in the TGCTL register (No.0x50) and set the EVENTPAT0EN or EVENTPAT1EN bit to “1” in the PATEN register (No.0x53) before accessing these registers. After completing access, set the EVENTPAT0EN or EVENTPAT1EN bit to “0”.

Restriction 2
If the TGSTART bit is set to “1” in the TGCTL register (No.0x50), setting the EVENTPAT0EN or EVENTPAT1EN bit to “1” in the PATEN register (No.0x53) is not allowed.

Restriction 3
Setting all of the SNCKPATEN, EVENTPAT0EN and EVENTPAT1EN bits simultaneously to “1” in the PATEN register (No.0x53) is not allowed. Make sure only single bank is effective at a time.

7.4.2 0x40 SLINE Starting Line Setting Register (SLINEST)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x40	SLINEST	R/W	15: SLINEST[15]	SLINE starting line setting	0x0000
			14: SLINEST[14]		
			13: SLINEST[13]		
			12: SLINEST[12]		
			11: SLINEST[11]		
			10: SLINEST[10]		
			9: SLINEST[9]		
			8: SLINEST[8]		
			7: SLINEST[7]		
			6: SLINEST[6]		
			5: SLINEST[5]		
			4: SLINEST[4]		
			3: SLINEST[3]		
			2: SLINEST[2]		
			1: SLINEST[1]		
			0: SLINEST[0]		

Register used to set the rising line output timing when internally generating the SLINE signal.

Restriction

The set value must not exceed the value of the SLINEEND register.

7.4.3 0x41 SLINE Ending Line Setting Register (SLINEEND)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x41	SLINEEND	R/W	15: SLINEEND[15]	SLINE ending line setting	0x0000
			14: SLINEEND[14]		
			13: SLINEEND[13]		
			12: SLINEEND[12]		
			11: SLINEEND[11]		
			10: SLINEEND[10]		
			9: SLINEEND[9]		
			8: SLINEEND[8]		
			7: SLINEEND[7]		
			6: SLINEEND[6]		
			5: SLINEEND[5]		
			4: SLINEEND[4]		
			3: SLINEEND[3]		
			2: SLINEEND[2]		
			1: SLINEEND[1]		
			0: SLINEEND[0]		

Register used to set the falling line output timing when internally generating the SLINE signal.

Restriction

The set value must not exceed the 0xFFFD value of the SLINEEND register.

7.4.4 0x42 Shift Pulse Signal Output Delay Setting Register 1 (SH_ADJ1)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x42	SH_ADJ1		15:		0x0000
		R/W	14: SH4_ADJ[2]	SH4 signal output delay setting	
			13: SH4_ADJ[1]		
			12: SH4_ADJ[0]		
			11:		
		R/W	10: SH3_ADJ[2]	SH3 signal output delay setting	
			9: SH3_ADJ[1]		
			8: SH3_ADJ[0]		
			7:		
		R/W	6: SH2_ADJ[2]	SH2 signal output delay setting	
			5: SH2_ADJ[1]		
			4: SH2_ADJ[0]		
			3:		
		R/W	2: SH1_ADJ[2]	SH1 signal output delay setting	
			1: SH1_ADJ[1]		
			0: SH1_ADJ[0]		

This register sets the amount of delay of the SH1/SH2/SH3/SH4 signal.

Bit15 Reserved

Bit14 to 12 SH4_ADJ[2:0]
Sets the output delay amount of the SH4 signal.

Bit11 Reserved

Bit10 to 8 SH3_ADJ[2:0]
Sets the output delay amount of the SH3 signal.

Bit7 Reserved

Bit6 to 4 SH2_ADJ[2:0]
Sets the output delay amount of the SH2 signal.

Bit3 Reserved

Bit2 to 0 SH1_ADJ[2:0]
Sets the output delay amount of the SH1 signal.

Restriction

The setting range is as follows, depending on the drive pattern resolution setting.
During 6 dividings: 0x00 to 0x05
During 3 dividings: 0x00 to 0x02

7.4.5 0x43 Shift Pulse Signal Output Delay Setting Register 2 (SH_ADJ2)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x43	SH_ADJ2		15:		0x0000
		R/W	14: SH8_ADJ[2]	SH8 signal output delay setting	
			13: SH8_ADJ[1]		
			12: SH8_ADJ[0]		
			11:		
		R/W	10: SH7_ADJ[2]	SH7 signal output delay setting	
			9: SH7_ADJ[1]		
			8: SH7_ADJ[0]		
			7:		
		R/W	6: SH6_ADJ[2]	SH6 signal output delay setting	
			5: SH6_ADJ[1]		
			4: SH6_ADJ[0]		
			3:		
		R/W	2: SH5_ADJ[2]	SH5 signal output delay setting	
			1: SH5_ADJ[1]		
			0: SH5_ADJ[0]		

This register sets the amount of delay of the SH5/SH6/SH7/SH8 signal.

Bit15 Reserved

Bit14 to 12 SH8_ADJ[2:0]
Sets the output delay amount of the SH8 signal.

Bit11 Reserved

Bit10 to 8 SH7_ADJ[2:0]
Sets the output delay amount of the SH7 signal.

Bit7 Reserved

Bit6 to 4 SH6_ADJ[2:0]
Sets the output delay amount of the SH6 signal.

Bit3 Reserved

Bit2 to 0 SH5_ADJ[2:0]
Sets the output delay amount of the SH5 signal.

Restriction

The setting range is as follows, depending on the drive pattern resolution setting.
During 6 dividings: 0x00 to 0x05
During 3 dividings: 0x00 to 0x02

7.4.6 0x44 Shift Pulse Signal Output Delay Setting Register 3 (SH_ADJ3)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x44	SH_ADJ3		15:		0x0000
			14:		
			13:		
			12:		
			11:		
			10:		
			9:		
			8:		
			7:		
			6:		
			5:		
			4:		
			3:		
		R/W	2: SH9_ADJ[2]	SH9 signal output delay setting	
			1: SH9_ADJ[1]		
			0: SH9_ADJ[0]		

This register sets the amount of delay of the SH9 signal.

Bit15 to 3 Reserved

Bit2 to 0 SH9_ADJ[2:0]
Sets the output delay amount of the SH9 signal.

Restriction
The setting range is as follows, depending on the drive pattern resolution setting.
During 6 dividings: 0x00 to 0x05
During 3 dividings: 0x00 to 0x02

7.4.7 0x45 Shift Pulse Signal Output Delay Setting Register 4 (SH_ADJ4)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x45	SH_ADJ4		15:		0x0000
		R/W	14: WHPIX_ADJ[2]	WHPIX signal output delay setting	
			13: WHPIX_ADJ[1]		
			12: WHPIX_ADJ[0]		
			11:		
		R/W	10: OBPIX_ADJ[2]	OBPIX signal output delay setting	
			9: OBPIX_ADJ[1]		
			8: OBPIX_ADJ[0]		
			7:		
		R/W	6: SLINE_ADJ[2]	SLINE signal output delay setting	
			5: SLINE_ADJ[1]		
			4: SLINE_ADJ[0]		
			3:		
		R/W	2: CLMP_ADJ[2]	SH4 signal output delay setting	
			1: CLMP_ADJ[1]		
			0: CLMP_ADJ[0]		

This register sets the amount of delay of the WHPIX/SLINE/BKDMY/CLMP signal.

Bit15 Reserved

Bit14 to 12 WHPIX_ADJ[2:0]
Sets the output delay amount of the WHPIX signal.

Bit11 Reserved

Bit10 to 8 OBPIX_ADJ[2:0]
Sets the output delay amount of the OBPIX signal.

Bit7 Reserved

Bit6 to 4 SLINE_ADJ[2:0]
Sets the output delay amount of the SLINE signal.

Bit3 Reserved

Bit2 to 0 CLMP_ADJ[2:0]
Sets the output delay amount of the CLMP signal.

Restriction

The setting range is as follows, depending on the drive pattern resolution setting.
During 6 dividings: 0x00 to 0x05
During 3 dividings: 0x00 to 0x02

7.4.8 0x48 Clock Pulse Delay Setting Page Select Register (SNCK_ADJ_PAGESEL)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x48	SNCK_ADJ_PAGESEL		15:		0x0000
			14:		
			13:		
			12:		
			11:		
			10:		
			9:		
			8:		
			7:		
			6:		
			5:		
			4:		
		R/W	3: SNCK_ADJ_PAGESEL[3]	SNCK_CLKADJ page selection	
			2: SNCK_ADJ_PAGESEL[2]		
			1: SNCK_ADJ_PAGESEL[1]		
			0: SNCK_ADJ_PAGESEL[0]		

This register selects the page of the clock pulse delay amount setting register.

SNCK_ADJ_PAGESEL[3:0]: Delay time

00: Selects the SNCK1A setting register.
01: Selects the SNCK1B setting register.
02: Selects the SNCK1C setting register.
03: Selects the SNCK1D setting register.
04: Selects the SNCK1E setting register.
05: Selects the SNCK2 setting register.
06: Selects the SNCK3 setting register.
07: Selects the SNCK4 setting register.
08: Selects the SNCK5 setting register.
09: Selects the SNCK6 setting register.
0A: Selects the CK1 setting register.
0B: Selects the CK2 setting register.
0C: Selects the ADCK setting register.

7.4.9 0x49 Clock Pulse Output Delay Setting Register 1 (SNCK_ADJ1)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x49	SNCK_ADJ1	R/W	15: ANDxOR1	0: OR	1: AND	0x0000
			14:			
			13:			
			12:			
			11:			
			10:			
		R/W	9: SNCK_CLKADJ1[9]	SNCK output delay amount setting 1		
			8: SNCK_CLKADJ1[8]			
			7: SNCK_CLKADJ1[7]			
			6: SNCK_CLKADJ1[6]			
			5: SNCK_CLKADJ1[5]			
			4: SNCK_CLKADJ1[4]			
			3: SNCK_CLKADJ1[3]			
			2: SNCK_CLKADJ1[2]			
			1: SNCK_CLKADJ1[1]			
			0: SNCK_CLKADJ1[0]			

Sets the output delay amount for the corresponding clock pulse signal. Output can be delayed for the state set in the ADJ1_STATE[5:0] register by the time shown below by setting.

*****_ADJ[9:0]: Delay time
- 00: No output
- 01: Output without delay
- 02: 1/10T delay output
- 04: 2/10T delay output
- 08: 3/10T delay output
- 10: 4/10T delay output
- 20: 5/10T delay output
- 40: 6/10T delay output
- 80: 7/10T delay output
- 100: 8/10T delay output
- 200: 9/10T delay output

Bit15 ANDxOR1
Switches the delay circuit of the SNCK signal.

Bit14 to 10 Reserved

Bit9 to 0 SNCK_CLKADJ1[9:0]
Sets the output delay amount of the SNCK signal.

7.4.10 0x4A Clock Pulse Output Delay Setting Register 2 (SNCK_ADJ2)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x4A	SNCK_ADJ2	R/W	15: ANDxOR2	0: OR	1: AND	0x0000
			14:			
			13:			
			12:			
			11:			
			10:			
		R/W	9: SNCK_CLKADJ2[9]	SNCK output delay amount setting		
			8: SNCK_CLKADJ2[8]			
			7: SNCK_CLKADJ2[7]			
			6: SNCK_CLKADJ2[6]			
			5: SNCK_CLKADJ2[5]			
			4: SNCK_CLKADJ2[4]			
			3: SNCK_CLKADJ2[3]			
			2: SNCK_CLKADJ2[2]			
			1: SNCK_CLKADJ2[1]			
			0: SNCK_CLKADJ2[0]			

Sets the output delay amount for the corresponding clock pulse signal. Output can be delayed for the state set in the ADJ2_STATE[5:0] register by the time shown below by setting.

*****_ADJ[9:0]: Delay time
00: No output
01: Output without delay
02: 1/10T delay output
04: 2/10T delay output
08: 3/10T delay output
10: 4/10T delay output
20: 5/10T delay output
40: 6/10T delay output
80: 7/10T delay output
100: 8/10T delay output
200: 9/10T delay output

Bit15 ANDxOR2
Switches the delay circuit of the SNCK signal.

Bit14 to 10 Reserved

Bit9 to 0 SNCK_CLKADJ2[9:0]
Sets the output delay amount of the SNCK signal.

7.4.11 0x4B Clock Pulse Output Delay Setting Register 3 (SNCK_ADJ3)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x4B	SNCK_ADJ3	R/W	15: ANDxOR3	0: OR	1: AND	0x0000
			14:			
			13:			
			12:			
			11:			
			10:			
		R/W	9: SNCK_CLKADJ3[9]	SNCK output delay amount setting		
			8: SNCK_CLKADJ3[8]			
			7: SNCK_CLKADJ3[7]			
			6: SNCK_CLKADJ3[6]			
			5: SNCK_CLKADJ3[5]			
			4: SNCK_CLKADJ3[4]			
			3: SNCK_CLKADJ3[3]			
			2: SNCK_CLKADJ3[2]			
			1: SNCK_CLKADJ3[1]			
			0: SNCK_CLKADJ3[0]			

Sets the output delay amount for the corresponding clock pulse signal. Output can be delayed for the state set in the ADJ3_STATE[5:0] register by the time shown below by setting.

*****_ADJ[9:0]: Delay time
00: No output
01: Output without delay
02: 1/10T delay output
04: 2/10T delay output
08: 3/10T delay output
10: 4/10T delay output
20: 5/10T delay output
40: 6/10T delay output
80: 7/10T delay output
100: 8/10T delay output
200: 9/10T delay output

Bit15 ANDxOR3
Switches the delay circuit of the SNCK signal.

Bit14 to 10 Reserved

Bit9 to 0 SNCK_CLKADJ3[9:0]
Sets the output delay amount of the SNCK signal.

7.4.12 0x4C Clock Pulse Inverted Output Delay Setting Register 1 (SNCK_INV1)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x4C	SNCK_INV1	R/W	15: ADJ1_STATE[5]	SNCK delay output state selection	0x0000
			14: ADJ1_STATE[4]		
			13: ADJ1_STATE[3]		
			12: ADJ1_STATE[2]		
			11: ADJ1_STATE[1]		
			10: ADJ1_STATE[0]		
			9: SNCK_INV1[9]	SNCK inverted output delay amount setting	
			8: SNCK_INV1[8]		
			7: SNCK_INV1[7]		
			6: SNCK_INV1[6]		
			5: SNCK_INV1[5]		
			4: SNCK_INV1[4]		
			3: SNCK_INV1[3]		
			2: SNCK_INV1[2]		
			1: SNCK_INV1[1]		
			0:		

Sets the inverted output delay amount for the corresponding clock pulse signal. Output can be delayed for the state set in the ADJ1_STATE[5:0] register by the time shown below by setting.

ADJ*_STATE[5:0]: Selects the delay output state.
- 00: No selects state.
- 01: Selects state 0.
- 02: Selects state 1.
- 04: Selects state 2.
- 08: Selects state 3.
- 10: Selects state 4.
- 20: Selects state 5.

*****_INV[9:1]: Delay time
- 00: No inversion
- 01: Inverts 1/10T delay output signal
- 02: Inverts 2/10T delay output signal
- 04: Inverts 3/10T delay output signal
- 08: Inverts 4/10T delay output signal
- 10: Inverts 5/10T delay output signal
- 20: Inverts 6/10T delay output signal
- 40: Inverts 7/10T delay output signal
- 80: Inverts 8/10T delay output signal
- 100: Inverts 9/10T delay output signal

Bit15 to 10 ADJ1_STATE[5:0]
Sets the state number for setting delay of SNCK_CLKADJ1 and SNCK_INV1 of the SNCK signal.

Bit9 to 0 SNCK_INV1[9:1]
Sets the inverted output delay amount of the SNCK signal.

Bit0 Reserved

7.4.13 0x4D Clock Pulse Inverted Output Delay Setting Register 2 (SNCK_INV2)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x4D	SNCK_INV2	R/W	15: ADJ2_STATE[5]	SNCK delay output state selection	0x0000
			14: ADJ2_STATE[4]		
			13: ADJ2_STATE[3]		
			12: ADJ2_STATE[2]		
			11: ADJ2_STATE[1]		
			10: ADJ2_STATE[0]		
			9: SNCK_INV2[9]	SNCK inverted output delay amount setting	
			8: SNCK_INV2[8]		
			7: SNCK_INV2[7]		
			6: SNCK_INV2[6]		
			5: SNCK_INV2[5]		
			4: SNCK_INV2[4]		
			3: SNCK_INV2[3]		
			2: SNCK_INV2[2]		
			1: SNCK_INV2[1]		
			0:		

Sets the inverted output delay amount for the corresponding clock pulse signal. Output can be delayed for the state set in the ADJ2_STATE[5:0] register by the time shown below by setting.

ADJ*_STATE[5:0]: Selects the delay output state.
- 00: No selects state.
- 01: Selects state 0.
- 02: Selects state 1.
- 04: Selects state 2.
- 08: Selects state 3.
- 10: Selects state 4.
- 20: Selects state 5.

*****_INV[9:1]: Delay time
- 00: No inversion
- 01: Inverts 1/10T delay output signal
- 02: Inverts 2/10T delay output signal
- 04: Inverts 3/10T delay output signal
- 08: Inverts 4/10T delay output signal
- 10: Inverts 5/10T delay output signal
- 20: Inverts 6/10T delay output signal
- 40: Inverts 7/10T delay output signal
- 80: Inverts 8/10T delay output signal
- 100: Inverts 9/10T delay output signal

Bit15 to 10 ADJ2_STATE[5:0]
Sets the state number for setting delay of SNCK_CLKADJ2 and SNCK_INV2 of the SNCK signal.

Bit9 to 0 SNCK_INV2[9:1]
Sets the inverted output delay amount of the SNCK signal.

Bit0 Reserved

7.4.14 0x4E Clock Pulse Inverted Output Delay Setting Register 3 (SNCK_INV3)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x4E	SNCK_INV3	R/W	15: ADJ3_STATE[5]	SNCK delay output state selection	0x0000
			14: ADJ3_STATE[4]		
			13: ADJ3_STATE[3]		
			12: ADJ3_STATE[2]		
			11: ADJ3_STATE[1]		
			10: ADJ3_STATE[0]		
			9: SNCK_INV3[9]	SNCK inverted output delay amount setting	
			8: SNCK_INV3[8]		
			7: SNCK_INV3[7]		
			6: SNCK_INV3[6]		
			5: SNCK_INV3[5]		
			4: SNCK_INV3[4]		
			3: SNCK_INV3[3]		
			2: SNCK_INV3[2]		
			1: SNCK_INV3[1]		
			0:		

Sets the inverted output delay amount for the corresponding clock pulse signal. Output can be delayed for the state set in the ADJ3_STATE[5:0] register by the time shown below by setting.

ADJ*_STATE[5:0]: Selects the delay output state.
- 00: No selects state.
- 01: Selects state 0.
- 02: Selects state 1.
- 04: Selects state 2.
- 08: Selects state 3.
- 10: Selects state 4.
- 20: Selects state 5.

*****_INV[9:1]: Delay time
- 00: No inversion
- 01: Inverts 1/10T delay output signal
- 02: Inverts 2/10T delay output signal
- 04: Inverts 3/10T delay output signal
- 08: Inverts 4/10T delay output signal
- 10: Inverts 5/10T delay output signal
- 20: Inverts 6/10T delay output signal
- 40: Inverts 7/10T delay output signal
- 80: Inverts 8/10T delay output signal
- 100: Inverts 9/10T delay output signal

Bit15 to 10 ADJ3_STATE[5:0]
Sets the state number for setting delay of SNCK_CLKADJ3 and SNCK_INV3 of the SNCK signal.

Bit9 to 0 SNCK_INV3[9:1]
Sets the inverted output delay amount of the SNCK signal.

Bit0 Reserved

7.4.15 0x50 Timing Generator Function Control Register (TGCTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x50	TGCTL		15:			0x0000
			14:			
			13:			
			12:			
			11:			
			10:			
		R/W	9: AFEDISOE	0: ODD/EVEN OUT	1: EVEN OUT	
			8: AFECKOUT	0: Disable	1: Enable	
			7: ADCKEN	0: Disable	1: Enable	
			6:			
			5:			
			4:			
			3:			
			2:			
			1:			
		R/W	0: TGSTART	0: IDLE	1: TGSTART	

Bit15 to 10 Reserved

Bit9 AFEDISOE
Setting "1" for this bit outputs the ADCK/CK1/CK2 signal only in EVEN cycles.

Bit8 AFECKOUT
Setting "1" for this bit outputs the ADCK/CK1/CK2 signal as long as the ADCKEN signal is enabled, regardless of the effective timing.

Bit7 ADCKEN
Setting "1" for this bit internally generates the ADCK signal.

Bit6 to 1 Reserved

Bit0 TGSTART
Setting "1" for this bit changes to the image capture mode.

Restriction
This register cannot be accessed to read when the PLL is stopped.

7.4.16 0x51 Timing Generator Function Setting Register (TGMD)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x51	TGMD	R/W	15: TGCKWIDTH[2]	TGCK pulse width adjustment		0x0000
			14: TGCKWIDTH[1]			
			13: TGCKWIDTH[0]			
			12: TGCKINV	0: Normal	1: Inverted	
			11:			
			10:			
		R/W	9: MUXSLINE	0: Internal generation at rising timing	1: External input at rising timing	
			8: INSLINE	0: External input by generation trigger	1: Internal generation by generation trigger	
			7:			
		R/W	6: INTGCK	0: External input	1: Internal generation	
			5:			
			4:			
			3:			
		R/W	2: TGCK_ADJ[2]	TGCK clear timing adjustment		
			1: TGCK_ADJ[1]			
			0: TGCK_ADJ[0]			

Bit15 to 13 TGCK_WIDTH[2:0]
Adjusts the pulse width of the TGCK signal when outputting the TGCK signal.
Setting "000" adjusts the pulse width for 1 state, and setting "101" adjusts the pulse width for 5 states.

Bit12 TGCKINV
If set to "1", the logic of TGCK signal is reversed during external TGCK signal input.

Bit11 to 10 Reserved

Bit9 MUXSLINE
Select the event at the rising timing of the SLINE signal. Setting this bit to "0" will result in the rising event of the SLINE signal being set depending on the values of the internal event pattern setting registers (No.0x00 to 0x3F). Setting this bit to "1" will result in an external input signal being used as a rising event. A falling event is determined depending on the set values of the internal event pattern setting registers (No.0x00 to 0x3F).

Bit8 INSLINE
Select the event of the SLINE signal. Setting this bit to "1" will result in the SLINE signal operating as an event of the external input. Setting this bit to "0" will result in operation being performed depending on the internal event pattern setting registers (No.0x00 to 0x3F).

Bit7 Reserved

Bit6 INTGCK
Setting "1" for this bit internally generates the TGCK signal.

Bit5 to 3 Reserved

Bit2 to 0 TGCK_ADJ
Adjusts the timing of the clear generation by the TGCK signal.
Starting from "000" as a reference, each increment delays one state.

Restriction
This register cannot be accessed to read or write when the PLL is stopped.

7.4.17 0x52 Internal State Control Register (STCTL)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x52	STCTL		15:		0x0000
			14:		
			13:		
			12:		
			11:		
			10:		
			9:		
		R/W	8: STNUM	Drive pattern resolution setting	
			7: SYNCMD[1]	Synchronization mode setting	
			6: SYNCMD[0]		
			5:		
			4:		
		R/W	3: STADJ[3]	Internal state delay setting	
			2: STADJ[2]		
			1: STADJ[1]		
			0: STADJ[0]		

Bit15 to 9 Reserved

Bit8 STNUM
Sets the clock pattern resolution (number of internal states) and the division count of internal reference clocks (clk) in each ADCKREF1 cycle.
STNUM: Dividing count
0: 3 dividings
1: 6 dividings

Bit7 to 6 SYNCMD[1:0]
Sets the synchronization mode between CLK input signals and internal state.
SYNCMD[1:0]: Synchronization mode
00: Continuous synchronization
01: (Disable)
10: Synchronized only when a rise of TGCK signal is detected.
11: (Synchronization disabled)

Bit5 to 4 Reserved

Bit3 to 0 STADJ[3:0]
Sets a phase difference between the internal state and CLK input signals when the internal state and CLK input signals are synchronized.

Restriction 1
STADJ[3:0] can be set within the following range, depending on the drive pattern resolution setting.
During 6 dividings: 0x0 to 0x5, During 3 dividings: 0x0 to 0x2

Restriction 2
This register cannot be accessed to read or write when the PLL is stopped.

7.4.18 0x53 Pattern Setting Control Register (PATEN)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x53	PATEN		15:			0x0000
			14:			
			13:			
			12:			
			11:			
			10:			
			9:			
			8:			
			7:			
			6:			
			5:			
			4:			
			3:			
		R/W	2: EVENTPAT1EN	0: Disable	1: Enable	
			1: EVENTPAT0EN	0: Disable	1: Enable	
			0: SNCKPATEN	0: Disable	1: Enable	

Bit15 to 3 Reserved

Bit2 EVENTPAT1EN
Set this bit to “1” to access to PAT40 to PAT7F registers which is the event pattern setting for the 1st bank. Also, reset this bit to “0” after the access to register has completed.

Bit1 EVENTPAT0EN
Set this bit to “1” to access to PAT00 to PAT3F registers which is the event pattern setting for the 0th bank. Also, reset this bit to “0” after the access to register has completed.

Bit0 SNCKPATEN
Set this bit to “1” to set the line sensor drive clock pulse pattern. Also, reset this bit to “0” after the access to register has completed.

Restriction 1
Setting the SNCKPATEN, EVENTPAT0EN and EVENTPAT1EN bits to “1” simultaneously is not allowed.

Restriction 2
Be sure to set TGSTART bit to “0” in the TGCTL register (No.0x50) before accessing to this register.

7.4.19 0x54 Line Sensor Drive Clock Pulse Polarity Setting Register (SNCKINV)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x54	SNCKINV		15:			0x0000
			14:			
			13:			
		R/W	12: SNCK6INV	0: Normal	1: Invert	
			11: SNCK5INV	0: Normal	1: Invert	
			10: SNCK4INV	0: Normal	1: Invert	
			9: SNCK3INV	0: Normal	1: Invert	
			8: SNCK2INV	0: Normal	1: Invert	
			7:			
			6:			
			5:			
		R/W	4: SNCK1EINV	0: Normal	1: Invert	
			3: SNCK1DINV	0: Normal	1: Invert	
			2: SNCK1CINV	0: Normal	1: Invert	
			1: SNCK1BINV	0: Normal	1: Invert	
			0: SNCK1AINV	0: Normal	1: Invert	

Bit15 to 13 Reserved

Bit12 to 8 SNCK6INV to SNCK2INV
Setting this bit to "1" inverts the output polarity of the SNCK2 to SNCK6 signals.

Bit7 to 5 Reserved

Bit4 to 0 SNCK1EINV to SNCK1AINV
Setting this bit to "1" inverts the output polarity of the SNCK1A to SNCK1E signals.

7.4.20 0x55 Line Sensor Drive Clock Pulse Pattern Setting Register 1 (SNCK1CTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x55	SNCK1CTL		15:			0x0000
			14:			
			13:			
		R/W	12: SNCK1ELV2	0: Low	1: High	
			11: SNCK1DLV2	0: Low	1: High	
			10: SNCK1CLV2	0: Low	1: High	
			9: SNCK1BLV2	0: Low	1: High	
			8: SNCK1ALV2	0: Low	1: High	
			7:			
			6:			
			5:			
		R/W	4: SNCK1ELV1	0: Low	1: High	
			3: SNCK1DLV1	0: Low	1: High	
			2: SNCK1CLV1	0: Low	1: High	
			1: SNCK1BLV1	0: Low	1: High	
			0: SNCK1ALV1	0: Low	1: High	

Bit15 to 13 Reserved

Bit12 to 8 SNCK1ELV2 to SNCK1ALV2
Sets the output level of the fixed value 2 of the SNCK1E to 1A signals.

Bit7 to 5 Reserved

Bit4 to 0 SNCK1ELV1 to SNCK1ALV1
Sets the output level of the fixed value 1 of the SNCK1E to 1A signals.

7.4.21 0x56 Line Sensor Drive Clock Pulse Pattern Setting Register 2 (SNCK2CTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x56	SNCK2CTL		15:			0x0000
			14:			
			13:			
		R/W	12: SNCK6LV2	0: Low	1: High	
			11: SNCK5LV2	0: Low	1: High	
			10: SNCK4LV2	0: Low	1: High	
			9: SNCK3LV2	0: Low	1: High	
			8: SNCK2LV2	0: Low	1: High	
			7:			
			6:			
			5:			
		R/W	4: SNCK6LV1	0: Low	1: High	
			3: SNCK5LV1	0: Low	1: High	
			2: SNCK4LV1	0: Low	1: High	
			1: SNCK3LV1	0: Low	1: High	
			0: SNCK2LV1	0: Low	1: High	

Bit15 to 13 Reserved

Bit12 to 8 SNCK6LV2 to SNCK2LV2
Sets the output level of the fixed value 2 of the SNCK2 to 6 signals.

Bit7 to 5 Reserved

Bit4 to 0 SNCK6LV1 to SNCK2LV1
Sets the output level of the fixed value 1 of the SNCK2 to 6 signals.

7.4.22 0x57 Line Sensor Drive Clock Pulse Output Setting Register (SNCKxSHCTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x57	SNCKxSHCTL		15:			0x0000
			14:			
			13:			
			12:			
		R/W	11: SNCK5xSH9	0: SNCK5	1: SNCK5 OR SH9	
			10: SNCK4xSH8	0: SNCK4	1: SNCK4 OR SH8	
			9: SNCK3xSH7	0: SNCK3	1: SNCK3 OR SH7	
			8: SNCK2xSH6	0: SNCK2	1: SNCK2 OR SH6	
			7:			
			6:			
			5:			
			4:			
		R/W	3: SNCK1DxSH9	0: SNCK1D	1: SNCK1D OR SH9	
			2: SNCK1CxSH8	0: SNCK1C	1: SNCK1C OR SH8	
			1: SNCK1BxSH7	0: SNCK1B	1: SNCK1B OR SH7	
			0: SNCK1AxSH6	0: SNCK1A	1: SNCK1A OR SH6	

Bit15 to 12 Reserved

Bit11 to 8 SNCK5xSH9 to SNCK2xSH6
Sets the output method of the SNCK5 to 2 signals.
If "0" is set, the set value for the SNCK5 to 2 signals is output.
If "1" is set, the SNCK5 to 2 signals and the SH9 to 6 signals are logically ORed.

Bit7 to 4 Reserved

Bit3 to 0 SNCK1DxSH9 to SNCK1AxSH6
Sets the output method of the SNCK1D to 1A signals.
If "0" is set, the set value for the SNCK1D to 1A signals is output.
If "1" is set, the SNCK9 to 6 signals and the SNCK1D to 1A signals are logically ORed.

7.4.23 0x58 Polarity Control Register (POLCTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x58	POLCTL	R/W	15: CLMPPOL	0: Normal	1: Invert	0x0000
			14: GPIO5POL	0: Normal	1: Invert	
			13: GPIO4POL	0: Normal	1: Invert	
			12: GPIO3POL	0: Normal	1: Invert	
			11:			
			10:			
			9:			
		R/W	8: SH9POL	0: Normal	1: Invert	
			7: SH8POL	0: Normal	1: Invert	
			6: SH7POL	0: Normal	1: Invert	
			5: SH6POL	0: Normal	1: Invert	
			4: SH5POL	0: Normal	1: Invert	
			3: SH4POL	0: Normal	1: Invert	
			2: SH3POL	0: Normal	1: Invert	
			1: SH2POL	0: Normal	1: Invert	
			0: SH1POL	0: Normal	1: Invert	

Bit15 CLMPPOL
Setting this bit to "1" will invert the output polarity of the CLMP signal.

Bit14 GPIO5POL
Setting this bit to "1" will invert the output polarity of the GPIO5 (WHPIX) signal.

Bit13 GPIO4POL
Setting this bit to "1" will invert the output polarity of the GPIO4 (SLINE) signal.

Bit12 GPIO3POL
Setting this bit to "1" will invert the output polarity of the GPIO3 (OBPIX) signal.
If the INSLINE bit is set to "0", setting this bit to "1" will invert the SLINE signal.

Bit11 to 9 Reserved

Bit8 SH9POL
Setting this bit to "1" will invert the output polarity of the SH9 signal.

Bit7 SH8POL
Setting this bit to "1" will invert the output polarity of the SH8 signal.

Bit6 SH7POL
Setting this bit to "1" will invert the output polarity of the SH7 signal.

Bit5 SH6POL
Setting this bit to "1" will invert the output polarity of the SH6 signal.

Bit4 SH5POL
Setting this bit to "1" will invert the output polarity of the SH5 signal.

Bit3 SH4POL
Setting this bit to "1" will invert the output polarity of the SH4 signal.

Bit2 SH3POL
Setting this bit to "1" will invert the output polarity of the SH3 signal.

Bit1 SH2POL
Setting this bit to "1" will invert the output polarity of the SH2 signal.

Bit0 SH1POL
Setting this bit to "1" will invert the output polarity of the SH1 signal.

7.4.24 0x59 General-purpose Port Control Register (GPIOEN1)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x59	GPIOEN1		15:			0x1F1F
			14:			
			13:			
		R/W	12: PSNCK6EN	0: SNCK6	1: General purpose port	
			11: PSNCK5EN	0: SNCK5	1: General purpose port	
			10: PSNCK4EN	0: SNCK4	1: General purpose port	
			9: PSNCK3EN	0: SNCK3	1: General purpose port	
			8: PSNCK2EN	0: SNCK2	1: General purpose port	
			7:			
			6:			
			5:			
		R/W	4: PSNCK1EEN	0: SNCK1E	1: General purpose port	
			3: PSNCK1DEN	0: SNCK1D	1: General purpose port	
			2: PSNCK1CEN	0: SNCK1C	1: General purpose port	
			1: PSNCK1BEN	0: SNCK1B	1: General purpose port	
			0: PSNCK1AEN	0: SNCK1A	1: General purpose port	

This register controls the pin that doubles as a general-purpose port. Setting "0" enables the pin that corresponds to the register to output the functional signal of the appropriate pin. Setting "1" enables the general-purpose port function of the corresponding pin.

7.4.25 0x5A General-purpose Port Control Register (GPIOEN2)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x5A	GPIOEN2	R/W	15: PCLMPEN	0: CLMP	1: General purpose port	0xF0FF
			14: PADCKEN	0: ADCK	1: General purpose port	
			13: PCK2EN	0: CK2	1: General purpose port	
			12: PCK1EN	0: CK1	1: General purpose port	
			11:			
			10:			
			9:			
			8:			
		R/W	7: PGPIO5EN	0: GPIO5	1: General purpose port	
			6: PGPIO4EN	0: GPIO4	1: General purpose port	
			5: PGPIO3EN	0: GPIO3	1: General purpose port	
			4: PGPIO2EN	0: GPIO2	1: General purpose port	
			3: PGPIO1EN	0: GPIO1	1: General purpose port	
			2: PSH3EN	0: SH3	1: General purpose port	
			1: PSH2EN	0: SH2	1: General purpose port	
			0: PSH1EN	0: SH1	1: General purpose port	

This register controls the pin that doubles as a general-purpose port. Setting "0" enables the pin that corresponds to the register to output the functional signal of the appropriate pin. Setting "1" enables the general-purpose port function of the corresponding pin.

7.4.26 0x5B General-purpose Port I/O Switching Register 1 (GPIODIR1)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x5B	GPIODIR1		15:		0x0000
			14:		
			13:		
			12:		
			11:		
			10:		
		R/W	9: PSNCK1EDIR[1]	SNCK1E pin I/O switching select	
			8: PSNCK1EDIR[0]		
			7: PSNCK1DDIR[1]	SNCK1D pin I/O switching select	
			6: PSNCK1DDIR[0]		
			5: PSNCK1CDIR[1]	SNCK1C pin I/O switching select	
			4: PSNCK1CDIR[0]		
			3: PSNCK1BDIR[1]	SNCK1B pin I/O switching select	
			2: PSNCK1BDIR[0]		
			1: PSNCK1ADIR[1]	SNCK1A pin I/O switching select	
			0: PSNCK1ADIR[0]		

This register sets the I/O switching of the pins shared with general-purpose ports.
If the register is set to "00", the pins corresponding to the register turn to input ports.
If the register is set to "01", the pins turn to the output ports that can drive 12 mA output current.
In addition, if the register is set to "10", the pins turn to the output ports that can drive 24 mA output current.

Restriction 1
If you want to output functional signals, the register must be set to "01" or "10" to turn the pins to the output state.

Restriction 2
When you set the relevant pin to output, you must not set this register to "11". Not that, if this register is set to "11", the relevant pin may be destroyed.

7.4.27 0x5C General-purpose Port I/O Switching Register 2 (GPIODIR2)

No.	Register Name	R/W	Bit Symbol	Description	Reset
0x5C	GPIODIR2		15:		0x0000
			14:		
			13:		
			12:		
			11:		
			10:		
		R/W	9: PSNCK6DIR[1]	SNCK6 pin I/O switching select	
			8: PSNCK6DIR[0]		
			7: PSNCK5DIR[1]	SNCK5 pin I/O switching select	
			6: PSNCK5DIR[0]		
			5: PSNCK4DIR[1]	SNCK4 pin I/O switching select	
			4: PSNCK4DIR[0]		
			3: PSNCK3DIR[1]	SNCK3 pin I/O switching select	
			2: PSNCK3DIR[0]		
			1: PSNCK2DIR[1]	SNCK2 pin I/O switching select	
			0: PSNCK2DIR[0]		

This register sets the I/O switching of the pins shared with general-purpose ports.
If the register is set to "00", the pins corresponding to the register turn to input ports.
If the register is set to "01", the pins turn to the output ports that can drive 12 mA output current.

In addition, if the register is set to “10”, the pins turn to the output ports that can drive 24 mA output current.

Restriction 1
If you want to output functional signals, the register must be set to “01” or “10” to turn the pins to the output state.

Restriction 2
When you set the relevant pin to output, you must not set this register to “11”. Not that, if this register is set to “11”, the relevant pin may be destroyed.

7.4.28 0x5D General-purpose Port I/O Switching Register 3 (GPIODIR3)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x5D	GPIOEN3	R/W	15: PCLMPDIR	0: Input port	1: Output port	0x0000
			14: PADCKDIR	0: Input port	1: Output port	
			13: PCK2DIR	0: Input port	1: Output port	
			12: PCK1DIR	0: Input port	1: Output port	
			11:			
			10:			
			9:			
			8:			
			7:			
			6:			
		R/W	5: PGPIO3DIR	0: Input port	1: Output port	
			4: PGPIO2DIR	0: Input port	1: Output port	
			3: PGPIO1DIR	0: Input port	1: Output port	
			2: PSH3DIR	0: Input port	1: Output port	
			1: PSH2DIR	0: Input port	1: Output port	
			0: PSH1DIR	0: Input port	1: Output port	

This register sets the I/O switching of the pins shared with general-purpose ports. If the register is set to “0”, the pin corresponding to the register turns to an input port. If it is set to “1”, the pin turns to an output port.

Restriction
To output a functional signal, set to “1” and bring to the output state.

7.4.29 0x5E General-purpose Port Register 1 (GPIOST1)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x5E	GPIOST1		15:			0x0000
			14:			
			13:			
		R/W	12: PSNCK6	0: Low	1: High	
			11: PSNCK5	0: Low	1: High	
			10: PSNCK4	0: Low	1: High	
			9: PSNCK3	0: Low	1: High	
			8: PSNCK2	0: Low	1: High	
			7:			
			6:			
			5:			
		R/W	4: PSNCK1E	0: Low	1: High	
			3: PSNCK1D	0: Low	1: High	
			2: PSNCK1C	0: Low	1: High	
			1: PSNCK1B	0: Low	1: High	
			0: PSNCK1A	0: Low	1: High	

This register indicates the state of the general-purpose port.
If you write this register, the corresponding signal outputs the value set for the register when output is set for the general-purpose port. If you read this register, you can read the state of the corresponding pin regardless of the setting of the general-purpose port.

7.4.30 0x5F General-purpose Port Register 2 (GPIOST2)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x5F	GPIOST2	R/W	15: PCLMP	0: Low	1: High	0x0000
			14: PADCK	0: Low	1: High	
			13: PCK2	0: Low	1: High	
			12: PCK1	0: Low	1: High	
			11:			
			10:			
			9:			
			8:			
		R/W	7: PGPIO5	0: Low	1: High	
			6: PGPIO4	0: Low	1: High	
			5: PGPIO3	0: Low	1: High	
			4: PGPIO2	0: Low	1: High	
			3: PGPIO1	0: Low	1: High	
			2: PSH3	0: Low	1: High	
			1: PSH2	0: Low	1: High	
			0: PSH1	0: Low	1: High	

This register indicates the state of the general-purpose port.
If you write this register, the corresponding signal outputs the value set for the register when output is set for the general-purpose port. If you read this register, you can read the state of the corresponding pin regardless of the setting of the general-purpose port. However, the setting value is read for the PGPIO4 and PGPIO5 bits.

7.4.31 0x70 Analog Module Reset Register (ANA_RESET)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x70	ANA_RESET		15:			0x0000
			14:			
			13:			
		R/W	12: xPD_RSDS	0: Power down	1: Normal	
			11:			
			10:			
			9:			
		R/W	8: xPD_PLL	0: Power down	1: Normal	
			7:			
			6:			
			5:			
			4:			
			3:			
			2:			
			1:			
			0:			

Bit15 to 13 Reserved

Bit12 xPD_RSDS
This is a power-down register to the built-in RSDS (LVDS).

Bit11 to 9 Reserved

Bit8 xPD_PLL
This is a power-down register to the built-in PLL.

Bit7 to 0 Reserved

7.4.32 0x7F PLL・image Output Control Register (PLL_IMGSIG_CTL)

No.	Register Name	R/W	Bit Symbol	Description		Reset
0x7F	PLL_IMGSIG_CTL	R/W	15: VCOSEL	0: ≤100MHz	1: ≥100MHz	0x2000
			14:			
		R/W	13: RSEL[1]	PLL built-in filter selection		
			12: RSEL[0]			
			11: CLKSEL[1]	Input clock selection		
			10: CLKSEL[0]			
			9:			
			8:			
			7:			
			6:			
			5:			
			4:			
			3:			
			2:			
			1:			
			0:			

Bit15 VCOSEL

Set this bit by following below in accordance with frequency of the internal reference clock (CLK signal) output from the built-in PLL.

VCOSEL: CLK signal frequency

0: 100 MHz or less

1: 100 MHz or more

Bit14 Reserved

Bit13 to 12 RSEL[1:0]

Select the constant of the filter circuit of the built-in PLL. Normally set to “10”.

Bit11 to 10 CLKSEL[1:0]

Sets the input clock, as follows.

CLKSEL[1:0]: Selects the CLK input.

00: Clock input

01: RSDS (LVDS) differential input

10: Oscillation circuit input

Bit9 to 0 Reserved

Restriction

When setting CLKSEL, this register must not be set to “11”.

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	HV_{DD} ※	-0.3 to +7.0	V
	LV_{DD} ※	-0.3 to +4.0	V
	RXV_{DD} ※	-0.3 to +4.0	V
Input voltage	HV_I	-0.3 to HV_{DD}+0.5	V
	LV_I	-0.3 to LV_{DD}+0.5 (-0.3V to +7.0V at 5V tolerant input *2)	V
	RXV_I	-0.3 to RXV_{DD}+0.5	V
Output voltage	HV_O	-0.3 to HV_{DD}+0.5	V
	LV_O	-0.3 to LV_{DD}+0.5	V
Output current/pin	I_{OUT}	±30	mA
Storage temperature	T_{stg}	-65 to 150	°C

V_{SS}=0V, RXV_{SS}=0V

※ $HV_{DD} \geq LV_{DD}$, RXV_{DD}、 $LV_{DD} = RXV_{DD}$

8.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	HV_{DD}	4.500	5.000	5.500	V
	LV_{DD}	3.135	3.300	3.465	V
	RXV_{DD}	3.135	3.300	3.465	V
Input voltage	HV_I	V_{SS}	—	HV_{DD}	V
	LV_I	V_{SS}	—	LV_{DD}	V
	RXV_I	RXV_{SS}	—	RXV_{DD}	V
Ambient temperature	Ta	0	25	70	°C
Input rise (normal input)	t_{ri} ※	—	—	50	ns
Input fall (normal output)	t_{fa} ※	—	—	50	ns
Input rise (Schmidt input)	t_{ri} ※	—	—	5	ms
Input fall (Schmidt input)	t_{fa} ※	—	—	5	ms

V_{SS}=0V, RXV_{SS}=0V

※ Time of change of HV_{DD} or LV_{DD} by 10 to 90 %

8.3 Power Sequence

Follow the power sequence shown in the following to turn on the power. Note that, if you do not follow the sequence, the IC may be destroyed.

8.3.1 Upon power-on

LV_{DD} ON → RXV_{DD} ON
HV_{DD} ON
All the power must be turned on within one second after LV_{DD} has been turned on.
* Because there is no phase relation between RXV_{DD} and HV_{DD}, whichever can be turned on first.

8.3.2 Upon power-off

RXV_{DD} OFF → LV_{DD} OFF
HV_{DD} OFF
All the power must be shut down within one second after RXV_{DD} or HV_{DD} has been shut down.
* Because there is no phase relation between RXV_{DD} and HV_{DD}, whichever can be shut down first.

8.3.3 DC Characteristics

(1) Input/output characteristics in DC state

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static current	I_{HDDS}	HV_{DD}=5V±10%	—	—	10	μA
	I_{LDDS}	LV_{DD}=3.3V±5%	—	—	10	μA
	RXI_{DDS}	RXV_{DD}=3.3V±5%	—	—	10	μA
Consumption current [10 MHz]	I_{HDD} ※	HV_{DD}=5V±10%	—	50	—	mA
	I_{LDD}	LV_{DD}=3.3V±5%	—	220	—	mA
	RXI_{DD}	AV_{DD}=3.3V±5%	—	6	—	mA
Input leak current [HV_{DD}]	I_{HLI}	HV_{DD}=5V, V_{HIH}=HV_{DD}, V_{HIL}=V_{SS}	-5	—	5	μA
Input leak current [LV_{DD}]	I_{LLI}	LV_{DD}=3.3V, V_{LIH}=LV_{DD},V_{LIL}=V_{SS}	-5	—	5	μA
Off-state leak current [HV_{DD}]	I_{HOZ}	—	-5	—	5	μA
Off-state leak current [LV_{DD}]	I_{LOZ}	—	-5	—	5	μA

※ At no-load to external pins

(2) Input characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage [HV_{DD}]	V_{HIH}	TTL, HV_{DD}=Max	2.0	—	—	V
Low-level input voltage [HV_{DD}]	V_{HIL}	TTL, HV_{DD}=Min	—	—	0.8	V
Positive trigger voltage [HV_{DD}]	V_{HT+}	TTL Schmidt	1.2	—	2.4	V
Negative trigger voltage [HV_{DD}]	V_{HT-}	TTL Schmidt	0.6	—	1.8	V
Hysteresis voltage [HV_{DD}]	V_{HH}	TTL Schmidt	0.1	—	—	V
High-level input voltage [LV_{DD}]	V_{LIH}	LVTTL, LV_{DD}=Max	2.0	—	—	V
Low-level input voltage [LV_{DD}]	V_{LIL}	LVTTL, LV_{DD}=Min	—	—	0.8	V
Positive trigger voltage [LV_{DD}]	V_{LT+}	LVTTL Schmidt	1.1	—	2.4	V
Negative trigger voltage [LV_{DD}]	V_{LT-}	LVTTL Schmidt	0.6	—	1.8	V
Hysteresis voltage [LV_{DD}]	V_{LH}	LVTTL Schmidt	0.1	—	—	V

(3) Input pull-down characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Pull-down resistance value [HV_{DD}]	R_{HPD}	HV_I=HV_{DD}	30	60	120	KΩ
Pull-down resistance value [LV_{DD}]	R_{LPD}	LV_I=LV_{DD}	20	50	100	KΩ

(4) Input pull-up characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Pull-up resistance value [HV_{DD}]	R_{HPU}	HV_I=0V	30	60	120	KΩ
Pull-up resistance value [LV_{DD}]	R_{LPU}	LV_I=0V	20	50	100	KΩ

(5) Output characteristics

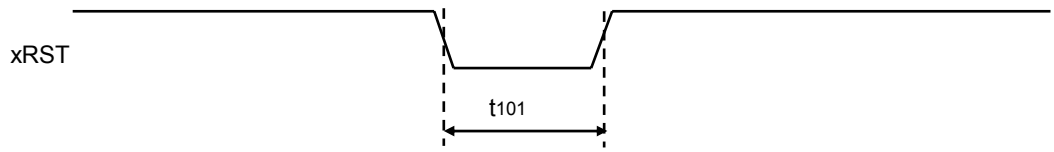
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level output voltage [HV_{DD}]	V_{HOH}	HV_{DD}=Min, I_{HOH}=-8mA	HV_{DD}-0.4	—	—	V
Low-level output voltage [HV_{DD}]	V_{HOL}	HV_{DD}=Min, I_{HOL}=8mA	—	—	0.4	V
High-level output voltage [LV_{DD}]	V_{LOH}	LV_{DD}=Min, I_{LOH}=-6mA	LV_{DD}-0.4	—	—	V
Low-level output voltage [LV_{DD}]	V_{LOL}	LV_{DD}=Min, I_{LOL}=6mA	—	—	0.4	V

(6) RSDS (LVDS) -RX characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Terminating resistor	R_{trm}	RXV_{DD}=3.3V	99	100	101	Ω
Differential input voltage	V_{id}	RXV_{DD}=3.3V	250	350	450	|mV|
Input common mode voltage	V_{os}	RXV_{DD}=3.3V	1.0	1.25	2.0	V

8.4 AC Characteristics

8.4.1 AC Characteristics

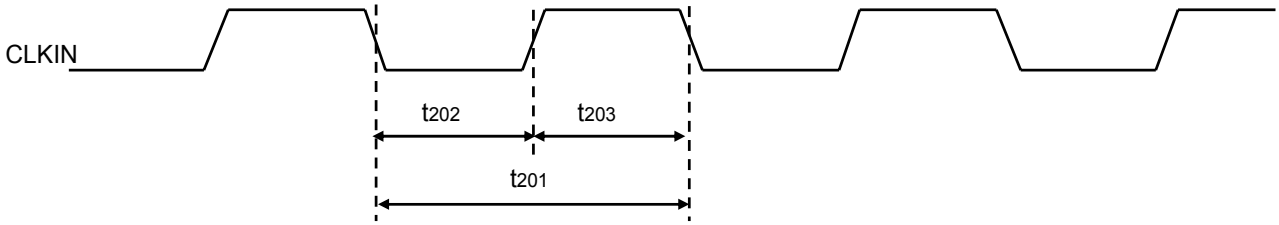


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{101}	xRST low-level pulse width	10	–	–	ms

* To avoid an operation error, the xRST signal entered must have a pulse width longer than the above minimum value.

8.4.2 Clock Timing

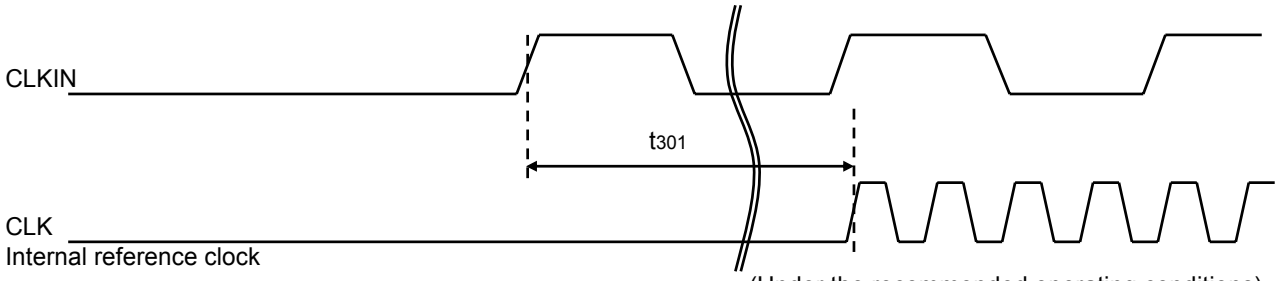


(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{201}	CLK cycle	-100ppm	1/(10M～25M)	+100ppm	s
t_{202}	CLK Low-level pulse width of CLK	(t_{201}/2)-10%	t_{201}/2	(t_{201}/2)+10%	ns
t_{203}	CLK High-level pulse width of CLK	(t_{201}/2)-10%	t_{201}/2	(t_{201}/2)+10%	ns

* $t_{201}$is a cycle of a clock input to the CLKIN pin.

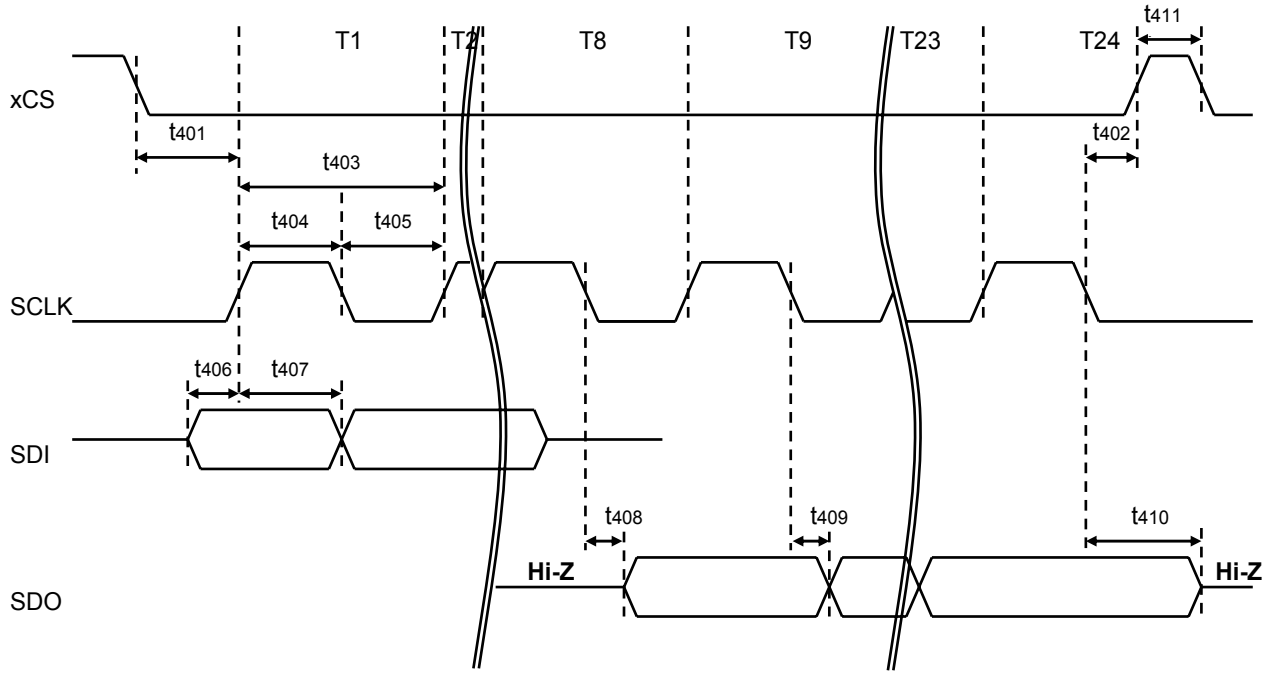
8.4.3 PLL Lock Timing



(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{301}	PLL lock time	10	–	–	ms

8.4.4 Serial Interface Timing

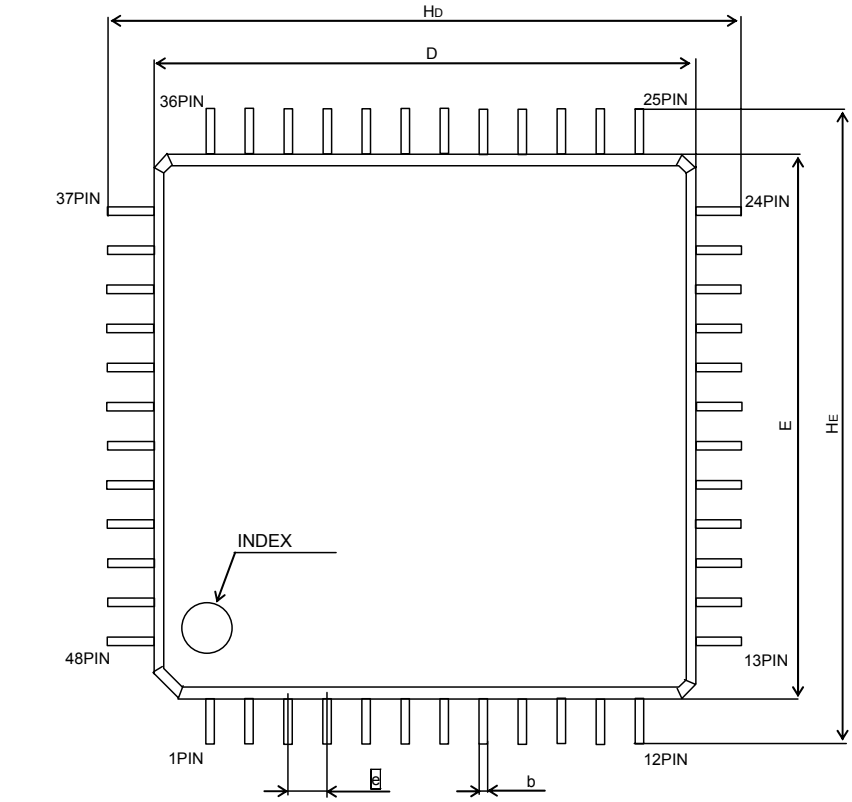


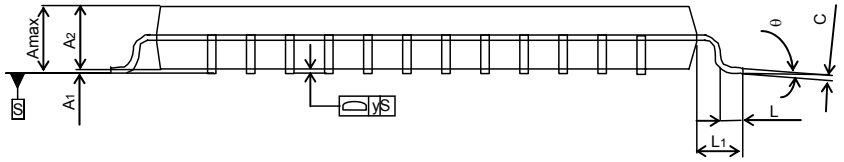
(Under the recommended operating conditions)

Symbol	Item	Min.	Typ.	Max.	Unit
t401	Serial interface access start setup time	100	–	–	ns
t402	Serial interface access end hold time	10	–	–	ns
t403	SCLK cycle	100	–	–	ns
t404	SCLK high-level pulse width	40	–	–	ns
t405	SCLK low-level pulse width	40	–	–	ns
t406	SDI setup time	20	–	–	ns
t407	SDI hold time	20	–	–	ns
t408	SDO read delay time	5	–	–	ns
t409	SDO switching delay time	–	–	30	ns
t410	SDO hold time	–	–	30	ns
t411	Serial interface access cycle wait time	100	–	–	ns

9. EXTERNAL DIMENSIONS

QFP12-48 package





Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	—	7	—
D	—	7	—
Amax	—	—	1.7
A1	—	0.1	—
A2	—	1.4	—
e	—	0.5	—
b	0.13	—	0.27
c	0.09	—	0.2
θ	0°	—	10°
L	0.3	—	0.7
L1	—	1	—
HE	—	9	—
HD	—	9	—
y	—	—	0.08

1＝1mm

Any information of this manual is subject to change without prior notice according to the continual improvement.

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