

CMOS 32-bit Application Specific Controller

- S1C33 32-bit RISC CPU Core with 1K-byte Instruction Cache and 1K-byte Data Cache (EPSON S1C33 PE) (Max. 90 MHz operation)
- 100K-byte RAM Including 2K-byte Cache and 2K-byte Battery Backup RAM
- Built-in PLL (frequency multiplication rate: $\times 1$ to $\times 16$)
- Local Bus Interface Designed Specifically for Graphics LSI 8/16-bit Data Bus
- Built-in 16 ch. DMA Controller (triggered by peripherals)
- SDRAM Controller with Burst Control
- Abundant Serial Interfaces
UART $\times 2$ ch., SIF (serial I/F with IrDA 1.0 support) $\times 2$ ch., EFSIO (serial I/F with FIFO and ISO7816/IrDA 1.0 support) $\times 2$ ch., SPI $\times 4$ ch., DCSIO (I²C bus master I/F emulation) $\times 4$ ch.
- 4 ch. of 16-bit PWM Control Timers with IGBT Control Features
- 4 ch. of 8-bit Programmable Timers
- Card Interface Connectable with NAND Flash

■ DESCRIPTIONS

The S1C33S03 is a 32-bit RISC I/O companion controller for amusement equipment that has an I/O controller for LEDs (lamps), and an independent bus interface for graphic LSIs that makes the high-performance graphics LSI reach its full potential. The graphic LSI bus is completely independent of the CPU, and allows high-speed DMA transfer between an internal I/O device, internal memory, or an external device connected to the CPU bus and the graphics LSI. The S1C33S03 incorporates a maximum 100K bytes of large capacity RAM and the S1C33 PE mini-cache controller to execute the program in the internal RAM in high-speed. The S1C33 PE mini-cache and the SDRAM controller that supports burst transfer improve the S1C33 PE CPU Core and it makes it possible to run the S1C33S03 at a maximum of 90 MHz operating frequency. Furthermore, the 2KB internal RAM can be operated using a power supply separate from the system power source, so RAM data can be bucked up even if the system is in power down status while only the real-time clock is running. The S1C33S03 incorporates eight channels of timers (8-bit timers and 16-bit timers) and the serial interfaces that have channels in abundance (SIO, SPI, and DSIO that emulates I²C bus master interface) and they are capable of being used for inter LSI communication and LED (lamp) control in the amusement equipment. The S1C33S03 also provides card interface signals to connect Compact Flash or PC cards, and NAND Flash memories. In the S1C33S03, the above functions are implemented by EPSON SoC (System on Chip) technology that adopts the 0.18 μ m Vth. mixed CMOS process.

■ FEATURES

- **Technology**
 - 0.18 μ m AL-4-layers Vth. mixed CMOS process technology
- **CPU**
 - Seiko Epson original 32-bit RISC processor S1C33 PE Core with AMBA bus that optimized for SoC
 - Maximum operating frequency: 90 MHz
 - Internal 2-stage pipeline
 - Instruction set: 125 instructions (16-bit fixed length)
 - Caches: 1K-byte instruction cache + 1K-byte data cache
 - Memory space
 - Up to 4G bytes accessible (32-bit address)
- **Internal Memories**
 - RAM
 - 16K-byte IRAM1 (Usable as a high-speed general-purpose RAM. 2K bytes are used as caches)
 - 64K-byte IRAM2 (Usable as a general-purpose RAM. Can be connected to the CPU bus or the local bus for graphics LSI.)
 - 16K-byte IRAM3 (Usable as a general-purpose RAM. Can be connected to the CPU bus or the local bus for graphics LSI.)
 - 2K-byte DSTRAM (Usable as a general-purpose RAM or a DMA descriptor table RAM)
 - 2K-byte BBRAM (Data can be maintained using a power source separated from the system power supply.)

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● Operating Clock

- Main clock
 - 90 MHz (max.)
 - On-chip oscillator (crystal or ceramic) or external clock input
 - PLL: Integral multiplication PLL circuit
- Sub clock
 - 32.768 kHz (typ.) for RTC and low speed (power save) operations
 - On-chip oscillator (crystal)

● Mini Cache Controller (miniCache)

- 1K-byte instruction cache and 1K-byte data cache with 4-way set associative frame architecture (4 frames/way, 4 lines/frame, 4 words/line)
- LRU replacement algorithm
- Automatic lock function in debug mode or interrupt handling with specified priority
- Write through function with 1-word buffer
- * The cache memory is allocated in IRAM1.

● Universal DMA Controller (UDMA)

- 2 channels of fast-DMA and 14 channels of table-DMA
- Supports dual address transfer by specifying source and destination addresses.
- Single transfer mode or continuous transfer mode is selectable.
- High performance burst transfer function interlocked with SDRAM controller
- 1-byte, 1-halfword, 1-word, 4-byte, 4-halfword, and 4-word burst transfer programmable
- Built-in DMA trigger system with a linkage function
- Software trigger or hardware triggers by various peripheral circuits are selectable.

● SRAM Controller (SRAMC)

- Up to 8 chip enable signals are available for connecting external devices.
- Flash ROM, SRAM, and ASSP (LCD driver) devices can be connected.
- 24-bit address bus and 8/16-bit selectable data bus
- Programmable bus access wait cycles (1 to 16 cycles)
- Supports little endian access.
- Memory mapped I/O
- On-chip peripheral I/O areas are reserved in the memory space (Area 6).
- Supports either A0 or BS (Bus Strobe) access type.
- Supports external wait requests using the #WAIT pin.

● SDRAM Controller (SDRAMC)

- 16-bit SDRAM interface that operates with up to 90 MHz
- Supports 16M-bit (2MB) to 512M-bit (64MB) SDRAMs.
- IQB (Instruction Queue Buffer) and DQB (Data Queue Buffer) are built in. (IQB is usable only when the mini cache controller is not used.)
- Optimized multi-master access request to reduce average read latency
- Programmable CAS latency (1, 2 and 3)
- Supports burst transfer.
- The sync clock is configurable to the same or double frequency as the CPU clock.
- Incorporates a 12-bit auto-refresh counter.
- Intelligent self-refresh function for low power operation

● Local Bus for External Graphics LSI

- An 8/16-bit data bus is provided to connect an external graphics LSI.
- Maximum 8MB or 16MB address space (Up to 24 address signals are available.)
- Supports external wait requests using the #LWAIT/#LREADY pin.
- Supports single address DMA.

● Clock Management Unit (CMU)

- Selects the system clock source (OSC3, PLL, or OSC1).
- Controls the OSC3 and OSC1 oscillator circuits on and off.
- Controls the clock divider (1/1 to 1/16) and frequency multiplication rate of the PLL (x1 to x16).
- Controls clocks according to the standby mode (SLEEP and HALT).
- Controls divide ratios of the core clock, peripheral clock, and external bus clock.

● Interrupt Controller (ITC)

- Controls 16 channels of interrupts reserved for the S1C33 PE Core.
- Supports up to 48 channels of interrupt sources (including some reserved channels)

● Card Interface (CARD)

- Generates SmartMedia (NAND Flash), Compact Flash and PC card interface signals.
- Supports NAND Flash booting function.

● Watchdog Timer (WDT)

- 30-bit watchdog timer that can generate an NMI (non-maskable interrupt)
- Programmable watchdog timer overflow cycle (NMI generating cycle) can be set.
- The watchdog timer overflow signal can be output to external devices.

● 16-bit Timers (T16)

- 4 channels of 16-bit timers/counters with PWM control function
- An digital DAC function can be implemented using the PWM output and an external RC filter.
- Incorporates 4 channels of output comparators that can be used to control IGBT.

● 8-bit Timers (T8)

- 4 channels of 8-bit programmable timers/counters
- * Up to 2 channels may be used as the baud rate generator for the serial interface (UART).

● Serial Interface (UART, SIF, EFSIO)

UART

- 2 channels of UART
- Supports IrDA 1.0 interface.
- 2-byte receive data buffer and 1-byte transmit data buffer are built in to support full-duplex communication.
- Transfer rate: 150 to 115200 bps, Data length: 7 or 8 bits, Parity mode: even, odd, or no parity, Stop bit: 1 or 2 bits
- Parity, framing, and overrun errors are detectable.

SIF (Serial Interface)

- 2 channels of clock sync/asynchronous serial interface
- 1-byte receive data buffer and 1-byte transmit data buffer are built into each channel.
- IrDA1.0 interface is built in.
- A baud-rate generator (12-bit programmable timer) is built in.

EFSIO (Extended Serial Interface with FIFO)

- 2 channels of clock sync/asynchronous serial interface
- FIFO is built in. (4-byte receive data buffer and 2-byte transmit data buffer are provided for each channel.)
- IrDA1.0 interface is built in.
- A baud-rate generator (12-bit programmable timer) is built in.
- Supports ISO7816 mode (available only for Ch.1)
 - Alternative transfer data direction (MSB first or LSB first)
 - Memory card interface compatible with ISO7816-3 T=0 & T=1 protocol
 - Programmable baud-rate and guard-time generation
 - ISO7816 acknowledge and automatically repeat transmission

● SPI (Serial Peripheral Interface)

- 4 channels of SPI
- Supports both master and slave modes.
- Data length: 1 to 8 bits
- Can be operated with up to a half of system frequency.
- Supports bit mask function and DMA transfer.

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● DCSIO (I²C master emulator)

- 4 channels of input/output ports with a serial shifter
- An I²C bus master control feature can be implemented.
- Input/output level detector to drive state machine
- Emulates 1-wire or 2-wire communication protocol by software

● Real Time Clock (RTC)

- Contains time counters (second, minute, and hour) and calendar counters (day, day of the week, month, and year).
- BCD data can be read/written from/to the counters.
- 24-hour or 12-hour mode can be selected.
- Operates with an independent power source (RTCVDD = 1.8 V typ.) separated from the system power source (LVDD).
- The WAKEUP output pin and the #STBY input pins are provided for standby/wake-up control of the chip.

● General-Purpose I/O Ports (GPIO)

- Maximum 96 I/O ports (in QFP20-184pin or PFBGA12U-180) or 64 I/O ports (in TQFP24-144pin) can be controlled.
- The pull-up resistors can be enabled/disabled with the control registers (except some I/O ports).
- * The I/O port pins are shared with other peripheral functions (e.g. interface, timer). Therefore, the number of GPIO ports depends on the peripheral functions used.

● Operating Voltage

- Core voltage (LVDD): 1.65 to 1.95 V (1.8 V typ.)
- I/O voltage (HVDD): 2.70 to 3.60 V (3.3 V typ.)
- SDRAM voltage (BUSVDD): 2.30 to 3.60 V (3.3 V typ.)
- RTC voltage (RTCVDD): 1.65 to 1.95 V (1.8 V typ.)
- PLL voltage (PLLVD): 1.65 to 1.95 V (1.8 V typ.)

● Operating Temperatures

- -40 to 85°C

● Current Consumption

- During execution (typ.)

CPU clock	Peripheral clock	SDRAM clock	Current consumption 1 (*1)	Current consumption 2 (*2)
20 MHz	20 MHz	20 MHz	17.0 mA	28.0 mA
25 MHz	25 MHz	25 MHz	21.0 mA	35.0 mA
33 MHz	33 MHz	33 MHz	27.0 mA	47.0 mA
45 MHz	45 MHz	45 MHz	37.0 mA	64.0 mA
48 MHz	48 MHz	48 MHz	40.0 mA	68.0 mA
60 MHz	30 MHz	60 MHz	50.0 mA	70.0 mA
66 MHz	33 MHz	66 MHz	55.0 mA	75.0 mA
72 MHz	36 MHz	72 MHz	60.0 mA	83.5 mA
84 MHz	42 MHz	84 MHz	69.0 mA	97.0 mA
90 MHz	45 MHz	90 MHz	74.0 mA	103.5 mA
20 MHz	20 MHz	40 MHz	14.0 mA	25.0 mA
27 MHz	27 MHz	54 MHz	17.5 mA	31.0 mA
33 MHz	33 MHz	66 MHz	23.0 mA	41.5 mA
40 MHz	40 MHz	80 MHz	31.0 mA	56.5 mA
45 MHz	45 MHz	90 MHz	33.0 mA	60.0 mA

*1: All peripheral clocks, OSC1, RTC, and PLL are turned On.

*2: All peripheral clocks (except SDRAM clock), OSC1, RTC, and PLL are turned Off.

*3: The current consumption in the above table indicates the value when a test program that consists of 55% load instructions, 23% arithmetic operation instructions, 1% mac instructions, 12% branch instructions and 9% ext instructions is being executed in the built-in RAM.

- In HALT mode (Typ.)

System clock	Current consumption (*4)
20 MHz	1.5 mA
25 MHz	1.9 mA
33 MHz	2.5 mA
45 MHz	3.3 mA
48 MHz	3.5 mA

*4: OSC1 and all peripheral circuits are turned OFF.

- In SLEEP mode (Typ.)

System clock	Current consumption
45/90 MHz (*5)	16.0 μ A
32 kHz	14.0 μ A
32 kHz (*6)	1.0 μ A

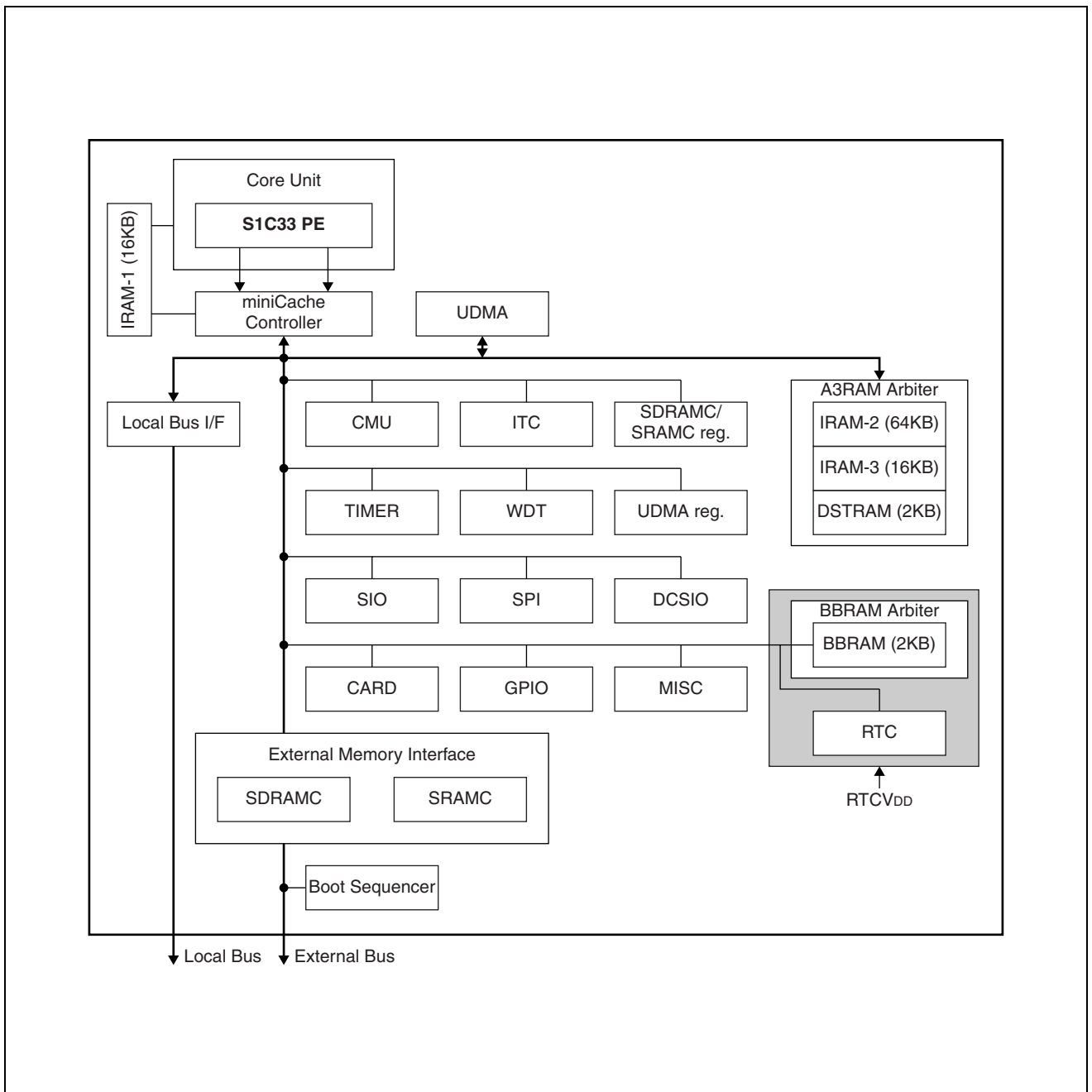
*5: Peripheral clock = 45 MHz, CPU clock = SDRAM clock = 90 MHz

*6: All power sources except for RTC (RTCVdd) are turned OFF.

● Shipping Form

- PFBGA12U-180 (12 mm × 12 mm × 1.2 mm, 0.8 mm ball-pitch)
- TQFP24-144pin (16 mm × 16 mm × 1.0 mm, 0.4 mm pin-pitch)
- QFP20-184pin (20 mm × 20 mm × 1.4 mm, 0.4 mm pin-pitch)

■ BLOCK DIAGRAM



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PIN LAYOUT DIAGRAM

