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S1C33A01

CMOS 32-bit Application Specific Controller

- 32-bit RISC CPU Core (EPSON S1C33 PE core) (Max. 90 MHz operation)
- 1KB Instruction Cache and 1KB Data Cache
- 100KB RAM (including cache and battery backup RAM)
- Programmable Operating Clock using PLL
  (division ratio: 1/1 to 1/16, multiplication rate: ×1 to ×16)
- Hardware Multimedia Accelerator (64-bit internal processing)
- Multifunctional Calculation Module
  (multiply and accumulation, matrix, and vector computations)
- I2S Audio Interface with One I nput and One Output Channel
  (supports 24-bit format)
- 16-ch. DMA Controller (triggered with peripheral circuits)
- Local Bus Interface for External LSI (8/16-bit data bus)
- SDRAM Controller with Burst Control
- Abundant Serial Inter faces (UART × 2ch., FSIO (serial I/F with FIFO, supports IrDA1.0) × 2ch., EFSIO(extended serial I/F with FIFO, supports ISO7816 mode/IrDA1.0) × 2ch., SPI × 4ch., DCSIO (I 2C bus master I/F emulator) × 4ch.)
- 4ch. of 16-bit PWM Control Timers with IGBT Control Function
- 4ch. of 8-bit programmable timers
- NAND Flash Inter face
- Infrared Remote Controller

■ DESCRIPTIONS

The S1C33A01 is a high performance 32-bit controller with various serial interfaces, I2S I/O interface, MMC controller and infrared remote controller. It is suitable for multimedia interface controllers such as audio and various I/O equipment.
The S1C33A01 provides an I2S interface that has bidirectional I/O channels, this allows recording and external audio input as well as audio and voice outputs. Also it has a hardware arithmetic accelerator to lighten the load on multimedia processing such as audio decoding. An audio player system can be implemented using the accelerator with the I2S interface.
The infrared remote controller, input ports and the serial interfaces are used to easily implement various user interfaces. The S1C33A01 supports reading/writing data from/to large capacity storage media such as various card media and Flash memory through the built-in MMC controller, SPI interface and SLC/MLC NAND Flash interface.
Furthermore, the local bus interface for an external LSI allows connection of an external LSI such as an LCD controller and USB controller to expand the functions. The S1C33A01 is equipped with the 32-bit RISC CPU core C33, 2KB instruction/data caches, 100KB RAM, DMA controller, memory controller (SRAM/SDRAM), various timers, real-time clock and general-purpose I/O ports as its basic functions, so it can also be used as a high performance general-purpose CPU. These S1C33A01 functions are implemented by EPSON SoC (System on Chip) design technology using 0.18 μm Multi-Vth. CMOS Process.

■ FEATURES

- Technology
  - 0.18 μm AL-4-layers Multi-Vth. CMOS process technology
- CPU
  - Seiko Epson original 32-bit RISC CPU Core C33 PE with AMBA bus, optimized for SoC
  - Maximum operating frequency: 90 MHz
  - Internal 2-stage pipeline
  - Instruction set: 125 instructions (16-bit fixed length)
  - Cache: 1KB instruction cache and 1KB data cache
  - Memory space
    - Up to 4GB accessible (32-bit address)
- Internal Memories (RAM)
  - 16KB IRAM 1 Used as a general-purpose RAM. 2KB are used as cache.
  - 64KB IRAM 2 Used as a general-purpose RAM.
  - 16KB IRAM 3 Used as a general-purpose RAM.
  - 2KB DST RAM Used as a general-purpose RAM or a DMA descriptor table RAM.
  - 2KB BBRAM Data can be held by a power supply separated with the system power.
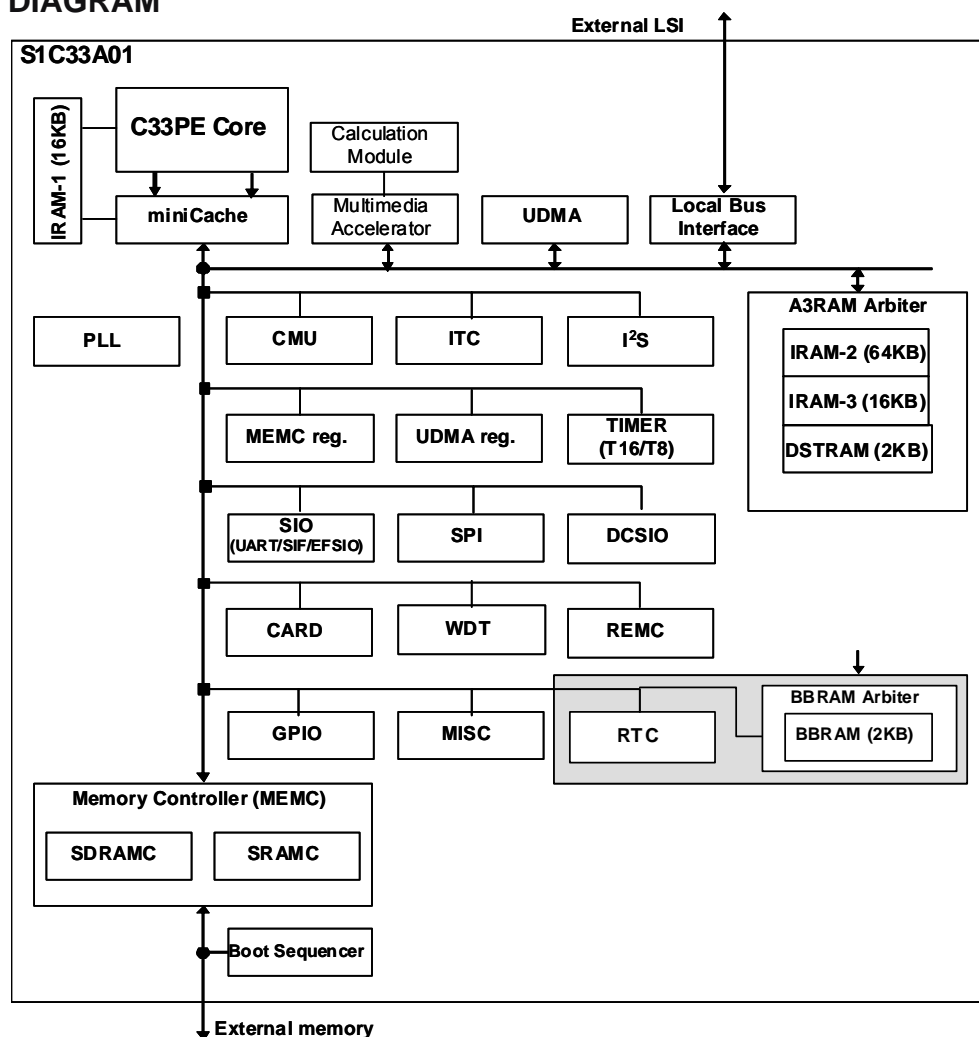- Operating Clock
  - Main clock
    - 100 MHz (max.) (TBD)

- On-chip oscillator (crystal or ceramic) or external clock input
- PLL: Integer multiplication PLL circuit
- Sub clock
  - 32.768kHz(typ.) for RTC or low-speed (low power) operation
  - On-chip oscillator (crystal

● Mini Cache Controller (mini Cache)
- 1KB instruction cache and 1KB data cache with 4-way associative frame architecture
- LRU replacement algorithm
- Automatic lock function in debug mode or interrupt handling with specified priority
- Write through function with 1-word write buffer
  * Cache memory is shared with IRAM1.

● Multimedia Accelerator
- Hardware continuous multiply and accumulation circuit (64-bit internal processing)
- Supports signed/unsigned integer arithmetic operations and fixed-point arithmetic operations with saturation processing.

● Universal DMA Controller (UDMA)
- 2 channels of fast-UDMA and 14 channels of table-UDMA
- Dual-address transfer (source and destination addresses are specified)
- Supports single or successive transfer.
- High performance burst transfer function through SDRAM controller
- 1-byte, 1-halfword, 1-word, 4-byte, 4-halfword or 4-word burst transfer programmable
- Built-in DMA trigger system with a linkage function
- Software or hardware triggers are selectable.

● SRAM Controller (SRAMC)
- Provides up to 8 chip enable signals to connect external devices.
- Flash ROM, SRAM, or ASSP (LCD driver) devices can be connected.
- 24-bit address bus and 8/16-bit selectable data bus
- Programmable bus access wait cycles (1 to 16 cycles)
- Supports little endian access.
- Memory mapped I/O
- A memory area (Area 6) is reserved for on-chip resources use.
- Supports both A0 and BS (Bus Strobe) access types.
- Supports external wait requests using the #WAIT pin.

● SDRAM Controller (SDRAMC)
- 16-bit SDRAM interface up to 90 MHz clock rate (TBD)
- Supports 16M-bit (2MB) to 512M-bit (64MB) SDRAM.
- Embedded IQB (Instruction Queue Buffer) and DQB (Data Queue Buffer) (mini-cache must be disabled.)
- Optimized multi-master access request to minimize average read latency
- Programmable CAS latency, 1, 2 and 3
- Supports burst transfer.
- Sync. clock is configurable into the same or double CPU clock frequency.
- Incorporates a 12-bit auto-refresh counter.
- Intelligent self-refresh function for low power operation

● Multifunctional Calculation Module (Calculation Module)
- Vector computations (addition, subtraction and multiplication)
- Multiply and accumulation (MAC)
- Matrix computation ($2 \cdot 2$, $3 \cdot 3$, $4 \cdot 4$)
- Affine transformation ($3 \cdot 3 + 3$)
- Butterfly computation
- Supports signed/unsigned 32-bit integer operation mode and 32-bit fixed-point values operation mode with saturation processing.

● I2S Audio Interface (I2S)
- Supports universal audio I_2S bus interface.
- I_2S bus interface with 1 input channel and 1 output channel
- Supports up to 24-bit data format.
- DAC device clock, word clock and bit clock can be controlled in output channel (external clock can be used).
- Provides FIFO (24 bits $\cdot$ 2 channels $\cdot$ 4) individually for input and output channels.
- Supports DMA transfer.
  *An external DAC and/or ADC are required to output an audio signal to speakers/ear phone and/or to input sound from a microphone.

● Local Bus for External LSI
- An 8/16-bit local bus to connect a graphics LSI or a USB LSI.
- Maximum 8MB or 16MB local bus address space (up to 24 address signals are available.)
- External wait requests input to the #LWAIT/#LREADY pin are acceptable.
- Supports single address mode DMA.

● Clock Management Unit (CMU)

- Selects the system clock source (OSC3, PLL or OSC1).
- Controls the OSC3 and OSC1 oscillator circuits.
- Controls the clock division ratio (1/1 to 1/16) and PLL frequency multiplication rate (·1 to ·16).
- Controls clocks in standby mode (SLEEP and HALT).
- Controls division ratios of the internal core and peripheral clocks. Controls external bus clock.

● Interrupt Controller (ITC)
- Controls 16 channels of interrupts reserved for C33 PE Core.
- Supports 48 channels of interrupt sources (some of them are reserved).

● Watchdog Timer (WDT)
- 30-bit watchdog timer that generates a NMI (non-maskable interrupt) or reset
- The watchdog timer overflow period (NMI/reset generation cycle) can be programmed.
- The watchdog timer overflow signal can be output to external devices.

● 16-bit Timers (T16)
- 4 channels of 16-bit timer/counters with PWM control function
- A digital DAC function is implemented using the PWM output and an external RC filter.
- 4 channels of built-in output comparators can be used for controlling IGBT.

● 8-bit Timers (T8)
- 4 channels of 8-bit programmable timer/counters
  * Two channels are reserved as the baud-rate counters for the serial interface (UART).

● Serial Interface (UART, FSIO, EFSIO)
- UART
  - 2 channels of UART
  - Supports IrDA 1.0 interface
  - Contains 2-byte receive data buffer and 1-byte transmit data buffer to support full-duplex communication.
  - Transfer rate: 150 to 115200 bps
  - Data length: 7 or 8 bits
  - Parity mode: even, odd or no parity
  - Stop bit: 1 or 2 bits
  - Parity error, framing error and overrun error are detectable.
  - Supports DMA transfer.
- FSIO (serial interface with FIFO)
  - 2 channels of clock synchronous/asynchronous serial interface
  - Contains FIFO (4-byte receive data buffer and 2-byte transmit data buffer are available for each channel).
  - Contains an IrDA1.0 interface.
  - Contains a baud-rate generator (12-bit programmable timer).
  - Supports DMA transfer.
- EFSIO (extended serial interface with FIFO)
  - 2 channels of clock synchronous/asynchronous serial interface
  - Contains FIFO (4-byte receive data buffer and 2-byte transmit data buffer are available for each channel).
  - Contains an IrDA1.0 interface.
  - Contains a baud-rate generator (12-bit programmable timer).
  - Supports ISO7816 mode (Ch.1 only).
    Alternative MSB or LSB
    Memory card interface compatible with ISO7816-3 T=0 & T=1 protocol
    Programmable baud-rate and guard-time generation
    ISO7816 acknowledge and automatically repeat transmission
  - Supports DMA transfer.

● SPI (Serial Peripheral Interface)
- 4 channels of SPI
- Supports both master and slave modes.
- Data length: 1 to 8 bits
- Can be operated with up to a half of the system clock frequency.
- Supports DMA transfer.

● DCSIO (I_2C Master Emulator)
- 4 channels of I/O ports with a serial shifter
- Emulates I_2C master device.
- Input/output level detector to drive state machine
- Emulates 1-wire or 2-wire communication protocol by software.
- Supports DMA transfer.

● Real Time Clock (RTC)
- Contains time counters (second, minute, and hour) and calendar counters (day, day of the week, month, and year).
- BCD data can be read/written from/to the counters.
- 24-hour or 12-hour mode can be selected.
- Operates with the power source ($RTCV_{DD}$ = 1.8 V typ.) separated from the system power supply (LV_{DD}).
- The WAKEUP output pin and #STBY input pin are provided for chip standby/wakeup control.

● General-purpose I/O Port Control (GPIO)
- Controls up to 96 (QFP20-184pin, PFBGA12U-180) or 64 (TQFP24-144pin) I/O ports.

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- Built-in pull-up resistors can be controlled by software (except some ports).
  The I/O ports are shared with other peripheral function pins (for interfaces and timers). Therefore, the number of I/O ports depends on the peripheral functions used.
- SLC/MLC NAND Flash Interface with Reed-Solomon ECC (CARD)
  - 8-bit SLC/MLC NAND Flash can be controlled.
  - Hardware Reed-Solomon ECC calculation for SLC/MLC NAND Flash
    The hardware Reed-Solomon ECC calculation function supports error detection only.
  - Provides SmartMedia I/F signals (#SMRE and #SMWE can be generated).
  - Supports NAND Flash booting function.
- Infrared Remote Controller (REMC)
  - Infrared remote controller with 1 input channel and 1 output channel
  - Duty and pulse width can be configured in bit units (supports various logical formats by software control).
    An external infrared detecting unit is required to receive infrared remote control signals.
- Operating Voltage
  - Core voltage (LV$_{DD}$): 1.65 to 1.95 V (1.80 V typ.)
  - I/O voltage (HV$_{DD}$): 2.70 to 3.60 V (3.30 V typ.)
  - System bus voltage (BUSV$_{DD}$): 2.30 to 3.60 V (3.30 V typ.)
  - RTC voltage (RTCV$_{DD}$): 1.65 to 1.95 V (1.80 V typ.)
  - PLL voltage (PLLV$_{DD}$): 1.65 to 1.95 V (1.80 V typ.)
- Operating Temperatures
  - -40 to 85°C
- Power Consumption
  - During SLEEP: 1.0 uA (While only RTC is operating (Power is supplied only to RTCVDD and not supplied to all others)
  - During HALT: 3.5 mA (When PLL = Off, and all clocks are set to 48MHz)
  - During execution: 103.5 mA (When PCLK = 45MHz, MCLK = SDCLK = 90MHz, and the clock is supplied to all peripheral circuites)
    By controlling the clocks through the clock management unit (CMU), power consumption can be reduced.
- Shipping Form
  - PFBGA12U-180 (12 mm × 12 mm × 1.2 mm, 0.8 mm ball-pitch)
  - TQFP24-144pin (16 mm × 16 mm × 1.0 mm, 0.4 mm pin-pitch)
  - QFP20-184pin (20 mm × 20 mm × 1.4 mm, 0.4 mm pin-pitch)

■ BLOCK DIAGRAM

NOTICE: