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S1V30120

Application Note

(Application Circuit Example)

SEIKO EPSON CORPORATION

Rev. 1.06

NOTICE

Table of Contents

1. Outline

This application note describes an application circuit example for the S1V30120.

2. Application Circuit Example

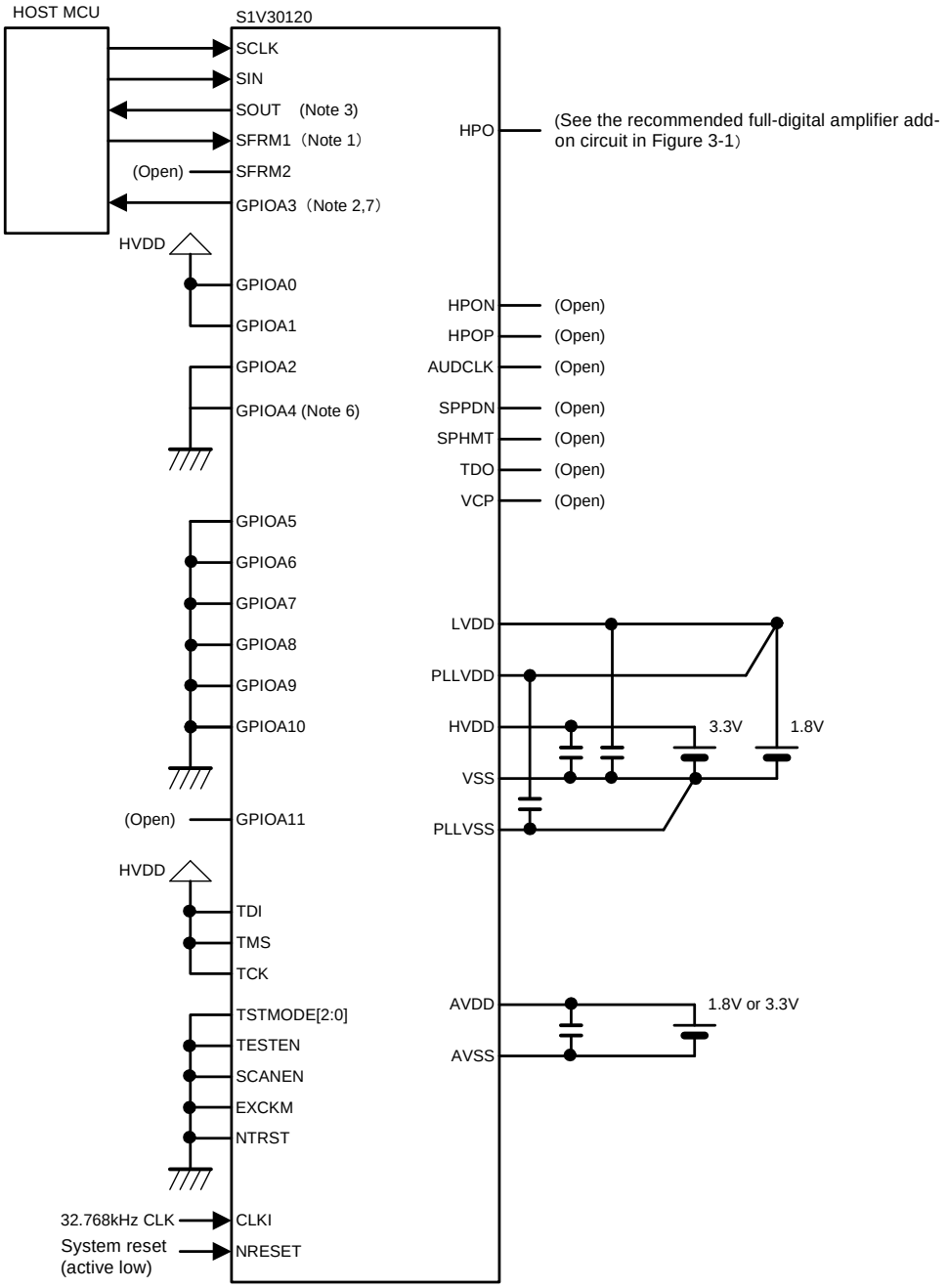


Figure 2.1 Application circuit example

Notes:

1. For the connection with clock synchronous serial interface, also refer to Chapter 7, “S1V30120 Hardware Specifications.” When controlling the SFRM1 pin by the CPU port, set the SFRM1 pin to Low before transmitting each message and set it to High after receiving all messages. For details on RESP and other messages, refer to the”S1V30120 Message Protocol Specifications.”
2. For GPIOA3 setups, also refer to Section 3.2 of the “S1V30120 Message Protocol Specifications.” Generating an interrupt at the rising edge of GPIO3 (MSG_READY) allows the CPU to reduce the load of controlling the S1V30120.
3. The SOUT pin is internally pulled up from the power-on to the completion of initialization. If the SOUT pin is externally pulled down, their lines may go into the middle-level state. To avoid this, turn off the external pull-down resistors. And please connect SOUT to 50kohms resister. After initialization SOUT pin is pulled down when SFRM1=High. Therefore if SOUT is shared with the other deivce, S1V30120 should be connected Tri-state buffer IC controlled by SFRM1.
4. The voltage fluctuation of the AVDD power line may degrade the electrical characteristics of full digital amplifiers. Make sure to use stable power supply.
5. The S1V30120 initialization sequence is as follows:

   Step 1: Sets the SPI port on the CPU active.

   Step 2: Starts supplying the system clock signal to the S1V30120.

   Step 3: Releases the system reset signal to the S1V30120.

   Note: For the timings of power-on, clock and reset, refer to Section 6.4.2 of the ”S1V30120 Hardware Specifications” as well.
6. The GPIOA4 pin is internally pulled down from the power-on to the completion of initialization. If the GPIOA4 pin is externally pulled up, their lines may go into the middle-level state. To avoid this, turn off the external pull-up resistors.
7. The GPIOA3 pin is internally pulled down from the power-on to the completion of initialization. If the GPIOA3 pin is externally pulled up, their lines may go into the middle-level state. To avoid this, turn off the external pull-up resistors. And please connect GPIOA3 to 50 kohms pulled down resister.

3. Example External Audio Output Circuits

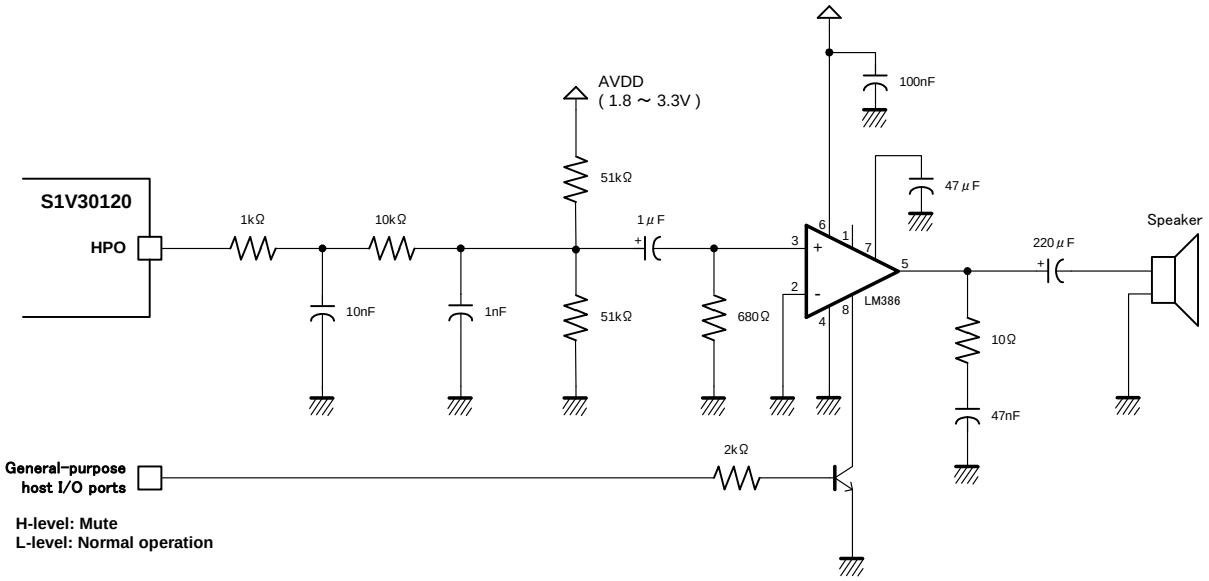


Figure 3.1 Example of full-digital amplifier add-on circuit using a linear op-amp

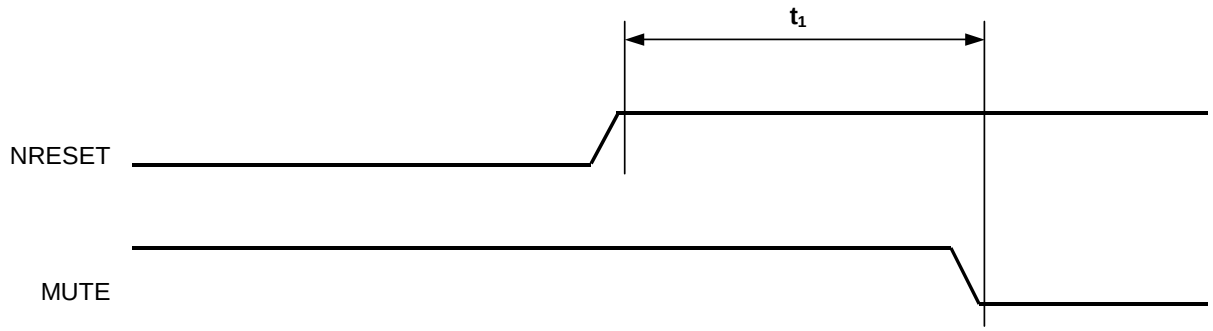
Notes:

Figure 3.1 shows an example of the full-digital amplifier add-on circuit. To reduce noise when powering on, it is recommended to control the mute function of the speaker amplifier using a general-purpose I/O port.

Minimize the wire length from the HPO pin of the S1V30120 to the LPF (1KΩ, 10nF, 10KΩ, 1nF). The GND end of the second LPF capacitor (10nF, 1nF) should be connected with the AVSS of S1V30120 by the shortest possible wire.

4. Mute Timing

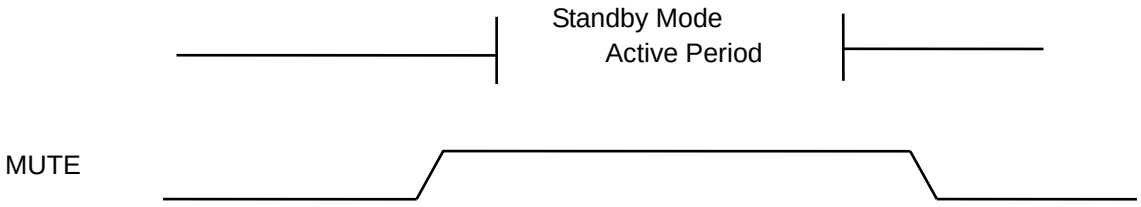
■ RESET Valid → Invalid



Symbol	Parameter	Min.	Max.	Unit
t_1	Delay from NRESET released to MUTE released.	120	-	ms

Note: In the timing chart above, the MUTE signal to the external circuit is active high.

■ Stand-by



The following is the flow of MUTE control before and after the Standby Mode:

◆ When entering the Standby Mode:
Receive FINISHED_IND → Enable MUTE → Issue the Standby Command

◆ When exiting from the Standby Mode:
Send STANDBY_EXIT_IND → Wait 120ms → Receive STANDBY_EXIT_IND → Release MUTE

For more information on the Standby Mode, refer to the “Message Protocol Specifications.”

■ In the timing chart above, the MUTE signal to the external circuit is active high.

Revision History

Date	Revision details			
	Rev.	**Page**	**Type**	**Details**
07/03/2007	1.01	All	New	change the format
10/18/2007	1.02	All	Revise	2.Application circuit example Add Notes 6: The GPIOA4 pin is internally pulled down from the power-on to the completion of initialization. If the GPIOA4 pin is externally pulled up, their lines may go into the middle-level state. To avoid this, turn off the external pull-up resistors.
10/29/2007	1.03	Page.2	Add	2.Applicatin circut example Add Notes 7: The GPIOA3 pin is internally pulled down from the power-on to the completion of initialization. If the GPIOA3 pin is externally pulled up, their lines may go into the middle-level state. To avoid this, turn off the external pull-up resistors. And please connect GPIOA3 to 50 ohms pulled down resister.
01/15/2008	1.04	Page.1	Revise	Modified Fig2.1GPIOA3 arrow direction.
06/26/2008	1.05	Page.2	Revise	Notes 3: To avoid this, turn off the external pull-down resistors. And please connect SOUT to 50kohms resister. Notes 7: And please connect GPIOA3 to 50 kohms pulled down resister.
04/05/2010	1.06	Page.2	Revise	Notes 3: If SOUT is shared with the other deivce, S1V30120 should be connected Tri-state buffer IC controlled by SFRM1.

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