S1C17602

EPSON
EXCEED YOUR VISION

- ●Low power MCU (Operating voltage 1.8V, 0.75μA/SLEEP, 2.5μA/HALT)
- ●Built in Flash memory (64K bytes). 8.2MHz high-speed operation with 1.8V low voltage.
- ●Built-in LCD driver (with booster circuit for power supply voltage)
- ●10-bit A/D converter ±1.5 LSB, R/F converter
- ●Has compact codes optimized for C, and high throughput of an instruction/clock. Supports serial ICE, and comes equipped with RISC CPU core S1C17.

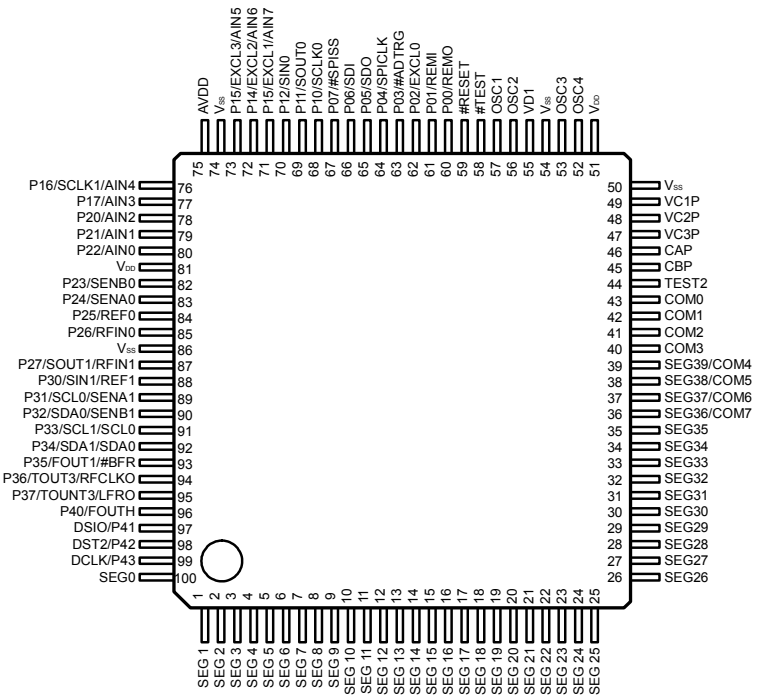
■ DESCRIPTIONS

S1C17602 is a 16-bit MCU that has achieved high processing speeds with low voltage operation, compact size, wide address space and on-chip ICE. It has a built-in A/D converter and R/F converter enabling S1C17602 to connect to various analog I/F sensors. It is suitable for applications including sensor-equipped health care appliances, sports watches and meter modules, products requiring battery operation, and compact and highly precise display.

■ FEATURES

● CPU	EPSON originally designed 16-bit RISC CPU core S1C17, 16-bit x 16-bit + 32-bit product sum computing unit
● IOSC oscillator circuit	2.7MHz (±20% @1.8 V, 25°C), Oscillation start time 5 μsec. (Max.)
● OSC3 oscillator circuit	Crystal oscillation circuit/Ceramic oscillation circuit 8.2MHz (Max.)
● OSC1 oscillator circuit	Crystal oscillation circuit 32.768KHz (standard value)
● Internal flash memory	64K bytes shared by instructions/data. Allows 1,000 rewrites (Min.) Read/write protection function. Allows onboard rewriting with the ICD Mini debug tool self-rewriting via software.
● Internal RAM	4K bytes
● Internal Display RAM	40 bytes
● A/D converter	10-bit resolution, ±1.5 LSB, 8 ch, AVDD = 1.8 V - 3.6 V
● R/F converter	DC oscillation/AC oscillation/External input 2ch.
● Input/output port	Max. 36-bit general purpose input/output
● Serial interface	SPI (master/slave) 1 ch I^2C (master) 1 ch I^2C (slave) 1 ch UART (supports IrDA1.0) 2 ch Remote controller(REMC) 1 ch
● Timer	8-bit timer (T8F) 2 ch 16-bit timer (T16) 3 ch PWM capture timer (T16E) 1 ch Clock timer (CT) 1 ch Stopwatch timer (SWT) 1 ch Watchdog timer (WDT) 1 ch 8-bit OSC1 timer (T8OSC1) 1 ch
● LCD driver	40 SEG x 4 COM, or 36 SEG x 8 COM, 1/3 bias, built in power supply voltage booster circuit.
● Supply voltage detector(SVD)	15 values programmable (1.8 V – 3.2 V)
● Interrupts	NMI P port input 2 systems Serial interface 5 systems Timer 9 systems LCD 1 system SVD 1 system ACD 1 system RFC 1 system
● Supply voltage	V_{DD} = 1.8 - 3.6 V (1.8 V low power internally with regulator during normal operation) V_{DD} = 2.7 - 3.6 V (2.5 V internally when erasing/writing flash ROM)
● Current consumption	SLEEP mode: 0.75 μA typ. (OSC1=OFF, IOSC=OFF, OSC3=OFF) HALT mode: 2.5 μA typ. (OSC1=32kHz, IOSC=OFF, OSC3=OFF, PCKEN=0x0, LCD OFF) Operating mode: 15 μA typ. (OSC1=32kHz, IOSC=OFF, OSC3=OFF, LCD=OFF) 410 μA typ. (OSC1=OFF, IOSC=OFF, OSC3=1MHz ceramic oscillator)
● Shipment package	PTQFP14-100 12 x 12 mm (body) 0.4 mm pitch, VFBGA7H-144 7 x 7 mm (body) 0.5 mm pitch, Bare chip 100 μm pitch

■ PTQFP14-100 PIN ASSIGNMENT



■ VFBGA7H-144 PIN DESCRIPTION

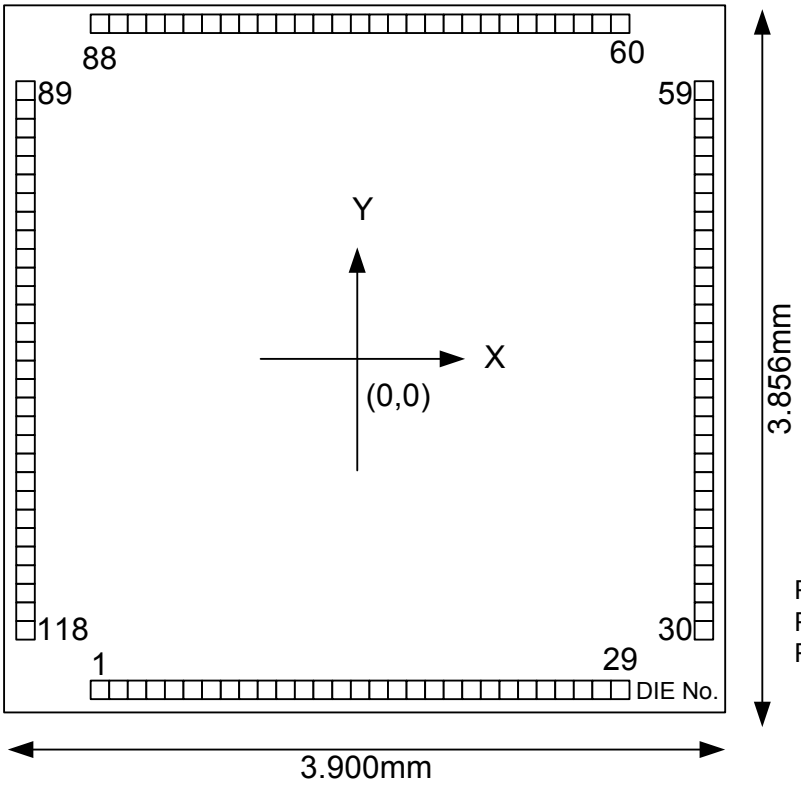
	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	NC	DCLK	DST2	DSIO	P37	P34	P27	VSS	P26	VDD	P21	P16	NC	A
B	SEG1	SEG0	VSS	VSS	P36	P33	P31	P30	P24	P22	P20	VSS	AVDD	B
C	SEG3	SEG4	SEG2	VSS	P40	P35	P32	VSS	P25	P23	P17	P15	P14	C
D	SEG5	SEG6	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	P13	P12	D
E	SEG8	SEG7	VSS	VSS						VDD	VDD	P11	P10	E
F	SEG10	SEG11	SEG9	VSS						VDD	VDD	P07	P06	F
G	SEG13	SEG14	SEG12	VSS						VSS	P05	P04	P03	G
H	SEG16	SEG15	VSS	VSS						VDD	P02	P01	P00	H
J	SEG18	SEG17	VSS	VSS						VDD	VDD	#TEST	#RESET	J
K	SEG21	SEG20	SEG19	VSS	VSS	VSS	VSS	VSS	VDD	VSS	VD1	OSC1	OSC2	K
L	SEG23	SEG22	VSS	SEG29	SEG32	COM6	COM3	COM0	TEST1	VC3	VDD	VDD	VSS	L
M	SEG25	SEG24	SEG27	SEG30	SEG34	COM7	COM4	COM1	TEST2	CA	VC1	OSC3	OSC4	M
N	NC	SEG26	SEG28	SEG31	SEG33	SEG35	COM5	COM2	TEST3	CB	VC2	VSS	NC	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

■ S1C17602 PTQFP14-100 PIN DESCRIPTION

Pin name	Pin No.		I/O	Initial state	Function
	QFP	VFBGA			
SEG1-35	1-35	B1, C3, C1, C2, D1, D2, E2, E1, F3, F1, F2, G3, G1,G2, H2, H1, J2, J1, K3, K2, K1, L2, L1, M2, M1,N2, M3,N3, L4, M4, N4, L5, M5,N5, N6	O	O(L)	LCD segment output
SEG36-39/COM7-4	36-39	M6,L6, N7, M7	O	O(L)	LCD segment output/LCD common output
COM3-0	40-43	L7, N8, M8, L8	O	O(L)	LCD common output
TEST2	44	M9	—	—	Test pin (fixed to V_{DD} at normal operation)
CBP	45	N10	—	—	Connected to LCD booster capacitor
CAP	46	M10	—	—	Connected to LCD booster capacitor
VC3P	47	L10			LCD related drive power voltage output
VC2P	48	N11			LCD related drive power voltage output
VC1P	49	M11			LCD related drive power voltage output
V_{SS}	50	N12	—	—	Power supply (-)
V_{DD}	51	L12			Power supply (+)
OSC4	52	M13	O	O	OSC3 oscillation output
OSC3	53	M12	I	I	OSC3 oscillation input
V_{SS}	54	L13	—	—	Power supply (-)
VD1	55	K11	—	—	Constant voltage circuit output related to internal logic and oscillation
OSC2	56	K13	O	O	OSC1 oscillation output
OSC1	57	K12	I	I	OSC1 oscillation input
#TEST	58	J12	I	I(Pull-UP)	Test pin (fixed to High at normal operation)
#RESET	59	J13	I	I(Pull-UP)	Initial set input
P00/REMO	60	H13	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/REMC output
P01/REMI	61	H12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/REMC input
P02/ EXCL0	62	H11	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/T16 ch. 0 external clock input
P03/#ADTRG	63	G13	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/AD conversion external trigger
P04/SPICLK	64	G12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/SPI clock input/output
P05/SDO	65	G11	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/SPI data output
P06/SDI	66	F13	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/SPI data input
P07/#SPISS	67	F12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/SPI slave select input
P10/SCLK0	68	E11	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/UART ch. 0 clock input
P11/SOUT0	69	E12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/UART ch. 0 data output
P12/SIN0	70	D13	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/UART ch. 0 data input
P13/EXCL1/AIN7	71	D12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/T16 ch. 1 external clock input/AD converter ch. 7 input

Pin name	Pin No.		I/O	Initial state	Function
	QFP	VFBGA			
P14/EXCL2/AIN6	72	C13	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/T16 ch. 2 external clock input/AD converter ch. 6 input
P15/ EXCL3/AIN5	73	C12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/T16E ch. 0 external clock input/AD converter ch. 5 input
VSS	74	B12	—	—	Power supply (-)
AVDD	75	B13	I/O	I(Pull-UP)	Analog power supply (+)
P16/SCLK1/AIN4	76	A12	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/UART ch. 1 clock input/AD converter ch. 4 input
P17/AIN3	77	C11	I/O	I(Pull-UP)	Port shared by input/output (with interrupt)/AD converter ch. 3 input
P20/AIN2	78	B11	I/O	I(Pull-UP)	Port shared by input/output /AD converter ch. 2 input
P21/AIN1	79	A11	I/O	I(Pull-UP)	Port shared by input/output /AD converter ch. 1 input
P22/AIN0	80	B10	I/O	I(Pull-UP)	Port shared by input/output /AD converter ch. 0 input
VDD	81	A10	—	—	Power supply (+)
P23/SENB0	82	C10	I/O	I(Pull-UP)	Port shared by input/output /for RF converter
P24/SENA0	83	B9	I/O	I(Pull-UP)	Port shared by input/output /for RF converter
P25/REF0	84	C9	I/O	I(Pull-UP)	Port shared by input/output /for RF converter
P26/RFIN0	85	A9	I/O	I(Pull-UP)	Port shared by input/output /for RF converter
VSS	86	A8	—	—	Power supply (-)
P27/SOUT1/RFIN1	87	A7	I/O	I(Pull-UP)	Port shared by input/output /UART ch. 1 data output /for RF converter
P30/SIN1/REF1	88	B8	I/O	I(Pull-UP)	Port shared by input/output /UART ch. 1 data input /for RF converter
P31/SCL0/SENA1	89	B7	I/O	I(Pull-UP)	Port shared by input/output /I2C master clock output /for RF converter
P32/SDA0/SENB1	90	C7	I/O	I(Pull-UP)	Port shared by input/output /I2C master data input/output /for RF converter
P33/SCL1/SCL0	91	B6	I/O	I(Pull-UP)	Port shared by input/output /I2C slave clock input /I2C master clock output
P34/SDA1/SDA0	92	A6	I/O	I(Pull-UP)	Port shared by input/output /I2C slave data input/output /I2C master data input/output
P35/ FOUT1/#BFR	93	C6	I/O	I(Pull-UP)	Port shared by input/output /OSC1 external clock output /I2C slave bus release
P36/TOUT3/RFCLKO	94	B5	I/O	I(Pull-UP)	Port shared by input/output /T16E ch. 0 PWM signal output (non-inverted) /RF clock monitor
P37/TOUTN3/LFRO	95	A5	I/O	I(Pull-UP)	Port shared by input/output /T16E ch. 0 PWM signal output (inverted) /LCD frames output
P40/FOUTH	96	C5	I/O	I(Pull-UP)	Port shared by input/output /HSCLK clock output (with division)
DSIO/P41	97	A4	I/O	I(Pull-UP)	Port shared by input/output of on-chip debugger data, and input/output
DST2/P42	98	A3	I/O	O(L)	Port shared by output of on-chip debugger status, and input/output
DCLK/P43	99	A2	I/O	O(H)	Port shared by output of on-chip debugger clock, and input/output
SEG0	100	B2	O	O(L)	LCD segment output

■ S1C17602 PAD LAYOUT DRAWING



PAD opening
Pad No. 1 - 29, 60 - 88 : 87 x 85um
Pad No.30 - 59, 89 - 118 : 85 x 87um

■ S1C17602 PAD COORDINATE

PAD No.	X (mm)	Y (mm)	Allocation	PAD No.	X (mm)	Y (mm)	Allocation	PAD No.	X (mm)	Y (mm)	Allocation
1	-1.4	-1.827	N.C.	51	1.849	0.67	TEST3	101	-1.849	0.27	P27
2	-1.3	-1.827	SEG1	52	1.849	0.77	TEST2	102	-1.849	0.17	P30
3	-1.2	-1.827	N.C.	53	1.849	0.87	TEST1	103	-1.849	0.07	P31
4	-1.1	-1.827	SEG2	54	1.849	0.97	CB	104	-1.849	-0.03	P32
5	-1	-1.827	SEG3	55	1.849	1.07	CA	105	-1.849	-0.13	P33
6	-0.9	-1.827	SEG4	56	1.849	1.17	VC3	106	-1.849	-0.23	P34
7	-0.8	-1.827	SEG5	57	1.849	1.27	VC2	107	-1.849	-0.33	P35
8	-0.7	-1.827	SEG6	58	1.849	1.37	VC1	108	-1.849	-0.43	P36
9	-0.6	-1.827	SEG7	59	1.849	1.48	VSS	109	-1.849	-0.53	P37
10	-0.5	-1.827	SEG8	60	1.5	1.827	VDD	110	-1.849	-0.63	N.C.
11	-0.4	-1.827	SEG9	61	1.4	1.827	OSC4	111	-1.849	-0.73	P40
12	-0.3	-1.827	SEG10	62	1.3	1.827	OSC3	112	-1.849	-0.83	DSIO
13	-0.2	-1.827	SEG11	63	1.2	1.827	VSS	113	-1.849	-0.93	DST2
14	-0.1	-1.827	SEG12	64	1	1.827	VD1	114	-1.849	-1.03	N.C.
15	0	-1.827	SEG13	65	0.9	1.827	OSC2	115	-1.849	-1.13	DCLK
16	0.1	-1.827	SEG14	66	0.8	1.827	OSC1	116	-1.849	-1.23	N.C.
17	0.2	-1.827	SEG15	67	0.7	1.827	#TEST	117	-1.849	-1.33	SEG0
18	0.3	-1.827	SEG16	68	0.6	1.827	#RESET	118	-1.849	-1.43	N.C.
19	0.4	-1.827	SEG17	69	0.5	1.827	N.C.				
20	0.5	-1.827	SEG18	70	0.4	1.827	P00				
21	0.6	-1.827	SEG19	71	0.3	1.827	N.C.				
22	0.7	-1.827	SEG20	72	0.2	1.827	P01				
23	0.8	-1.827	SEG21	73	0.1	1.827	P02				
24	0.9	-1.827	SEG22	74	0	1.827	P03				
25	1	-1.827	SEG23	75	-0.1	1.827	P04				
26	1.1	-1.827	SEG24	76	-0.2	1.827	P05				
27	1.2	-1.827	N.C.	77	-0.3	1.827	P06				
28	1.3	-1.827	SEG25	78	-0.4	1.827	P07				
29	1.4	-1.827	N.C.	79	-0.5	1.827	P10				
30	1.849	-1.43	N.C.	80	-0.6	1.827	P11				
31	1.849	-1.33	SEG26	81	-0.7	1.827	N.C.				
32	1.849	-1.23	N.C.	82	-0.8	1.827	P12				
33	1.849	-1.13	SEG27	83	-0.9	1.827	N.C.				
34	1.849	-1.03	N.C.	84	-1	1.827	P13				
35	1.849	-0.93	SEG28	85	-1.1	1.827	P14				
36	1.849	-0.83	SEG29	86	-1.2	1.827	P15				
37	1.849	-0.73	SEG30	87	-1.3	1.827	VSS				
38	1.849	-0.63	SEG31	88	-1.4	1.827	AVDD				
39	1.849	-0.53	SEG32	89	-1.849	1.47	P16				
40	1.849	-0.43	SEG33	90	-1.849	1.37	P17				
41	1.849	-0.33	SEG34	91	-1.849	1.27	P20				
42	1.849	-0.23	SEG35	92	-1.849	1.17	P21				
43	1.849	-0.13	COM7	93	-1.849	1.07	P22				
44	1.849	-0.03	COM6	94	-1.849	0.97	VDD				
45	1.849	0.07	COM5	95	-1.849	0.87	P23				
46	1.849	0.17	COM4	96	-1.849	0.77	P24				
47	1.849	0.27	COM3	97	-1.849	0.67	P25				
48	1.849	0.37	COM2	98	-1.849	0.57	P26				
49	1.849	0.47	COM1	99	-1.849	0.47	VSS				
50	1.849	0.57	COM0	100	-1.849	0.37	N.C.				

Note) Open the pin at the N.C. pad.

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■ EPSON Electronic devices Website

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