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Interlace / Progressive Conversion IC

S2S65P10
Data Sheet

SEIKO EPSON CORPORATION

Rev.1.0

NOTICE

CONTENTS

1. DESCRIPTION

S2S65P10 is an IC which converts the interlace signals into the progressive signals. Combining S2S65P10 with S1S65010 (or S2S65A00) makes it possible to convert the NTSC / PAL digital signals sent from a video decoder into the JPEG format. S2S65P10 has a large SRAM built in, so it requires no external RAM. S2S65P10 has four channels of video input, and provides versatile video outputs, including fixed, auto-scan, and 4-input-merge screen outputs. It has also the motion detect function built in. It interrupts the host CPU upon detecting a moving object, so it saves power consumption of the system.

2. FEATURE

- Video input
  4 channel inputs (any one of them can be set to an output)
  8 bit input
  Support ITU-R BT.601 (4:2:2) / ITU-R BT.656
  Support NTSC / PAL
  Support the interlace / progressive inputs

- Video output
  2 channel outputs (one of them is shared by video input)
  8 bit output
  Support ITU-R BT.601 (4:2:2) / ITU-R BT.656
  Support progressive output
  VGA, 30frame/sec
  4 - 1 Intelligent Image Switch Function
  Support 4-inputs-merged screen (QVGA × 4 = VGA)

- Host Interface
  I^2C Interface
  Interrupt output (Interrupted upon by area sensor)

- Image Processing
  Interlace / progressive conversion
  Aspect conversion
  Area sensor (for motion detect)

- I^2C Through Function (Camera control or video decoder control) / GPIO

- No external RAM required

- Operating temperature: -40 to +105 °C (T_a)

- CMOS 0.18μm Process

- Operating voltage IO: 2.4 to 3.6V / Internal: 1.8 ± 0.15V

- Package: QFP15-100pin (0.5mm pitch)

3. BLOCK DIAGRAM

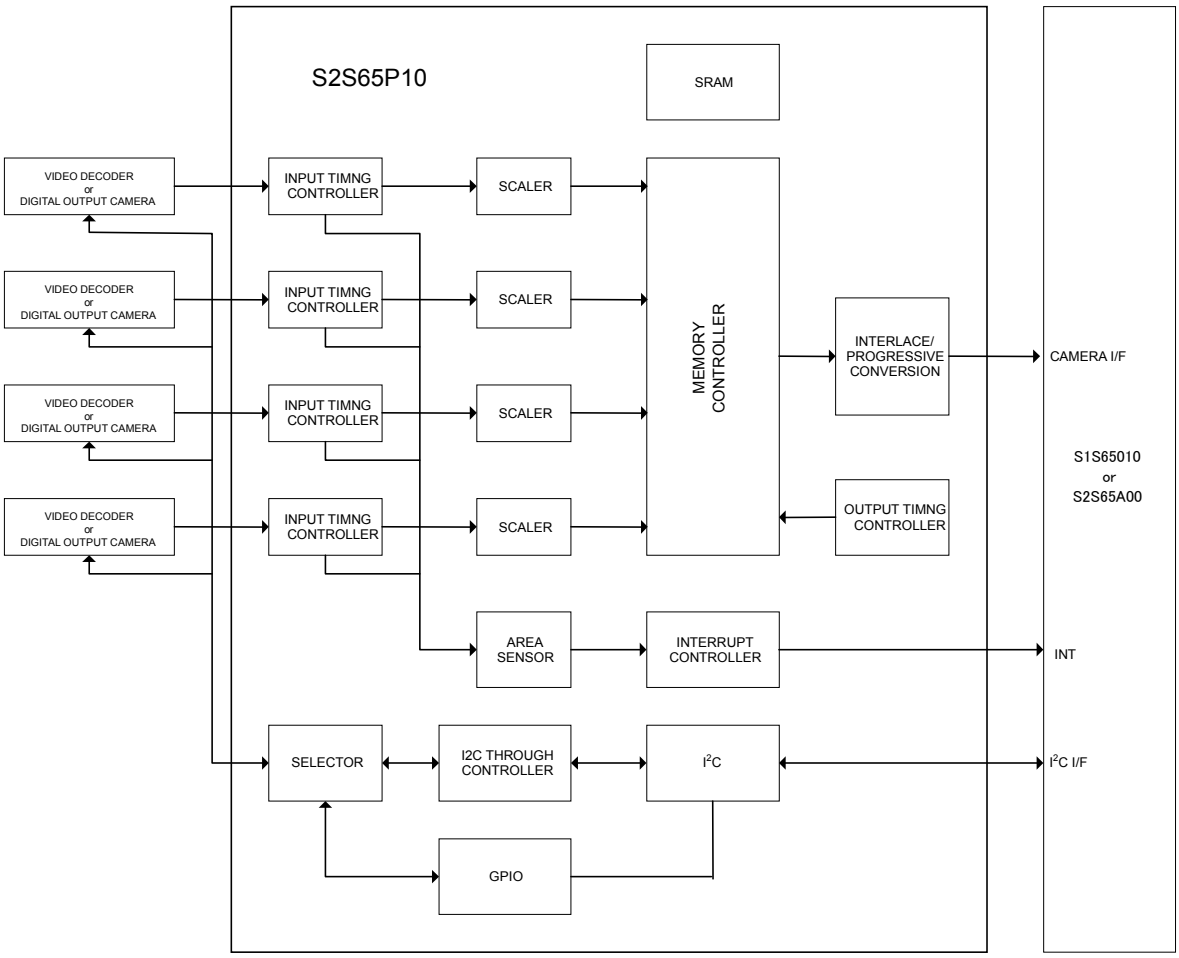


Fig.3.1 S2S65P10 Block Diagram

4. PIN LIST

4.1 Pin Assignment

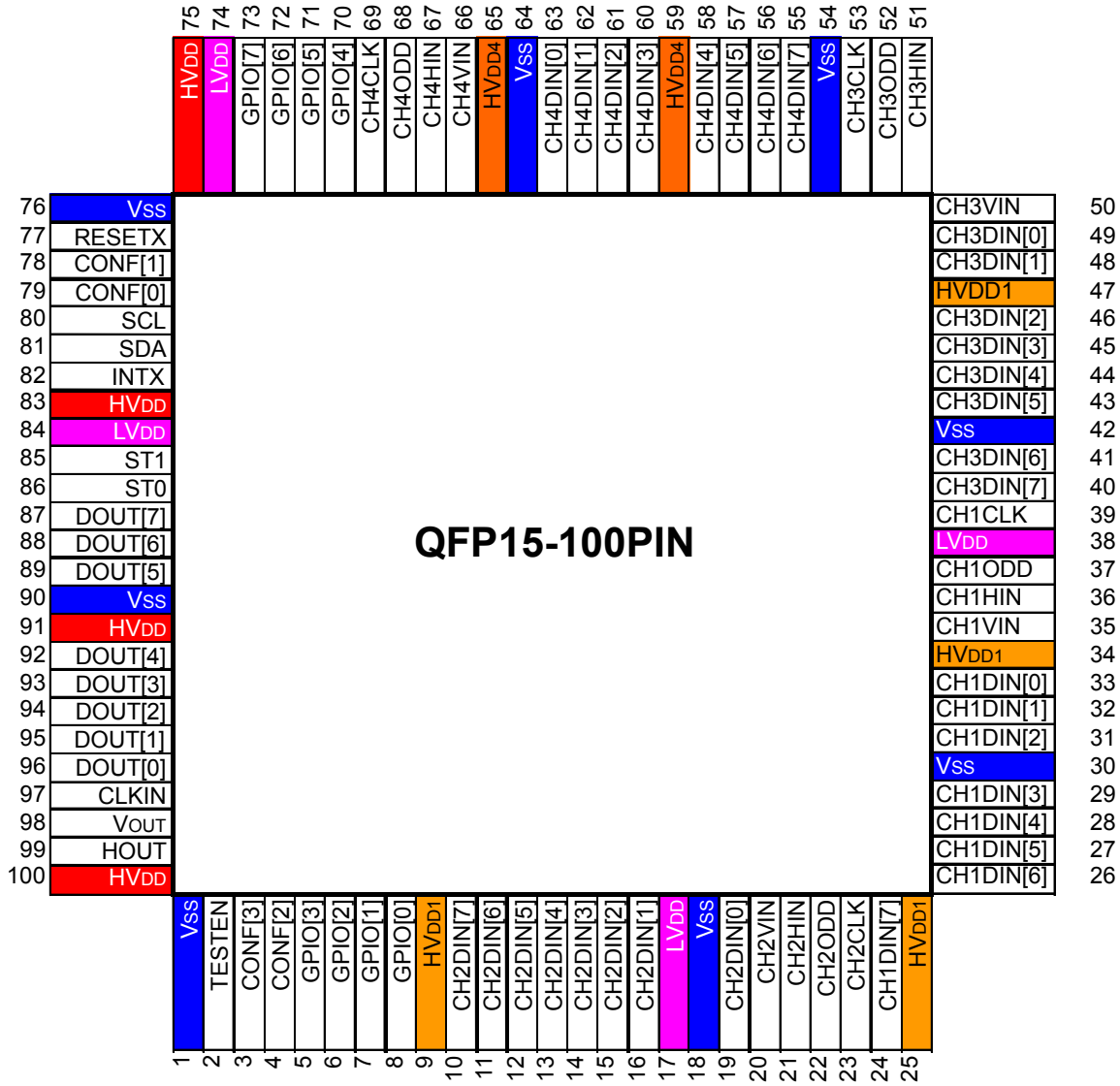


Fig.4.1 Top View

4.2 Pin Description

Reset / Clock Pins

Pin Name	Pin No.	Type	Input Level	Description
RESETX	77	I	LVCMOS SCHMITT	System Reset Input
CLKIN	97	I	LVCMOS	System Clock Input(from S1S65010,S2S65A00)

Video Interface Pins

Pin Name	Pin No.	Type	Input Level	Output Current	Description
CH1CLK	39	I	LVCMOS SCHMITT	2mA	Video1 Clock input
CH1VIN CH1VOUT	35	I/O	LVCMOS SCHMITT	2mA	Video1 Vertical Synchronization input/output
CH1HIN CH1HOUT	36	I	LVCMOS SCHMITT	2mA	Video1 Horizontal Synchronization input/output
CH1DIN[7:0] CH1DOUT[7:0]	33,32,31,29, 28,27,26,24	I/O	LVCMOS SCHMITT	2mA	Video1 Data input/output
CH1ODD	37	I	LVCMOS SCHMITT	2mA	Video1 Field Signal input
CH2CLK	23	I	LVCMOS SCHMITT	2mA	Video2 Clock input
CH2VIN CH2VOUT	20	I/O	LVCMOS SCHMITT	2mA	Video2 Vertical Synchronization input/output
CH2HIN CH2HOUT	21	I	LVCMOS SCHMITT	2mA	Video2 Horizontal Synchronization input/output
CH2DIN[7:0]	19,16,15,14, 13,12,11,10	I/O	LVCMOS SCHMITT	2mA	Video2 Data input/output
CH2ODD	22	I	LVCMOS SCHMITT	2mA	Video2 Field Signal input
CH3CLK	53	I	LVCMOS SCHMITT	2mA	Video3 Clock input
CH3VIN CH3VOUT	50	I/O	LVCMOS SCHMITT	2mA	Video3 Vertical Synchronization input/output
CH3HIN CH3HOUT	51	I/O	LVCMOS SCHMITT	2mA	Video3 Horizontal Synchronization input/output
CH3DIN[7:0] CH3DOUT[7:0]	49,48,46,45, 44,43,41,40	I/O	LVCMOS SCHMITT	2mA	Video3 Data input/output
CH3ODD	52	I	LVCMOS SCHMITT	2mA	Video3 Field Signal input
CH4DCLK	69	I	LVCMOS SCHMITT	2mA	Video4 Clock input
CH4VIN CH4VOUT	66	I/O	LVCMOS SCHMITT	2mA	Video4 Vertical Synchronization input/output
CH4HIN CH4HOUT	67	I/O	LVCMOS SCHMITT	2mA	Video4 Horizontal Synchronization input/output
CH4DIN[7:0] CH4DOUT[7:0]	63,62,61,60, 58,57,56,55	I/O	LVCMOS SCHMITT	2mA	Video4 Data input/output
CH4ODD	68	I	LVCMOS SCHMITT	2mA	Video4 Field Signal input
VOUT	98	O	—	2mA	Video Vertical Synchronization output
HOUT	99	O	—	2mA	Video4 Horizontal Synchronization output
DOUT[7:0]	96,95,94,93, 92,89,88,87	O	—	2mA	Video Data output

* Input and output are switched to each other by the setting of internal register with I^2C.

Host Interface

Pin Name	Pin No.	Type	Input Level	Output Current	Description
SDA	81	I/O	LVCMOS	2mA	I^2C Data I/O
SCL	80	I	LVCMOS	—	I^2C Clock
INTX	82	O	—	2mA	Interrupt Output
ST[1:0]	86,85	O	LVCMOS	2mA	Status Output

Miscellaneous

Pin Name	Pin No.	Type	Input Level	Output Current	Description
CONF[3:0]	79,78,4,3	I	LVCMOS SCHMITT	—	System configuration input Sets the functions which configure the system when it is booted.
GPIO0 TH_I^2C_SCL	8	I/O	LVCMOS SCHMITT	2mA	GPIO0 I^2C Through function SCL(Clock)
GPIO1 TH_I^2C_SDA	7	I/O	LVCMOS SCHMITT	2mA	GPIO1 I^2C Through function SDAL(Data)
GPIO2 TH_I^2C_SCL	6	I/O	LVCMOS SCHMITT	2mA	GPIO2 I^2C Through function SCL(Clock)
GPIO3 TH_I^2C_SDA	5	I/O	LVCMOS SCHMITT	2mA	GPIO3 I^2C Through function SDAL(Data)
GPIO4 TH_I^2C_SCL	70	I/O	LVCMOS SCHMITT	2mA	GPIO4 I^2C Through function SCL(Clock)
GPIO5 TH_I^2C_SDA	71	I/O	LVCMOS SCHMITT	2mA	GPIO5 I^2C Through function SDAL(Data)
GPIO6 TH_I^2C_SCL	72	I/O	LVCMOS SCHMITT	2mA	GPIO6 I^2C Through function SCL(Clock)
GPIO7 TH_I^2C_SDA	73	I/O	LVCMOS SCHMITT	2mA	GPIO7 I^2C Through function SDAL(Data)

* The GPIO functions are switched to each other by the setting of internal register with I^2C.

Test Pin

Pin Name	Pin No.	Type	Input Level	Output Current	Description
TESTEN	2	I	LVCMOS	—	Test pin for the IC; connect it to V_{SS}.

Power Pins

Pin Name	Pin No.	Type	Input Level	Output Current	Description
HV_{DD}	75,83, 91,100	P	—	—	I/O power supply (2.4V to 3.6V)
HV_{DD1}	9,25, 34,47	P	—	—	I/O power supply for video inputs 1 to 3 (2.4V to 3.6V)
HV_{DD4}	59,65	P	—	—	I/O power supply for video input 4 (2.4V to 3.6V)
LV_{DD}	17,38, 74,84	P	—	—	Power supply for internal logic (1.8V ± 0.15V)
V_{SS}	1,18,30, 42,54,64, 76,90	P	—	—	GND

5. REGISTER MAP

The register of S2S65P10 is accessed from the host CPU with I^2C. The I^2C slave address of S2S65P10 is "0x36" or "0x37". The selection of the slave address is set by CONF[3].

5.1 Register Table

Table 5.1 Memory MAP

Address	Description
0x0000 to 0x03FF	SYSTEM
0x0400 to 0x07FF	I^2C
0x0800 to 0x0BFF	Video Input Timing1
0x0C00 to 0x0FFF	Video Input Timing2
0x1000 to 0x13FF	Video Input Timing3
0x1400 to 0x17FF	Video Input Timing4
0x1800 to 0x1BFF	Video Out Timing
0x1C00 to 0x1FFF	Area Sensor
0x2000 to 0x23FF	Reserved
0x2400 to 0x27FF	Reserved
0x2800 to 0x2BFF	Reserved
0x2C00 to 0x2FFF	Reserved
0x3000 to 0x33FF	Interlace/Progressive Converter
0x3400 to 0x37FF	Reserved
0x3800 to 0x3BFF	Interrupt Controller
0x3C00 to 0x3FFF	GPIO

6. FUNCTION DESCRIPTION

6.1 I/P Conversion (Interlace/Progressive Conversion)

S2S65P10 has following three modes for this function. They are set by I^2C.

- Weave Mode
  Synthesizes two consecutive fields to build one frame.

- Bob Mode
  Doubles each line in either one field to build one frame.

- Interpolation Mode
  Interpolates linearly two consecutive horizontal lines in either one field to build one frame.

6.2 Intelligent Auto Image Switching

S2S65P10 has following four modes for this function. They are set by I^2C.

- Fixed Mode
  Outputs one input channel preset.

Fig.6.1 Fixed Mode

- Auto Scan Mode
  Outputs input channels one by one switching them in turn.

Fig.6.2 Auto Scan Mode

- Compress Mode
  Outputs images resized into QVGA.

Fig.6.3 Compress Mode

- Merge Mode
  Outputs images in each channel resized into QVGA and synthesizing four screens into one.

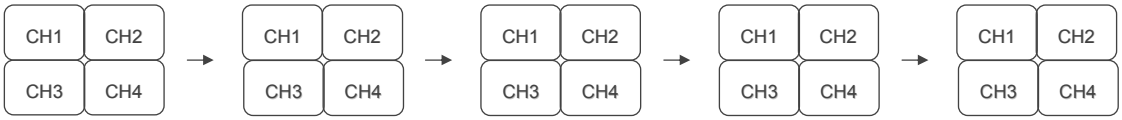


Fig.6.4 Merge Mode

<Frame rate>

Video output synchronizes with each video input; therefore, the frame rate may reduce when switching video input. The table below lists the minimum and maximum values of the frame rate in each video output mode.

Table 6.1 Output Frame Rate (when VGA is input at 30fps)

Unit: fps

Mode		Min.	Max.
Fixed Mode	Interlace	—	30
	Progressive	—	30
Auto Scan Mode	Interlace	15	30
	Progressive	15	30
Compress Mode (QVGA output)	Interlace	60	120
	Progressive	30	60
Merge Mode	Interlace	15	30
	Progressive	—	15

6.3 Conversion of Aspect Ratio

S2S65P10 has the following modes for this function. They are set by I^2C.

- VGA Conversion

Video Input	Pixel Aspect Ratio	Number of pixels		After Conversion
NTSC	10:11	704:480	--→	640:480
	8:9	720:480	--→	640:480
PAL	16:15	720:576	--→	768:576
VGA	1:1	640:480	--→	640:480

Fig.6.5 VGA Conversion

- QVGA Conversion

Video Input	Pixel Aspect Ratio	Number of pixels		After Conversion
NTSC	10:11	704:480	--→	320:240
	8:9	720:480	--→	320:240
PAL	16:15	720:576	--→	384:288
VGA	1:1	640:480	--→	320:240

* In the case of NTSC/PAL, only either one field is converted.
* In the case of VGA (Progressive), the conversion in the vertical direction is carried out by thinning the scan operation.

Fig.6.6 QVGA Conversion

6.4 Area Sensor

The area sensor divides a screen from any channel into 48 rectangle areas, and gets difference between two consecutive frames for each rectangle area. It outputs an interrupt signal if the difference is greater than a threshold preset.

- The data of the difference between frames is selectable from the YUV components.
- The interruption factor can be set for each area.
- The setting can be made from I^2C.

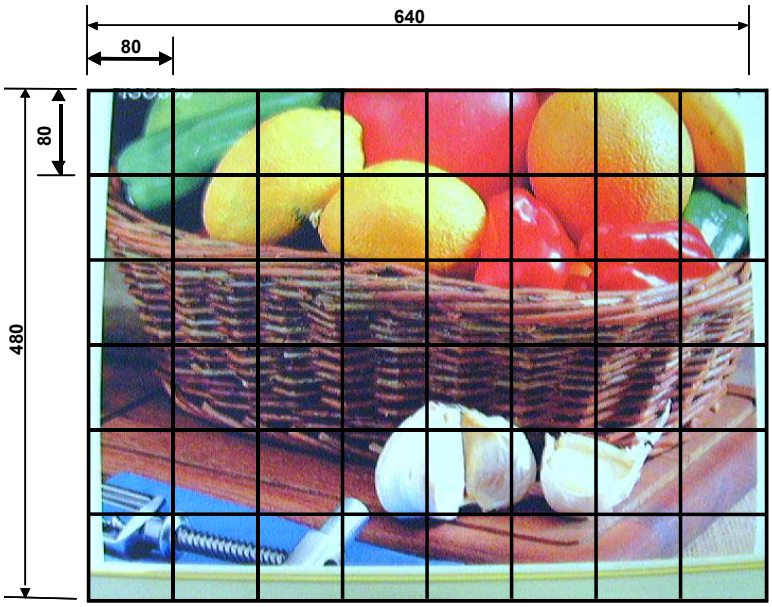


Fig.6.7 Division into Areas

6.5 GPIO/I²C Through Function

The GPIO [7:0] pin has two functions: it can work as the general-purpose I/O port, and it can pass through the I²C signals sent from the host CPU. Using the latter function makes it possible to control a device having the same I²C device address from the host CPU.

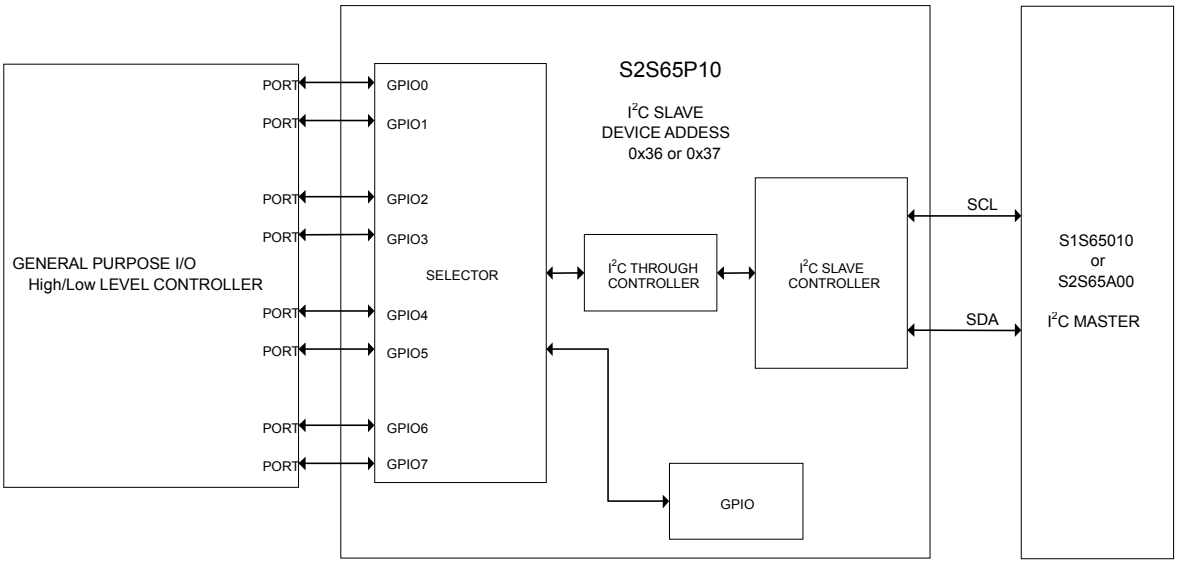


Fig.6.8 GPIO Function

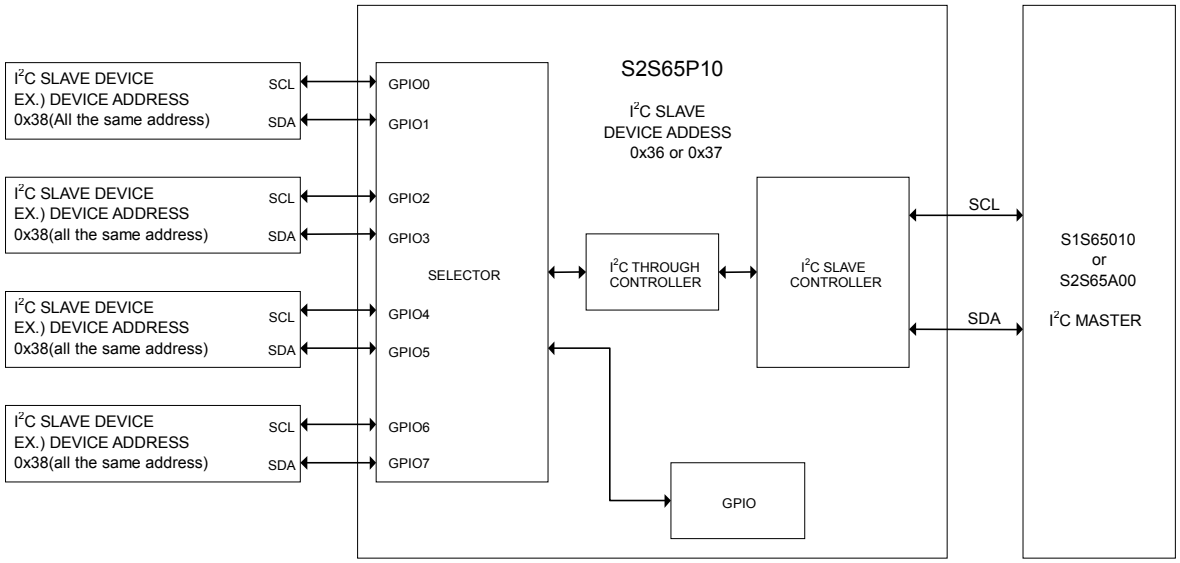


Fig.6.9 I²C Through Function

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

Table 7.1 Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit
Supply voltage	HV_{DD}*1	V_{SS}, LVDS_V_{SS}-0.3 to 4.0	V
	HV_{DD1}*1	V_{SS}, LVDS_V_{SS} -0.3 to 4.0	V
	HV_{DD4}*1	V_{SS}, LVDS_V_{SS} -0.3 to 4.0	V
	LV_{DD}*1	V_{SS}, LVDS_VSS -0.3 to 2.5	V
Input voltage	HV_I	V_{SS}-0.3 to HV_{DD}, HV_{DD1}, HV_{DD4}+0.5	V
	LV_I	V_{SS}-0.3 to LV_{DD}+0.5	V
Output voltage	HV_O	V_{SS}-0.3 to HV_{DD}, HV_{DD1}, HV_{DD3}+0.5	V
	LV_O	V_{SS}-0.3 to LV_{DD}+0.5*2	V
Output current/pin	I_{OUT}	±10	mA
Storage temperature	T_{stg}	-65 to +150	°C

(Note) *1 : HV_{DD}, HV_{DD1}, HV_{DD4} ≥ LV_{DD}

7.2 Recommended Operating Conditions

Table 7.2 Recommended Operating Conditions

(2 Power supply HV_{DD}, HV_{DD1}, HV_{DD4}/LV_{DD}=3.3/1.8V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (High)	HV_{DD}	2.40	3.30	3.60	V
Power supply voltage (High: Video input 1, 2, 3)	HV_{DD1}	2.40	3.30	3.60	V
Power supply voltage (High: Video input 4)	HV_{DD4}	2.40	3.30	3.60	V
Power supply voltage (Low)	LV_{DD}	1.65	1.80	1.95	V
Input voltage	HV_I	V_{SS}	—	HV_{DD} HV_{DD1} HV_{DD4}	V
	LV_I	V_{SS}	—	LV_{DD}	V
Ambient temperature	T_a	-40	25	105*1	°C
		—	—	—	°C

(Note) *1 This ambient temperature range represents a recommended one assuming T_j = -40 to +105°C.

7.3 DC Characteristics

Table 7.3 DC Characteristics

(Under the recommended operating conditions)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static power consumption (static current between HV_{DD} and V_{SS})						
Static power consumption	I_{DDSH1}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	—	16	μA
Static power consumption (static current between HV_{DD1} and V_{SS})						
Static power consumption	I_{DDSH2}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	—	18	μA
Static power consumption (static current between HV_{DD4} and V_{SS})						
Static power consumption	I_{DDSH3}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	—	6	μA

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static current (static current between LV_{DD} and V_{SS})						
Static power consumption	I_{DDSL}	V_{IN}=HV_{DD} or HV_{DD1} or HV_{DD4} or LV_{DD} or V_{SS} HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. I_{OH}=I_{OL}=0 When T_a(Max.)=105(°C), T_a=T_j=105(°C)	—	70	900	μA
Power consumption (current consumption between LV_{DD} and V_{SS})						
Operational power consumption	I_{DDL}	HV_{DD}=3.3V HV_{DD1}=3.3V HV_{DD4}=3.3V LV_{DD}=1.8V T_a=-40 to +105°C CHxCLK=27MHz(x=1, 2, 3, 4) CLKIN=25MHz	—	25	40	mA
Input leak						
Input leak current	I_L	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. HV_{IH}=HV_{DD}, HV_{DD1}, HV_{DD4} LV_{IH}=LV_{DD} V_{IL}=V_{SS}	-5	—	5	μA
Input characteristics (H-type LVCMOS) CLKIN, SDA, SDC						
HIGH level input voltage	V_{IH1H}	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max.	2.2	—	—	V
LOW level input voltage	V_{IL1H}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min.	—	—	0.8	V
Input characteristics (L-type LVCMOS) TESTEN						
HIGH level input voltage	V_{IH1L}	LV_{DD}=Max.	1.27	—	—	V
LOW level input voltage	V_{IL1L}	LV_{DD}=Min.	—	—	0.57	V

7. ELECTRICAL CHARACTERISTICS

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Schmitt input characteristics (H-type LVCMOS) RESETX, CHxCLK< CHxVIN, CHxHIN, CHxDIN[7:0], CHxODD, GPIO[7:0], CONF[3:0] (x=1, 2, 3, 4)						
HIGH level trigger voltage	V_{T1+}	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max.	1.4	—	2.7	V
Low level trigger voltage	V_{T1-}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD2}=Min. LV_{DD}=Min.	0.6	—	1.8	V
Hysteresis voltage	ΔV	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min. LV_{DD}=Min.	0.3	—	—	V
Input characteristics GPIO[7:0]						
Pull-up resistor	RPLU1H	V_I=V_{SS}	25	50	120	kΩ
Input characteristics CHxCLK< CHxVIN, CHxHIN, CHxDIN[7:0], CHxODD, CONF[3:0] (x=1, 2, 3, 4)						
Pull-down resistance	RPLD1H	V_I=HV_{DD}, HV_{DD1}, HV_{DD4}	25	50	120	kΩ
Output characteristics CHxVIN, CHxHIN, CHxDIN[7:0], V_{OUT}, H_{OUT}, D_{OUT}[7:0], SDA, INTX, ST[1:0] (x=1, 2, 3, 4)						
HIGH level output voltage	V_{OH1H}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min. I_{OH}=-2mA	HV_{DD}-0.4 HV_{DD1}-0.4 HV_{DD4}-0.4	—	—	V
LOW level output voltage	V_{OL1H}	HV_{DD}=Min. HV_{DD1}=Min. HV_{DD4}=Min. I_{OL}=2mA	—	—	V_{SS}+0.4	V
Output characteristics CHxVIN, CHxHIN, CHxDIN[7:0], GPIO[7:0] (x=1, 2, 3, 4)						
OFF-STATE leak current	I_{OZ}	HV_{DD}=Max. HV_{DD1}=Max. HV_{DD4}=Max. LV_{DD}=Max. HV_{OH}=HV_{DD}, HV_{DD1}, HV_{DD4} LV_{OH}=LV_{DD} V_{OL}=V_{SS}	-5	—	5	μA

7.4 AC Characteristics

7.4.1 Video Input Interface

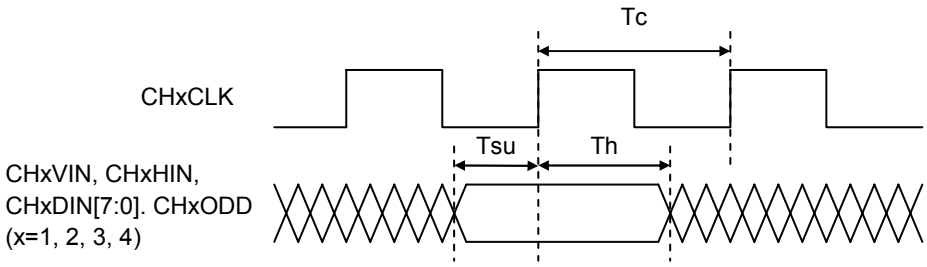


Fig.7.1 Video Input Timing Chart

Table 7.4 Video input

Top= -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD}=1.65 to 1.95 V , V_{SS} = 0 V, CL=30pF (output)

Item	Symbol	Min.	Typ.	Max.	Unit
Video input clock frequency	Tf	—	27	28.5	MHz
Video input clock cycle time	Tc	35	37	—	ns
Data setup time	Tsu	10	—	—	ns
Data hold time	Th	10	—	—	ns

7.4.2 Video Output Interface

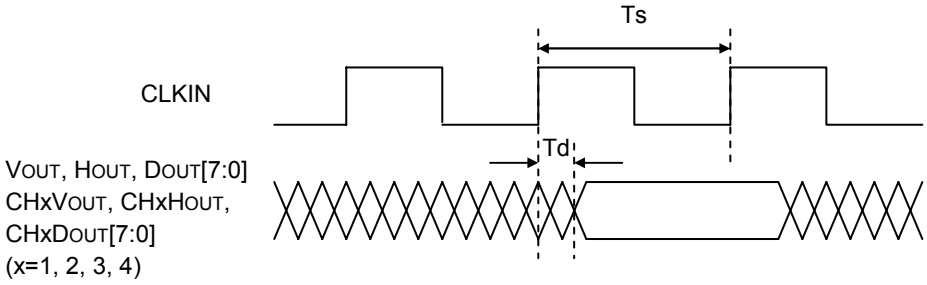


Fig.7.2 Video Output Timing Chart

Table 7.5 Video Timing

Top= -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD}=1.65 to 1.95 V , V_{SS} = 0 V, CL=30pF (output)

Item	Symbol	Min.	Typ.	Max.	Unit
CLKIN clock frequency	fc	20	25	28.5	MHz
CLKIN clock cycle time	Ts	35	40	50	ns
Data output delay time	Td	5	—	20	ns

7.4.3 I²C Interface

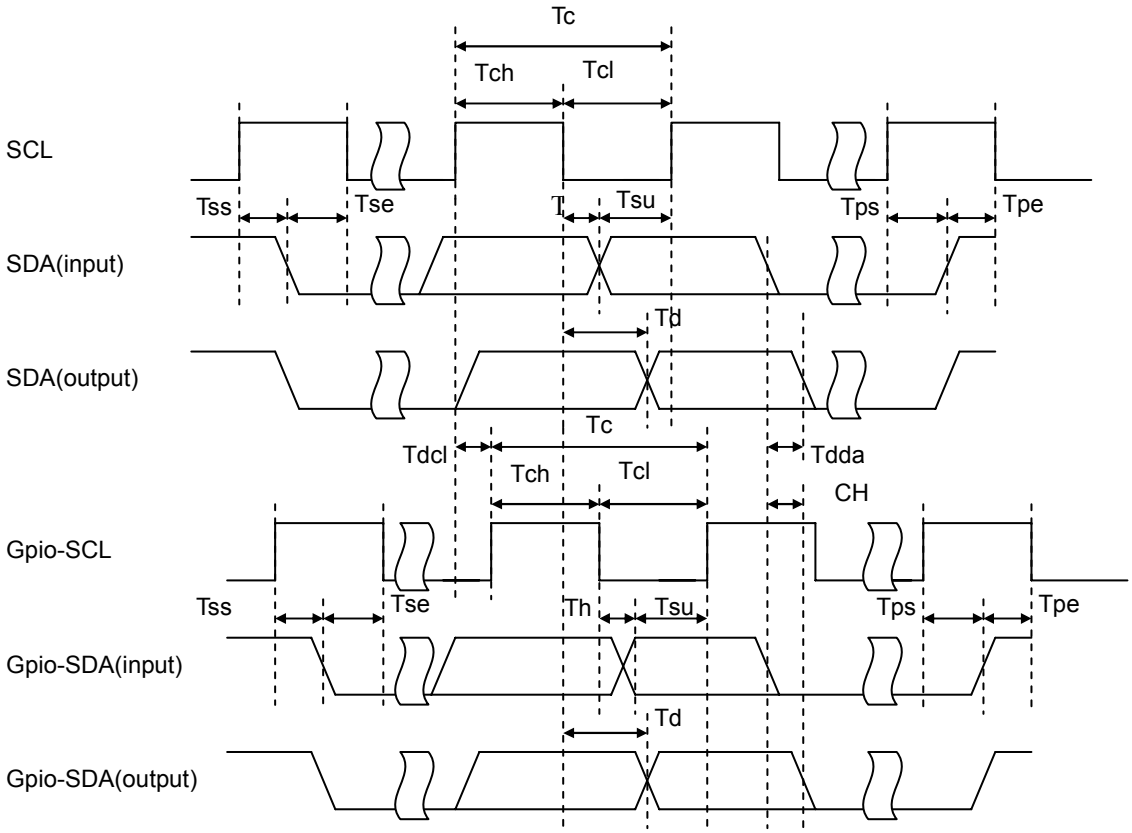


Fig.7.3 I²C Interface Timing Chart

Table 7.6 I²C Interface

Top= -40 to +105 °C, HV_{DD}, HV_{DD1}, HV_{DD4} = 2.4 to 3.6 V, LV_{DD} = 1.65 to 1.95 V, V_{SS} = 0 V, CL=30pF (output)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fc	—	—	$10^9/(Tc^* Ts)$ *1,4	Hz
SCL clock cycle time	Tc	25 *3,4	—	—	Ts*1
SCL clock pulse width (High)	Tch	10	—	—	Ts*1
SCL clock pulse width (Low)	Tcl	15 *3,4	—	—	Ts*1
SDA input setup time	Tsu	0	—	—	ns
SDA input hold time	Th	0	—	—	ns
SDA output delay time	Td	10	—	*2,3	Ts*1
START condition start time	Tss	5	—	—	Ts*1
START condition end time	Tse	5	—	—	Ts*1
STOP condition start time	Tps	5	—	—	Ts*1
STOP condition end time	Tpe	5	—	—	Ts*1

SCL to Gpio-SCL delay time	Tdcl	5	—	6 *3	Ts*1
SDA(input) to Gpio-SDA(output) delay time Gpio-SDA(input) to SDA(output) delay time	Tdda	5	—	6 *3	Ts*1

*1 Ts: CLKIN clock cycle time (Example: Ts=40ns if f=25MHz)
*2 This numeric value can be adjusted up to 4µs depending on the set value of I2C HOLD COUNTER [041Ch].
*3 This numeric value is set, assuming that the rising time of the external bus is within 1Ts (40ns if f=25MHz). Note that this numeric value increases if the rising time of the external bus exceeds 1Ts depending on the load capacity and pull-up resistance value.
Reference) At f=25MHz, the numeric value will increase approximately +10Ts when the rising time is 400ns and approximately +25Ts when it is +25Ts.
*4 This numeric value is set, assuming that the set value of I2C HOLD COUNTER [041Ch] is set to 0. Note that this numeric value increases (the clock frequency decreases) as the output delay time increases depending on the set value of I2C HOLD COUNTER.
Reference) At f=25MHz, the numeric value will increase approximately +10Ts when the set value of I2C HOLD COUNTER is 0Ah (approximately 400ns).

7.4.4 Reset

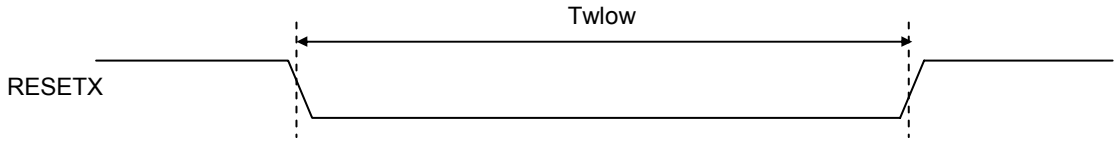


Fig.7.4 Reset Timing Chart

Table 7.7 Reset

Top= -40 to +105 °C, HV_{DD},HV_{DD1},HV_{DD4} = 2.4 to 3.6 V, LV_{DD}=1.65 to 1.95 V , V_{SS} = 0 V, CL=30pF (output)

Item	Symbol	Min.	Typ.	Max.	Unit
Reset pulse width	Twlow	100	—	—	ns

8. APPLICATION DIAGRAM

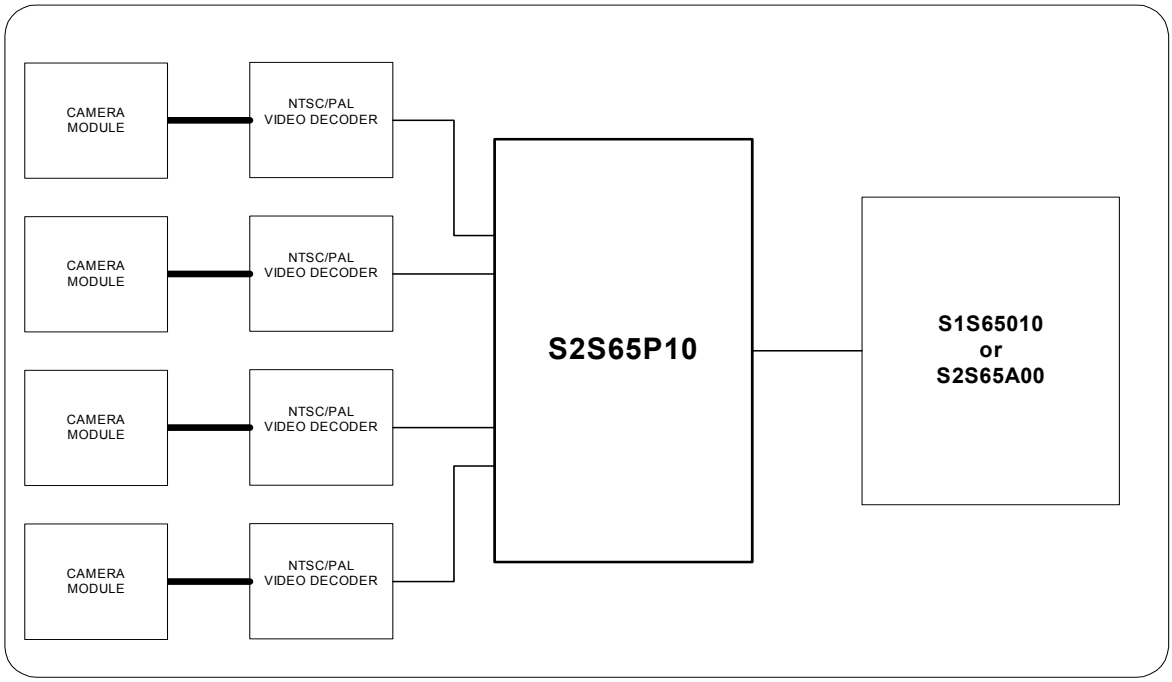


Fig.8.1 System Example 1

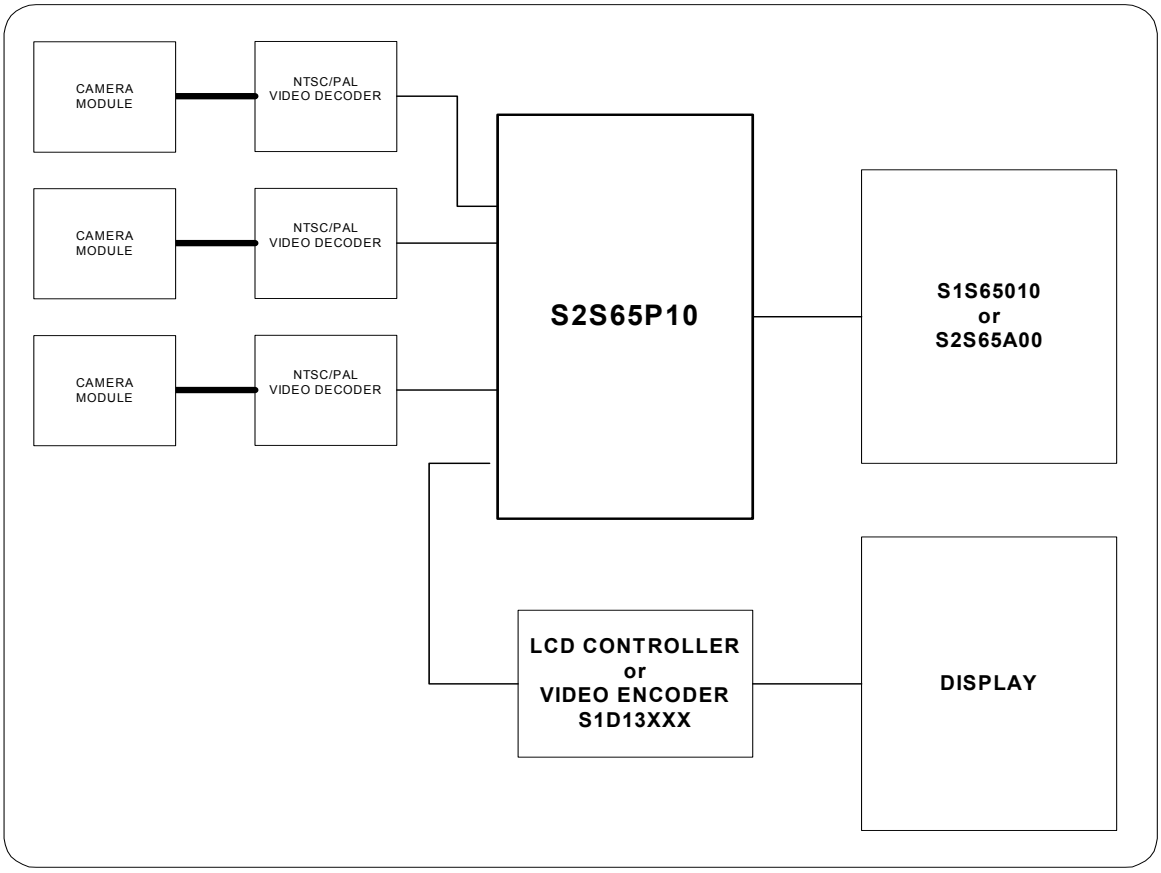
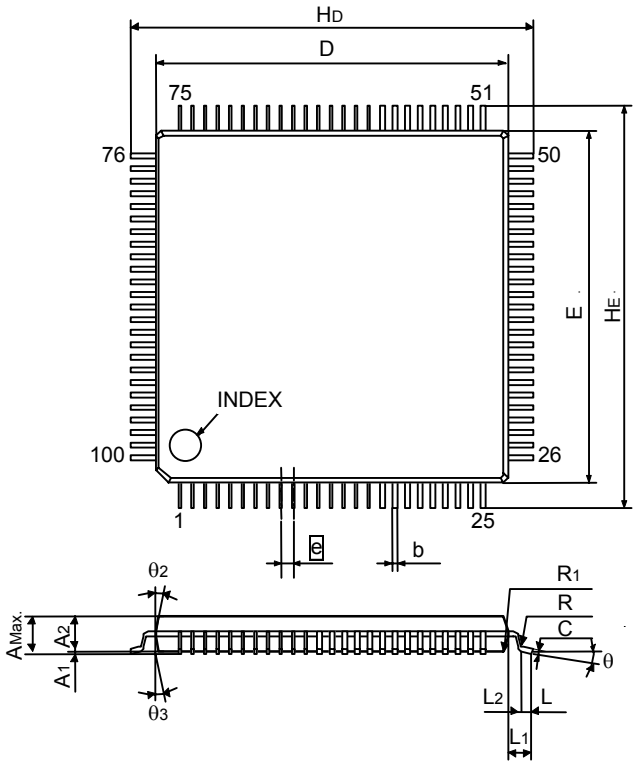


Fig.8.2 System Example 2

9. MECHANICAL DIMENSIONS

* Subject to change without notice for improvement.



Symbol	Dimension in Milimeters		
	Min.	Nom.	Max.
E	13.9	14	14.1
D	13.9	14	14.1
A			1.7
A_1		0.1	
A_2	1.3	1.4	1.5
e		0.5	
b	0.13	0.18	0.28
C	0.1	0.125	0.175
θ	0°		10°
L	0.3	0.5	0.7
L_1		1	
L_2		0.5	
H_E	15.7	16	16.3
H_D	15.7	16	16.3
$θ_2$		12°	
$θ_3$		12°	
R		0.2	
R_1		0.2	

Fig.9.1 QFP15-100pin PACKAGE

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