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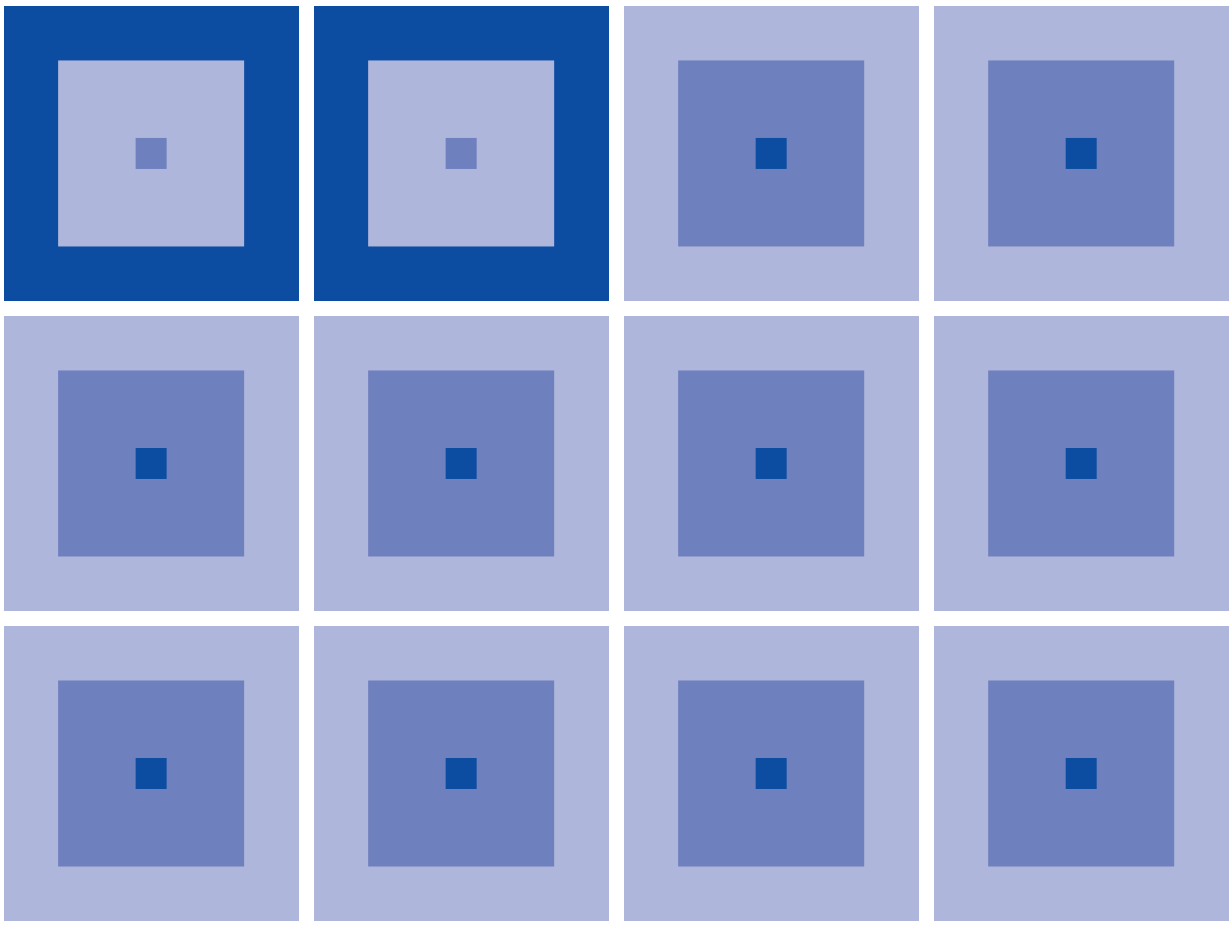
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C63709

Technical Manual



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NOTICE

Configuration of product number

Devices

S1 C 63158 F 0A01 00

Packing specifications
- 00 : Besides tape & reel
- 0A : TCP BL 2 directions
- 0B : Tape & reel BACK
- 0C : TCP BR 2 directions
- 0D : TCP BT 2 directions
- 0E : TCP BD 2 directions
- 0F : Tape & reel FRONT
- 0G : TCP BT 4 directions
- 0H : TCP BD 4 directions
- 0J : TCP SL 2 directions
- 0K : TCP SR 2 directions
- 0L : Tape & reel LEFT
- 0M : TCP ST 2 directions
- 0N : TCP SD 2 directions
- 0P : TCP ST 4 directions
- 0Q : TCP SD 4 directions
- 0R : Tape & reel RIGHT
- 99 : Specs not fixed

Specification

Package
[D: die form; F: QFP, B: BGA]

Model number

Model name
[C: microcomputer, digital products]

Product classification
[S1: semiconductor]

Development tools

S5U1 C 63000 A1 1 00

Packing specifications
[00: standard packing]

Version
[1: Version 1]

Tool type
- Hx : ICE
- Ex : EVA board
- Px : Peripheral board
- Wx : Flash ROM writer for the microcomputer
- Xx : ROM writer peripheral board
- Cx : C compiler package
- Ax : Assembler package
- Dx : Utility tool by the model
- Qx : Soft simulator

Corresponding model number
[63000: common to S1C63 Family]

Tool classification
[C: microcomputer use]

Product classification
[S5U1: development tool for semiconductor products]

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CHAPTER 1 OUTLINE

The S1C63709 is a microcomputer which consists of a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (12,288 words × 13 bits), RAM (2,048 words × 4 bits), serial interface, 2-channel motor driver, solar charging circuit, an LCD driver that can drive a maximum 64 segments × 8 commons, sound generator and time base counters. The S1C63709 features low current consumption, this makes it suitable for solar-powered radio-controlled watches.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit
OSC3 oscillation circuit	4 MHz (Typ.) ceramic, 1.1 MHz (Typ.) CR (external R) or 200 kHz (Typ.) CR (built-in R) oscillation circuit (∗1)
Instruction set	Basic instruction: 47 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec
ROM capacity	Code ROM: 12,288 words × 13 bits Data ROM: 2,048 words × 4 bits
RAM capacity	Data memory: 2,048 words × 4 bits Display memory: 160 words × 4 bits
Input port	4 bits for general-purpose input ports 4 bits for crown switches 5 bits for theoretical regulation (pull-down resistors may be supplemented ∗1)
I/O port	18 bits (usable as special output and serial I/F ports ∗2)
Serial interface	1 port (8-bit clock synchronous system)
LCD driver	64 segments × 4, 5 or 8 commons (∗2)
Time base counter	Clock timer Stopwatch timer (1/1000 sec, with direct key input function)
Programmable timer	8 bits × 3 ch. or 16 bits × 1 ch. + 8 bits × 1 ch. (∗2)
Watchdog timer	Built-in
Sound generator	With envelope and 1-shot output functions
Motor driver	2 channels
Solar charge-control circuit	Built in
Supply voltage detection (SVD) circuit	24 detection voltage values are configurable (∗2)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 7 systems Stopwatch timer interrupt: 4 systems Programmable timer interrupt: 3 systems Serial interface interrupt: 1 system Motor driver interrupt: 2 systems Solar interrupt: 1 system
Power supply voltage	1.0 to 3.6 V (when CR (built-in R) oscillation circuit is selected) 2.1 to 3.6 V (when CR (external R) or ceramic oscillation circuit is selected)
Operating temperature range	-20 to 70°C
Current consumption (Typ.)	32 kHz HALT state (3.0 V, LCD off) 0.15 µA 32 kHz run state (3.0 V, LCD on) 3.50 µA
Shipping form	QFP20-144pin (plastic) or chip

∗1: Can be selected with mask option ∗2: Can be selected with software

1.2 Block Diagram

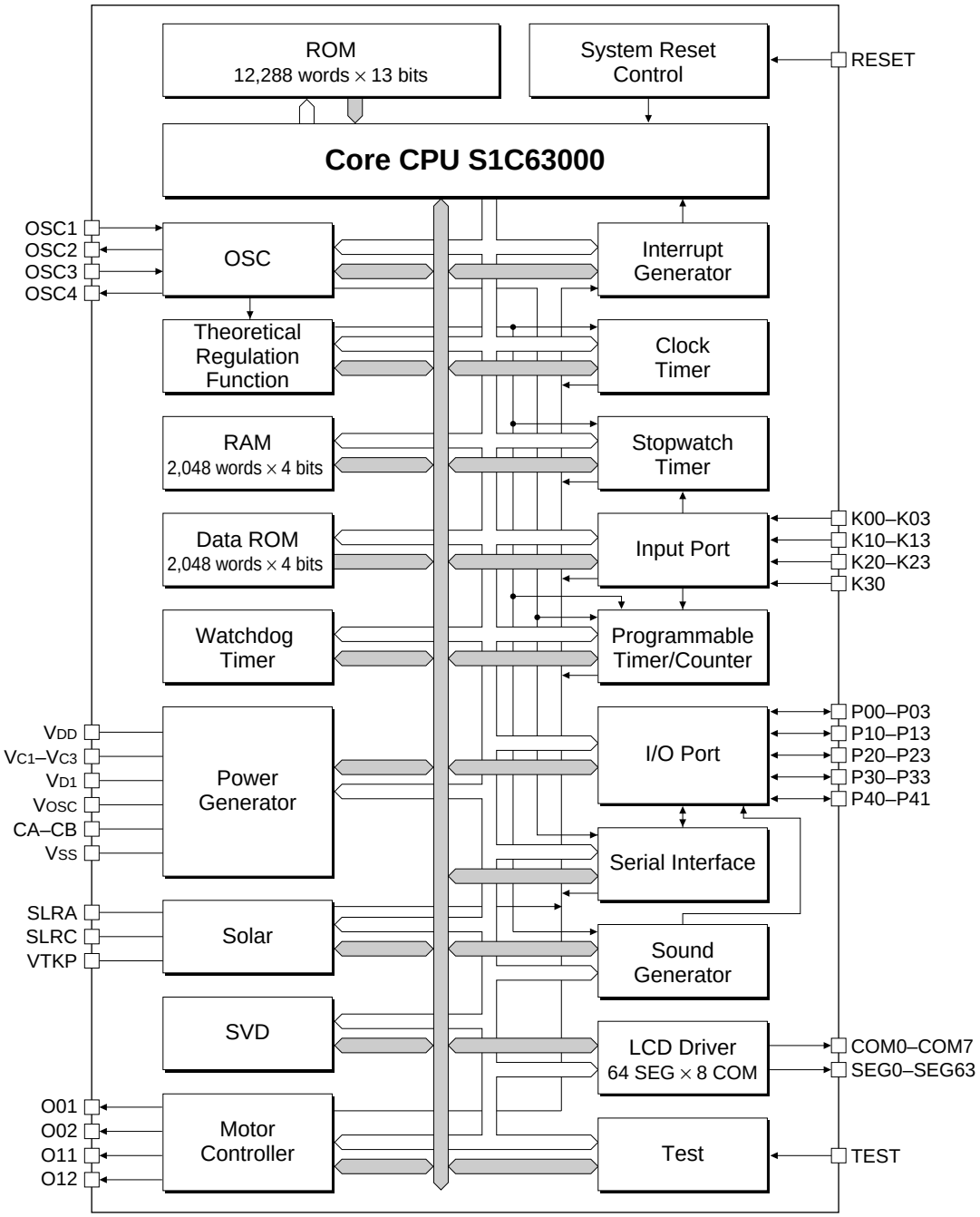
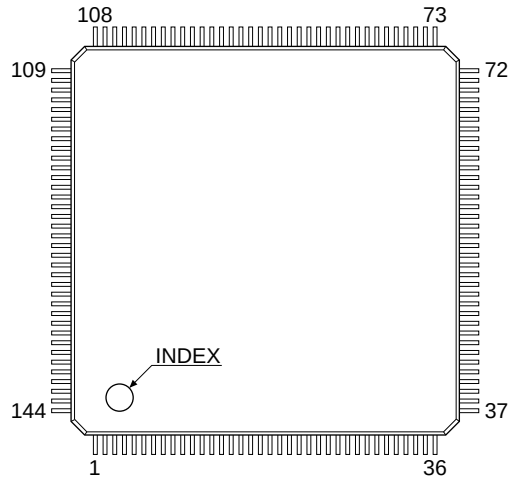


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP20-144pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	37	COM0	73	N.C.	109	N.C.
2	N.C.	38	COM1	74	N.C.	110	N.C.
3	SEG0	39	COM2	75	SEG32	111	COM4
4	SEG1	40	COM3	76	SEG33	112	COM5
5	SEG2	41	CA	77	SEG34	113	COM6
6	SEG3	42	CB	78	SEG35	114	COM7
7	SEG4	43	V_{C1}	79	SEG36	115	P41
8	SEG5	44	V_{C2}	80	SEG37	116	P40
9	SEG6	45	V_{C3}	81	SEG38	117	P33
10	SEG7	46	V_{DD}	82	SEG39	118	P32
11	SEG8	47	V_{OSC}	83	SEG40	119	P31
12	SEG9	48	N.C.	84	SEG41	120	P30
13	SEG10	49	OSC1	85	SEG42	121	P23
14	SEG11	50	OSC2	86	SEG43	122	P22
15	SEG12	51	N.C.	87	SEG44	123	P21
16	SEG13	52	V_{D1}	88	SEG45	124	P20
17	SEG14	53	OSC3	89	SEG46	125	V_{DD}
18	SEG15	54	OSC4	90	SEG47	126	SLRA
19	SEG16	55	N.C.	91	SEG48	127	VTKP
20	SEG17	56	V_{SS}	92	SEG49	128	SLRC
21	SEG18	57	TEST	93	SEG50	129	V_{SS}
22	SEG19	58	RESET	94	SEG51	130	V_{DD}
23	SEG20	59	K00	95	SEG52	131	O01
24	SEG21	60	K01	96	SEG53	132	N.C.
25	SEG22	61	K02	97	SEG54	133	O02
26	SEG23	62	K03	98	SEG55	134	O11
27	SEG24	63	K10	99	SEG56	135	O12
28	SEG25	64	K11	100	SEG57	136	V_{SS}
29	SEG26	65	K12	101	SEG58	137	P13
30	SEG27	66	K13	102	SEG59	138	P12
31	SEG28	67	K20	103	SEG60	139	P11
32	SEG29	68	K21	104	SEG61	140	P10
33	SEG30	69	K22	105	SEG62	141	P03
34	SEG31	70	K23	106	SEG63	142	P02
35	N.C.	71	K30	107	N.C.	143	P01
36	N.C.	72	N.C.	108	N.C.	144	P00

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram (QFP20-144pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function
V_{DD}	46, 125, 130	–	Power (+) supply pin
V_{SS}	56, 129, 136	–	Power (–) supply pin
V_{D1}	52	–	Internal logic system regulated voltage output pin
V_{OSC}	47	–	OSC1 oscillation system regulated voltage output pin
V_{C1}–V_{C3}	43–45	–	LCD system power supply pins
CA, CB	41, 42	–	LCD system voltage boosting/halving capacitor connecting pins
OSC1	49	I	Crystal oscillation input pin
OSC2	50	O	Crystal oscillation output pin
OSC3	53	I	Ceramic or CR oscillation input pin (selectable by mask option)
OSC4	54	O	Ceramic or CR oscillation output pin (selectable by mask option)
K00–K03	59–62	I	Input port pins
K10–K13	63–66	I	Input port pins
K20–K23	67–70	I	Input port pins
K30	71	I	Input port pin
P00–P03	144–141	I/O	I/O port pins
P10/SIN	140	I/O	I/O port or serial I/F data input pin (selected by software)
P11/SOUT	139	I/O	I/O port or serial I/F data output pin (selected by software)
P12/SCLK	138	I/O	I/O port or serial I/F clock I/O pin (selected by software)
P13/SRDY	137	I/O	I/O port or serial I/F ready signal output pin (selected by software)
P20/TOUT	124	I/O	I/O port or TOUT clock output pin (selected by software)
P21/SVDDT	123	I/O	I/O port or SVDDT signal monitor output pin (selected by software)
P22/VCWON	122	I/O	I/O port or VCWON signal monitor output pin (selected by software)
P23/ISOR1	121	I/O	I/O port or ISOR1 signal monitor output pin (selected by software)
P30/ISOR3	120	I/O	I/O port or ISOR3 signal monitor output pin (selected by software)
P31/ISOR2	119	I/O	I/O port or ISOR2 signal monitor output pin (selected by software)
P32/CLIM	118	I/O	I/O port or CLIM signal monitor output pin (selected by software)
P33/F16HZ	117	I/O	I/O port or 16 Hz clock output pin (selected by software)
P40/BZ	116	I/O	I/O port or buzzer output pin (selected by software)
P41/FOUT	115	I/O	I/O port or FOUT clock output pin (selected by software)
COM0–COM7	37–40, 111–114	O	LCD common output pins (1/4, 1/5 or 1/8 duty is selectable by software)
SEG0–SEG63	3–34, 75–106	O	LCD segment output pins
O01, O02	131, 133	O	Motor 0 drive pulse output pins
O11, O12	134, 135	O	Motor 1 drive pulse output pins
SLRA	126	–	Solar cell anode connecting pin
SLRC	128	–	Solar cell cathode connecting pin
VTKP	127	–	Solar voltage detection pin
RESET	58	I	Initial reset input pin
TEST	57	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the S1C63709. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog and segment option generator winsog, that have been prepared as the development software tool of S1C63709, is used for this selection. Mask pattern of the IC is finally generated based on the data created by winfog and winsog. Refer to the "S5U1C63000A Manual" for winfog and winsog.

<Outline of the mask option>

(1) OSC3 oscillation circuit

The OSC3 oscillator type can be selected from ceramic oscillation, CR oscillation (external R), and CR oscillation (built-in R). Refer to Section 4.3.3, "OSC3 oscillation circuit", for details.

(2) Input port pull-down resistor

This mask option is used to select whether the pull-down resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports.
Refer to Section 4.4.2, "Mask option", for details.

(3) Reset port pull-down resistor

This mask option is used to select whether the pull-down resistor is supplemented to the reset port or not.
Refer to Section 2.2.1, "Reset terminal (RESET)", for details.

(4) I/O port pull-down resistor

This mask option is used to select whether the pull-down resistor working in the input mode is supplemented to the I/O ports or not. It is possible to select for each bit of the input ports.
Refer to Section 4.5.2, "Mask option", for details.

(5) Output specification of the I/O port

For the output specification when the I/O ports are in the output mode, either complementary output or P-channel open drain output can be selected in 1-bit units.
Refer to Section 4.5.2, "Mask option", for details.

(6) External reset by simultaneous high input to the input port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected.
Refer to Section 2.2.2, "Simultaneous high input to terminals K00–K03", for details.

(7) Synchronous clock polarity in the serial interface

The polarity of the synchronous clock SCLK and the SRDY signal in slave mode of the serial interface is selected by mask option. Either positive polarity or negative polarity can be selected.
Refer to Section 4.10.2, "Mask option", for details.

(8) Motor control

Whether K13 input port is used for controlling motor 0 or not can be selected.
Refer to Section 4.12, "Motor Control Circuit", for details.

(9) Use or no use of solar

Whether the solar control functions are used or not can be selected.
Refer to Section 4.16, "Solar Function", for details.

(10) Input port noise reject circuit (K12 and K13)

Whether the K12 and K13 noise reject circuits are used or not can be selected individually.
Refer to Section 4.4.2, "Mask option", for details.

(11) f_{OSC1} regulation type

Either theoretical regulation or C_G regulation can be selected to adjust the OSC1 oscillation frequency.
Refer to Section 4.3.2, "OSC1 oscillation circuit", for details.

(12) Limiter detection voltage

The limiter detection voltage can be selected from 9 values, 2.1 V or 2.5–3.2 V (0.1 V increments).
Refer to Section 4.16.2, "Mask option", for details.

(13) LCD drive power

Either the internal power supply or an external power supply can be selected for driving the LCD. Furthermore, the voltage regulator output can be selected from V_{C1} and V_{C2} when using the internal power supply.
Refer to Section 4.6.2, "Power supply for LCD driving", for details.

(14) LCD segment specification

The display memory can be allocated to the optional SEG terminal. It is also possible to set the optional SEG terminal for DC output.
Refer to Section 4.6.5, "Segment option", for details.

<Option list>

The following is the option list for the S1C63709.
Multiple selections are available in each option item as indicated in the option list. Select the specifications that meet the target system and check the appropriate box. Be sure to record the specifications for unused functions too.

1. OSC3 SYSTEM CLOCK

☐ 1. CR (built-in R)
☐ 2. CR (external R)
☐ 3. Ceramic

2. INPUT PORT PULL DOWN RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct
• K20	☐ 1. With Resistor	☐ 2. Gate Direct
• K21	☐ 1. With Resistor	☐ 2. Gate Direct
• K22	☐ 1. With Resistor	☐ 2. Gate Direct
• K23	☐ 1. With Resistor	☐ 2. Gate Direct
• K30	☐ 1. With Resistor	☐ 2. Gate Direct

3. RESET PORT PULL DOWN RESISTOR

• RESET	☐ 1. With Resistor	☐ 2. Gate Direct

4. I/O PORT PULL DOWN RESISTOR

- P00 ☐ 1. With Resistor ☐ 2. Gate Direct
- P01 ☐ 1. With Resistor ☐ 2. Gate Direct
- P02 ☐ 1. With Resistor ☐ 2. Gate Direct
- P03 ☐ 1. With Resistor ☐ 2. Gate Direct
- P10 ☐ 1. With Resistor ☐ 2. Gate Direct
- P11 ☐ 1. With Resistor ☐ 2. Gate Direct
- P12 ☐ 1. With Resistor ☐ 2. Gate Direct
- P13 ☐ 1. With Resistor ☐ 2. Gate Direct
- P20 ☐ 1. With Resistor ☐ 2. Gate Direct
- P21 ☐ 1. With Resistor ☐ 2. Gate Direct
- P22 ☐ 1. With Resistor ☐ 2. Gate Direct
- P23 ☐ 1. With Resistor ☐ 2. Gate Direct
- P30 ☐ 1. With Resistor ☐ 2. Gate Direct
- P31 ☐ 1. With Resistor ☐ 2. Gate Direct
- P32 ☐ 1. With Resistor ☐ 2. Gate Direct
- P33 ☐ 1. With Resistor ☐ 2. Gate Direct
- P40 ☐ 1. With Resistor ☐ 2. Gate Direct
- P41 ☐ 1. With Resistor ☐ 2. Gate Direct

5. I/O PORT OUTPUT SPECIFICATION

- P00 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P01 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P02 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P03 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P10 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P11 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P12 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P13 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P20 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P21 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P22 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P23 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P30 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P31 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P32 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P33 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P40 ☐ 1. Complementary ☐ 2. Pch-OpenDrain
- P41 ☐ 1. Complementary ☐ 2. Pch-OpenDrain

6. MULTIPLE KEY ENTRY RESET COMBINATION

☐ 1. Not Use
☐ 2. Use (K00, K01)
☐ 3. Use (K00, K02)
☐ 4. Use (K00, K03)
☐ 5. Use (K00, K01, K02)
☐ 6. Use (K00, K01, K03)
☐ 7. Use (K00, K01, K02, K03)

7. SERIAL INTERFACE POLARITY

☐ 1. Negative
☐ 2. Positive

8. MOTOR PULSE OUTPUT SPECIFICATION

- K13 ☐ 1. Use ☐ 2. Not Use

9. SOLAR SPECIFICATION

☐ 1. Use
☐ 2. Not Use

10. CHATTERING PROTECT OF K12/K13 PORT

- K12 ☐ 1. Use ☐ 2. Not Use
- K13 ☐ 1. Use ☐ 2. Not Use

11. F_{OSC1} REGULATION TYPE

☐ 1. Theoretical Regulation
☐ 2. C_G Regulation

12. CHARGE LIMIT DETECT VOLTAGE

☐ 1. 2.1 V
☐ 2. 2.5 V
☐ 3. 2.6 V
☐ 4. 2.7 V
☐ 5. 2.8 V
☐ 6. 2.9 V
☐ 7. 3.0 V
☐ 8. 3.1 V
☐ 9. 3.2 V

13. LCD DRIVING POWER

☐ 1. Internal Power Supply with V_{C1} Regulator (for 3.0 V Panel)
☐ 2. External Power Supply, 1/3 bias, V_{DD}=V_{C2} (for 4.5 V Panel)
☐ 3. External Power Supply, 1/3 bias, V_{DD}=V_{C3} (for 3.0 V Panel)
☐ 4. External Power Supply, 1/2 bias, V_{DD}=V_{C3}, V_{C1}=V_{C2} (for 3.0 V Panel)
☐ 5. Internal Power Supply with V_{C2} Regulator (for 3.0 V Panel)

14. SEGMENT OPTION

Pin name	Address (F0xx)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									SEG output ☐S
SEG1																									DC output ☐C ☐N
SEG2																									SEG output ☐S
SEG3																									DC output ☐C ☐N
SEG4																									SEG output ☐S
SEG5																									DC output ☐C ☐N
SEG6																									SEG output ☐S
SEG7																									DC output ☐C ☐N
SEG8																									SEG output ☐S
SEG9																									DC output ☐C ☐N
SEG10																									SEG output ☐S
SEG11																									DC output ☐C ☐N
SEG12																									SEG output ☐S
SEG13																									DC output ☐C ☐N
SEG14																									SEG output ☐S
SEG15																									DC output ☐C ☐N
SEG16																									SEG output ☐S
SEG17																									DC output ☐C ☐N
SEG18																									SEG output ☐S
SEG19																									DC output ☐C ☐N
SEG20																									SEG output ☐S
SEG21																									DC output ☐C ☐N
SEG22																									SEG output ☐S
SEG23																									DC output ☐C ☐N
SEG24																									SEG output ☐S
SEG25																									DC output ☐C ☐N
SEG26																									SEG output ☐S
SEG27																									DC output ☐C ☐N
SEG28																									SEG output ☐S
SEG29																									DC output ☐C ☐N
SEG30																									SEG output ☐S
SEG31																									DC output ☐C ☐N
SEG32																									SEG output ☐S
SEG33																									DC output ☐C ☐N
SEG34																									SEG output ☐S
SEG35																									DC output ☐C ☐N
SEG36																									SEG output ☐S
SEG37																									DC output ☐C ☐N
SEG38																									SEG output ☐S
SEG39																									DC output ☐C ☐N
SEG40																									SEG output ☐S
SEG41																									DC output ☐C ☐N
SEG42																									SEG output ☐S
SEG43																									DC output ☐C ☐N
SEG44																									SEG output ☐S
SEG45																									DC output ☐C ☐N
SEG46																									SEG output ☐S
SEG47																									DC output ☐C ☐N
SEG48																									SEG output ☐S
SEG49																									DC output ☐C ☐N
SEG50																									SEG output ☐S
SEG51																									DC output ☐C ☐N
SEG52																									SEG output ☐S
SEG53																									DC output ☐C ☐N
SEG54																									SEG output ☐S
SEG55																									DC output ☐C ☐N
SEG56																									SEG output ☐S
SEG57																									DC output ☐C ☐N
SEG58																									SEG output ☐S
SEG59																									DC output ☐C ☐N
SEG60																									SEG output ☐S
SEG61																									DC output ☐C ☐N
SEG62																									SEG output ☐S
SEG63																									DC output ☐C ☐N

<address> H: RAM data high-order address (0–9)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply System

The S1C63709 operating power voltage is as follows.

Table 2.1.1 Operating voltage

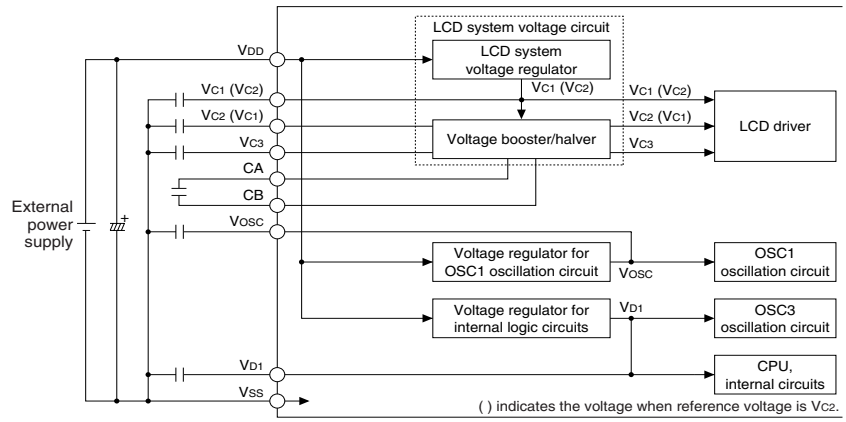
OSC1 oscillation circuit	OSC3 oscillation circuit	Operating voltage
Crystal	Not used	1.0 V to 3.6 V
	CR (built-in R)	1.0 V to 3.6 V
	Ceramic or CR (external R)	2.1 V to 3.6 V

The S1C63709 operates by applying a single power supply within the above range between VDD and VSS. The S1C63709 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.2.

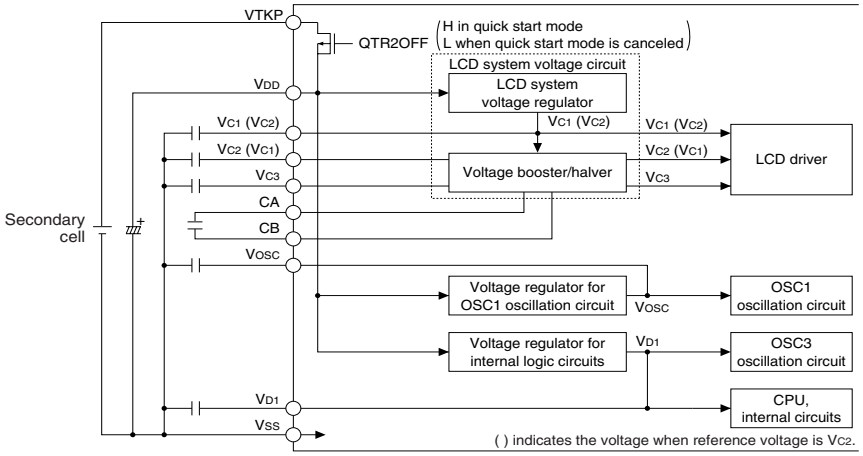
Table 2.1.2 Power supply circuits

Circuit	Power supply	Output voltage
OSC1 circuit	Voltage regulator for OSC1 oscillation circuit	VOSC
OSC3 and internal circuits	Voltage regulator for internal logic circuit	VD1
LCD driver	LCD system voltage circuit	VC1–VC3

Notes:
- *Do not drive external loads with the output voltage from the internal power supply circuits.*
- *When the internal LCD power supply (VC2 regulator) is used, supply a power voltage within the range from 2.1 V to 3.6 V.*
- *See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.*



(1) When solar cell is not used



(2) When solar cell is used

Fig. 2.1.1 Configuration of power supply system

The S1C63709 is capable of being operated with a 0.75 V power voltage for quick start mode when using a solar cell and a secondary cell. (The solar function is selectable by mask option.)
When using a solar cell, connect a secondary cell between the VTKP and VSS terminals.

Notes: • The quick start mode prohibits the use of the OSC3 clock in the voltage range of 0.75 to 1.0 V.

- *The quick start mode activation voltage may vary 0.75 ± 0.20 V depending on the sample.*
- *When no solar power is used, be sure to supply a 1.0 V or more power source voltage.*

2.1.1 Voltage regulator for OSC1 oscillation circuit

This voltage regulator generates the VOSC voltage for driving the OSC1 oscillation circuit and is provided separately with the voltage regulator for the internal logic system to stabilize the oscillation.
The voltage regulator for the OSC1 oscillation circuit requires at least a 0.75 V power source voltage to generates the VOSC voltage capable of driving the oscillation circuit. However, the oscillation circuit will start oscillating if the power source voltage is less than 0.75 V to output a stable clock when the power source voltage rises to 0.75 V or more. To start the oscillation, the voltage regulator for the OSC1 oscillation circuit attempts to stabilize the output voltage while the oscillation-detect circuit (described later) does not detect oscillation. Current consumption increases during this operation.

2.1.2 Voltage regulator for the internal logic system

This voltage regulator generates the VD1 voltage for driving the OSC3 oscillation circuit and the internal logic circuits.

2.1.3 LCD system voltage circuit

The LCD system voltage circuit generates the LCD drive voltage. This circuit allows the software to turn on and off. Turn this circuit on before starting display on the LCD. The LCD system voltage circuit generates VC1 or VC2 with the voltage regulator built-in, and generates two other voltages by boosting/halving VC1 or VC2. The VC1 or VC2 voltage value can be adjusted using software in 16 steps.
The LCD system voltage regulator can be disabled by mask option. In this case, external elements can be minimized because the external capacitors for the LCD system voltage regulator are not necessary. However when the LCD system voltage regulator is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system voltage regulator is used.
Figure 2.1.3.1 shows the external element configuration when the LCD system voltage regulator is not used.

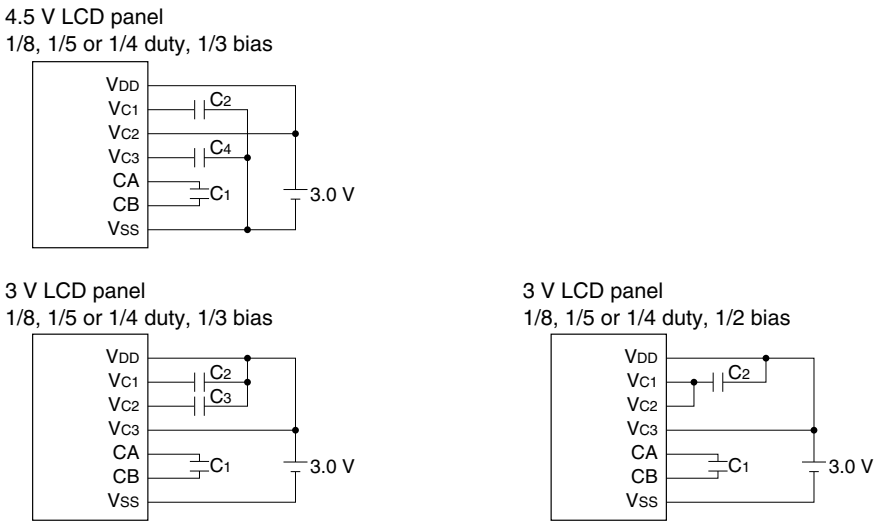


Fig. 2.1.3.1 External elements when LCD system voltage regulator is not used

Refer to Section 4.6, "LCD Driver", for control of the LCD drive voltage.

2.1.4 Operating mode according to the power source voltage

The S1C63709 is able to operate with a minimum power source voltage of 0.75 V to support the quick start function when using a solar cell and a secondary cell. However, it enters a special operating mode to prevent erroneous operation since 0.75 V is out of the operating voltage range. The S1C63709 has three operating modes, including this CPU erroneous-operation-prevent mode, according to the power source voltage level. The hardware automatically switches the operating mode with no software control required. Figure 2.1.4.1 shows the relationship between the operating mode and the power source voltage.

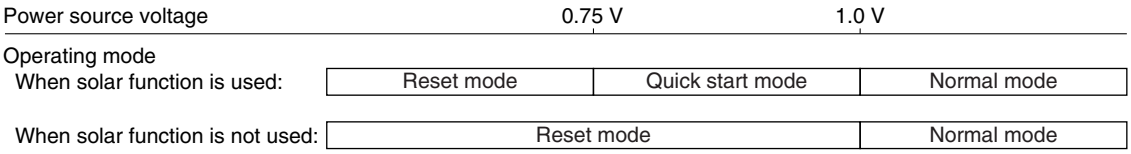


Fig. 2.1.4.1 Operating mode

(1) Reset mode

The internal reset circuit includes an oscillation-detect circuit that outputs an internal reset signal when oscillation cannot be detected. When the power-source voltage is less than 0.75 V, the S1C63709 is placed in reset state by this circuit as the OSC1 oscillation circuit cannot be operated normally. This state is called reset mode.

(2) CPU erroneous-operation-prevent mode (quick start mode)

When the oscillation-detect circuit detects oscillation, it releases the CPU from reset mode and the CPU starts executing. However, the oscillation-detect circuit may release reset mode due to an unstable power source voltage less than 0.75 V, it may cause erroneous operation of the CPU. Therefore this mode can reset the system in 16-second cycles to recover from a system error due to a misdetection of the oscillation-detect circuit.

This mode is provided for quick starting when using a solar cell and a secondary cell (to start up the system as soon as possible after the solar cell starts charging the empty battery), and is controlled by the solar function (mask option). A status bit is available to check whether the system is placed in this mode or not with software. Refer to Section 4.16, "Solar Function", for details.

Therefore, the system in which the solar function has been disabled does not have this mode. In this case, be sure to operate the system with a 1.0 V or more power source voltage.

Notes: • *The quick start mode prohibits the use of the OSC3 clock in the voltage range of 0.75 to 1.0 V.*

• *The quick start mode activation voltage may vary 0.75 ± 0.20 V depending on the sample.*

(3) Normal mode

In quick start mode, the solar control circuit samples the secondary cell voltage periodically, and releases the system from quick start mode when the voltage rises to 1.0 V or more. At this time, the cyclic reset function is disabled and the system enters normal mode.

The system in which the solar function has been disabled operates in normal mode from a 1.0 V power source voltage.

2.2 Initial Reset

To initialize the S1C63709 circuits, initial reset must be executed. There are five ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous high input to terminals K00–K03 (mask option)
(3) Internal initial reset by the oscillation-detect circuit
(4) Software reset using the reset register (only for resetting the peripheral circuits)
(5) Internal initial reset by the VTKP-detect circuit (quick start mode, mask option)

When the power is turned on, be sure to initialize using the reset function (1) or (2). It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

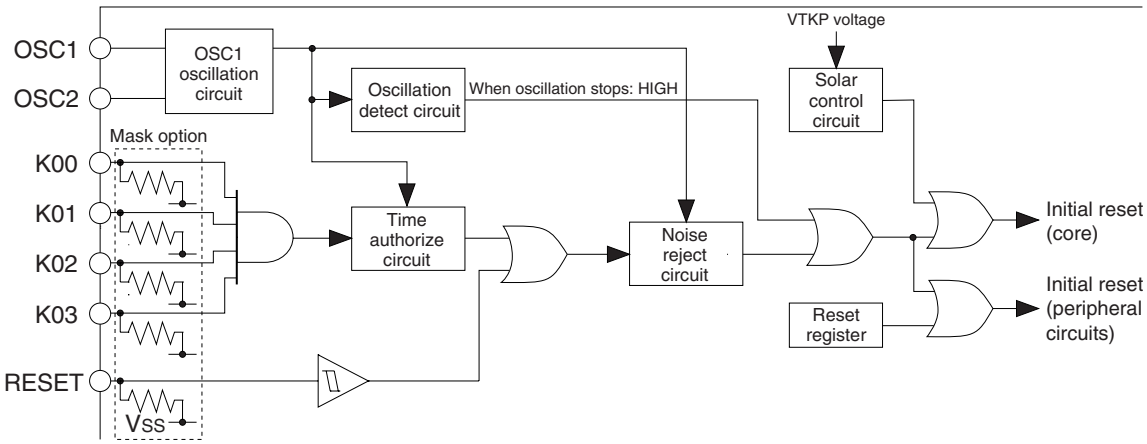


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level (V_{DD}). However, be sure to observe the following precautions, because the reset signal passes through the noise reject circuit. When the RESET terminal is used for initial resetting during operation, a pulse (high level) of 0.4 msec or less is considered to be noise by the noise reject circuit. Maintain a high level of 1.5 msec (when f_{OSC1} = 32.768 kHz) or more to securely perform the initial reset.
After that the initial reset is released by setting the reset terminal to a low level (V_{SS}) and the CPU starts operation.
Since the noise reject circuit does not operate when oscillation is stopped, it is necessary to maintain the reset input at a high level until stabilizing oscillation after turning power on.
The reset terminal incorporates a pull-down resistor and a mask option is provided to select whether the resistor is used or not.

2.2.2 Simultaneous high input to terminals K00–K03

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at high level for at least 1.5 msec (when f_{OSC1} is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at high level for at least 1.5 msec after oscillation starts. Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not used
2	K00∗K01
3	K00∗K02
4	K00∗K03
5	K00∗K01∗K02
6	K00∗K01∗K03
7	K00∗K01∗K02∗K03

When, for instance, mask option 7 (K00∗K01∗K02∗K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time. When other option is selected, the initial reset is done when a key entry including a combination of selected input ports is made.
Further, the time authorize circuit checks the input time of the simultaneous high input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.3 Oscillation-detect circuit

The oscillation-detect circuit outputs the initial reset signal at power-on until the OSC1 oscillation circuit starts oscillating, or when the OSC1 oscillation circuit stops oscillating for some reason.
However, for the initial reset at power-on, use a simultaneous high input of the input ports (K00–K03) or reset terminal, but do not execute it by this function alone.

2.2.4 Software reset for the peripheral circuits

The S1C63709 allows software to reset the peripheral circuits. Write "1" to the reset register (FF00H•D0) to reset.

Table 2.2.4.1 Reset register

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	HVLDON	0	0	SRPER	HVLDON	0	Enable	Disable	Heavy load protection mode enable
					0 *3	– *2			Unused
					0 *3	– *2			Unused
	R/W	R		R/W	SRPER	0	Reset	Invalid	Software reset for peripheral circuits

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

SRPER: Software reset for peripheral circuits (FF00H•D0)
Resets the peripheral circuits.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to SRPER, the peripheral circuits are reset to the initial status.
Writing "0" to the reset register has no effect and the register is always "0" when it is read.
This function does not reset the core CPU.

Note: When the solar control circuit is enabled by mask option, do not perform the software reset for peripheral circuits during quick start mode (when either ISOR2 or ISOR3 is set to "1").

2.2.5 Reset function in quick start mode

When the solar function is enabled by mask option, it resets the system periodically (in 16-second intervals) while the system is in quick start mode (VTKP terminal voltage = 0.75 V to 1.0 V). Refer to Section 4.16, "Solar Function", for details.

2.2.6 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.6.1.
The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.
When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.6.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Other peripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.2.7 Terminal settings at initial resetting

The I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface. These functions are selected by the software. At initial reset, these terminals are set to the general purpose I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of the terminals when designing a system.
Table 2.2.7.1 shows the list of the shared terminal settings.

Table 2.2.7.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output										Serial I/F	
		TOUT	SVDDT	VCWON	ISOR1	ISOR2	ISOR3	CLIM	F16HZ	BZ	FOUT	Master	Slave
P00–P03	P00–P03 (Input & pulled down*)												
P10	P10 (Input & pulled down*)											SIN(I)	SIN(I)
P11	P11 (Input & pulled down*)											SOUT(O)	SOUT(O)
P12	P12 (Input & pulled down*)											SCLK(O)	SCLK(I)
P13	P13 (Input & pulled down*)												SRDY(O)
P20	P20 (Input & pulled down*)	TOUT											
P21	P21 (Input & pulled down*)		SVDDT										
P22	P22 (Input & pulled down*)			VCWON									
P23	P23 (Input & pulled down*)				ISOR1								
P30	P30 (Low output)						ISOR3						
P31	P31 (Low output)					ISOR2							
P32	P32 (Low output)							CLIM					
P33	P33 (Low output)								F16HZ				
P40	P40 (Low output)									BZ			
P41	P41 (Low output)										FOUT		

* When "With Pull-Down" is selected by mask option (high impedance when "Gate Direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal (TEST)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the TEST terminal to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C63709 has a 4-bit core CPU S1C63000 built-in as its CPU part.
Refer to the "S1C63000 Core CPU Manual" for the S1C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the S1C63709.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 12,288 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C63709 is step 0000H to step 2FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

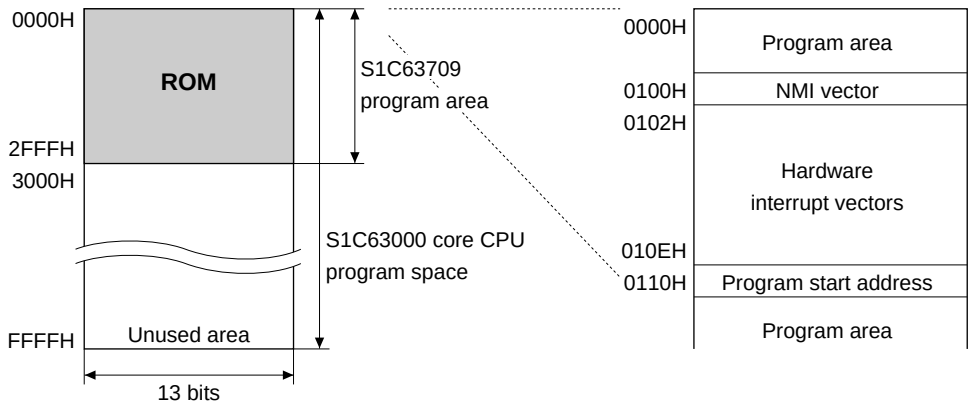


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 2,048 words × 4 bits. The RAM area is assigned to addresses 0000H to 07FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63709 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

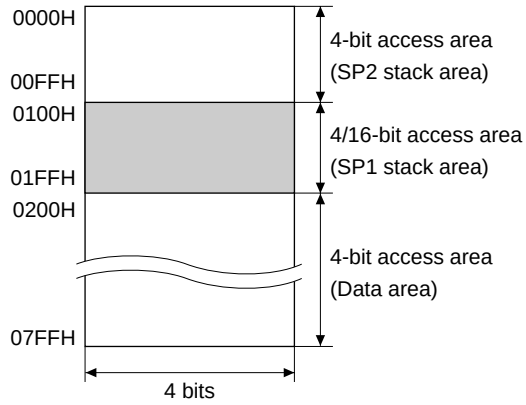


Fig. 3.3.1 Configuration of data RAM

3.4 Data ROM

The data ROM is a mask ROM for loading various static data such as a character generator, and has a capacity of 2,048 words × 4 bits. The data ROM is assigned to addresses 8000H to 87FFH on the data memory map, and the data can be read using the same data memory access instructions as the RAM.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of S1C63709 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The S1C63709 data memory consists of 2,048-word RAM, 2,048-word data ROM, 160-word display memory and 117-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the S1C63709, and Table 4.1.1 the peripheral circuits' (I/O space) memory maps.

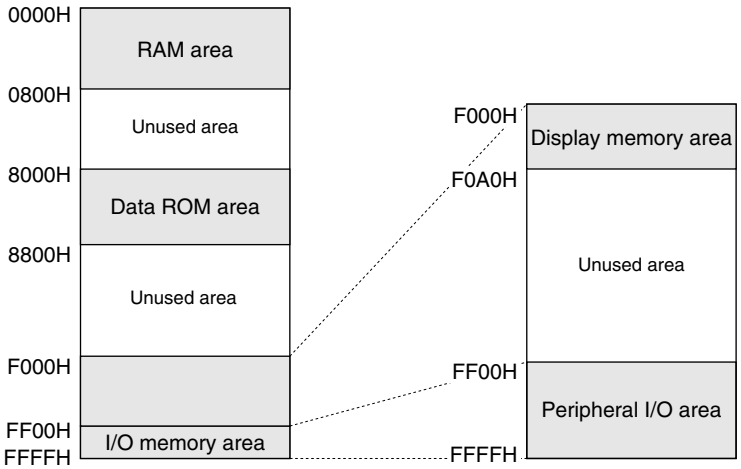


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is created, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF18H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF00H	HVLDON	0	0	SRPER	HVLDON	0	Enable	Disable	Heavy load protection mode enable
					0 *3	– *2			Unused
	R/W	R		R/W	0 *3	– *2			Unused
					SRPER	0	Reset	Invalid	Software reset for peripheral circuits
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FF04H	SVDCHG	SVDS2	SVDS1	SVDS0	SVDCHG	0	3.0 V	1.5 V	SVD voltage system selection
					SVDS2	0			┌ SVD criteria voltage setting
	R/W				SVDS1	0			[SVDS2–0] 0 1 2 3 4 5 6 7
					SVDS0	0			Level 0 1 2 3 4 5 6 7 (highest)
									└ (Use FF50H–FF55H to select voltage values)
FF05H	SVDS3	ESVDDT	SVDDT	SVDON	SVDS3	0	1	0	General-purpose register
					ESVDDT	0	Enable	Disable	SVDDT monitor output enable (P21)
	R/W		R	R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable (P41)
					SWDIR	0			Stopwatch direct input switch
									0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1	0			┌ FOUT frequency selection [FOFQ1, 0] 0 1 2 3
					FOFQ0	0			└ Frequency fosc1/64 fosc1/8 fosc1 fosc3
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF09H	ENISOR3	ENISOR2	E16HZ	0	ENISOR3	0	Enable	Disable	ISOR3 monitor output enable (P30)
					ENISOR2	0	Enable	Disable	ISOR2 monitor output enable (P31)
	R/W			R	E16HZ	0	Enable	Disable	F16HZ clock output enable (P33)
					0 *3	– *2			Unused
FF10H	M0KRNM1	M0KRNM0	0	0	M0KRNM1	0			┌ Number of M0 Kr pulses selection [M0KRNM1, 0] 0 1 2 3
					M0KRNM0	0			└ Count 4 6 8 10
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FF11H	M0K2LN3	M0K2LN2	M0K2LN1	M0K2LN0	M0K2LN3	0			┌ M0 K2 pulse width selection
					M0K2LN2	0			[M0K2LN3–0] 0 1 2 3 4 5 6 7
	R/W				M0K2LN1	0			Width (msec) 3.42 3.66 3.91 4.15 4.39 4.64 4.88 5.13
					M0K2LN0	0			[M0K2LN3–0] 8 9 10 11 12 13 14 15
									└ Width (msec) 5.37 5.62 5.86 6.10 6.35 6.84 7.32 7.81
FF12H	M0KRDY	0	0	0	M0KRDY	0	1/2	1/4	M0 Kr pulse duty cycle selection
					0 *3	– *2			Unused
	R/W	R			0 *3	– *2			Unused
					0 *3	– *2			Unused
FF14H	0	0	M0K2	0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	R	M0K2	0	Output	Not output	M0 fixed drive (K2) pulse output
					0 *3	– *2			Unused
FF16H	0	0	M1PRDEL	M0PRDEL	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		M1PRDEL	0	Pr = 0	M1PRNM	M1 forced 0 Pr pulse selection
					M0PRDEL	0	Pr = 0	M0PRNM	M0 forced 0 Pr pulse selection
FF17H	0	0	M1CL8HZ	M0CL8HZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		M1CL8HZ	0	8 Hz	M1CLS	M1 8-Hz motor clock selection
					M0CL8HZ	0	8 Hz	M0CLS	M0 8-Hz motor clock selection
FF18H	M0PSEL	M0CLS2	M0CLS1	M0CLS0	M0PSEL	0	Reverse	Normal	M0 motor pulse normal/reverse rotation select
					M0CLS2	1			┌ M0 motor clock selection
	R/W				M0CLS1	1			[M0CLS2–0] 0 1 2 3 4 5 6 7
					M0CLS0	1			└ Clock (Hz) 16 25.6 32 42.7 51.2 64 85.3 128

Remarks

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF19H–FF2DH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF19H	M0P1LN3	M0P1LN2	M0P1LN1	M0P1LN0	M0P1LN3	0			M0 P1 pulse width selection
					M0P1LN2	0			[M0P1LN3–0] 0 1 2 3 4 5 6 7
	R/W				M0P1LN1	0			Width (msec) 2.93 3.17 3.42 3.66 3.91 4.15 4.39 4.64
					M0P1LN0	0			[M0P1LN3–0] 8 9 10 11 12 13 14 15
									Width (msec) 4.88 5.13 5.37 5.62 5.86 6.10 6.35 6.59
FF1AH	M0PRNM1	M0PRNM0	M0PRDY	M0GRDY	M0PRNM1	0			Number of M0 Pr pulses selection [M0PRNM1, 0] 0 1 2 3 Count 4 6 8 10
					M0PRNM0	0			
	R/W				M0PRDY	0	1/2	1/4	M0 Pr pulse duty cycle selection
					M0GRDY	0	1/2	1/4	M0 Gr pulse duty cycle selection
FF1BH	M0GRNM	M0G1LN2	M0G1LN1	M0G1LN0	M0GRNM	0	8	4	Number of M0 Gr pulses selection
					M0G1LN2	0			M0 G1 pulse width selection
	R/W				M0G1LN1	0			[M0G1LN2–0] 0 1 2 3 4 5 6 7
					M0G1LN0	0			Width (msec) 0.73 0.98 1.22 1.46 1.71 1.95 2.20 0.49
FF1CH	M0G3LN	M0G2LN2	M0G2LN1	M0G2LN0	M0G3LN	0	6.84 msec	4.88 msec	M0 G3 pulses width selection
					M0G2LN2	0			M0 G2 pulse width selection
	R/W				M0G2LN1	0			[M0G2LN2–0] 0 1 2 3 4 5 6 7
					M0G2LN0	0			Width (msec) 1.71 1.95 2.20 2.44 2.69 2.93 3.17 3.42
FF1DH	M0PD3	M0PD2	M0PD1	M0PD0	M0PD3	0			M0 motor pulse register
					M0PD2	0			
	R/W				M0PD1	0			
					M0PD0	0			
FF1EH	M0PC3	M0PC2	M0PC1	M0PC0	M0PC3	0			M0 motor pulse counter
					M0PC2	0			
	R				M0PC1	0			
					M0PC0	0			
FF1FH	M0POL	M0PCCL	M0RUNM	M0ENM	M0POL	0	O02	O01	M0 output polarity
					M0PCCL	Clear	Clear	Invalid	M0 motor pulse counter clear
	R	W	R	R/W	M0RUNM	0	Run	Stop	M0 motor drive status
					M0ENM	0	Run	Stop	M0 motor drive Run/Stop control
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	K00–K03 input comparison register
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF29H	K23	K22	K21	K20	K23	– *2	High	Low	K20–K23 input port data
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
FF2AH	TRIM23	TRIM22	TRIM21	TRIM20	TRIM23	0	1	0	K20–K23 theoretical regulation input data register
					TRIM22	0	1	0	
	R				TRIM21	0	1	0	
					TRIM20	0	1	0	
FF2DH	ENISOR1	ECLIM	CLIM	K30	ENISOR1	0	Enable	Disable	ISOR1 monitor output enable (P23)
					ECLIM	0	Enable	Disable	CLIM monitor output enable (P32)
	R/W		R		CLIM	0	On	Off	Limit level monitor
					K30	– *2	High	Low	K30 input port data

Table 4.1.1 (c) I/O memory map (FF2EH–FF40H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF2EH	0	0	0	TRIM30	0 *3	0			Unused
					0 *3	0			Unused
	R				0 *3	0			Unused
					TRIM30	0	1	0	K30 theoretical regulation input data register
FF30H	IOC43	IOC42	IOC41	IOC40	IOC43	1	1	0	General-purpose register
					IOC42	1	1	0	General-purpose register
	R/W				IOC41	1	Output	Input	P41 I/O control register Fix at "1" when FOUT is used.
					IOC40	1	Output	Input	P40 I/O control register Fix at "1" when BZ is used.
FF31H	PUL43	PUL42	PUL41	PUL40	PUL43	0	1	0	General-purpose register
					PUL42	0	1	0	General-purpose register
	R/W				PUL41	0	On	Off	P41 pull-down control register Fix at "0" when FOUT is used.
					PUL40	0	On	Off	P40 pull-down control register Fix at "0" when BZ is used.
FF32H	P43	P42	P41	P40	P43	– *2	High	Low	General-purpose register
					P42	– *2	High	Low	General-purpose register
	R/W				P41	– *2	High	Low	P41 I/O port data (FOUTE="0") Fix at "0" when FOUT is used.
					P40	– *2	High	Low	P40 I/O port data (BZE="0") Fix at "0" when BZ is used.
FF33H	K1SMP7	K1SMP6	K1SMP5	K1SMP4	K1SMP7	0	256 Hz	32 Hz	K10–K13 port sampling clock select register
					K1SMP6	0	256 Hz	32 Hz	
	R/W				K1SMP5	0	256 Hz	32 Hz	
					K1SMP4	0	256 Hz	32 Hz	
FF34H	K1SMP3	K1SMP2	K1SMP1	K1SMP0	K1SMP3	0	256/32 Hz	Off	K10–K13 port sampling control register
					K1SMP2	0	256/32 Hz	Off	
	R/W				K1SMP1	0	256/32 Hz	Off	
					K1SMP0	0	256/32 Hz	Off	
FF38H	M1PSEL	M1CLS2	M1CLS1	M1CLS0	M1PSEL	0	Reverse	Normal	M1 motor pulse normal/reverse rotation select
					M1CLS2	1			M1 motor clock selection
	R/W				M1CLS1	1			[M1CLS2–0] 0 1 2 3 4 5 6 7
					M1CLS0	1			Clock (Hz) 16 25.6 32 42.7 51.2 64 85.3 128
FF39H	M1P1LN3	M1P1LN2	M1P1LN1	M1P1LN0	M1P1LN3	0			M1 P1 pulse width selection
					M1P1LN2	0			[M1P1LN3–0] 0 1 2 3 4 5 6 7
	R/W				M1P1LN1	0			Width (msec) 2.93 3.17 3.42 3.66 3.91 4.15 4.39 4.64
					M1P1LN0	0			[M1P1LN3–0] 8 9 10 11 12 13 14 15
									Width (msec) 4.88 5.13 5.37 5.62 5.86 6.10 6.35 6.59
FF3AH	M1PRNM1	M1PRNM0	M1PRDY	M1GRDY	M1PRNM1	0			Number of M1 Pr pulses selection [M1PRNM1, 0] 0 1 2 3 Count 4 6 8 10
					M1PRNM0	0			
	R/W				M1PRDY	0	1/2	1/4	M1 Pr pulse duty cycle selection
					M1GRDY	0	1/2	1/4	M1 Gr pulse duty cycle selection
FF3BH	M1GRNM	M1G1LN2	M1G1LN1	M1G1LN0	M1GRNM	0	8	4	Number of M1 Gr pulses selection
					M1G1LN2	0			M1 G1 pulse width selection
	R/W				M1G1LN1	0			[M1G1LN2–0] 0 1 2 3 4 5 6 7
					M1G1LN0	0			Width (msec) 0.73 0.98 1.22 1.46 1.71 1.95 2.20 0.49
FF3CH	M1G3LN	M1G2LN2	M1G2LN1	M1G2LN0	M1G3LN	0	6.84 msec	4.88 msec	M1 G3 pulses width selection
					M1G2LN2	0			M1 G2 pulse width selection
	R/W				M1G2LN1	0			[M1G2LN2–0] 0 1 2 3 4 5 6 7
					M1G2LN0	0			Width (msec) 1.71 1.95 2.20 2.44 2.69 2.93 3.17 3.42
FF3DH	M1PD3	M1PD2	M1PD1	M1PD0	M1PD3	0			M1 motor pulse register
					M1PD2	0			
	R/W				M1PD1	0			
					M1PD0	0			
FF3EH	M1PC3	M1PC2	M1PC1	M1PC0	M1PC3	0			M1 motor pulse counter
					M1PC2	0			
	R				M1PC1	0			
					M1PC0	0			
FF3FH	M1POL	M1PCCL	M1RUNM	M1ENM	M1POL	0	O12	O11	M1 output polarity
					M1PCCL	Clear	Clear	Invalid	M1 motor pulse counter clear
	R	W	R	R/W	M1RUNM	0	Run	Stop	M1 motor drive status
					M1ENM	0	Run	Stop	M1 motor drive Run/Stop control
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	

Table 4.1.1 (d) I/O memory map (FF41H–FF4EH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF="0") functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF="0") functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF="0") functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF="0") functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-down control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF="0") functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF="0") SIN pull-down control register when SIF is selected
FF46H	P13 (XSRDY)	P12 (XSCLK)	P11 (SOUT)	P10 (SIN)	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF="0") functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF="0") functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF="0") functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register (Fix at "1" when ISOR1 is output.)
					IOC22	0	Output	Input	P22 I/O control register (Fix at "1" when VCWON is output.)
	R/W				IOC21	0	Output	Input	P21 I/O control register (Fix at "1" when SVDDT is output.)
					IOC20	0	Output	Input	P20 I/O control register (Fix at "1" when TOUT is output.)
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register (Fix at "0" when ISOR1 is output.)
					PUL22	1	On	Off	P22 pull-down control register (Fix at "0" when VCWON is output.)
	R/W				PUL21	1	On	Off	P21 pull-down control register (Fix at "0" when SVDDT is output.)
					PUL20	1	On	Off	P20 pull-down control register (Fix at "0" when TOUT is output.)
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P23 I/O port data (Fix at "0" when ISOR1 is output.)
					P22	– *2	High	Low	P22 I/O port data (Fix at "0" when VCWON is output.)
	R/W				P21	– *2	High	Low	P21 I/O port data (Fix at "0" when SVDDT is output.)
					P20	– *2	High	Low	P20 I/O port data (Fix at "0" when TOUT is output.)
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	1	Output	Input	P33 I/O control register (Fix at "1" when F16HZ is output.)
					IOC32	1	Output	Input	P32 I/O control register (Fix at "1" when CLIM is output.)
	R/W				IOC31	1	Output	Input	P31 I/O control register (Fix at "1" when ISOR2 is output.)
					IOC30	1	Output	Input	P30 I/O control register (Fix at "1" when ISOR3 is output.)
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	0	On	Off	P33 pull-down control register (Fix at "0" when F16HZ is output.)
					PUL32	0	On	Off	P32 pull-down control register (Fix at "0" when CLIM is output.)
	R/W				PUL31	0	On	Off	P31 pull-down control register (Fix at "0" when ISOR2 is output.)
					PUL30	0	On	Off	P30 pull-down control register (Fix at "0" when ISOR3 is output.)
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P33 I/O port data (Fix at "0" when F16HZ is output.)
					P32	– *2	High	Low	P32 I/O port data (Fix at "0" when CLIM is output.)
	R/W				P31	– *2	High	Low	P31 I/O port data (Fix at "0" when ISOR2 is output.)
					P30	– *2	High	Low	P30 I/O port data (Fix at "0" when ISOR3 is output.)

Table 4.1.1 (e) I/O memory map (FF50H–FF70H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF50H	S15V12	S15V115	S15V11	S15V105	S15V12	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.2 V)
					S15V115	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.15 V)
	R/W				S15V11	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.1 V)
					S15V105	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.05 V)
FF51H	S15V14	S15V135	S15V13	S15V125	S15V14	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.4 V)
					S15V135	0	Enable	Disable	SVD 1.5-V system detection voltage selection (1.35 V)
	R/W				S15V13	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.3 V)
					S15V125	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.25 V)
FF52H	S3V18	S3V17	S15V16	S15V15	S3V18	1	Enable	Disable	SVD 3.0-V system detection voltage selection (1.8 V)
					S3V17	1	Enable	Disable	SVD 3.0-V system detection voltage selection (1.7 V)
	R/W				S15V16	0	Enable	Disable	SVD 1.5-V system detection voltage selection (1.6 V)
					S15V15	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.5 V)
FF53H	S3V22	S3V21	S3V20	S3V19	S3V22	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.2 V)
					S3V21	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.1 V)
	R/W				S3V20	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.0 V)
					S3V19	1	Enable	Disable	SVD 3.0-V system detection voltage selection (1.9 V)
FF54H	S3V24	S3V235	S3V23	S3V225	S3V24	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.4 V)
					S3V235	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.35 V)
	R/W				S3V23	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.3 V)
					S3V225	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.25 V)
FF55H	S3V27	S3V265	S3V26	S3V25	S3V27	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.7 V)
					S3V265	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.65 V)
	R/W				S3V26	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.6 V)
					S3V25	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.5 V)
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 / Duty 1/4 1/5 1/8
					LDUTY0	0			
	R/W				STCD	0	Static	Dynamic	LCD drive switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	LCFCHG	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all Off control
	R	R/W			ALON	0	All On	Normal	LCD all On control
					LCFCHG	0	25.6 Hz	32 Hz	Frame frequency selection (when 1/4 or 1/8 duty is selected)
FF62H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment [LC3–0] 0 – 15 / Contrast Light – Dark
					LC2	0			
	R/W				LC1	0			
					LC0	0			
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable (P40)
FF6DH	EMPON	BZSTP	BZSHT	SHTPW	EMPON	0	Enable	Disable	Buzzer output enable in motor pulse output period
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
	R/W	W	R/W		BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
							Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3 / Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 / [BZFQ2, 1, 0] 4 5 6 7 / Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
	R	R/W			BZFQ1	0			
					BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
	R	R/W			BDTY1	0			
					BDTY0	0			
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
	R	R/W			SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)

Table 4.1.1 (f) I/O memory map (FF71H–FFC1H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0			Serial I/F clock phase selection –Negative polarity (mask option) –Positive polarity (mask option)
	R/W				SCS1	0			Serial I/F clock mode selection [SCS1, 0] 0 1 Clock Slave Reserved [SCS1, 0] 2 3 Clock OSC1/2 OSC1
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
	R/W				SD1	– *2	High	Low	
					SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
	R/W				SD5	– *2	High	Low	
					SD4	– *2	High	Low	LSB
FF74H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF75H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF76H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FF78H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Direct input enable
					DKM2	0			Key mask selection [DKM2, 1, 0] 0 1 2 3 Key mask None K02 K02–03 K02–03,10 [DKM2, 1, 0] 4 5 6 7 Key mask K10 K10–11 K10–12 K10–13
	R/W				DKM1	0			
					DKM0	0			
FF79H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF7AH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7BH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF7CH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FF88H	0	0	EVCWON	VCWON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EVCWON	0	Enable	Disable	VCWON monitor output enable (P22)
					VCWON	0	On	Off	Theoretical regulation status/trigger (Writing "0" is ineffective.)
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0			Timer 0 pulse polarity selection (for event counter mode)
FFC1H	0	CHSEL1	CHSEL0	PTOUT	0 *3	– *2			Unused
					CHSEL1	0			TOUT output selection [CHSEL1,0] 0 1 2 Timer Timer 0 Timer 1 Timer 2
	R	R/W			CHSEL0	0			
					PTOUT	0	On	Off	TOUT output control (P20)

Table 4.1.1 (g) I/O memory map (FFC2H–FFD0H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC2H	0	CKSEL2	CKSEL1	CKSEL0	0 *3	– *2			Unused
					CKSEL2	0	OSC3	OSC1	Prescaler 2 source clock selection
	R	R/W			CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC3H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00] 0 1 2 3 / Division ratio 1/1 1/4 1/32 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC4H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10] 0 1 2 3 / Division ratio 1/1 1/4 1/32 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC5H	PTPS21	PTPS20	PTRST2	PTRUN2	PTPS21	0			Prescaler 2 division ratio selection [PTPS21, 20] 0 1 2 3 / Division ratio 1/1 1/4 1/32 1/256
					PTPS20	0			
	R/W		W	R/W	PTRST2*3	– *2	Reset	Invalid	Timer 2 reset (reload)
					PTRUN2	0	Run	Stop	Timer 2 Run/Stop
FFC6H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC7H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC8H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC9H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFCAH	RLD23	RLD22	RLD21	RLD20	RLD23	0			MSB
					RLD22	0			Programmable timer 2 reload data (low-order 4 bits)
	R/W				RLD21	0			
					RLD20	0			LSB
FFCBH	RLD27	RLD26	RLD25	RLD24	RLD27	0			MSB
					RLD26	0			Programmable timer 2 reload data (high-order 4 bits)
	R/W				RLD25	0			
					RLD24	0			LSB
FFCCH	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFCDH	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCEH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCFH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFD0H	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB
					PTD22	0			Programmable timer 2 data (low-order 4 bits)
	R				PTD21	0			
					PTD20	0			LSB

Table 4.1.1 (h) I/O memory map (FFD1H–FFF5H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFD1H	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB
					PTD26	0			Programmable timer 2 data (high-order 4 bits)
	R				PTD25	0			
					PTD24	0			LSB
FFE1H	0	EIPT2	EIPT1	EIPT0	0 *3	– *2			Unused
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2)
	R	R/W			EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE2H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE6H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFE8H	0	0	EISMD1	EISMD0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISMD1	0	Enable	Mask	Interrupt mask register (Motor driver 1)
					EISMD0	0	Enable	Mask	Interrupt mask register (Motor driver 0)
FFE9H	0	EIT6	EIT5	EIT4	0 *3	– *2			Unused
					EIT6	0	Enable	Mask	Interrupt mask register (Clock timer 128 Hz)
	R	R/W			EIT5	0	Enable	Mask	Interrupt mask register (Clock timer 64 Hz)
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFECH	EISOR3	EISOR2	EISOR1	EISOR0	EISOR3	0	1	0	General-purpose register
					EISOR2	0	1	0	General-purpose register
	R/W				EISOR1	0	1	0	General-purpose register
					EISOR0	0	Enable	Mask	Interrupt mask register (Solar wakeup)
FFF1H	0	IPT2	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
	R	R/W			IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF2H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)

Table 4.1.1 (i) I/O memory map (FFF6H–FFFCH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFF6H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFF8H	0	0	ISMD1	ISMD0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISMD1	0	(W)	(W)	Interrupt factor flag (Motor driver 1)
					ISMD0	0	Reset	Invalid	Interrupt factor flag (Motor driver 0)
FFF9H	0	IT6	IT5	IT4	0 *3	– *2	(R)	(R)	Unused
					IT6	0	Yes	No	Interrupt factor flag (Clock timer 128 Hz)
	R	R/W			IT5	0	(W)	(W)	Interrupt factor flag (Clock timer 64 Hz)
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFFCH	ISOR3	ISOR2	ISOR1	ISOR0	ISOR3	– *2	Pre Q start	Normal	Quick start mode flag 1
					ISOR2	– *2	Quick start	Normal	Quick start mode flag 2
					ISOR1	– *2	Charge	Not charged	Recharging flag
	R			R/W	ISOR0	0	(R)Yes (W)Reset	(R)No (W)Invalid	Interrupt factor flag (Solar wakeup)

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C63709 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

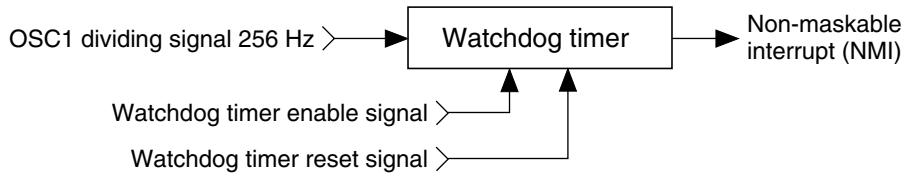


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.2.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.2.3 I/O memory of watchdog timer

Table 4.2.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C63709 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the S1C63709 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software.
Figure 4.3.1.1 is the block diagram of this oscillation system.

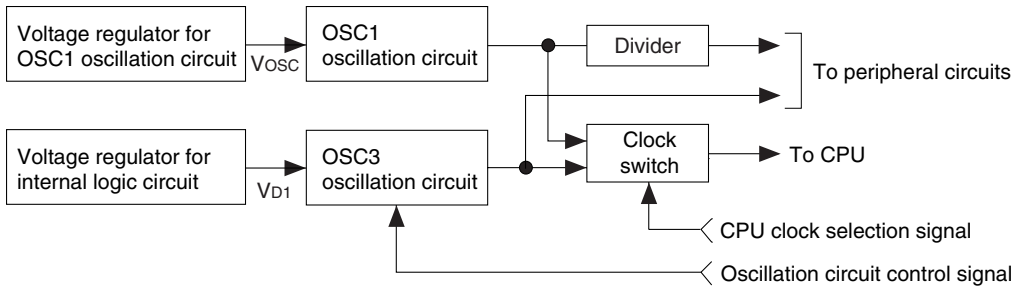


Fig. 4.3.1.1 Oscillation system block diagram

Note: The power supply voltage must be 2.1 V or more to use the OSC3 oscillation circuit.

4.3.2 OSC1 oscillation circuit

The OSC1 crystal oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillation frequency is 32.768 kHz (Typ.).
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

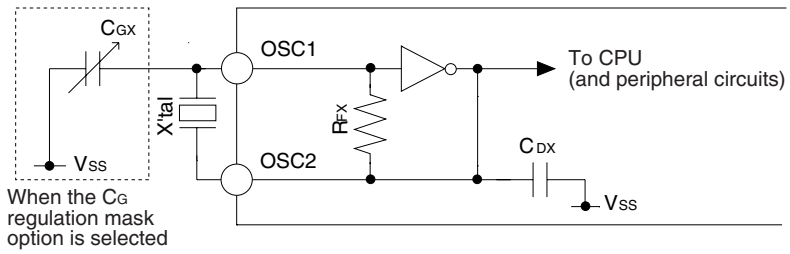


Fig. 4.3.2.1 OSC1 oscillation circuit

As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal resonator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals.

The OSC1 oscillation circuit provides a mask option to select the oscillation frequency adjustment method. Either theoretical regulation or CG regulation can be selected.
When CG regulation is selected by mask option, connect a 0 to 20 pF trimmer capacitor (CGX) between the OSC1 and VSS terminals.

Note: When theoretical regulation is selected, do not connect a capacitor between the OSC1 and Vss terminals.

Refer to Section 4.13, "Theoretical Regulation", for details of theoretical regulation.

4.3.3 OSC3 oscillation circuit

The S1C63709 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 4.2 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, serial interface, FOUT output). The mask option enables selection of the oscillator type from CR (external R type), CR (built-in R type) and ceramic oscillation circuit. When CR oscillation (external R type) is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required. When CR oscillation (built-in R type) is selected, no external element is required.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.

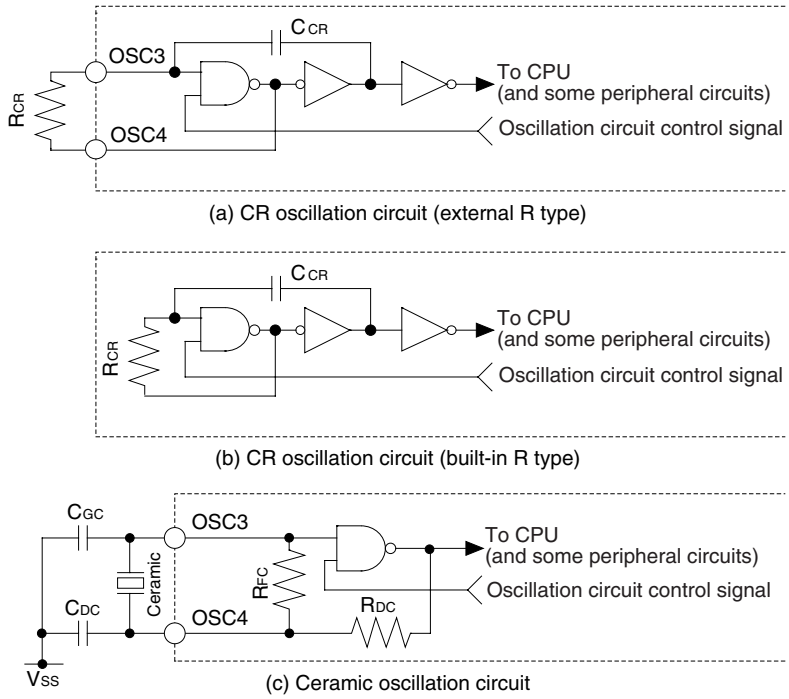


Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit (external R type) can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of RCR.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 4.2 MHz) between the OSC3 and OSC4 terminals, capacitor CGC between the OSC3 and OSC4 terminals, and capacitor CDC between the OSC4 and VSS terminals. For both CGC and CDC, connect capacitors that are about 30 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

Table 4.3.3.1 OSC3 oscillation frequency

Oscillation circuit	Oscillation frequency
Ceramic oscillation	Max. 4.2 MHz
CR oscillation (built-in R type)	Typ. 200 kHz ±30%
CR oscillation (external R type)	200 kHz to 2.2 MHz

4.3.4 Switching of CPU clock

The system clock can be selected between OSC1 and OSC3 with software (using the CLKCHG register). The CPU clock should be switched using the following procedure. Pay special attention to the stability waiting time for oscillation.

OSC1 → OSC3

1. Set OSCC to "1". (OSC3 oscillation: off → on)
2. Wait 5 msec or more.
3. Set CLKCHG to "1". (CPU clock: OSC1 → OSC3)

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC3 → OSC1

1. Set CLKCHG to "0". (CPU clock: OSC3 → OSC1)
2. Set OSCC to "0". (OSC3 oscillation: on → off)

Note: When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC3: 200 kHz	10	20	30
OSC3: 1.1 MHz	1.8	3.6	5.5
OSC3: 2 MHz	1	2	3
OSC3: 4 MHz	0.5	1	1.5

4.3.6 I/O memory of oscillation circuit

Table 4.3.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF01H	CLKCHG	OSCC	0	0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

OSCC: OSC3 oscillation control register (FF01H•D2)

Turns the OSC3 oscillation circuit on and off.

When "1" is written: OSC3 oscillation On
When "0" is written: OSC3 oscillation Off
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF01H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation on (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) The quick start mode prohibits the use of the OSC3 clock.

4.4 Input Ports (K00–K03, K10–K13, K20–K23 and K30)

4.4.1 Configuration of input ports

The S1C63709 has 13 bits of general-purpose input ports. Four bits in these ports can be used as general-purpose input ports and the other nine bits have a special circuit configuration for supporting watch applications.

K0 ports (K00–K03): General-purpose input ports (with programmable interrupt timings)
K1 ports (K10–K11): Input ports for crown switches (with a rising and falling edge trigger interrupt function)
(K12–K13): Input ports for noise rejection (with a rising and falling edge trigger interrupt function)
K2 ports (K20–K23): Input ports for theoretical regulation
(with no interrupt function, pulled-down while reading)
K3 port (K30): Input port for theoretical regulation
(with no interrupt function, pulled-down while reading)

Each input port terminal provides an internal pull-down resistor that can be enabled by mask option. Figure 4.4.1.1 shows the configuration of input ports.

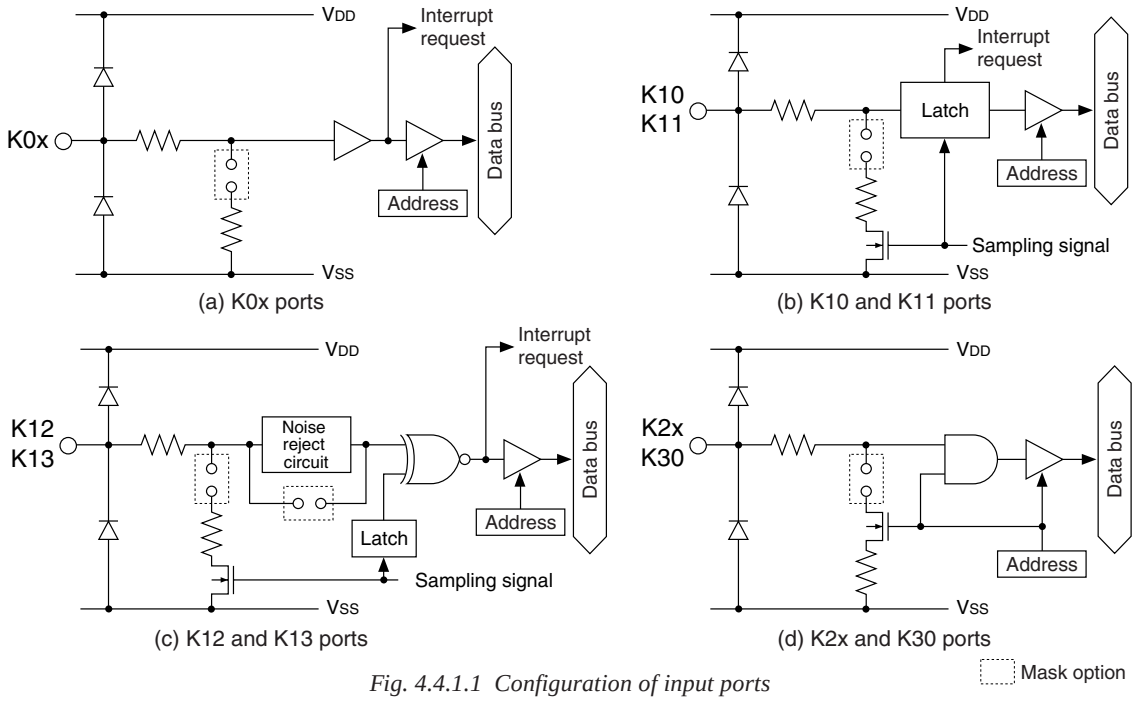


Fig. 4.4.1.1 Configuration of input ports

The K0 ports allow software to select either the rising edge or falling edge of input signals as the trigger to generate an interrupt. The K00 and K01 input ports can also be used as the Run/Stop and Lap direct inputs for the stopwatch timer.

The K1 ports are intended to be used for inputs of crown switches. These ports generate an interrupt at both the rising and falling edges of the input signals. Furthermore, the K1 ports allow software to use an input signal sampling circuit. When this circuit is enabled, the input signal is sampled with the specified clock (32 Hz or 256 Hz selectable) and the sampling results can be read out as the port input data. The pull-down resistor activates and an input interrupt occurs at the same time the signal is sampled.

The K12 and K13 ports can be used with a noise-reject circuit for eliminating chattering that can be attached by mask option.

The five bits of K2 and K3 ports are intended to be used for inputting a theoretical regulation value, so they do not have an interrupt function. Since these ports may not be used frequently, the pull-down resistors, even if enabled by mask option, are turned on only when the input status is read. Refer to Section 4.13, "Theoretical Regulation".

4.4.2 Mask option

Pull-down resistor

Internal pull-down resistor can be selected for each of the 13 bits of the input ports (K00–K03, K10–K13, K20–K23 and K30) with the input port mask option.
Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.
When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

Noise-reject circuit for K12 and K13

The K12 and K13 ports provide a mask option to select whether a noise-reject circuit is attached or not. When this circuit is attached, pulses within 6.84 msec to 14.65 msec are regarded as noise and are not input. To input the signal reliably, the input signals must have an active level width of more than 14.65 msec.

4.4.3 Interrupt function

The K0 (K00–K03) and K1 (K10–K13) input ports provide the interrupt function.
There is little difference in the interrupt functions between the K0 ports and K1 ports, so the following describes the interrupt functions separately.

(1) K0 input interrupt

In the K0 port, the conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.4.3.1 shows the configuration of the K0 port interrupt circuit.

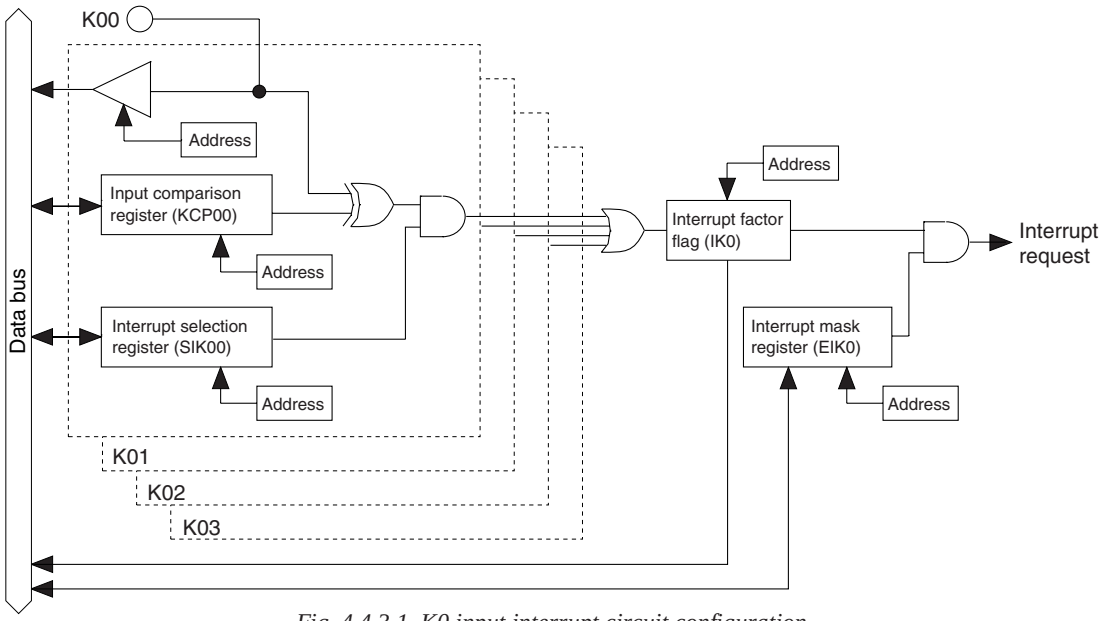


Fig. 4.4.3.1 K0 input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually provided for the input ports K00–K03, and can specify the terminals for generating interrupt and interrupt timing.
The interrupt selection registers (SIK00–SIK03) select what input of K00–K03 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.

The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03).
By setting these two conditions, the interrupt for K00–K03 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.
The interrupt mask register (EIK0) enables the interrupt mask to be selected for K00–K03.
When the interrupt is generated, the interrupt factor flag (IK0) is set to "1".
Figure 4.4.3.2 shows an example of an interrupt for K00–K03.

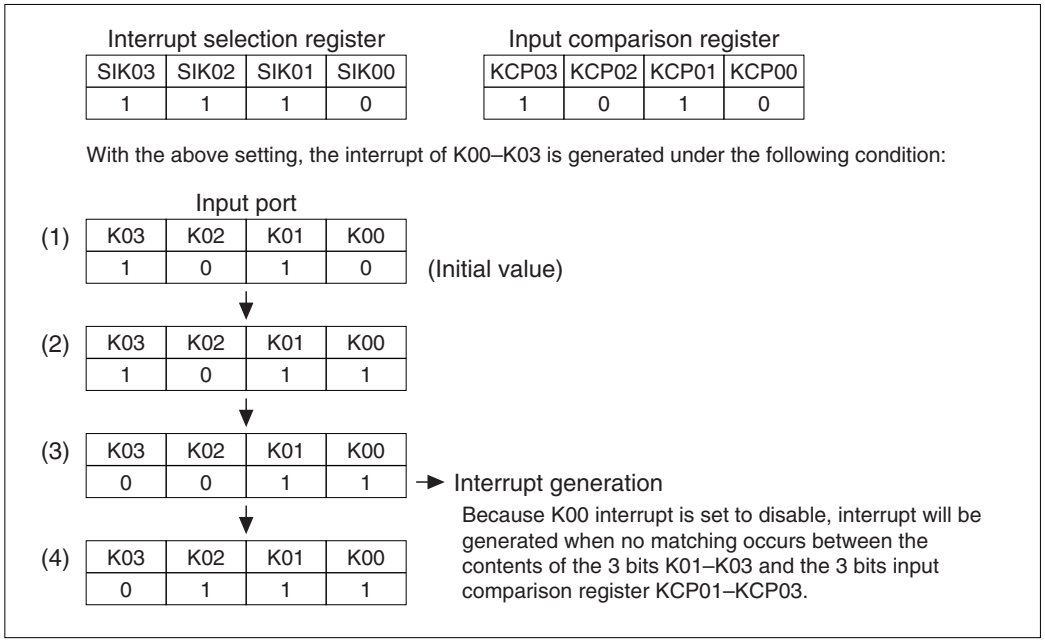


Fig. 4.4.3.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

(2) K1 input interrupt

Each of these four ports (K10–K13) allows software to select whether its interrupt function is used or not. Furthermore, interrupt requests to the CPU can be masked in software.
Figure 4.4.3.3 shows the configuration of the K1 port interrupt circuit.

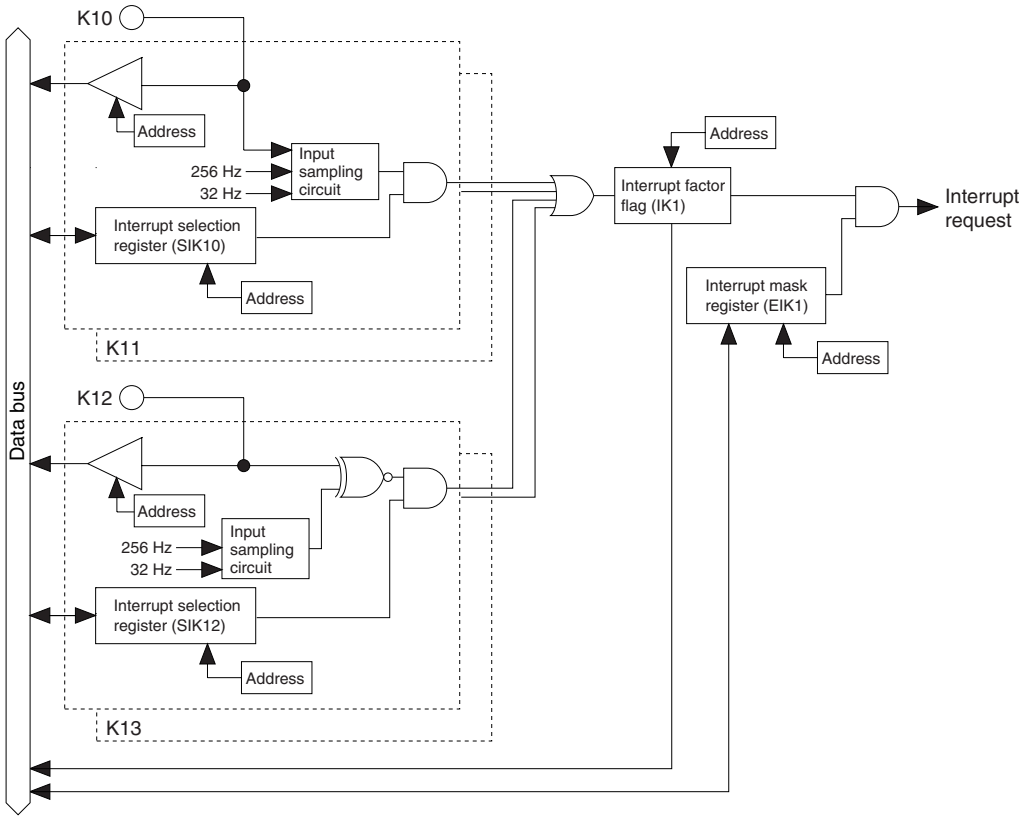


Fig. 4.4.3.3 K1 input interrupt circuit configuration

The K10–K13 input ports have interrupt selection registers (SIK) used to specify the terminals for generating interrupts, similar to the K0 ports. Writing "1" to an interrupt selection register incorporates the corresponding input port into the interrupt generation conditions. Changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
Each K1 port has an embedded input sampling circuit. The input sampling circuit is enabled by writing "1" to the K1x sampling control register provided individually for the K1x port. Furthermore, a 32-Hz or 256-Hz sampling clock can be selected individually in each port.

The K10 and K11 ports are intended to be used for inputs of crown switches (can also be used as general-purpose input ports). When the sampling function is enabled, an interrupt will occur at the rising edge of the sampling clock immediately after the input signal to the port, which has been enabled for an interrupt to occur, changes (rises or falls). This interrupt can be used to execute the process when the crown of the watch is pulled out and pushed in. To check whether the interrupt has occurred by the rising edge or falling edge, read the input port data. If the input sampling circuit is disabled, the K10 and K11 input ports cannot generate an interrupt.

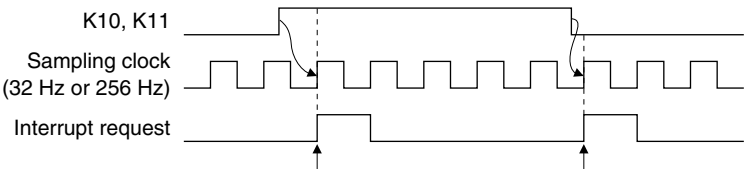


Fig. 4.4.3.4 K10 and K11 input interrupt timing

The K12 and K13 ports can also generate interrupts at the rising edge and falling edge of the input signal. However, to generate interrupts at both signal edges, two or more sampling clock cycles are required. Therefore, maintain the signal level (high or low) after the signal rises or falls for 62.5 msec or more when the 32 Hz clock is selected using the sampling clock select register, or 7.82 msec or more when the 256 Hz clock is selected.

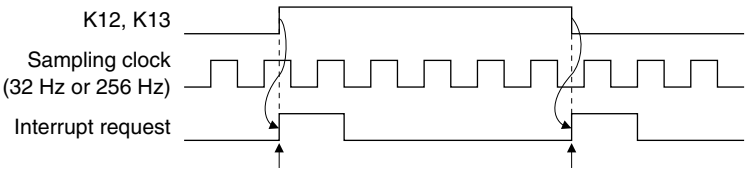


Fig. 4.4.3.5 K12 and K13 input interrupt timing (when input sampling circuit is on)

The K12 and K13 ports generate interrupts at only the rising edge of the input signal if the input sampling circuit is off.

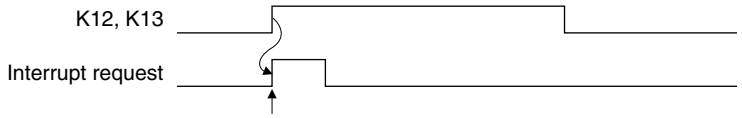


Fig. 4.4.3.6 K12 and K13 input interrupt timing (when input sampling circuit is off)

The interrupt mask register (EIK1) enables or masks the K1 input interrupt requests to the CPU. When an interrupt occurs, the interrupt factor flag (IK1) is set to "1".

4.4.4 I/O memory of input ports

Table 4.4.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.4.4.1 Control bits of input ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	K00–K03 input comparison register
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF29H	K23	K22	K21	K20	K23	– *2	High	Low	K20–K23 input port data
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
FF2DH	ENISOR1	ECLIM	CLIM	K30	ENISOR1	0	Enable	Disable	ISOR1 monitor output enable (P23)
					ECLIM	0	Enable	Disable	CLIM monitor output enable (P32)
	R/W		R		CLIM	0	On	Off	Limit level monitor
					K30	– *2	High	Low	K30 input port data
FF33H	K1SMP7	K1SMP6	K1SMP5	K1SMP4	K1SMP7	0	256 Hz	32 Hz	K10–K13 port sampling clock select register
					K1SMP6	0	256 Hz	32 Hz	
	R/W				K1SMP5	0	256 Hz	32 Hz	
					K1SMP4	0	256 Hz	32 Hz	
FF34H	K1SMP3	K1SMP2	K1SMP1	K1SMP0	K1SMP3	0	256/32 Hz	Off	K10–K13 port sampling control register
					K1SMP2	0	256/32 Hz	Off	
	R/W				K1SMP1	0	256/32 Hz	Off	
					K1SMP0	0	256/32 Hz	Off	
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)
K10–K13: K1 port input port data (FF25H)
K20–K23: K2 port input port data (FF29H)
K30: K3 port input port data (FF2DH•D0)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of each input port goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)
SIK10–SIK13: K1 port interrupt selection register (FF24H)

Selects the ports to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)

Interrupt conditions for terminals K00–K03 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the four bits (K00–K03), through the input comparison registers (KCP00–KCP03).
A comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers.
At initial reset, these registers are set to "0".

K1SMP0–K1SMP3: K1 port sampling control register (FF34H)

Selects whether the K1 port input sampling function is used or not.

When "1" is written: Use 256-Hz or 32-Hz sampling
When "0" is written: Not used (sampling circuit is disabled)
Reading: Valid

K1SMP0–K1SMP3 are the sampling control registers corresponding to the K10–K13 ports. When the register is set to "1", the input signal of the corresponding port will be sampled with the 256-Hz or 32-Hz clock.
In this setting, an K10 or K11 interrupt will occur at the rising edge of the sampling clock immediately after the input signal to the port changes (rises or falls). When the register is set to "0", no interrupt will occur from the corresponding input port.
The K12 or K13 interrupts will occur at the rising or falling edge of the input signal when the signal has changed. When the input sampling circuit is off, interrupts will occur at only the rising edge of the input signal.
At initial reset, these registers are set to "0".

K1SMP4–K1SMP7: K1 port sampling clock select register (FF33H)

Selects the K1 port sampling clock frequency.

When "1" is written: 256 Hz
When "0" is written: 32 Hz
Reading: Valid

K1SMP4–K1SMP7 are the sampling clock select registers corresponding to the K10–K13 ports. The 256-Hz sampling clock is selected when the register is set to "1" and the 32-Hz sampling clock is selected when the register is set to "0". Use K1SMP0–K1SMP3 to enable or disable the sampling function for each port.
At initial reset, these registers are set to "0".

EIK0: K0 input interrupt mask register (FFE3H•D0)
EIK1: K1 input interrupt mask register (FFE4H•D0)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the two systems (K00–K03, K10–K13).
At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF3H•D0)
IK1: K1 input interrupt factor flag (FFF4H•D0)

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

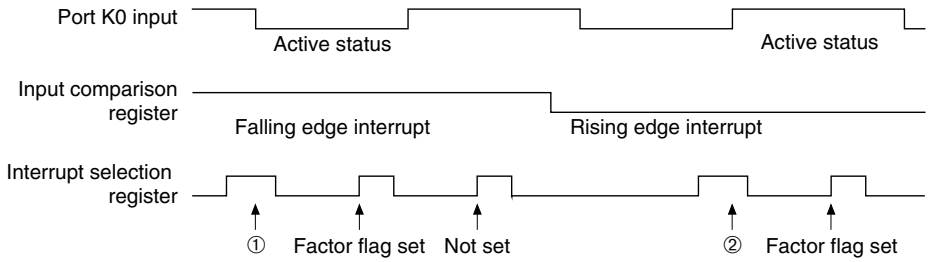
The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 300 kΩ (Max.)

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) Input interrupt programming related precautions



When the content of the interrupt selection register is rewritten while the port K0 input is in the active status, the input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 4.4.5.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the interrupt selection register, when the value of the input terminal which becomes the interrupt input is in active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies
input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.
When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 4.4.5.1. However, when clearing the content of the interrupt selection register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in active status (low status), do not rewrite the interrupt selection register (clearing, then setting the interrupt selection register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the interrupt selection register, set the interrupt selection register, when the input terminal is not in active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 4.4.5.1. In this case, when the interrupt selection registers cleared, then set, you should set the interrupt selection register, when the input terminal is in low status.
In addition, when the interrupt selection register = "1" and the content of the input comparison register is rewritten in input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the interrupt selection register = "0" status.

The same applies to the K12 and K13 ports when the input sampling circuit is off. When the input terminal is in active status (high status), do not rewrite the interrupt selection register (clearing, then setting the interrupt selection register).

4.5 I/O Ports (P00–P03, P10–P13, P20–P23, P30–P33 and P40–P41)

4.5.1 Configuration of I/O ports

The S1C63709 has 18 bits of general-purpose I/O ports. Figure 4.5.1.1 shows the configuration of the I/O port.

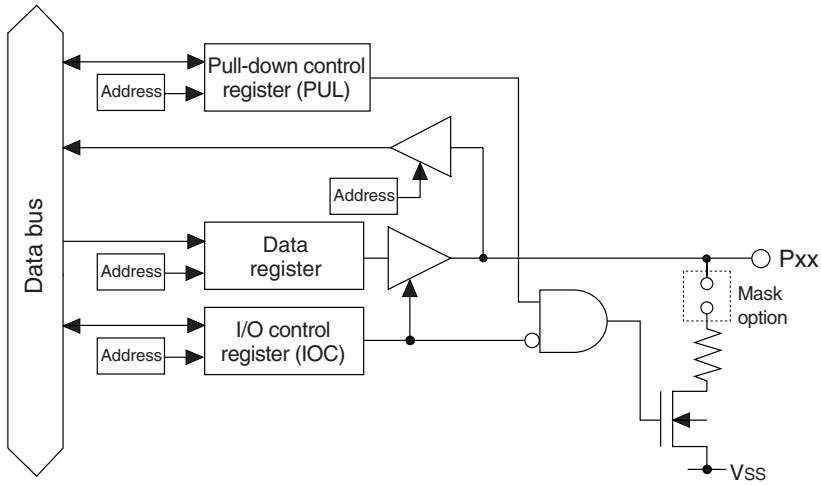


Fig. 4.5.1.1 Configuration of I/O port

The I/O port terminals P10 to P13 are shared with the serial interface input/output ports. Also the I/O port terminals P20 to P23, P30 to P33, P40 and P41 are shared with the special output ports. The software can select the function to be used. At initial reset, these terminals are all set to the I/O port.
Table 4.5.1.1 shows the setting of the input/output terminals by function selection.

Table 4.5.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	Special output										Serial I/F	
		TOUT	SVDDT	VCWON	ISOR1	ISOR2	ISOR3	CLIM	F16HZ	BZ	FOUT	Master	Slave
P00–P03	P00–P03 (Input & pulled down*)	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03	P00–P03
P10	P10 (Input & pulled down*)											SIN(I)	SIN(I)
P11	P11 (Input & pulled down*)											SOUT(O)	SOUT(O)
P12	P12 (Input & pulled down*)											SCLK(O)	SCLK(I)
P13	P13 (Input & pulled down*)												SRDY(O)
P20	P20 (Input & pulled down*)	TOUT											
P21	P21 (Input & pulled down*)		SVDDT										
P22	P22 (Input & pulled down*)			VCWON									
P23	P23 (Input & pulled down*)				ISOR1								
P30	P30 (Low output)						ISOR3						
P31	P31 (Low output)					ISOR2							
P32	P32 (Low output)							CLIM					
P33	P33 (Low output)								F16HZ				
P40	P40 (Low output)									BZ			
P41	P41 (Low output)										FOUT		

* When "With Pull-Down" is selected by mask option (high impedance when "Gate Direct" is selected)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit unit). Modes can be set by writing data to the I/O control registers.
Refer to Section 4.10, "Serial Interface", for controlling the serial interface. Refer to Section 4.11, "Sound Generator", for controlling the BZ output.

4.5.2 Mask option

Output specification

The output specification of each I/O port during output mode can be selected from either complementary output or P-channel open drain output by mask option. This selection can be done in 1-bit units. When P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

Pull-down resistor

The mask option also allows selection of whether the pull-down resistor is used or not during input mode. This selection can be done in 1-bit units. When "without pull-down" during the input mode is selected, take care that the floating status does not occur.

The pull-down resistor for input mode and output specification (complementary output or P-channel open drain output) selected by mask option are effective even when I/O port terminals are used for the serial interface and special outputs.

4.5.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-down explained in the following section has been set by software, the input line is pulled down only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode, it works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the IOC00–IOC03, IOC10–IOC13 and IOC20–IOC23 registers are set to "0", so the P0, P1 and P2 I/O ports enter in input mode. The IOC30–IOC33 and IOC40–IOC41 registers are set to "1" for setting the P3 and P4 I/O ports in output mode.

The I/O control registers of the ports that are set as input/output for the serial interface can be used as general purpose registers that do not affect the I/O control.

4.5.4 Pull-down during input mode

A pull-down resistor that operates during the input mode is built into each I/O port of the S1C63709. Mask option can set the use or non-use of this pull-down.

The pull-down resistor becomes effective by writing "1" to the pull-down control register PULxx that corresponds to each port, and the input line is pulled down during the input mode. When "0" has been written, no pull-down is done.
At initial reset, the PUL00–PUL03, PUL10–PUL13 and PUL20–PUL23 registers are set to "1", so the P0, P1 and P2 port pull-down resistors are enabled. The PUL30–PUL33 and PUL40–PUL41 registers are set to "0" for disabling the P3 and P4 port pull-down resistors.

The pull-down control registers of the ports in which "gate direct" has been selected can be used as general purpose registers.
Even when "with pull-down" has been selected, the pull-down control registers of the ports, that are set as output for the serial interface, can be used as general purpose registers that do not affect the pull-down control.
The pull-down control registers of the ports, that are set as input for the serial interface and special outputs, function the same as the I/O port.

4.5.5 Special output

In addition to the general-purpose I/O port function, a special signal output function can be selected for the I/O ports P20 to P23, P30 to P33, P40 and P41 as shown in Table 4.5.5.1 with the software.

Table 4.5.5.1 Special output

Terminal	Special output	Output control register
P20	TOUT	PTOUT
P21	SVDDT	ESVDDT
P22	VCWON	EVCWON
P23	ISOR1	ENISOR1
P30	ISOR3	ENISOR3
P31	ISOR2	ENISOR2
P32	CLIM	ECLIM
P33	F16HZ	E16HZ
P40	BZ	BZE, BZSHT
P41	FOUT	FOUTE

At initial reset, the P20 to P23 I/O control registers are set to "0" (input), the port data registers are set to "0" and the pull-down control registers are set to "1" (pull-down enabled). Consequently, the terminals are configured as input ports. The P30 to P33, P40 and P41 I/O control registers are set to "1" (output), the port data registers are set to "0" and the pull-down control registers are set to "0" (pull-down disabled). Consequently, the terminals are configured as output ports with low (V_{SS}) level output.
When using the Pxx port as the special output port, fix the I/O control register (IOCxx) at "1" (output), the data register (Pxx) at "0" and the pull-down control register (PULxx) at "0" (pull-down disabled). The respective signal output should be turned on and off using the special output control register.

Note: The data register, I/O control register and pull-down control register are effective even if the Pxx is used for special output. To prevent the occurrence of undesired terminal conditions, do not change the register values after setting the data register (Pxx) to "0", the I/O control register (IOCxx) to "1", and the pull-down control register (PULxx) to "0".

SVDDT (P21), ISOR1–3 (P23, P31, P30), CLIM (P32)

The P21, P23 and P30 to P32 ports can be configured as the output ports for monitoring the internal signals (control register values) shown below.

Table 4.5.5.2 Internal signals that can be output for monitoring

Terminal	Internal signal	Description	Output control register
P21	SVDDT	SVD detection data (SVDDT register value)	ESVDDT
P23	ISOR1	Recharging flag status (ISOR1 register value)	ENISOR1
P30	ISOR3	Quick start mode flag 1 status (ISOR3 register value)	ENISOR3
P31	ISOR2	Quick start mode flag 2 status (ISOR2 register value)	ENISOR2
P32	CLIM	Solar recharging (limiter) status (CLIM register value)	ECLIM

Use the special output control register corresponding to each signal to enable and disable monitor output. Figure 4.5.5.1 shows the output waveform of the internal signal.

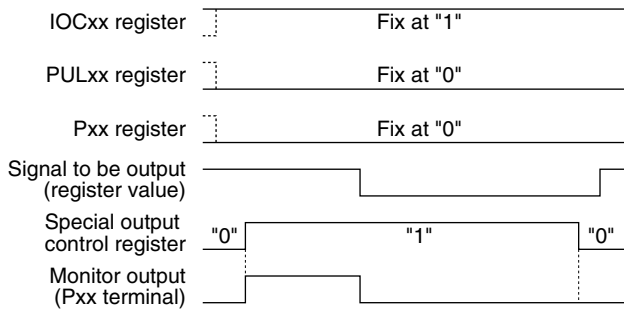


Fig. 4.5.5.1 Internal signal monitor output

Refer to the respective section of the peripheral circuit for details of the signal (register).

TOUT (P20)

The P20 terminal can output the TOUT signal.
The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
To output the TOUT signal, fix the IOC20 register at "1", the P20 register at "0" and the PUL20 register at "0", and turn the signal on and off using the PTOUT register. It is, however, necessary to control the programmable timer.
Refer to Section 4.9, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned on and off.

Figure 4.5.5.2 shows the output waveform of the TOUT signal.

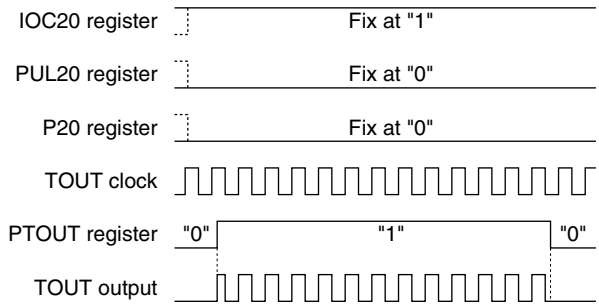


Fig. 4.5.5.2 Output waveform of TOUT signal

VCWON (P22)

The P22 terminal can output the VCWON write signal.
This allows monitoring of the theoretical regulation execution status.
To output the VCWON write signal, fix the IOC22 register at "1", the P22 register at "0" and the PUL22 register at "0", and turn the signal output on and off using the EVCWON register.
Refer to Section 4.13, "Theoretical Regulation", for more information on VCWON.
Figure 4.5.5.3 shows the output waveform of the VCWON write signal.

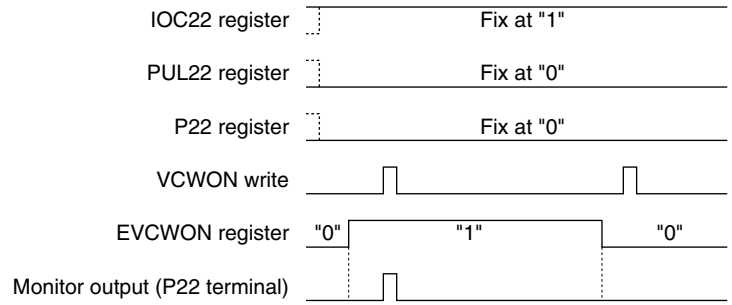


Fig. 4.5.5.3 VCWON write signal output

F16HZ (P33)

The P33 terminal can output the F16HZ signal.
The F16HZ signal is a 16 Hz clock for an external device.
Use the E16HZ register to turn the clock output on and off.

Note: A hazard may occur when the F16HZ signal is turned on and off.

Figure 4.5.5.4 shows the output waveform of the F16HZ signal.

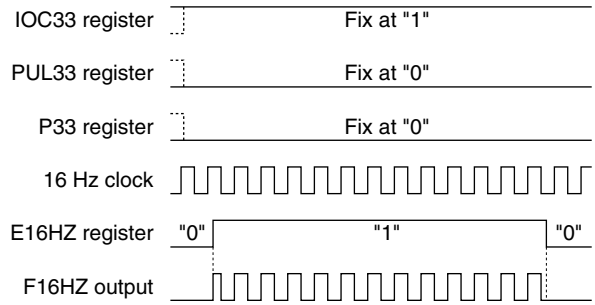


Fig. 4.5.5.4 Output waveform of F16HZ signal

BZ (P40)

The P40 terminal can output a BZ signal.
The BZ signal is the buzzer signal that is output from the sound generator.
Use the BZE or BZSHT register for controlling (ON/OFF) the BZ signal output.
Refer to Section 4.11, "Sound Generator" for details of the buzzer signal and controlling method.

FOUT (P41)

The P41 terminal can output the FOUT signal.
The FOUT signal is a clock (f_{OSC1} or f_{OSC3}) that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
To output the FOUT signal, fix the IOC41 register at "1", the P41 register at "0" and the PUL41 register at "0", and turn the signal on and off using the FOUTE register.
The frequency of the output clock may be selected from among 4 types shown in Table 4.5.5.3 by setting the FOFQ0 and FOFQ1 registers.

Table 4.5.5.3 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and precautions.

Note: A hazard may occur when the FOUT signal is turned on and off.

Figure 4.5.5.5 shows the output waveform of the FOUT signal.

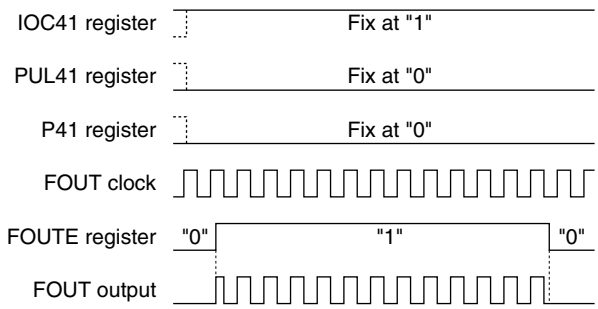


Fig. 4.5.5.5 Output waveform of FOUT signal

4.5.6 I/O memory of I/O ports

Table 4.5.6.1 shows the I/O addresses and the control bits for the I/O ports.

Table 4.5.6.1(a) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF30H	IOC43	IOC42	IOC41	IOC40	IOC43	1	1	0	General-purpose register
					IOC42	1	1	0	General-purpose register
	R/W				IOC41	1	Output	Input	P41 I/O control register Fix at "1" when FOUT is used.
					IOC40	1	Output	Input	P40 I/O control register Fix at "1" when BZ is used.
FF31H	PUL43	PUL42	PUL41	PUL40	PUL43	0	1	0	General-purpose register
					PUL42	0	1	0	General-purpose register
	R/W				PUL41	0	On	Off	P41 pull-down control register Fix at "0" when FOUT is used.
					PUL40	0	On	Off	P40 pull-down control register Fix at "0" when BZ is used.
FF32H	P43	P42	P41	P40	P43	– *2	High	Low	General-purpose register
					P42	– *2	High	Low	General-purpose register
	R/W				P41	– *2	High	Low	P41 I/O port data (FOUTE="0") Fix at "0" when FOUT is used.
					P40	– *2	High	Low	P40 I/O port data (BZE="0") Fix at "0" when BZ is used.
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-down control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF="0") functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF="0") functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF="0") functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF="0") functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-down control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF="0") functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF="0") SIN pull-down control register when SIF is selected
FF46H	P13 (XSRDY)	P12 (XSCLK)	P11 (SOUT)	P10 (SIN)	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF="0") functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF="0") functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF="0") functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register (Fix at "1" when ISOR1 is output.)
					IOC22	0	Output	Input	P22 I/O control register (Fix at "1" when VCWON is output.)
	R/W				IOC21	0	Output	Input	P21 I/O control register (Fix at "1" when SVDDT is output.)
					IOC20	0	Output	Input	P20 I/O control register (Fix at "1" when TOUT is output.)
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-down control register (Fix at "0" when ISOR1 is output.)
					PUL22	1	On	Off	P22 pull-down control register (Fix at "0" when VCWON is output.)
	R/W				PUL21	1	On	Off	P21 pull-down control register (Fix at "0" when SVDDT is output.)
					PUL20	1	On	Off	P20 pull-down control register (Fix at "0" when TOUT is output.)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

Table 4.5.6.1(b) Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P23 I/O port data (Fix at "0" when ISOR1 is output.)
					P22	– *2	High	Low	P22 I/O port data (Fix at "0" when VCWON is output.)
					P21	– *2	High	Low	P21 I/O port data (Fix at "0" when SVDDT is output.)
	R/W				P20	– *2	High	Low	P20 I/O port data (Fix at "0" when TOUT is output.)
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	1	Output	Input	P33 I/O control register (Fix at "1" when F16HZ is output.)
					IOC32	1	Output	Input	P32 I/O control register (Fix at "1" when CLIM is output.)
					IOC31	1	Output	Input	P31 I/O control register (Fix at "1" when ISOR2 is output.)
	R/W				IOC30	1	Output	Input	P30 I/O control register (Fix at "1" when ISOR3 is output.)
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	0	On	Off	P33 pull-down control register (Fix at "0" when F16HZ is output.)
					PUL32	0	On	Off	P32 pull-down control register (Fix at "0" when CLIM is output.)
					PUL31	0	On	Off	P31 pull-down control register (Fix at "0" when ISOR2 is output.)
	R/W				PUL30	0	On	Off	P30 pull-down control register (Fix at "0" when ISOR3 is output.)
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P33 I/O port data (Fix at "0" when F16HZ is output.)
					P32	– *2	High	Low	P32 I/O port data (Fix at "0" when CLIM is output.)
					P31	– *2	High	Low	P31 I/O port data (Fix at "0" when ISOR2 is output.)
	R/W				P30	– *2	High	Low	P30 I/O port data (Fix at "0" when ISOR3 is output.)
FF05H	SVDS3	ESVDDT	SVDDT	SVDON	SVDS3	0	1	0	General-purpose register
					ESVDDT	0	Enable	Disable	SVDDT monitor output enable (P21)
	R/W		R	R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable (P41)
					SWDIR	0			Stopwatch direct input switch 0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1 FOFQ0	0 0			FOUT frequency selection [FOFQ1, 0] 0: Frequency fOSC1/64; 1: fOSC1/8; 2: fOSC1; 3: fOSC3
FF09H	ENISOR3	ENISOR2	E16HZ	0	ENISOR3	0	Enable	Disable	ISOR3 monitor output enable (P30)
					ENISOR2	0	Enable	Disable	ISOR2 monitor output enable (P31)
	R/W			R	E16HZ	0	Enable	Disable	F16HZ clock output enable (P33)
					0 *3	– *2			Unused
FF2DH	ENISOR1	ECLIM	CLIM	K30	ENISOR1	0	Enable	Disable	ISOR1 monitor output enable (P23)
					ECLIM	0	Enable	Disable	CLIM monitor output enable (P32)
	R/W		R		CLIM	0	On	Off	Limit level monitor
					K30	– *2	High	Low	K30 input port data
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable (P40)
FF6DH	EMPON	BZSTP	BZSHT	SHTPW	EMPON	0	Enable	Disable	Buzzer output enable in motor pulse output period
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R/W	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF88H	0	0	EVCWON	VCWON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EVCWON	0	Enable	Disable	VCWON monitor output enable (P22)
					VCWON	0	On	Off	Theoretical regulation status/trigger (Writing "0" is ineffective.)
FFC1H	0	CHSEL1	CHSEL0	PTOUT	0 *3	– *2			Unused
					CHSEL1	0			TOUT output selection [CHSEL1,0] 0: Timer; 1: Timer 0; 2: Timer 1; Timer 2
	R	R/W			CHSEL0	0			
					PTOUT	0	On	Off	TOUT output control (P20)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

(1) Selection of port function

ESIF: Serial interface enable register (FF70H•D0)
Selects function for P10–P13.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P10–P13 are used as the I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS1 and SCS0 registers (see Section 4.10).
In the slave mode, all the P10–P13 ports are set to the serial interface input/output port. In the master mode, P10–P12 are set to the serial interface input/output port and P13 can be used as the I/O port. Furthermore, when the SOUT terminal is disabled (ESOUT = "0"), P11 can be used as the I/O port.
At initial reset, this register is set to "0".

(2) I/O port control

P00–P03: P0 I/O port data register (FF42H)
P10–P13: P1 I/O port data register (FF46H)
P20–P23: P2 I/O port data register (FF4AH)
P30–P33: P3 I/O port data register (FF4EH)
P40–P41: P4 I/O port data register (FF32H•D0–D1)
I/O port data can be read and output data can be set through these registers.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When "with pull-down resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-down resistor goes on during input mode, so that the I/O port terminal is pulled down.

The data registers of the port, which are set for the input/output of the serial interface (P10–P13), become general-purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 300 kΩ (Max.)

IOC00–IOC03: P0 port I/O control register (FF40H)
IOC10–IOC13: P1 port I/O control register (FF44H)
IOC20–IOC23: P2 port I/O control register (FF48H)
IOC30–IOC33: P3 port I/O control register (FF4CH)
IOC40–IOC41: P4 port I/O control register (FF30H•D0–D1)
The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, the IOC00–IOC03, IOC10–IOC13 and IOC20–IOC23 registers are set to "0", so the P0, P1 and P2 I/O ports enter in input mode. The IOC30–IOC33 and IOC40–IOC41 registers are set to "1" for setting the P3 and P4 I/O ports in output mode.
The I/O control registers of the port, which are set for the input/output of the serial interface (P10–P13), become general-purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-down control register (FF41H)
PUL10–PUL13: P1 port pull-down control register (FF45H)
PUL20–PUL23: P2 port pull-down control register (FF49H)
PUL30–PUL33: P3 port pull-down control register (FF4DH)
PUL40–PUL41: P4 port pull-down control register (FF31H•D0–D1)
The pull-down during input mode are set with these registers.

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

The built-in pull-down resistor which is turned on during input mode is set to enable in 1-bit units. (The pull-down resistor is included into the ports selected by mask option.)
By writing "1" to the pull-down control register, the corresponding I/O ports are pulled down (during input mode), while writing "0" disables the pull-down function.
At initial reset, the PUL00–PUL03, PUL10–PUL13 and PUL20–PUL23 registers are set to "1", so the P0, P1 and P2 port pull-down resistors are enabled. The PUL30–PUL33 and PUL40–PUL41 registers are set to "0" for disabling the P3 and P4 port pull-down resistors.

The pull-down control registers of the ports in which the pull-down resistor is not included become the general purpose register. The registers of the ports that are set as output for the serial interface can also be used as general purpose registers that do not affect the pull-down control.
The pull-down control registers of the port that are set as input for the serial interface and special outputs function the same as the I/O port.

(3) Special output control

Note: When using the Pxx port as the special output port, fix the I/O control register (IOCxx) at "1" (output), data register (Pxx) at "0" and the pull-down control register (PULxx) at "0" (pull-down disabled).

ESVDDT: SVDDT monitor output enable register (FF05H•D2)
Controls the SVDDT output.

When "1" is written: SVDDT output On
When "0" is written: SVDDT output Off
Reading: Valid

By writing "1" to the ESVDDT register, the SVDDT signal (supply voltage detection data) is output from the P21 terminal. When "0" is written, the P21 terminal goes low (V_{SS}).
At initial reset, this register is set to "0".

E16HZ: F16HZ output enable register (FF09H•D1)
Controls the F16HZ output.

When "1" is written: F16HZ output On
When "0" is written: F16HZ output Off
Reading: Valid

By writing "1" to the E16HZ register, the F16HZ signal is output from the P33 terminal. When "0" is written, the P33 terminal goes low (VSS).
At initial reset, this register is set to "0".
At initial reset, this register is set to "0".

ENISOR3: ISOR3 monitor output enable register (FF09H•D3)
Controls the ISOR3 output.

When "1" is written: ISOR3 output On
When "0" is written: ISOR3 output Off
Reading: Valid

By writing "1" to the ENISOR3 register, the ISOR3 signal (quick start mode flag 1 status) is output from the P30 terminal. When "0" is written, the P30 terminal goes low (VSS).
At initial reset, this register is set to "0".

ENISOR2: ISOR2 monitor output enable register (FF09H•D2)
Controls the ISOR2 output.

When "1" is written: ISOR2 output On
When "0" is written: ISOR2 output Off
Reading: Valid

By writing "1" to the ENISOR2 register, the ISOR2 signal (quick start mode flag 2 status) is output from the P31 terminal. When "0" is written, the P31 terminal goes low (VSS).

ENISOR1: ISOR1 monitor output enable register (FF2DH•D3)
Controls the ISOR1 output.

When "1" is written: ISOR1 output On
When "0" is written: ISOR1 output Off
Reading: Valid

By writing "1" to the ENISOR1 register, the ISOR1 signal (recharging flag status) is output from the P23 terminal. When "0" is written, the P23 terminal goes low (VSS).
At initial reset, this register is set to "0".

ECLIM: CLIM monitor output enable register (FF2DH•D2)
Controls the CLIM output.

When "1" is written: CLIM output On
When "0" is written: CLIM output Off
Reading: Valid

By writing "1" to the ECLIM register, the CLIM signal (solar recharging limiter status) is output from the P32 terminal. When "0" is written, the P32 terminal goes low (VSS).
At initial reset, this register is set to "0".

EVCWON: VCWON monitor output enable register (FF88H•D1)

Controls the VCWON write signal monitor output.

When "1" is written: VCWON output On
When "0" is written: VCWON output Off
Reading: Valid

By writing "1" to the EVCWON register, the VCWON write signal is output from the P22 terminal. When "0" is written, the P22 terminal goes low (VSS).
At initial reset, this register is set to "0".

BZE: Buzzer output control register (FF6CH•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the P40 terminal. When "0" is written, the P40 terminal goes to low (VSS).
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF6DH•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output from the P40 terminal.
This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***When reading***

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".
At initial reset, this bit is set to "0".

FOUTE: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output On
When "0" is written: FOUT output Off
Reading: Valid

By writing "1" to the FOUTE register, the FOUT signal is output from the P41 terminal. When "0" is written, the P41 terminal goes low (VSS).
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)
Selects a frequency of the FOUT signal.

Table 4.5.6.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D0)
Controls the TOUT output.

When "1" is written: TOUT output On
When "0" is written: TOUT output Off
Reading: Valid

By writing "1" to the PTOUT register, the TOUT signal is output from the P20 terminal. When "0" is written, the P20 terminal goes low (V_{SS}).
At initial reset, this register is set to "0".

4.5.7 Programming notes

(1) When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 300 kΩ (Max.)

(2) The data register, I/O control register and pull-down control register are effective even if the Pxx is used for special output. To prevent the occurrence of undesired terminal conditions, do not change the register values after setting the data register (Pxx) to "0", the I/O control register (IOCxx) to "1", and the pull-down control register (PULxx) to "0".

(3) A hazard may occur when the FOUT, TOUT or F16HZ signal is turned on and off.

(4) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

4.6 LCD Driver (COM0–COM7, SEG0–SEG63)

4.6.1 Configuration of LCD driver

The S1C63709 has 8 common terminals (COM0–COM7) and 64 segment terminals (SEG0–SEG63), so that it can drive an LCD with a maximum of 512 (64 × 8) segments. The driving method is 1/4 duty, 1/5 duty or 1/8 duty dynamic drive with three voltages (1/3 bias), V_{C1}, V_{C2} and V_{C3}.
LCD display on/off can be controlled by the software.

4.6.2 Power supply for LCD driving

The power supply for driving LCD can be selected from the internal power supply and an external power supply.

When the internal power supply is selected, the LCD drive voltages V_{C1}–V_{C3} are generated by the built-in LCD system voltage circuit. The LCD system voltage circuit is turned on and off using the LPWR register. When LPWR is set to "1", the LCD system voltage circuit outputs the LCD drive voltages V_{C1}–V_{C3} to the LCD driver. The LCD system voltage circuit generates V_{C1} or V_{C2} with the voltage regulator built-in, and generates two other voltages by boosting or halving V_{C1} or V_{C2}. Table 4.6.2.1 shows the V_{C1}, V_{C2} and V_{C3} voltage boosting/halving status.

Table 4.6.2.1 LCD drive voltage when generated internally

LCD drive voltage	V_{C1} regulator	V_{C2} regulator
V_{C1}	V_{C1} (constant voltage)	$1/2 \times V_{C2}$
V_{C2}	$2 \times V_{C1}$	V_{C2} (constant voltage)
V_{C3}	$3 \times V_{C1}$	$3/2 \times V_{C2}$

Note: The LCD drive voltage can be adjusted by the software (see Section 4.6.6).
When V_{C2} regulator is selected, the operating voltage range is changed to 2.1–3.6 V.

A mask option is provided to select either V_{C1} regulator or V_{C2} regulator.

When using an external power supply, select the voltage from the following 3 types and supply the LCD drive voltage to the V_{C1}–V_{C3} terminals.
1) External power supply 1/3 bias (for 4.5 V panel) $V_{DD} = V_{C2}$
2) External power supply 1/3 bias (for 3.0 V panel) $V_{DD} = V_{C3}$
3) External power supply 1/2 bias (for 3.0 V panel) $V_{DD} = V_{C3}$, $V_{C1} = V_{C2}$ (static drive function is available)

Note that the power control using the LPWR register is necessary even if an external power supply is used. SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power on/off control by the LPWR register.

4.6.3 Control of LCD display and drive waveform

(1) Display on/off control

The S1C63709 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the segments go on, and when "1" is written to ALOFF, all the segments go off. At such a time, an on waveform or an off waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all on) has priority over the ALOFF (all off).

(2) Setting of drive duty

In the S1C63709, the drive duty can be set to 1/4, 1/5 or 1/8 using the LDUTY1 and LDUTY0 registers as shown in Table 4.6.3.1.

Table 4.6.3.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/8	COM0–COM7	512 (64 × 8)
0	1	1/5	COM0–COM4	320 (64 × 5)
0	0	1/4	COM0–COM3	256 (64 × 4)

The frame frequency can be set to 25.6 Hz or 32 Hz using the LCFCHG register as shown in Table 4.6.3.2. However, it is fixed at 25.6 Hz when 1/5 duty is selected.

Table 4.6.3.2 Frame frequency

LCFCHG	1/8 duty	1/5 duty	1/4 duty
1	25.6 Hz	25.6 Hz	25.6 Hz
0	32 Hz	25.6 Hz	32 Hz

Note: Be sure to turn the LCD power off before the frame frequency can be switched.

Figures 4.6.3.1 to 4.6.3.3 show the dynamic drive waveform according to the duty.

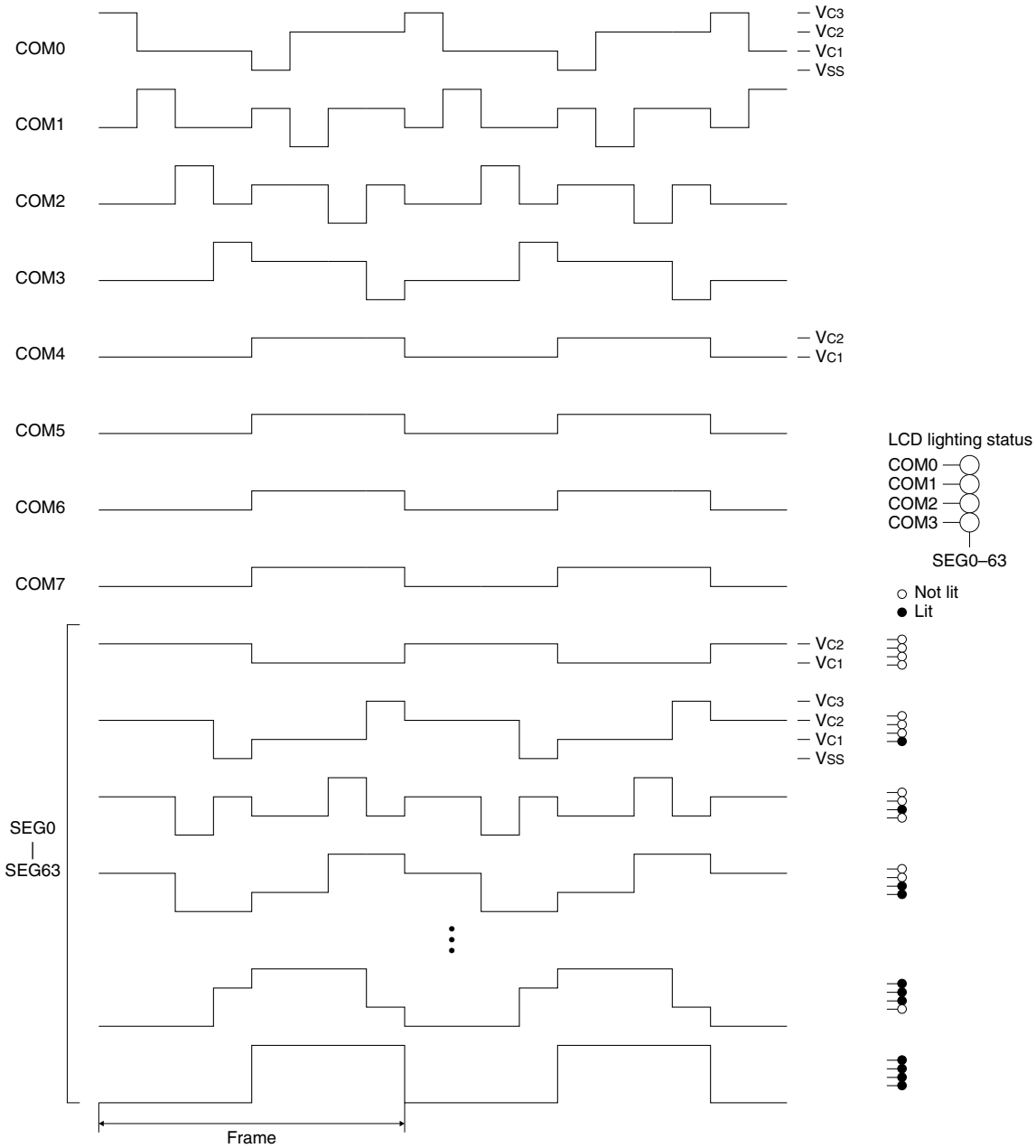


Fig. 4.6.3.1 Dynamic drive waveform for 1/4 duty

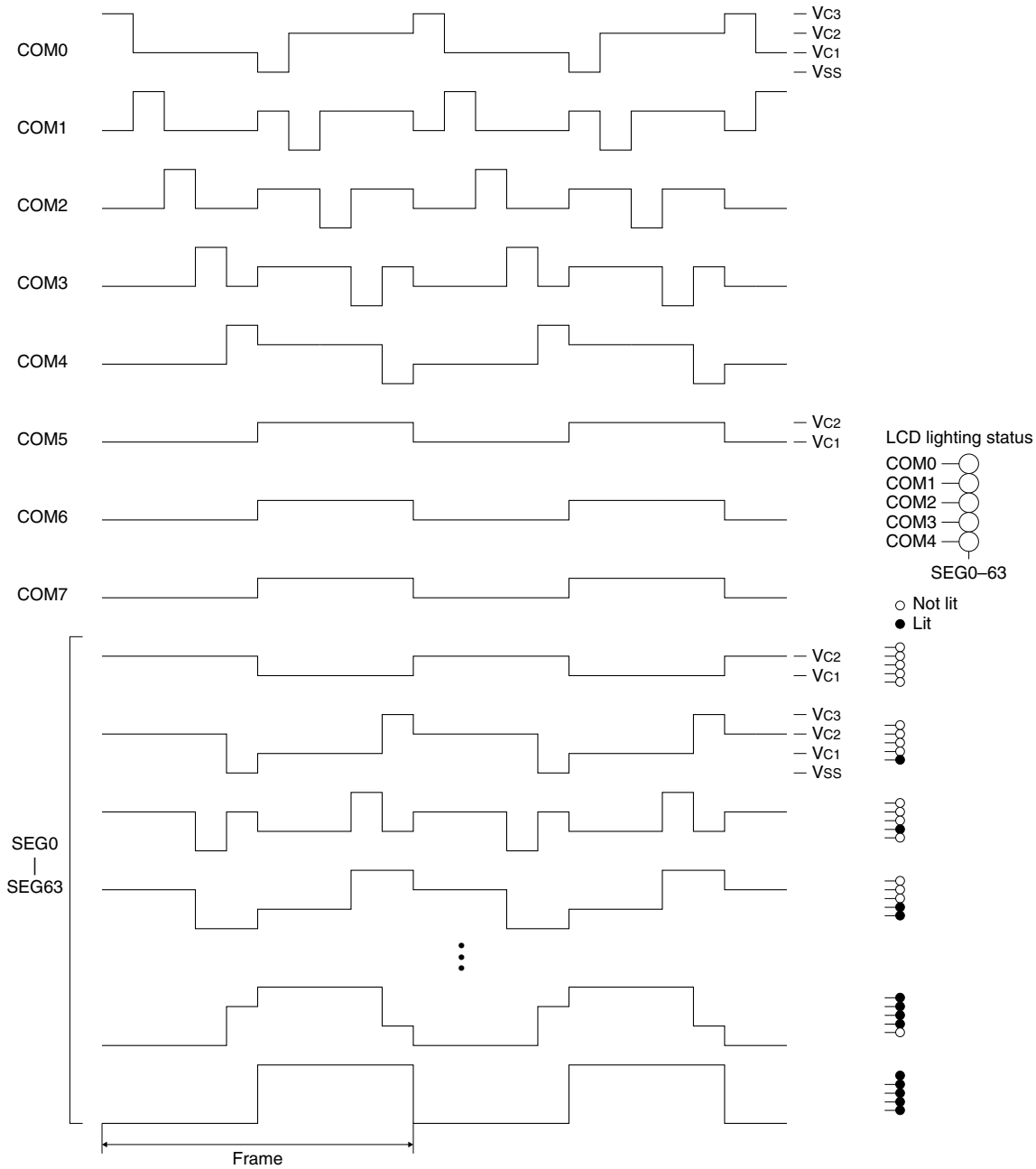


Fig. 4.6.3.2 Dynamic drive waveform for 1/5 duty

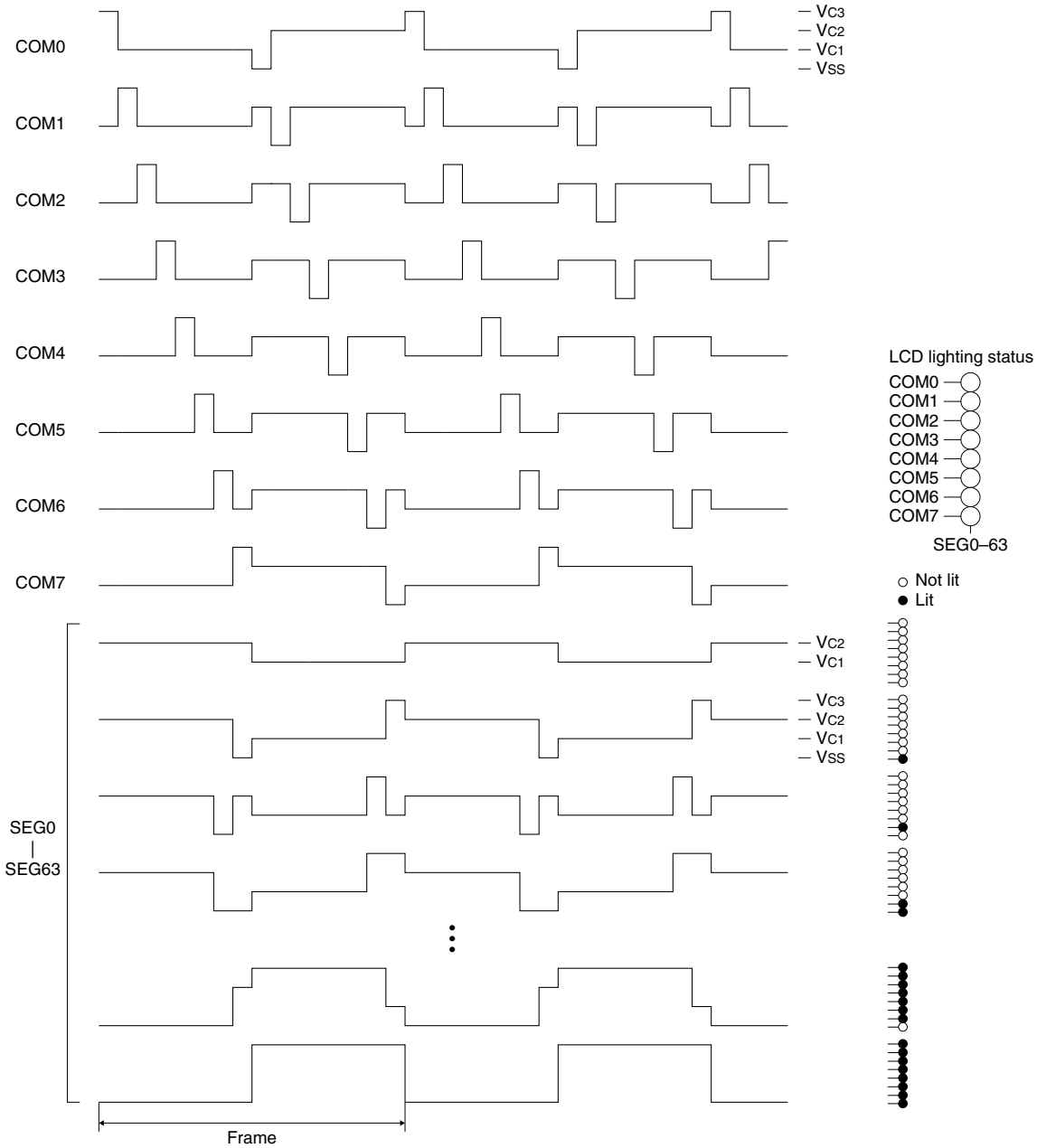


Fig. 4.6.3.3 Dynamic drive waveform for 1/8 duty

(3) Static drive

The S1C63709 provides software setting of the LCD static drive. However, this function is available only when "External power supply 1/2 bias (for 3.0 V panel)" is selected by mask option.
To set in static drive, write "1" to the common output signal control register STCD. Then, by writing "1" to any one of COM0 to COM7 (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static on waveform. When all the COM0 to COM7 bits are set to "0", the SEG terminal outputs a dynamic off waveform.
Figure 4.6.3.4 shows the static drive waveform.

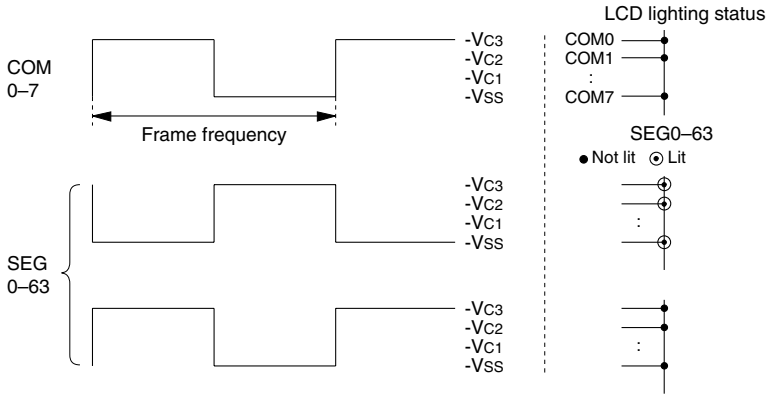


Fig. 4.6.3.4 Static drive waveform

Note: To use the static drive function, select the "External power supply 1/2 bias (for 3.0 V panel)" mask option. When an option for using the internal power supply or a 1/3 bias external power supply is selected, static drive cannot be set using the STCD register.

4.6.4 Display memory

The display memory is allocated to F000H–F09FH in the data memory area and each data bit can be allocated to an segment terminal (SEG0–SEG63) by mask option.
When a bit in the display memory is set to "1", the corresponding LCD segment goes on, and when it is set to "0", the segment goes off.
At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.
The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

4.6.5 Segment option

Segment allocation

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F09FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
Figure 4.6.5.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/4 duty.

Address	Data			
	D3	D2	D1	D0
F060H	d	c	b	a
F061H	p	g	f	e

Display memory allocation

	Common 0	Common 1	Common 2	Common 3
SEG10	61, D1 (f)	61, D0 (e)	60, D2 (c)	60, D3 (d)
SEG11	60, D0 (a)	61, D2 (g)	60, D1 (b)	61, D3 (p)

Pin address allocation

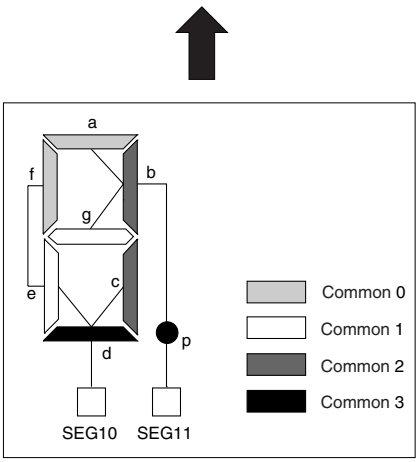


Fig. 4.6.5.1 Segment allocation

Output specification

1. The segment terminals (SEG0–SEG63) can be selected with the mask option in pairs* for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
   When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
2. When DC output is selected, either complementary output or N-channel open drain output can be selected for each terminal with the mask option.

   * The terminal pairs are combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 31).

Segment option list

Pin name	Address (F0xx)																								Output specification
	COM0			COM1			COM2			COM3			COM4			COM5			COM6			COM7			
	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	H	L	D	
SEG0																									SEG output ☐S
SEG1																									DC output ☐C ☐N
SEG2																									SEG output ☐S
SEG3																									DC output ☐C ☐N
SEG4																									SEG output ☐S
SEG5																									DC output ☐C ☐N
SEG6																									SEG output ☐S
SEG7																									DC output ☐C ☐N
SEG8																									SEG output ☐S
SEG9																									DC output ☐C ☐N
SEG10																									SEG output ☐S
SEG11																									DC output ☐C ☐N
SEG12																									SEG output ☐S
SEG13																									DC output ☐C ☐N
SEG14																									SEG output ☐S
SEG15																									DC output ☐C ☐N
SEG16																									SEG output ☐S
SEG17																									DC output ☐C ☐N
SEG18																									SEG output ☐S
SEG19																									DC output ☐C ☐N
SEG20																									SEG output ☐S
SEG21																									DC output ☐C ☐N
SEG22																									SEG output ☐S
SEG23																									DC output ☐C ☐N
SEG24																									SEG output ☐S
SEG25																									DC output ☐C ☐N
SEG26																									SEG output ☐S
SEG27																									DC output ☐C ☐N
SEG28																									SEG output ☐S
SEG29																									DC output ☐C ☐N
SEG30																									SEG output ☐S
SEG31																									DC output ☐C ☐N
SEG32																									SEG output ☐S
SEG33																									DC output ☐C ☐N
SEG34																									SEG output ☐S
SEG35																									DC output ☐C ☐N
SEG36																									SEG output ☐S
SEG37																									DC output ☐C ☐N
SEG38																									SEG output ☐S
SEG39																									DC output ☐C ☐N
SEG40																									SEG output ☐S
SEG41																									DC output ☐C ☐N
SEG42																									SEG output ☐S
SEG43																									DC output ☐C ☐N
SEG44																									SEG output ☐S
SEG45																									DC output ☐C ☐N
SEG46																									SEG output ☐S
SEG47																									DC output ☐C ☐N
SEG48																									SEG output ☐S
SEG49																									DC output ☐C ☐N
SEG50																									SEG output ☐S
SEG51																									DC output ☐C ☐N
SEG52																									SEG output ☐S
SEG53																									DC output ☐C ☐N
SEG54																									SEG output ☐S
SEG55																									DC output ☐C ☐N
SEG56																									SEG output ☐S
SEG57																									DC output ☐C ☐N
SEG58																									SEG output ☐S
SEG59																									DC output ☐C ☐N
SEG60																									SEG output ☐S
SEG61																									DC output ☐C ☐N
SEG62																									SEG output ☐S
SEG63																									DC output ☐C ☐N

<address> H: RAM data high-order address (0–9)
L: RAM data low-order address (0–F)
D: Data bit (0–3)

<Output specification> S: Segment output
C: Complementary output
N: Nch open drain output

4.6.6 LCD contrast adjustment

In the S1C63709, the LCD contrast can be adjusted by the software.
It is realized by controlling the voltages V_{C1}, V_{C2} and V_{C3} output from the LCD system voltage circuit.
The contrast can be adjusted to 16 levels as shown in Table 4.6.6.1.
When V_{C1} regulator is selected by mask option, the V_{C1} value varies within the range from 1.07 V to 1.41 V according to the register setting. When V_{C2} regulator is selected by mask option, the V_{C2} value varies within the range from 2.08 V to 2.84 V. For the voltage value, refer to Chapter 7, "Electrical Characteristics".

Table 4.6.6.1 LCD contrast

No.	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	↓
15	1	1	1	1	dark

At initial reset, the LC0–LC3 are set to 0000B. The software should initialize the register to get the desired contrast.
When an external power supply is selected by mask option, the LC0–LC3 register becomes invalid.

Notes:
- *To attain correct contrast, supply the V_{DD} voltage higher than the V_{C1} or V_{C2} value when the LC0–LC3 register is set to 15 (Max.).*
- *Use a 3.0 V LCD panel when the internal LCD power supply is enabled by mask option. When using an LCD panel with different specifications, perform a matching evaluation for the panel to determine whether it can be used or not.*

4.6.7 I/O memory of LCD driver

Table 4.6.7.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.6.7.1 shows the display memory map.

Table 4.6.7.1 Control bits of LCD driver

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF60H	LDUTY1	LDUTY0	STCD	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0]: 0 = Duty 1/4, 1 = Duty 1/5, 2, 3 = Duty 1/8
					LDUTY0	0			
	R/W				STCD	0	Static	Dynamic	LCD drive switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	LCFCHG	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all Off control
	R	R/W			ALON	0	All On	Normal	LCD all On control
					LCFCHG	0	25.6 Hz	32 Hz	Frame frequency selection (when 1/4 or 1/8 duty is selected)
FF62H	LC3	LC2	LC1	LC0	LC3	0			LCD contrast adjustment [LC3–0]: 0 = Contrast Light, 15 = Contrast Dark
					LC2	0			
	R/W				LC1	0			
					LC0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Address Base \ Low	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000H	Display memory (160 words × 4 bits) R/W															
F010H																
F020H																
F030H																
F040H																
F050H																
F060H																
F070H																
F080H																
F090H																

Fig. 4.6.7.1 Display memory map

LPWR: LCD power control (on/off) register (FF60H•D0)

Turns the LCD system voltage circuit on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes on and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to VSS level.
It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.6.7.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/8	COM0–COM7	512 (64 × 8)
0	1	1/5	COM0–COM4	320 (64 × 5)
0	0	1/4	COM0–COM3	256 (64 × 4)

At initial reset, this register is set to "0".

STCD: LCD drive switch register (FF60H•D1)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0".

LCFCHG: Frame frequency selection register (FF61H•D0)

Selects the frame frequency (when 1/4 or 1/8 duty is selected).

When "1" is written: 25.6 Hz
When "0" is written: 32 Hz
Reading: Valid

By writing "1" to LCFCHG, the frame frequency is set to 25.6 Hz. When "0" is written, the frame frequency is set to 32 Hz. However, it is fixed at 25.6 Hz regardless of the register value when 1/5 duty is selected.
At initial reset, this register is set to "0".

ALON: LCD all on control register (FF61H•D1)

Displays the all LCD segments on.

When "1" is written: All LCD segments displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALON register, all the LCD segments go on, and when "0" is written, it returns to normal display. This function outputs an on waveform to the SEG terminals, and segments not affect the content of the display memory. ALON has priority over ALOFF.
At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALOFF register, all the LCD segments go off, and when "0" is written, it returns to normal display. This function outputs an off waveform to the SEG terminals, and does not affect the content of the display memory.
ALON (FF61H•D1) has priority over ALOFF, so all the LCD segments go on when ALON and ALOFF are set to "1" simultaneously.
At initial reset, this register is set to "1".

LC3–LC0: LCD contrast adjustment register (FF62H)

Adjusts the LCD contrast.

LC3–LC0 = 0000B light
: :
LC3–LC0 = 1111B dark

When the LCD drive voltage is supplied from outside by mask option selection, this adjustment becomes invalid.
At initial reset, LC0–LC3 is set to 0000B.

4.6.8 Programming note

Because at initial reset, the contents of display memory are undefined and LC3–LC0 (LCD contrast) is set to 0000B, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes off.

4.7 Clock Timer

4.7.1 Configuration of clock timer

The S1C63709 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.7.1.1 is the block diagram for the clock timer.

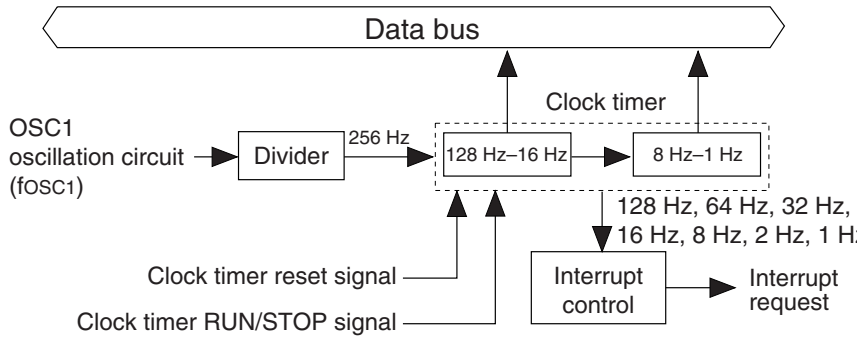


Fig. 4.7.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.7.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF75H and FF76H.

<FF75H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF76H>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the S1C63709 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.7.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 128 Hz, 64 Hz, 32 Hz, 16 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.7.3.1 is the timing chart of the clock timer.

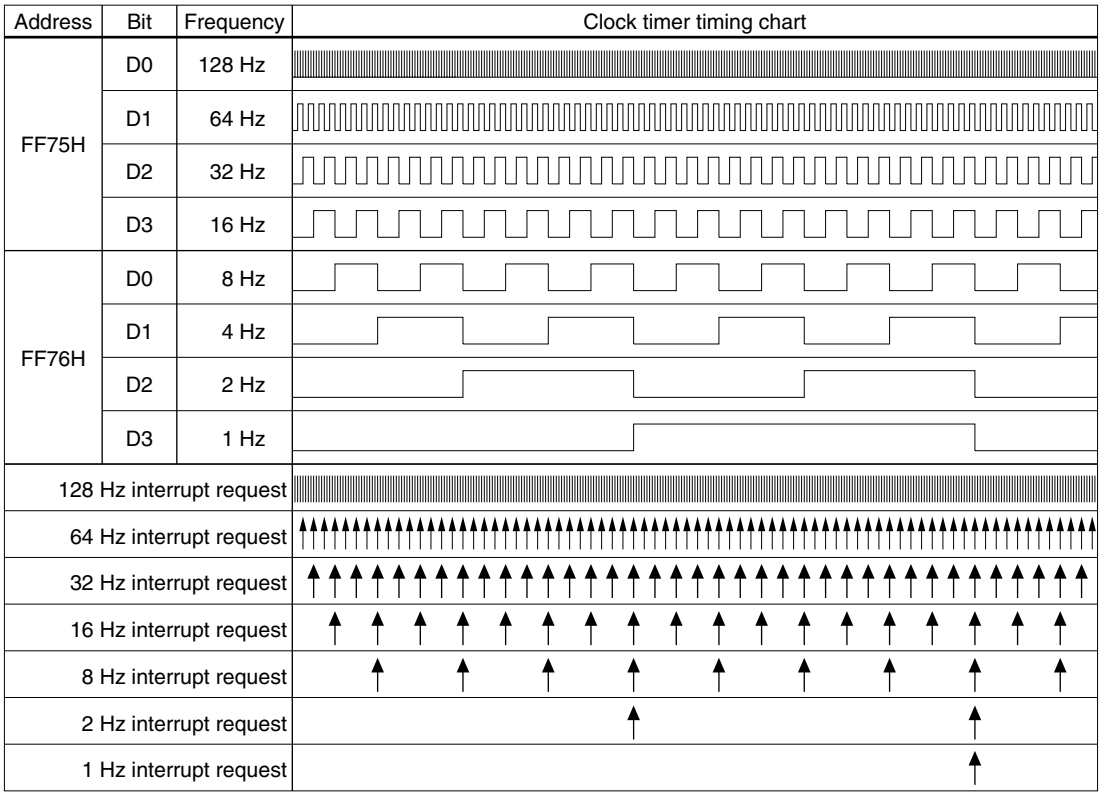


Fig. 4.7.3.1 Timing chart of clock timer

As shown in Figure 4.7.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz, 16 Hz, 64 Hz, 128 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3, IT4, IT5, IT6) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3, EIT4, EIT5, EIT6). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.7.4 I/O memory of clock timer

Table 4.7.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.7.4.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF74H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF75H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF76H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE9H	0	EIT6	EIT5	EIT4	0 *3	– *2			Unused
					EIT6	0	Enable	Mask	Interrupt mask register (Clock timer 128 Hz)
	R	R/W			EIT5	0	Enable	Mask	Interrupt mask register (Clock timer 64 Hz)
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF9H	0	IT6	IT5	IT4	0 *3	– *2	(R)	(R)	Unused
					IT6	0	Yes	No	Interrupt factor flag (Clock timer 128 Hz)
	R	R/W			IT5	0	(W)	(W)	Interrupt factor flag (Clock timer 64 Hz)
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF75H, FF76H)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF75H), the high-order data (FF76H) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF74H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF74H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0: 32 Hz interrupt mask register (FFE5H•D0)
EIT1: 8 Hz interrupt mask register (FFE5H•D1)
EIT2: 2 Hz interrupt mask register (FFE5H•D2)
EIT3: 1 Hz interrupt mask register (FFE5H•D3)
EIT4: 16 Hz interrupt mask register (FFE9H•D0)
EIT5: 64 Hz interrupt mask register (FFE9H•D1)
EIT6: 128 Hz interrupt mask register (FFE9H•D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3, EIT4, EIT5, EIT6) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz, 16 Hz, 64 Hz, 128 Hz).
At initial reset, these registers are set to "0".

IT0: 32 Hz interrupt factor flag (FFF5H•D0)
IT1: 8 Hz interrupt factor flag (FFF5H•D1)
IT2: 2 Hz interrupt factor flag (FFF5H•D2)
IT3: 1 Hz interrupt factor flag (FFF5H•D3)
IT4: 16 Hz interrupt factor flag (FFF9H•D0)
IT5: 64 Hz interrupt factor flag (FFF9H•D1)
IT6: 128 Hz interrupt factor flag (FFF9H•D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3, IT4, IT5, IT6) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz, 16 Hz, 64 Hz, 128 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.7.5 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.8 Stopwatch Timer

4.8.1 Configuration of stopwatch timer

The S1C63709 has a 1/1,000 sec stopwatch timer. The stopwatch timer is configured of a 3-stage, 4-bit BCD counter serving as the input clock of a 1,000 Hz signal output from the prescaler. Data can be read out four bits (1/1,000 sec, 1/100 sec and 1/10 sec) at a time by the software.
In addition it has a direct input function that controls the stopwatch timer RUN/STOP and LAP using the input ports K00 and K01.
Figure 4.8.1.1 is the block diagram of the stopwatch timer.

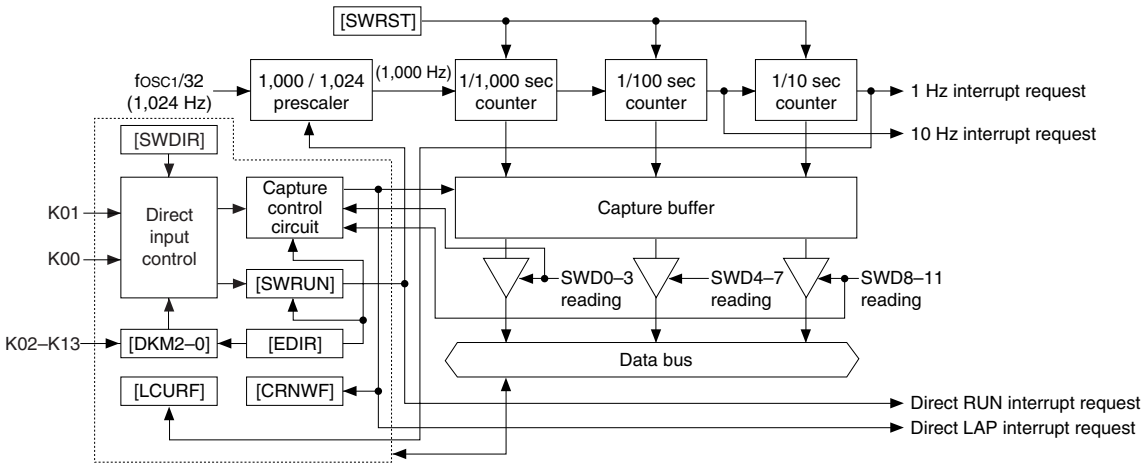


Fig. 4.8.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

4.8.2 Counter and prescaler

The stopwatch timer is configured of four-bit BCD counters SWD0–3, SWD4–7 and SWD8–11.
The counter SWD0–3, at the stage preceding the stopwatch timer, has a 1,000 Hz signal generated by the prescaler for the input clock. It counts up every 1/1,000 sec, and generates 100 Hz signal. The counter SWD4–7 has a 100 Hz signal generated by the counter SWD0–3 for the input clock. It count-up every 1/100 sec, and generated 10 Hz signal. The counter SWD8–11 has an approximated 10 Hz signal generated by the counter SWD4–7 for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.

The prescaler inputs a 1,024 Hz clock dividing fOSC1 (output from the OSC1 oscillation circuit), and outputs 1,000 Hz counting clock for SWD0–3. To generate a 1,000 Hz clock from 1,024 Hz, 24 pulses from 1,024 pulses that are input to the prescaler every second are taken out.
When the counter becomes the value indicated below, one pulse (1,024 Hz) that is input immediately after to the prescaler will be pulled out.

<Counter value (msec) in which the pulse correction is performed>
39, 79, 139, 179, 219, 259, 299, 319, 359, 399, 439, 479, 539, 579, 619, 659, 699, 719, 759, 799, 839, 879, 939, 979

Figure 4.8.2.1 shows the operation of the prescaler.

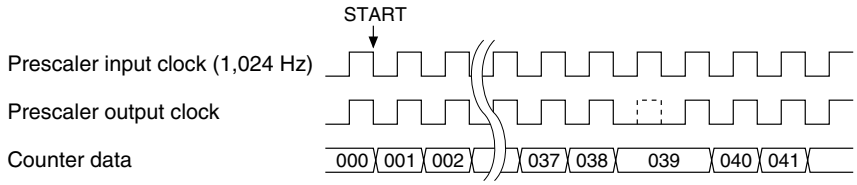


Fig. 4.8.2.1 Timing of the prescaler operation

For the above reason, the counting clock is 1,024 Hz (0.9765625 msec) except during pulse correction. Consequently, frequency of the prescaler output clock (1,000 Hz), 100 Hz generated by SWD0–3 and 10 Hz generated by SWD4–7 are approximate values.

4.8.3 Capture buffer and hold function

The stopwatch data, 1/1,000 sec, 1/100 sec and 1/10 sec, can be read from SWD0–3 (FF7AH), SWD4–7 (FF7BH) and SWD8–11 (FF7CH), respectively. The counter data are latched in the capture buffer when reading, and are held until reading of three words is completed. For this reason, correct data can be read even when a carry from lower digits occurs during reading the three words. Further, three counter data are latched in the capture buffer at the same time when SWD0–3 (1/1,000 sec) is read. The data hold is released when SWD8–11 (1/10 sec) reading is completed. Therefore, data should be read in order of SWD0–3 → SWD4–7 → SWD8–11. If SWD4–7 or SWD8–11 is first read when data have not been held, the hold function does not work and data in the counter is directly read out. When data that has not been held is read in the stopwatch timer RUN status, you cannot judge whether it is correct or not.

The stopwatch timer has a LAP function using an external key input (explained later). The capture buffer is also used to hold LAP data. In this case, data is held until SWD8–11 is read. However, when a LAP input is performed before completing the reading, the content of the capture buffer is renewed at that point. Remaining data that have not been read become invalid by the renewal, and the hold status is not released if SWD8–11 is read. When SWD8–11 is read after the capture buffer is updated, the capture renewal flag is set to "1" at that point. In this case, it is necessary to read from SWD0–3 again. The capture renewal flag is renewed by reading SWD8–11.

Figure 4.8.3.1 shows the timing for data holding and reading.

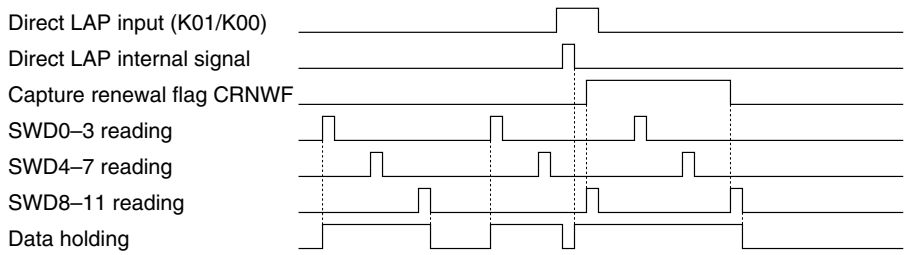


Fig. 4.8.3.1 Timing for data holding and reading

4.8.4 Stopwatch timer RUN/STOP and reset

RUN/STOP control and reset of the stopwatch timer can be done by the software.

Stopwatch timer RUN/STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. The RUN/STOP operation of the stopwatch timer by writing to the SWRUN register is performed in synchronization with the falling edge of the 1,024 Hz same as the prescaler input clock. The SWRUN register can be read, and in this case it indicates the operating status of the stopwatch timer.

Figure 4.8.4.1 shows the operating timing when controlling the SWRUN register.

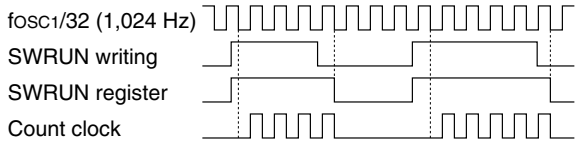


Fig. 4.8.4.1 Operating timing when controlling SWRUN

When the direct input function (explained in next section) is set, RUN/STOP control is done by an external key input. In this case, SWRUN becomes read only register that indicates the operating status of the stopwatch timer.

Stopwatch timer reset

The stopwatch timer is reset when "1" is written to SWRST. With this, the counter value is cleared to "000". Since this resetting does not affect the capture buffer, data that has been held in the capture buffer is not cleared and is maintained as is. When the stopwatch timer is reset in the RUN status, counting restarts from count "000". Also, in the STOP status the reset data "000" is maintained until the next RUN.

4.8.5 Direct input function and key mask

The stopwatch timer has a direct input function that can control the RUN/STOP and LAP operation of the stopwatch timer by external key input. This function is set by writing "1" to the EDIR register. When EDIR is set to "0", only the software control is possible as explained in the previous section.

Input port configuration

In the direct input function, the input ports K00 and K01 are used as the RUN/STOP and LAP input ports. The key assignment can be selected using the SWDIR register.

Table 4.8.5.1 RUN/STOP and LAP input ports

SWDIR	K00	K01
0	RUN/STOP	LAP
1	LAP	RUN/STOP

Direct RUN

When the direct input function is selected, RUN/STOP operation of the stopwatch timer can be controlled by using the key connected to the input port K00/K01 (selected by SWDIR). K00/K01 works as a normal input port, but the input signal is sent to the stopwatch control circuit. The key input signal from the K00/K01 port works as a toggle switch. When it is input in STOP status, the stopwatch timer runs, and in RUN status, the stopwatch timer stops. RUN/STOP status of the stopwatch timer can be checked by reading the SWRUN register. An interrupt is generated by direct RUN input.

The sampling for key input signal is performed at the falling edge of 1,024 Hz signal same as the SWRUN control. The chattering judgment is performed at the point where the key turns off, and a chattering less than 46.8–62.5 msec is removed. Therefore, more time is needed for an interval between RUN and STOP key inputs.

Figure 4.8.5.1 shows the operating timing for the direct RUN input.

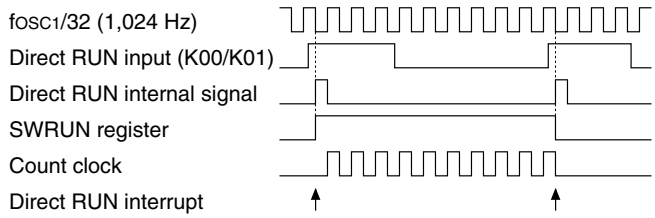


Fig. 4.8.5.1 Operating timing for direct RUN input

Direct LAP

Control for the LAP can also be done by key input same as the direct RUN. When the direct input function is selected, the input port K01/K00 (selected by SWDIR) becomes the LAP key input port. Sampling for the input signal and the chattering judgment are the same as a direct RUN.
By entering the LAP key, the counter data at that point is latched into the capture buffer and is held. The counter continues counting operation. Furthermore, an interrupt occurs by direct LAP input.
As stated above, the capture buffer data is held until SWD8–11 is read. If the LAP key is input when data has been already held, it renews the content of the capture buffer. When SWD8–11 is read after renewing, the capture renewal flag is set to "1". In this case, the hold status is not released by reading SWD8–11, and it continues. Normally the LAP data should be read after the interrupt is generated. After that, be sure to check the capture renewal flag. When the capture renewal flag is set, renewed data is held in the capture buffer. So it is necessary to read from SWD0–3 again.
The stopwatch timer sets the 1 Hz interrupt factor flag ISW1 to "1" when requiring a carry-up to 1-sec digit by an SWD8–11 overflow. If the capture buffer shifts into hold status (when SWD0–3 is read or when LAP is input) while the 1 Hz interrupt factor flag ISW1 is set to "1", the lap data carry-up request flag LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required for the processing of LAP input. In normal software processing, LAP processing may take precedence over 1-sec or higher digits processing by a 1 Hz interrupt, therefore carry-up processing using this flag should be used for time display in the LAP processing to prevent the 1-sec digit data decreasing by 1 second. This flag is renewed when the capture buffer shifts into hold status.
Figure 4.8.5.2 shows the operating timing for the direct LAP input, and Figure 4.8.5.3 shows the timings for data holding and reading during a direct LAP input and reading.

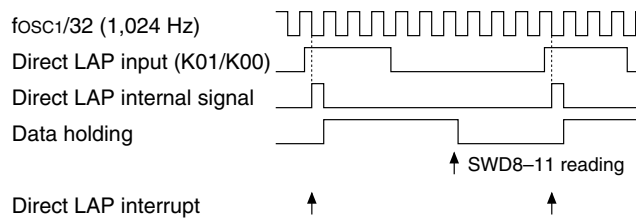


Fig. 4.8.5.2 Operating timing for direct LAP input

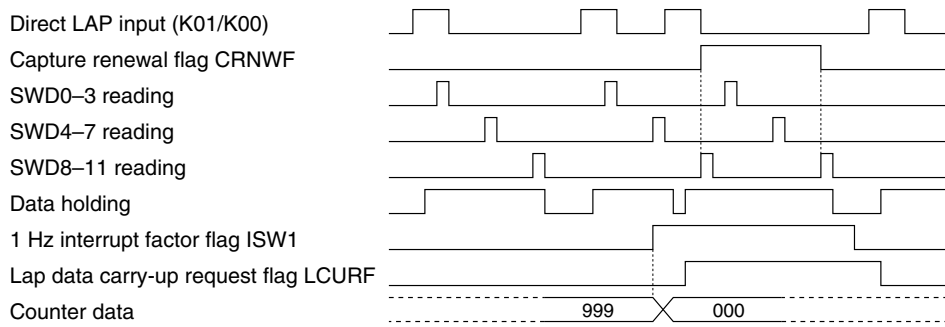


Fig. 4.8.5.3 Timing for data holding and reading during direct LAP input

Key mask

In stopwatch applications, some functions may be controlled by a combination of keys including direct RUN or direct LAP. For instance, the RUN key can be used for other functions, such as reset and setting a watch, by pressing the RUN key with another key. In this case, the direct RUN function or direct LAP function must be invalid so that it does not function. For this purpose, the key mask function is set so that it judges concurrence of input keys and invalidates RUN and LAP functions. A combination of the key inputs for this judgment can be selected using the DKM0–DKM2 registers.

Table 4.8.5.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

RUN or LAP inputs become invalid in the following status.

1. The RUN or LAP key is pressed when one or more keys that are included in the selected combination (here in after referred to as mask) are held down.
2. The RUN or LAP key has been pressed when the mask is released.

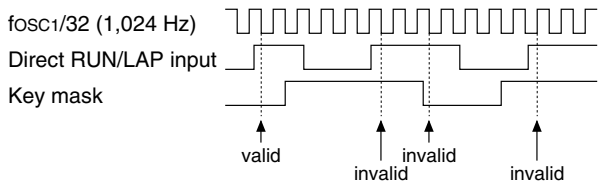


Fig. 4.8.5.4 Operation of key mask

RUN or LAP inputs become valid in the following status.

1. Either the RUN or LAP key is pressed independently if no other key is been held down.
2. Both the RUN and LAP keys are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)
3. The RUN or LAP key is pressed if either is held down. (RUN and LAP functions are effective.)
4. Either the RUN or LAP key and the mask key are pressed at the same time if no other key is held down.
5. Both the RUN and LAP keys and the mask key are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)

* Simultaneous key input is referred to as two or more key inputs are sampled at the same falling edge of 1,024 Hz clock.

4.8.6 Interrupt function

10 Hz and 1 Hz interrupts

The 10 Hz and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWD4–7 and SWD8–11 respectively. Also, software can set whether to separately mask the frequencies described earlier.

Figure 4.8.6.1 is the timing chart for the counters.

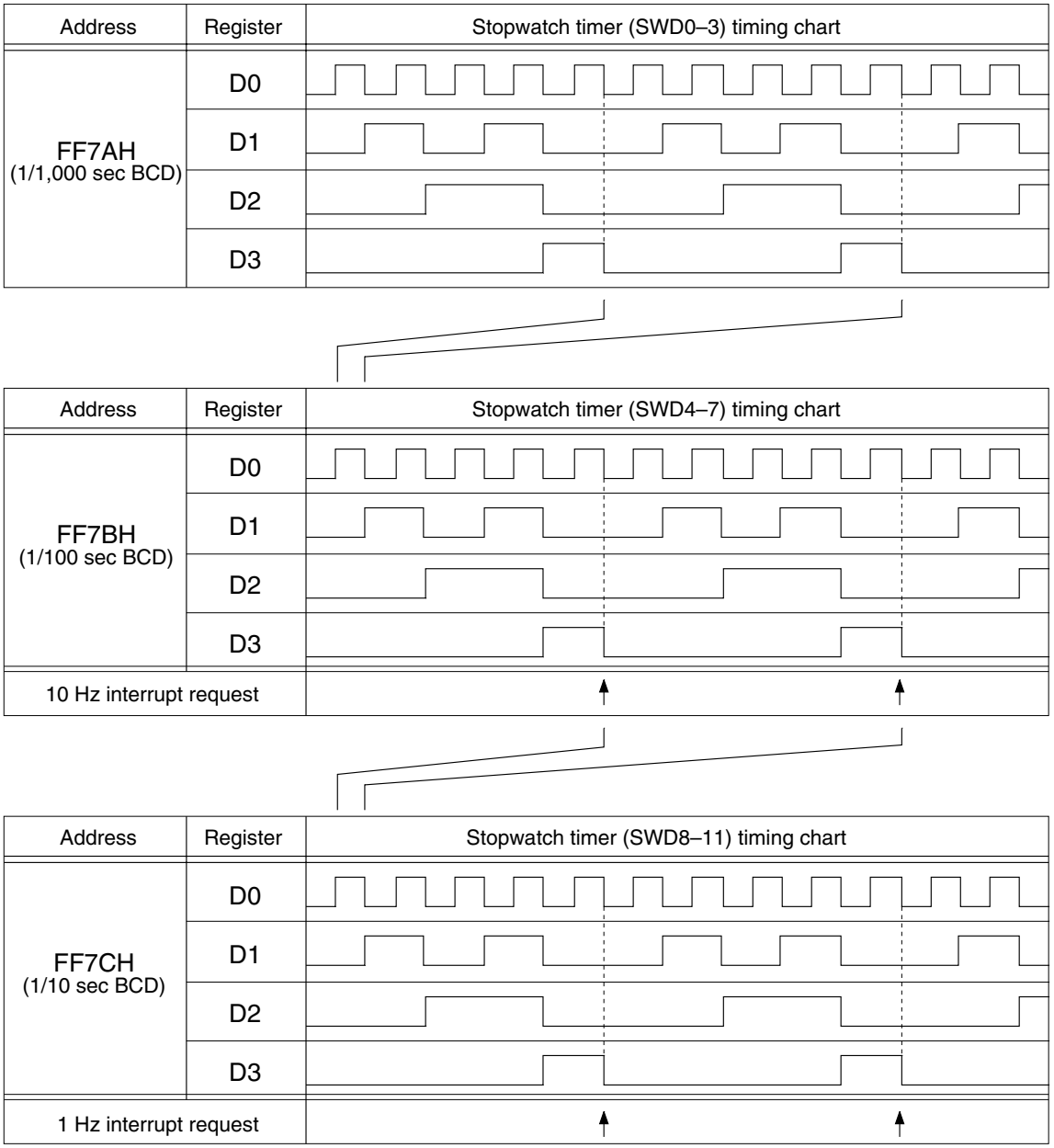


Fig. 4.8.6.1 Timing chart for counters

As shown in Figure 4.8.6.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flag (ISW10, ISW1) is set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW10, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Direct RUN and direct LAP interrupts

When the direct input function is selected, the direct RUN and direct LAP interrupts can be generated. The respective interrupts occur at the rising edge of the internal signal for direct RUN and direct LAP after sampling the direct input signal in the falling edge of 1,024 Hz signal. Also, at this time the corresponding interrupt factor flag (IRUN, ILAP) is set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EIRUN, EILAP). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the inputs of the RUN and LAP.

The direct RUN and LAP functions use the K00 and K01 ports. Therefore, the direct input interrupt and the K00–K03 inputs interrupt may generate at the same time depending on the interrupt condition setting for the input port K00–K03. Consequently, when using the direct input interrupt, set the interrupt selection registers SIK00 and SIK01 to "0" so that the input interrupt does not generate by K00 and K01 inputs.

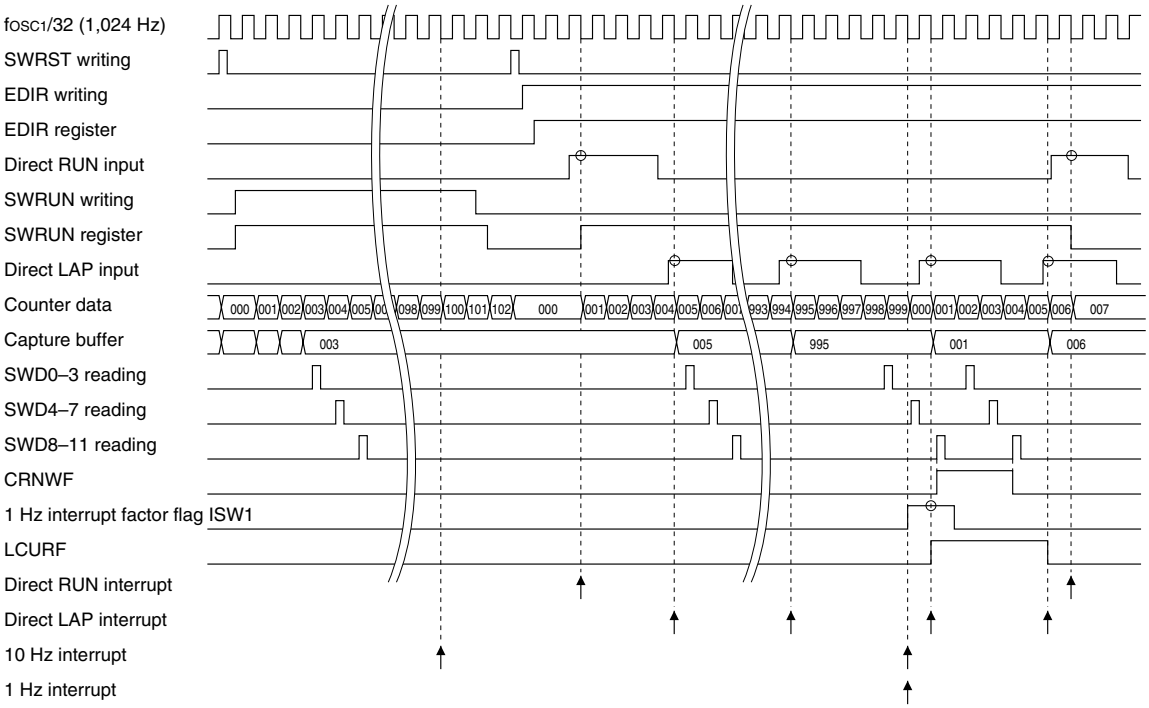


Fig. 4.8.6.2 Timing chart for stopwatch timer

4.8.7 I/O memory of stopwatch timer

Table 4.8.7.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.8.7.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	SWDIR	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable (P41)
					SWDIR	0			Stopwatch direct input switch 0: K00=Run/Stop, K01=Lap 1: K00=Lap, K01=Run/Stop
	R/W				FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3 Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
					FOFQ0	0			
FF78H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Direct input enable
					DKM2	0			Key mask selection [DKM2, 1, 0] 0 1 2 3 Key mask None K02 K02–03 K02–03,10 [DKM2, 1, 0] 4 5 6 7 Key mask K10 K10–11 K10–12 K10–13
	R/W				DKM1	0			
					DKM0	0			
FF79H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Request	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
FF7AH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/1000 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7BH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/100 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FF7CH	SWD11	SWD10	SWD9	SWD8	SWD11	0			Stopwatch timer data BCD (1/10 sec)
					SWD10	0			
	R				SWD9	0			
					SWD8	0			
FFE6H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF6H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWD0–SWD3: Stopwatch timer data 1/1,000 sec (FF7AH)

Data (BCD) of the 1/1,000 sec column of the capture buffer can be read out.
The hold function of the capture buffer works by reading this data.
These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD4–SWD7: Stopwatch timer data 1/100 sec (FF7BH)

Data (BCD) of the 1/100 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWD8–SWD11: Stopwatch timer data 1/10 sec (FF7CH)

Data (BCD) of the 1/10 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

Note: Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

EDIR: Direct input function enable register (FF78H•D3)

Enables the direct input (RUN/LAP) function.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function is enabled by writing "1" to EDIR, and then RUN/STOP and LAP control can be done by external key input. When "0" is written, the direct input function is disabled, and the stopwatch timer is controlled by the software only.
Further the function switching is actually done by synchronizing with the falling edge of fOSC1/32 (1,024 Hz) after the data is written to this register (after 977 µsec maximum).
At initial reset, this register is set to "0".

SWDIR: Direct input switch register (FF06H•D2)

Switches the direct-input key assignment for the K00 and K01 ports.

When "1" is written: K00 = LAP, K01 = RUN/STOP
When "0" is written: K00 = RUN/STOP, K01 = LAP
Reading: Valid

The direct-input key assignment is selected using this register. The K00 and K01 port statuses are input to the stopwatch timer as the RUN/STOP and LAP inputs according to this selection.
At initial reset, this register is set to "0".

DKM0–DKM2: Direct key mask selection registers (FF78H•D0–D2)

Selects a combination of the key inputs for concurrence judgment with RUN and LAP inputs when the direct input function is set.

Table 4.8.7.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

When the concurrence is detected, RUN and LAP inputs cannot be accepted until the concurrence is released.
At initial reset, these registers are set to "0".

SWRST: Stopwatch timer reset (FF79H•D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
Since this reset does not affect the capture buffer, the capture buffer data in hold status is not cleared and is maintained.
This bit is write-only, and is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP (FF79H•D1)

This register controls the RUN/STOP of the stopwatch timer, and the operating status can be monitored by reading this register.

• ***When writing data***

When "1" is written: RUN
When "0" is written: STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count. RUN/STOP control with this register is valid only when the direct input function is set to disable. When the direct input function is set, it becomes invalid.

• ***When reading data***

When "1" is read: RUN
When "0" is read: STOP

Reading is always valid regardless of the direct input function setting. "1" is read when the stopwatch timer is in the RUN status, and "0" is read in the STOP status.
At initial reset, this register is set to "0".

LCURF: Lap data carry-up request flag (FF79H•D3)

This flag indicates a carry that has been generated to 1 sec-digit when the data is held. Note that this flag is invalid when the direct input function is disabled.

When "1" is read: Carry is required
When "0" is read: Carry is not required
Writing: Invalid

If the capture buffer shifts into hold status while the 1 Hz interrupt factor flag ISW1 is set to "1", LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required. When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read this flag before processing and check whether carry-up is needed or not.
This flag is renewed (set/reset) every time the capture buffer shifts into hold status.
At initial reset, this flag is set to "0".

CRNWF: Capture renewal flag (FF79H•D2)

This flag indicates that the content of the capture buffer has been renewed.

When "1" is read: Renewed
When "0" is read: Not renewed
Writing: Invalid

The content of the capture buffer is renewed if the LAP key is input when the data held into the capture buffer has not yet been read. Reading SWD8–11 in that status sets this flag to "1", and the hold status is maintained. Consequently, when data that is held by a LAP input is read, read this flag after reading the SWD8–11 and check whether the data has been renewed or not.
This flag is renewed when SWD8–11 is read.
At initial reset, this flag is set to "0".

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFE6H)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers EIRUN, EILAP, EISW1 and EISW10 are used to separately select whether to mask the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts.
At initial reset, these registers are set to "0".

IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFF6H)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IRUN, ILAP, ISW1 and ISW10 correspond to the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts respectively. The software can judge from these flags whether there is a stopwatch timer interrupt. However, even if the interrupt is masked, the flags are set to "1" when the timing condition is established.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.8 Programming notes

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.9 Programmable Timer

4.9.1 Configuration of programmable timer

The S1C63709 has three 8-bit programmable timer systems (timer 0, timer 1 and timer 2) built-in.
The timers are composed of 8-bit presettable down counters and they can be used as 8 bits × 3 channels or 16 bits × 1 channel + 8 bits × 1 channel of programmable timers. Timer 0 also has an event counter function using the K11 input port terminal.
Figure 4.9.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the P20 I/O port terminal
- Generating the synchronous clock source for the serial interface (timer 2 underflow is used, and it is possible to set the transfer rate)

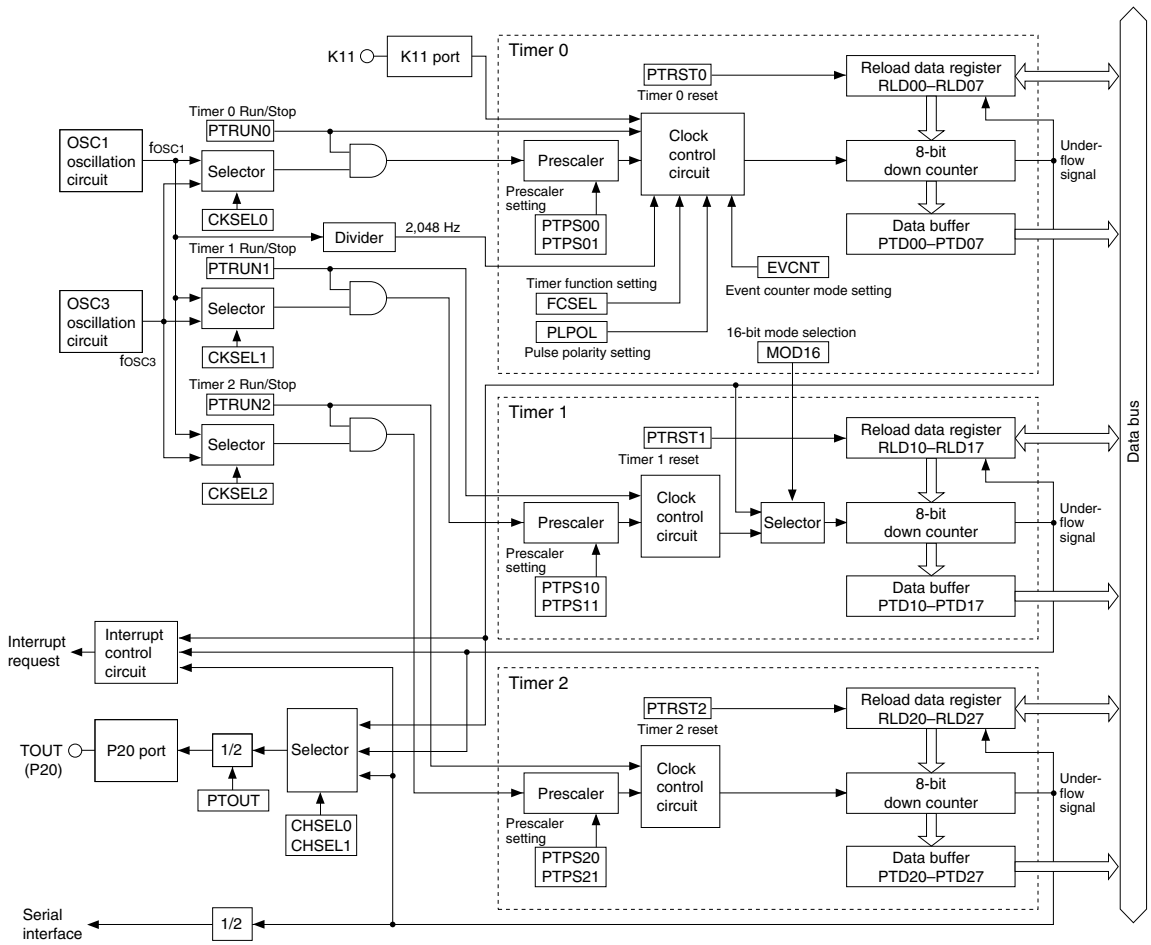


Fig. 4.9.1.1 Configuration of programmable timer

4.9.2 Basic count operation

This section explains the basic count operation when each timer is used as an individual 8-bit timer.

Each timer has an 8-bit down counter and an 8-bit reload data register.
The reload data register RLDx0–RLDx7 (x = timer number) is used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRSTx, the down counter loads the initial value set in the reload register. Therefore, down-counting is executed from the stored initial value by the input clock.
The PTRUNx register is provided to control the RUN/STOP for each timer. By writing "1" to this register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.
The counter data can be read via the data buffer PTDx0–PTDx7 in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data (PTDx4–PTDx7) when the low-order data (PTDx0–PTDx3) is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.
The counter reloads the initial value set in the reload data register when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

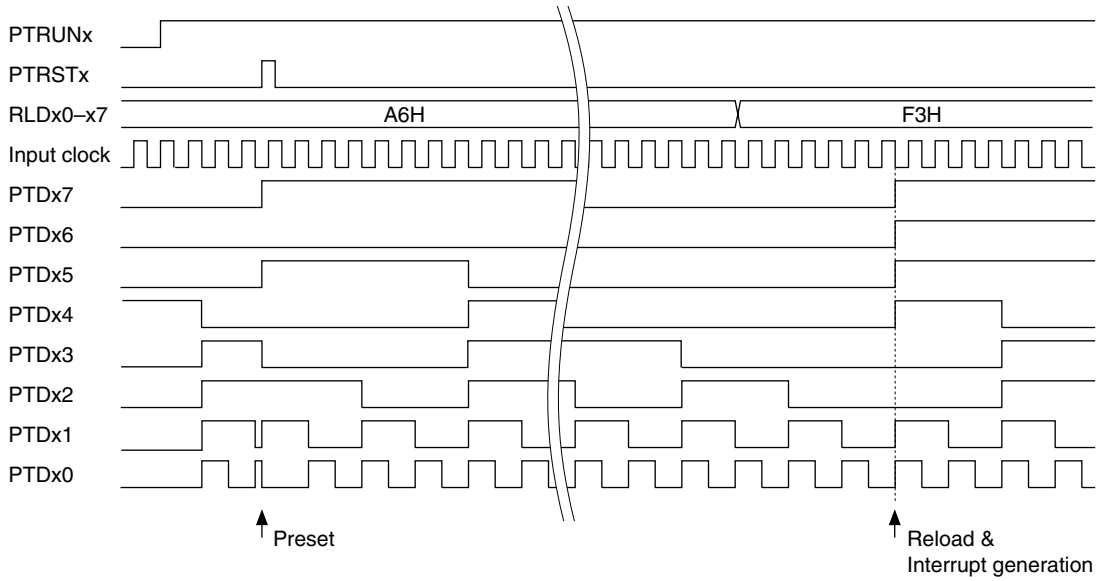


Fig. 4.9.2.1 Basic operation timing of down counter

4.9.3 Setting the input clock

A prescaler is provided for each timer. The prescaler generates the input clock for the timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.
The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for each timer individually.
The input clock is set in the following sequence.

Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSELx; when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation on, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit on until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit on to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in off state.

Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection register PTPSx0/PTPSx1. Table 4.9.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.9.3.1 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the PTRUNx register, the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.9.4 Event counter mode (timer 0)

Timer 0 has an event counter function that counts an external clock input to the input port K11. This function is selected by writing "1" to timer 0 counter mode selection register EVCNT. At initial reset, EVCNT is set to "0" and timer 0 is configured as a normal timer that counts the internal clock.
In the event counter mode, the clock is supplied to timer 0 from outside the IC, therefore, the settings of the timer 0 prescaler division ratio selection register PTPS00–PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.
Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.9.4.1.

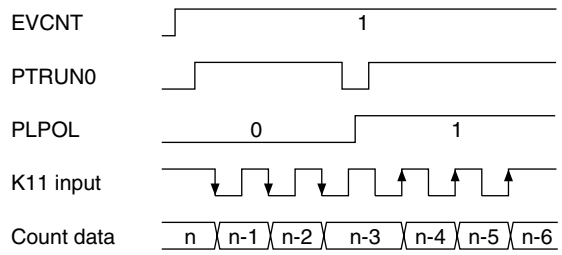


Fig. 4.9.4.1 Timing chart in event counter mode

The event counter mode also allows use of a noise reject function to eliminate noise such as chattering on the external clock (K11 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec∗ or more to count reliably. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz∗ signal after changing the input level of the K11 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec∗ or less.
(∗: f_{OSC1} = 32.768 kHz)
Figure 4.9.4.2 shows the count down timing with noise rejector.

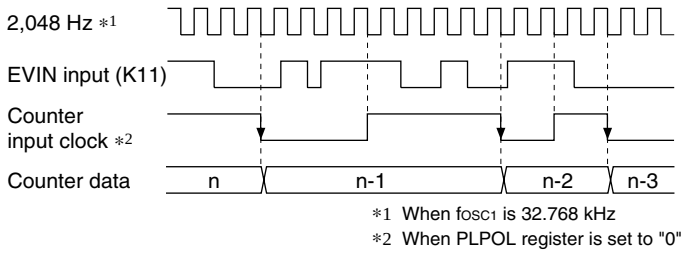


Fig. 4.9.4.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the normal timer except it uses the K11 input as the clock. Refer to Section 4.9.2, "Basic count operation" for basic operation and control.

4.9.5 16-bit timer (timer 0 + timer 1)

Timers 0 and 1 can be used as a 16-bit timer.
To use the 16-bit timer, write "1" to the timer 0 16-bit mode selection register MOD16.
The 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte as shown in Figure 4.9.5.1.

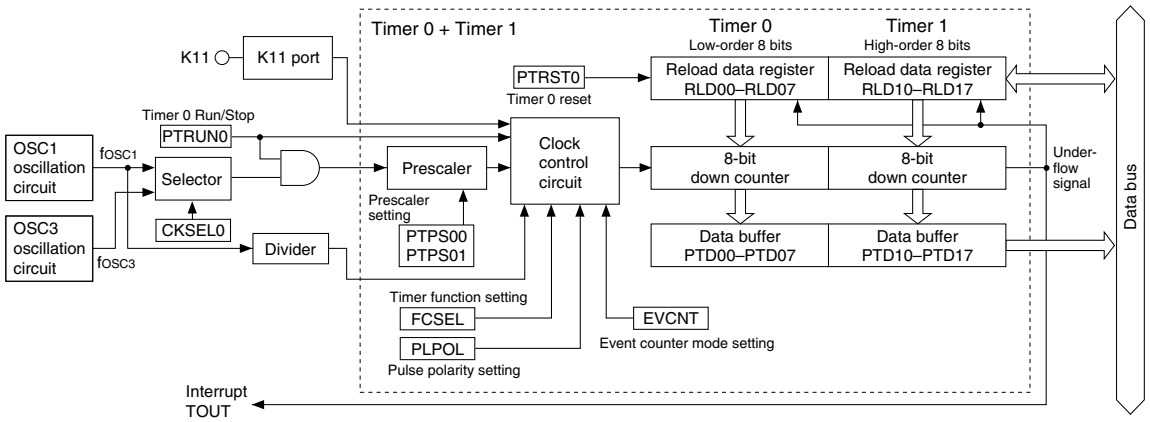


Fig. 4.9.5.1 Configuration of 16-bit timer

The registers for timer 0 are used to control the timer. Thus the event counter function can also be used. Timer 1 operates with the timer 0 underflow signal as the count clock, so the clock and RUN/STOP control registers for timer 1 become invalid.
The counter data in 16-bit mode must be read in the order below.
PTD00–PTD03 → PTD04–PDT07 → PTD10–PTD13 → PTD14–PTD17

4.9.6 Interrupt function

The programmable timer can generate an interrupt due to an underflow of each timer. See Figure 4.9.2.1 for the interrupt timing.

An underflow of timer x sets the corresponding interrupt factor flag IPTx to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPTx. However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

When timers 0 and 1 are used as a 16-bit timer, an interrupt is generated by an underflow of timer 1. In this case, IPT0 is not set to "1" by a timer 0 underflow.

4.9.7 Control of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of a timer. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL0–CHSEL1.

Table 4.9.7.1 Selecting a timer for TOUT output

CHSEL1	CHSEL0	TOUT output timer
1	*	Timer 2
0	1	Timer 1
0	0	Timer 0

Select timer 1 when generating the TOUT signal from the 16-bit timer output.

The TOUT signal can be output from the P20 I/O port terminal. Programmable clocks can be supplied to external devices.
The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the P20 port terminal and when "0" is written, the terminal goes low (VSS). However, the I/O control register (IOC20) must always be "1" (output), the data register (P20) must always be "0" and the pull-down control register (PUL20) must always be "0" (pull-down disabled).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.
Figure 4.9.7.1 shows the output waveform of the TOUT signal.

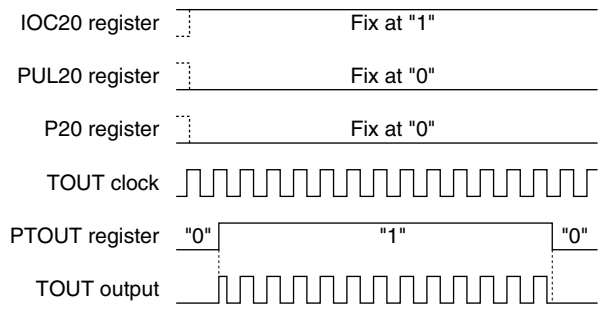


Fig. 4.9.7.1 Output waveform of the TOUT signal

4.9.8 Transfer rate setting for serial interface

The signal that is made from underflows of timer 2 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 2 into RUN state (PTRUN2 = "1"). It is not necessary to control with the PTOUT register.

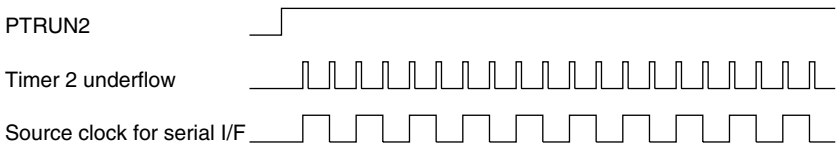


Fig. 4.9.8.1 Synchronous clock of serial interface

A setting value for the RLD2x register according to a transfer rate is calculated by the following expression:

RLD2x = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD2x)

Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source.

4.9.9 I/O memory of programmable timer

Table 4.9.9.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.9.9.1(a) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC0H	MOD16	EVCNT	FCSEL	PLPOL	MOD16	0	16 bits	8 bits	16-bit mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	0	CHSEL1	CHSEL0	PTOUT	0 *3	– *2			Unused
					CHSEL1	0			TOUT output selection [CHSEL1,0]: 0 Timer, 1 Timer 0, 2 Timer 1, Timer 2
	R	R/W			CHSEL0	0			
					PTOUT	0	On	Off	TOUT output control (P20)
FFC2H	0	CKSEL2	CKSEL1	CKSEL0	0 *3	– *2			Unused
					CKSEL2	0	OSC3	OSC1	Prescaler 2 source clock selection
	R	R/W			CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC3H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 Division ratio 1/1, 1 1/4, 2 1/32, 3 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC4H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 Division ratio 1/1, 1 1/4, 2 1/32, 3 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC5H	PTPS21	PTPS20	PTRST2	PTRUN2	PTPS21	0			Prescaler 2 division ratio selection [PTPS21, 20]: 0 Division ratio 1/1, 1 1/4, 2 1/32, 3 1/256
					PTPS20	0			
	R/W		W	R/W	PTRST2*3	– *2	Reset	Invalid	Timer 2 reset (reload)
					PTRUN2	0	Run	Stop	Timer 2 Run/Stop
FFC6H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC7H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC8H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC9H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFCAH	RLD23	RLD22	RLD21	RLD20	RLD23	0			MSB
					RLD22	0			Programmable timer 2 reload data (low-order 4 bits)
	R/W				RLD21	0			
					RLD20	0			LSB
FFCBH	RLD27	RLD26	RLD25	RLD24	RLD27	0			MSB
					RLD26	0			Programmable timer 2 reload data (high-order 4 bits)
	R/W				RLD25	0			
					RLD24	0			LSB
FFCCH	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFCDH	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.9.9.1(b) Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFCEH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCFH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFD0H	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB
					PTD22	0			Programmable timer 2 data (low-order 4 bits)
	R				PTD21	0			
					PTD20	0			LSB
FFD1H	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB
					PTD26	0			Programmable timer 2 data (high-order 4 bits)
	R				PTD25	0			
					PTD24	0			LSB
FFE1H	0	EIPT2	EIPT1	EIPT0	0 *3	– *2			Unused
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2)
	R	R/W			EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF1H	0	IPT2	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
	R	R/W			IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC2H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC2H•D1)
CKSEL2: Prescaler 2 source clock selection register (FFC2H•D2)
Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSELx register, the OSC1 clock is selected as the input clock for the prescaler x (for timer x) and when "1" is written, the OSC3 clock is selected.
When the event counter mode is selected for timer 0, the setting of CKSEL0 becomes invalid.
When timers 0 and 1 are used as a 16-bit timer, the setting of CKSEL1 becomes invalid.
At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC3H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC4H•D2, D3)
PTPS20, PTPS21: Timer 2 prescaler division ratio selection register (FFC5H•D2, D3)
Sets the division ratio of the prescaler as shown in Table 4.9.9.2.

Table 4.9.9.2 Selection of prescaler division ratio

PTPSx1	PTPSx0	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of PTPS00 and PTPS01 becomes invalid.
When timers 0 and 1 are used as a 16-bit timer, the setting of PTPS10 and PTPS11 becomes invalid.
At initial reset, these registers are set to "0".

MOD16: 16-bit mode selection register (FFC0H•D3)

Selects whether timers 0 and 1 are used as a 16-bit timer or 2 channels of 8-bit timer.

When "1" is written: 16-bit timer
When "0" is written: 8-bit timer
Reading: Valid

When "1" is written to MOD16, a 16-bit timer is configured with timer 0 for low-order byte and timer 1 for high-order byte. Use the timer 0 registers for control. When "0" is written to MOD16, timer 0 and timer 1 are used as independent 8-bit timers.
At initial reset, this register is set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)

Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector
When "0" is written: Without noise rejector
Reading: Valid

When "1" is written to the FCSEL register, the noise rejector is used and counting is done by an external clock (K11) with 0.98 msec* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the K11 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less.
(*: f_{OSC1} = 32.768 kHz)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K11 input port terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K11 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC6H, FFC7H)
RLD10–RLD17: Timer 1 reload data register (FFC8H, FFC9H)
RLD20–RLD27: Timer 2 reload data register (FFCAH, FFCBH)
Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRSTx register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFCCH, FFCDH)
PTD10–PTD17: Timer 1 counter data (FFCEH, FFCFH)
PTD20–PTD27: Timer 2 counter data (FFD0H, FFD1H)
Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer x can be read from PTDx0–PTDx3, and the high-order data can be read from PTDx4–PTDx7. Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC3H•D1)
PTRST1: Timer 1 reset (reload) (FFC4H•D1)
PTRST2: Timer 2 reset (reload) (FFC5H•D1)
Resets the timer and presets reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRSTx, the reload data in the reload register RLDx0–RLDx7 is preset to the counter in timer x. When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC3H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC4H•D0)
PTRUN2: Timer 2 RUN/STOP control register (FFC5H•D0)
Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in timer x starts counting down by writing "1" to the PTRUNx register and stops by writing "0". In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
At initial reset, these registers are set to "0".

CHSEL0, CHSEL1: TOUT output channel selection register (FFC1H•D1, D2)
Selects the channel used for TOUT signal output.

Table 4.9.9.3 Selecting a timer for TOUT output

CHSEL1	CHSEL0	TOUT output timer
1	*	Timer 2
0	1	Timer 1
0	0	Timer 0

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D0)
Turns TOUT signal output on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the P20 port terminal and when "0" is written, the terminal goes low (V_{SS}). However, the I/O control register (IOC20) must always be "1" (output), the data register (P20) must always be "0" and the pull-down control register (PUL20) must always be "0" (pull-down disabled).
At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE1H•D0)
EIPT1: Timer 1 interrupt mask register (FFE1H•D1)
EIPT2: Timer 2 interrupt mask register (FFE1H•D2)
These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The timer x interrupt can be masked individually by the interrupt mask registers EIPTx.
At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF1H•D0)
IPT1: Timer 1 interrupt factor flag (FFF1H•D1)
IPT2: Timer 2 interrupt factor flag (FFF1H•D2)
These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IPTx correspond to the timer x interrupt. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.10 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) should be read within 0.73 msec (when fOSC1 is 32.768 kHz) of reading the low-order 4 bits (PTDx0–PTDx3).

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.
Figure 4.9.10.1 shows the timing chart for the RUN/STOP control.

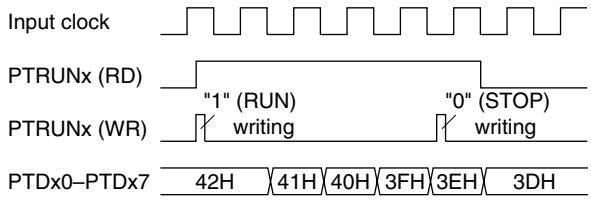


Fig. 4.9.10.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

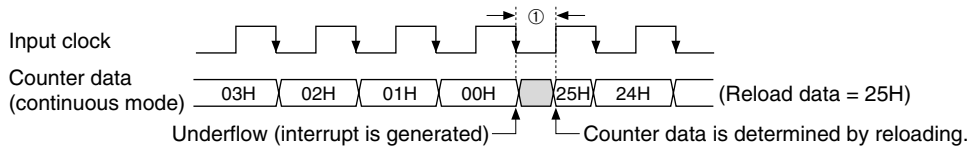


Fig. 4.9.10.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

4.10 Serial Interface (SIN, SOUT, SCLK, SRDY)

4.10.1 Configuration of serial interface

The S1C63709 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.10.1.1.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of three types of master mode (internal clock mode: when the S1C63709 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the S1C63709 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, SRDY signal which indicates whether or not the serial interface is available to transmit or receive can be output to the SRDY terminal.

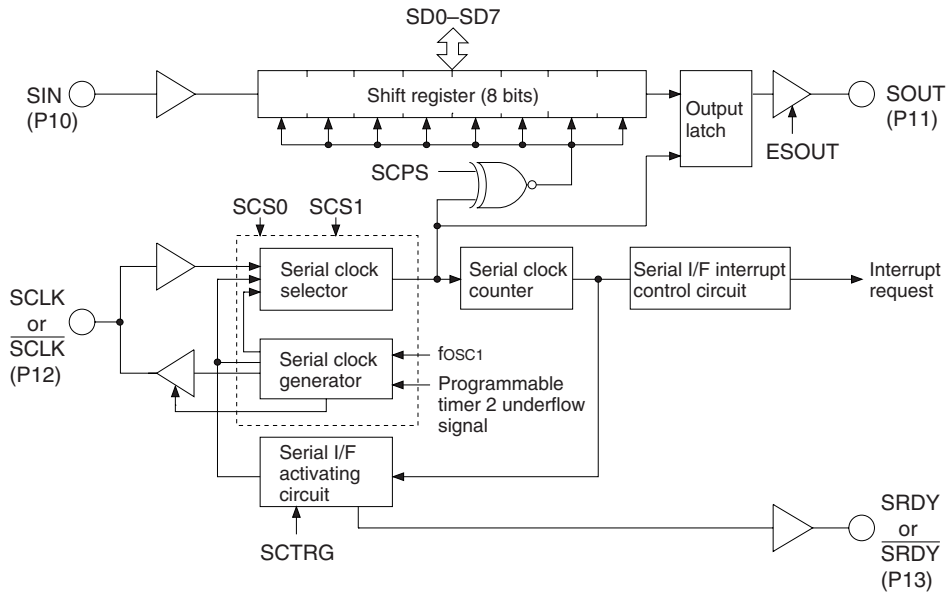


Fig. 4.10.1.1 Configuration of serial interface

The input/output ports of the serial interface are shared with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = SCLK (O)	P12 = SCLK (I)
P13 = I/O port (I/O)	P13 = SRDY (O)

The SOUT output using the P11 port is enabled when "1" is written to the ESOUT register. If ESOUT is "0", P11 functions as a general-purpose I/O port.

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1", ESOUT = "1") in the initial routine.

4.10.2 Mask option

Terminal specification

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13), the mask option that selects the output specification for the I/O port is also applied to the serial interface. The output specification of the terminals SOUT, SCLK (during the master mode) and SRDY (during the slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P11, P12 and P13. Either complementary output or P-channel open drain output can be selected as the output specification. However, when P-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the terminal.

Furthermore, the pull-down resistor for the SIN terminal and the SCLK terminal (during slave mode) that are used as input terminals can be selected by mask option. The pull-down register can be added by the mask options of P10 and P12. When "without pull-down" is selected, take care that the floating status does not occur.

Polarity of synchronous clock and ready signal

Polarity of the synchronous clock and the ready signal that is output in the slave mode can be selected from either positive polarity (high active, SCLK & SRDY) or negative polarity (low active, $\overline{\text{SCLK}}$ & $\overline{\text{SRDY}}$).
When operating the serial interface in the slave mode, the synchronous clock is input from a external device. Be aware that the terminal specification is pull-down only and a pull-up resistor cannot be built in if negative polarity is selected.
In the following explanation, it is assumed that positive polarity (SCLK, SRDY) has been selected.

4.10.3 Master mode and slave mode of serial interface

The serial interface of the S1C63709 has two types of operation mode: master mode and slave mode.
The master mode uses an internal clock as the synchronous clock for the built-in shift register, and outputs this internal clock from the SCLK (P12) terminal to control the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK (P12) terminal and it is used as the synchronous clock for the built-in shift register.
The master mode and slave mode are selected by writing data to the SCS1 and SCS0 registers.
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.10.3.1.

Table 4.10.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer *
0	0	Slave mode	External clock *

* The maximum clock is limited to 1 MHz.

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 2) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for the control of the programmable timer.

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the SCLK (P12) terminal, clock output is automatically suspended and the SCLK (P12) terminal is fixed at low level (or high level when negative polarity is selected by mask option).
- In the slave mode, after input of 8 clocks to the SCLK (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.10.3.1.

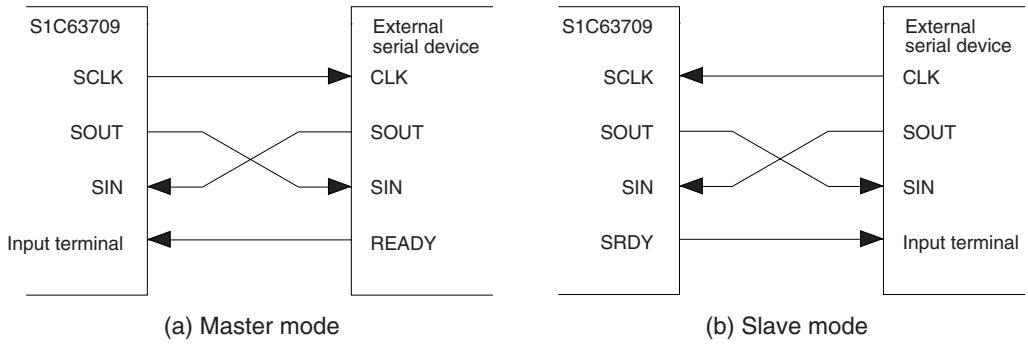


Fig. 4.10.3.1 Sample basic connection of serial input/output section

4.10.4 Data input/output and interrupt function

The serial interface of S1C63709 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the SCLK (P12) terminal (master mode), or the synchronous clock input to the SCLK (P12) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock SCLK; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

Serial data output procedure and interrupt

The S1C63709 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to the data registers SD0–SD3 (FF72H) and SD4–SD7 (FF73H) and writing "1" to SCTRG bit (FF70H•D1), it synchronizes with the synchronous clock and the serial data is output to the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.
Shift timing of serial data is as follows:

- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the rising edge of the clock input or output from/to the SCLK (P12) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS register is "1" and is shifted at the falling edge of the SCLK signal when the SCPS register is "0".

- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P12) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register (FF71H•D2) is "1" and is shifted at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0".

  When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF2H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE2H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

Serial data input procedure and interrupt

The S1C63709 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.
Shift timing of serial data is as follows:

- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS register is "1" and is read at the falling edge of the SCLK signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.
- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "1" and is read at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

Serial data input/output permutation

The S1C63709 allows the input/output permutation of serial data to be selected by the SDP register (FF71H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.10.4.1. The SDP register should be set before setting data to SD0–SD7.

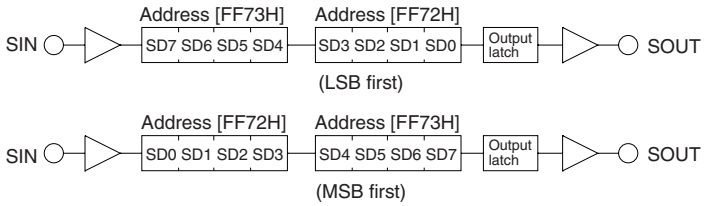


Fig. 4.10.4.1 Serial data input/output permutation

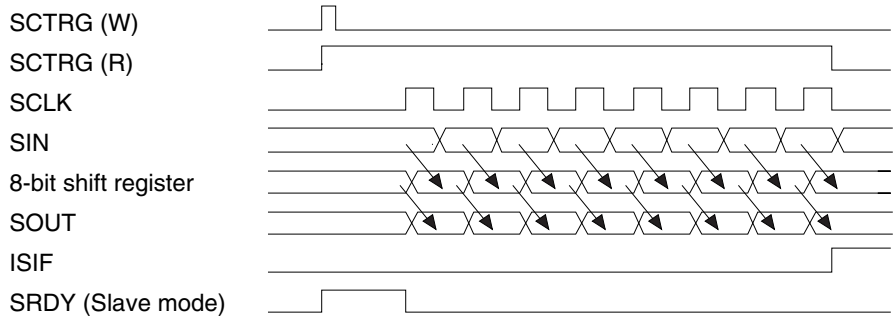
SRDY signal

When the S1C63709 serial interface is used in the slave mode (external clock mode), SRDY signal is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. SRDY signal is output from the SRDY (P13) terminal.
Output timing of SRDY signal is as follows:

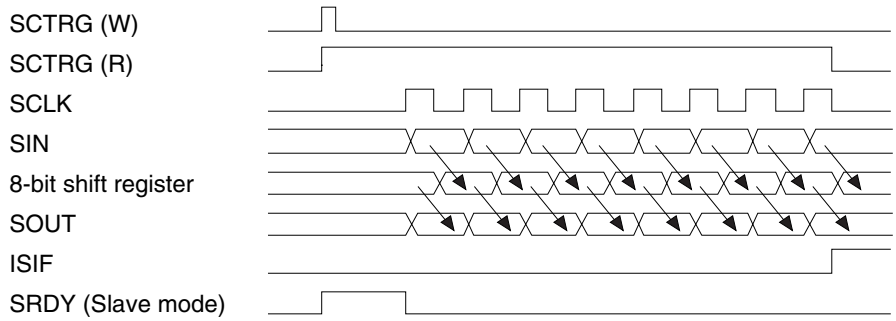
- ***When positive polarity is selected (mask option):***
  SRDY signal goes "1" (high) when the S1C63709 serial interface is available to transmit or receive data; normally, it is at "0" (low).
  SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the SRDY signal returns to "0".
- ***When negative polarity is selected (mask option):***
  $\overline{\text{SRDY}}$ signal goes "0" (low) when the S1C63709 serial interface is available to transmit or receive data; normally, it is at "1" (high).
  $\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

Timing chart

The S1C63709 serial interface timing charts are shown in Figures 4.10.4.2 and 4.10.4.3.

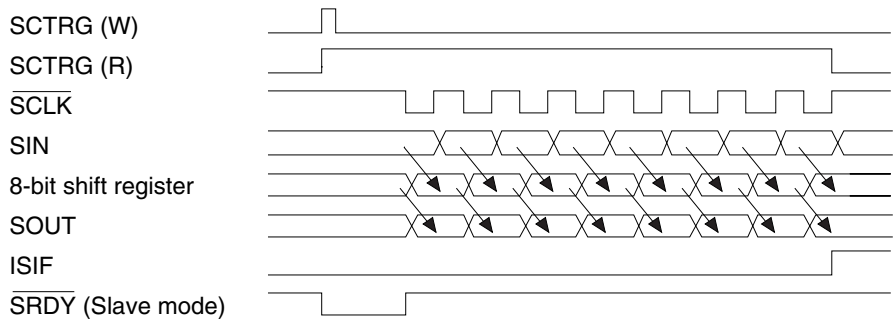


(a) When SCPS = "1"

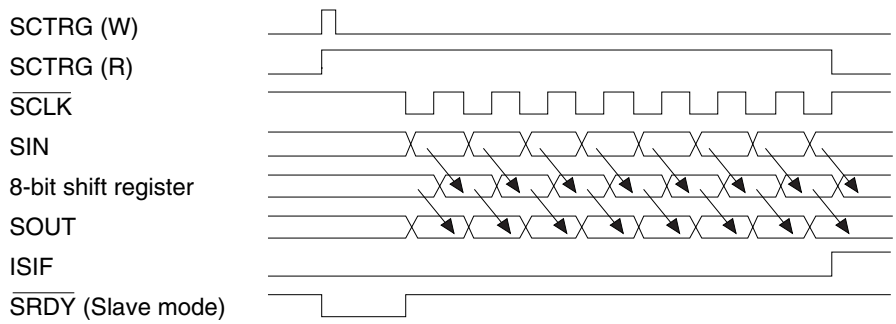


(b) When SCPS = "0"

Fig. 4.10.4.2 Serial interface timing chart (when synchronous clock is positive polarity SCLK)



(a) When SCPS = "1"



(b) When SCPS = "0"

Fig. 4.10.4.3 Serial interface timing chart (when synchronous clock is negative polarity $\overline{SCLK}$)

4.10.5 I/O memory of serial interface

Table 4.10.5.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.10.5.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-down control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-down control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-down control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-down control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-down control register (ESIF=0) SIN pull-down control register when SIF is selected
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0	⌐	⌐	Serial I/F clock phase selection
							⌐	⌐	–Negative polarity (mask option)
							⌐	⌐	–Positive polarity (mask option)
	R/W				SCS1	0			Serial I/F clock mode selection
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	LSB
FFE2H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFF2H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)

Clock mode selection:

[SCS1, 0]	0	1
Clock	Slave	PT
[SCS1, 0]	2	3
Clock	OSC1/2	OSC1

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (P1 port function selection) (FF70H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P10, P11, P12 and P13 function as SIN, SOUT, SCLK, SRDY, respectively.
In the slave mode, the P13 terminal functions as SRDY output terminal, while in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

ESOUT: SOUT enable register (FF70H•D2)

Enables serial data output from the P11 port.

When "1" is written: Enabled (SOUT)
When "0" is written: Disabled (I/O port)
Reading: Valid

When serial data output is not used, the SOUT output can be disabled to use P11 as an I/O port. When performing serial output, write "1" to ESOUT to set P11 as the SOUT output port.
At initial reset, this register is set to "0".

PUL10: SIN (P10) pull-down control register (FF45H•D0)
PUL12: SCLK (P12) pull-down control register (FF45H•D2)

Sets the pull-down of the SIN terminal and the SCLK terminals (in the slave mode).

When "1" is written: Pull-down On
When "0" is written: Pull-down Off
Reading: Valid

Enables or disables the pull-down resistor built into the SIN (P10) and SCLK (P12) terminals. (Pull-down resistor is only built in the port selected by mask option.)
SCLK pull-down is effective only in the slave mode. In the master mode, the PUL12 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and pull-down goes on.

SCS0, SCS1: Clock mode selection register (FF71H•D0, D1)

Selects the synchronous clock (SCLK) for the serial interface.

Table 4.10.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer ∗
0	0	Slave mode	External clock ∗

∗ The maximum clock is limited to 1 MHz.

Synchronous clock (SCLK) is selected from among the above 4 types: 3 types of internal clock and external clock.
When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 2) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for the control of the programmable timer.
At initial reset, external clock is selected.

SCPS: Clock phase selection register (FF71H•D2)

Selects the timing for reading in the serial data input from the SIN (P10) terminal.

• ***When positive polarity is selected:***

When "1" is written: Rising edge of SCLK
When "0" is written: Falling edge of SCLK
Reading: Valid

• ***When negative polarity is selected:***

When "1" is written: Falling edge of $\overline{\text{SCLK}}$
When "0" is written: Rising edge of $\overline{\text{SCLK}}$
Reading: Valid

Select whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge or falling edge of the synchronous signal.

Pay attention to the polarity of the synchronous clock selected by the mask option because the selection content is different.
The input data fetch timing may be selected but output timing for output data is fixed at the rising edge of SCLK (when positive polarity is selected) or at the falling edge of $\overline{SCLK}$ (when negative polarity is selected).
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection register (FF71H•D3)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF70H•D1)

This is a trigger to start input/output of synchronous clock (SCLK).

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

• ***When reading***

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)

When this bit is read, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (FF72H, FF73H)

These registers are used for writing and reading serial data.

• ***When writing***

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P11) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

• When reading

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read from these registers.
The serial data input from the SIN (P10) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFE2H•D0)

Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFF2H•D0)

This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.
This flag is reset to "0" by writing "1" to it.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.10.6 Programming notes

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Sound Generator

4.11.1 Configuration of sound generator

The S1C63709 has a built-in sound generator for generating a buzzer signal.
Hence, the generated buzzer signal can be output from the P40 (BZ) terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 4.11.1.1 shows the configuration of the sound generator.

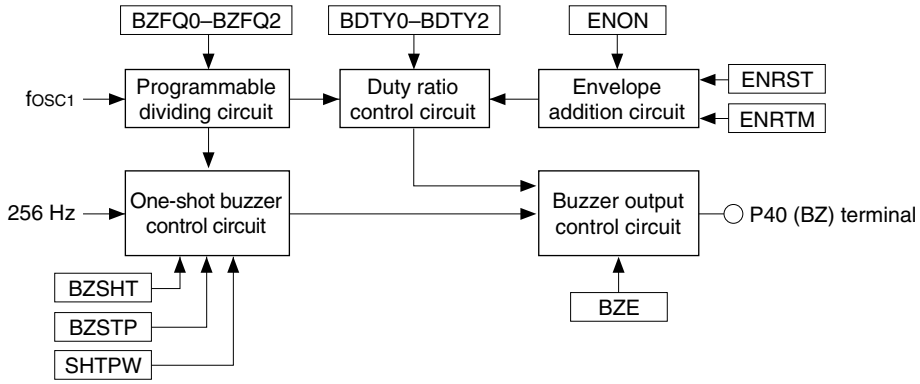


Fig. 4.11.1.1 Configuration of sound generator

4.11.2 Control of buzzer output

The BZ signal generated by the sound generator is output from the P40 (BZ) terminal by setting "1" for the buzzer output enable register BZE. When "0" is set to BZE register, the P40 (BZ) terminal goes low (VSS).

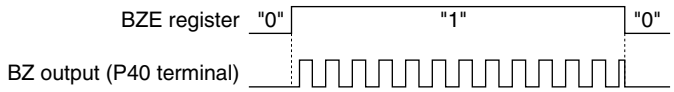


Fig. 4.11.2.1 Buzzer signal output timing chart

Notes:
- *When using the P40 port as the BZ output port, fix the I/O control register (IOC40) at "1" (output), data register (P40) at "0" and the pull-down control register (PUL40) at "0" (pull-down disabled).*
- *Since it generates the buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.*

4.11.3 Setting of buzzer frequency and sound level

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency selection registers BZFQ0–BZFQ2 as shown in Table 4.11.3.1.

Table 4.11.3.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.
The duty ratio can be selected from among the 8 types shown in Table 4.11.3.2 according to the setting of the buzzer duty selection registers BDTY0–BDTY2.

Table 4.11.3.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

When the high level output time has been made TH and when the low level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes TH/(TH+TL).
When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.11.3.2.

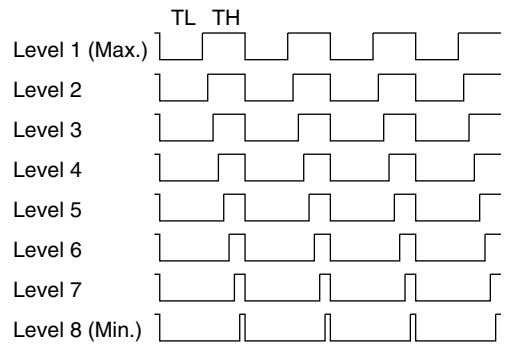


Fig. 4.11.3.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.

4.11.4 Digital envelope

A digital envelope for duty control can be added to the buzzer signal.
The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.11.3.2 in the preceding item from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.
When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8.
When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal.
The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.
Figure 4.11.4.1 shows the timing chart of the digital envelope.

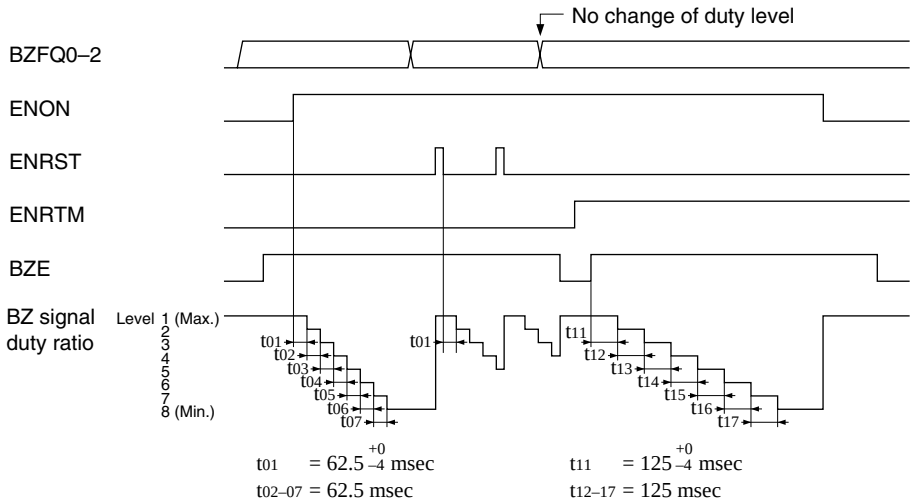


Fig. 4.11.4.1 Timing chart for digital envelope

4.11.5 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.
The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the buzzer output terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.
The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes off in synchronization with the 256 Hz signal.

When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.
One-shot output is invalid during normal buzzer output (during BZE = "1").

Figure 4.11.5.1 shows timing chart for one-shot output.

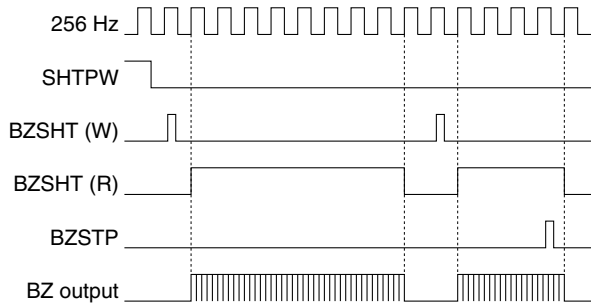


Fig. 4.11.5.1 Timing chart for one-shot output

4.11.6 Buzzer output while the motor is driving

The EMPON register is provided to select whether the buzzer signal will be able to output or not while the motor drive pulses are outputting.
When EMPON is set to "0" (default), the buzzer signal is disabled to output only in the motor drive pulse output period. The period that does not output the pulses in a motor drive step cycle enables output of the buzzer signal.
When EMPON is set to "1", the buzzer output is always enabled regardless of the motor drive pulse output status.

This selection is effective for all motors (motor 0 and motor 1) and drive pulse types (normal rotation and reverse rotation).

Figure 4.11.6.1 shows an example of buzzer output while the normal rotation pulses are outputting to a motor.

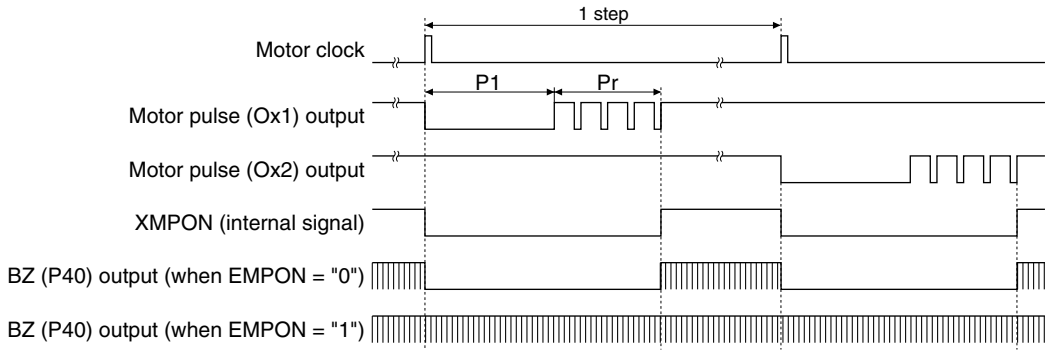


Fig. 4.11.6.1 Buzzer output during driving motor (when normal rotation pulse is output)

4.11.7 I/O memory of sound generator

Table 4.11.7.1 shows the I/O addresses and the control bits for the sound generator.

Table 4.11.7.1 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time selection
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable (P40)
FF6DH	EMPON	BZSTP	BZSHT	SHTPW	EMPON	0	Enable	Disable	Buzzer output enable in motor pulse output period
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R/W	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3 — Frequency (Hz) 4096.0 3276.8 2730.7 2340.6; [BZFQ2, 1, 0] 4 5 6 7 — Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
					BZFQ1	0			
	R	R/W			BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
					BDTY1	0			
	R	R/W			BDTY0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

BZE: Buzzer output control register (FF6CH•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output On
When "0" is written: Buzzer output Off
Reading: Valid

When "1" is written to BZE, the BZ signal is output from the P40 (BZ) terminal.
When "0" is written, the P40 (BZ) terminal goes to low (VSS).
At initial reset, this register is set to "0".

Note: When using the P40 port as the BZ output port, fix the I/O control register (IOC40) at "1" (output), data register (P40) at "0" and the pull-down control register (PUL40) at "0" (pull-down disabled).

BZFQ0–BZFQ2: Buzzer frequency selection register (FF6EH•D0–D2)

Selects the buzzer signal frequency.

Table 4.11.7.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock.
At initial reset, this register is set to "0".

BDTY0–BDTY2: Duty level selection register (FF6FH•D0–D2)

Selects the duty ratio of the buzzer signal as shown in Table 4.11.7.3.

Table 4.11.7.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.
However, when the envelope has been set to on (ENON = "1"), this setting becomes invalid.
At initial reset, this register is set to "0".

ENRST: Envelope reset (FF6CH•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

Writing "1" into ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.
This bit is dedicated for writing, and is always "0" for reading.

ENON: Envelope On/Off control register (FF6CH•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: On
When "0" is written: Off
Reading: Valid

Writing "1" into the ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.
At initial reset, this register is set to "0".

ENRTM: Envelope releasing time selection register (FF6CH•D3)

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.
When "1" has been written in ENRTM, it becomes 125 msec (8 Hz) units and when "0" has been written, it becomes 62.5 msec (16 Hz) units.
At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width setting register (FF6DH•D0)

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

Writing "1" into SHTPW causes the one-short output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF6DH•D1)

Controls the one-shot buzzer output.

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output. This output is automatically turned off after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***When reading***

When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes off, it shifts to "0".
At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer stop (FF6DH•D2)

Stops the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Always "0"

Writing "1" into BZSTP permits the one-shot buzzer output to be turned off prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

EMPON: Buzzer output enable in motor pulse output period (FF6DH•D3)

Enables and disables buzzer output during the motor drive pulse output period.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

When EMPON is set to "1", the buzzer output is always enabled regardless of the motor drive pulse output status. When EMPON is set to "0", the buzzer signal is disabled to output only in the motor drive pulse output period. The period that does not output the pulses in a motor drive step cycle enables output of the buzzer signal.
At initial reset, this register is set to "0".

4.11.8 Programming notes

(1) When using the P40 port as the BZ output port, fix the I/O control register (IOC40) at "1" (output), data register (P40) at "0" and the pull-down control register (PUL40) at "0" (pull-down disabled).

(2) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(3) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

4.12 Motor Control Circuit

4.12.1 Configuration of motor control circuit

The S1C63709 contains 2-channel motor drivers capable of driving a stepping-motor for watches. Each motor driver is functionally different. The following describes 2-channel motors as motors 0 (M0) and 1 (M1); the motor drivers are called motor drivers 0 and 1. For the contents common to all motors (including control bit names), the motor numbers are denoted by 'x'.
Table 4.12.1.1 lists the features of each motor driver. Figure 4.12.1.1 shows a block diagram of the motor control circuit.

Table 4.12.1.1 Features of motor drivers 0 and 1

Motor driver	Drive method
Motor driver 0	Two drive modes controllable by software • Normal rotation drive by fixed pulse • Fast-feed drive in normal/reverse directions by fixed pulse
Motor driver 1	• Fast-feed drive in normal/reverse directions by fixed pulse

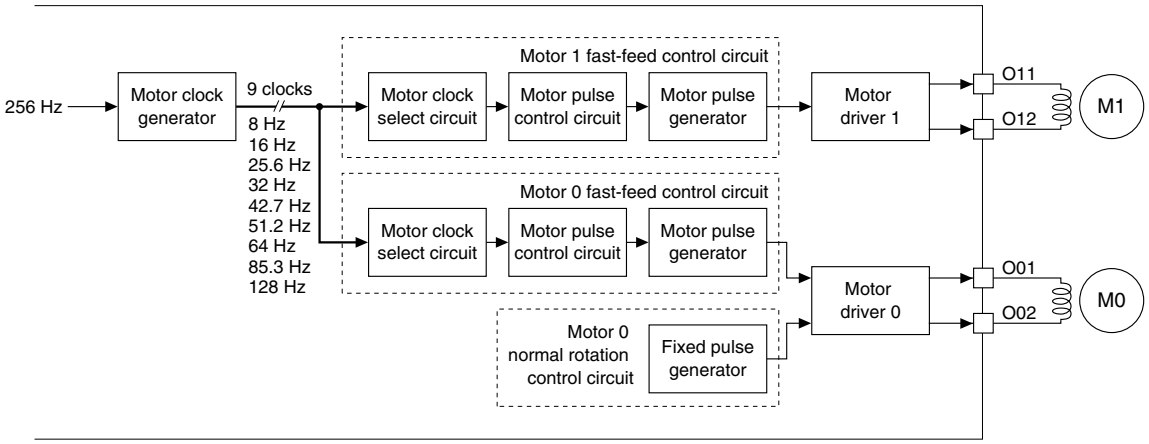


Fig. 4.12.1.1 Block diagram of motor control circuit

The following describes the functionality of each block of the motor control circuit. Circuit blocks are provided for each motor allowing control of the motors individually.

Motor clock generator circuit and motor clock select circuit

These two circuits select a motor clock with which to drive motors 0 and 1 for fast-feed drive. The motor clock generator circuit divides the 256-Hz clock to generate 8-Hz, 16-Hz, 25.6-Hz, 32-Hz, 42.7-Hz, 51.2-Hz, 64-Hz, 85.3-Hz, and 128-Hz clocks. The motor clock select circuit (provided separately for each motor) outputs one of these clocks (selected by software as the motor clock) to the motor pulse control circuit located in the next stage.

Motor pulse control circuit

This circuit controls the number of pulses (number of steps) to drive motors 0 and 1 for fast-feed drive. Software can set the number of fast-feed drive pulses for each motor. The motor pulse control circuit that counts the motor clock supplied by the motor clock select circuit outputs a given number of clocks (as set by software) to the motor pulse generator circuit located in the next stage.

Motor pulse generator circuit

This circuit generates pulses to drive a motor for fast-feed drive in the normal or reverse direction synchronously with the motor clock supplied by the motor pulse control circuit. Software selects the direction of rotation (normal or reverse). The generated drive pulses are fed to the respective motor drives.

Fixed pulse generator circuit

This circuit is provided for motor 0 for generating fixed pulses for normal rotation drive. These drive pulses are output to the motor driver 0. Software can control the pulse generation timing.

Motor drivers

These units drive the respective motors using the motor drive pulses generated by the circuits above. The following lists the output pins for each motor driver.
Motor driver 0 (for driving motor 0): O01 and O02 pins
Motor driver 1 (for driving motor 1): O11 and O12 pins

4.12.2 Mask option

Available mask options allow the fixed drive pulses output for motor 0 to be disabled while K13 input is held high (e.g., when winding crown is positioned where the time of day changes). (See Section 4.12.4.)

4.12.3 Fast-feed control (motors 0 and 1)

Motors 0 and 1 can be controlled independently of fast-feed operation for resetting the stopwatch function or second hand. A drive pulse generator circuit is provided for each motor, with the fast-feed speeds of respective motors selectable from nine frequencies by software.

Fast-feed drive pulses

The motor control circuit described here is capable of fast-feed drive in both normal and reverse rotation directions. Thus, the motor pulse generator circuit generates drive pulses for both normal and reverse rotation.

(1) Fast-feed drive pulse waveform for normal rotation

Figure 4.12.3.1 shows the fast-feed drive pulse waveform for normal rotation.

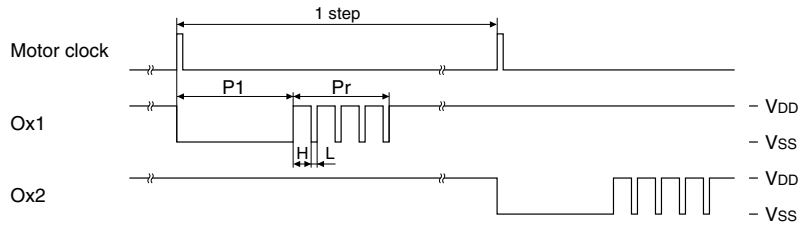


Fig. 4.12.3.1 Fast-feed drive pulse waveform for normal rotation

As shown in Figure 4.12.3.1, the fast-feed drive pulse waveform for normal rotation per motor rotation step consists of the P1 and Pr pulses. The drive pulses are output alternately from the Ox1 and Ox2 pins for each step (x = motor number) in synchronism with the motor clock.
The P1 pulse width, number of Pr pulses, and Pr pulse duty cycle can be set by using the control registers based on the motor used and motor clock frequency, as shown in Tables 4.12.3.1 and 4.12.3.2.

Table 4.12.3.1(a) Settings of fast-feed drive pulse waveform for normal rotation (1)

Recommended settings for 128-Hz motor clock

Motor clock (Hz)	P1 pulse width (msec)	Number of Pr pulses	Pulse output time (msec) *
128	2.93	4 or 0	6.836
	3.17	4 or 0	7.080
	3.42	4 or 0	7.324
	3.66	4 or 0	7.568
	3.91	3 (Pr duty = 1/4) 3.5 (Pr duty = 1/2) or 0	7.568

* The pulse output time is [P1 pulse width + 0.976 × number of Pr pulses]. (0.976 msec = Pr pulse period)

The number of Pr pulses can be set to 0 using the motor-x forced 0 Pr pulse select register MxPRDEL, note, however, that the pulse count set in the motor-x Pr pulses select registers MxPRNM1–MxPRNM0 must be substituted into the "number of Pr pulses" in the above equation to calculate the pulse output time.

Recommended settings for 85.3-Hz motor clock

Motor clock (Hz)	P1 pulse width (msec)	Number of Pr pulses	Pulse output time (msec) *
85.3	2.93	4 or 0	6.836
		6 or 0	8.789
		8 or 0	10.742
	3.17	4 or 0	7.080
		6 or 0	9.033
		8 or 0	10.986
	3.42	4 or 0	7.324
		6 or 0	9.277
		8 or 0	11.230
	3.66	4 or 0	7.568
		6 or 0	9.521
	3.91	4 or 0	7.813
		6 or 0	9.766
	4.15	4 or 0	8.057
		6 or 0	10.010
	4.39	4 or 0	8.301
		6 or 0	10.254
	4.64	4 or 0	8.545
		6 or 0	10.498
	4.88	4 or 0	8.789
		6 or 0	10.742
	5.13	4 or 0	9.033
		6 or 0	10.986
	5.37	4 or 0	9.277
		6 or 0	11.230
	5.62	4 or 0	9.521
	5.86	4 or 0	9.766
	6.1	4 or 0	10.010
	6.35	4 or 0	10.254
	6.59	4 or 0	10.498

Table 4.12.3.1(b) Settings of fast-feed drive pulse waveform for normal rotation (2)

Recommended settings for 64-Hz motor clock

Motor clock (Hz)	P1 pulse width (msec)	Number of Pr pulses	Pulse output time (msec) *
64	2.93	4 or 0	6.836
		6 or 0	8.789
		8 or 0	10.742
		10 or 0	12.695
	3.17	4 or 0	7.080
		6 or 0	9.033
		8 or 0	10.986
		10 or 0	12.939
	3.42	4 or 0	7.324
		6 or 0	9.277
		8 or 0	11.230
		10 or 0	13.184
	3.66	4 or 0	7.568
		6 or 0	9.521
		8 or 0	11.475
		10 or 0	13.428
	3.91	4 or 0	7.813
		6 or 0	9.766
		8 or 0	7.813
		10 or 0	13.672
	4.15	4 or 0	8.057
		6 or 0	10.010
		8 or 0	11.963
		10 or 0	13.916
	4.39	4 or 0	8.301
		6 or 0	10.254
		8 or 0	12.207
		10 or 0	14.160
	4.64	4 or 0	8.545
		6 or 0	10.498
		8 or 0	12.451
		10 or 0	14.404
	4.88	4 or 0	8.789
		6 or 0	10.742
		8 or 0	12.695
		10 or 0	14.648
	5.13	4 or 0	9.033
		6 or 0	10.986
		8 or 0	12.939
		10 or 0	14.893
	5.37	4 or 0	9.277
		6 or 0	11.230
		8 or 0	13.184
		10 or 0	15.137
	5.62	4 or 0	9.521
		6 or 0	11.475
		8 or 0	13.428
	5.86	4 or 0	9.766
		6 or 0	11.719
		8 or 0	13.672
	6.1	4 or 0	10.010
		6 or 0	11.963
		8 or 0	13.916
	6.35	4 or 0	10.254
		6 or 0	12.207
		8 or 0	14.160
	6.59	4 or 0	10.498
		6 or 0	12.451
		8 or 0	14.404

Motor clock (Hz)	P1 pulse width (msec)	Number of Pr pulses	Pulse output time (msec) *
(128)	2.93	4 or 0	6.836
(85.3)		6 or 0	8.789
(64)		8 or 0	10.742
51.2		10 or 0	12.695
42.7	3.17	4 or 0	7.080
32		6 or 0	9.033
25.6		8 or 0	10.986
16		10 or 0	12.939
8	3.42	4 or 0	7.324
		6 or 0	9.277
		8 or 0	11.230
		10 or 0	13.184
	3.66	4 or 0	7.568
		6 or 0	9.521
		8 or 0	11.475
		10 or 0	13.428
	3.91	4 or 0	7.813
		6 or 0	9.766
		8 or 0	7.813
		10 or 0	13.672
	4.15	4 or 0	8.057
		6 or 0	10.010
		8 or 0	11.963
		10 or 0	13.916
	4.39	4 or 0	8.301
		6 or 0	10.254
		8 or 0	12.207
		10 or 0	14.160
	4.64	4 or 0	8.545
		6 or 0	10.498
		8 or 0	12.451
		10 or 0	14.404
	4.88	4 or 0	8.789
		6 or 0	10.742
		8 or 0	12.695
		10 or 0	14.648
	5.13	4 or 0	9.033
		6 or 0	10.986
		8 or 0	12.939
		10 or 0	14.893
	5.37	4 or 0	9.277
		6 or 0	11.230
		8 or 0	13.184
		10 or 0	15.137
	5.62	4 or 0	9.521
		6 or 0	11.475
		8 or 0	13.428
		10 or 0	15.381
	5.86	4 or 0	9.766
		6 or 0	11.719
		8 or 0	13.672
		10 or 0	15.625
	6.1	4 or 0	10.010
		6 or 0	11.963
		8 or 0	13.916
		10 or 0	15.869
	6.35	4 or 0	10.254
		6 or 0	12.207
		8 or 0	14.160
		10 or 0	16.113
	6.59	4 or 0	10.498
		6 or 0	12.451
		8 or 0	14.404
		10 or 0	16.357

* The pulse output time is
[P1 pulse width + 0.976 × number of Pr pulses].
(0.976 msec = Pr pulse period)

The number of Pr pulses can be set to 0 using the motor-x forced 0 Pr pulse select register MxPRDEL, note, however, that the pulse count set in the motor-x Pr pulses select registers MxPRNM1–MxPRNM0 must be substituted into the "number of Pr pulses" in the above equation to calculate the pulse output time.

Table 4.12.3.2 Pr pulse duty cycle

Duty cycle	High period (msec)	Low period (msec)
1/2	0.488	0.488
1/4	0.732	0.244

(2) Fast-feed drive pulse waveform for reverse rotation

Figure 4.12.3.2 shows the fast-feed drive pulse waveform for reverse rotation.

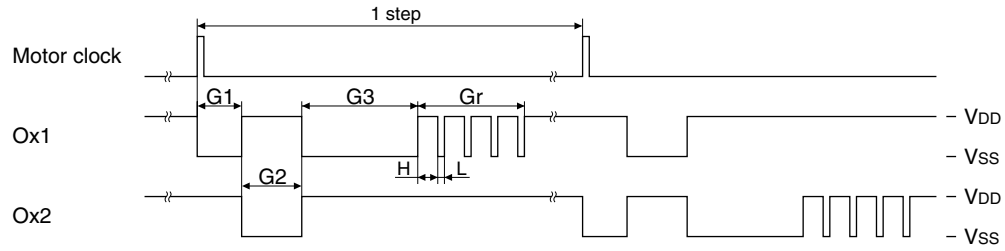


Fig. 4.12.3.2 Fast-feed drive pulse waveform for reverse rotation

As shown in Figure 4.12.3.2, the fast-feed drive pulse waveform for reverse rotation per motor rotation step consists of the G1, G2, G3 and Gr pulses.
The drive pulses are output alternately from the Ox1 and Ox2 pins for each step in synchronism with the motor clock.
The G1, G2 and G3 pulse widths, number of Gr pulses, and Gr pulse duty cycle can be set by using the control registers based on the motor used, as shown in Tables 4.12.3.3 and 4.12.3.4.

Table 4.12.3.3(a) Settings of fast-feed drive pulse waveform for reverse rotation (1)

G1 pulse width (msec)	G2 pulse width (msec)	G3 pulse width (msec)	Number of Gr pulses	G1 + G2 (msec)	G1 + G2 + G3 (msec)	Drive pulse output time (msec) *
0.49	1.71	4.88	4 (3.91 msec)	2.20	7.08	10.986
			8 (7.81 msec)	2.20	7.08	14.893
		6.84	4 (3.91 msec)	2.20	9.03	12.939
			8 (7.81 msec)	2.20	9.03	16.846
	1.95	4.88	4 (3.91 msec)	2.44	7.32	11.230
			8 (7.81 msec)	2.44	7.32	15.137
		6.84	4 (3.91 msec)	2.44	9.28	13.184
			8 (7.81 msec)	2.44	9.28	17.090
	2.20	4.88	4 (3.91 msec)	2.69	7.57	11.475
			8 (7.81 msec)	2.69	7.57	15.381
		6.84	4 (3.91 msec)	2.69	9.52	13.428
			8 (7.81 msec)	2.69	9.52	17.334
	2.44	4.88	4 (3.91 msec)	2.93	7.81	11.719
			8 (7.81 msec)	2.93	7.81	15.625
		6.84	4 (3.91 msec)	2.93	9.77	13.672
			8 (7.81 msec)	2.93	9.77	17.578
	2.69	4.88	4 (3.91 msec)	3.17	8.06	11.963
			8 (7.81 msec)	3.17	8.06	15.869
		6.84	4 (3.91 msec)	3.17	10.01	13.916
			8 (7.81 msec)	3.17	10.01	17.822
	2.93	4.88	4 (3.91 msec)	3.42	8.30	12.207
			8 (7.81 msec)	3.42	8.30	16.113
		6.84	4 (3.91 msec)	3.42	10.25	14.160
			8 (7.81 msec)	3.42	10.25	18.066
	3.17	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	3.42	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555

Table 4.12.3.3(b) Settings of fast-feed drive pulse waveform for reverse rotation (2)

G1 pulse width (msec)	G2 pulse width (msec)	G3 pulse width (msec)	Number of Gr pulses	G1 + G2 (msec)	G1 + G2 + G3 (msec)	Drive pulse output time (msec) *
0.73	1.71	4.88	4 (3.91 msec)	2.44	7.32	11.230
			8 (7.81 msec)	2.44	7.32	15.137
		6.84	4 (3.91 msec)	2.44	9.28	13.184
			8 (7.81 msec)	2.44	9.28	17.090
	1.95	4.88	4 (3.91 msec)	2.69	7.57	11.475
			8 (7.81 msec)	2.69	7.57	15.381
		6.84	4 (3.91 msec)	2.69	9.52	13.428
			8 (7.81 msec)	2.69	9.52	17.334
	2.20	4.88	4 (3.91 msec)	2.93	7.81	11.719
			8 (7.81 msec)	2.93	7.81	15.625
		6.84	4 (3.91 msec)	2.93	9.77	13.672
			8 (7.81 msec)	2.93	9.77	17.578
	2.44	4.88	4 (3.91 msec)	3.17	8.06	11.963
			8 (7.81 msec)	3.17	8.06	15.869
		6.84	4 (3.91 msec)	3.17	10.01	13.916
			8 (7.81 msec)	3.17	10.01	17.822
	2.69	4.88	4 (3.91 msec)	3.42	8.30	12.207
			8 (7.81 msec)	3.42	8.30	16.113
		6.84	4 (3.91 msec)	3.42	10.25	14.160
			8 (7.81 msec)	3.42	10.25	18.066
	2.93	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	3.17	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	3.42	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
0.98	1.71	4.88	4 (3.91 msec)	2.69	7.57	11.475
			8 (7.81 msec)	2.69	7.57	15.381
		6.84	4 (3.91 msec)	2.69	9.52	13.428
			8 (7.81 msec)	2.69	9.52	17.334
	1.95	4.88	4 (3.91 msec)	2.93	7.81	11.719
			8 (7.81 msec)	2.93	7.81	15.625
		6.84	4 (3.91 msec)	2.93	9.77	13.672
			8 (7.81 msec)	2.93	9.77	17.578
	2.20	4.88	4 (3.91 msec)	3.17	8.06	11.963
			8 (7.81 msec)	3.17	8.06	15.869
		6.84	4 (3.91 msec)	3.17	10.01	13.916
			8 (7.81 msec)	3.17	10.01	17.822
	2.44	4.88	4 (3.91 msec)	3.42	8.30	12.207
			8 (7.81 msec)	3.42	8.30	16.113
		6.84	4 (3.91 msec)	3.42	10.25	14.160
			8 (7.81 msec)	3.42	10.25	18.066
	2.69	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	2.93	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	3.17	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
	3.42	4.88	4 (3.91 msec)	4.39	9.28	13.184
			8 (7.81 msec)	4.39	9.28	17.090
		6.84	4 (3.91 msec)	4.39	11.23	15.137
			8 (7.81 msec)	4.39	11.23	19.043

Table 4.12.3.3(c) Settings of fast-feed drive pulse waveform for reverse rotation (3)

G1 pulse width (msec)	G2 pulse width (msec)	G3 pulse width (msec)	Number of Gr pulses	G1 + G2 (msec)	G1 + G2 + G3 (msec)	Drive pulse output time (msec) *
1.22	1.71	4.88	4 (3.91 msec)	2.93	7.81	11.719
			8 (7.81 msec)	2.93	7.81	15.625
		6.84	4 (3.91 msec)	2.93	9.77	13.672
			8 (7.81 msec)	2.93	9.77	17.578
	1.95	4.88	4 (3.91 msec)	3.17	8.06	11.963
			8 (7.81 msec)	3.17	8.06	15.869
		6.84	4 (3.91 msec)	3.17	10.01	13.916
			8 (7.81 msec)	3.17	10.01	17.822
	2.20	4.88	4 (3.91 msec)	3.42	8.30	12.207
			8 (7.81 msec)	3.42	8.30	16.113
		6.84	4 (3.91 msec)	3.42	10.25	14.160
			8 (7.81 msec)	3.42	10.25	18.066
	2.44	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	2.69	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	2.93	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
	3.17	4.88	4 (3.91 msec)	4.39	9.28	13.184
			8 (7.81 msec)	4.39	9.28	17.090
		6.84	4 (3.91 msec)	4.39	11.23	15.137
			8 (7.81 msec)	4.39	11.23	19.043
	3.42	4.88	4 (3.91 msec)	4.64	9.52	13.428
			8 (7.81 msec)	4.64	9.52	17.334
		6.84	4 (3.91 msec)	4.64	11.47	15.381
			8 (7.81 msec)	4.64	11.47	19.287
1.46	1.71	4.88	4 (3.91 msec)	3.17	8.06	11.963
			8 (7.81 msec)	3.17	8.06	15.869
		6.84	4 (3.91 msec)	3.17	10.01	13.916
			8 (7.81 msec)	3.17	10.01	17.822
	1.95	4.88	4 (3.91 msec)	3.42	8.30	12.207
			8 (7.81 msec)	3.42	8.30	16.113
		6.84	4 (3.91 msec)	3.42	10.25	14.160
			8 (7.81 msec)	3.42	10.25	18.066
	2.20	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	2.44	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	2.69	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
	2.93	4.88	4 (3.91 msec)	4.39	9.28	13.184
			8 (7.81 msec)	4.39	9.28	17.090
		6.84	4 (3.91 msec)	4.39	11.23	15.137
			8 (7.81 msec)	4.39	11.23	19.043
	3.17	4.88	4 (3.91 msec)	4.64	9.52	13.428
			8 (7.81 msec)	4.64	9.52	17.334
		6.84	4 (3.91 msec)	4.64	11.47	15.381
			8 (7.81 msec)	4.64	11.47	19.287
	3.42	4.88	4 (3.91 msec)	4.88	9.77	13.672
			8 (7.81 msec)	4.88	9.77	17.578
		6.84	4 (3.91 msec)	4.88	11.72	15.625
			8 (7.81 msec)	4.88	11.72	19.531

Table 4.12.3.3(d) Settings of fast-feed drive pulse waveform for reverse rotation (4)

G1 pulse width (msec)	G2 pulse width (msec)	G3 pulse width (msec)	Number of Gr pulses	G1 + G2 (msec)	G1 + G2 + G3 (msec)	Drive pulse output time (msec) *
1.71	1.71	4.88	4 (3.91 msec)	3.42	8.30	12.207
			8 (7.81 msec)	3.42	8.30	16.113
		6.84	4 (3.91 msec)	3.42	10.25	14.160
			8 (7.81 msec)	3.42	10.25	18.066
	1.95	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	2.20	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	2.44	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
	2.69	4.88	4 (3.91 msec)	4.39	9.28	13.184
			8 (7.81 msec)	4.39	9.28	17.090
		6.84	4 (3.91 msec)	4.39	11.23	15.137
			8 (7.81 msec)	4.39	11.23	19.043
	2.93	4.88	4 (3.91 msec)	4.64	9.52	13.428
			8 (7.81 msec)	4.64	9.52	17.334
		6.84	4 (3.91 msec)	4.64	11.47	15.381
			8 (7.81 msec)	4.64	11.47	19.287
	3.17	4.88	4 (3.91 msec)	4.88	9.77	13.672
			8 (7.81 msec)	4.88	9.77	17.578
		6.84	4 (3.91 msec)	4.88	11.72	15.625
			8 (7.81 msec)	4.88	11.72	19.531
	3.42	4.88	4 (3.91 msec)	5.13	10.01	13.916
			8 (7.81 msec)	5.13	10.01	17.822
		6.84	4 (3.91 msec)	5.13	11.96	15.869
			8 (7.81 msec)	5.13	11.96	19.775
1.95	1.71	4.88	4 (3.91 msec)	3.66	8.54	12.451
			8 (7.81 msec)	3.66	8.54	16.357
		6.84	4 (3.91 msec)	3.66	10.50	14.404
			8 (7.81 msec)	3.66	10.50	18.311
	1.95	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	2.20	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
	2.44	4.88	4 (3.91 msec)	4.39	9.28	13.184
			8 (7.81 msec)	4.39	9.28	17.090
		6.84	4 (3.91 msec)	4.39	11.23	15.137
			8 (7.81 msec)	4.39	11.23	19.043
	2.69	4.88	4 (3.91 msec)	4.64	9.52	13.428
			8 (7.81 msec)	4.64	9.52	17.334
		6.84	4 (3.91 msec)	4.64	11.47	15.381
			8 (7.81 msec)	4.64	11.47	19.287
	2.93	4.88	4 (3.91 msec)	4.88	9.77	13.672
			8 (7.81 msec)	4.88	9.77	17.578
		6.84	4 (3.91 msec)	4.88	11.72	15.625
			8 (7.81 msec)	4.88	11.72	19.531
	3.17	4.88	4 (3.91 msec)	5.13	10.01	13.916
			8 (7.81 msec)	5.13	10.01	17.822
		6.84	4 (3.91 msec)	5.13	11.96	15.869
			8 (7.81 msec)	5.13	11.96	19.775
	3.42	4.88	4 (3.91 msec)	5.37	10.25	14.160
			8 (7.81 msec)	5.37	10.25	18.066
		6.84	4 (3.91 msec)	5.37	12.21	16.113
			8 (7.81 msec)	5.37	12.21	20.020

Table 4.12.3.3(e) Settings of fast-feed drive pulse waveform for reverse rotation (5)

G1 pulse width (msec)	G2 pulse width (msec)	G3 pulse width (msec)	Number of Gr pulses	G1 + G2 (msec)	G1 + G2 + G3 (msec)	Drive pulse output time (msec) *
2.20	1.71	4.88	4 (3.91 msec)	3.91	8.79	12.695
			8 (7.81 msec)	3.91	8.79	16.602
		6.84	4 (3.91 msec)	3.91	10.74	14.648
			8 (7.81 msec)	3.91	10.74	18.555
	1.95	4.88	4 (3.91 msec)	4.15	9.03	12.939
			8 (7.81 msec)	4.15	9.03	16.846
		6.84	4 (3.91 msec)	4.15	10.99	14.893
			8 (7.81 msec)	4.15	10.99	18.799
	2.20	4.88	4 (3.91 msec)	4.39	9.28	13.184
			8 (7.81 msec)	4.39	9.28	17.090
		6.84	4 (3.91 msec)	4.39	11.23	15.137
			8 (7.81 msec)	4.39	11.23	19.043
	2.44	4.88	4 (3.91 msec)	4.64	9.52	13.428
			8 (7.81 msec)	4.64	9.52	17.334
		6.84	4 (3.91 msec)	4.64	11.47	15.381
			8 (7.81 msec)	4.64	11.47	19.287
	2.69	4.88	4 (3.91 msec)	4.88	9.77	13.672
			8 (7.81 msec)	4.88	9.77	17.578
		6.84	4 (3.91 msec)	4.88	11.72	15.625
			8 (7.81 msec)	4.88	11.72	19.531
	2.93	4.88	4 (3.91 msec)	5.13	10.01	13.916
			8 (7.81 msec)	5.13	10.01	17.822
		6.84	4 (3.91 msec)	5.13	11.96	15.869
			8 (7.81 msec)	5.13	11.96	19.775
	3.17	4.88	4 (3.91 msec)	5.37	10.25	14.160
			8 (7.81 msec)	5.37	10.25	18.066
		6.84	4 (3.91 msec)	5.37	12.21	16.113
			8 (7.81 msec)	5.37	12.21	20.020
	3.42	4.88	4 (3.91 msec)	5.62	10.50	14.404
			8 (7.81 msec)	5.62	10.50	18.311
		6.84	4 (3.91 msec)	5.62	12.45	16.357
			8 (7.81 msec)	5.62	12.45	20.264

* The drive pulse output time is [G1 pulse width + G2 pulse width + G3 pulse width + 0.976 × number of Gr pulses]. (0.976 msec = Gr pulse period)

Note: The control registers must be set so that the drive pulse output time is less than one cycle of the motor clock.

Table 4.12.3.4 Gr pulse duty cycle

Duty cycle	High period (msec)	Low period (msec)
1/2	0.488	0.488
1/4	0.732	0.244

Items to be set before fast-feed drive

The following describes the items that must be selected or set before executing fast-feed drive.

(1) Selecting the motor clock

The fast-feed drive pulses are output synchronously with the motor clock, as shown in Figures 4.12.3.1 and 4.12.3.2. Consequently, the motor rotation speed is determined by the motor clock frequency. This motor clock is one of eight clocks (16 Hz, 25.6 Hz, 32 Hz, 42.7 Hz, 51.2 Hz, 64 Hz, 85.3 Hz, or 128 Hz) output by the motor clock generator circuit as selected by software. The motor clock select registers MxCLS2–MxCLS0 are used to select these clocks, as shown in Table 4.12.3.5.

Table 4.12.3.5 Selection of motor clock

MxCLS2	MxCLS1	MxCLS0	Motor clock frequency
1	1	1	128 Hz
1	1	0	85.3 Hz
1	0	1	64 Hz
1	0	0	51.2 Hz
0	1	1	42.7 Hz
0	1	0	32 Hz
0	0	1	25.6 Hz
0	0	0	16 Hz

At initial reset, the motor clock frequency is set to 128 Hz.
Furthermore, an 8-Hz motor clock can be selected by writing "1" to the 8-Hz motor clock select register MxCL8HZ. In this case, the MxCLS register setting is ignored (the MxCLS register is effective only when MxCL8HZ = "0").

The motor clocks are changed over in synchronism with the currently active motor clock. In other words, when an MxCLS register is altered by software, the motor clocks are changed over at the end of the motor clock cycle in which the register was altered. (See Figure 4.12.3.3.) Consequently, before the motor clocks are actually changed over after a register is altered, there is a delay of up to one cycle of the active clock before the changeover.

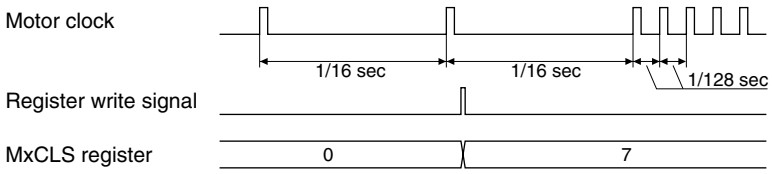


Fig. 4.12.3.3 Timing of motor clock changeover

(2) Setting drive pulse specifications

Set the specifications of fast-feed drive pulses for normal and reverse rotation exactly as described in "Fast-feed drive pulses" above.

Fast-feed drive pulses for normal rotation

P1 pulse width

Use the motor-x P1 pulse width select registers MxP1LN3–MxP1LN0 to select, as shown in Table 4.12.3.6.

Table 4.12.3.6 Selecting the P1 pulse width

MxP1LN3	MxP1LN2	MxP1LN1	MxP1LN0	P1 pulse width
1	1	1	1	6.59 msec
1	1	1	0	6.35 msec
1	1	0	1	6.10 msec
1	1	0	0	5.86 msec
1	0	1	1	5.62 msec
1	0	1	0	5.37 msec
1	0	0	1	5.13 msec
1	0	0	0	4.88 msec
0	1	1	1	4.64 msec
0	1	1	0	4.39 msec
0	1	0	1	4.15 msec
0	1	0	0	3.91 msec
0	0	1	1	3.66 msec
0	0	1	0	3.42 msec
0	0	0	1	3.17 msec
0	0	0	0	2.93 msec

At initial reset, the P1 pulse width is set to 2.93 msec.

Number of Pr pulses

Use the motor-x Pr pulses select registers MxPRNM1–MxPRNM0 to select, as shown in Table 4.12.3.7.

Table 4.12.3.7 Selecting the number of Pr pulses

MxPRNM1	MxPRNM0	Number of Pr pulses
1	1	10 pulses (Pr width = 9.77 msec)
1	0	8 pulses (Pr width = 7.81 msec)
0	1	6 pulses (Pr width = 5.86 msec)
0	0	4 pulses (Pr width = 3.91 msec)

At initial reset, the number of Pr pulses is set to 4.
Furthermore, the number of Pr pulses can forcibly be set to 0 by writing "1" to the motor-x forced 0 Pr pulse select register MxPRDEL. In this case, the MxPRNM register setting is ignored (the MxPRNM register is effective only when MxPRDEL = "0"). However, the pulse output time includes the time equivalent to the number of Pr pulses specified by MxPRNM (it is not reduced to the P1 pulse width).

Pr pulse duty cycle

Use the motor-x Pr pulse duty cycle select register MxPRDY to select.
MxPRDY = "1": 1/2 (high for 0.488 msec, low for 0.488 msec)
MxPRDY = "0": 1/4 (high for 0.732 msec, low for 0.244 msec)

At initial reset, the Pr pulse duty cycle is set to 1/4.

Note: If the sum total of the P1 and Pr pulses exceeds the motor clock cycle, the Pr pulse output is forcibly terminated before the next motor clock output is started. In this case, a hazard may occur on the waveform at forced termination of the Pr pulse output. Therefore, always be sure that said sum total is less than the motor clock cycle.
The table below shows the actual P1 and Pr output period (or the time from start of the pulse output until the Pr pulse output is terminated) when the setting of the P1 and Pr pulses exceeds the motor clock cycle.

Table 4.12.3.8 Drive pulse output period when Pr pulse is forcibly terminated

Motor clock	Forced terminating conditions	Drive pulse output period
128 Hz	[P1+Pr] > 7.324 msec	7.568 msec
85.3 Hz	[P1+Pr] > 11.230 msec	11.475 msec
64 Hz	[P1+Pr] > 15.137 msec	15.381 msec

Fast-feed drive pulses for reverse rotation

G1 pulse width

Use the motor-x G1 pulse width select registers MxG1LN2–MxG1LN0 to select, as shown in Table 4.12.3.9.

Table 4.12.3.9 Selecting the G1 pulse width

MxG1LN2	MxG1LN1	MxG1LN0	G1 pulse width
1	1	1	0.49 msec
1	1	0	2.20 msec
1	0	1	1.95 msec
1	0	0	1.71 msec
0	1	1	1.46 msec
0	1	0	1.22 msec
0	0	1	0.98 msec
0	0	0	0.73 msec

At initial reset, the G1 pulse width is set to 0.73 msec.

G2 pulse width

Use the motor-x G2 pulse width select registers MxG2LN2–MxG2LN0 to select, as shown in Table 4.12.3.10.

Table 4.12.3.10 Selecting the G2 pulse width

MxG2LN2	MxG2LN1	MxG2LN0	G2 pulse width
1	1	1	3.42 msec
1	1	0	3.17 msec
1	0	1	2.93 msec
1	0	0	2.69 msec
0	1	1	2.44 msec
0	1	0	2.20 msec
0	0	1	1.95 msec
0	0	0	1.71 msec

At initial reset, the G2 pulse width is set to 1.71 msec.

G3 pulse width

Use the motor-x G3 pulse width select register MxG3LN to select.
MxG3LN = "1": 6.84 msec
MxG3LN = "0": 4.88 msec

At initial reset, the G3 pulse width is set to 4.88 msec.

Number of Gr pulses

Use the motor-x Gr pulses select register MxGRNM to select.
MxGRNM = "1": 8 pulses (Gr width = 7.81 msec)
MxGRNM = "0": 4 pulses (Gr width = 3.91 msec)

At initial reset, the number of Gr pulses is set to 4.

Gr pulse duty cycle

Use the motor-x Gr pulse duty cycle select register MxGRDY to select.
MxGRDY = "1": 1/2 (high for 0.488 msec, low for 0.488 msec)
MxGRDY = "0": 1/4 (high for 0.732 msec, low for 0.244 msec)

At initial reset, the Gr pulse duty cycle is set to 1/4.

Note: If the sum total of the G1, G2, G3, and Gr pulses exceeds the motor clock cycle, the motor driver will not operate normally. Always be sure that said sum total is less than the motor clock cycle.

(3) Selecting the direction of rotation (normal or reverse)

The direction of motor rotation can be selected individually for each motor by using the motor pulse normal/reverse select register MxPSEL.
Writing "1" to MxPSEL selects reverse rotation, so that the fast-feed pulse for reverse rotation is output from the motor driver during motor drive. Writing "0" to MxPSEL selects normal rotation, so that the fast-feed pulse for normal rotation is output from the motor driver during motor drive.
At initial reset, normal rotation is selected.

(4) Setting the number of motor drive pulses

Software sets the number of motor drive pulses for each motor, and the motor pulse control circuit controls this number. Figure 4.12.3.4 shows the configuration of the motor pulse control circuit.

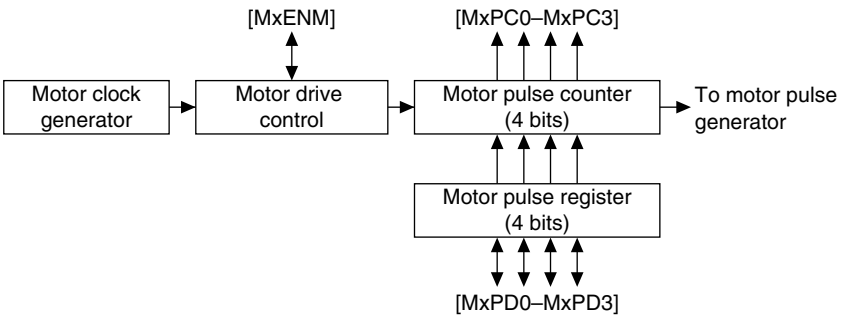


Fig. 4.12.3.4 Configuration of motor pulse control circuit

The motor pulse control circuit has built-in motor pulse registers MxPD3–MxPD0 to set the number of motor drive pulses. Write the number of motor drive pulses to these registers.
The data set in the MxPD registers are loaded into the motor pulse counters MxPC3–MxPC0 used to count the motor clock. The following describes the timing at which data written to the MxPD registers is loaded into the motor pulse counters.

1. When data is written to an MxPD register while the motor pulse counter = 0, the written data is loaded from the register into the counter at the same time.
2. When the motor pulse counter reaches terminal count 0 during fast-feed drive, data written to an MxPD register is loaded into the counter.

Unless the motor pulse counter = 0 (regardless of whether the motor is idle or being driven), data written to an MxPD register is retained there and not loaded into the counter until count 0 is reached. The MxPD register is cleared to 0 when its stored data has been loaded into the motor pulse counter. Software can read data from and write data to a motor pulse register MxPD. The value read from a register is the data written to that register if accessed for read before being loaded into the counter, and 0 if accessed for read after being loaded into the counter. The motor pulse counter MxPC can only be read when accessed by software. At initial reset, the registers and counters are both set to 0.
Because each MxPD register is 4 bits wide, the number of pulses that can be set at one time is limited to 15 steps of motor rotation. However, pulses can be output consecutively for more than 15 steps of motor rotation by using a motor interrupt (described next) to repeatedly write additional steps.
Before starting fast-feed drive, make sure the appropriate value is written to an MxPD register. That is, write a value that matches the number of motor rotation steps when the number of drive pulses is less than 15 steps, or write 15 when the number of drive pulses is 15 steps or more. Although the motor pulse counter may contain a remaining count due to fast-feed drive being stopped (described later), the motor pulse counter is assumed to have been loaded with the value written to an MxPD register for simplified explanatory purposes.

Fast-feed control and motor interrupt

Before executing fast-feed drive, be sure to set each item described above (i.e., motor clock, drive pulse specification, normal/reverse rotation, number of initial motor drive pulses) in software.

(1) Starting fast-feed drive

Before starting fast-feed drive, write "1" to the motor drive control register MxENM. After this write operation, the drive pulse for the first step is output from one output pin (Ox1 or Ox2) synchronously with the first rise of the motor clock. The motor pulse counter then counts down (i.e., decremented by 1). The drive pulse for the second step is output from the other output pin at the next rise of the motor clock. Subsequent drive pulses are output the same way until the motor pulse counter reaches terminal count 0.

When the motor must be turned 15 steps or more, make sure the remaining number of drive pulses is written to an MxPD register before the motor pulse counter reaches 0 (or immediately after starting fast-feed drive).

When data is written to the motor pulse register while MxENM = "1" and the motor pulse register and motor pulse counter are both = 0, the motor driver starts outputting the drive pulse synchronously with the first rise of the motor clock. Therefore, it normally does not matter whether MxENM remains set to "1" when data is written to the motor pulse register.

(2) Checking driver status during drive

The remaining number of steps and motor driver status can be checked during fast-feed drive.

Motor RUN/STOP

The motor drive control register MxENM is readable as well as writable, so that when accessed for read after writing "1", MxENM reads "1" until value "0" is written to it. However, because the register also reads "1" when the motor pulse counter = 0, this does not necessarily indicate that the motor is turning. Therefore, another read-only bit MxRUNM is provided. MxRUNM is the bit used to indicate that the motor is turning, so that when MxENM is "1" and the motor pulse counter is not 0, MxRUNM = "1". (See Figures 4.12.3.5 and 4.12.3.6.)

Drive pulse output pins

The drive pulses are output alternately from the Ox1 and Ox2 pins for each step in synchronism with the motor clock. By reading out the MxPOL bit, it is possible to determine from which pin the next drive pulse will be output. When MxPOL = "0", the drive pulse is output from the Ox1 pin; otherwise, it is output from the Ox2 pin.

Remaining number of steps

The number of drive steps that currently remain can be determined by adding the values together that are read out from the motor pulse register MxPD and motor pulse counter MxPC.

(3) Motor interrupt and end of fast-feed drive

When the motor pulse counter reaches terminal count 0, the motor interrupt factor flag ISMDx is set to "1", thereby generating a motor interrupt. Specifically, this interrupt is generated at the same time the motor driver starts outputting the last drive pulse synchronously with the rising transition of the motor clock, at which the motor pulse counter reaches 0. The interrupt mask register EISMDx can be used to mask the interrupt factor. When EISMDx is set to "1", a motor interrupt is generated to the CPU. When EISMDx is set to "0", no interrupts are generated to the CPU (although the interrupt factor flag is set to "1"). Note that writing "1" resets the motor interrupt factor flag ISMDx.

When a motor interrupt occurs, the MxPD register data is loaded into the motor pulse counter at the same time the interrupt is generated.

At this time, fast-feed drive terminates if the content of the MxPD register is 0. Thus, there is no need to write "0" to the MxENM register to terminate fast-feed drive.

If the content of the MxPD register is not 0 (with data written to it before the interrupt occurred), the data is loaded into the motor pulse counter and the motor driver continues outputting drive pulses for a number of steps equal to the loaded data. In this way, it is possible to turn the motor more than 15 consecutive steps.

Since the MxPD register is cleared to 0 when its data is loaded into the motor pulse counter, the next data can be written to the register. If the motor must be turned another 15 steps or more, use this interrupt function to write data to the MxPD register.

Figure 4.12.3.5 shows the timing chart for fast-feed drive. Note that 50 steps of fast-feed operation are shown as an example.

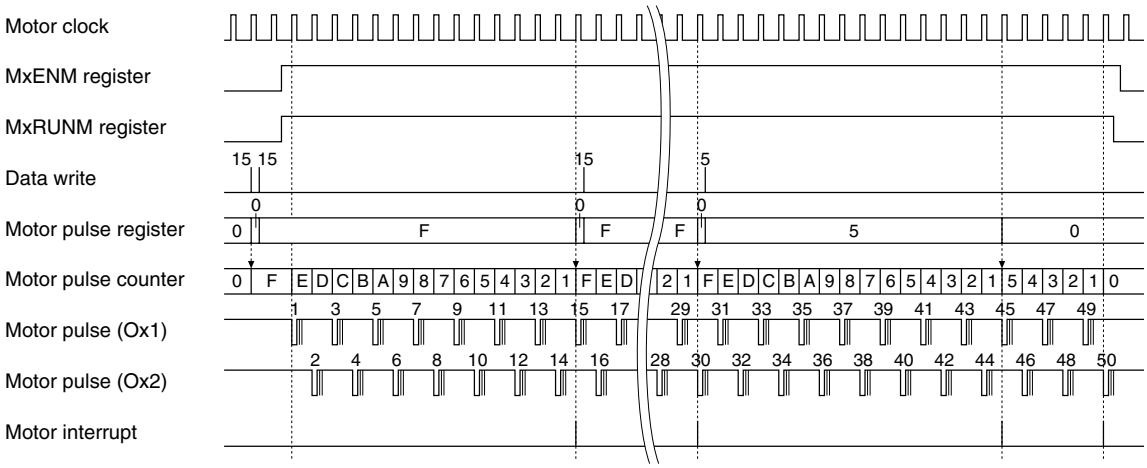


Fig. 4.12.3.5 Timing chart for fast-feed drive

(4) Temporarily stopping and aborting drive

To temporarily stop motor rotation, write "0" to MxENM. If this write operation occurs while the motor driver is outputting a drive pulse, the motor does not stop until after the motor driver outputs the pulse. The motor pulse register and counter both retain the contents held at that time.
To restart drive, write "1" to MxENM. The motor driver will restart outputting drive pulses beginning with the value retained in the counter.

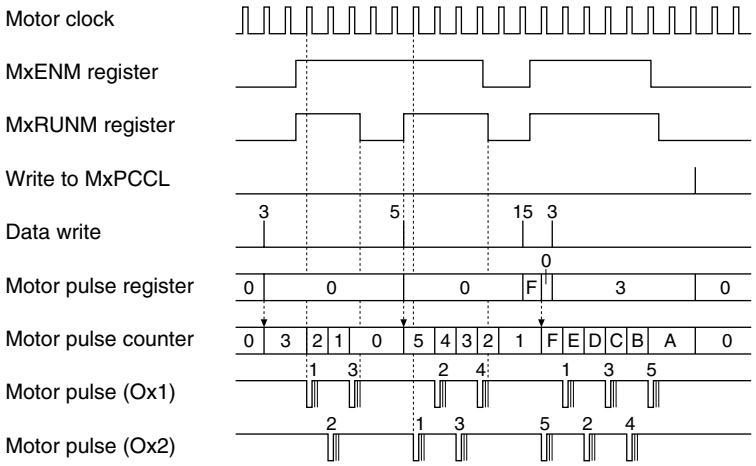


Fig. 4.12.3.6 Timing of temporary stop

To abort drive, first write "0" to MxENM to temporarily stop the motor. Then write "1" to the motor pulse counter clear register MxPCCL. The motor pulse register and motor pulse counter both will be cleared to 0.

Note: To abort drive, always be sure to temporarily stop the motor (MxENM = "0") before clearing the motor pulse counter. Clearing the counter during drive may cause the motor driver to operate erratically.

4.12.4 K2 fixed drive control (motor 0)

Motor 0 is assumed to be used as the main motor, and therefore it can be driven in the direction of normal rotation by applying a fixed drive pulse. Software controls each step of the drive pulse output timing.

Fixed drive pulse (K2 and Kr pulses) and demagnetization pulse (KE pulse)

Figure 4.12.4.1 shows the waveform of the fixed drive pulse.

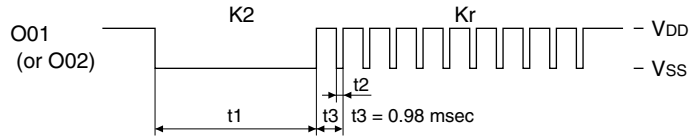


Fig. 4.12.4.1 Fixed drive pulse

The fixed drive pulse consists of the K2 and Kr pulses.
Control registers can be used to set the specifications of the fixed drive pulse based on the motor used.

K2 pulse width (t1 in the diagram)

The K2 pulse width can be selected from the following 16 available choices:

1) 3.42 msec 2) 3.66 msec 3) 3.91 msec 4) 4.15 msec 5) 4.39 msec 6) 4.64 msec
7) 4.88 msec 8) 5.13 msec 9) 5.37 msec 10) 5.62 msec 11) 5.86 msec 12) 6.10 msec
13) 6.35 msec 14) 6.84 msec 15) 7.32 msec 16) 7.81 msec

Kr pulse duty cycle (t2/t3 in the diagram)

The Kr pulse duty cycle (t2/t3) can be selected from 1/4 (25%) or 1/2 (50%). Table 4.12.4.1 lists the lengths of high and low periods of the Kr pulse at the selected duty cycle.

Table 4.12.4.1 Kr pulse duty cycle

Duty cycle (t2/t3)	t2 (msec)	t3 (msec)
1/2	0.488	0.977
1/4	0.244	0.977

Number of Kr pulses

The number of Kr pulses can be selected from the following four available choices:

1) 4
2) 6
3) 8
4) 10

Since the fixed drive pulse generates a stronger magnetic field, the motor driver outputs a demagnetization pulse (KE pulse) from the other output pin after outputting the fixed drive pulse. Figure 4.12.4.2 shows the timing of demagnetization pulse output.

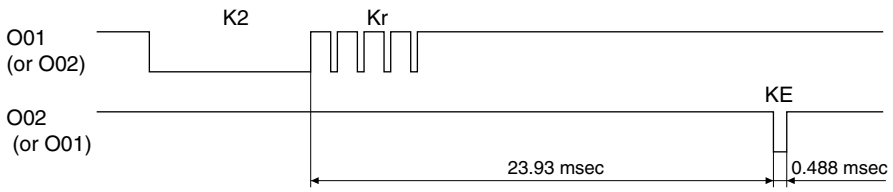


Fig. 4.12.4.2 Timing of demagnetization pulse output

<Mask option: Motor pulse output disabled by K13 input>

By using the mask option, it is possible to disable fixed drive pulse output to motor 0 while K13 input is held high. Setting this mask option inhibits the motor driver from outputting new drive pulses and disables output control by software from the rise to the fall of K13 input. Should a drive pulse be output when K13 input goes high, the entire pulse is output before new drive pulses are disabled.

Fixed drive control

(1) Setting the drive pulses

Before outputting pulses, select specifications of the fixed drive pulse as described in "Fixed drive pulse (K2 and Kr pulses) and demagnetization pulse (KE pulse)" above.

K2 pulse width

Use the motor 0 K2 pulse width select registers M0K2LN3–M0K2LN0 to select the K2 pulse width from the 16 choices listed in Table 4.12.4.2.

Table 4.12.4.2 K2 pulse width

M0K2LN3	M0K2LN2	M0K2LN1	M0K2LN0	K2 pulse width
1	1	1	1	7.81 msec
1	1	1	0	7.32 msec
1	1	0	1	6.84 msec
1	1	0	0	6.35 msec
1	0	1	1	6.10 msec
1	0	1	0	5.86 msec
1	0	0	1	5.62 msec
1	0	0	0	5.37 msec
0	1	1	1	5.13 msec
0	1	1	0	4.88 msec
0	1	0	1	4.64 msec
0	1	0	0	4.39 msec
0	0	1	1	4.15 msec
0	0	1	0	3.91 msec
0	0	0	1	3.66 msec
0	0	0	0	3.42 msec

At initial reset, the K2 pulse width is set to 3.42 msec.

Kr pulse duty cycle

Use the motor 0 Kr pulse duty cycle select register M0KRDY to select the Kr pulse duty cycle.
M0KRDY = "1": 1/2 (high for 0.488 msec, low for 0.488 msec)
M0KRDY = "0": 1/4 (high for 0.732 msec, low for 0.244 msec)

At initial reset, the Kr pulse duty cycle is set to 1/4.

Number of Kr pulses

Use the motor 0 Kr pulses select registers M0KRNM1–M0KRNM0 to select, as shown in Table 4.12.4.3.

Table 4.12.4.3 Selecting the number of Kr pulses

M0KRNM1	M0KRNM0	Number of Kr pulses
1	1	10 pulses
1	0	8 pulses
0	1	6 pulses
0	0	4 pulses

At initial reset, the number of Kr pulses is set to 4.

(2) K2 pulse output control

To start K2 fixed drive, write "1" to the motor 0 fixed drive K2 pulse output register M0K2. After this write operation, K2 fixed drive pulses will be output synchronously with the 256-Hz clock supplied from the divider circuit.

Note that before the motor driver starts outputting drive pulses after a write to the register, there is a finite delay time depending on the K2 pulse width selected, as shown below.

Table 4.12.4.4 K2 pulse output delay time

M0K2LN3–0	K2 pulse width	Maximum delay time
0	3.42 msec	16.11 msec
1	3.66 msec	15.87 msec
2	3.91 msec	15.63 msec
3	4.15 msec	15.38 msec
4	4.39 msec	15.14 msec
5	4.64 msec	14.89 msec
6	4.88 msec	14.65 msec
7	5.13 msec	14.40 msec
8	5.37 msec	14.16 msec
9	5.62 msec	13.92 msec
A	5.86 msec	13.67 msec
B	6.10 msec	13.43 msec
C	6.35 msec	13.18 msec
D	6.84 msec	12.70 msec
E	7.32 msec	12.21 msec
F	7.81 msec	11.72 msec

M0K2 retains value "1" until after all drive pulses for one step of motor rotation are output. Therefore, by reading this register value, it is possible to determine whether motor driver 0 is operating. When the motor driver completes drive pulse output, M0K2 is automatically reset to "0".

Writing "0" to M0K2 has no effect, thus the drive pulse being output cannot be aborted.

Figure 4.12.4.3 shows the timing chart for K2 fixed drive pulse output.

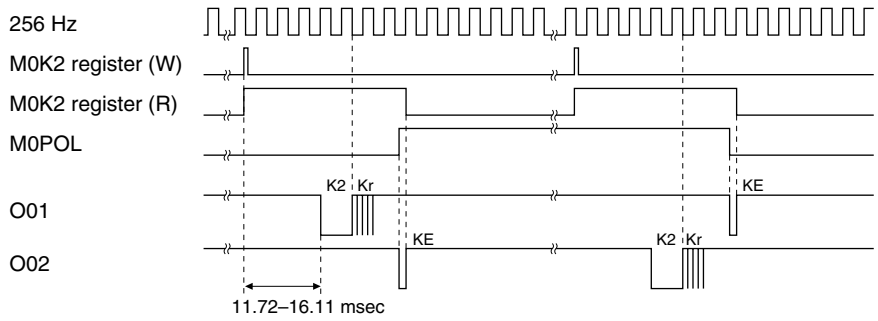


Fig. 4.12.4.3 Timing chart for K2 fixed drive pulse output

(3) Status confirmation during drive

During K2 fixed drive, the motor driver status can be inspected.

Motor RUN/STOP

The motor 0 fixed drive pulse output register M0K2 is readable as well as writable, so that when accessed for read after writing "1", M0K2 reads "1" until all drive pulses for one step of motor rotation are output.

Drive pulse output pins

The drive pulses are output alternately from the O01 and O02 pins for each step. By reading out the M0POL register, it is possible to determine from which pin the next drive pulse will be output. When M0POL = "0", the drive pulse is output from the O01 pin; otherwise, output is from the O02 pin. M0POL changes its state at the time the motor driver starts KE pulse output. (See the timing chart in Figure 4.12.4.3.)

4.12.5 I/O memory of motor control circuit

Table 4.12.5.1 shows the I/O addresses and the control bits for the motor control circuit.

Table 4.12.5.1(a) Control bits of motor control circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF10H	M0KRNM1	M0KRNM0	0	0	M0KRNM1	0			Number of M0 Kr pulses selection [M0KRNM1, 0]: 0 = Count 4; 1 = 6; 2 = 8; 3 = 10
					M0KRNM0	0			
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FF11H	M0K2LN3	M0K2LN2	M0K2LN1	M0K2LN0	M0K2LN3	0			M0 K2 pulse width selection [M0K2LN3–0] 0: Width (msec) 3.42 1: 3.66 2: 3.91 3: 4.15 4: 4.39 5: 4.64 6: 4.88 7: 5.13 [M0K2LN3–0] 8: Width (msec) 5.37 9: 5.62 10: 5.86 11: 6.10 12: 6.35 13: 6.84 14: 7.32 15: 7.81
					M0K2LN2	0			
	R/W				M0K2LN1	0			
					M0K2LN0	0			
FF12H	M0KRDY	0	0	0	M0KRDY	0	1/2	1/4	M0 Kr pulse duty cycle selection
					0 *3	– *2			Unused
	R/W	R			0 *3	– *2			Unused
					0 *3	– *2			Unused
FF14H	0	0	M0K2	0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	R	M0K2	0	Output	Not output	M0 fixed drive (K2) pulse output
					0 *3	– *2			Unused
FF16H	0	0	M1PRDEL	M0PRDEL	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		M1PRDEL	0	Pr = 0	M1PRNM	M1 forced 0 Pr pulse selection
					M0PRDEL	0	Pr = 0	M0PRNM	M0 forced 0 Pr pulse selection
FF17H	0	0	M1CL8HZ	M0CL8HZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		M1CL8HZ	0	8 Hz	M1CLS	M1 8-Hz motor clock selection
					M0CL8HZ	0	8 Hz	M0CLS	M0 8-Hz motor clock selection
FF18H	M0PSEL	M0CLS2	M0CLS1	M0CLS0	M0PSEL	0	Reverse	Normal	M0 motor pulse normal/reverse rotation select
					M0CLS2	1			M0 motor clock selection [M0CLS2–0] 0: Clock (Hz) 16 1: 25.6 2: 32 3: 42.7 4: 51.2 5: 64 6: 85.3 7: 128
	R/W				M0CLS1	1			
					M0CLS0	1			
FF19H	M0P1LN3	M0P1LN2	M0P1LN1	M0P1LN0	M0P1LN3	0			M0 P1 pulse width selection [M0P1LN3–0] 0: Width (msec) 2.93 1: 3.17 2: 3.42 3: 3.66 4: 3.91 5: 4.15 6: 4.39 7: 4.64 [M0P1LN3–0] 8: Width (msec) 4.88 9: 5.13 10: 5.37 11: 5.62 12: 5.86 13: 6.10 14: 6.35 15: 6.59
					M0P1LN2	0			
	R/W				M0P1LN1	0			
					M0P1LN0	0			
FF1AH	M0PRNM1	M0PRNM0	M0PRDY	M0GRDY	M0PRNM1	0			Number of M0 Pr pulses selection [M0PRNM1, 0]: 0 = Count 4; 1 = 6; 2 = 8; 3 = 10
					M0PRNM0	0			
	R/W				M0PRDY	0	1/2	1/4	M0 Pr pulse duty cycle selection
					M0GRDY	0	1/2	1/4	M0 Gr pulse duty cycle selection
FF1BH	M0GRNM	M0G1LN2	M0G1LN1	M0G1LN0	M0GRNM	0	8	4	Number of M0 Gr pulses selection
					M0G1LN2	0			M0 G1 pulse width selection [M0G1LN2–0] 0: Width (msec) 0.73 1: 0.98 2: 1.22 3: 1.46 4: 1.71 5: 1.95 6: 2.20 7: 0.49
	R/W				M0G1LN1	0			
					M0G1LN0	0			
FF1CH	M0G3LN	M0G2LN2	M0G2LN1	M0G2LN0	M0G3LN	0	6.84 msec	4.88 msec	M0 G3 pulses width selection
					M0G2LN2	0			M0 G2 pulse width selection [M0G2LN2–0] 0: Width (msec) 1.71 1: 1.95 2: 2.20 3: 2.44 4: 2.69 5: 2.93 6: 3.17 7: 3.42
	R/W				M0G2LN1	0			
					M0G2LN0	0			
FF1DH	M0PD3	M0PD2	M0PD1	M0PD0	M0PD3	0			M0 motor pulse register
					M0PD2	0			
	R/W				M0PD1	0			
					M0PD0	0			
FF1EH	M0PC3	M0PC2	M0PC1	M0PC0	M0PC3	0			M0 motor pulse counter
					M0PC2	0			
	R				M0PC1	0			
					M0PC0	0			
FF1FH	M0POL	M0PCCL	M0RUNM	M0ENM	M0POL	0	O02	O01	M0 output polarity
					M0PCCL	Clear	Clear	Invalid	M0 motor pulse counter clear
	R	W	R	R/W	M0RUNM	0	Run	Stop	M0 motor drive status
					M0ENM	0	Run	Stop	M0 motor drive Run/Stop control

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.12.5.1(b) Control bits of motor control circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF38H	M1PSEL	M1CLS2	M1CLS1	M1CLS0	M1PSEL	0	Reverse	Normal	M1 motor pulse normal/reverse rotation select
					M1CLS2	1			M1 motor clock selection
	R/W				M1CLS1	1			[M1CLS2–0] 0 1 2 3 4 5 6 7
					M1CLS0	1			Clock (Hz) 16 25.6 32 42.7 51.2 64 85.3 128
FF39H	M1P1LN3	M1P1LN2	M1P1LN1	M1P1LN0	M1P1LN3	0			M1 P1 pulse width selection
					M1P1LN2	0			[M1P1LN3–0] 0 1 2 3 4 5 6 7
	R/W				M1P1LN1	0			Width (msec) 2.93 3.17 3.42 3.66 3.91 4.15 4.39 4.64
					M1P1LN0	0			[M1P1LN3–0] 8 9 10 11 12 13 14 15
									Width (msec) 4.88 5.13 5.37 5.62 5.86 6.10 6.35 6.59
FF3AH	M1PRNM1	M1PRNM0	M1PRDY	M1GRDY	M1PRNM1	0			Number of M1 Pr pulses selection [M1PRNM1, 0] 0 1 2 3 Count 4 6 8 10
					M1PRNM0	0			
	R/W				M1PRDY	0	1/2	1/4	M1 Pr pulse duty cycle selection
					M1GRDY	0	1/2	1/4	M1 Gr pulse duty cycle selection
FF3BH	M1GRNM	M1G1LN2	M1G1LN1	M1G1LN0	M1GRNM	0	8	4	Number of M1 Gr pulses selection
					M1G1LN2	0			M1 G1 pulse width selection
	R/W				M1G1LN1	0			[M1G1LN2–0] 0 1 2 3 4 5 6 7
					M1G1LN0	0			Width (msec) 0.73 0.98 1.22 1.46 1.71 1.95 2.20 0.49
FF3CH	M1G3LN	M1G2LN2	M1G2LN1	M1G2LN0	M1G3LN	0	6.84 msec	4.88 msec	M1 G3 pulses width selection
					M1G2LN2	0			M1 G2 pulse width selection
	R/W				M1G2LN1	0			[M1G2LN2–0] 0 1 2 3 4 5 6 7
					M1G2LN0	0			Width (msec) 1.71 1.95 2.20 2.44 2.69 2.93 3.17 3.42
FF3DH	M1PD3	M1PD2	M1PD1	M1PD0	M1PD3	0			M1 motor pulse register
					M1PD2	0			
	R/W				M1PD1	0			
					M1PD0	0			
FF3EH	M1PC3	M1PC2	M1PC1	M1PC0	M1PC3	0			M1 motor pulse counter
					M1PC2	0			
	R				M1PC1	0			
					M1PC0	0			
FF3FH	M1POL	M1PCCL	M1RUNM	M1ENM	M1POL	0	O12	O11	M1 output polarity
					M1PCCL	Clear	Clear	Invalid	M1 motor pulse counter clear
	R	W	R	R/W	M1RUNM	0	Run	Stop	M1 motor drive status
					M1ENM	0	Run	Stop	M1 motor drive Run/Stop control
FFE8H	0	0	EISMD1	EISMD0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISMD1	0	Enable	Mask	Interrupt mask register (Motor driver 1)
					EISMD0	0	Enable	Mask	Interrupt mask register (Motor driver 0)
FFF8H	0	0	ISMD1	ISMD0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISMD1	0	(W)	(W)	Interrupt factor flag (Motor driver 1)
					ISMD0	0	Reset	Invalid	Interrupt factor flag (Motor driver 0)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Note: The designations "M0" and "M1" prefixed to control bit names denote the corresponding motors (motors 0 and 1).

M0KRNM0, M0KRNM1: Number of M0 Kr pulses select register (FF10H•D2, D3)

This register selects the number of Kr pulses that comprise the fixed drive waveform.

Table 4.12.5.2 Selecting the number of Kr pulses

M0KRNM1	M0KRNM0	Number of Kr pulses
1	1	10 pulses
1	0	8 pulses
0	1	6 pulses
0	0	4 pulses

Make sure the motor is idle when writing to the M0KRNM register to select the number of Kr pulses.
At initial reset, this register is set to "00B".

M0K2LN0–M0K2LN3: M0 K2 pulse width select register (FF11H)

This register selects the K2 pulse width of the fixed drive waveform.

Table 4.12.5.3 Selecting the K2 pulse width

M0K2LN3	M0K2LN2	M0K2LN1	M0K2LN0	K2 pulse width
1	1	1	1	7.81 msec
1	1	1	0	7.32 msec
1	1	0	1	6.84 msec
1	1	0	0	6.35 msec
1	0	1	1	6.10 msec
1	0	1	0	5.86 msec
1	0	0	1	5.62 msec
1	0	0	0	5.37 msec
0	1	1	1	5.13 msec
0	1	1	0	4.88 msec
0	1	0	1	4.64 msec
0	1	0	0	4.39 msec
0	0	1	1	4.15 msec
0	0	1	0	3.91 msec
0	0	0	1	3.66 msec
0	0	0	0	3.42 msec

Make sure the motor is idle when writing to M0K2LN to select the K2 pulse width.
At initial reset, this register is set to "0000B".

M0KRDY: M0 Kr pulse duty cycle select register (FF12H•D3)

This register selects the Kr pulse duty cycle used for fixed drive.

When "1" is written: 1/2 (50%)
When "0" is written: 1/4 (25%)
Reading: Valid

This duty cycle represents the low period per cycle of the Kr pulse.
Writing "1" to the M0KRDY register selects a 1/2 duty cycle; writing "0" selects a 1/4 duty cycle.
Make sure the motor is idle when writing to M0KRDY to select the Kr pulse duty cycle.
At initial reset, this register is set to "0".

M0K2: Motor 0 fixed drive K2 pulse output register (FF14H•D1)

This register is used to output fixed drive K2 pulses to motor 0.

• ***When writing***

When "1" is written: Pulse output
When "0" is written: No operation

Writing "1" to the M0K2 register causes the motor driver to output K2 drive pulses for one step of normal motor rotation. These pulses are output synchronously with the 256-Hz clock supplied from the divider circuit. Writing "0" to the M0K2 register performs no operation.

• ***When reading***

When "1" is read: Pulse output in progress
When "0" is read: No pulse output

The value read from the M0K2 register indicates the output status of K2 drive pulses for normal rotation. When the read value is "1", drive pulses are being output. The M0K2 register is reset to "0" when the motor driver completes all drive pulse output for one step of motor rotation.
At initial reset, this register is set to "0".

M0CLS0–M0CLS2: M0 motor clock select register (FF18H•D0–D2)
M1CLS0–M1CLS2: M1 motor clock select register (FF38H•D0–D2)

These registers select the motor clock that determines the fast-feed rate.

Table 4.12.5.4 Selection of the motor clock

MxCLS2	MxCLS1	MxCLS0	Motor clock frequency
1	1	1	128 Hz
1	1	0	85.3 Hz
1	0	1	64 Hz
1	0	0	51.2 Hz
0	1	1	42.7 Hz
0	1	0	32 Hz
0	0	1	25.6 Hz
0	0	0	16 Hz

However, when MxCL8HZ = "1", an 8-Hz motor clock is used and the MxCLS register setting is ignored. When a MxCLS register is altered, the motor clocks are changed over at the end of the motor clock cycle in which the register was altered. Consequently, before the motor clocks are actually changed over after the register is altered, there is a delay of up to one cycle of the active clock before the changeover.
At initial reset, these registers are set to "111B".

M0CL8HZ: M0 8-Hz motor clock select register (FF17H•D0)
M1CL8HZ: M1 8-Hz motor clock select register (FF17H•D1)

Selects an 8-Hz motor clock.

When "1" is written: 8 Hz clock
When "0" is written: Clock selected by MxCLS2–MxCLS0
Reading: Valid

When "1" is written to MxCL8HZ, an 8-Hz motor clock is selected. In this case, the MxCLS register setting is ignored. The MxCLS register is effective when MxCL8HZ is set to "0".
At initial reset, this register is set to "0".

M0PSEL: M0 motor pulse normal/reverse rotation select register (FF18H•D3)
M1PSEL: M1 motor pulse normal/reverse rotation select register (FF38H•D3)

These registers select the direction of motor rotation in fast-feed drive.

When "1" is written: Reverse rotation
When "0" is written: Normal rotation
Reading: Valid

Writing "1" to a MxPSEL register selects reverse rotation in the fast-feed direction. Writing "0" to a MxPSEL register selects normal rotation in the fast-feed direction.
Make sure the motor is idle when writing to a MxPSEL register to select the direction of rotation.
At initial reset, these registers are set to "0".

M0P1LN0–M0P1LN3: M0 P1 pulse width select registers (FF19H)
M1P1LN0–M1P1LN3: M1 P1 pulse width select registers (FF39H)

These registers select the P1 pulse width of the fast-feed drive waveform for normal rotation.

Table 4.12.5.5 Selection of the P1 pulse width

MxP1LN3	MxP1LN2	MxP1LN1	MxP1LN0	P1 pulse width
1	1	1	1	6.59 msec
1	1	1	0	6.35 msec
1	1	0	1	6.10 msec
1	1	0	0	5.86 msec
1	0	1	1	5.62 msec
1	0	1	0	5.37 msec
1	0	0	1	5.13 msec
1	0	0	0	4.88 msec
0	1	1	1	4.64 msec
0	1	1	0	4.39 msec
0	1	0	1	4.15 msec
0	1	0	0	3.91 msec
0	0	1	1	3.66 msec
0	0	1	0	3.42 msec
0	0	0	1	3.17 msec
0	0	0	0	2.93 msec

Make sure the motor is idle when writing to a MxP1LN register to select the P1 pulse width.
At initial reset, these registers are set to "0000B".

M0GRDY: M0 Gr pulse duty cycle select register (FF1AH•D0)
M1GRDY: M1 Gr pulse duty cycle select register (FF3AH•D0)

These registers select the duty cycle of the Gr pulse used for fast-feed drive at reverse rotation.

When "1" is written: 1/2 (50%)
When "0" is written: 1/4 (25%)
Reading: Valid

This duty cycle represents the low period per cycle of the Gr pulse.
Writing "1" to a MxGRDY register selects a 1/2 duty cycle; writing "0" selects a 1/4 duty cycle.
Make sure the motor is idle when writing to a MxGRDY register to select the Gr pulse duty cycle.
At initial reset, these registers are set to "0".

M0PRDY: M0 Pr pulse duty cycle select register (FF1AH•D1)
M1PRDY: M1 Pr pulse duty cycle select register (FF3AH•D1)
These registers select the duty cycle of the Pr pulse used for fast-feed drive at normal rotation.

When "1" is written: 1/2 (50%)
When "0" is written: 1/4 (25%)
Reading: Valid

This duty cycle represents the low period per cycle of the Pr pulse.
Writing "1" to a MxPRDY register selects a 1/2 duty cycle; writing "0" selects a 1/4 duty cycle.
Make sure the motor is idle when writing to a MxPRDY register to select the Pr pulse duty cycle.
At initial reset, these registers are set to "0".

M0PRNM0, M0PRNM1: Number of M0 Pr pulses select register (FF1AH•D2, D3)
M1PRNM0, M1PRNM1: Number of M1 Pr pulses select register (FF3AH•D2, D3)
These registers select the number of Pr pulses that comprise the fast-feed drive waveform for normal rotation.

Table 4.12.5.6 Selecting the number of Pr pulses

MxPRNM1	MxPRNM0	Number of Pr pulses
1	1	10 pulses (Pr width = 9.77 msec)
1	0	8 pulses (Pr width = 7.81 msec)
0	1	6 pulses (Pr width = 5.86 msec)
0	0	4 pulses (Pr width = 3.91 msec)

However, when MxPRDEL = "1", the number of Pr pulses is forcibly set to 0 and the MxPRNM register setting is ignored.
Make sure the motor is idle when writing to a MxPRNM register to select the number of Pr pulses.
At initial reset, these registers are set to "00B".

M0PRDEL: M0 forced 0 Pr pulse select register (FF16H•D0)
M1PRDEL: M1 forced 0 Pr pulse select register (FF16H•D1)
Sets the number of Pr pulses to 0.

When "1" is written: 0 pulses
When "0" is written: Number of pulses set by MxPRNM1–MxPRNM0
Reading: Valid

When "1" is written to MxPRDEL, the number of Pr pulses is forcibly set to 0. In this case, the MxPRNM register setting is ignored. The MxPRNM register is effective when MxPRDEL is set to "0".
At initial reset, this register is set to "0".

M0G1LN0–M0G1LN2: M0 G1 pulse width select register (FF1BH•D0–D2)
M1G1LN0–M1G1LN2: M1 G1 pulse width select register (FF3BH•D0–D2)
These registers select the G1 pulse width of the fast-feed drive waveform for reverse rotation.

Table 4.12.5.7 Selection of the G1 pulse width

MxG1LN2	MxG1LN1	MxG1LN0	G1 pulse width
1	1	1	0.49 msec
1	1	0	2.20 msec
1	0	1	1.95 msec
1	0	0	1.71 msec
0	1	1	1.46 msec
0	1	0	1.22 msec
0	0	1	0.98 msec
0	0	0	0.73 msec

Make sure the motor is idle when writing to a MxG1LN register to select the G1 pulse width.
At initial reset, these registers are set to "000B".

M0GRNM: Number of M0 Gr pulses select register (FF1BH•D3)
M1GRNM: Number of M1 Gr pulses select register (FF3BH•D3)

These registers select the number of Gr pulses that comprise the fast-feed drive waveform for reverse rotation.

When "1" is written: 8 pulses
When "0" is written: 4 pulses
Reading: Valid

Writing "1" to a MxGRNM register selects 8 Gr pulses; writing "0" selects 4 Gr pulses.
Make sure the motor is idle when writing to a MxGRNM register to select the number of Gr pulses.
At initial reset, these registers are set to "0".

M0G2LN0–M0G2LN2: M0 G2 pulse width select registers (FF1CH•D0–D2)
M1G2LN0–M1G2LN2: M1 G2 pulse width select registers (FF3CH•D0–D2)

These registers select the G2 pulse width of the fast-feed drive waveform for reverse rotation.

Table 4.12.5.8 Selection of the G2 pulse width

MxG2LN2	MxG2LN1	MxG2LN0	G2 pulse width
1	1	1	3.42 msec
1	1	0	3.17 msec
1	0	1	2.93 msec
1	0	0	2.69 msec
0	1	1	2.44 msec
0	1	0	2.20 msec
0	0	1	1.95 msec
0	0	0	1.71 msec

Make sure the motor is idle when writing to a MxG2LN register to select the G2 pulse width.
At initial reset, these registers are set to "000B".

M0G3LN: M0 G3 pulse width select register (FF1CH•D3)
M1G3LN: M1 G3 pulse width select register (FF3CH•D3)

These registers select the G3 pulse width of the fast-feed drive waveform for reverse rotation.

When "1" is written: 6.84 msec
When "0" is written: 4.88 msec
Reading: Valid

Writing "1" to a MxG3LN register sets the G3 pulse width to 6.84 msec; writing "0" sets it to 4.88 msec.
Make sure the motor is idle when writing to a MxG3LN register to select the G3 pulse width.
At initial reset, these registers are set to "0".

M0PD0–M0PD3: M0 motor pulse registers (FF1DH)
M1PD0–M1PD3: M1 motor pulse registers (FF3DH)

These registers set the number of fast-feed steps. The register data can also be read out.
The data set in these registers is loaded into the motor pulse counters to control the number of fast-feed drive pulses. The register data is loaded into a motor pulse counter at the following timing:
1. When data is written to the register while the motor pulse counter is 0
2. When the motor pulse counter reaches terminal count 0 during fast-feed drive

The motor pulse register is cleared to 0 when written data is loaded into the motor pulse counter.
At initial reset, these registers are set to "0000B".

M0PC0–M0PC3: M0 motor pulse counters (FF1EH)
M1PC0–M1PC3: M1 motor pulse counters (FF3EH)

The data written to the motor pulse registers is loaded into these counters to control the number of output pulses for fast-feed drive. The data is loaded from the registers into these counters at the timing described above.
These counters are also readable. Writing data to a counter in software has no effect.
At initial reset, these counters are set to "0000B".

M0ENM: M0 motor drive Run/Stop control register (FF1FH•D0)
M1ENM: M1 motor drive Run/Stop control register (FF3FH•D0)

These registers control Run/Stop of fast-feed drive.

When "1" is written: Run
When "0" is written: Stop
Reading: Valid

Writing "1" to a MxENM register causes the motor driver to start fast-feed drive for the number of steps set on the motor pulse counter. The drive pulses are output synchronously with the motor clock selected. If fast-feed drive is started by writing "1" to a MxENM register while the motor pulse counter = 0, no drive pulses will be output until after data is loaded into said motor pulse counter.
Writing "0" to a MxENM register causes the motor driver to temporarily stop fast-feed drive. When stopping fast-feed drive by writing "0" to the register during drive pulse output by the motor driver, the motor will not stop until the motor driver outputs that pulse. The motor pulse counter retains the value held when stopped, so that when starting fast-feed drive by writing "1" to the MxENM register, counting and drive pulse output resume beginning with that value.
At initial reset, these registers are set to "0".

M0RUNM: M0 motor drive status (FF1FH•D1)
M1RUNM: M1 motor drive status (FF3FH•D1)

These registers indicate whether fast-feed drive pulses are turning the motor, thus moving the needle.

When "1" is read: Run
When "0" is read: Stop
Writing: Invalid

After fast-feed drive is started by writing "1" to a MxENM register, MxRUNM remains set to "1" until fast-feed drive is stopped or the last drive pulse output (to set the motor pulse counter = 0). By reading MxRUNM, it is possible to determine that drive pulses are turning the motor, thus moving the needle.
MxRUNM is reset to "0" when MxENM = "0" or the motor pulse counter = 0 (upon completion of drive pulse output).
MxRUNM is a read-only register, so that writing to it has no effect.
At initial reset, these bits are set to "0".

M0PCCL: M0 motor pulse counter clear (FF1FH•D2)
M1PCCL: M1 motor pulse counter clear (FF3FH•D2)

These registers clear the respective motor pulse counters and motor pulse registers.

When "1" is written: Clear
When "0" is written: No operation
Reading: Always "0"

Writing "1" to MxPCCL clears the motor pulse counter and motor pulse register for motor driver 'x' to 0. Because clearing said counter and register during fast-feed drive causes the motor driver to operate erratically, always be sure to temporarily stop the motor driver (by writing "0" to MxENM) before clearing. Writing "0" to MxPCCL performs no operation.
MxPCCL is a write-only bit, so that when accessed for read, it always reads "0".

M0POL: M0 motor output polarity register (FF1FH•D3)
M1POL: M1 motor output polarity register (FF3FH•D3)
The read values of these registers indicate the pin from which to output the next drive pulse.

When "1" is read: Ox2 pin
When "0" is read: Ox1 pin
Writing: Invalid

Reading a MxPOL register helps to determine the output pin from which to output the next drive pulse. (Drive pulses are alternately output from two output pins.) The MxPOL register is set to "1" when the Ox1 pin is to output the next drive pulse, and to "0" when the Ox2 pin is to output the next drive pulse. The content of MxPOL is effective for any drive method.
These bits are read-only, so that writing to these bits has no effect.
At initial reset, these registers are set to "0".

EISMD0: Motor driver 0 interrupt mask register (FFE8H•D0)
EISMD1: Motor driver 1 interrupt mask register (FFE8H•D1)
These registers are used to select whether to mask the motor driver interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask register EISMDx is used to select whether to mask the motor driver-x interrupt or not.
At initial reset, these registers are set to "0".

ISMD0: Motor driver 0 interrupt factor flag (FFF8H•D0)
ISMD1: Motor driver 1 interrupt factor flag (FFF8H•D1)
These flags indicate the status of the motor driver interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

When the motor pulse counter reaches terminal count 0, the corresponding motor interrupt factor flag ISMDx is set to "1", thereby generating a motor interrupt. Even if the interrupt is masked, the flags are set to "1" when the motor pulse counter reaches terminal count 0.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.12.6 Programming notes

(1) Motor driver 0 supports two drive methods (fast-feed drive for normal/reverse rotation and fixed drive), with different control registers used for the respective drive methods. Please exercise caution regarding control to prevent the output of different drive waveforms at the same time.

(2) To abort fast-feed drive, be sure to temporarily stop it (by setting MxENM = "0") before clearing the motor pulse counter. Clearing this counter during drive may cause the motor driver to operate erratically.

(3) If the sum total of fast-feed drive pulses (P1 + Pr, G1 + G2 + G3 + Gr) exceeds the motor clock period, the motor driver will not operate normally. Always make sure the said sum total is less than the motor clock period.

(4) If the sum total of the P1 and Pr pulses exceeds the motor clock cycle, the Pr pulse output is forcibly terminated before the next motor clock output is started. In this case, a hazard may occur on the waveform at forced termination of the Pr pulse output. Therefore, always be sure that said sum total is less than the motor clock cycle.
The table below shows the actual P1 and Pr output period (or the time from start of the pulse output until the Pr pulse output is terminated) when the setting of the P1 and Pr pulses exceeds the motor clock cycle.

Table 4.12.6.1 Drive pulse output period when Pr pulse is forcibly terminated

Motor clock	Forced terminating conditions	Drive pulse output period
128 Hz	[P1+Pr] > 7.324 msec	7.568 msec
85.3 Hz	[P1+Pr] > 11.230 msec	11.475 msec
64 Hz	[P1+Pr] > 15.137 msec	15.381 msec

(5) It is prohibited to use the 128-Hz motor clock for fast-feed drive at reverse rotation. Even if fast-feed drive at reverse rotation is attempted with the 128-Hz motor clock selected, the motor driver will be unable to perform fast-feed drive normally.

(6) Do not change the pulse width, number of pulses, or duty cycle when the motor driver is outputting drive pulses. Changing these parameters during pulse output may cause the motor driver to operate erratically.

(7) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.13 Theoretical Regulation

4.13.1 Theoretical regulation function

The S1C63709 has a function known as "theoretical regulation" that theoretically corrects time clock errors due to deviation in oscillation frequencies. Software can execute theoretical regulation at any time, thus allowing time clock errors to be adjusted within -15/32768 to +16/32768 seconds at a time.

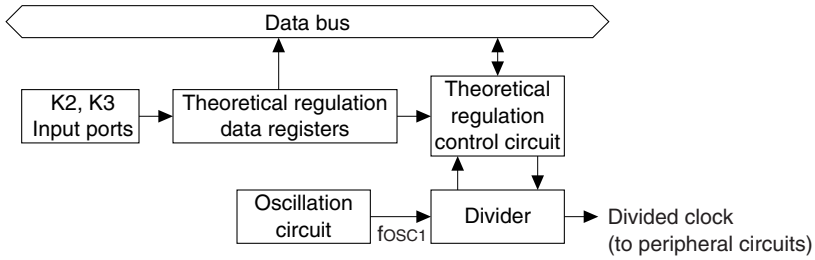


Fig. 4.13.1.1 Configuration of theoretical regulation circuit

Writing "1" to VCWON starts theoretical regulation. The clock adjustment is performed in the system clock (32.768 kHz) divider circuit. VCWON is the theoretical regulation execution register and theoretical regulation is performed only once by writing "1" to the register. Writing "0" is ineffective.

When "1" is written to VCWON, the divider circuit extends or reduces its output signal as below according to the read results from the K30 and K20–K23 ports.
When K30 = "1", the output clock signal is reduced for the number of system clock cycles (-15 to 0 cycles) specified with the K2 port inputs.
When K30 = "0", the output clock signal is extended for the number of system clock cycles (+1 to +16 cycles) specified with the K2 port inputs.

This operation is performed synchronously with the first falling edge of the 512XM (512 Hz) signal after the 64-Hz signal goes low. Therefore, there is a delay of up to 16.6 msec before theoretical regulation actually starts after writing to VCWON. Writing "1" to VCWON in this period is ineffective, so to write "1" to VCWON successively, an interval at least 16.6 msec is necessary between writings.
The timer and other peripheral circuits are supplied with clocks that have been corrected for lead or lag by theoretical regulation.

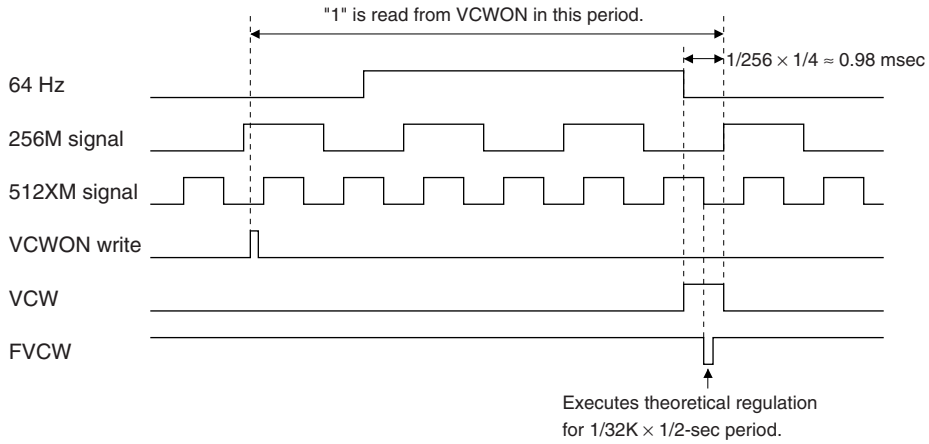


Fig. 4.13.1.2 Timing of theoretical regulation

4.13.2 K2 and K3 inputs for specifying the amount of correction

It is necessary to set an amount of correction for theoretical regulation according to the deviation in oscillation frequencies. The K20–K23 and K30 input ports can be used for setting the amount of correction. (Refer to Section 4.4, "Input Ports", for the input port functions".)
These 5 bits in which the K30 port input used as the sign bit allows specification of a correction value from -15 to +16 steps. To set the amount of correction for theoretical regulation, read the K20–K23 and K30 input status that specifies the correction value from the K20–K23 and K30 theoretical regulation input data registers (TRIM20–TRIM23, TRIM30). Use the timer or other interrupt handler routine for writing to VCWON.
The table below shows theoretical regulation execution examples. The values in the table are the correction results when theoretical regulation is executed in 10-second cycles using the read data from the input ports above as the amount of correction.

Table 4.13.2.1 <Execution example> Rates when theoretical regulation is executed in 10-second cycles

TRIM registers					Amount of correction/	Rate	TRIM registers					Amount of correction/	Rate
30	23	22	21	20	one adjustment (n/32K)	(Sec/Day)	30	23	22	21	20	one adjustment (n/32K)	(Sec/Day)
0	0	0	0	0	+1	-0.264	1	0	0	0	0	-15	+3.955
0	0	0	0	1	+2	-0.527	1	0	0	0	1	-14	+3.691
0	0	0	1	0	+3	-0.791	1	0	0	1	0	-13	+3.428
0	0	0	1	1	+4	-1.055	1	0	0	1	1	-12	+3.164
0	0	1	0	0	+5	-1.318	1	0	1	0	0	-11	+2.900
0	0	1	0	1	+6	-1.582	1	0	1	0	1	-10	+2.637
0	0	1	1	0	+7	-1.846	1	0	1	1	0	-9	+2.373
0	0	1	1	1	+8	-2.109	1	0	1	1	1	-8	+2.109
0	1	0	0	0	+9	-2.373	1	1	0	0	0	-7	+1.846
0	1	0	0	1	+10	-2.637	1	1	0	0	1	-6	+1.582
0	1	0	1	0	+11	-2.900	1	1	0	1	0	-5	+1.318
0	1	0	1	1	+12	-3.164	1	1	0	1	1	-4	+1.055
0	1	1	0	0	+13	-3.428	1	1	1	0	0	-3	+0.791
0	1	1	0	1	+14	-3.691	1	1	1	0	1	-2	+0.527
0	1	1	1	0	+15	-3.955	1	1	1	1	0	-1	+0.264
0	1	1	1	1	+16	-4.219	1	1	1	1	1	0	0

Lag ↓ ↑ Lead

Notes:
- *Make sure that the CPU is operating with the OSC1 clock before reading the amount of correction from the K20–K23 and K30 ports.*
- *The F16HZ (P33) special output signal can be used to verify the amount of correction by executing theoretical regulations.*

4.13.3 VCWON monitor output

The VCWON write signal can be output to outside the IC from the P22 terminal.
Before the VCWON write signal can be output, fix the I/O control register (IOC22) at "1" (output), the data register (P22) at "0" and the pull-down control register (PUL22) at "0" (pull-down disabled). Use the EVCWON register to enable/disable signal output. When EVCWON is set to "1", the VCWON write signal is output from the P22 terminal and when it is set to "0", the P22 terminal goes low (VSS) level.

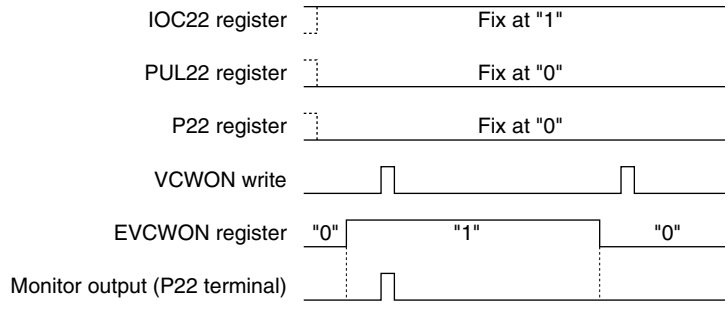


Fig. 4.13.3.1 VCWON write signal output

4.13.4 I/O memory of theoretical regulation

Table 4.13.4.1 shows the I/O addresses and the control bits of theoretical regulation.

Table 4.13.4.1 Control bits of theoretical regulation

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF29H	K23	K22	K21	K20	K23	– *2	High	Low	K20–K23 input port data
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
FF2AH	TRIM23	TRIM22	TRIM21	TRIM20	TRIM23	0	1	0	K20–K23 theoretical regulation input data register
					TRIM22	0	1	0	
	R				TRIM21	0	1	0	
					TRIM20	0	1	0	
FF2DH	ENISOR1	ECLIM	CLIM	K30	ENISOR1	0	Enable	Disable	ISOR1 monitor output enable (P23)
					ECLIM	0	Enable	Disable	CLIM monitor output enable (P32)
	R/W		R		CLIM	0	On	Off	Limit level monitor
					K30	– *2	High	Low	K30 input port data
FF2EH	0	0	0	TRIM30	0 *3	0			Unused
					0 *3	0			Unused
	R				0 *3	0			Unused
					TRIM30	0	1	0	K30 theoretical regulation input data register
FF88H	0	0	EVCWON	VCWON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EVCWON	0	Enable	Disable	VCWON monitor output enable (P22)
					VCWON	0	On	Off	Theoretical regulation status/trigger (Writing "0" is ineffective.)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

VCWON: Theoretical regulation execution register (FF88H•D0)

Executes theoretical regulation.

When "1" is written: Execute theoretical regulation
When "0" is written: No operation

When "1" is read: Theoretical regulation in progress
When "0" is read: Theoretical regulation stopped

Writing "1" to VCWON executes one session of theoretical regulation.
When "1" is written to VCWON, the theoretical regulation starts synchronously with the first falling edge of the 512XM signal after the 64-Hz signal goes low. Therefore, there is a delay of up to 16.6 msec before theoretical regulation actually starts. Writing "1" to VCWON in this period is ineffective, so to write "1" to VCWON successively, an interval at least 16.6 msec is necessary between writings.
No operation results when "0" is written to VCWON.
At initial reset, this register is set to "0".

K20–K23: K2 port input port data (FF29H)
K30: K3 port input port data (FF2DH•D0)

Input data of the K20–K23 and K30 input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of each input port goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These registers are read only, so a writing operation is ineffective.

TRIM20–TRIM23: K2 theoretical regulation input data register (FF2AH)
TRIM30: K3 theoretical regulation input data register (FF2EH•D0)

The correction value that has been specified with the K2 and K3 inputs can be read through these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

By reading the K20–K23 and K30 input port data registers (FF29H, FF2DH•D0), the amount of correction for theoretical regulation is set to the TRIM20–TRIM23 and TRIM30 registers (FF2AH, FF2EH•D0). After the correction value has been set to the TRIM20–TRIM23 and TRIM30 registers, the set value can be read from these registers. See Table 4.13.2.1 for the relationship between port input values and amounts of correction.
These registers are read only, so a writing operation is ineffective.

EVCWON: VCWON monitor output enable register (FF88H•D1)

Controls the VCWON write signal output.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Before the VCWON write signal can be output, fix the I/O control register (IOC22) at "1" (output), the data register (P22) at "0" and the pull-down control register (PUL22) at "0" (pull-down disabled). When EVCWON is set to "1" under the conditions above, the VCWON write signal is output from the P22 terminal and when it is set to "0", the P22 terminal goes low (V_{SS}) level.
At initial reset, this register is set to "0".

4.13.5 Programming notes

(1) Caution is required since executing theoretical regulation during drive pulse output by the motor driver may change the pulse width.

(2) When "1" is written to VCWON, the theoretical regulation starts synchronously with the first falling edge of the 512XM signal after the 64-Hz signal goes low. Therefore, there is a delay of up to 16.6 msec before theoretical regulation actually starts. Writing "1" to VCWON in this period is ineffective, so to write "1" to VCWON successively, an interval at least 16.6 msec is necessary between writings.

(3) Make sure that the CPU is operating with the OSC1 clock before reading an amount of correction from the K20–K23 and K30 ports.

4.14 SVD (Supply Voltage Detection) Circuit

4.14.1 Configuration of SVD circuit

The S1C63709 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers.
Turning the SVD circuit on/off and the SVD criteria voltage setting can be done with software.
Figure 4.14.1.1 shows the configuration of the SVD circuit.

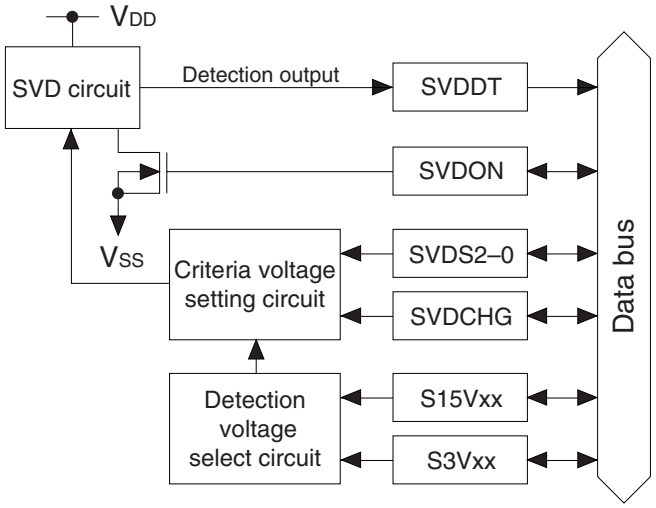


Fig. 4.14.1.1 Configuration of SVD circuit

4.14.2 Setting a criteria voltage

Eight voltage values for comparing with supply voltage can be configured for each of the 3.0 V and 1.5 V power supply voltage systems and one of the voltage values can be selected using the SVDCHG and SVDS2–SVDS0 registers as a criteria voltage for supply voltage detection.

Table 4.14.2.1 Selecting a criteria voltage

for 1.5 V supply voltage (SVDCHG = "0")

SVDS2	SVDS1	SVDS0	Criteria voltage
1	1	1	1.5 V system level 7 (1.5 V)
1	1	0	1.5 V system level 6 (1.4 V)
1	0	1	1.5 V system level 5 (1.3 V)
1	0	0	1.5 V system level 4 (1.25 V)
0	1	1	1.5 V system level 3 (1.2 V)
0	1	0	1.5 V system level 2 (1.15 V)
0	0	1	1.5 V system level 1 (1.1 V)
0	0	0	1.5 V system level 0 (1.05 V)

for 3.0 V supply voltage (SVDCHG = "1")

SVDS2	SVDS1	SVDS0	Criteria voltage
1	1	1	3.0 V system level 7 (2.7 V)
1	1	0	3.0 V system level 6 (2.6 V)
1	0	1	3.0 V system level 5 (2.3 V)
1	0	0	3.0 V system level 4 (2.1 V)
0	1	1	3.0 V system level 3 (2.0 V)
0	1	0	3.0 V system level 2 (1.9 V)
0	0	1	3.0 V system level 1 (1.8 V)
0	0	0	3.0 V system level 0 (1.7 V)

( ) indicates the initially set criteria voltages.

The eight voltage values for level 0 (lowest) to level 7 (highest) can also be selected from 10 values for 1.5 V system and 14 values for 3.0 V system.

Table 4.14.2.2 List of detection voltages for 1.5 V system

Address	Register	Register initial value	Detection voltage	Initial criteria voltage level
FF52H•D1	S15V16	0	1.6 V	–
FF52H•D0	S15V15	1	1.5 V	Level 7 (SVDS = 7)
FF51H•D3	S15V14	1	1.4 V	Level 6 (SVDS = 6)
FF51H•D2	S15V135	0	1.35 V	–
FF51H•D1	S15V13	1	1.3 V	Level 5 (SVDS = 5)
FF51H•D0	S15V125	1	1.25 V	Level 4 (SVDS = 4)
FF50H•D3	S15V12	1	1.2 V	Level 3 (SVDS = 3)
FF50H•D2	S15V115	1	1.15 V	Level 2 (SVDS = 2)
FF50H•D1	S15V11	1	1.1 V	Level 1 (SVDS = 1)
FF50H•D0	S15V105	1	1.05 V	Level 0 (SVDS = 0)

Table 4.14.2.3 List of detection voltages for 3.0 V system

Address	Register	Register initial value	Detection voltage	Initial criteria voltage level
FF55H•D3	S3V27	1	2.7 V	Level 7 (SVDS = 7)
FF55H•D2	S3V265	0	2.65 V	–
FF55H•D1	S3V26	1	2.6 V	Level 6 (SVDS = 6)
FF55H•D0	S3V25	0	2.5 V	–
FF54H•D3	S3V24	0	2.4 V	–
FF54H•D2	S3V235	0	2.35 V	–
FF54H•D1	S3V23	1	2.3 V	Level 5 (SVDS = 5)
FF54H•D0	S3V225	0	2.25 V	–
FF53H•D3	S3V22	0	2.2 V	–
FF53H•D2	S3V21	1	2.1 V	Level 4 (SVDS = 4)
FF53H•D1	S3V20	1	2.0 V	Level 3 (SVDS = 3)
FF53H•D0	S3V19	1	1.9 V	Level 2 (SVDS = 2)
FF52H•D3	S3V18	1	1.8 V	Level 1 (SVDS = 1)
FF52H•D2	S3V17	1	1.7 V	Level 0 (SVDS = 0)

Set the registers for the detection voltages to be used to "1" and set the registers for unused voltages to "0". The voltages selected by writing "1" to the registers are assigned to the criteria voltage levels 7 to 0 in order from highest value to lowest value.

Note: Eight detection voltages must be selected from addresses FF50H–FF55H for each of the 1.5 V and 3.0 V systems. The SVD circuit may not work normally if eight voltages are not selected (e.g., seven or ten voltages are selected).

4.14.3 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD} terminal–V_{SS} terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
When the SVDON register is set to "1", source voltage or external voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes off.
To obtain a stable detection result, the SVD circuit must be on for at least 1 msec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 1 msec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is on, the IC draws a large current, so keep the SVD circuit off unless it is.

4.14.4 SVDDT monitor output

The SVDDT signal (SVDDT register value) can be output to outside the IC from the P21 terminal. This allows external hardware to monitor the supply voltage detection results.
Before the SVDDT signal can be output, fix the I/O control register (IOC21) at "1" (output), the data register (P21) at "0" and the pull-down control register (PUL21) at "0" (pull-down disabled). Use the ESVDDT register to enable/disable signal output. When ESVDDT is set to "1", the SVDDT signal is output from the P21 terminal and when it is set to "0", the P21 terminal goes low (V_{SS}) level.

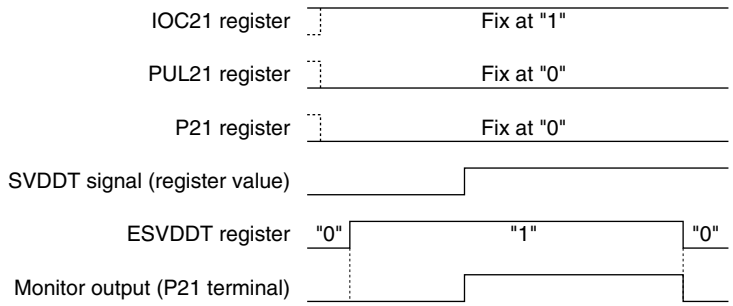


Fig. 4.14.4.1 SVDDT signal output

4.14.5 I/O memory of SVD circuit

Table 4.14.5.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.14.5.1 Control bits of SVD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF04H	SVDCHG	SVDS2	SVDS1	SVDS0	SVDCHG	0	3.0 V	1.5 V	SVD voltage system selection
					SVDS2	0			SVD criteria voltage setting
					SVDS1	0			[SVDS2–0] 0 1 2 3 4 5 6 7
	R/W				SVDS0	0			Level 0 1 2 3 4 5 6 7 (Use FF50H–FF55H to select voltage values) (highest)
FF05H	SVDS3	ESVDDT	SVDDT	SVDON	SVDS3	0	1	0	General-purpose register
					ESVDDT	0	Enable	Disable	SVDDT monitor output enable (P21)
	R/W		R	R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF50H	S15V12	S15V115	S15V11	S15V105	S15V12	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.2 V)
					S15V115	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.15 V)
	R/W				S15V11	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.1 V)
					S15V105	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.05 V)
FF51H	S15V14	S15V135	S15V13	S15V125	S15V14	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.4 V)
					S15V135	0	Enable	Disable	SVD 1.5-V system detection voltage selection (1.35 V)
	R/W				S15V13	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.3 V)
					S15V125	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.25 V)
FF52H	S3V18	S3V17	S15V16	S15V15	S3V18	1	Enable	Disable	SVD 3.0-V system detection voltage selection (1.8 V)
					S3V17	1	Enable	Disable	SVD 3.0-V system detection voltage selection (1.7 V)
	R/W				S15V16	0	Enable	Disable	SVD 1.5-V system detection voltage selection (1.6 V)
					S15V15	1	Enable	Disable	SVD 1.5-V system detection voltage selection (1.5 V)
FF53H	S3V22	S3V21	S3V20	S3V19	S3V22	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.2 V)
					S3V21	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.1 V)
	R/W				S3V20	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.0 V)
					S3V19	1	Enable	Disable	SVD 3.0-V system detection voltage selection (1.9 V)
FF54H	S3V24	S3V235	S3V23	S3V225	S3V24	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.4 V)
					S3V235	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.35 V)
	R/W				S3V23	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.3 V)
					S3V225	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.25 V)
FF55H	S3V27	S3V265	S3V26	S3V25	S3V27	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.7 V)
					S3V265	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.65 V)
	R/W				S3V26	1	Enable	Disable	SVD 3.0-V system detection voltage selection (2.6 V)
					S3V25	0	Enable	Disable	SVD 3.0-V system detection voltage selection (2.5 V)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDCHG: SVD voltage system select register (FF04H•D3)

Selects a power supply voltage system.

When "1" is written: 3.0 V system
When "0" is written: 1.5 V system
Reading: Valid

When SVDCHG is set to "1", the 8-level criteria voltage set is configured for a 3.0 V supply voltage and when it is set to "0", voltages are configured for a 1.5 V supply voltage.
At initial reset, this register is set to "0".

SVDS2–SVDS0: SVD criteria voltage setting register (FF04H•D2–D0)

Selects an SVD criteria voltage from 8 levels (level 7 to level 0) as shown in Table 4.14.2.1.
At initial reset, this register is set to "0".

SVDON: SVD control (on/off) register (FF05H•D0)

Turns the SVD circuit on and off.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be on for at least 1 msec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

ESVDDT: SVDDT monitor output enable register (FF05H•D2)

Controls the SVDDT signal output.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Before the SVDDT signal can be output, fix the I/O control register (IOC21) at "1" (output), the data register (P21) at "0" and the pull-down control register (PUL21) at "0" (pull-down disabled). When ESVDDT is set to "1" under the conditions above, the SVDDT signal is output from the P21 terminal and when it is set to "0", the P21 terminal goes low (V_{SS}) level.
At initial reset, this register is set to "0".

S15Vxx: 1.5 V system detection voltage select registers (FF50H, FF51H, FF52H•D0, D1)
S3Vxx: 3.0 V system detection voltage select registers (FF52H•D2, D3, FF53H, FF54H, FF55H)

These registers are used to configure the 1.5-V and 3.0-V system criteria voltage levels 7 to 0 that can be selected using SVDS2–SVDS0.
Set the registers for the detection voltages to be used to "1" and set the registers for unused voltages to "0". The voltages selected by writing "1" to the registers are assigned to the criteria voltage levels 7 to 0 in order from highest value to lowest value.
Eight detection voltages must be selected from addresses FF50H–FF55H for each of 1.5 V and 3.0 V systems.
At initial reset, the voltage values listed in Table 4.14.2.1 are selected.

4.14.6 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be on for at least 1 msec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 1 msec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

(3) Eight detection voltages must be selected from addresses FF50H–FF55H for each of the 1.5 V and 3.0 V systems. The SVD circuit may not work normally if eight voltages are not selected (e.g., seven or ten voltages are selected).

4.15 Heavy Load Protection Function

4.15.1 Outline of heavy load protection function

The S1C63709 has a heavy load protection function for when the battery load becomes heavy, such as when an external lamp is lit or the buzzer is on (piezoelectric buzzer is driven). In such case, the heavy load protection function is suitable.
The normal mode (heavy load protection function is off) changes to the heavy load protection mode (heavy load protection function is on) when the software sets HVLDON to "1".

Note: In the heavy load protection mode, more current is consumed than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

4.15.2 I/O memory of heavy load protection function

Table 4.15.2.1 shows the I/O address and the control bit for the heavy load protection function.

Table 4.15.2.1 Control bit of heavy load protection function

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	HVLDON	0	0	SRPER	HVLDON	0	Enable	Disable	Heavy load protection mode enable
					0 *3	– *2			Unused
	R/W	R		R/W	0 *3	– *2			Unused
					SRPER	0	Reset	Invalid	Software reset for peripheral circuits

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

HVLDON: Heavy load protection mode enable (FF00H•D3)

Enables/disables heavy load protection mode.

When "1" is written: Heavy load protection enabled
When "0" is written: Heavy load protection disabled
Reading: Valid

The device enters the heavy load protection mode by writing "1" to HVLDON, and returns to the normal mode by writing "0".
At initial reset, this register is set to "0".

4.15.3 Programming note

In the heavy load protection mode, more current is consumed than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

4.16 Solar Function

4.16.1 Configuration of solar control circuit

The S1C63709 contains a solar control circuit to support the solar watch. The solar control circuit detects whether the secondary battery is being recharged or not using the recharging detection circuit, and it controls the recharging path from the solar cell to the secondary battery according to the detection results. This circuit also detects the secondary battery voltage (VTKP), based on which controls the quick start function and overcharge prevention.

The solar control circuit consists of the following circuits built around the recharging control circuit:

- Recharging detection circuit
- Recharging voltage (VTKP) detection circuit
- Limiter circuit
- Quick start circuit

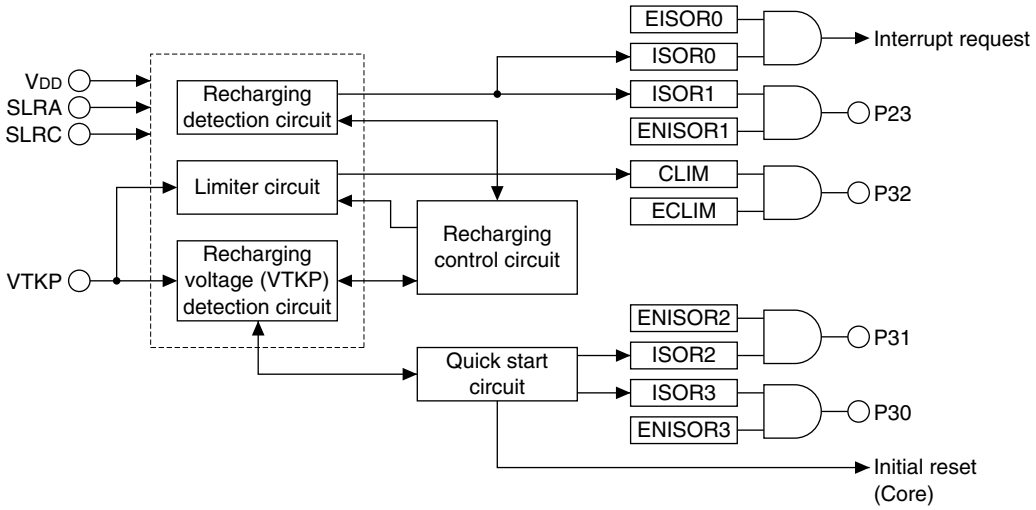


Fig. 4.16.1.1 Configuration of solar control circuit

4.16.2 Mask option

Use or no use of the solar control circuit

The mask option enables the selection of solar function use or nonuse.

Limiter detection voltage

This mask option is used to select a VTKP voltage value to activate the limiter for preventing overcharging of the secondary battery. Table 4.16.2.1 lists the voltage values that can be selected.

Table 4.16.2.1 Limiter on voltage

No.	Limiter ON voltage
1	2.1 V
2	2.5 V
3	2.6 V
4	2.7 V
5	2.8 V
6	2.9 V
7	3.0 V
8	3.1 V
9	3.2 V

4.16.3 Circuit description

Recharging detection circuit

The recharging detection circuit compares the SLRA pin voltage with the VDD voltage to detect whether the secondary battery is being recharged.

- SLRA pin voltage > VDD: Recharging status
- SLRA pin voltage ≤ VDD: Discharging status

The detection results can be checked by reading the recharging flag ISOR1.

Recharging voltage (VTKP) detection circuit

The recharging voltage (VTKP) detection circuit detects the quick start negation voltage and limiter ON voltage synchronously with the two sampling signals sent from the recharging control circuit every two seconds. The respective voltage values are given below.

Quick start negation voltage: 1.0 ± 0.08 V

Limiter ON voltage: See Table 4.16.2.1.

When the quick start negation voltage is detected twice in succession, the solar function exits quick start mode and enters normal operation mode. If the VTKP voltage drops below the quick start negation voltage after the solar function enters normal operation mode, the quick start negation voltage is not sampled until the oscillation detect circuit detects oscillation stoppage. The quick start flags ISOR2 and ISOR3 remain set to "1" in quick start mode, and are reset to "0" upon entry into normal operation mode.

Quick start circuit

The quick start function allows the IC start to operating before the secondary battery is sufficiently recharged during recharging. When powered on, the IC starts operating in quick start mode and continues in this mode until the power supply voltage (VTKP) being recharged reaches 1.0 ± 0.08 V or more. During this period, device operation is unstable due to low-voltage drive, so that the IC is periodically reset internally to prevent erratic operation.

Once the power supply voltage (VTKP) reaches 1.0 ± 0.08 V or more, normal operation is possible with quick start mode consequently deactivated. The quick start circuit is provided for this internal reset processing in quick start mode, and for deactivating quick start mode.

Activating quick start mode

When the OSC1 oscillation circuit starts oscillating after power-on, the IC starts operating in quick start mode. The quick start mode flags ISOR2 and ISOR3 remain set in quick start mode, so that it is possible to determine whether the IC is operating in quick start mode by reading the flag in software.

Resetting during quick start mode

Because VTKP is at a low voltage in quick start mode, the CPU is likely to operate erratically. Therefore, the quick start circuit asserts an internal reset signal every 16 seconds to reset the IC. However, when the oscillation detection circuit detects oscillation, the IC is reset one second after that point.

Note: The contents of timer processing and other control by software in quick start mode are forcibly initialized in hardware every 16 seconds. Therefore, precise time management cannot be sustained in quick start mode.

Deactivating quick start mode

If the recharging voltage (VTKP) detection circuit detects a VTKP value equal to or greater than the quick start negation voltage (1.0 ± 0.08 V) once, ISOR3 (quick start mode flag 1) is reset to "0". When this condition is detected once again (twice in succession), quick start mode is deactivated with ISOR2 (quick start mode flag 2) reset to "0".

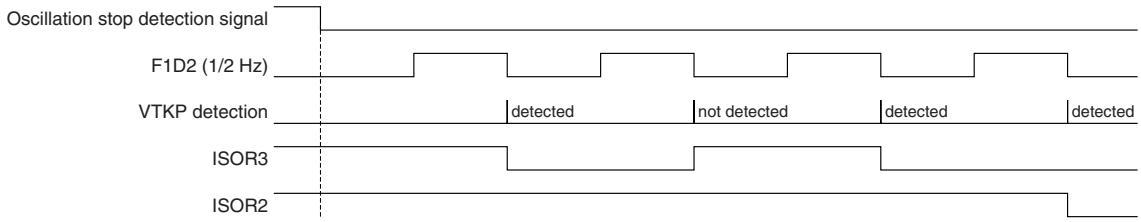


Fig. 4.16.3.1 Quick start mode flag reset condition

Notes: • *A status in which ISOR3 (quick start flag1) = "0" and ISOR2 (quick start flag 2) = "1" does not indicate that quick start mode is deactivated.*

• *Do not perform the software reset for peripheral circuits (FF00H•D0) during quick start mode (when either ISOR2 or ISOR3 is set to "1").*

If the recharging voltage (VTKP) detection circuit detects a VTKP value equal to or greater than the quick start negation voltage (1.0 ± 0.08 V) twice in succession, quick start mode is deactivated (and normal operation mode entered).
When quick start mode is deactivated, the quick start circuit stops generating a periodic reset signal. Once quick start mode is deactivated (even if the power supply voltage drops below 1.0 ± 0.08 V), quick start mode is not entered again unless the IC is reset due to stopped oscillation or multiple-key entry or an NMI occurs. The recharging voltage (VTKP) detection circuit also has a function to simultaneously detect the quick start negation voltage disabled when quick start mode is deactivated. This function is not reenabled until quick start mode is entered after the IC is reset due to stopped oscillation or multiple-key entry or an NMI occurs.

Note: The IC does not enter quick start mode by initial reset using the RESET pin.

Limiter circuit

The limiter circuit prevents overcharging of the secondary battery. If the recharging voltage (VTKP) detection circuit detects a VTKP value equal to or greater than the limiter ON voltage (see Table 4.16.2.1), the limiter circuit is turned on, thus preventing recharging current from flowing into the secondary battery. Thereafter, when the recharging voltage (VTKP) detection circuit detects a drop in VTKP below the limiter ON voltage, the limiter circuit is turned off, allowing recharging to restart.
The CLIM flag (FF2DH•D1) is provided to indicates the limiter circuit operating status.
- CLIM flag = "1" when the recharging voltage (VTKP) ≥ limiter ON voltage
- CLIM flag = "0" when the recharging voltage (VTKP) < limiter ON voltage

4.16.4 Recharging flag and wakeup interrupt function

The solar control circuit has a recharging flag (to indicate secondary battery recharging) and a wakeup interrupt function. When the recharging detection circuit detects a recharging state, the recharging flag ISOR1 is set to "1", with the wakeup interrupt flag ISOR0 set to "1" 0.75 to 1 second later. The interrupt mask register EISOR0 can mask the interrupt factor. Setting the mask bit for this interrupt to "1" generates a wakeup interrupt to the CPU; setting the mask bit to "0" generates no interrupts to the CPU (although the interrupt factor flag is set to "1"). The wakeup interrupt factor flag ISOR0 is reset to "0" by writing "1". Figure 4.16.4.1 shows the timing of a wakeup interrupt.

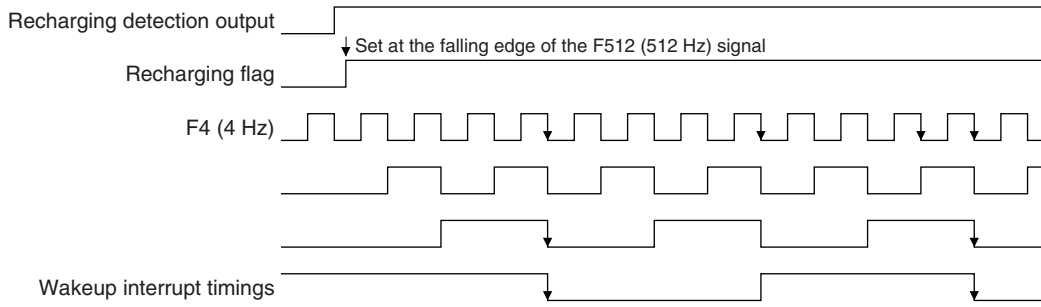


Fig. 4.16.4.1 Timing of wakeup interrupt

Once initially generated, a wakeup interrupt is generated again at 2-second intervals as long as the recharging flag remains set.

4.16.5 ISOR flag monitor outputs

The ISOR1 to ISOR3 flag values (signals) can be output to outside the IC from the I/O port terminals shown in Table 4.16.5.1. This allows external hardware to monitor the quick start mode and recharging statuses.

Table 4.16.5.1 ISOR signal output ports and monitor output enable registers

Terminal	Flag signal	Description	Monitor output enable register
P23	ISOR1	Recharging flag status	ENISOR1
P31	ISOR2	Quick start mode flag 2 status	ENISOR2
P30	ISOR3	Quick start mode flag 1 status	ENISOR3

Before the signal can be output, fix the I/O control register (IOCxx) at "1" (output), the data register (Pxx) at "0" and the pull-down control register (PULxx) at "0" (pull-down disabled). Use the monitor output enable register to enable/disable signal output. When the monitor output enable register is set to "1", the flag signal is output from the Pxx terminal and when it is set to "0", the Pxx terminal goes low (VSS) level.

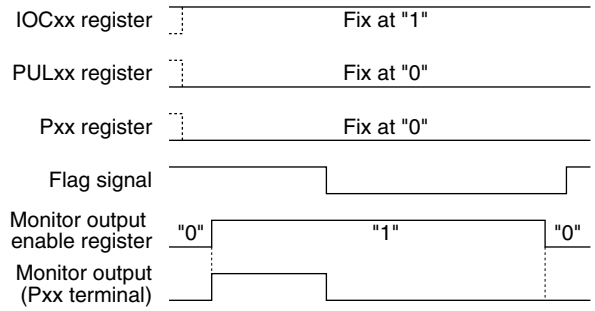


Fig. 4.16.5.1 ISOR signal output

4.16.6 I/O memory of solar function

Table 4.16.6.1 shows the I/O addresses and the control bits of solar function.

Table 4.16.6.1 Control bits of solar function

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF09H	ENISOR3	ENISOR2	E16HZ	0	ENISOR3	0	Enable	Disable	ISOR3 monitor output enable (P30)
					ENISOR2	0	Enable	Disable	ISOR2 monitor output enable (P31)
	R/W			R	E16HZ	0	Enable	Disable	F16HZ clock output enable (P33)
					0 *3	– *2			Unused
FF2DH	ENISOR1	ECLIM	CLIM	K30	ENISOR1	0	Enable	Disable	ISOR1 monitor output enable (P23)
					ECLIM	0	Enable	Disable	CLIM monitor output enable (P32)
	R/W		R		CLIM	0	On	Off	Limit level monitor
					K30	– *2	High	Low	K30 input port data
FFECH	EISOR3	EISOR2	EISOR1	EISOR0	EISOR3	0	1	0	General-purpose register
					EISOR2	0	1	0	General-purpose register
	R/W				EISOR1	0	1	0	General-purpose register
					EISOR0	0	Enable	Mask	Interrupt mask register (Solar wakeup)
FFFCH	ISOR3	ISOR2	ISOR1	ISOR0	ISOR3	– *2	Pre Q start	Normal	Quick start mode flag 1
					ISOR2	– *2	Quick start	Normal	Quick start mode flag 2
					ISOR1	– *2	Charge	Not charged	Recharging flag
	R			R/W	ISOR0	0	(R)Yes (W)Reset	(R)No (W)Invalid	Interrupt factor flag (Solar wakeup)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

EISOR0: Interrupt mask register (FFECH•D0)

This register selects whether to mask the solar interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

EISOR0 is the mask register for wakeup interrupts of the solar function. Writing "1" to this register enables an interrupt; writing "0" masks the interrupt.
At initial reset, this register is set to "0".

ISOR0: Interrupt factor flag (FFFCH•D0)

This flag indicates the solar interrupt status.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

ISOR0 is set to "1" 0.75 to 1 seconds after the recharging flag ISOR1 is set to "1". Once initially generated, a wakeup interrupt is generated again at 2-second intervals as long as the recharging flag remains set. Note that this flag is set to "1" under the said condition, regardless of how the interrupt mask register is set.
This flag is reset to "0" by writing "1".
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

ISOR1: Recharging flag (FFFCH•D1)

This flag indicates whether the secondary battery is being recharged.

When "1" is read: Being recharged
When "0" is read: Not being recharged
Writing: Invalid

When the recharging detection circuit detects recharging of the secondary battery, this flag is set to "1" and retains value "1" during recharging. This flag is reset to "0" when no recharging operation is detected (as upon completion of recharging).
This flag is read-only, so that writing to this flag has no effect.
At initial reset, this flag is indeterminate.

ISOR2: Quick start mode flag 2 (FFFCH•D2)

This flag indicates whether the IC is operating in quick start mode.

When "1" is read: Quick start mode
When "0" is read: Normal mode
Writing: Invalid

When the IC exits the reset state (power supply voltage = 0.75 V) where it was placed due to stopped oscillation, it starts operating in quick start mode and simultaneously sets this flag to "1". This flag remains set in quick start mode, and is reset to "0" when the recharging voltage (VTKP) detection circuit detects a VTKP value equal to or greater than the quick start negation voltage (1.0 ± 0.08 V) twice in succession. When this flag = "0", the IC is operating in normal mode.
This flag is read-only, so that writing to this flag has no effect.
At initial reset, this flag is indeterminate.

ISOR3: Quick start mode flag 1 (FFFCH•D3)

This flag indicates whether the IC is operating in quick start mode.

When "1" is read: Quick start mode
When "0" is read: Normal mode
or when the quick start negation voltage is detected in quick start mode
Writing: Invalid

When the IC exits the reset state (power supply voltage = 0.75 V) where it was placed due to stopped oscillation, it starts operating in quick start mode and simultaneously sets this flag to "1". This flag remains set in quick start mode, and is reset to "0" when the recharging voltage (VTKP) detection circuit detects a VTKP value equal to or greater than the quick start negation voltage (1.0 ± 0.08 V) once.
This flag is read-only, so writing to this flag has no effect.
At initial reset, this flag is indeterminate.

ENISOR1: ISOR1 monitor output enable register (FF2DH•D3)
ENISOR2: ISOR2 monitor output enable register (FF09H•D2)
ENISOR3: ISOR3 monitor output enable register (FF09H•D3)

Control the ISOR1 to ISOR3 signal outputs.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

The ISOR1, ISOR2 and ISOR3 flag signals can be output to outside the IC from the P23, P31 and P30 ports, respectively. Before the signal can be output, fix the I/O control register (IOCxx) at "1" (output), the data register (Pxx) at "0" and the pull-down control register (PULxx) at "0" (pull-down disabled). When ENISORx is set to "1" under the conditions above, the ISORx signal is output from the Pxx terminal and when it is set to "0", the Pxx terminal goes low (V_{SS}) level.
At initial reset, these registers are set to "0".

CLIM: Overcharge status register (FF2DH•D1)

Indicates recharging status in the solar recharging control circuit.

When "1" is read: Overcharged (limiter ON)
When "0" is read: Not overcharged (limiter OFF)
Writing: Invalid

This register allows monitoring of overcharging status in the solar recharging control circuit.
At initial reset, this register is set to "0".

ECLIM: CLIM monitor output enable register (FF2DH•D2)

Controls the CLIM signal output.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Before the CLIM signal can be output, fix the I/O control register (IOC32) at "1" (output), the data register (P32) at "0" and the pull-down control register (PUL32) at "0" (pull-down disabled). When ECLIM is set to "1" under the conditions above, the CLIM signal is output from the P32 terminal and when it is set to "0", the P32 terminal goes low (V_{SS}) level.
At initial reset, this register is set to "0".

4.16.7 Programming notes

(1) The contents of timer processing and other control by software in quick start mode are forcibly initialized in hardware every 16 seconds. Therefore, precise time management cannot be sustained in quick start mode.

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) Do not perform the software reset for peripheral circuits (FF00H•D0) during quick start mode (when either ISOR2 or ISOR3 is set to "1").

4.17 Interrupt and HALT

<Interrupt types>

The S1C63709 provides the following interrupt functions.

External interrupt:	• Input interrupt	(2 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Solar interrupt	(1 system)
	• Programmable timer interrupt	(3 systems)
	• Serial interface interrupt	(1 system)
	• Motor interrupt	(2 systems)
	• Clock timer interrupt	(7 systems)
	• Stopwatch timer interrupt	(4 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.17.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The S1C63709 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped and the clock supply to the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

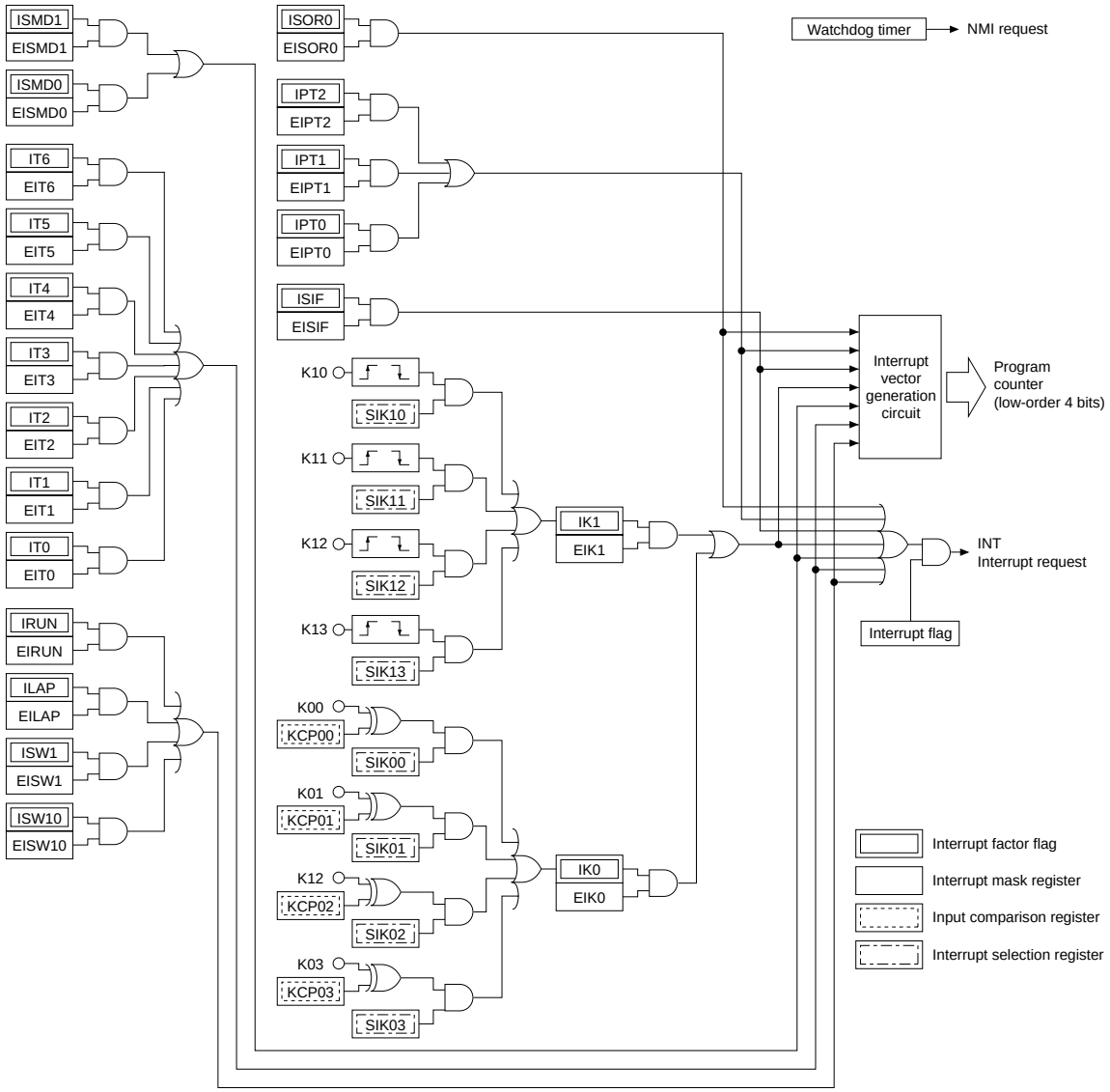


Fig. 4.17.1 Configuration of the interrupt circuit

4.17.1 Interrupt factor

Table 4.17.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.17.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Solar (wakeup)	ISOR0	(FFFCH•D0)
Programmable timer 2 (counter = 0)	IPT2	(FFF1H•D2)
Programmable timer 1 (counter = 0)	IPT1	(FFF1H•D1)
Programmable timer 0 (counter = 0)	IPT0	(FFF1H•D0)
Serial interface (8-bit data input/output completion)	ISIF	(FFF2H•D0)
K00–K03 input (falling edge or rising edge)	IK0	(FFF3H•D0)
K10–K13 input (falling edge or rising edge)	IK1	(FFF4H•D0)
Motor 1 (motor pulse counter = 0)	ISMD1	(FFF8H•D1)
Motor 0 (motor pulse counter = 0)	ISMD0	(FFF8H•D0)
Clock timer 128 Hz (falling edge)	IT6	(FFF9H•D2)
Clock timer 64 Hz (falling edge)	IT5	(FFF9H•D1)
Clock timer 16 Hz (falling edge)	IT4	(FFF9H•D0)
Clock timer 1 Hz (falling edge)	IT3	(FFF5H•D3)
Clock timer 2 Hz (falling edge)	IT2	(FFF5H•D2)
Clock timer 8 Hz (falling edge)	IT1	(FFF5H•D1)
Clock timer 32 Hz (falling edge)	IT0	(FFF5H•D0)
Stopwatch timer (direct RUN)	IRUN	(FFF6H•D3)
Stopwatch timer (direct LAP)	ILAP	(FFF6H•D2)
Stopwatch timer (1 Hz)	ISW1	(FFF6H•D1)
Stopwatch timer (10 Hz)	ISW10	(FFF6H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.17.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is reset to "0".
Table 4.17.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.17.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EISOR0	(FFECH•D0)	ISOR0	(FFFCH•D0)
EIPT2	(FFE1H•D2)	IPT2	(FFF1H•D2)
EIPT1	(FFE1H•D1)	IPT1	(FFF1H•D1)
EIPT0	(FFE1H•D0)	IPT0	(FFF1H•D0)
EISIF	(FFE2H•D0)	ISIF	(FFF2H•D0)
EIK0	(FFE3H•D0)	IK0	(FFF3H•D0)
EIK1	(FFE4H•D0)	IK1	(FFF4H•D0)
EISMD1	(FFE8H•D1)	ISMD1	(FFF8H•D1)
EISMD0	(FFE8H•D0)	ISMD0	(FFF8H•D0)
EIT6	(FFE9H•D2)	IT6	(FFF9H•D2)
EIT5	(FFE9H•D1)	IT5	(FFF9H•D1)
EIT4	(FFE9H•D0)	IT4	(FFF9H•D0)
EIT3	(FFE5H•D3)	IT3	(FFF5H•D3)
EIT2	(FFE5H•D2)	IT2	(FFF5H•D2)
EIT1	(FFE5H•D1)	IT1	(FFF5H•D1)
EIT0	(FFE5H•D0)	IT0	(FFF5H•D0)
EIRUN	(FFE6H•D3)	IRUN	(FFF6H•D3)
EILAP	(FFE6H•D2)	ILAP	(FFF6H•D2)
EISW1	(FFE6H•D1)	ISW1	(FFF6H•D1)
EISW10	(FFE6H•D0)	ISW10W10	(FFF6H•D0)

4.17.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.
2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.
4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.17.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.17.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High ↑
0102H	Solar	
0104H	Programmable timer	
0106H	Serial interface	
0108H	K0, K1 inputs	
010AH	Motor	
010CH	Clock timer	↓
010EH	Stopwatch timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.17.4 I/O memory of interrupt

Tables 4.17.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.17.4.1(a) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	K00–K03 input comparison register
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
					SIK11	0	Enable	Disable	
	R/W				SIK10	0	Enable	Disable	
FFE1H	0	EIPT2	EIPT1	EIPT0	0 *3	– *2			Unused
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2)
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
	R	R/W			EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE2H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE3H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE4H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE5H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE6H	EIRUN	EILAP	EISW1	EISW10	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
					EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
	R/W				EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFE8H	0	0	EISMD1	EISMD0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISMD1	0	Enable	Mask	Interrupt mask register (Motor driver 1)
					EISMD0	0	Enable	Mask	Interrupt mask register (Motor driver 0)
FFE9H	0	EIT6	EIT5	EIT4	0 *3	– *2			Unused
					EIT6	0	Enable	Mask	Interrupt mask register (Clock timer 128 Hz)
	R	R/W			EIT5	0	Enable	Mask	Interrupt mask register (Clock timer 64 Hz)
					EIT4	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFECH	EISOR3	EISOR2	EISOR1	EISOR0	EISOR3	0	1	0	General-purpose register
					EISOR2	0	1	0	General-purpose register
					EISOR1	0	1	0	General-purpose register
	R/W				EISOR0	0	Enable	Mask	Interrupt mask register (Solar wakeup)
FFF1H	0	IPT2	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
					IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
	R	R/W			IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF2H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
					0 *3	– *2	(W)	(W)	Unused
	R			R/W	ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.17.4.1(b) Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFF3H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF4H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF5H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF6H	IRUN	ILAP	ISW1	ISW10	IRUN	0	(R)	(R)	Interrupt factor flag (Stopwatch direct RUN)
					ILAP	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R/W				ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFF8H	0	0	ISMD1	ISMD0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISMD1	0	(W)	(W)	Interrupt factor flag (Motor driver 1)
					ISMD0	0	Reset	Invalid	Interrupt factor flag (Motor driver 0)
FFF9H	0	IT6	IT5	IT4	0 *3	– *2	(R)	(R)	Unused
					IT6	0	Yes	No	Interrupt factor flag (Clock timer 128 Hz)
	R	R/W			IT5	0	(W)	(W)	Interrupt factor flag (Clock timer 64 Hz)
					IT4	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFFCH	ISOR3	ISOR2	ISOR1	ISOR0	ISOR3	– *2	Pre Q start	Normal	Quick start mode flag 1
					ISOR2	– *2	Quick start	Normal	Quick start mode flag 2
					ISOR1	– *2	Charge	Not charged	Recharging flag
	R			R/W	ISOR0	0	(R)Yes (W)Reset	(R)No (W)Invalid	Interrupt factor flag (Solar wakeup)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

EISOR0: Interrupt mask register (FFECH•D0)
ISOR0: Interrupt factor flag (FFFCH•D0)

Refer to Section 4.16, "Solar Function".

EIPT2, EIPT1, EIPT0: Interrupt mask registers (FFE1H•D2, D1, D0)
IPT2, IPT1, IPT0: Interrupt factor flags (FFF1H•D2, D1, D0)

Refer to Section 4.9, "Programmable Timer".

EISIF: Interrupt mask register (FFE2H•D0)
ISIF: Interrupt factor flag (FFF2H•D0)

Refer to Section 4.10, "Serial Interface".

KCP03–KCP00: Input comparison registers (FF22H)
SIK03–SIK00, SIK13–SIK10: Interrupt selection registers (FF20H, FF24H)
EIK0, EIK1: Interrupt mask registers (FFE3H•D0, FFE4H•D0)
IK0, IK1: Interrupt factor flags (FFF3H•D0, FFF4H•D0)

Refer to Section 4.4, "Input Ports".

EISMD1, EISMD0: Interrupt mask registers (FFE8H•D1, D0)
ISMD1, ISMD0: Interrupt factor flags (FFF8H•D1, D0)

Refer to Section 4.12, "Motor Control Circuit".

EIT6–EIT4, EIT3–EIT0: Interrupt mask registers (FFE9H•D2–D0, FFE5H)
IT6–IT4, IT3–IT0: Interrupt factor flags (FFF9H•D2–D0, FFF5H)

Refer to Section 4.7, "Clock Timer".

EIRUN, EILAP, EISW1, EISW10: Interrupt mask registers (FFE6H)
IRUN, ILAP, ISW1, ISW10: Interrupt factor flags (FFF6H)

Refer to Section 4.8, "Stopwatch Timer".

4.17.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C63709 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
LCD system voltage circuit	LPWR
SVD circuit	SVDON
Heavy load protection	HVLDON

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in off status (OSCC = "0")

LCD system voltage circuit: Off status (LPWR = "0")

SVD circuit: Off status (SVDON = "0")

Heavy load protection: Off status (HVLDON = "0")

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Table 4.1.1 for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1). 16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63709 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access. After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

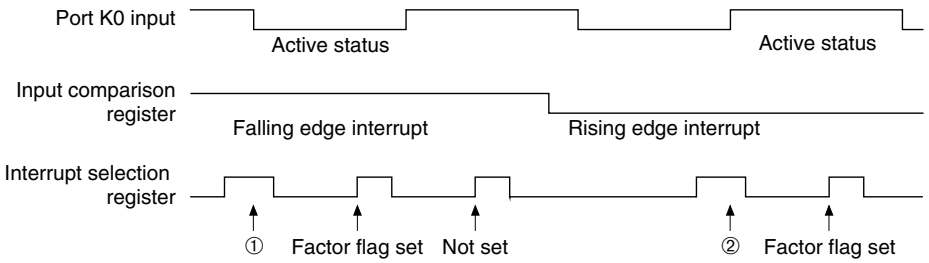
(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) The quick start mode prohibits the use of the OSC3 clock.

Input port

(1) When input ports are changed from high to low by pull-down resistors, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time. Particular care needs to be taken of the key scan during key matrix configuration. Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 300 kΩ (Max.)

(2) Input interrupt programming related precautions
When using an input interrupt, if you rewrite the content of the interrupt selection register, when the value of the input terminal which becomes the interrupt input is in active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies
input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.



When the content of the interrupt selection register is rewritten while the port K0 input is in the active status, the input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 5.2.1 Input interrupt timing

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 5.2.1. However, when clearing the content of the interrupt selection register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in active status (low status), do not rewrite the interrupt selection register (clearing, then setting the interrupt selection register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the interrupt selection register, set the interrupt selection register, when the input terminal is not in active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 5.2.1. In this case, when the interrupt selection registers cleared, then set, you should set the interrupt selection register, when the input terminal is in low status.
In addition, when the interrupt selection register = "1" and the content of the input comparison register is rewritten in input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the interrupt selection register = "0" status.

The same applies to the K12 and K13 ports when the input sampling circuit is off. When the input terminal is in active status (high status), do not rewrite the interrupt selection register (clearing, then setting the interrupt selection register).

I/O port

(1) When in the input mode, I/O ports are changed from high to low by pull-down resistor, the fall of the waveform is delayed on account of the time constant of the pull-down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$ C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-down resistance 300 kΩ (Max.)

(2) The data register, I/O control register and pull-down control register are effective even if the Pxx is used for special output. To prevent the occurrence of undesired terminal conditions, do not change the register values after setting the data register (Pxx) to "0", the I/O control register (IOCxx) to "1", and the pull-down control register (PULxx) to "0".

(3) A hazard may occur when the FOUT, TOUT or F16HZ signal is turned on and off.

(4) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

LCD driver

Because at initial reset, the contents of display memory are undefined and LC3–LC0 (LCD contrast) is set to 0000B, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes off.

Clock timer

Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

Stopwatch timer

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWD0–3 → SWD4–7 → SWD8–11.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWD8–11 and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTDx0–PTDx3) first. Furthermore, the high-order 4 bits (PTDx4–PTDx7) should be read within 0.73 msec (when f_{OSC1} is 32.768 kHz) of reading the low-order 4 bits (PTDx0–PTDx3).

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to the PTRUNx register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUNx register maintains "1" for reading until the timer actually stops.
Figure 5.2.2 shows the timing chart for the RUN/STOP control.

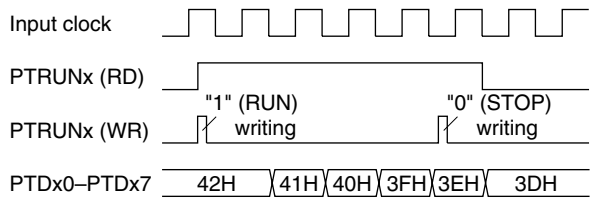


Fig. 5.2.2 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned on and off by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the off state.

(5) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

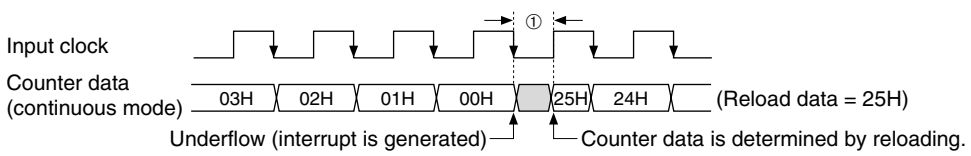


Fig. 5.2.3 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

Serial interface

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

Sound generator

(1) When using the P40 port as the BZ output port, fix the I/O control register (IOC40) at "1" (output), data register (P40) at "0" and the pull-down control register (PUL40) at "0" (pull-down disabled).

(2) Since it generates a buzzer signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes on/off due to the setting of the BZE register.

(3) The one-shot output is only valid when the normal buzzer output is off (BZE = "0") and will be invalid when the normal buzzer output is on (BZE = "1").

Motor control circuit

(1) Motor driver 0 supports two drive methods (fast-feed drive for normal/reverse rotation and fixed drive), with different control registers used for the respective drive methods. Please exercise caution regarding control to prevent the output of different drive waveforms at the same time.

(2) To abort fast-feed drive, be sure to temporarily stop it (by setting MxENM = "0") before clearing the motor pulse counter. Clearing this counter during drive may cause the motor driver to operate erratically.

(3) If the sum total of fast-feed drive pulses (P1 + Pr, G1 + G2 + G3 + Gr) exceeds the motor clock period, the motor driver will not operate normally. Always make sure the said sum total is less than the motor clock period.

(4) If the sum total of the P1 and Pr pulses exceeds the motor clock cycle, the Pr pulse output is forcibly terminated before the next motor clock output is started. In this case, a hazard may occur on the waveform at forced termination of the Pr pulse output. Therefore, always be sure that said sum total is less than the motor clock cycle.
The table below shows the actual P1 and Pr output period (or the time from start of the pulse output until the Pr pulse output is terminated) when the setting of the P1 and Pr pulses exceeds the motor clock cycle.

Table 5.2.1 Drive pulse output period when Pr pulse is forcibly terminated

Motor clock	Forced terminating conditions	Drive pulse output period
128 Hz	[P1+Pr] > 7.324 msec	7.568 msec
85.3 Hz	[P1+Pr] > 11.230 msec	11.475 msec
64 Hz	[P1+Pr] > 15.137 msec	15.381 msec

(5) It is prohibited to use the 128-Hz motor clock for fast-feed drive at reverse rotation. Even if fast-feed drive at reverse rotation is attempted with the 128-Hz motor clock selected, the motor driver will be unable to perform fast-feed drive normally.

(6) Do not change the pulse width, number of pulses, or duty cycle when the motor driver is outputting drive pulses. Changing these parameters during pulse output may cause the motor driver to operate erratically.

Theoretical regulation function

(1) Caution is required since executing theoretical regulation during drive pulse output by the motor driver may change the pulse width.

(2) When "1" is written to VCWON, the theoretical regulation starts synchronously with the first falling edge of the 512XM signal after the 64-Hz signal goes low. Therefore, there is a delay of up to 16.6 msec before theoretical regulation actually starts. Writing "1" to VCWON in this period is ineffective, so to write "1" to VCWON successively, an interval at least 16.6 msec is necessary between writings.

(3) Make sure that the CPU is operating with the OSC1 clock before reading an amount of correction from the K20–K23 and K30 ports.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be on for at least 1 msec. So, to obtain the SVD detection result, follow the programming sequence below.
1. Set SVDON to "1"
2. Maintain for 1 msec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned off because SVD operation increase current consumption.

(3) Eight detection voltages must be selected from addresses FF50H–FF55H for each of the 1.5 V and 3.0 V systems. The SVD circuit may not work normally if eight voltages are not selected (e.g., seven or ten voltages are selected).

Heavy load protection mode

In the heavy load protection mode, more current is consumed than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

Solar function

(1) The contents of timer processing and other control by software in quick start mode are forcibly initialized in hardware every 16 seconds. Therefore, precise time management cannot be sustained in quick start mode.

(2) Do not perform the software reset for peripheral circuits (FF00H•D0) during quick start mode (when either ISOR2 or ISOR3 is set to "1").

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

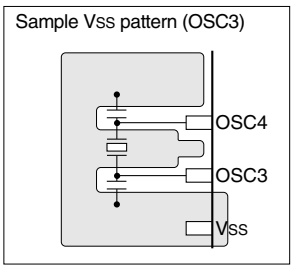
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

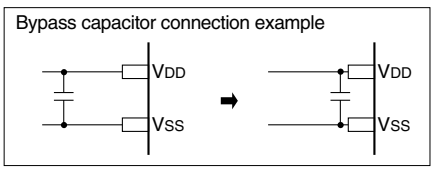
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When using the built-in pull-down resistor of the RESET terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminals with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.

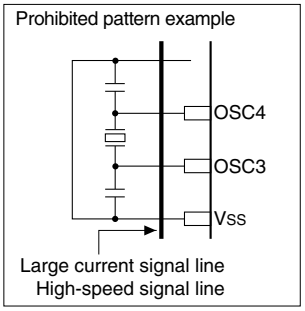


  (3) Components which are connected to the VD1, VOSC and VC1–VC3 terminals, such as capacitors, should be connected in the shortest line.
  In particular, the VC1–VC3 voltages affect the display quality.

- Do not connect anything to the VC1–VC3 terminals when the LCD driver is not used.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

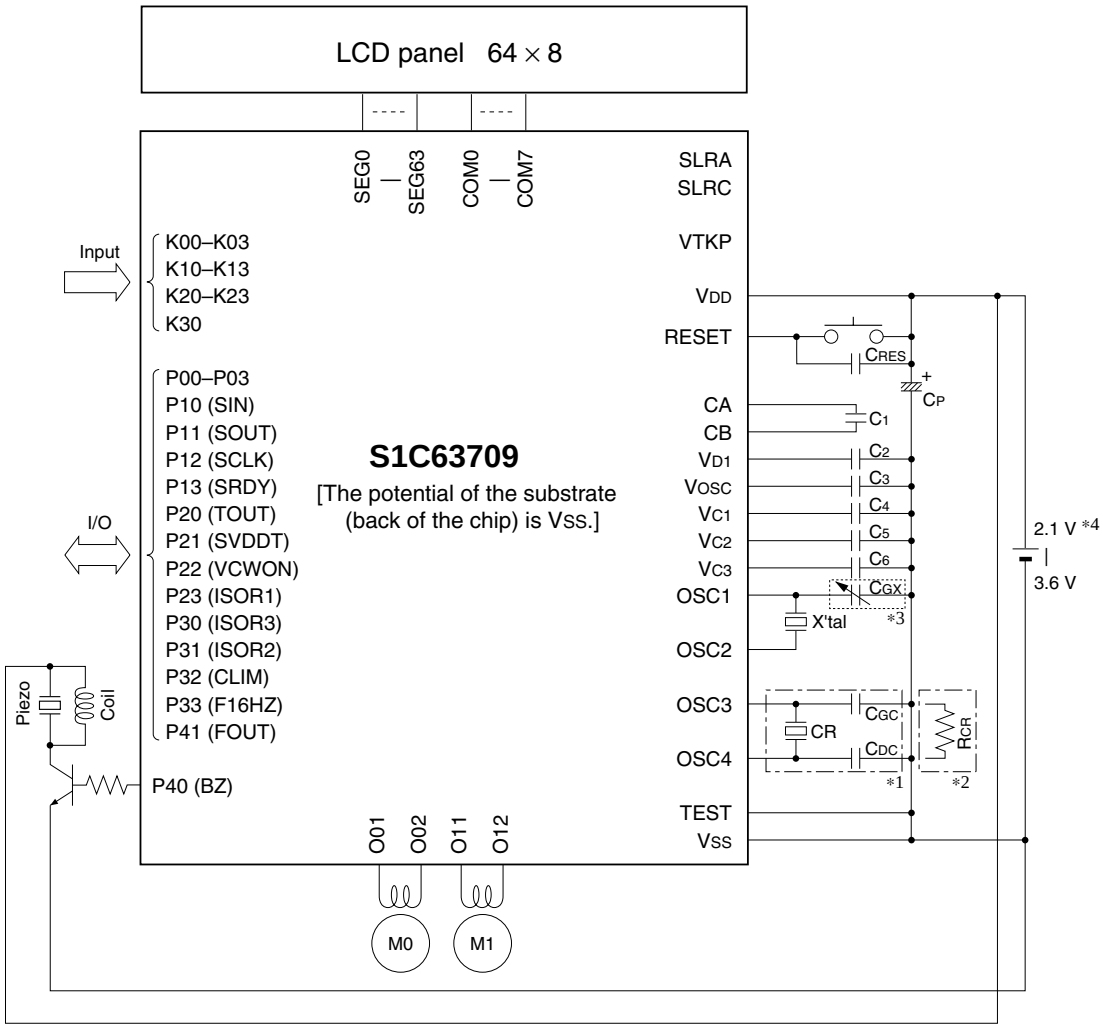
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM

(1) When a primary cell is used

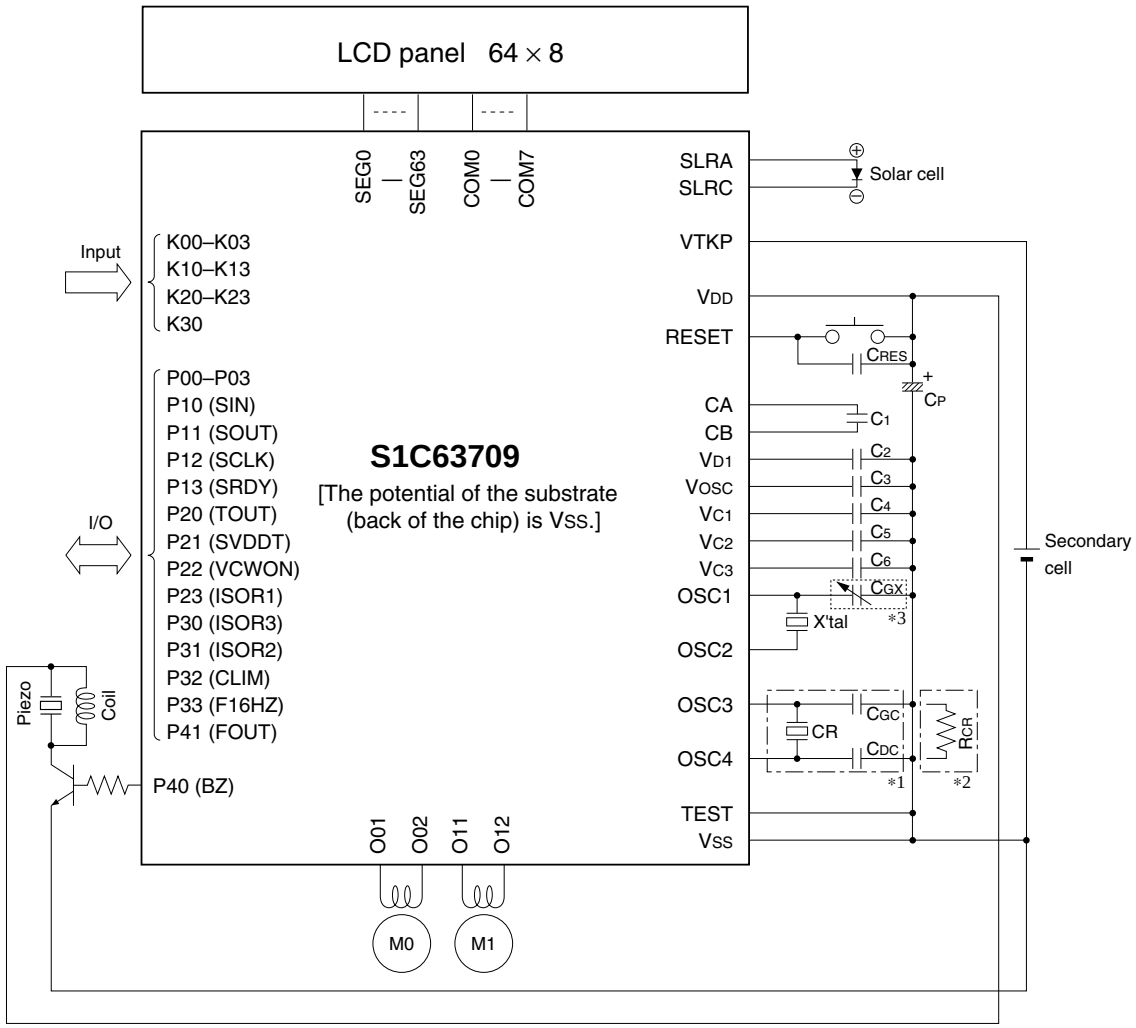


X'tal	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ, CL(Typ.) = 6 pF
CGX	Trimmer capacitor	0–20 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR	Resistor for OSC3 CR oscillation	75 kΩ (1.1 MHz)
C1–C6	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

*1: Ceramic oscillation
*2: CR oscillation (external R)
*3: CG regulation
*4: 1.0–3.6 V when OSC3 is not used or OSC3 CR oscillation (built-in R) is used

Note: The above table is simply an example, and is not guaranteed to work.

(2) When a solar cell is used



X'tal	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ, CL(Typ.) = 6 pF
CGX	Trimmer capacitor	0–20 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR	Resistor for OSC3 CR oscillation	75 kΩ (1.1 MHz)
C1–C6	Capacitor	0.2 µF
CP	Capacitor	4.7 µF
CRES	RESET terminal capacitor	0.1 µF

*1: Ceramic oscillation
*2: CR oscillation (external R)
*3: CG regulation

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(VSS=0V)

Item	Symbol	Rated value	Unit
Supply voltage	VDD	-0.5 to 4.5	V
Input voltage (1)	VI	-0.5 to VDD + 0.3	V
Input voltage (2)	VIOSC	-0.5 to VD1 + 0.3	V
Permissible total output current *1	ΣIVDD	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	PD	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP20-144pin).

7.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	VDD	VSS=0V	when OSC3 is not used	1.0 *1		3.6	V
			when OSC3 is used, 260kHz (Max.)	1.0 *1		3.6	V
			when OSC3 is used, 4.2MHz (Max.)	2.1		3.6	V
Oscillation frequency	fOSC1	Crystal oscillation		–	32.768	–	kHz
	fOSC3	CR oscillation (built-in R), VDD=1.0 to 3.6V		140	200	260	kHz
		CR oscillation (external R), VDD=2.1 to 3.6V		200	1,100	2,200	kHz
		Ceramic oscillation, VDD=2.1 to 3.6V				4,200	kHz

*1 2.1 V when internal power supply (VC2 regulator) is selected as the power supply for driving the LCD.

7.3 DC Characteristics

Unless otherwise specified:

VDD=3.0V, VSS=0V, fOSC1=32.768kHz, Ta=25°C, VD1/VC1–VC3 are internal voltage, C1–C6=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	VIH1		Kxx, Pxx	0.8·VDD		VDD	V
High level input voltage (2)	VIH2		RESET, TEST	0.9·VDD		VDD	V
Low level input voltage (1)	VIL1		Kxx, Pxx	0		0.2·VDD	V
Low level input voltage (2)	VIL2		RESET, TEST	0		0.1·VDD	V
High level input current (1)	IIH1	VIH1=3.0V No pull down	Kxx, Pxx, RESET, TEST	0		0.5	µA
High level input current (2)	IIH2	VIH2=3.0V With pull down	Kxx, Pxx, RESET, TEST	8	12	20	µA
Low level input current (1)	IIL1	VIL1=VSS No pull down	Kxx, Pxx, RESET, TEST	-0.5		0	µA
Low level input current (2)	IIL2	VIL2=VSS With pull down	Kxx, Pxx, RESET, TEST	-0.5		0	µA
High level output current (1)	IOH1	VOH1=0.9·VDD	Pxx			-0.5	mA
High level output current (2)	IOH2	VOH2=VDD-0.05V	O01, O02, O11, O12			-0.8	mA
Low level output current (1)	IOL1	VOL1=0.1·VDD	Pxx	0.5			mA
Low level output current (2)	IOL2	VOL2=VSS+0.05V	O01, O02, O11, O12	0.8			mA
Common output current	IOH3	VOH3=VC3-0.05V	COM0–7			-10	µA
	IOL3	VOL3=VSS+0.05V		10			µA
Segment output current (during LCD output)	IOH4	VOH4=VC3-0.05V	SEG0–63			-10	µA
	IOL4	VOL4=VSS+0.05V		10			µA
Segment output current (during DC output)	IOH5	VOH5=0.9·VDD	SEG0–63			-150	µA
	IOL5	VOL5=0.1·VDD		150			µA

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} regulator is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"		1.07		V
			LC0–3="1"		1.10		
			LC0–3="2"		1.13		
			LC0–3="3"		1.16		
			LC0–3="4"		1.19		
			LC0–3="5"		1.21		
			LC0–3="6"		1.23		
			LC0–3="7"	Typ.	1.25	Typ.	
			LC0–3="8"	-100mV	1.27	+100mV	
			LC0–3="9"		1.29		
			LC0–3="10"		1.31		
			LC0–3="11"		1.33		
			LC0–3="12"		1.35		
			LC0–3="13"		1.37		
			LC0–3="14"		1.39		
			LC0–3="15"		1.41		
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1}	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1}	V
LCD drive voltage (when V_{C2} regulator is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C2} ×0.95		1/2·V_{C2}	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"		2.08		V
			LC0–3="1"		2.14		
			LC0–3="2"		2.20		
			LC0–3="3"		2.26		
			LC0–3="4"		2.32		
			LC0–3="5"		2.38		
			LC0–3="6"		2.44		
			LC0–3="7"	Typ.	2.50	Typ.	
			LC0–3="8"	-100mV	2.56	+100mV	
			LC0–3="9"		2.60		
			LC0–3="10"		2.64		
			LC0–3="11"		2.68		
			LC0–3="12"		2.72		
			LC0–3="13"		2.76		
			LC0–3="14"		2.80		
			LC0–3="15"		2.84		
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3/2·V_{C2} ×0.95		3/2·V_{C2}	V
SVD voltage for 1.5 V system (SVDCHG = "0") *1	V_{SVD15}	S15V16="1"			1.60		V
		S15V15="1" (default)			1.50		
		S15V14="1" (default)			1.40		
		S15V135="1"			1.35		
		S15V13="1" (default)		Typ.	1.30	Typ.	
		S15V125="1" (default)		-100mV	1.25	+100mV	
		S15V12="1" (default)			1.20		
		S15V115="1" (default)			1.15		
		S15V11="1" (default)			1.10		
		S15V105="1" (default)			1.05		
SVD voltage for 3.0 V system (SVDCHG = "1") *1	V_{SVD30}	S3V27="1" (default)			2.70		V
		S3V265="1"		Typ.	2.65	Typ.	
		S3V26="1" (default)		-100mV	2.60	+100mV	
		S3V25="1"			2.50		
		S3V24="1"			2.40		
		S3V235="1"		Typ.	2.35	Typ.	
		S3V23="1" (default)		-60mV	2.30	+60mV	
		S3V225="1"			2.25		
		S3V22="1"			2.20		
		S3V21="1" (default)			2.10		
		S3V20="1" (default)		Typ.	2.00	Typ.	
		S3V19="1" (default)		-100mV	1.90	+100mV	
		S3V18="1" (default)			1.80		
		S3V17="1" (default)			1.70		
SVD circuit response time	t_{SVD}					1	ms

*1 8 values only can be used for voltage detection.

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in HALT mode (when theoretical regulation is selected)	I_{HALT1}	32kHz crystal, LCD OFF *1, *2		0.15	0.30	µA
		32kHz crystal, LCD ON (V_{C1} regulator) *1, *2		1.10	1.40	µA
		32kHz crystal, LCD ON (V_{C2} regulator) *1, *2		0.90	1.20	µA
		32kHz crystal, LCD OFF *1, *3		0.25	0.70	µA
		32kHz crystal, LCD ON (V_{C1} regulator) *1, *3		1.25	1.60	µA
		32kHz crystal, LCD ON (V_{C2} regulator) *1, *3		1.05	1.35	µA
Current consumption in HALT mode (when CG regulation is selected)	I_{HALT2}	32kHz crystal, LCD OFF *1, *2		0.25	0.45	µA
		32kHz crystal, LCD ON (V_{C1} regulator) *1, *2		1.20	1.55	µA
		32kHz crystal, LCD ON (V_{C2} regulator) *1, *2		1.00	1.35	µA
		32kHz crystal, LCD OFF *1, *3		0.35	0.85	µA
		32kHz crystal, LCD ON (V_{C1} regulator) *1, *3		1.35	1.75	µA
		32kHz crystal, LCD ON (V_{C2} regulator) *1, *3		1.15	1.50	µA
Current consumption in Run state	I_{EXE}	32kHz crystal, LCD OFF *1, *2		2.3	2.6	µA
		32kHz crystal, LCD ON *1, *2, *4		3.5	4.0	µA
		32kHz crystal, LCD OFF *1, *3		5.5	6.5	µA
		32kHz crystal, LCD ON *1, *3, *4		6.7	8.0	µA
		200kHz CR, LCD ON *1, *2		25	40	µA
		1.1MHz CR, LCD ON *1, *3		600	750	µA
		2MHz ceramic, LCD ON *1, *3		650	900	µA
		4MHz ceramic, LCD ON *1, *3		950	1200	µA
SVD circuit current	I_{SVD}	During voltage detection, V_{DD}=1.0 to 3.6V		2.0	3.0	µA

∗1 No panel load. When the SVD circuit and motor driver are OFF
∗2 When CR (built-in R type) is selected for the OSC3 oscillation circuit by mask option
∗3 When CR (external R type) is selected for the OSC3 oscillation circuit by mask option
∗4 When theoretical regulation and V_{C1} regulator are selected by mask option

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit (when theoretical regulation is selected)

Unless otherwise specified:
V_{DD}=1.0 to 3.6V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=C_D=built-in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	1.0			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	1.0			V
Built-in capacitance (gate)	C_G	Including the parasitic capacitance inside the IC (in chip)		12		pF
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		8		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=1.0 to 3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Harmonic oscillation start voltage	V_{hho}		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC1 crystal oscillation circuit (when C_G regulation is selected)

Unless otherwise specified:
V_{DD}=1.0 to 3.6V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=C_D=built-in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	1.0			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	1.0			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		8		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=1.0 to 3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=0 to 20pF	10	20		ppm
Harmonic oscillation start voltage	V_{hho}		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC3 ceramic oscillation circuit

Unless otherwise specified:
V_{DD}=2.1 to 3.6V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.1			V
Oscillation start time	tsta	V_{DD}=2.1 to 3.6V			5	ms
Oscillation stop voltage	Vstp	(V_{DD})	2.1			V

OSC3 CR oscillation circuit (built-in R type)

Unless otherwise specified:
V_{DD}=1.0 to 3.6V, V_{SS}=0V, R_{CR}=Built in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	200kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	1.0			V
Oscillation start time	tsta	V_{DD}=1.0 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(V_{DD})	1.0			V

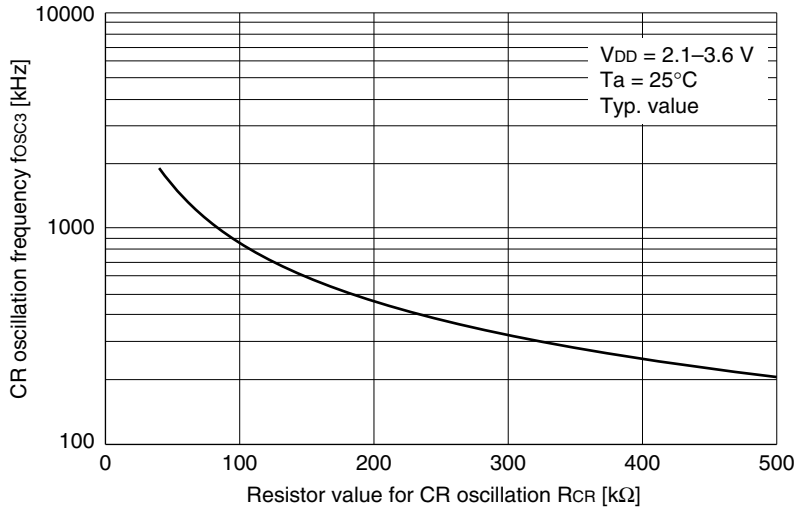
OSC3 CR oscillation circuit (external R type)

Unless otherwise specified:
V_{DD}=2.1 to 3.6V, V_{SS}=0V, R_{CR}=75kΩ (1.1MHz), Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30		30	%
Oscillation start voltage	Vsta	(V_{DD})	2.1			V
Oscillation start time	tsta	V_{DD}=2.1 to 3.6V			3	ms
Oscillation stop voltage	Vstp	(V_{DD})	2.1			V

OSC3 CR oscillation frequency-resistance characteristic (external R type)

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



7.6 Solar Control Circuit Characteristics

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_6=0.2µF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Quick start negation voltage	V_{ON}	VTKP voltage	Typ. -80mV	1.0	Typ. +80mV	V
Limiter ON voltage (selected by mask option)	V_{LIM}	VTKP voltage	Typ. -80mV	2.1	Typ. +80mV	V
				2.5		
				2.6		
				2.7		
				2.8		
				2.9		
				3.0		
				3.1		
				3.2		

7.7 Serial Interface AC Characteristics

Clock synchronous master mode

• During 32 kHz operation

Condition: V_{DD}=1.0 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µs
Receiving data input set-up time	tsms	10			µs
Receiving data input hold time	tsmh	5			µs

• During 1 MHz operation

Condition: V_{DD}=2.1 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	ns
Receiving data input set-up time	tsms	400			ns
Receiving data input hold time	tsmh	200			ns

Note that the maximum clock frequency is limited to 1 MHz.

Clock synchronous slave mode

• During 32 kHz operation

Condition: V_{DD}=1.0 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µs
Receiving data input set-up time	tsss	10			µs
Receiving data input hold time	tssh	5			µs

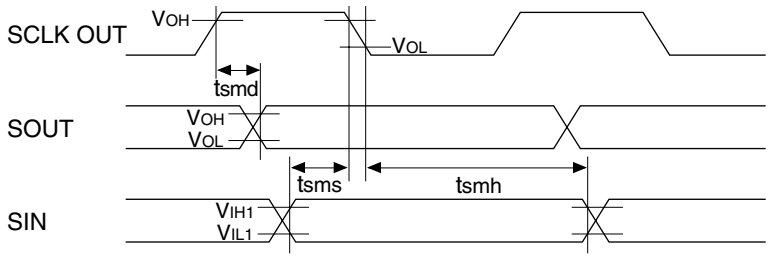
• During 1 MHz operation

Condition: V_{DD}=2.1 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

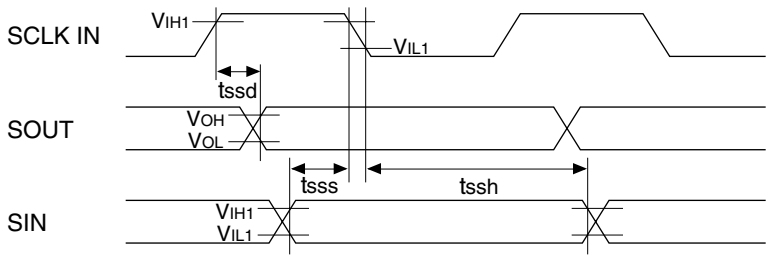
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	ns
Receiving data input set-up time	tsss	400			ns
Receiving data input hold time	tssh	200			ns

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

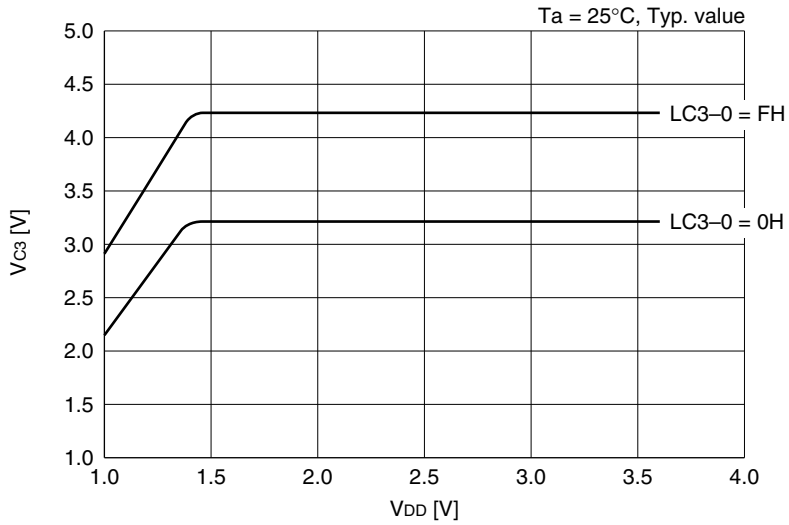


<Slave mode>

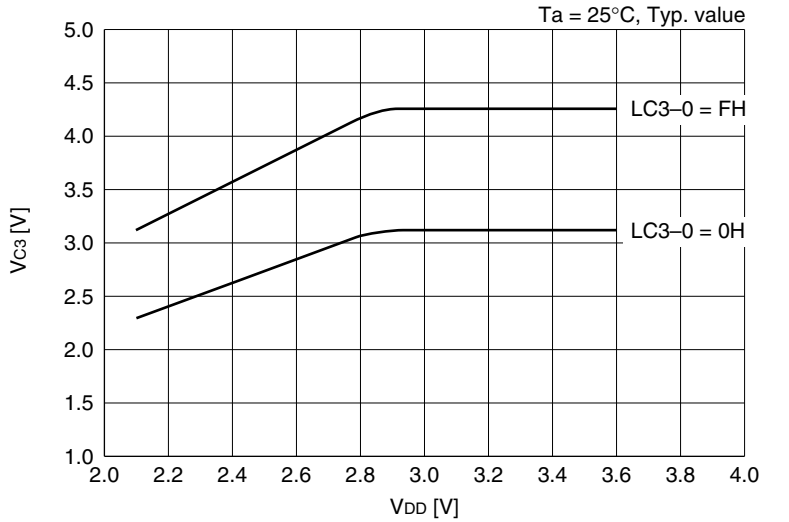


7.8 Characteristics Curves (reference value)

LCD drive voltage - power supply voltage characteristic (V_{C1} regulator)



LCD drive voltage - power supply voltage characteristic (V_{C2} regulator)

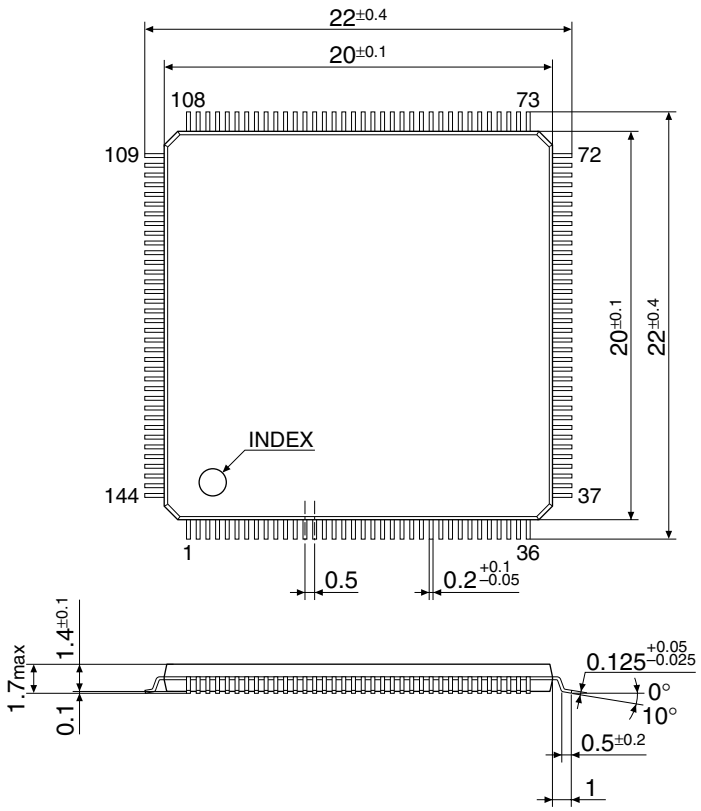


CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP20-144pin

(Unit: mm)

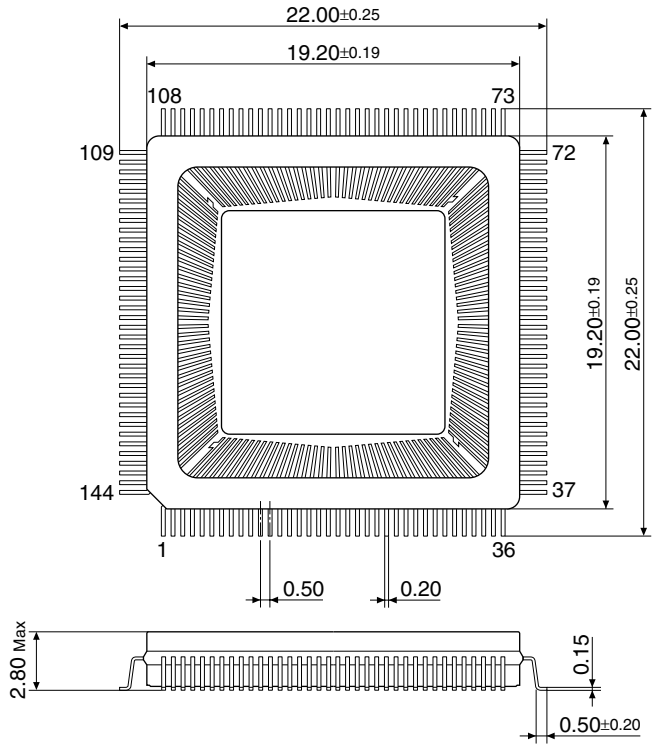


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

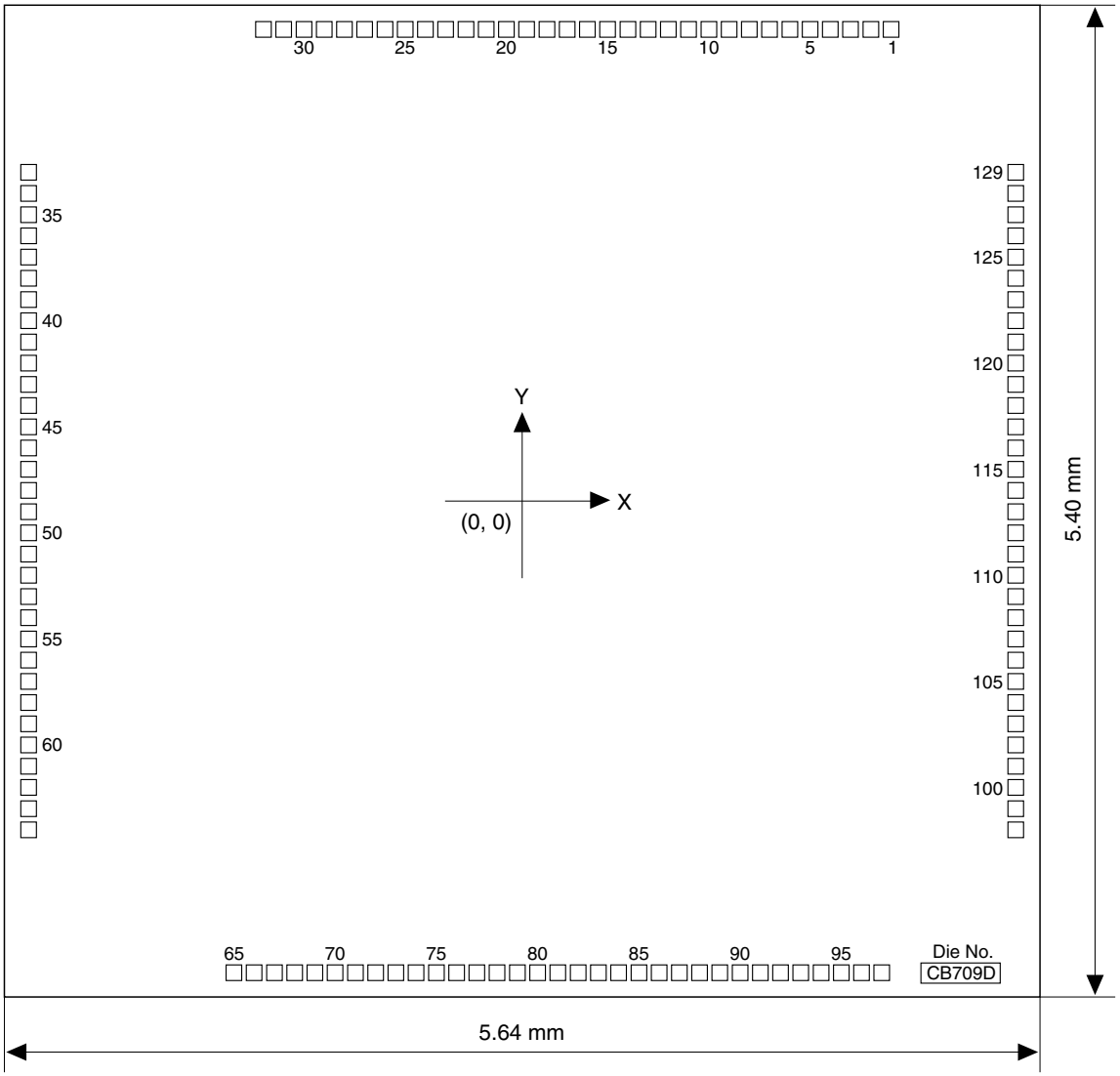
QFP17-144pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 90 µm

9.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	COM0	2.009	2.568	33	SEG32	-2.688	1.790	65	COM4	-1.570	-2.568	98	SEG0	2.688	-1.790
2	COM1	1.899	2.568	34	SEG33	-2.688	1.675	66	COM5	-1.460	-2.568	99	SEG1	2.688	-1.675
3	COM2	1.788	2.568	35	SEG34	-2.688	1.559	67	COM6	-1.349	-2.568	100	SEG2	2.688	-1.559
4	COM3	1.678	2.568	36	SEG35	-2.688	1.444	68	COM7	-1.239	-2.568	101	SEG3	2.688	-1.444
5	CA	1.568	2.568	37	SEG36	-2.688	1.328	69	P41	-1.129	-2.568	102	SEG4	2.688	-1.328
6	CB	1.458	2.568	38	SEG37	-2.688	1.213	70	P40	-1.019	-2.568	103	SEG5	2.688	-1.213
7	V_{C1}	1.347	2.568	39	SEG38	-2.688	1.097	71	P33	-0.908	-2.568	104	SEG6	2.688	-1.097
8	V_{C2}	1.237	2.568	40	SEG39	-2.688	0.982	72	P32	-0.798	-2.568	105	SEG7	2.688	-0.982
9	V_{C3}	1.127	2.568	41	SEG40	-2.688	0.866	73	P31	-0.688	-2.568	106	SEG8	2.688	-0.866
10	V_{DD}	1.017	2.568	42	SEG41	-2.688	0.751	74	P30	-0.578	-2.568	107	SEG9	2.688	-0.751
11	V_{OSC}	0.906	2.568	43	SEG42	-2.688	0.635	75	P23	-0.467	-2.568	108	SEG10	2.688	-0.635
12	OSC1	0.796	2.568	44	SEG43	-2.688	0.520	76	P22	-0.357	-2.568	109	SEG11	2.688	-0.520
13	OSC2	0.686	2.568	45	SEG44	-2.688	0.404	77	P21	-0.247	-2.568	110	SEG12	2.688	-0.404
14	V_{D1}	0.576	2.568	46	SEG45	-2.688	0.289	78	P20	-0.137	-2.568	111	SEG13	2.688	-0.289
15	OSC3	0.465	2.568	47	SEG46	-2.688	0.173	79	V_{DD}	-0.026	-2.568	112	SEG14	2.688	-0.173
16	OSC4	0.355	2.568	48	SEG47	-2.688	0.058	80	SLRA	0.084	-2.568	113	SEG15	2.688	-0.058
17	V_{SS}	0.245	2.568	49	SEG48	-2.688	-0.058	81	VTKP	0.194	-2.568	114	SEG16	2.688	0.058
18	TEST	0.135	2.568	50	SEG49	-2.688	-0.173	82	SLRC	0.305	-2.568	115	SEG17	2.688	0.173
19	RESET	0.024	2.568	51	SEG50	-2.688	-0.289	83	V_{SS}	0.415	-2.568	116	SEG18	2.688	0.289
20	K00	-0.086	2.568	52	SEG51	-2.688	-0.404	84	V_{DD}	0.525	-2.568	117	SEG19	2.688	0.404
21	K01	-0.196	2.568	53	SEG52	-2.688	-0.520	85	O01	0.635	-2.568	118	SEG20	2.688	0.520
22	K02	-0.306	2.568	54	SEG53	-2.688	-0.635	86	O02	0.746	-2.568	119	SEG21	2.688	0.635
23	K03	-0.417	2.568	55	SEG54	-2.688	-0.751	87	O11	0.856	-2.568	120	SEG22	2.688	0.751
24	K10	-0.527	2.568	56	SEG55	-2.688	-0.866	88	O12	0.966	-2.568	121	SEG23	2.688	0.866
25	K11	-0.637	2.568	57	SEG56	-2.688	-0.982	89	V_{SS}	1.076	-2.568	122	SEG24	2.688	0.982
26	K12	-0.747	2.568	58	SEG57	-2.688	-1.097	90	P13	1.187	-2.568	123	SEG25	2.688	1.097
27	K13	-0.858	2.568	59	SEG58	-2.688	-1.213	91	P12	1.297	-2.568	124	SEG26	2.688	1.213
28	K20	-0.968	2.568	60	SEG59	-2.688	-1.328	92	P11	1.407	-2.568	125	SEG27	2.688	1.328
29	K21	-1.078	2.568	61	SEG60	-2.688	-1.444	93	P10	1.517	-2.568	126	SEG28	2.688	1.444
30	K22	-1.188	2.568	62	SEG61	-2.688	-1.559	94	P03	1.628	-2.568	127	SEG29	2.688	1.559
31	K23	-1.299	2.568	63	SEG62	-2.688	-1.675	95	P02	1.738	-2.568	128	SEG30	2.688	1.675
32	K30	-1.409	2.568	64	SEG63	-2.688	-1.790	96	P01	1.848	-2.568	129	SEG31	2.688	1.790
–	–	–	–	–	–	–	–	97	P00	1.958	-2.568	–	–	–	–

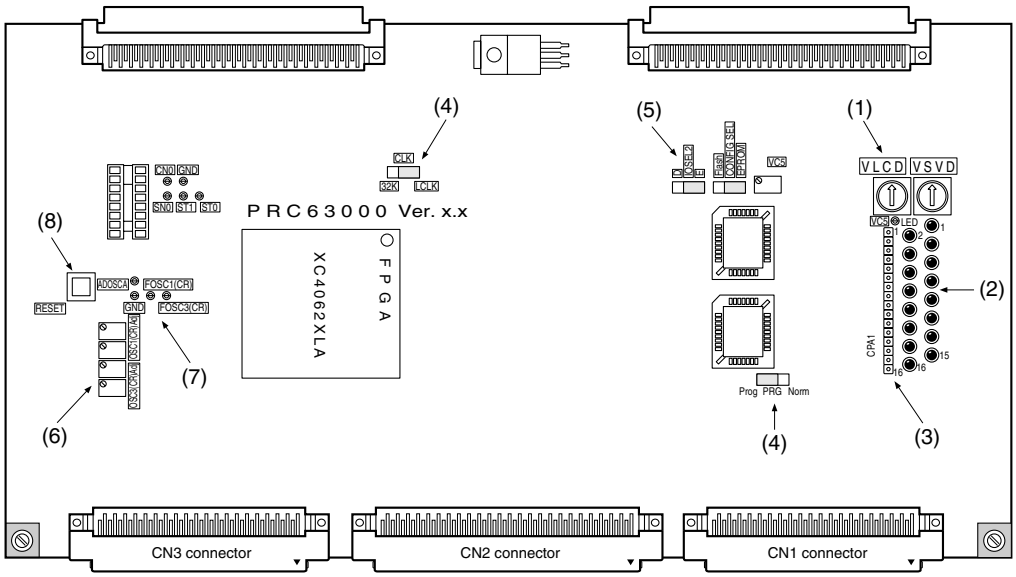
APPENDIX PERIPHERAL CIRCUIT BOARDS FOR S1C63709

This section describes how to use the Peripheral Circuit Boards for the S1C63709 (S5U1C63000P1 and S5U1C63709P2), which provide emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H1/S5U1C63000H2).
This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P1) provided in this document assumes that circuit data for the S1C63709 has already been downloaded to the board. For information on downloading various circuit data, please see Section A.3. Please refer to the user's manual provided with your ICE for detailed information on its functions and method of use.

A.1 Names and Functions of Each Part

A.1.1 S5U1C63000P1

The S5U1C63000P1 board provides peripheral circuit functions of S1C63 Family microcomputers other than the core CPU. The following explains the names and functions of each part of the S5U1C63000P1 board. Switches, sockets and other parts on the board are not used for development of an S1C63709 system if they are not explained below.



(1) VLCD

When external LCD power supply has been selected by mask option, you can turn this control to adjust the LCD drive power supply voltage.

(2) Register monitor LEDs

These LEDs correspond one-to-one to the registers, functions and signals listed below. The LED lights or goes out according to their statuses.

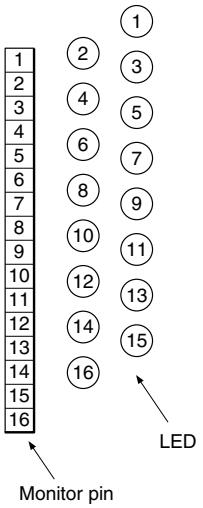
- OSCC, CLKCHG, LPWR, SVDS0–SVDS2, SVDCHG, SVDON, HVLDON, and VCWON (register status)
  Lit: register = "1", Not lit: register = "0"
- HVLD (heavy load protection function status)
  Lit: heavy load protection on, Not lit: heavy load protection off
- SLRCPUPOFF (electricity generation signal status)
  Lit: generated, Not lit: not generated (unused)
- PGDCGATE (recharging detection output signal status)
  Lit: output, Not lit: not output
- TRIM (regulation repeat counts setting register TRIM0 status)
  Lit: register = "1", Not lit: register = "0"
- QUIRE (solar circuit's "reset in quick start mode" signal status)
  Lit: output, Not lit: not output

(3) Register monitor pins

These pins correspond one-to-one to the registers listed below. The pin outputs a high for logic "1" and a low for logic "0".

Monitor		LED	
Pin No.	Name	LED No.	Name
1	DONE *	1	DONE *
2	SVDS0	2	SVDS0
3	SVDS1	3	SVDS1
4	SVDS2	4	SVDS2
5	SVDCHG	5	SVDCHG
6	SVDON	6	SVDON
7	LPWR	7	LPWR
8	HVLDON	8	HVLDON
9	HVLD	9	HVLD
10	VCWON	10	VCWON
11	SLRCPUPOFF	11	SLRCPUPOFF
12	PGDCGATE	12	PGDCGATE
13	TRIM	13	TRIM
14	QUIRE	14	QUIRE
15	OSCC	15	OSCC
16	CLKCHG	16	CLKCHG

∗ DONE: The monitor pin outputs a high while the LED lights when initialization of this board completes without problems.



(4) CLK and PRG switch

If power to the ICE is shut down before circuit data downloading is complete, the circuit configuration in this board will remain incomplete, and the debugger may not be able to start when you power on the ICE once again. In this case, temporarily power off the ICE and set CLK to the 32K position and the PRG switch to the Prog position, then switch on power for the ICE once again. This should allow the debugger to start up, allowing you to download circuit data. After downloading the circuit data, temporarily power off the ICE and reset CLK and PRG to the LCLK and the Norm position, respectively. Then power on the ICE once again.

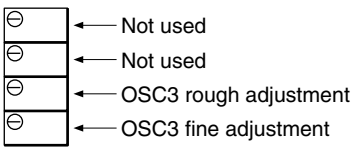
(5) IOSEL2

When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

(6) CR oscillation frequency adjusting control

This control allows you to adjust the OSC3 oscillation frequency. This function is effective when ceramic oscillation is selected for the OSC3 oscillation circuit by mask option as well as when CR oscillation is selected. The oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "Electrical Characteristics", to select the appropriate operating frequency.

Adjust the frequency before inserting the S5U1C63709P2 board.

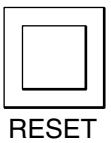


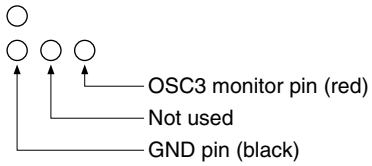
(7) CR oscillation frequency monitor pins

These pins allow you to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that these pins always output a signal waveform whether or not the oscillation circuit is operating.

(8) RESET switch

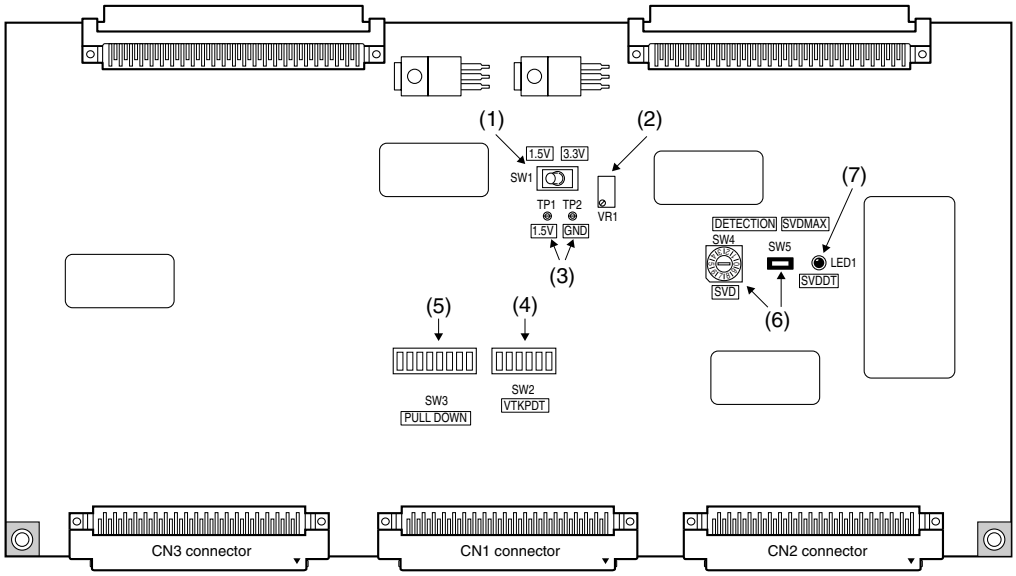
This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.





A.1.2 S5U1C63709P2

The S5U1C63709P2 board provides the functions of the S1C63709 motor and solar control circuits. The following explains the names and functions of each part of the S5U1C63709P2 board.



(1) Power supply voltage select switch (SW1)

This switch is used to select 1.5 V or 3.3 V for the motor and solar power supply voltage. Note that the power supply voltage of other internal circuits and the port interface voltage are fixed at 3.3 V.

Note: Be sure to turn all the connected equipment off before switching the power supply voltage using SW1.

(2) 1.5 V power supply voltage adjustment control (VR1)

This control is used to adjust the 1.5 V power supply voltage. Do not set any voltage level other than 1.5 V for this power supply voltage.

(3) 1.5 V power supply voltage monitor pins (TP1, TP2)

TP1 and TP2 are the 1.5 V monitor pin and GND pin, respectively. Use these pins when adjusting the 1.5 V power supply voltage using the VR1 control.

(4) VTKP voltage detection select switch (SW2)

This jumper switch selects a signal used as the VTKP pin voltage detection results (VTKPDT). The signal for which a jumper is installed is selected. Be sure to select one signal, and do not install two or more jumpers. Table A.1.2.1 shows the relationship between the jumper switch and the signal.

Table A.1.2.1 SW2 setting

Jumper pin No.	Signal used as VTKPDT
1–12	QUISMP (quick start negation)
2–11	QLSMP (quick start negation + limiter ON)
3–10	LIMSMP (limiter ON)
4–9	EXVTKPDT (external input)
5–8	Fixed at HIGH
6–7	Fixed at LOW

This tool cannot generate the VTKP detection result signal (VTKPDT) used in the actual IC. Therefore, the detection result judgment timing signals, QUISMP (quick start negation voltage detection timing), QLSMP (quick start negation and limiter ON voltage detection timing), and LIMSMP (limiter ON voltage detection timing), can be used as a substitute for the actual VTKPDT signal.

In the actual IC, the VTKPDT signal goes high while the judgment timing signal is high when a predefined or higher voltage is detected, or the VTKPDT signal goes low when less than the predefined voltage is detected. In other words, selecting "QUISMP" or "Fixed at HIGH" makes a condition in which the quick start negation voltage or more has been detected from the VTKP pin. The QLSMP and LIMSMP signals can also be used like this. Furthermore, this tool allows input of an external signal equivalent to the VTKPDT to simulate the detection results. Select "EXVTKPDT (external input)" when using this function. In this case, generate a detection result signal using the QUISMP, QLSMP and LIMSMP signals above that are output from Pins 25 to 27 in the CN1-1 connector, and input it to Pin 24 in the CN1-1 connector (see Table A.2.1).

(5) K0 port pull-down resistor select switch (SW3)

This jumper switch is used to select whether a pull-down resistor is attached to the K00–K03 ports individually or not. When a jumper is installed, a pull-down resistor is attached to the corresponding port; when the jumper is removed, no pull-down resistor is attached to the corresponding port. Table A.1.2.2 shows the relationship between the jumper pin and the input port.

Table A.1.2.2 SW3 setting

Jumper pin No.	Input port
1–16	K00
2–15	K01
3–14	K02
4–13	K03
5–12	– (On)
6–11	– (On)
7–10	– (On)
8–9	– (On)

Note: When using the S5U1C63709P2, setting of this switch is effective to select K00–K03 port pull-down resistors and the mask option data for this selection is ignored.
Although the K20–K23 names are printed on the board, the switches are not used. The K20–K23 port pull-down resistors are configured with the mask option data.

(6) Power supply voltage level select switch for SVD (SW4, SW5)

These switches are used to select a power supply voltage level for evaluating the SVD function. Table A.1.2.3 shows the relationship between the switch position and the SVD control registers. Note that these switches do not change the actual power supply voltage. The switches are intended to be used only for changing the detection results to debug whether the SVD routine works normally or not.

Table A.1.2.3 Relationship between SW4/SW5 set position and SVD control registers

Switch position		Setting	SVDCHG
SW4	SW5		
0	DETECTION	Voltage level < (SVDS = 0)	0
1	DETECTION	(SVDS = 0) < Voltage level < (SVDS = 1)	0
2	DETECTION	(SVDS = 1) < Voltage level < (SVDS = 2)	0
3	DETECTION	(SVDS = 2) < Voltage level < (SVDS = 3)	0
4	DETECTION	(SVDS = 3) < Voltage level < (SVDS = 4)	0
5	DETECTION	(SVDS = 4) < Voltage level < (SVDS = 5)	0
6	DETECTION	(SVDS = 5) < Voltage level < (SVDS = 6)	0
7	DETECTION	(SVDS = 6) < Voltage level < (SVDS = 7)	0
8	DETECTION	Voltage level < (SVDS = 0)	1
9	DETECTION	(SVDS = 0) < Voltage level < (SVDS = 1)	1
A	DETECTION	(SVDS = 1) < Voltage level < (SVDS = 2)	1
B	DETECTION	(SVDS = 2) < Voltage level < (SVDS = 3)	1
C	DETECTION	(SVDS = 3) < Voltage level < (SVDS = 4)	1
D	DETECTION	(SVDS = 4) < Voltage level < (SVDS = 5)	1
E	DETECTION	(SVDS = 5) < Voltage level < (SVDS = 6)	1
F	DETECTION	(SVDS = 6) < Voltage level < (SVDS = 7)	1
×	SVDMAX	(SVDS = ×) < Voltage level	×

Setting SW5 to the "SVDMAX" position emulates the maximum voltage level. The SVD results (SVDDT) is always set to "0" no matter how SW4 is set.

(7) SVD result LED (LED1)

This LED indicates the SVD results according to the SW4 settings. The LED lights when the voltage level set using SW4 is lower than the level set using the SVDS register (SVDDT = "1").
The set value of SW4 is always compared with the SVDS register value regardless of the SVDON register setting. Therefore, this LED lights/goes off according to the set status of SW4 and the SVDS register even if SVDON is set to "0". Read the SVDDT register to obtain the actual SVDDT value.

A.2 Connecting to the Target System

This section explains how to connect the S5U1C63000P1 to the target system.
First insert the S5U1C63000P1 board into the second upper slot of the ICE and the S5U1C63709P2 board into the top slot.
Download the circuit data to the S5U1C63000P1 board before installing the S5U1C63709P2 board if the S5U1C63000P1 board does not include the correct circuit data. See Section A.3 for downloading circuit data.

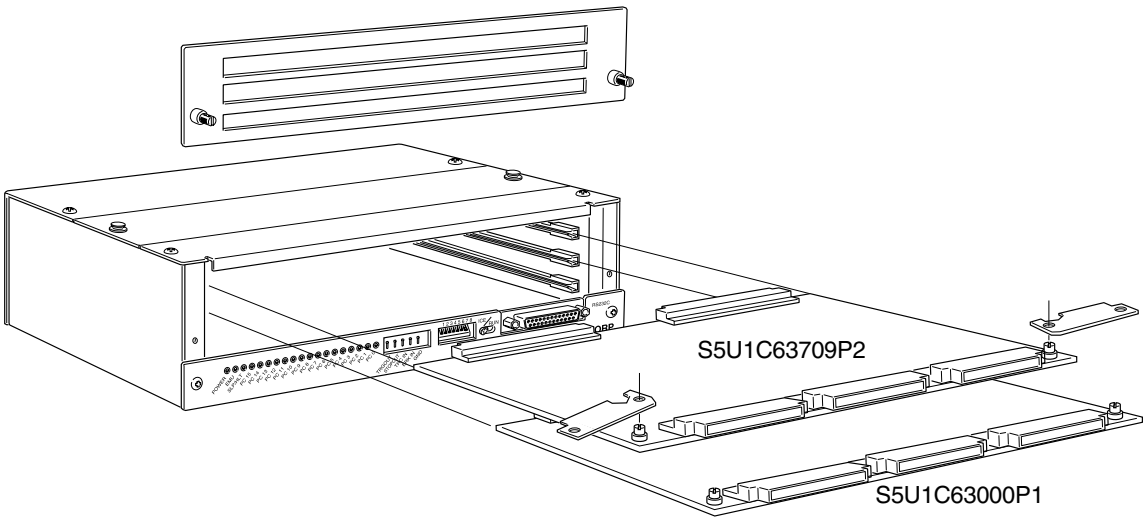


Fig. A.2.1 Installing the peripheral circuit boards to the ICE

- **Installing the S5U1C63000P1/63709P2 board**

  Set the jig included with the ICE into position as shown in Figure A.2.2. Using this jig as a lever, push it toward the inside of the board evenly on the left and right sides. After confirming that the board has been firmly fitted into the internal slot of the ICE, remove the jig.

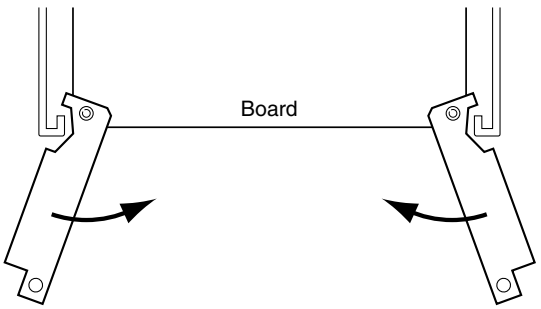


Fig. A.2.2
Installing the board

- **Dismounting the S5U1C63000P1/63709P2 board**

  Set the jig included with the ICE into position as shown in Figure A.2.3. Using this jig as a lever, push it toward the outside of the board evenly on the left and right sides. After confirming that the board has been dismounted from the backboard connector, pull the board out of the ICE.

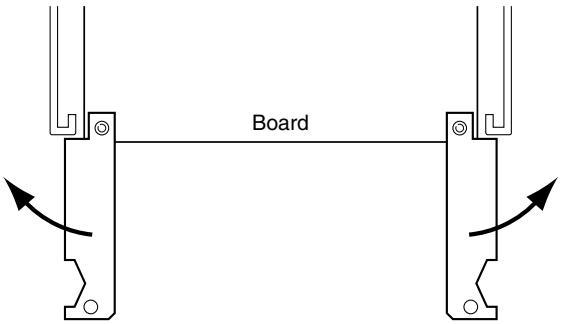


Fig. A.2.3
Dismounting the board

Connect the S5U1C63000P1, S5U1C63709P2 and target board as follows:

(1) Connecting between S5U1C63709P2's CN3 and S5U1C63000P1's CN3
Connect these connectors using the I/O cable (80-pin to 80-pin) supplied with the S5U1C63709P2.

(2) Connecting between S5U1C63709P2's CN2 and S5U1C63000P1's CN1
Connect these connectors using the I/O cable (80-pin to 80-pin) supplied with the S5U1C63709P2.

(3) Connecting between S5U1C63709P2's CN1 and target board
Connect the S5U1C63709P2 and the target board using the I/O cable (80-pin × 1 to 40-pin × 2) supplied with the S5U1C63709P2. Take care when handling the connectors, since they have power supply pins (3.3 V and 1.5 V).

(4) Connecting between S5U1C63000P1's CN2 and target board
Connect the S5U1C63000P1 and the target board using the I/O cable (100-pin × 1 to 50-pin × 2) supplied with the S5U1C63000P1. The CN2 connector is used when the SEG pins are set for DC output by mask option. Take care when handling the connectors, since they have power supply pins (3.3 V).

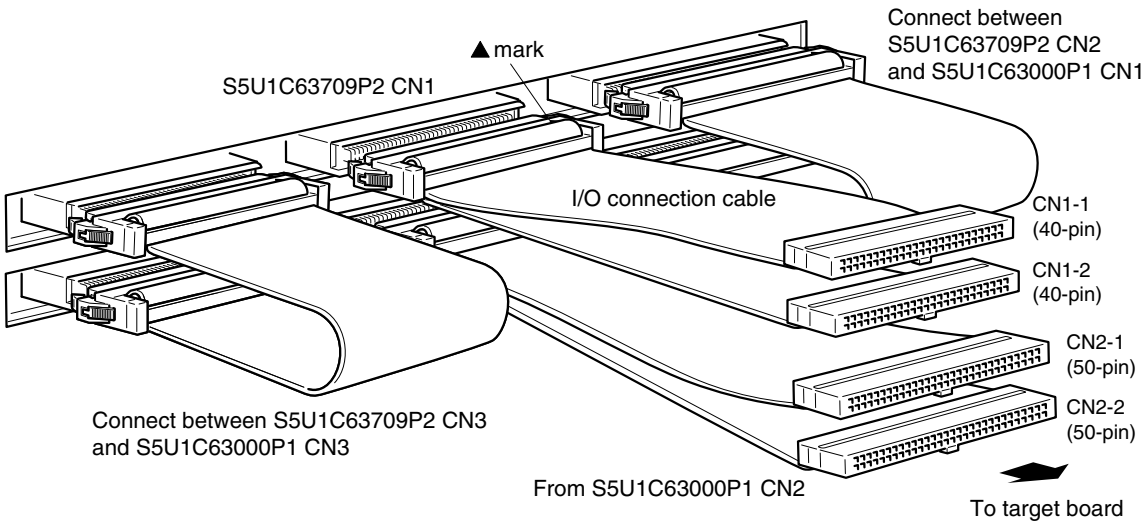


Fig. A.2.4 Connecting to the target system

Table A.2.1 I/O connector (CN1) pin assignment

40-pin CN1-1 connector		40-pin CN1-2 connector	
No.	Pin name	No.	Pin name
1	K00 (IN)	1	P00 (I/O)
2	K01 (IN)	2	P01 (I/O)
3	K02 (IN)	3	P02 (I/O)
4	K03 (IN)	4	P03 (I/O)
5	K10 (IN)	5	P10 (I/O)
6	K11 (IN)	6	P11 (I/O)
7	K12 (IN)	7	P12 (I/O)
8	K13 (IN)	8	P13 (I/O)
9	Vss	9	Vss
10	Vss	10	Vss
11	Cannot be connected	11	P20 (I/O)
12	Cannot be connected	12	P21 (I/O)
13	Cannot be connected	13	P22 (I/O)
14	Cannot be connected	14	P23 (I/O)
15	K20 (IN)	15	P30 (I/O)
16	K21 (IN)	16	P31 (I/O)
17	K22 (IN)	17	P32 (I/O)
18	K23 (IN)	18	P33 (I/O)
19	K30 (IN)	19	P40 (I/O)
20	Cannot be connected	20	P41 (I/O)
21	Vss	21	Vss
22	Vss	22	Vss
23	OSD *1 (IN)	23	O01 (OUT)
24	EXVTKPDT *2 (IN)	24	O02 (OUT)
25	QLSMP *3 (OUT)	25	Cannot be connected
26	QUISMP *3 (OUT)	26	Cannot be connected
27	LIMSMP *3 (OUT)	27	O11 (OUT)
28	TEST (IN)	28	O12 (OUT)
29	RESET (IN)	29	Cannot be connected
30	Cannot be connected	30	Cannot be connected
31	Vss	31	Vss
32	Vss	32	Vss
33	Cannot be connected	33	SLRA (IN)
34	Cannot be connected	34	SLRC (IN)
35	Cannot be connected	35	Cannot be connected
36	Cannot be connected	36	Cannot be connected
37	3.3 V	37	1.5 V
38	3.3 V	38	1.5 V
39	3.3 V	39	1.5 V
40	3.3 V	40	1.5 V

3.3 V signals | 1.5 V signals

∗1: The OSD pin (Pin 23 in CN1-1) is used for evaluating the oscillation stoppage detection function. By setting this pin to "1" (high), the oscillation stoppage detection signal is asserted to activate the internal reset function.

∗2: The EXVTKPDT pin (Pin 24 in CN1-1) is used to input a VTKP sampling signal when "EXVTKPDT (external input)" is selected using SW2. (See description for SW2.)

∗3: The QLSMP, QUISMP and LIMSMP pins (Pins 25–27 in CN1-1) are used to monitor the internal signals for VTKP sampling that can be selected using SW2. (See description for SW2.)

Note: The motor and solar interface voltage is set to 1.5 V at shipment of the S5U1C63709P2 (for 1.5 V signals in the table). This voltage level can be changed to 3.3 V using SW1.

Table A.2.2 I/O connector (CN2) pin assignment

50-pin CN2-1 connector		50-pin CN2-2 connector	
No.	Pin name	No.	Pin name
1	VDD (=3.3 V)	1	VDD (=3.3 V)
2	VDD (=3.3 V)	2	VDD (=3.3 V)
3	SEG0 (DC)	3	SEG40 (DC)
4	SEG1 (DC)	4	SEG41 (DC)
5	SEG2 (DC)	5	SEG42 (DC)
6	SEG3 (DC)	6	SEG43 (DC)
7	SEG4 (DC)	7	SEG44 (DC)
8	SEG5 (DC)	8	SEG45 (DC)
9	SEG6 (DC)	9	SEG46 (DC)
10	SEG7 (DC)	10	SEG47 (DC)
11	VSS	11	VSS
12	VSS	12	VSS
13	SEG8 (DC)	13	SEG48 (DC)
14	SEG9 (DC)	14	SEG49 (DC)
15	SEG10 (DC)	15	SEG50 (DC)
16	SEG11 (DC)	16	SEG51 (DC)
17	SEG12 (DC)	17	SEG52 (DC)
18	SEG13 (DC)	18	SEG53 (DC)
19	SEG14 (DC)	19	SEG54 (DC)
20	SEG15 (DC)	20	SEG55 (DC)
21	VDD (=3.3 V)	21	VDD (=3.3 V)
22	VDD (=3.3 V)	22	VDD (=3.3 V)
23	SEG16 (DC)	23	SEG56 (DC)
24	SEG17 (DC)	24	SEG57 (DC)
25	SEG18 (DC)	25	SEG58 (DC)
26	SEG19 (DC)	26	SEG59 (DC)
27	SEG20 (DC)	27	SEG60 (DC)
28	SEG21 (DC)	28	SEG61 (DC)
29	SEG22 (DC)	29	SEG62 (DC)
30	SEG23 (DC)	30	SEG63 (DC)
31	VSS	31	VSS
32	VSS	32	VSS
33	SEG24 (DC)	33	Cannot be connected
34	SEG25 (DC)	34	Cannot be connected
35	SEG26 (DC)	35	Cannot be connected
36	SEG27 (DC)	36	Cannot be connected
37	SEG28 (DC)	37	Cannot be connected
38	SEG29 (DC)	38	Cannot be connected
39	SEG30 (DC)	39	Cannot be connected
40	SEG31 (DC)	40	Cannot be connected
41	VDD (=3.3 V)	41	VDD (=3.3 V)
42	VDD (=3.3 V)	42	VDD (=3.3 V)
43	SEG32 (DC)	43	Cannot be connected
44	SEG33 (DC)	44	Cannot be connected
45	SEG34 (DC)	45	Cannot be connected
46	SEG35 (DC)	46	Cannot be connected
47	SEG36 (DC)	47	Cannot be connected
48	SEG37 (DC)	48	Cannot be connected
49	SEG38 (DC)	49	Cannot be connected
50	SEG39 (DC)	50	Cannot be connected

∗ Connectors CN2-1 and CN2-2 are used when the SEG pins are set for DC output by mask option.

A.3 Downloading to S5U1C63000P1

A.3.1 Downloading Circuit Data 1 – when new ICE (S5U1C63000H2) is used

The S5U1C63000P1 board comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

1) Remove the ICE top cover and then set the jumper switches on the S5U1C63000P1 board as follows:
   CLK: "32K" position
   PRG: "Prog" position
   IOSEL2: "E" position
2) Connect the ICE to the host PC. Then turn the host PC and ICE on.
3) Invoke the debugger included in the assembler package (ver. 5 or later). For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
4) Download the circuit data file (.mot) corresponding to the model by entering the following commands in the command window.

`>XFER`		(erase all main-FPGA)
`>XFWR`	<*file name 1*>	(download the main-FPGA file)*
`>XFCP`	<*file name 1*>	(compare the main-FPGA file and downloaded data)
`>XFERS`		(erase all sub-FPGA)
`>XFWRS`	<*file name 2*>	(download the sub-FPGA file)*
`>XFCPS`	<*file name 2*>	(compare the sub-FPGA file and downloaded data)

   * The downloading takes about 15 minutes.

Note: The files must be downloaded from the main-FPGA file first then the sub-FPGA file.

5) Terminate the debugger and then turn the ICE off.
6) Set the jumper switches on the S5U1C63000P1 board as follows:
   CLK: "LCLK" position
   PRG: "Norm" position
   IOSEL2: "D" position
7) Turn the ICE on and invoke the debugger again. Debugging can be started here.

A.3.2 Downloading Circuit Data 2 – when previous ICE (S5U1C63000H1) is used

The standard ICE (S5U1C63000H1, previous model) did not support the circuit data download function for this board. To use the download function, update the ICE firmware according to the following procedure.

1) Set the baud rate of the ICE to 9600 bps. Refer to the manual supplied with the ICE for setting the DIP switch.
2) Connect the ICE to the host PC and then start up the host PC in DOS. When Windows is running, restart in DOS mode.

   Note: Do not use the DOS prompt of Windows.
3) Turn the ICE on.
4) Configure the RS232C parameters for the host PC as follows:

   `C:\>MODE COM1:9600,n,8,1,p` (9600 bps, 8-bit data, 1 stop bit, no parity)
5) Copy the following files included in the assembler package (ver. 5 or later) to a directory on the hard disk.

   `tm63.exe, ice63.com, i63com.o, i63par`
6) Move to the directory in Step 5, run the TM63. TM63 enters command ready status after invocation, enter a command as follows:

```
C:\>tm63 xat↵
TM63 start on IBM PC
TM63 start V01.01
>dlf ice63.com i63com.o i63par 0b↵
                ...
>q↵
```

7) Enter "q" to terminate TM63 after the prompt mark is displayed.
8) The ICE firmware is now updated. Turn the ICE off and then download the circuit data by the procedure described in Section A.3.1.

A.4 Usage Precautions

To ensure correct use of the peripheral circuit board, please observe the following precautions.

A.4.1 Operational precautions

(1) Before inserting or removing cables, turn off power to all pieces of connected equipment.
(2) Do not turn on power or load mask option data if all of the input ports (K00–K03) are held low. Doing so may activate the multiple key entry reset function.
(3) Before debugging, always be sure to load mask option data.

A.4.2 Differences with the actual IC

(1) Differences in I/O

<Interface power supply>

- S5U1C63709P2 and target system interface voltage (except for motor and solar) is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter circuit, etc. on the target system side to accommodate the required interface voltage.
- The motor and solar interface voltage is set to +1.5 V at shipment of the S5U1C63709P2. This voltage level can be changed to +3.3 V using SW1.

<Each output port's drive capability>

The drive capability of each output port on S5U1C63000P1 is higher than that of the actual IC. When designing application system and software, refer to Chapter 7, "Electrical Characteristics", to confirm each output port's drive capability.

<Each port's protective diode>

All I/O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between S5U1C63000P1 and the target system are set to +3.3 V. Therefore, S5U1C63000P1 and the target system cannot be interfaced with voltages exceeding V_{DD} by setting the output ports for open-drain mode.

<Pull-down resistance value>

The pull-down resistance values on S5U1C63000P1 and S5U1C63709P2 are set to 220 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "Electrical Characteristics".
Note that when using pull-down resistors to pull the input pins low, the input pins may require a certain period to reach a valid low level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since fall delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by the peripheral circuit boards differ significantly from that of the actual IC. Inspecting the LEDs on S5U1C63000P1 may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

<Those which can be verified by LEDs and monitor pins>

a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
b) OSC3 oscillation on/off circuit (OSCC)
c) CPU clock select circuit (CLKCHG)
d) SVD circuit on/off circuit (SVDON)
e) LCD power supply on/off circuit (LPWR)
f) Heavy load protection circuit on/off status (HVLDON, HVLD)

<Those that can only be counteracted by system or software>

g) Current consumed by the internal pull-down resistors
h) Input ports in a floating state

(3) Functional precautions

<LCD power supply circuit>

There is a finite delay time from the point at which the LCD power supply circuit (LPWR) turns on until an LCD drive waveform is output. On this board, this delay is set to approx. 125 msec, which differs from that of the actual IC. Refer to Section 4.6, "LCD Driver (COM0–COM7, SEG0–SEG63)".

<Differences in LCD drive waveform>

This board is capable of static waveform output even if the internal LCD power supply is used. However, select 1/2-bias external power supply by mask option when driving the LCD with the static waveform.

<SVD circuit>

- The SVD function is realized by artificially varying the power supply voltage level using the SW4 switch on the S5U1C63709P2.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. On S5U1C63000P1, this delay time is 1.007 msec to 1.038 msec, which differs from that of the actual IC. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.

<Oscillation circuit>

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. On S5U1C63000P1, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to Chapter 7, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with S5U1C63000P1, may not function properly well with the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on S5U1C63000P1 differs from that of the actual IC.
- S5U1C63000P1 contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, its emulator can operate with the OSC3 circuit.
- S5U1C63000P1 generates the OSC3 clock using the onboard CR oscillation circuit even if ceramic oscillation is selected for the OSC3 oscillation circuit by mask option.

<Solar pins (SLRA, SLRC)>

The SLRA and SLRC pins in the I/O connector that are used to connect the solar panel in the actual IC are used to simulate recharging status by applying a voltage in the S5U1C63709P2 board. Furthermore, the actual IC uses voltage levels on these pins to activate the quick start function and the limiter function. The S5U1C63709P2 board simulates these functions using the signal selected by the VTKP voltage detection select switch (SW2). (See description for SW2.)

Recharging detection

To simulate the status in which the secondary cell is being recharged, set the SLRC pin to V_{SS} and the SLRA pin to V_{DD} + 0.5 V. This sets the recharging flag (ISOR1) to "1". Furthermore, a solar wakeup interrupt is generated.

To simulate the status in which the secondary cell is not being recharged, set both the SLRC and SLRA pins to V_{DD}. This resets the recharging flag (ISOR1) to "0". In this case, a solar wakeup interrupt is not generated.

Controlling detection of limiter ON voltage

The S5U1C63709P2 board allows start/stop sampling for limiter ON voltage detection by setting the SLRC pin voltage level.

To start sampling for limiter ON voltage detection, set the SLRC pin to VSS. The sampling function is controlled by the SLRC pin voltage only, the SLRA pin can be set to either VDD or VSS levels. This setting outputs the LIMSMP signal (the signal is enabled during sampling). Furthermore, the QLSMP signal will be asserted during the sampling period by the LIMSMP signal as well as the sampling period by the QUISMP signal.

To stop sampling for limiter ON voltage detection, set the SLRC pin to VDD. The LIMSMP signal is disabled (fixed at low). The QLSMP signal is asserted only during the sampling period by the QUISMP signal.

The VDD level described above is the motor - solar interface voltage value in the I/O connector (Pins 37 to 40 in CN1-2).

<Motor connection pins>

The O01 to O12 pins in the I/O connector are used to connect motors.
These pins are used for magnetic field detection and rotation detection the same as the actual IC.

<Access to undefined address space>

If any undefined space in the S1C63709's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between S5U1C63000P1 and the actual IC. Note that the ICE (S5U1C63000H1/S5U1C63000H2) incorporates the program break function caused by accessing to an undefined address space.

<Reset circuit>

Keep in mind that the operation sequence from when the ICE and the peripheral circuit boards are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because S5U1C63000P1 becomes capable of operating as a debugging system after the user program and optional data are down-loaded. When operating the ICE after placing it in free-running mode, always apply a system reset. A system reset can be performed by pressing the reset switch on S5U1C63000P1, by a reset pin input, or by holding the input ports high simultaneously.

A.5 Product Specifications

A.5.1 Specifications of S5U1C63000P1

S5U1C63000P1

Dimension:	254 mm (wide) × 144.8 mm (depth) × 13 mm (height)	(including screws)
Weight:	Approx. 300 g	
Power supply:	DC 5 V ± 5%, less than 1 A	(supplied from ICE main unit)

I/O connection cable (80-pin)

S5U1C63000P1 connector:	KEL8830E-080-170L	
Cable connector (80-pin):	KEL8822E-080-171	
Cable connector (40-pin):	3M7940-6500SC	1 pair
Cable:	40-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

I/O connection cable (100-pin)

S5U1C63000P1 connector:	KEL8830E-100-170L	
Cable connector (100-pin):	KEL8822E-100-171	
Cable connector (50-pin):	3M7950-6500SC	1 pair
Cable:	50-pin flat cable	1 pair
Interface:	CMOS interface (3.3 V)	
Length:	Approx. 40 cm	

Accessories

40-pin connector for connecting to target system:
3M3432-6002LCSC × 2
50-pin connector for connecting to target system:
3M3433-6002LCSC × 2

A.5.2 Specifications of S5U1C63709P2

S5U1C63709P2

Dimension:	254 mm (width) × 144.8 mm (depth) × 13 mm (height)	(including screws)
Weight:	Approx. 130 g	
Power supply:	DC 5 V ± 5%, less than 15 mA (supplied from ICE main unit and converted into 3.3 V by the onboard regulator)	

Target connection cable (80-pin)

Connector (80-pin):	KEL8822E-080-171-F	
Connector (40-pin):	3M7940-6500SC	1 pair
Cable:	40-pin flat cable	1 pair
Length:	Approx. 20 cm	

S5U1C63000P1 connection cable (80-pin)

Connector (80-pin):	KEL8822E-080-171-F
Cable:	80-pin flat cable
Length:	Approx. 10 cm

Accessories

40-pin connector for connecting to target system:
3M3432-6002LCPL × 2

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