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124-OUTPUT EPD DRIVER

S1C05112

Technical Manual

SEIKO EPSON CORPORATION

S1C05112 Revision History

Code No.	Page	Chapter/Section	Contents
411004401 (8. 2007)	4	3.1 Pad Layout	Figure 3.1.1 was modified.
	7	4.2 MPU Interface Block	Figures 4.2.1 and 4.2.2 were modified.
	16	6.5 Interface AC Characteristics	The figures (Interface AC characteristic, Recommended timing) were modified.
411004402 (10. 2008)	15	6.4 Analog Circuit Characteristics and Power Current Consumption	The DC-DC converter current consumption (MV_{DD}) - DCK frequency characteristic graph was modified.

CONTENTS

1 Overview

The S1C05112 is the EPD (Electrophoretic Display) driver IC designed specifically for EPD panels.
The IC consists of an external MPU interface block, a DC-DC converter block, and an EPD driver block. It outputs the EPD drive voltage from any EPD drive pin by supplying an external 3-V DC voltage and sending display data and control signals to the IC.
A low-power EPD controller system can be configured by the S1C05112 with the S1C63808 (4-bit single chip microcomputer) and is suitable for battery driven applications such as clocks, watches and price tags.

1.1 Features

The main functions and features of the S1C05112 are outlined below.

MPU interface block

The MPU interface block inputs the control signals, data and clocks shown below.

Driver control signals	XCS:	Chip select signal
	SCK:	Clock for data shift register operation
	SDAT[3:0]:	4-bit data
	SEN:	Driver output trigger signal
IC power control signals	LO_ACT:	Power control (active-standby switch) signal for the logic blocks (MPU interface block and low-voltage driver block)
	DD_ACT:	Power control (active-standby switch) signal for the DC-DC converter block
Clock for the DC-DC converter	DCK:	512-Hz clock (recommended)

DC-DC converter block

The DC-DC converter performs sextuple boosting to generate an 18-V EPD drive voltage from the 3-V supply voltage (MV_{DD}) and outputs the boosted voltage from the VSC pin.
The DC-DC converter requires 10 capacitors for boosting voltage and provides 20 pins (C00P–C04P, C00N–C04N, C10P–C14P, and C10N–C14N) for connecting external voltage-boost capacitors.
Supply a voltage-boost clock from the MPU or other controller to the DCK pin to drive the DC-DC converter.

EPD driver block

The EPD driver block outputs the drive voltage to any EPD drive pin (EO0–EO123) according to the input data.
The EPD drive pins have three output states: H (high), L (low) and Hi-Z (high impedance).

Power supply voltage

Power supply voltage for DC-DC converter (MV_{DD}): 2.1 V to 3.6 V
Power supply voltage for MPU interface (LV_{DD}): 1.0 V to 3.6 V

Current consumption

Typical MV_{DD} current consumption when EPD (10 MΩ load resistance) is being driven: 15 µA
Typical MV_{DD} current consumption when no EPD is driven (no load): 5 µA
Typical LV_{DD} current consumption when display data is being input (SCK frequency = 50 kHz): 13 µA
Typical current consumption in standby state: 0.1 µA or less

Shipment form

Die

1.2 Characteristic Overview

Table 1.2.1 Characteristic Overview

Item		Specification			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage		2.1		3.6	V	LV_{DD} = MV_{DD} when a single power supply is used ∗1
LV_{DD}		1.0		3.6	V	For MPU interface block ∗2
MV_{DD}		2.1		3.6	V	For DC-DC converter and its controller block ∗2
Maximum voltage rating		-0.5		4.5	V	LV_{DD}, MV_{DD} ∗2
Current consumption (LV_{DD})	Standby state			0.1	µA	When all circuit blocks are in standby state (LV_{DD} = 3 V)
	During display data input		13	16.3	µA	SCK frequency = 50 kHz (LV_{DD} = 3 V) Depends on the operating frequency
Current consumption (MV_{DD})	When no EPD is driven		5	7.5	µA	No load (MV_{DD} = 3 V)
	When EPD is being driven		15	21	µA	10 MΩ load resistance (EPD leak current is included, MV_{DD} = 3 V)
DC-DC converter (VSC)	Output voltage		18		V	VSC = MV_{DD} × 6 (Depends on MV_{DD} voltage fluctuations) ∗3
	Output current		9		µA	Maximum load resistance: 2 MΩ (Output approx. 18 V)
	Control clock		512		Hz	Recommended frequency
	Voltage-boost capacitors		0.068		µF	0.047 to 0.068 µF are recommended
Number of driver output pads			124		pads	COM outputs can be assigned to any of 124 pads
Pad pitch			85/89		µm	Opening: 68 µm ∗4
Operating temperature range		-20		70	°C	

∗1) Supply a single power voltage (MV_{DD} = LV_{DD}) when an MPU other than S1C63808 is used.
∗2) $MV_{DD} \geq LV_{DD}$, LV_{DD} + 0.3 V ≥ V_{IH1} (high-level input voltage)
∗3) Maximum 0.5 V voltage loss after voltage boosting (at no load)
The DC-DC converter output voltage (VSC) is supplied to the driver (HV_{DD}).
∗4) See Section 3.1, “Pad Layout.”

2 Block Diagram

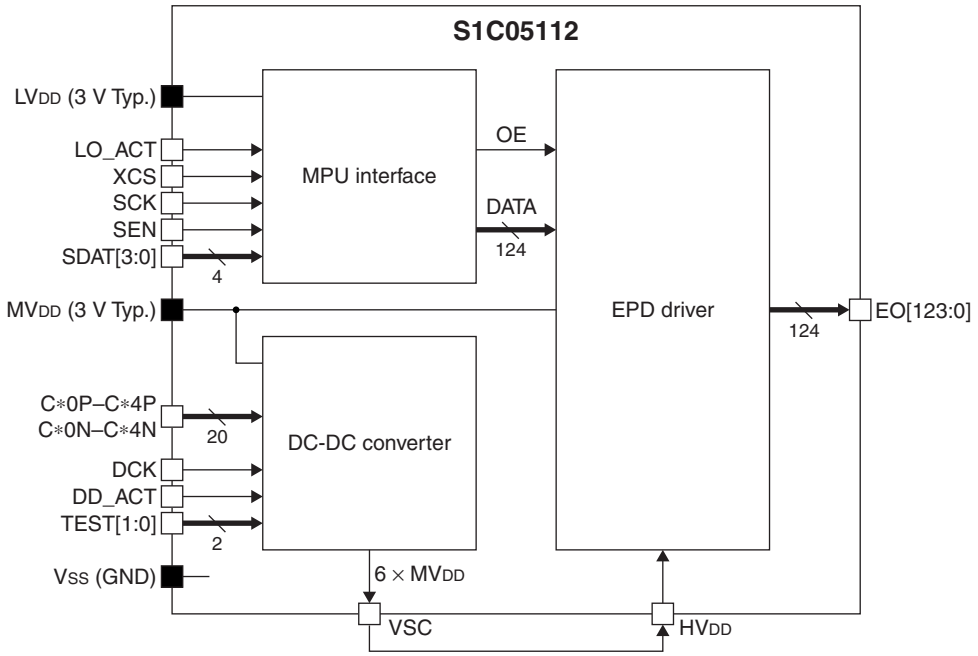


Figure 2.1 Block Diagram

3 Pads

3.1 Pad Layout

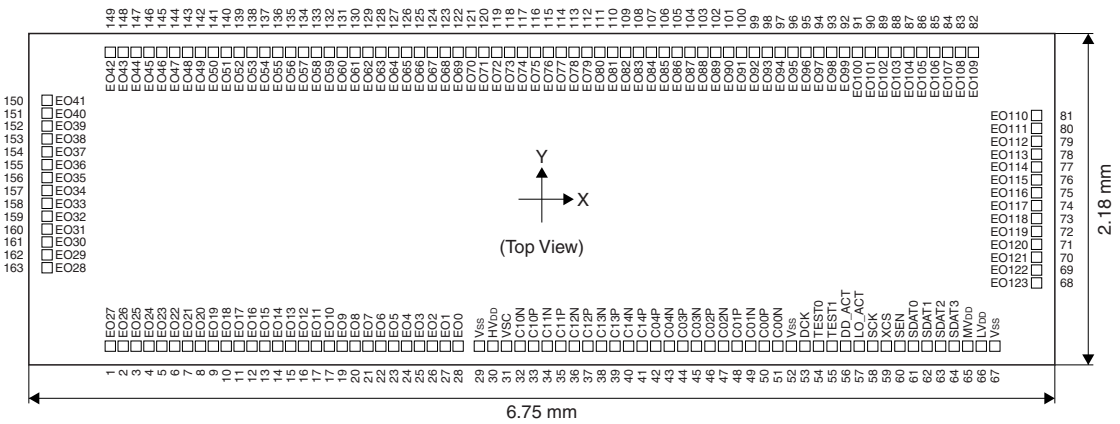


Figure 3.1.1 Pad Layout

Pad pitch 84.75 µm: 1–28, 68–163
89.25 µm: 29–67
Pad opening size 68 µm

3.2 Pin Description

Table 3.2.1 Pin Description

Pin name	Pin No.	I/O	Function
LV_{DD}	66	–	Logic power supply (+) pin (0.9 V to 3.6 V)
V_{SS}	29, 52, 67	–	Power supply (-) pins (0 V)
MV_{DD}	65	–	DC-DC converter power supply (+) pin (2.2 V to 3.6 V)
VSC	31	O	Boosted voltage output pin (18 V Typ.)
HV_{DD}	30	–	Driver power supply (+) pin (18 V Typ.)
LO_ACT	57	I	Logic block (MPU interface block) power control input pin
DD_ACT	56	I	DC-DC converter block power control input pin
DCK	53	I	DC-DC converter clock input pin
TEST0	54	I	TEST pin (Connect to V_{SS}.)
TEST1	55	I	TEST pin (Connect to V_{SS}.)
C00N–C04P	51–42	–	Voltage boost capacitor connect pins (Connect a capacitor between P and N pins.)
C10N–C14P	32–41	–	Voltage boost capacitor connect pins (Connect a capacitor between P and N pins.)
SCK	58	I	MPU interface clock input pin
XCS	59	I	MPU interface chip select input pin
SEN	60	I	MPU interface output enable input pin
SDAT3	64	I	MPU interface data input pins
SDAT2	63	I	
SDAT1	62	I	
SDAT0	61	I	
EO0–EO123	1–28, 68–163	O	EPD output pins (three state outputs; H, L, and Hi-Z)

3.3 Pad Coordinates

Table 3.3.1 Pad Coordinates (unit: µm)

No.	X	Y	No.	X	Y	No.	X	Y	No.	X	Y
1	-2839.125	-966.675	41	660.000	-966.675	82	2839.125	966.675	123	-635.625	966.675
2	-2754.375	-966.675	42	749.250	-966.675	83	2754.375	966.675	124	-720.375	966.675
3	-2669.625	-966.675	43	838.500	-966.675	84	2669.625	966.675	125	-805.125	966.675
4	-2584.875	-966.675	44	927.750	-966.675	85	2584.875	966.675	126	-889.875	966.675
5	-2500.125	-966.675	45	1017.000	-966.675	86	2500.125	966.675	127	-974.625	966.675
6	-2415.375	-966.675	46	1106.250	-966.675	87	2415.375	966.675	128	-1059.375	966.675
7	-2330.625	-966.675	47	1195.500	-966.675	88	2330.625	966.675	129	-1144.125	966.675
8	-2245.875	-966.675	48	1284.750	-966.675	89	2245.875	966.675	130	-1228.875	966.675
9	-2161.125	-966.675	49	1374.000	-966.675	90	2161.125	966.675	131	-1313.625	966.675
10	-2076.375	-966.675	50	1463.250	-966.675	91	2076.375	966.675	132	-1398.375	966.675
11	-1991.625	-966.675	51	1552.500	-966.675	92	1991.625	966.675	133	-1483.125	966.675
12	-1906.875	-966.675	52	1641.750	-966.675	93	1906.875	966.675	134	-1567.875	966.675
13	-1822.125	-966.675	53	1731.000	-966.675	94	1822.125	966.675	135	-1652.625	966.675
14	-1737.375	-966.675	54	1820.250	-966.675	95	1737.375	966.675	136	-1737.375	966.675
15	-1652.625	-966.675	55	1909.500	-966.675	96	1652.625	966.675	137	-1822.125	966.675
16	-1567.875	-966.675	56	1998.750	-966.675	97	1567.875	966.675	138	-1906.875	966.675
17	-1483.125	-966.675	57	2088.000	-966.675	98	1483.125	966.675	139	-1991.625	966.675
18	-1398.375	-966.675	58	2177.250	-966.675	99	1398.375	966.675	140	-2076.375	966.675
19	-1313.625	-966.675	59	2266.500	-966.675	100	1313.625	966.675	141	-2161.125	966.675
20	-1228.875	-966.675	60	2355.750	-966.675	101	1228.875	966.675	142	-2245.875	966.675
21	-1144.125	-966.675	61	2445.000	-966.675	102	1144.125	966.675	143	-2330.625	966.675
22	-1059.375	-966.675	62	2534.250	-966.675	103	1059.375	966.675	144	-2415.375	966.675
23	-974.625	-966.675	63	2623.500	-966.675	104	974.625	966.675	145	-2500.125	966.675
24	-889.875	-966.675	64	2712.750	-966.675	105	889.875	966.675	146	-2584.875	966.675
25	-805.125	-966.675	65	2802.000	-966.675	106	805.125	966.675	147	-2669.625	966.675
26	-720.375	-966.675	66	2891.250	-966.675	107	720.375	966.675	148	-2754.375	966.675
27	-635.625	-966.675	67	2980.500	-966.675	108	635.625	966.675	149	-2839.125	966.675
28	-550.875	-966.675	68	3254.925	-550.875	109	550.875	966.675	150	-3254.925	550.875
29	-411.000	-966.675	69	3254.925	-466.125	110	466.125	966.675	151	-3254.925	466.125
30	-321.750	-966.675	70	3254.925	-381.375	111	381.375	966.675	152	-3254.925	381.375
31	-232.500	-966.675	71	3254.925	-296.625	112	296.625	966.675	153	-3254.925	296.625
32	-143.250	-966.675	72	3254.925	-211.875	113	211.875	966.675	154	-3254.925	211.875
33	-54.000	-966.675	73	3254.925	-127.125	114	127.125	966.675	155	-3254.925	127.125
34	35.250	-966.675	74	3254.925	-42.375	115	42.375	966.675	156	-3254.925	42.375
35	124.500	-966.675	75	3254.925	42.375	116	-42.375	966.675	157	-3254.925	-42.375
36	213.750	-966.675	76	3254.925	127.125	117	-127.125	966.675	158	-3254.925	-127.125
37	303.000	-966.675	77	3254.925	211.875	118	-211.875	966.675	159	-3254.925	-211.875
38	392.250	-966.675	78	3254.925	296.625	119	-296.625	966.675	160	-3254.925	-296.625
39	481.500	-966.675	79	3254.925	381.375	120	-381.375	966.675	161	-3254.925	-381.375
40	570.750	-966.675	80	3254.925	466.125	121	-466.125	966.675	162	-3254.925	-466.125
			81	3254.925	550.875	122	-550.875	966.675	163	-3254.925	-550.875

4 Functional Description

4.1 DC-DC Converter Block

The on-chip DC-DC converter boosts the MVDD power supply voltage (3 V Typ.) to generate the 18 V EPD drive voltage.

DC-DC converter clock

Supply the voltage boost clock for the DC-DC converter to the DCK pin from outside the chip.
Example: When supplying the clock from the S1C63808, the FOUT output clock can be used.

The recommended clock frequency is 512 Hz.

Voltage boost capacitor connect pins

The DC-DC converter provides 20 pins for connecting voltage boost capacitors. Connect a capacitor to each pair of pins listed below.

1) C00N–C00P
2) C01N–C01P
3) C02N–C02P
4) C03N–C03P
5) C04N–C04P
6) C10N–C10P
7) C11N–C11P
8) C12N–C12P
9) C13N–C13P
10) C14N–C14P

The MVDD voltage is output between the pins of each pair.
The DC-DC converter does not allow connection of an element other than capacitor to these pins. Also no capacitor can be connected between the pins other than the above combinations.

VSC output pin

The DC-DC converter outputs the boosted voltage from the VSC pin. Connect this output to the HVDD pin to supply the voltage to the EPD driver block. Be sure to connect between the VSC and HVDD pins outside, as there is no wiring on the chip. Use 0.01 µF (recommended) if a capacitor is connected to the VSC pin (see Chapter 5, “External Wiring Diagram”).
Do not supply power other than the VSC output to the HVDD pin of the EPD driver block.

4.2 MPU Interface Block

The MPU interface inputs display data from the MPU and outputs the drive signals to the EPD driver block.

Input signals

The MPU interface uses seven signals as shown below. These signals are all input from the MPU.

XCS (chip select signal)
When the XCS signal is set to ‘L’ (VSS), the SCK input is enabled and the MPU interface starts the data shift register operation. When the signal is returned to ‘H’ (LVDD), the MPU interface latches input data.

SCK (clock signal)
The SCK clock signal is used for the data shift register operation. The MPU interface samples data input from the SDAT[3:0] pins at the falling edge of the clock.

SDAT[3:0] (4-bit data signals)
The SDAT[3:0] signals are used to input 4-bit parallel data.

SEN (enable signal)
While the SEN signal is set to ‘H’ (LVDD), the latched data is sent to the EPD driver and output from the EO pins.

Interface timing chart

MPU interface timing charts are shown below. See Section 6.5, "Interface AC Characteristics," for details.

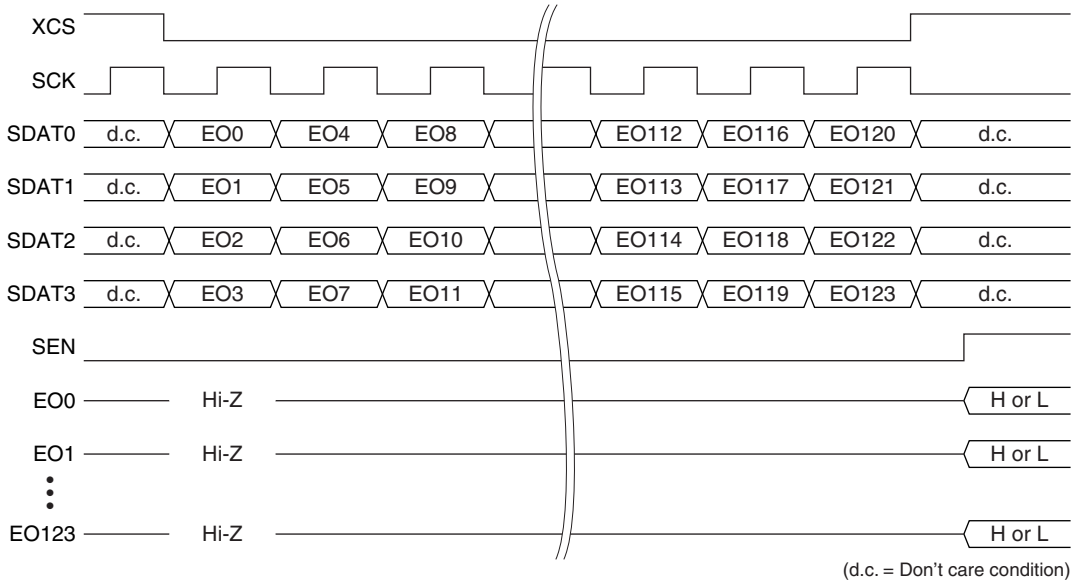


Figure 4.2.1 MPU Interface Timing Chart 1

(1) The MPU interface inputs the XCS, SCK, SDAT[3:0], and SEN signals sent from the MPU in the established timings.
(2) The SDAT signals (4-bit parallel data) are shift registered at the SCK clock edge while the XCS signal is 'L' (V_{SS}).
(3) The MPU interface generates up to 124 output data.
(4) When the MPU negates the XCS signal at an SCK falling edge, the MPU interface latches the data that has been input to that point.
(5) When the MPU asserts the SEN signal, the latched data is sent to the EPD driver and output from the EO pins.

If, for example, the EO112 to EO123 outputs only are required, set the XCS signal to 'L' (V_{SS}) and the SEN signal to 'H' (LV_{DD}) after the EO112–EO115 data has been shift registered. The MPU interface outputs the EO112–EO123 data at that point.

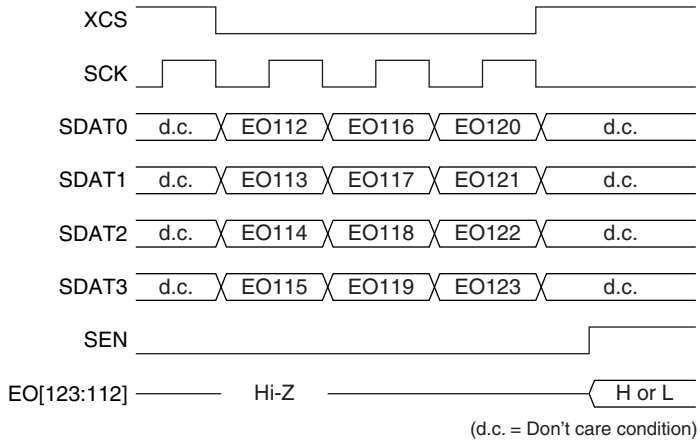


Figure 4.2.2 MPU Interface Timing Chart 2

4.3 EPD Driver Block

The EPD driver outputs the EPD drive signals according to data latched by the MPU interface as described above from the EO pins while the SEN signal is set to 'H' (LV_{DD}). The EO pin goes 'H' (HV_{DD}) when drive data is 1 or 'L' (V_{SS}) when drive data is 0. When the SEN signal is set to 'L' (V_{SS}), all EO pins are placed into high impedance state.

EO output timing chart

Each EO pin outputs 'H' (HV_{DD}) or 'L' (V_{SS}) levels only while the SEN signal is 'H' (LV_{DD}) as shown below.

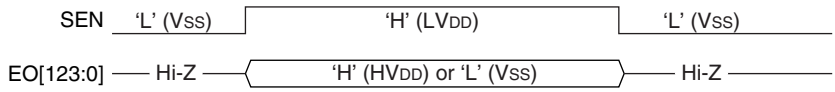


Figure 4.3.1 EO Output Timing Chart

4.4 Power Control (Standby) Function

The S1C05112 has a power control (standby) function for saving power. Two control pins (LO_ACT and DD_ACD) are provided to control the logic power (for MPU interface block and low-voltage driver block) and the DC-DC converter power individually.

Table 4.4.1 Standby Control

LO_ACT pin	DD_ACT pin	Logic power	DC-DC converter power	Display on EPD	Data transfer
H	H	Active	Active	Enabled	Enabled
H	L	Active	Standby	Disabled	Enabled
L	L	Standby	Standby	Disabled	Disabled

(H = LV_{DD}, L = V_{SS})

Note: Do not activate the DC-DC converter when the logic power is in standby state.

Logic power standby state

In this state, the power supply to the logic circuits (MPU interface block and low-voltage driver block) is disabled. The LV_{DD} supply to the circuits other than the input buffers is shut off.

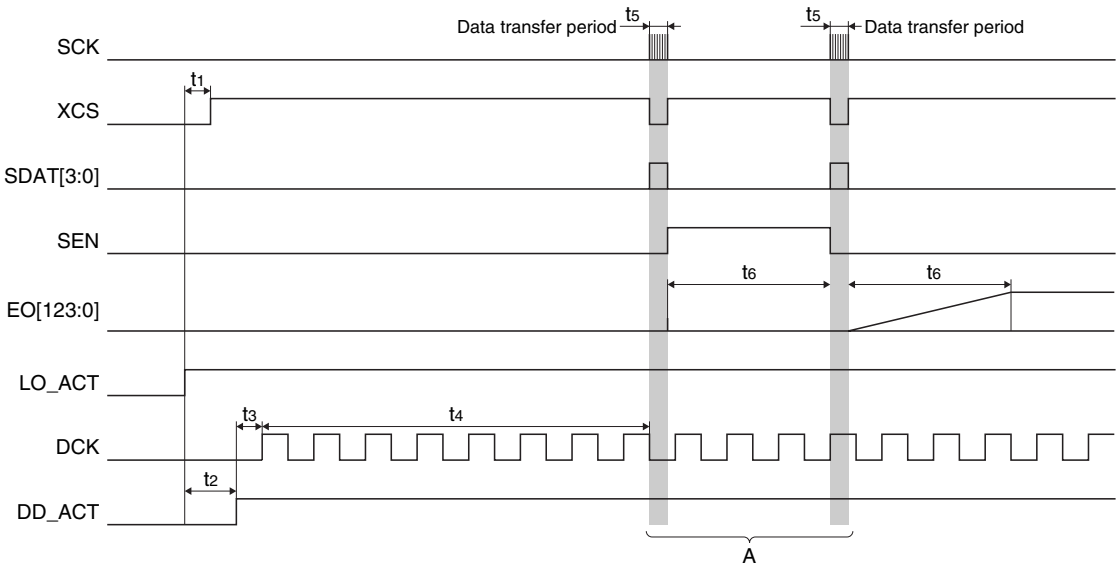
DC-DC converter power standby state

In this states, the MV_{DD} supply to the DC-DC converter is shut off. So the voltage boost operation is stopped.

Note that the power voltage must be supplied to the LV_{DD} pin even if the chip is in the standby state.

4.5 Control Sequence

4.5.1 Startup Sequence from Standby State

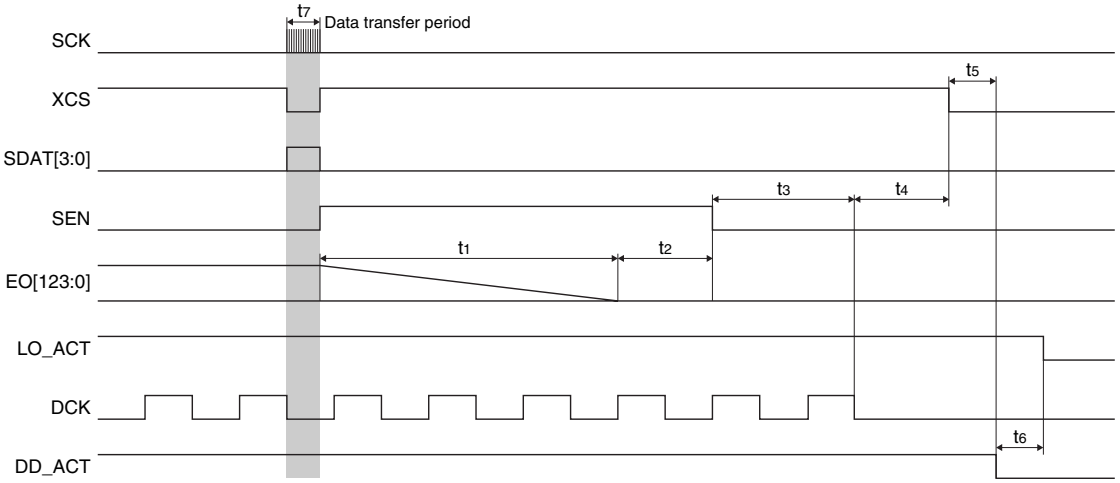


Item	Symbol	Min.	Recommended value	Max.	Unit
XCS Setup time	t_1	0			ns
DC-DC converter power supply start time	t_2	0			ns
DCK input start time	t_3	Half clock period (DCK•1/2)			ns
VSC settling time *1	t_4		15		ms
Data input period *2	t_5	43.33	650	9,750	µs
Driver output settling time *3	t_6		6		ms

*1 Depends on the capacitor connected to the VSC pin.
*2 Depends on the SCK frequency and the number of data.
*3 Depends on the EPD size.

'A' in the timing chart indicates an operation to stabilize the driver lines and EPD voltage level. Set all driver outputs to Vss or VSC level in this period. However, this operation is not absolutely necessary, so it can be omitted. Determine whether the operation is performed or not according to the EPD display condition.

4.5.2 Standby Sequence



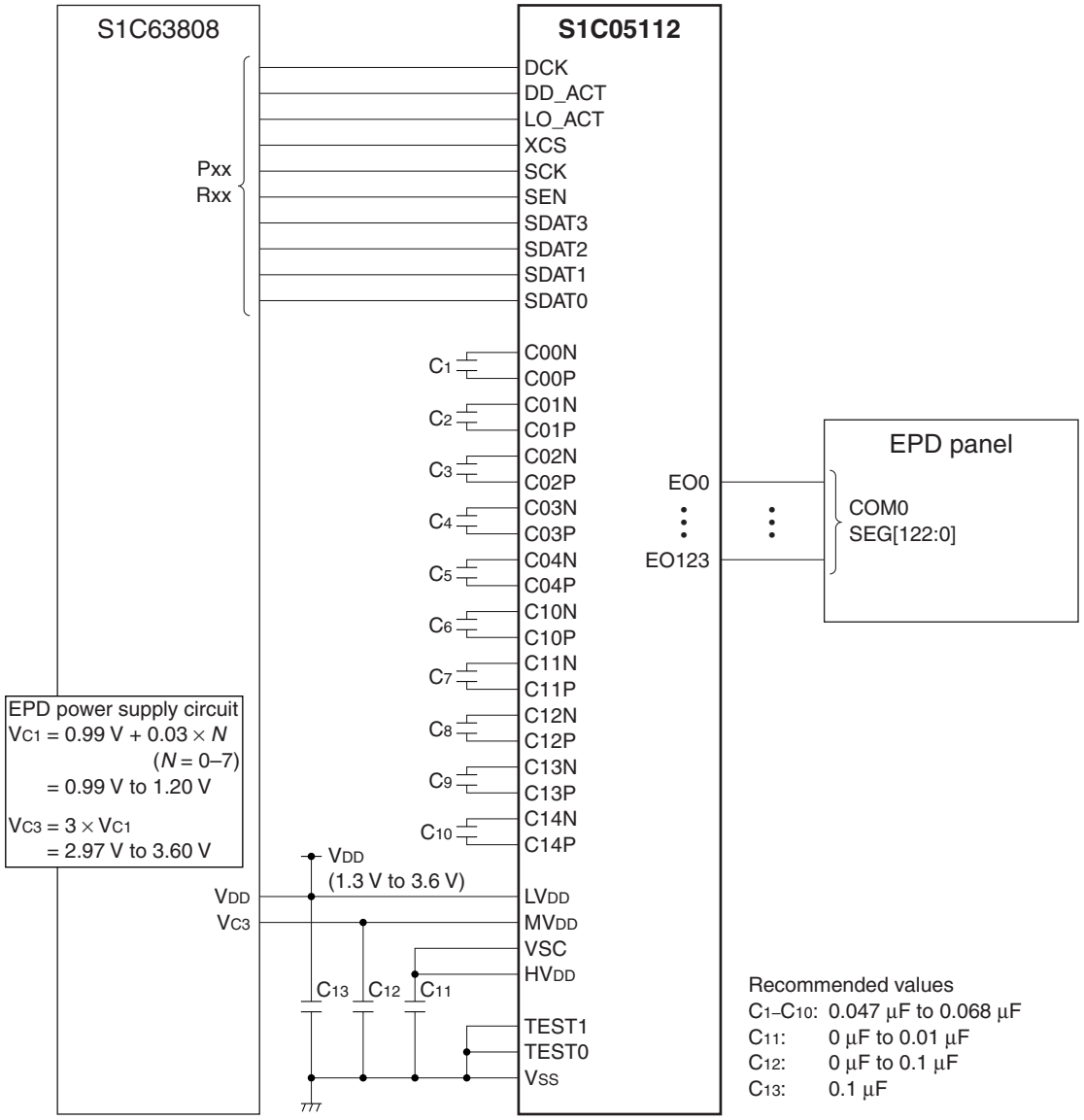
Item	Symbol	Min.	Recommended value	Max.	Unit
Driver output settling time *1	t_1		15		ms
V_{SS} level hold time of all driver outputs	t_2	0			ns
DCK off time	t_3	1			clock
XCS	t_4	600			ns
DD_ACT off time	t_5	0			ns
LO_ACT off time	t_6	0			ns
Data input period *2	t_7	43.33	650	9,750	µs

*1 Depends on the EPD size.
*2 Depends on the SCK frequency and the number of data.

5 External Wiring Diagram

Connection example 1

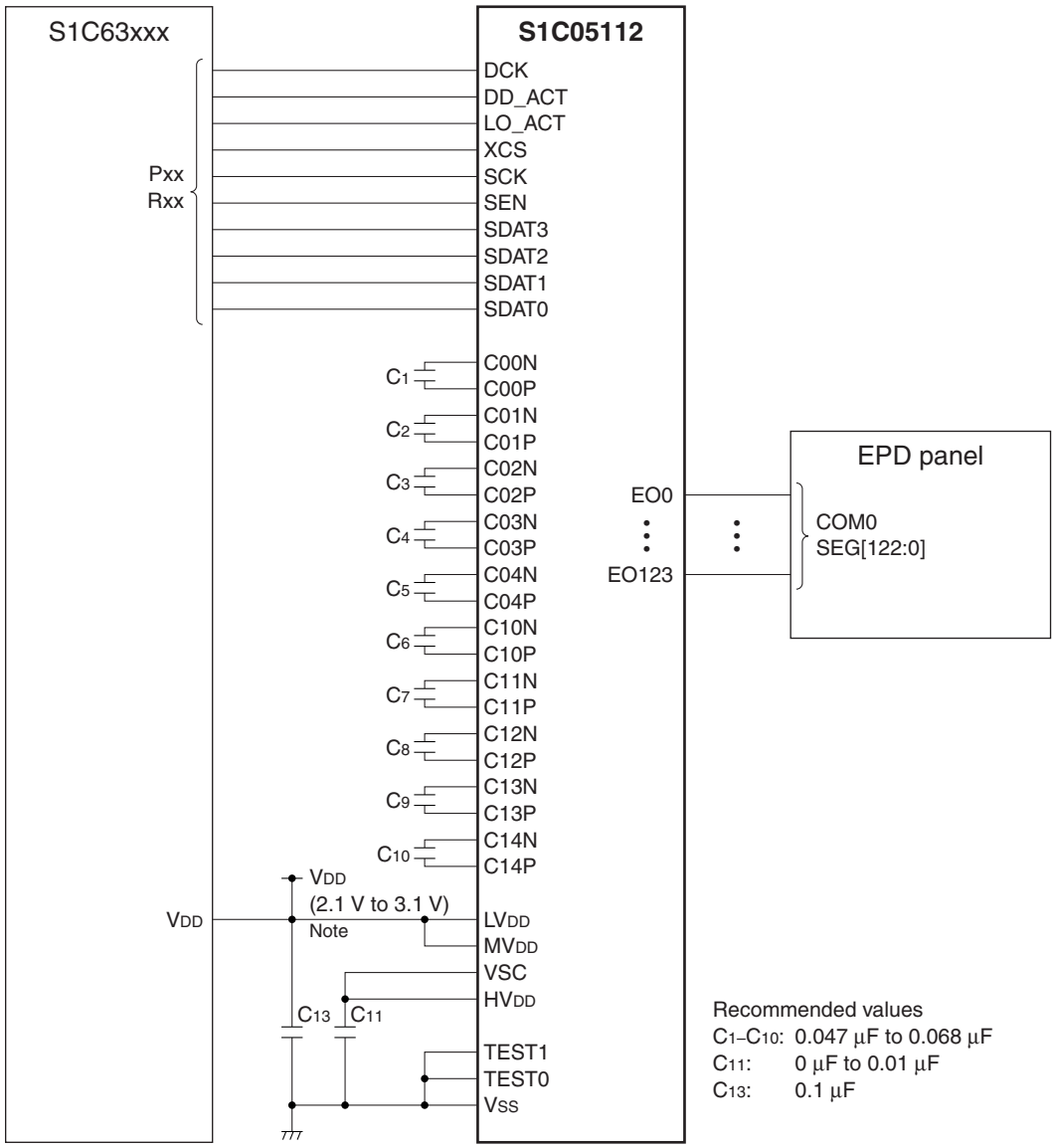
(When the S1C63808 EPD power supply circuit is used)



For details of the S1C63808, refer to the "S1C63808 Technical Manual."

Connection example 2

(When the S1C63808 EPD power supply circuit is not used, or when an MPU other than the S1C63808 is used)



Note: Select a power supply voltage so that the boosted voltage (HV_{DD}) does not exceed the maximum operating voltage of the EPD.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

(V_{SS} = 0V)

Item	Symbol	Rated value	Unit
Supply voltage (1)	LV_{DD}	-0.5 to 4.5	V
Supply voltage (2)	MV_{DD}	-0.5 to 4.5	V
Supply voltage (3) *1	HV_{DD}	-0.5 to 22	V
Input voltage	V_I	-0.5 to LV_{DD} + 0.3	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Permissible total output current *2	ΣI_{HVDD}	10	mA

*1 Power supply other than the DC-DC converter output (VSC) cannot be used.

*2 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

6.2 Recommended Operating Conditions

(Ta = -20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage (1)	LV_{DD}	V_{SS} = 0V	1.0	3.0	3.6	V
Supply voltage (2) *1	MV_{DD}	LV_{DD} = 1.0 to 3.6V	2.1	3.0	3.6	V
Supply voltage (3) *1	HV_{DD}	$MV_{DD} \leq$ 3.33V	12	18	20	V
Operating frequency (1)	DCK	LO_ACT = DD_ACT = H (On)	250	500	1000	Hz
Operating frequency (2)	SCK	LO_ACT = H, data transfer only	3.33	50	750	kHz

*1 Use a voltage within the range that satisfies the EPD maximum voltage specification.

6.3 DC Characteristics

Unless otherwise specified: LV_{DD} = MV_{DD} = 3.0V, Vss = 0V, C_1–C_{10} = 0.068µF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	LO_ACT, DD_ACT, DCK, SCK, SDAT[3:0], XCS, SEN	0.8•LV_{DD}		LV_{DD}	V
Low level input voltage	V_{IL}	LO_ACT, DD_ACT, DCK, SCK, SDAT[3:0], XCS, SEN	0		0.2•LV_{DD}	V
High level input current	I_{IH}	V_{IH} = 3.0V, LO_ACT, DD_ACT, DCK, SCK, SDAT[3:0], XCS, SEN	0		0.5	V
Low level input current	I_{IL}	V_{IL} = Vss, LO_ACT, DD_ACT, DCK, SCK, SDAT[3:0], XCS, SEN	-0.5		0	µA
High level output current	I_{OH}	V_{OH} = 0.9•HV_{DD} : EO[123:0]			-0.4	mA
Low level output current	I_{OL}	V_{OL} = 0.1•HV_{DD} : EO[123:0]	0.7			mA

6.4 Analog Circuit Characteristics and Power Current Consumption

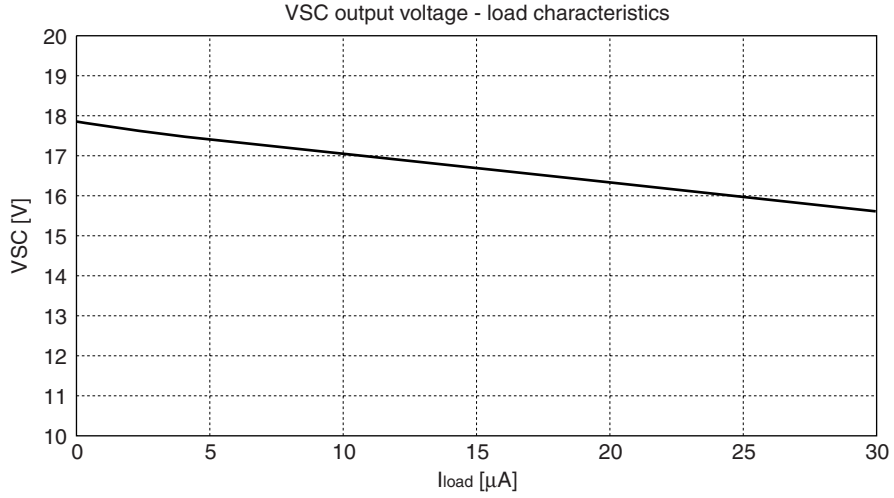
Unless otherwise specified: LV_{DD} = MV_{DD} = 3.0V, Vss = 0V, DCK = 500Hz, C_1–C_{10} = 0.068µF, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EPD driver power voltage 1	V_{SC1}	I_O = 10µA	16.5	17	17.5	V
EPD driver power voltage 2	V_{SC2}	No load	17.5	17.7	17.9	V
VSC settling time	T_{ST1}	10MΩ load, C_{11} = 0.01µF, time until the output reaches 90% after DCK (= 500Hz) is input		5	15	ms
Driver output (EO) settling time	T_{ST2}	10MΩ load, C_{11} = 0.01µF, time until the driver output becomes constant (95% or more) after SEN is set to H		0.5	6	ms
Static current (LV_{DD})	I_{Q1}	LO_ACT = DD_ACT = LV_{DD}, LV_{DD} = MV_{DD} = 3.6V		10	100	nA
Static current (MV_{DD})	I_{Q2}	LO_ACT = DD_ACT = LV_{DD}, LV_{DD} = MV_{DD} = 3.6V		6	100	nA
Standby current (LV_{DD})	I_{HLT1}	LO_ACT = DD_ACT = V_{SS}, LV_{DD} = MV_{DD} = 3.6V		2	100	nA
Standby current (MV_{DD})	I_{HLT2}	LO_ACT = DD_ACT = V_{SS}, LV_{DD} = MV_{DD} = 3.6V		3	100	nA
Current consumption in active state (LV_{DD})	I_{EXE1}	SCK = 50kHz		13	16.3	µA
Current consumption in active state (MV_{DD})	I_{EXE2}	DCK = 500Hz, 10MΩ load		15	21	µA
Current consumption in active state (MV_{DD})	I_{EXE3}	DCK = 500Hz, no load		5	7.5	µA
Current consumption in active state (MV_{DD})	I_{EXE4}	DCK = 500Hz, 10MΩ load		15	21	µA
Static current (HV_{DD})	I_{Q3}	LO_ACT = DD_ACT = LV_{DD}, LV_{DD} = MV_{DD} = 3.6V, HV_{DD} = 18V		2	100	nA

DC-DC converter output (VSC) - load characteristic

The load characteristics change depending on the conditions. Use the following characteristic curve only for reference and evaluation should be performed on the actual product.

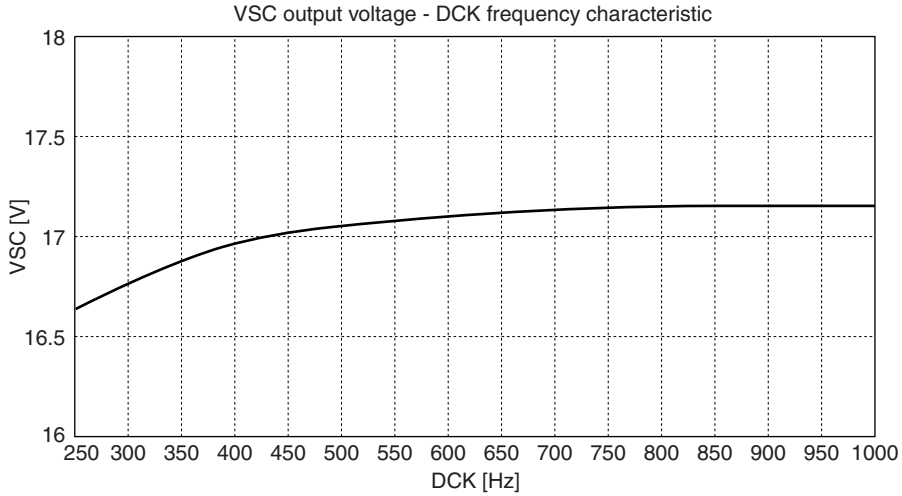
LV_{DD} = MV_{DD} = 3.0V, DCK = 500Hz, Ta = RT



DC-DC converter output (VSC) - DCK frequency characteristic

The frequency characteristics change depending on the conditions. Use the following characteristic curve only for reference and evaluation should be performed on the actual product.

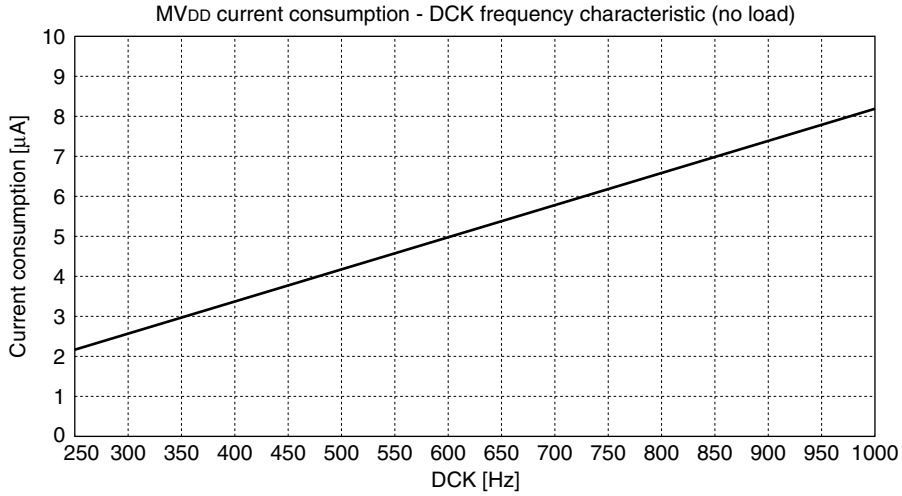
LV_{DD} = MV_{DD} = 3.0V, I_{load} = 10µA, Ta = RT



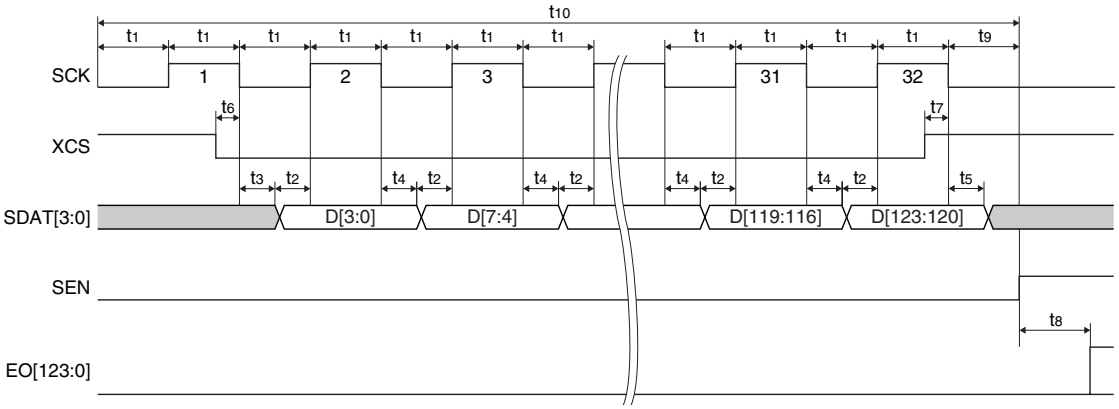
DC-DC converter current consumption (MV_{DD}) - DCK frequency characteristic

The frequency characteristics change depending on the conditions. Use the following characteristic curve only for reference and evaluation should be performed on the actual product.

LV_{DD} = MV_{DD} = 3.0V, I_{load} = 0µA, Ta = RT

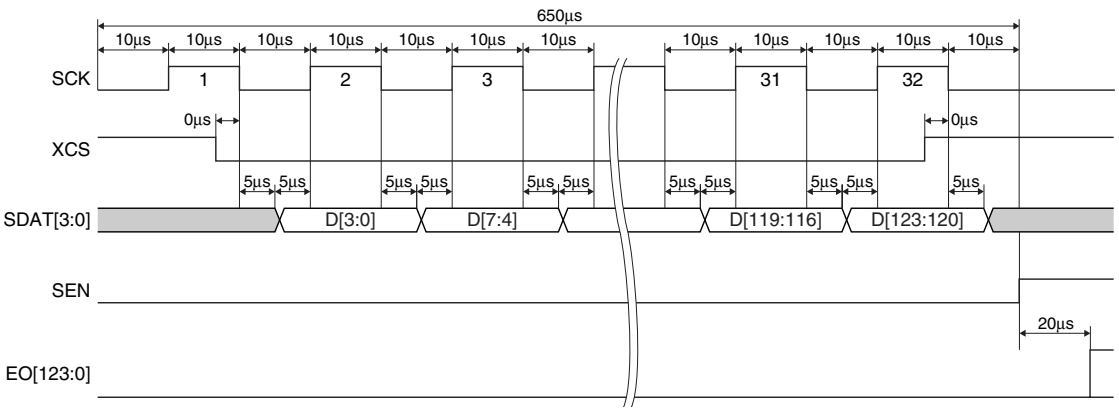


6.5 Interface AC Characteristics



Item	Symbol	Min.	Recommended value	Max.	Unit
SCK	t_1	0.666	10	150	µs
Data setup time ($t_2 \leq t_1$)	t_2	0.3	5		µs
Data input start time	t_3	0	5		µs
Data alteration time	t_4	0	5		µs
Data input end time ($t_5 < t_9$)	t_5	0.3	5		µs
XCS	t_6	-40	0	40	ns
XCS	t_7	-40	0	40	ns
Driver settling time (at no load)	t_8	20			µs
Driver output start time	t_9	0.6	10		µs
Data input period	t_{10}	43.33	650	9,750	µs

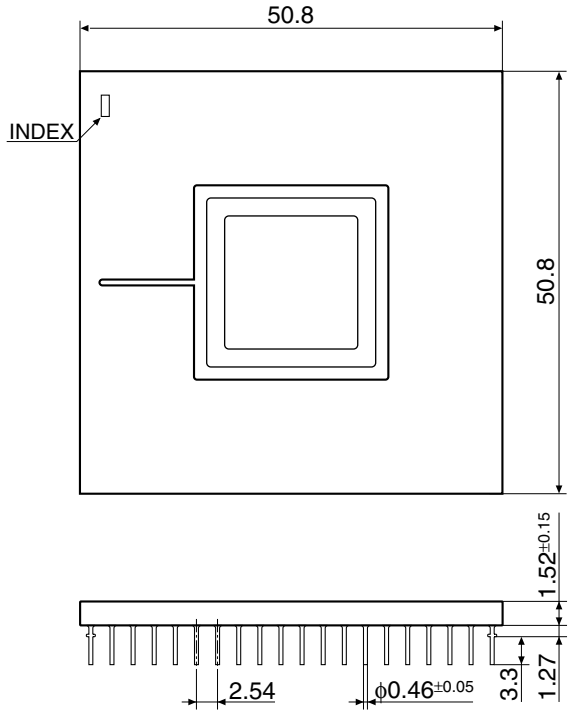
Recommended timing

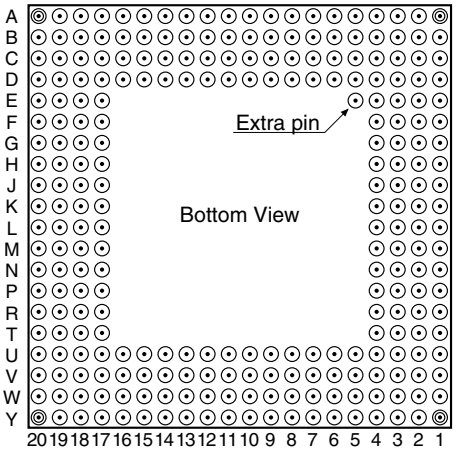


7 Package for Test Samples

PGA-256pin (Ceramic)

(Unit: mm)





Pin No.		Pin name	Pin No.		Pin name	Pin No.		Pin name	Pin No.		Pin name	Pin No.		Pin name
1	A1	N.C.	53	U1	N.C.	105	Y14	EO69	157	M20	N.C.	209	A16	EO7
2	D4	MV_{DD}	54	P4	N.C.	106	U12	EO68	158	L17	EO36	210	D13	EO6
3	C2	N.C.	55	U2	N.C.	107	W14	EO67	159	L20	N.C.	211	B14	EO5
4	D3	LV_{DD}	56	T3	N.C.	108	V12	EO66	160	L19	EO35	212	C13	EO4
5	B1	N.C.	57	V1	N.C.	109	Y15	EO65	161	K20	N.C.	213	A15	EO3
6	E4	V_{SS}	58	R4	EO109	110	V13	EO64	162	K19	EO34	214	C12	EO2
7	D2	N.C.	59	V2	N.C.	111	W15	EO63	163	J20	N.C.	215	B13	EO1
8	E3	N.C.	60	U3	EO108	112	U13	EO62	164	K17	EO33	216	D12	EO0
9	C1	N.C.	61	W1	N.C.	113	Y16	EO61	165	H20	N.C.	217	A14	N.C.
10	F4	N.C.	62	T4	EO107	114	V14	EO60	166	K18	EO32	218	B12	N.C.
11	E2	N.C.	63	W2	N.C.	115	W16	EO59	167	H19	N.C.	219	A13	V_{SS}
12	F3	N.C.	64	V3	EO106	116	V15	EO58	168	J19	EO31	220	C11	HV_{DD}
13	D1	N.C.	65	Y1	EO105	117	Y17	EO57	169	G20	N.C.	221	A12	VSC
14	G4	N.C.	66	U4	EO104	118	U14	EO56	170	J17	EO30	222	D11	C10N
15	F2	N.C.	67	W3	EO103	119	W17	EO55	171	G19	N.C.	223	A11	C10P
16	G3	N.C.	68	V4	EO102	120	V16	EO54	172	J18	EO29	224	B11	C11N
17	E1	N.C.	69	Y2	EO101	121	Y18	EO53	173	F20	N.C.	225	A10	C11P
18	H4	N.C.	70	U5	EO100	122	U15	EO52	174	H18	EO28	226	B10	C12N
19	G2	N.C.	71	W4	EO99	123	W18	EO51	175	F19	N.C.	227	A9	C12P
20	H3	EO123	72	V5	EO98	124	V17	EO50	176	H17	N.C.	228	D10	C13N
21	F1	N.C.	73	Y3	EO97	125	Y19	EO49	177	E20	N.C.	229	A8	C13P
22	J3	EO122	74	U6	EO96	126	U16	EO48	178	G18	N.C.	230	C10	C14N
23	H2	N.C.	75	W5	EO95	127	W19	EO47	179	E19	N.C.	231	B8	C14P
24	J4	EO121	76	V6	EO94	128	V18	EO46	180	F18	N.C.	232	B9	C04P
25	G1	N.C.	77	Y4	EO93	129	Y20	N.C.	181	D20	N.C.	233	A7	C04N
26	J2	EO120	78	U7	EO92	130	U17	EO45	182	G17	N.C.	234	D9	C03P
27	H1	N.C.	79	W6	EO91	131	V19	N.C.	183	D19	N.C.	235	B7	C03N
28	K3	EO119	80	V7	EO90	132	U18	EO44	184	E18	N.C.	236	C9	C02P
29	J1	N.C.	81	Y5	EO89	133	W20	N.C.	185	C20	N.C.	237	A6	C02N
30	K4	EO118	82	U8	EO88	134	T17	EO43	186	F17	EO27	238	C8	C01P
31	K1	N.C.	83	W7	EO87	135	U19	N.C.	187	C19	N.C.	239	B6	C01N
32	K2	EO117	84	V8	EO86	136	T18	EO42	188	D18	EO26	240	D8	C00P
33	L1	N.C.	85	Y6	EO85	137	V20	N.C.	189	B20	N.C.	241	A5	C00N
34	L2	EO116	86	V9	EO84	138	R17	N.C.	190	E17	EO25	242	C7	N.C.
35	M1	N.C.	87	W8	EO83	139	T19	N.C.	191	B19	N.C.	243	B5	N.C.
36	L4	EO115	88	U9	EO82	140	R18	N.C.	192	C18	EO24	244	C6	V_{SS}
37	N1	N.C.	89	Y7	EO81	141	U20	N.C.	193	A20	EO23	245	A4	DCK
38	L3	EO114	90	W9	EO80	142	P17	N.C.	194	D17	EO22	246	D7	DD0
39	N2	N.C.	91	Y8	EO79	143	R19	N.C.	195	B18	EO21	247	B4	DD1
40	M2	EO113	92	V10	EO78	144	P18	N.C.	196	C17	EO20	248	C5	DD_ACT
41	P1	N.C.	93	Y9	EO77	145	T20	N.C.	197	A19	EO19	249	A3	LO_ACT
42	M4	EO112	94	U10	EO76	146	N17	N.C.	198	D16	EO18	250	D6	SCK
43	P2	N.C.	95	Y10	N.C.	147	P19	N.C.	199	B17	EO17	251	B3	XCS
44	M3	EO111	96	W10	N.C.	148	N18	EO41	200	C16	EO16	252	C4	SEN
45	R1	N.C.	97	Y11	N.C.	149	R20	N.C.	201	A18	EO15	253	A2	SDAT0
46	N3	EO110	98	W11	N.C.	150	M18	EO40	202	D15	EO14	254	D5	SDAT1
47	R2	N.C.	99	Y12	EO75	151	N19	N.C.	203	B16	EO13	255	B2	SDAT2
48	N4	N.C.	100	U11	EO74	152	M17	EO39	204	C15	EO12	256	C3	SDAT3
49	T1	N.C.	101	Y13	EO73	153	P20	N.C.	205	A17	EO11			
50	P3	N.C.	102	V11	EO72	154	M19	EO38	206	D14	EO10			
51	T2	N.C.	103	W13	EO71	155	N20	N.C.	207	B15	EO9			
52	R3	N.C.	104	W12	EO70	156	L18	EO37	208	C14	EO8			

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S1C05112
Technical Manual

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Document code: 411004402
First issue April, 2007
Printed October, 2008 in Japan ⓁA