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S5U1C33001H (Ver. 4.1)

S1C33 Family In-Circuit Debugger

■ OVERVIEW

The S5U1C33001H (In-Circuit Debugger for the S1C33 Family) is a hardware tool (emulator) that allows software to be efficiently developed for the S1C33 Family of 32-bit Single-Chip Microcomputers. It provides a software development environment by communicating with the S1C33xxx chip.
This manual primarily explains how to use the S5U1C33001H. For details on the debugger (gdb.exe) functions and commands, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".
The figure below shows an external view of the S5U1C33001H.

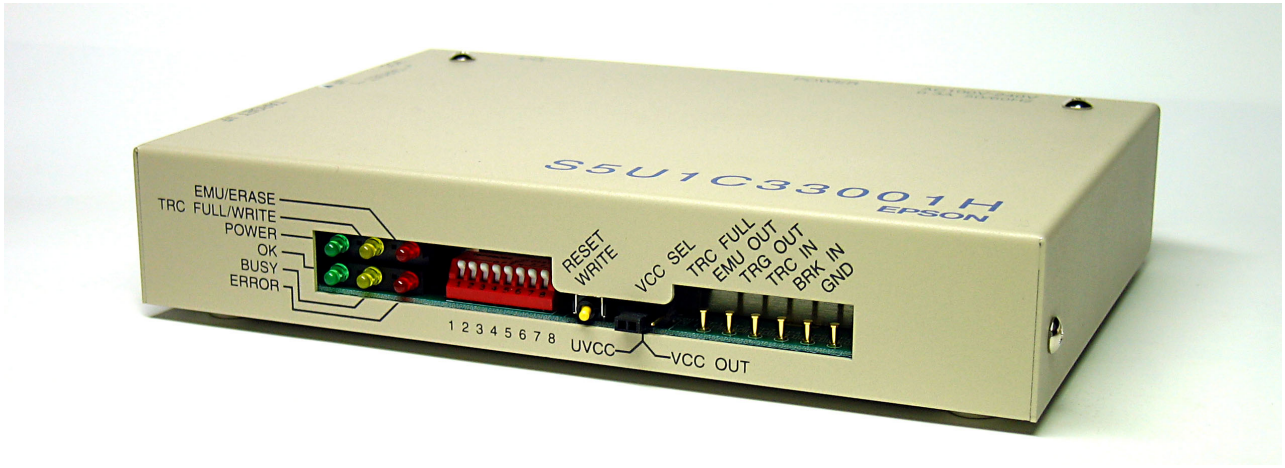


Figure 1 S5U1C33001H External View

Note: Do not open the case as it may cause a malfunction.

Precautions before using the S5U1C33001H

Please read the sections shown below before getting started with the S5U1C33001H. These sections, especially (2) and (3), describe the answers to frequently asked questions.

(1) "Components Included with Package" section
Make sure all of the listed items are included with your package.

(2) "Connecting the S5U1C33001H and the Host Computer" section
Install the USB driver before the S5U1C33001H can be used.

(3) "Connecting the Target System" section
Please pay particular attention to the Notes.

Table 1 ICD Models and Differences

Function \ Model	S5U1C33000H	S5U1C33001H		
		Ver. 3	Ver. 4.0	Ver. 4.1
C33 cores supported	C33 STD core C33 Mini core	C33 STD core C33 Mini core C33 PE core *5	C33 STD core C33 Mini core C33 PE core C33 ADV core	
Interface with the host PC	Serial and parallel I/F	USB 1.1	USB 1.1	
Data download speed (maximum rate: DCLK = 40 MHz)	Serial I/F: Approx. 8KB/s Parallel I/F: Approx. 30KB/s	About 65KB/s (About 50KB/s at 20 MHz)	About 65KB/s (About 50KB/s at 20 MHz)	
Clock frequency to communicate with the target	1 MHz to 40 MHz	1 MHz to 40 MHz	1 MHz to 40 MHz *3	
Core clock frequency for using the trace function	1 MHz to 60 MHz (3.3 V) *1 (4 or 10-pin cable)	1 MHz to 60 MHz (3.3 V) *1 (4 or 10-pin cable)	1 MHz to 120 MHz (3.3 V) *2, *3 (4 or 10-pin cable, or 30-pin coaxial cable)	
Maximum trace capacity	128K clock cycles	1M clock cycles	1M clock cycles	
Flash programmer function	–	Available	Available	
Firmware update function	–	–	Available	
Debugger mode	ICD2 mode	ICD3 mode	ICD3 mode	
Bus trace function	–	–	Available	
Bus break trigger trace function	–	–	Available	
TRC IN pin input signal trace function	–	–	Available	
User logic signal trace function *4	–	–	Available	
Target power supply	–	–	3.3 V and 1.8 V	
Target reset signal output	–	–	Available	
Target system I/O interface voltage	3.3 V	3.3 V	3.3 V or 1.8 V	
RESET/WRITE switch	–	Available	Available	
DIP switch	4 bits	8 bits	8 bits	
Jumper switch for monitoring power supply	–	Available	Available	
LEDs for flash programmer	–	Available	Available	
Target system interface connector	10 pins	10 pins	10 pins, 30 pins	
Target system interface method	4 pins, 10 pins	4 pins, 10 pins	4 pins, 10 pins, 30 pins	
Target power supply connector	–	–	6 pins	
Core sync simple logic analyzer function	–	–	Available *5	Available
PC tracing in the MCU that does not output DST1–0 and DPCO by default	–	–	–	Supported

*1 Indicates the frequency range for 3.3-V I/O. The upper-limit frequency may be lowered by environment noise, temperature condition, S1C33 model, unevenness in quality, etc.

Note: In the model with the C33 STD or Mini core embedded, the maximum CPU core clock frequency is 60 MHz but the maximum BCU (bus) clock frequency is 40 MHz. When operating the CPU with a clock higher than 40 MHz, the BCU clock must be setup to 1/2 CPU core clock (#X2SPD = 0).

*2 The maximum frequency may be half or less of the described value when the I/O voltage is 1.8 V.

*3 Supports 32 kHz by firmware update.

*4 Available only when the S1C33 model that supports the user logic signal trace function is used.

*5 Supports by firmware update.

Table 2 Correspondence between C33 Core and Debug Functions

Function \ Core	C33 STD/Mini	C33 PE	C33 ADV
DCLK while the program is halted	= Bus clock	= Core clock × set value	= Core clock × set value
DCLK while the program is being executed	= Core clock	= Core clock	= Core clock
PC trace method	Level 1	Level 1	Level 2
Switching the DCLK-core clock ratio (DCLK while the program is halted)	–	Available	Available
Address setup for the debug unit	–	Available	–
Area break function	–	–	Available
Bus break function	–	–	Available
Bus trace function	–	–	Available
Bus break trigger trace function	–	–	Available
TRC IN pin input signal trace function	–	–	Available
User logic signal trace function *4	–	–	Available
Use of MMU in debug mode	–	–	Available

*4 Available only when the S1C33 model that supports the user logic signal trace function is used.

Level 2 is a PC trace method upwardly compatible with Level 1. It realizes higher analytical accuracy than Level 1.
Functions that are not included in the table above can be used regardless of the core model.

■ FUNCTIONAL OUTLINE

The functions of the S5U1C33001H are outlined below.

(1) Break functions
- PC break function
- Data break function
- Forced break function
- External forced break function (BRK IN pin input)
- Area break function
- Bus break function
  - Logical or physical address is selectable.

(2) Trace functions
- Normal PC trace function/normal bus trace function
  - Either the 1M clock cycles after a go command or the last 1M clock cycles before a break can be traced.
  - The bus trace function allows selection of logical or physical addresses.
- Area PC trace function/area bus trace function
  - Only the area between trace trigger 1 and trace trigger 2 is traced.
  - Up to 1M clock cycles can be traced.
  - The bus trace function allows selection of logical or physical addresses.
- Bus break trigger trace function
- TRC IN pin input signal trace function
- User logic signal trace function

(3) Measurement of the target program execution time
- The total time within an area can be measured in area trace mode.

(4) Flash memory writing function

(5) Flash programmer function

(6) Data transfer rate
- Execution rate: About 65KB/s

(7) Power supply to the target system
- 3.3 V and 1.8 V. The power supply monitoring function is available.

(8) Reset signal output to the target system

(9) Firmware update function

(10) Core sync simple logic analyzer function

■ OPERATING ENVIRONMENT

As the host computer, the S5U1C33001H uses a PC with a USB port (USB 1.1) available. Windows 2000 or Windows XP is recommended for the OS.

■ COMPONENTS INCLUDED WITH PACKAGE

The following shows the components included with the package:

(1) S5U1C33001H (main unit) 1
(2) USB cable 1
(3) Target system interface cable (10-pin) 1
(4) Target system interface cable (4-pin) 1
(5) Target system interface cable (30-pin) 1
(6) Target system interface connectors (10-pin) ..... 4 (straight × 2, low-angle × 2)
(7) Target system interface connectors (4-pin) ..... 4 (straight × 2, low-angle × 2)
(8) Target system interface connectors (30-pin) ..... 2 (low-angle × 2)
(9) AC cable 1
(10) Target system power supply cable (6-pin) 1
(11) Target system power supply connector (6-pin) ..... 1 (low-angle)
(12) User registration card ..... English/Japanese, 1 each
(13) Warranty card ..... English/Japanese, 1 each
(14) Usage precautions ..... English/Japanese, 1 each
(15) Manual download guide ..... English/Japanese, 1 each

The items specified below are not included with the package. These items must be prepared separately.

(16) S5U1C33001H (Ver. 4.1) Manual (S1C33 Family In-Circuit Debugger) (this PDF, downloadable from the SEIKO EPSON HP)
(17) Debugger (gdb.exe) for the S1C33 Family (included in the S1C33 Family C Compiler Package)
(18) Debugger manual for the S1C33 Family (included in the S1C33 Family C Compiler Package)

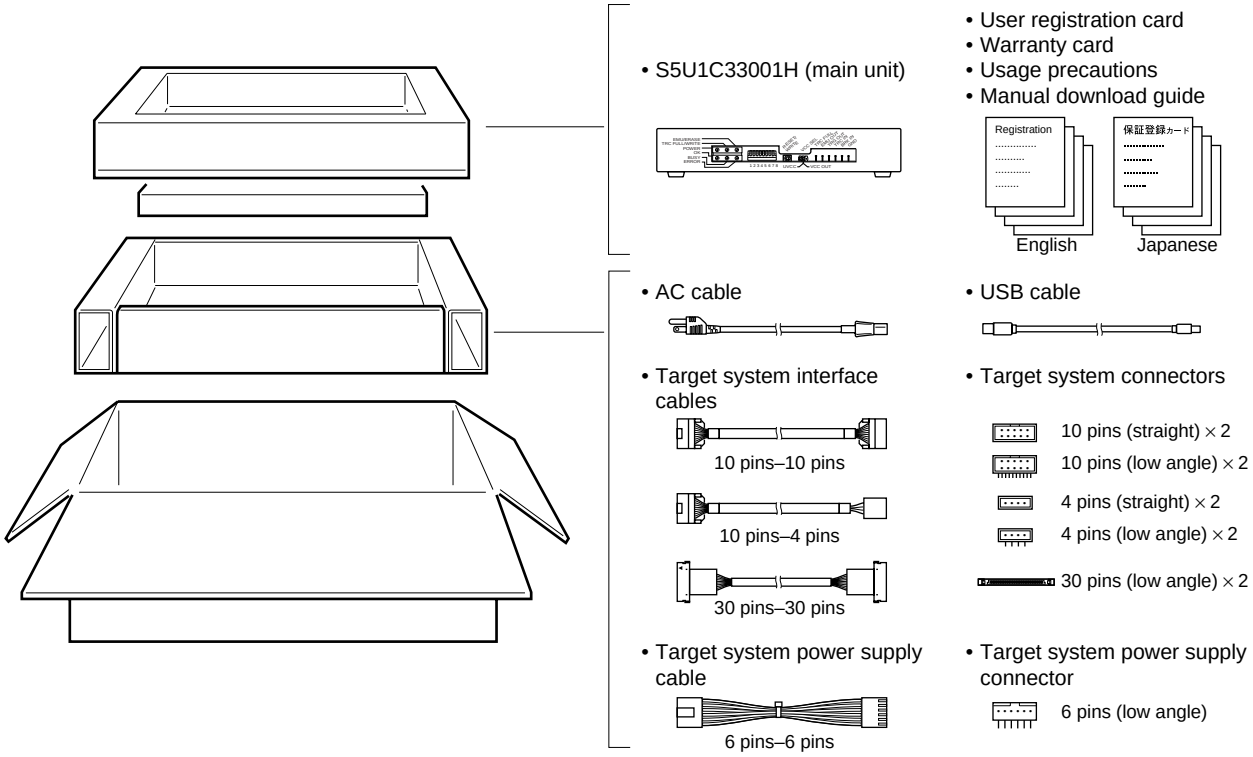


Figure 2 Package Components

■ NAME AND FUNCTION OF EACH PART

● Operation Panel

The following shows an external view of the S5U1C33001H's operating section and the name of each part.

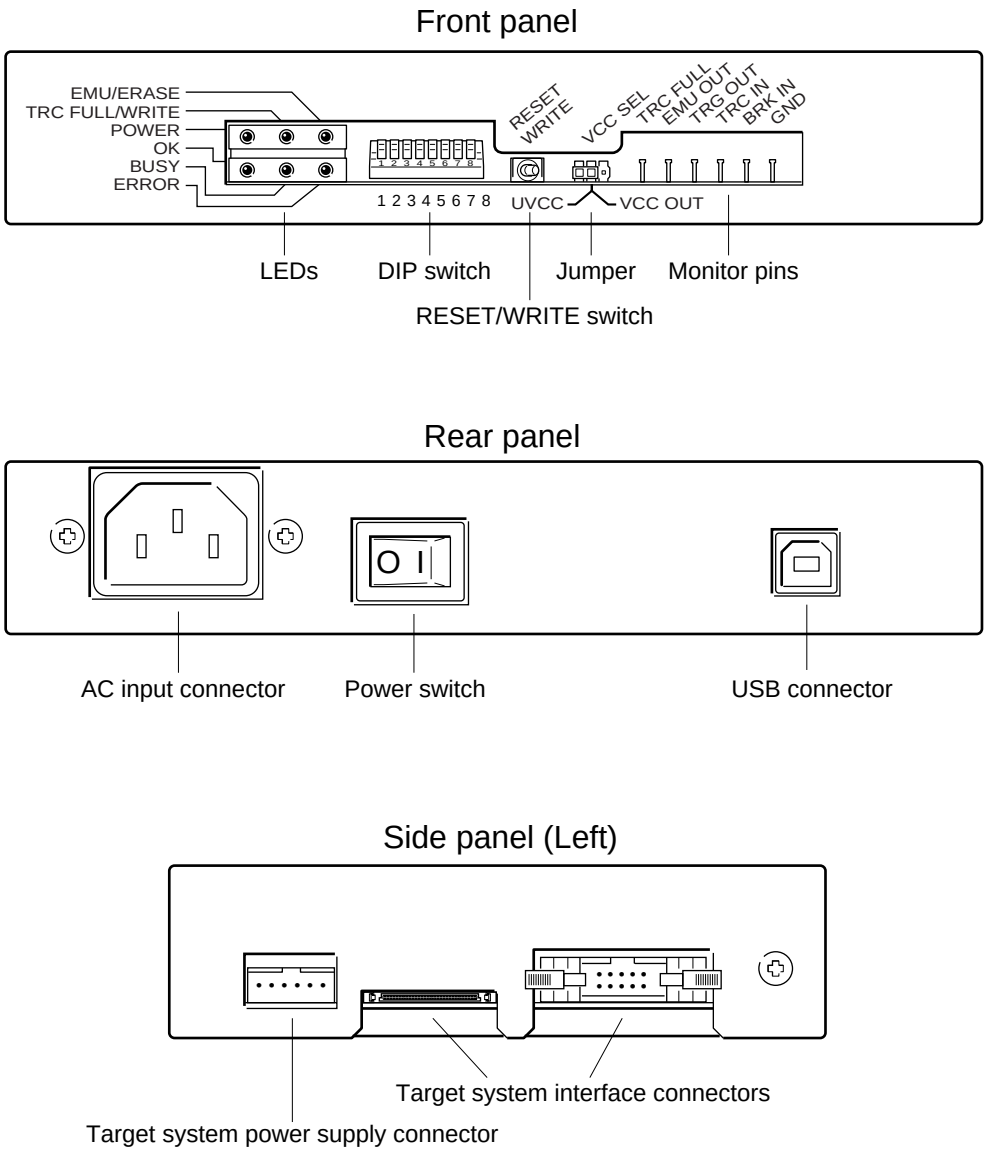


Figure 3 External View of Operating Section

● DIP Switches

Note: Before setting the DIP switch, be sure to turn off the power to the S5U1C33001H.

The DIP switch assembly on the S5U1C33001H front panel is used to set the following conditions: DCLK setting, flash programmer mode, target connection diagnostic function, flash programmer verification mode, and DSIO output level. The figure below shows an external view of the DIP switch assembly.

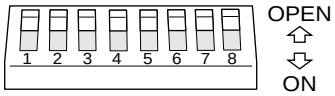


Figure 4 DIP Switch

• Flash programmer mode setting

DIP switches 1 and 7 enable/disable the flash programmer mode.

Table 3 DIP SW1 and SW7 Settings

SW1	SW7	Setting
OPEN	OPEN	Flash programmer mode disabled (default)
OPEN	ON	Flash programmer mode disabled
ON	OPEN	Flash programmer mode enabled (erase and write mode)
ON	ON	Flash programmer mode enabled (verify mode)

• DCLK - core clock ratio setting

DIP switches 2 and 3 set the ratio of the DCLK to the core clock frequencies.

Table 4 DIP SW2 and SW3 Settings

SW2	SW3	Setting
OPEN	OPEN	1/4 core clock (default)
OPEN	ON	1/2 core clock
ON	OPEN	1/1 core clock
ON	ON	1/8 core clock

These switches set the DCLK - core clock ratio while the program execution is halted. Select an appropriate value so that the DCLK frequency will not exceed 40 MHz. If DCLK exceeds 40 MHz, the S5U1C33001H will not be able to communicate with the target system normally; it may result in a target system failure.
While the program is being executed, the DCLK is set to the same frequency with the core clock. The upper-limit frequency in this case is 100 MHz to perform tracing. There is no limit when tracing is not performed.

• Trace function setting

DIP switches 4 and 5 enable/disable the trace function.

Table 5 DIP SW4 and SW5 Settings

SW4	SW5	Setting
OPEN	OPEN	PC trace enabled, bus trace disabled (default)
OPEN	ON	PC trace disabled, bus trace disabled
ON	OPEN	PC trace enabled, bus trace enabled
ON	ON	Illegal value

• Target system connection diagnostics setting

DIP switch 6 selects whether the target system connection diagnostics function is used or not.

Table 6 DIP SW6 Setting

SW6	Setting
OPEN	The target system connection test is run when the debugger is started. (default)
ON	The target system connection test is omitted when the debugger is started.

• DSIO output level setting

DIP switch 8 sets the DSIO output level.

Table 7 DIP SW8 Setting

SW8	Setting
OPEN	DSIO output level: 3.3 V (default)
ON	DSIO output level: 1.8 V

● RESET/WRITE Switch

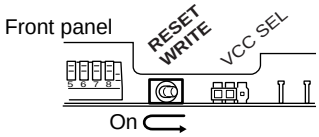


Figure 5 RESET/WRITE Switch

This switch functions as both the S5U1C33001H reset switch and as the erase/write switch when the S5U1C33001H is in flash programmer mode.

● VCC SEL Jumper

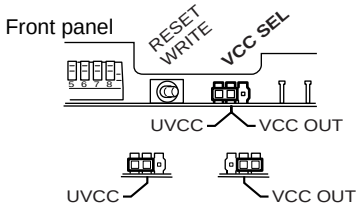


Figure 6 VCC SEL Jumper

This jumper selects whether the power supply monitoring function for the power supplied to the target system is used or not. The power supply monitoring function stops power supply to the target system when the input to the TARGET_VCC pin in the target power supply connector is 0 V.

Table 8 VCC SEL Setting

Jumper setting	Description
UVCC	The power supply monitoring function is used
VCC OUT	The power supply monitoring function is not used

● Monitor Pins

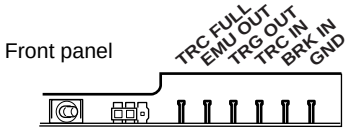


Figure 7 Monitor Pins

• TRC FULL output pin

This is the trace full state output pin. This pin outputs a high level when the trace memory becomes full.

• EMU OUT output pin

This pin outputs a low level when the EMU/ERASE LED is lit (that is, when the program is being executed) and outputs the 5 V level when that LCD is off (during a break). This signal can be used as the protect signal for the S5U1C33xxxM emulation memory.

• TRG OUT output pin

The TRG OUT pin outputs the trace trigger signal that indicates the beginning and end of tracing. When using area trace mode in the S5U1C33001H, two trigger points (trace area start and end addresses) are set up. The TRG OUT pin outputs a high level when the program execution address reaches the set trace trigger point. Also it outputs a high level while program execution is suspended. Refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)" for details on using the trace function.

The figure below shows output timing examples of this signal. Note that the program must be executed in the order of trace trigger points 1 and 2 to generate trace triggers. The following figure shows conditions that will generate trace triggers as well as those that will not.

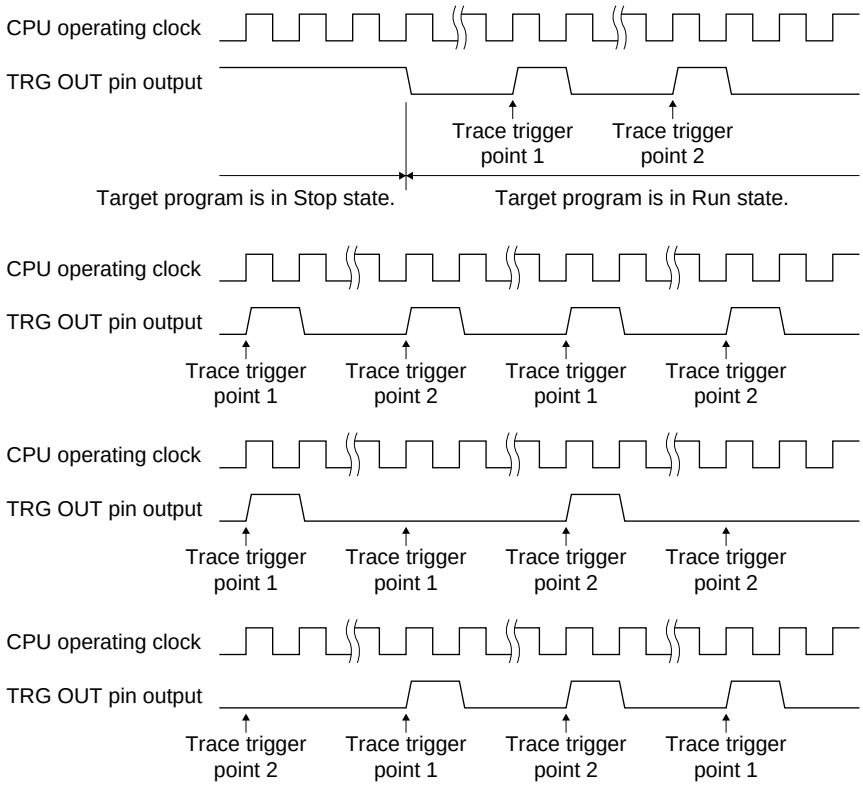


Figure 8 TRG OUT Output Timing Examples

• TRC IN input pin

This pin inputs an external trace signal. The input signal can also be traced when the bus trace is performed.

• BRK IN input pin

If a low-level signal is input to this pin when the target program is being executed, the target program execution is suspended. After a low level is input to the BRK IN terminal, a break will occur after a few instructions have been executed.

Note: Do not apply any voltages other than the following to the BRK IN pin: 0 V (low level), 3.3 to 5.0 V (high level), or open.

• GND pin

To monitor the signals output from the above pins, connect the GND of a measuring instrument such as an oscilloscope to this pin. If the ground level between the S5U1C33001H and the target system is unstable (particularly when the 4-pin cable is used), this pin can be used to stabilize the ground level.

● LEDs

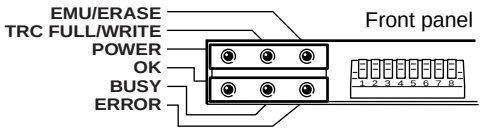


Figure 9 LEDs

• POWER (power-on LED, green)

This LED lights up when power is properly supplied to the S5U1C33001H by placing the power switch on the rear panel in the "I" position. If this LED does not light up even when the power switch is turned on, check if the AC cable is properly connected.

• TRC FULL/WRITE (trace memory full/flash memory write LED, yellow)

This LED lights up when the S5U1C33001H trace memory is filled by the target program execution. However, it does not light up if the trace function is disabled by DIP switches 4 and 5. For enabling/disabling the trace function using the DIP switch, refer to "Trace function setting" in the "DIP Switches" section.

Note: The TRC FULL LED that lights up does not go off until the S5U1C33001H starts sampling of trace data by restarting the target program.

The WRITE LED lights during writing to the target system flash memory and goes off when the writing completes. The ERASE LED also lights during verification.

• EMU/ERASE (emulation/flash memory erase LED, red)

This LED lights up when the debugger executes a program execution command, and indicates that the target program is being executed.
Furthermore, it lights up if the target system power is off or the target system is not connected to the S5U1C33001H when the S5U1C33001H is turned on. In this case, this LED goes off by turning the target system on. If the target system is not connected, connect it to the S5U1C33001H after turning the S5U1C33001H off, and then turn the target system and S5U1C33001H on. In break mode, this LED goes off and the S5U1C33001H can communicate with the S1C33xxx chip.

The ERASE LED lights when the target system flash memory is being erased and goes off when the erase operation completes. The WRITE LED also lights during verification.

• OK (flash programmer mode OK LED, green)

This LED lights in flash programmer mode when a target system flash memory write, erase, or verify operation completes with no error occurred.

• BUSY (flash programmer mode BUSY LED, yellow)

This LED lights in flash programmer mode when a target system flash memory write, erase, or verify operation is in progress. It also lights during initialization after power is turned on.

• ERROR (flash programmer mode ERROR LED, red)

This LED lights in flash programmer mode when an error occurs during a target system flash memory write, erase, or verify operation.

● Power-Supply Operation Section

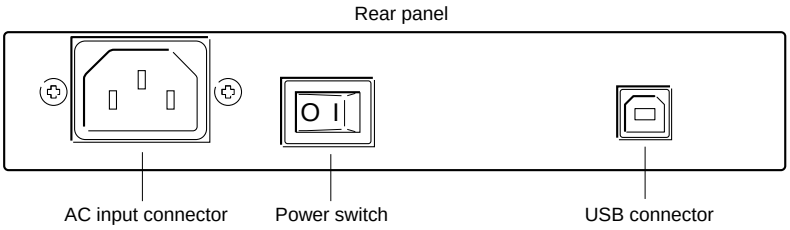


Figure 10 Power-Supply Operation Section

- **Power switch**
  This is the power switch of the S5U1C33001H. The S5U1C33001H turns on when this switch is set to the "I" position.
- **AC input connector**
  Plug the AC cable in this connector.
- **USB connector**
  This connector is used to connect a USB cable.

● Target System Interface Connectors

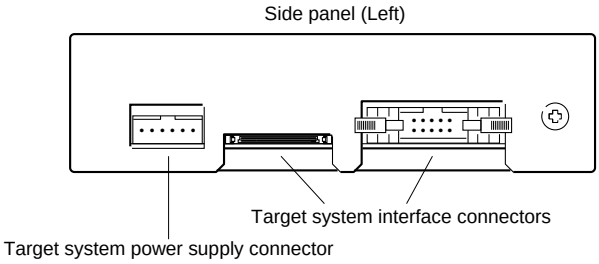


Figure 11 Target System Interface Connectors

- **10-pin target system interface connector**
  The target system is connected using the 10-pin or 10 to 4-pin cable.
- **30-pin target system interface connector**
  The target system is connected using the 30-pin cable.

Note: Use one connector only from either the 10-pin or 30-pin target system interface connectors.

- **Target system power supply connector**
  This connector can supply power and output a reset signal to the target system using the 6-pin cable.

■ CONNECTING THE S5U1C33001H AND THE HOST COMPUTER

● Connecting the AC Cable

The S5U1C33001H uses a 3-wire (grounded) AC power cable.
Connect the AC frame ground of the host computer and the S5U1C33001H to a common frame ground as shown in the figure below.

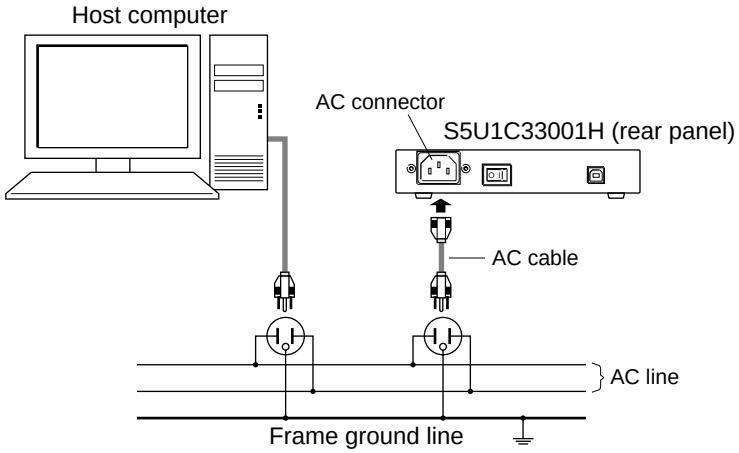


Figure 12 AC and Frame Ground Lines

● Connecting the USB Cable

The connectors at each end of the USB cable are type A (for the host computer) and type B (for the S5U1C33001H).
Turn on the S5U1C33001H power and connect the USB cable to the host computer. The host computer will request that the USB driver be installed.
Use the procedure described in the next section to install the USB driver.

Note: The USB driver is located in the directory in which the S5U1C33001C (S1C33 Family C Compiler Package) is installed: C:\gnu33\utility\drv_usb.

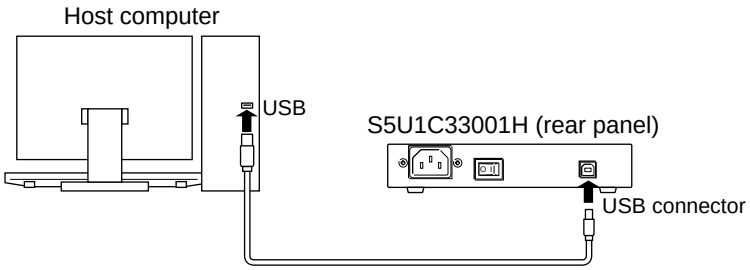
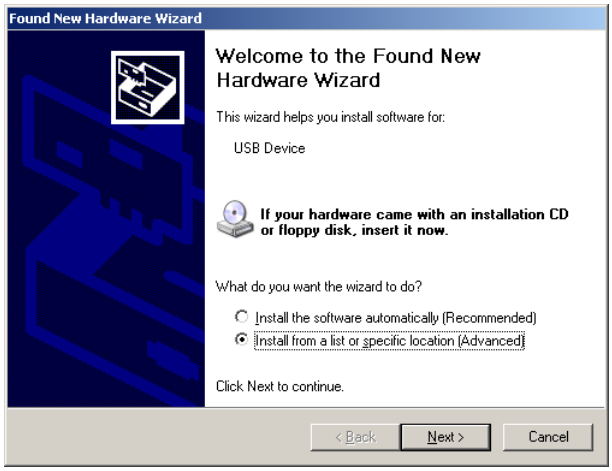


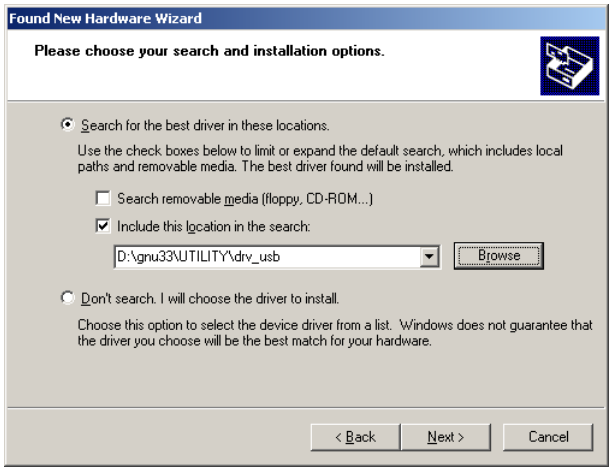
Figure 13 Connecting the USB Cable

● USB Driver Installation Procedure

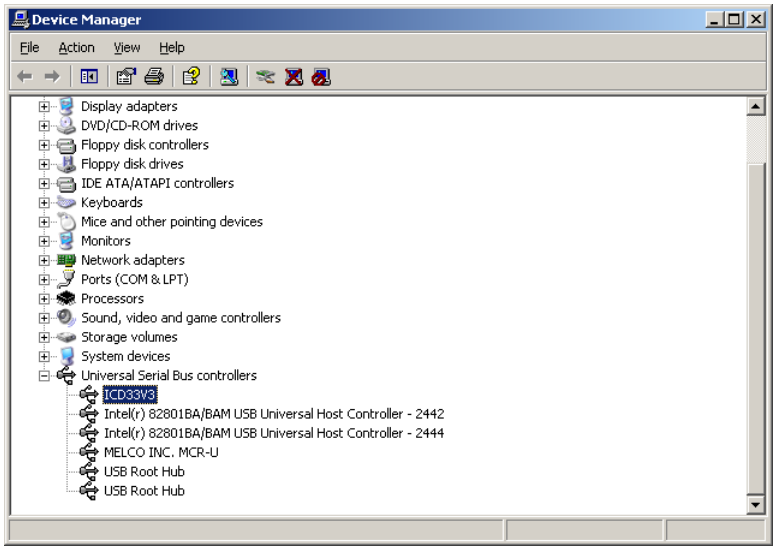
(1) When the USB cable is first connected to the host computer, the following window will be displayed.



(2) Install the USB driver by following the directions displayed by the wizard.
Specify "C:\gnu33\utility\drv_usb" as the USB driver directory.



The device manager will be displayed as shown below when the USB driver has been installed correctly.



Note: If the window above is not displayed correctly, reinstall the USB driver.

■ CONNECTING THE TARGET SYSTEM

Use the 30-pin, 10-pin or 4-pin target system interface cable supplied with the S5U1C33001H package to connect the target system. The target system must have a connector for connecting the above cable. For this, use the 30-pin, 10-pin or 4-pin target connector supplied with the S5U1C33001H package or an equivalent connector. The pin assignment of the target connector is shown in the tables below. For each signal pin number of the S1C33xxx chip, refer to the "S1C33xxx Technical Manual" of the specific model.

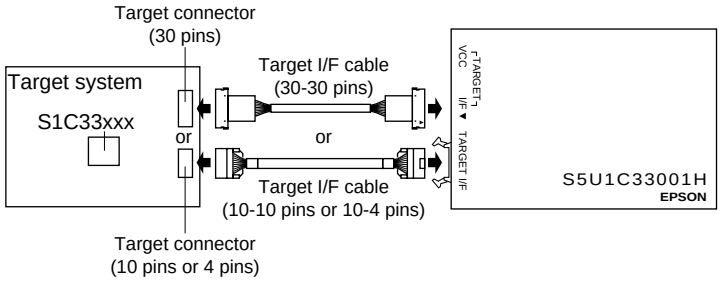
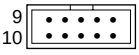


Figure 14 Connecting the Target System

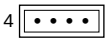
Table 9 Pin Assignment of Target Connectors

10-pin connector



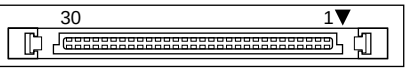
No.	Pin name	I/O	Pin function
1	DCLK	I	Clock for debugging
2	GND	–	Power supply (GND)
3	DSIO	I/O	Serial I/O signal for debugging
4	GND	–	Power supply (GND)
5	DST2	I	Debug status 2 signal
6	GND	–	Power supply (GND)
7	DST1	I	Debug status 1 signal
8	GND	–	Power supply (GND)
9	DST0	I	Debug status 0 signal
10	DPCO	I	PC signal

4-pin connector



No.	Pin name	I/O	Pin function
1	DCLK	I	Clock for debugging
2	GND	–	Power supply (GND)
3	DSIO	I/O	Serial I/O signal for debugging
4	DST2	I	Debug status 2 signal

30-pin connector



No.	Pin name	I/O	Pin function	No.	Pin name	I/O	Pin function
1	GND	–	Power supply (GND)	16	DTS2	I	Bus trace status 2 signal
2	DCLK	I	Clock for debugging	17	DTS1	I	Bus trace status 1 signal
3	GND	–	Power supply (GND)	18	DTS0	I	Bus trace status 0 signal
4	DSIO	I/O	Serial I/O signal for debugging	19	GND	–	Power supply (GND)
5	GND	–	Power supply (GND)	20	DTD7	I	Bus trace data 7 signal
6	DST2	I	Debug status 2 signal	21	DTD6	I	Bus trace data 6 signal
7	GND	–	Power supply (GND)	22	DTD5	I	Bus trace data 5 signal
8	DST1	I	Debug status 1 signal	23	DTD4	I	Bus trace data 4 signal
9	GND	–	Power supply (GND)	24	GND	–	Power supply (GND)
10	DST0	I	Debug status 0 signal	25	DTD3	I	Bus trace data 3 signal
11	GND	–	Power supply (GND)	26	DTD2	I	Bus trace data 2 signal
12	DPCO	I	PC signal	27	DTD1	I	Bus trace data 1 signal
13	GND	–	Power supply (GND)	28	DTD0	I	Bus trace data 0 signal
14	DTS4	I	Bus trace status 4 signal	29	GND	–	Power supply (GND)
15	DTS3	I	Bus trace status 3 signal	30	DBT	I	Bus break trigger signal

Notes:
- **The signals connected to the S5U1C33001H are very high-speed signals, so the target connector must mounted within 5 cm from the S1C33xxx. If there is more distance between the connector and the S1C33xxx chip, the S5U1C33001H may not work properly.**
- **A 33 Ω resistor must be connected in series to the DSIO signal line between the connector and the S1C33xxx chip. The resistor should be placed as close to the S1C33xxx as possible.**
- **Be sure to use the supplied 30-pin, 10-pin or 4-pin cable for connecting the target system to the S5U1C33001H. Using another cable may cause a malfunction. Furthermore, do not use the 30-pin cable and 10-pin or 4-pin cable simultaneously.**
- **Disable the trace function of the S5U1C33001H using DIP switch 4 in the following cases:**
  - **when using the 4-pin cable and connector.**
  - **when the signals (DST0, DST1, DPCO) necessary for tracing are not connected even if the 30-pin or 10-pin cable and connector is used.**
  - **when the trace function is not used due to some reason even if the 30-pin or 10-pin cable and connector is used and all the signals are connected.**
- **The 4-pin connector does not have a projection for preventing reverse insertion. Check the cable marker of pin 1 to be sure the insertion of connector is proper when connecting it to the target system.**

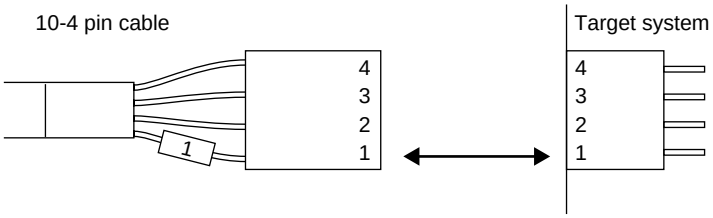
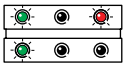


Figure 15 Connecting with 4-pin Connectors

■ START-UP METHOD (POWER-ON SEQUENCE)

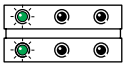
To start up the S5U1C33001H system, follow the sequence described below:

(1) Turn the S5U1C33001H on.



POWER LED (green) lit
OK LED (green) lit
EMU/ERASE LED (red) lit

(2) Turn the target system on.



EMU/ERASE LED (red) goes out

This indicates that the target system was connected correctly.

(3) Start up the debugger (gdb.exe) on the host computer in ICD mode.

To terminate the S5U1C33001H system, follow the sequence described below:

(1') Terminate the debugger (gdb.exe) on the host computer.

(2') Turn the target system off.

(3') Turn the S5U1C33001H off.

Notes:
- **Normally the S5U1C33001H system can work properly when the target system is turned on first and then the S5U1C33001H. However, the power-on sequence described above is recommended since the system may not work properly if the target system is in indeterminate operation or in runaway status.**
- **If the debugger (gdb.exe) is terminated after the S5U1C33001H is turned off, the debugger may not work properly with "Cannot open ICD33 usb driver." displayed on the screen when it is re-invoked. In this case, turn on or reset the S5U1C33001H after terminating the debugger (gdb.exe) once, and then re-invoke the debugger.**

For details on how to invoke/terminate the debugger, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)". Furthermore the debugger (gdb.exe) must be invoked after turning all the power of the system on.

Check the following if the debugger reports a target down error, which means that communication between the S5U1C33001H and the target system is not functioning.

- **If the target system power is turned on after the S5U1C33001H is turned on:**
  After the S5U1C33001H power is turned on, a forced break will be applied continuously to the target system. After the target system is turned on, the S1C33xxx chip is reset. The S1C33xxx chip enters debug mode and starts communication with the S5U1C33001H. If multiple power on/reset cycles occur caused by switch bounce when the target is turned on, the communication between the S5U1C33001H and the target system may be disconnected after the second reset. Design the target system so that switch bounce does not occur and the system starts up only once. Furthermore, if the reset is applied with either the power or the oscillator in an unstable state (for example, if the reset is applied within the first few ms after the power is turned on), the S1C33xxx chip operation will also be unstable. In this case the system will not enter debug mode and communication between the S5U1C33001H and the target system will not be possible. Apply the reset only after an adequate stabilization time has elapsed. Refer to the "S1C33xxx Technical Manual" for more information on the reset operation.

- **If the S5U1C33001H is turned on after the target system power is turned on:**
  When the S5U1C33001H is turned on, it issues a forcible break to the free-running target system. The S1C33xxx chip enters debug mode and starts communication with the S5U1C33001H. If a boot program was not loaded into ROM, the S1C33xxx chip cannot respond to the forced break since the S1C33xxx chip is in the runaway state, so communication is impossible. Load a boot program that operates correctly into boot ROM so that the target system will not be in the runaway state.

• **If the initial connection operation fails**

In this case, add a reset switch to the target system and start the system in the following sequence:
(1) Turn the target system on
(2) Hold down the reset switch on the target system and turn the S5U1C33001H on
(3) Release the reset switch to clear the reset state.

This will allow the system to operate reliably. This is because this sequence reliably reproduces the conditions in the "If the S5U1C33001H is turned on after the target system power is turned on" item above. If it is not possible to connect, install a reset switch on the target system. We recommend adding the reset switch at the system design stage.

• **RESET/WRITE switch on the S5U1C33001H**

Besides turning power on and off, the S5U1C33001H can be reset using the on-board RESET/WRITE switch.
Also the RESET/WRITE switch changes the signal output from the TARGET_RESET pin in the target system power supply connector (see next section).

■ POWER SUPPLY AND RESET SIGNAL OUTPUT TO THE TARGET SYSTEM

The S5U1C33001H includes the capability of supplying power and outputting a reset signal to the target system.

Table 10 Pin Assignment of the Target System Power Supply Connector

Pin No.	Pin name	Function
1	Vcc (3.3 V)	Target system power supply pin (3.3 V)
2	Vcc (1.8 V)	Target system power supply pin (1.8 V)
3	Vss	Target system power supply pin (GND)
4	TARGET_VCC	Target system power supply monitor input pin
5	Vss	Target system power supply pin (GND)
6	TARGET_RESET	Target system reset output pin

The TARGET_VCC pin is used for the target power monitoring function. When this function is enabled, the S5U1C33001H stops supplying power to the target system if the input voltage of the TARGET_VCC pin goes to 0 V.

The TARGET_RESET signal changes according to the RESET/WRITE switch operation.
When the RESET/WRITE switch is off: 3.3 V is output
When the RESET/WRITE switch is on: 0 V is output

When using the TARGET_RESET signal for resetting the target system, a reset circuit as shown in the figure below is recommended.

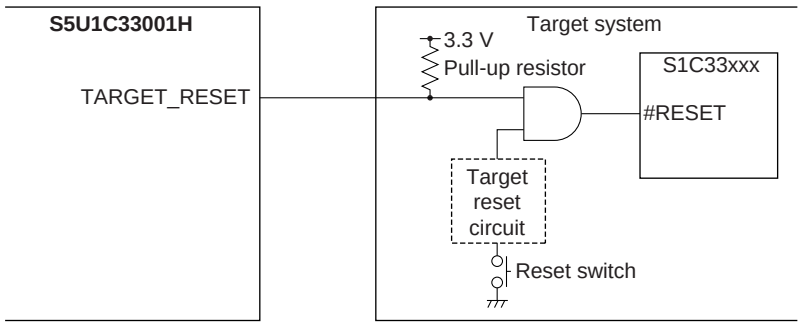


Figure 16 Example of Reset Circuit

The RESET/WRITE switch operation does not affect supplying power to the target system.
Note that the maximum current that can be supplied is 10 mA.

* The S5U1C33001H power supply circuit includes a PolySwitch (resettable fuse) that shuts down the power supply to the target system when the output current exceeds 500 mA (it is automatically reset when the output current returns within the range).

■ FIRMWARE UPDATE PROCEDURE

The S5U1C33001H has a firmware update function using the debugger (gdb.exe). The following show the procedure to update the S5U1C33001H firmware.

Note: Before the firmware can be updated, the USB driver must be installed.

(1) Connect the S5U1C33001H with the target system using the 4-pin, 10-pin or 30-pin cable.
The firmware update function is implemented as a part of target system debug function. Therefore, the target system must be connected to the S5U1C33001H, although the target system is not actually used for the update.

(2) Connect the S5U1C33001H with the host computer using the USB cable.

(3) Invoke the debugger (gdb.exe)

- To invoke at the command prompt:
```
>start /w gdb -nw --c33_no_ver
```
- To invoke from gwb33
Just click the [GDB] button with nothing selected.

(4) Enter the commands shown below after the debugger starts up.
```
(gdb) target icd usb
(gdb) c33 firmupdate icd33dmt.sa
```

(5) The update operation has completed when the OK LED is lit.
Terminate the debugger (gdb.exe) and turn the S5U1C33001H off then on again.

■ TARGET SYSTEM CONNECTION TEST

The S5U1C33001H can diagnose whether it can communicate with the target system or not when the debugger (gdb.exe) starts up. This function can be omitted or executed using the DIP switch.

• Omitting the target system connection test

If SW6 of the DIP switch located on the S5U1C33001H front panel is placed in the ON (lower) position, the S5U1C33001H omits the target system connection test when the debugger (gdb.exe) starts up.

• Executing the target system connection test

If SW6 of the DIP switch located on the S5U1C33001H front panel is placed in the OPEN (upper) position, the S5U1C33001H executes the target system connection test when the debugger (gdb.exe) starts up.
When the target system connection test is completed normally, the following is displayed on the debugger screen:

```
Connecting with target ... done
CPU type and debug unit address setting ... done
Initializing ............. done
CPU type and debug unit address setting ... done
CPU cold resetting ....... done
Target connection test ... done   ← display when terminated normally.
ICD hardware version   ... 4.1      ("omitted" will appear if the connection test is omitted.)
ICD software version   ... 4.2
CPU type and debug unit address setting ... done
CPU cold resetting ....... done
Boot address ............. 0xc00000
```

Note: Always be sure to turn off the power to the S5U1C33001H before setting the DIP switch.
If an error message is displayed after the target system connection test is executed, failure may have occurred in the target system. Check to see whether the target system is working properly or not.
Normally enable the target system connection test.

■ PRECAUTIONS

● Restrictions on Debugging

The debugging using the S5U1C33001H is subject to the restrictions specified below.

• Operation of the internal peripheral circuits

The peripheral circuits of the S1C33xxx stop operating when the debugger (gdb.exe) on the host computer is ready to accept commands, that is, unless the target program is running. For this reason, the peripheral circuits do not operate in real time when the target program is executed in the single-step mode. For details on single-step execution, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

• Interrupts when the target program is not running

If an interrupt request to the C33 core is generated by the target system when the target program is not running, interrupt processing is paused. The interrupt that has been paused is serviced immediately before the target program is executed or immediately after one instruction is executed after the debugger (gdb.exe) on the host computer has directed that the target program be executed.

• Interrupts when the target program is executed in a single step

If an interrupt request to the C33 core is generated by the target system during single-step execution of the target program, including functions and subroutines (STEP), the interrupt request is paused. During single-step execution of the target program, not including functions and subroutines (NEXT), an interrupt request received within a function or subroutine is serviced without being paused and an interrupt received in other parts of the program is paused as with the STEP command. The interrupt that has been paused is serviced immediately before the target program is executed or immediately after one instruction is executed after the debugger (gdb.exe) on the host computer has directed that the target program be executed. For details on single-step execution (STEP and NEXT), refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

• Break functions

The S5U1C33001H and the debugger support multiple break functions.
The timing at which a break occurs is classified into the following two categories depending on the break function.

(1) Break functions that suspend the target program before the instruction in which the cause of the break occurred is executed
    Software PC break, hardware PC break

(2) Break functions that suspend the target program after several instructions are executed from the instruction in which the cause of the break occurred
    Data break, area break, bus break

For details on break functions, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

• Trace function

Note that the trace function in the S5U1C33001H has the following restrictions. Furthermore, refer to the technical information of the trace function ("Implementation of the PC Trace Function" and "Implementation of the Bus Trace Function").

(1) The S5U1C33001H PC trace function can trace only instruction execution cycle information. Note that data access (read/write) information cannot be traced. When the target system uses the S1C33 model in which a C33 core that supports the bus trace function is embedded, data read/write information can be traced.

(2) Be aware that the trace function cannot be used when it is disabled using the DIP switch. For enabling/disabling the trace function using the DIP switch, refer to "Trace function setting" in the "DIP Switches" section.

(3) There are certain functional limitations to the PC trace function that are due to the analysis procedure being implemented in software. Refer to "Implementation of the PC Trace Function" section and the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)" for more information.

(4) Be aware that the trace function cannot be used when using the 4-pin cable to connect the target system to the S5U1C33001H.

(5) Be aware that the bus trace function cannot be used when using the 10-pin cable to connect the target system to the S5U1C33001H.

• Counts of the execution counter

The S5U1C33001H's execution counter is normally subject to the errors shown in the table below. These errors must be taken into account when calculating execution times. Note that execution and break overhead adds the prefetch cycles for two additional instructions, making the counters usable for only relatively long intervals. For short intervals, use the clock cycle counts from the trace function.

Table 11 Execution Counter Error

Execution counter	Count error
Cycle counter	±4 bus clock cycles
µs-unit time counter	±50 ns
Second-unit time counter	±1 µs

• Reserved areas in the internal peripheral circuits (C33 STD/Mini core)

When reserved areas in the internal peripheral circuits are displayed using the S5U1C33001H's data display function, note that, depending on the type of microcomputer, the last value read by the C33 core that is held in the bus latch circuit inside the chip may be displayed.

• Operating clock of the S5U1C33001H (C33 STD/Mini core)

When execution of the target program is suspended, the operating clock of S1C33xxx chip on the target system is forcibly switched to the high-speed clock even if the C33 core may have been operated with the low-speed clock while the target program was executed. For this reason, if the high-speed clock is turned off by the target program when the target system is being operated with the low-speed clock, the S5U1C33001H will be unable to operate normally after execution of the target program is suspended.

• Area 2 of S1C33xxx (C33 STD/Mini/ADV core)

Area 2 of the S1C33xxx (0x0060000 to 0x007FFFF) is reserved as a dedicated area for the programs that operate the S5U1C33001H. Therefore, no device can be mapped to this area using a parameter file, and data cannot be written to this area when the target program is suspended or being executed. If the contents of area 2 are rewritten, the S5U1C33001H will be unable to operate normally. For details on the parameter file, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

• Concurrent use of the S5U1C330M2S debug monitor

The S5U1C330M2S cannot be used with the S5U1C33001H simultaneously for debugging the target program.

The S5U1C33001H can be used for debugging the S5U1C330M2S. In this case, the S5U1C330M2S must be implemented using "mon33ice.lib" (library supplied with the S5U1C330M2S package). However, only the following parts in the S5U1C330M2S can be debugged:

- Part for initial connection to the debugger (gdb.exe)
- Confirming the command functions except for execution commands
- Part for communication to the debugger (gdb.exe)

• Reset sequence

The sequence from when the S5U1C33001H is powered on until the execution of the target program is executed is entirely different from that of the actual S1C33xxx chip.

However, a sequence for the reset requests input from the target system while the target program is being executed is the same as that for the actual S1C33xxx chip.

Regarding the reset sequence in the actual S1C33xxx chip, refer to the "S1C33xxx Technical Manual".

• Break functions when a reset request is accepted

If a cold reset request from the target system is accepted when the target system is being executed, the hardware PC break and data break functions are disabled until execution of the target program is suspended.

In the case of a hot reset request, there is no such restriction.

• I/O memory dump by the S5U1C33001H

Note that some S1C33xxx peripheral circuits may change the control register status due to their specifications when the I/O memory is read using the memory dump function of the S5U1C33001H or when the target program execution is suspended.

For details on the memory dump function, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

• **Parameter file**

Make sure the parameter file for the S5U1C33001H is set correctly according to the specifications of the target system. For details on the parameter file, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

• **Models with cache memory embedded**

The debugging operations performed while program execution is suspended rewrite the contents of the cache memory. Furthermore, the software PC break function cannot be used when the cache is used under conditions other than that listed in the table below. Use the hardware break function in such cases.

Table 12 Cache Usage Conditions to Use Software PC Break

	Instruction cache	Data cache
1	OFF	OFF
2	ON	ON
3	OFF	ON (write through mode only)

• **Models with MMU embedded**

The debugging operations performed while program execution is suspended access physical addresses in the default setting.

Although there are some restrictions, it can be changed so that logical addresses will be accessed. For more information, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

● Differences from the Actual IC

The S5U1C33001H is different from the actual IC in the way specified below. If this difference is not taken into consideration in an application, the program may not operate normally in the actual IC.

• **Register initialization**

When the actual IC is powered on, the contents of all registers except the PC (program counter) and PSR (processor status register) are indeterminate and retain the immediately preceding values after a reset, whereas in the S5U1C33001H all registers are initialized when the debugger on the host computer is invoked. At this time, the registers are initialized with the following data:

For all cores

PSR (processor status register):	0x00000000
AHR, ALR (arithmetic operation high/low registers):	0xAAAAAAAA
R0 through R15 (general-purpose registers):	0xAAAAAAAA

For C33 STD, Mini and PE cores

PC (program counter):	0x00C00000 (Note)
SP (stack pointer):	0x0AAAAAA8

For C33 ADV core

PC (program counter):	0x20000000 (Note)
LCO (loop count register):	0x00000000
LSA (loop start address register):	0x00000000
LEA (loop end address register):	0x00000000
SOR (shift out register):	0x00000000
TTBR (trap table base register):	0x20000000
DP (data pointer):	0x00000000
USP (user stack pointer):	0x00000000
SSP (supervisor stack pointer):	0x00000000

For this reason, never create a program that depends on the initialized value. However, for reset input from the target system when the target program is being executed, the S5U1C33001H retains the immediately preceding values, as with the actual IC. For details on each register, refer to the C33 Core Manual.

Note: The PC initial value is decided according to the setting value of the trap table base register (boot address). Refer to the "S1C33xxx Technical Manual" for details on the trap table base register (TTBR).

● Usage Precautions

When using the S5U1C33001H, observe the precautions described below.

• Connecting and disconnecting equipment

Before attaching or removing the target system and cables, and setting the DIP switch and jumper, be sure to turn off the power to the host computer, S5U1C33001H, and target system. Failure to take this precaution may result in equipment malfunction.

• Powering on/off

After turning off the power to the S5U1C33001H, wait at least 10 seconds before turning the power on again. If the power is turned on immediately after it is turned off, the S5U1C33001H may not be initialized correctly in a power-on reset, and may cause a malfunction.

• Connecting the target system

The signals connected to the S5U1C33001H are very high-speed signals, so the target connector must be mounted within 5 cm from the S1C33xxx. If there is more distance between the connector and the S1C33xxx chip, the S5U1C33001H may not work properly. Furthermore, be sure to use one of the supplied 30-pin, 10-pin and 4-pin cables for connecting the target system to the S5U1C33001H. Using two cables (30-pin and 10-pin or 4-pin cables) simultaneously or using another cable may cause a malfunction.

• Operation of the S5U1C33001H system

The S5U1C33001H can work by connecting a target system in which the actual S1C33xxx chip is mounted. Since the S5U1C33001H package does not include any board equivalent to a target system, please prepare separately.

• Wiring between the S1C33xxx chip and target connector

When wiring the S1C33xxx chip to the target connector for connecting the S5U1C33001H, insert a 33 Ω resistor in series between the S1C33xxx chip DSIO pin and the connector. This resistor must be placed as close to the S1C33xxx chip as possible. If the reset line is not connected, the system can be operated without this 33 Ω resistor. However, we recommend inserting this resistor to prevent malfunctions. The other pins are connected directly. The total length of the line must be under 5 cm. Forcible breaks are applied by inputting a low-level to the DSIO pin. Although this signal is pulled up through an about 100 kΩ internally, when not debugging, we recommend either removing the 33 Ω resistor to reduce noise and other problems or pulling this line up to the V_{DD} level (the core voltage).

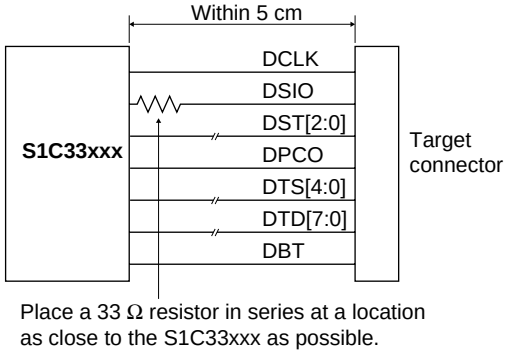


Figure 17 Wiring between S1C33xxx and Target Connector

• Reset request

Do not reset the target system while the target program execution is suspended as the S5U1C33001H will be unable to operate normally.

• Notes on target system power supply

The allowable voltage range for the signals input from the target system is 0 to 3.6 V. The S5U1C33001H may fail if voltages that exceed this range are input. Therefore, target systems to be connected to the S5U1C33001H must be designed so that voltages outside this range are not applied. Take special care in designing the target system power supply, and design the target system so that overvoltages are not applied to the S5U1C33001H when the target system power supply is turned on or off.

• Notes on S5U1C33001H power supply

When using the S5U1C33001H, install circuit breakers that automatically disconnect both conductors in the local power mains, and connect the S5U1C33001H power supply line to a power line protected in that manner.

■ TECHNICAL INFORMATION

● Flash Programmer Function

The flash programmer function allows writing data such as programs, which have been downloaded into the S5U1C33001H's internal flash memory, to the target system's flash memory directly from the S5U1C33001H.
The flash programmer function is enabled by setting DIP switches 1 and 7 on the S5U1C33001H. The function is disabled in the default setting.

Setting the DIP switch:
Refer to the "DIP Switches" section.

Download procedure and commands used:
Refer to the "Flash Writer Commands" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

Procedure for converting files to be written to the target system flash memory into Motorola S3 files:
Refer to the "Creating ROM Data" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)". See also the above manual for details on creating program files for writing to flash memory on the target system.

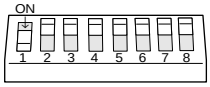
• Downloading to the target system flash memory

(1) Turn the S5U1C33001H on.

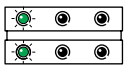
(2) Turn the target system on.

(3) Invoke the debugger (gdb.exe) and download the write data file to the S5U1C33001H.

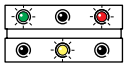
(4) When the download has completed, turn off the S5U1C33001H and target system, and set the S5U1C33001H DIP switches to "flash programmer enabled (erase and write mode)".



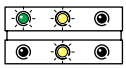
(5) Turn on the S5U1C33001H and target system, and set the RESET/WRITE switch to the ON position.



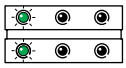
(6) The ERASE LED lights and the target system flash memory is erased. The BUSY LED lights during the erase operation.


(during erasing)

(7) The WRITE LED lights and data are written to the target system flash memory. If the data being written is a small program, this operation will complete instantly. The BUSY LED also lights during the write operation.


(during writing)

(8) The OK LED lights when the operation has completed normally.

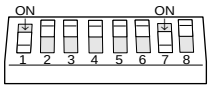


(9) If another target system is to be programmed, the S5U1C33001H's power must be turned off before programming that target system.
(completed)

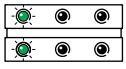
• Verifying the data downloaded to the target system

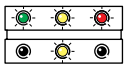
(1) Perform steps (1) to (8) in the download procedure shown above to write data. This operation is not necessary when verifying data immediately after the download has completed.

(2) When the download has completed, turn off the S5U1C33001H and target system, and set the S5U1C33001H DIP switches to "flash programmer enabled (verify mode)".

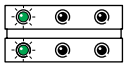


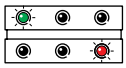
(3) Turn on the S5U1C33001H and target system, and set the RESET/WRITE switch to the ON position.
This starts verification of the downloaded data. The BUSY LED lights during the verify operation.




(during verification)

(4) The OK LED lights when the written data matches.
If the written data does not match, the ERROR LED lights.


(OK)


(error)

● Core Sync Simple Logic Analyzer Function

This function allows tracing of up to 14 arbitrary signals in the same cycles as the core clock. The traced information can be displayed with the core status. When using an evaluation board for development, any signals on the board may be traced. Before internal signals can be traced, when using an FPGA for development, they should be output from the unused pins.

The supplied 30-pin coaxial cable is used for tracing. Therefore, the signals to be traced must be output from the DTD7–0, DTS4–0, and DBT pins of the supplied 30-pin connector. (Use a connector conversion board, such as the CK-4 manufactured by Sunhayato Corp., to attach the 0.5 mm pitch 30-pin connector on the 2.54 mm pitch board.)

For operations of the debugger and the debug commands, refer to the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

Usage example:

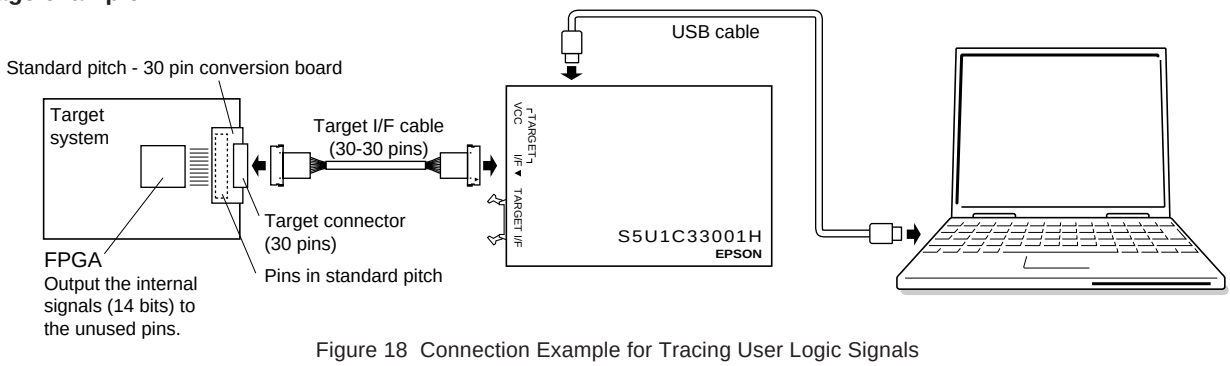


Figure 18 Connection Example for Tracing User Logic Signals

Example of traced result display:

```
Cycle   Address  Code Unassemble              Clk     DTD        DTS    UIN  Method File             Line ...

0000122 006003D4 0200 pushn    %r0           0000147 00010000   01000   0    DPC (../common/sys.c) 00083...
                                             0000148 10010000   01000   0
                                             0000149 11110000   01000   0
                                             0000150 10011000   01000   0
0000121 006003D6 2E60 ld.w     %r0,%r6       0000151 11010000   01010   0    DPC
                                             0000152 00010000   01010   0
                                             0000153 01010000   01010   0
                                             0000154 00010000   01010   0
0000120 006003D8 6C16 ld.w     %r6,0x1       0000155 01010000   01010   0    DPC (../common/sys.c) 00087...
0000119 006003DA 2E07 ld.w     %r7,%r0       0000156 00010000   01010   0    DPC
```

Traced 14-bit signals

● Implementation of the PC Trace Function

The PC trace function is implemented by a method that allows the debugger (gdb.exe) to analyze the target program flow using the information delivered on the DST0, DST1, DST2 and DPCO signals output from the S1C33xxx chip, and the target program information loaded into the debugger. The debugger obtains the absolute addresses information required for analyzing the target program flow from the following status.

(1) The PC (program counter) value when the target program restarts executing from suspended status
(2) Trace trigger set-up address when a trace trigger is generated
(3) The PC (program counter) value that is output on the 27- or 31-cycle DPCO signal (PC signal for debugging)

Furthermore, target program execution information is output on the DST0–DST2 signals (status signals for debugging). The debugger analyzes execution and branches successively using this absolute address and execution information, and displays the trace information. Therefore, there are some restrictions in the PC trace function. For details on the PC trace function and operating procedures, see the "Debugger" section in the "S5U1C33001C Manual (C Compiler Package for S1C33 Family)".

● **Implementation of the Bus Trace Function**

The S1C33xxx bus trace function monitors the internal bus to obtain the bus address, data, bus master, read/write, access size and access type (instruction fetch cycle or data access cycle) information when a read or write access is generated. The sampled information is divided and output from the DTS4–0 and DTD7–0 pins to the S5U1C33001H in maximum 8 cycles.

If a new bus access is generated while the current bus information is being output from the target system, the S1C33xxx will suspend outputting the current trace information and will start outputting the new trace information.

Therefore, frequent bus accesses reduce bus trace information to be obtained.

In this case, select a bus trace option for compressing the trace data. The information compress circuit in the S1C33xxx compresses the bus trace data before outputting, thus the amount of bus trace information that can be obtained will be increased.

Furthermore, the items to be traced can be narrowed by specifying a command parameter so that the desired bus trace information to be obtained will be increased.

The bus trace function does not affect the real-time program execution.

■ TROUBLESHOOTING

The following shows the problems attributable to the hardware:

Table 13 Troubleshooting

Symptom	Cause/remedy
The EMU/ERASE LED that has lit when the S5U1C33001H is turned on does not go out.	(1) Is the target system turned on? → Turn the target system on. (2) Is the target system connected with the S5U1C33001H? → See the "Connecting the Target System" section in this manual and check to see if the target system is connected correctly. (3) Was the power-on sequence correct? → See the "Start-up Method (Power-on Sequence)" section in this manual and turn the power on in the correct order.
The following message appears when the debugger (gdb.exe) in the host computer is invoked: Cannot open ICD33 usb driver.	(1) Is the S5U1C33001H turned on? → Place the power switch on the rear panel of the S5U1C33001H in the "I" position. (2) Is the S5U1C33001H connected to the host computer correctly? → See the "Connecting the S5U1C33001H and the Host Computer" section in this manual and check to see if the target system is connected correctly. (3) Was the debugger (gdb.exe) restarted after resetting the S5U1C33001H while the debugger is running? → See "Notes" in the " Start-up Method (Power-on Sequence)" section in this manual.
The following message suddenly appears while the target program is being executed by the debugger (gdb.exe) in the host computer: Break by external break. Program received signal SIGINT, Interrupt.	This problem is caused by low-level noise on the DSIO signal of the target or when the BRK IN pin on the front panel goes GND level. (1) Is the target system connected with a cable other than the one supplied, or is the supplied cable used with extension cables? → You are advised to use the supplied cable. If it cannot be used then use extension cables that are as short as possible and shield them in order to avoid occurrence of low-level noise on the DSIO signal. (2) Is there any conductive material near the BRK IN pin on the front panel? → Remove the conductive material.
The bus trace function is enabled, but trace information cannot be obtained at all.	(1) Is the 30-pin coaxial cable connected to the target system? → Use the 30-pin coaxial cable.
The operation is unstable.	(1) Is the DCLK-core clock ratio (SW2 and 3) set correctly? → See the "DIP Switches" section in this manual and make sure that the setting is correct. (2) Is the DSIO output level (SW8) set correctly? → See the "DIP Switches" section in this manual and make sure that the setting is correct. (3) Is the target system connected with a cable other than the one supplied, or is the supplied cable used with extension cables? → You are advised to use the supplied cable. If it cannot be used then use extension cables that are as short as possible and shield them in order to avoid occurrence of low-level noise on the DSIO signal. (4) Are the 30-pin coaxial cable and 10-pin or 4-pin cable used simultaneously? → Use either only the 30-pin coaxial cable, 10-pin or 4-pin cable.

■ SPECIFICATIONS

Table 14 Specifications

No.	Components	Items	Specifications	Remarks
1	S5U1C33001H	Dimensions	183 mm (W) × 125.7 mm (L) × 36.6 mm (H)	Rubber feet included
		Input voltage	100 V to 240 V AC (50 Hz/60 Hz)	
		Power consumption	10 W, max.	
2	USB cable	Length	2 m	
		Connectors	S5U1C33001H side: Standard-B type Host PC side: Standard-A type	
3	AC cable	Length	1.8 m	
		Plug type	Bipolar with ground	
4	Target system interface cables (30 pins, 10 pins, 4 pins)	Length	Approx. 15 cm	Shielded cable
5	Target system connectors (30 pins, 10 pins, 4 pins)	Connectors	30-pin (L angle): SL01-30L3 (KEL) 10-pin (straight): J3654-6002SC (3M) 10-pin (L angle): J3654-5002SC (3M) 4-pin (straight): HKP04M5S (Honda) 4-pin (L angle): HKP04M5LS (Honda)	
6	Target system power supply cable (6 pins)	Length	Approx. 15 cm	
7	Target system power supply connector (6 pins)	Connector	6-pin (L angle): IL-6P-S3FP2 (JAE)	

■ OPERATING ENVIRONMENT

Table 15 Operating Environment

No.	Items	Specifications	Remarks
1	Operating temperature	5 to 35°C	
2	Storage temperature	-10 to 60°C	
3	Operating humidity	35 to 80%	
4	Storage humidity	20 to 90%	No condensation
5	Resistance to vibration	Operating: 0.25 m/S^2	
		Transportation: 1 m/S^2	

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