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S1C88655

8-bit Single Chip Microcomputer

- Original Architecture Core CPU
- Built-in Font Data ROM for Kanji and Hangul (512K bytes)
- Dot-matrix LCD Driver (128 × 64)

■ DESCRIPTION

The S1C88655 is an 8-bit microcomputer for portable equipment with an LCD display that has a built-in LCD controller/driver and a font data ROM. The LCD controller/driver contains an LCD drive power supply circuit and can drive a maximum of 128 × 64-dot LCD panel. The S1C88655 has a built-in large-capacity ROM that can store various font data*. This microcomputer features low-voltage (1.8 V) and high-speed (8.2 MHz) operations as well as low-current consumption, for instance, 2 µA in standby mode (HALT mode during 32 kHz operation with crystal oscillation circuit). The S1C88655 is suitable for display modules such as PDAs and data banks that require an general-purpose LCD driver in conventional systems as well as portable CD/MD players and solid audio equipment with low-power and small-footprint.

* Fonts supported
- 12 × 12-dot Japanese font (JIS level-1 and level-2, other characters)
- 12 × 12-dot Korean font (KSX1001)

Please contact Seiko Epson for more information on the fonts provided.

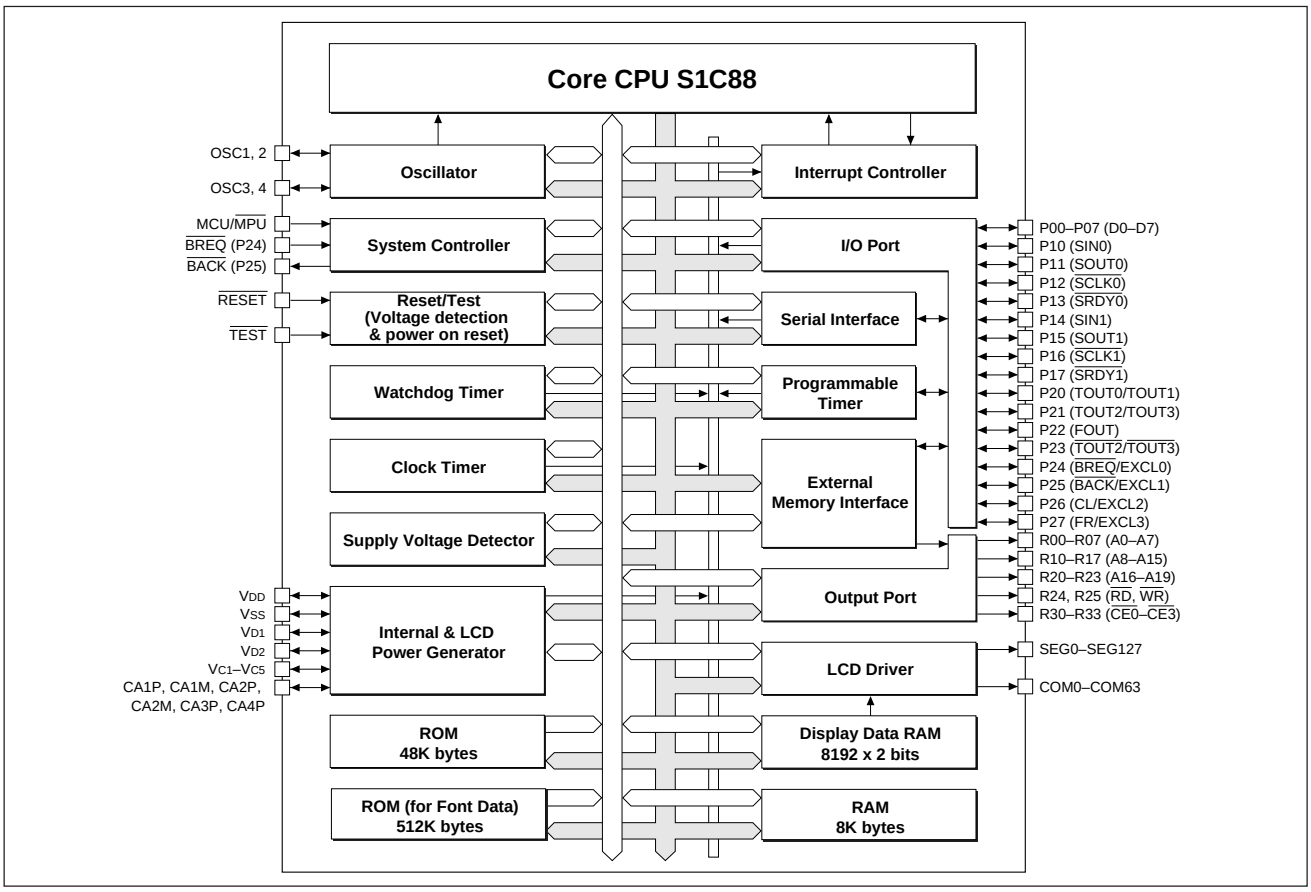
■ FEATURES

- Core CPU ..... S1C88 (MODEL3) CMOS 8-bit core CPU
- Main (OSC3) oscillation circuit ..... Crystal/ceramic oscillation circuit 8.2MHz (Max.)
  or CR oscillation circuit 2.2MHz (Max.)*1
- Sub (OSC1) oscillation circuit ..... Crystal oscillation circuit 32.768kHz (Typ.)
  or CR oscillation circuit 200kHz (Max.)*1
- Instruction set ..... 608 types (usable for multiplication and division instructions)
- Min. instruction execution time 0.244µsec/8.2MHz (2-clock)
- Internal ROM capacity ..... Program ROM: 48K bytes
  Font data ROM: 512K bytes (can be used for a program/data ROM)
- Internal RAM capacity ..... RAM: 8K bytes
  Display memory: 2K bytes (8192 bits per screen × 2)
- Bus line ..... Address bus: 20 bits
  Data bus: 8 bits
  $\overline{CE}$ signal: 4 bits (1MB addressing range × 4)
  $\overline{WR}$ signal: 1 bit
  $\overline{RD}$ signal: 1 bit
  (also usable as general output ports when not used for the bus)
- Output port ..... 0–3 bits (when the external bus is used)
  26 bits (when the external bus is not used)
- I/O port ..... 16 bits (when the external bus is used)
  24 bits (when the external bus is not used)
  (CMOS or Schmitt inputs*1, With or without pull-up resistors*1)
- Serial interface ..... 2 ch. (optional clock synchronous system or asynchronous system)
- Timer ..... Programmable timer: 16 bits (8 bits × 2) 4 ch.
  (with PWM waveform, SIF and LCD driver clock output functions)
  Clock timer: 1 ch.
- LCD driver ..... Dot matrix type
  128 segments × 64 commons
  Built-in LCD power supply circuit (boosting: ×2, ×3, ×4, and ×5)

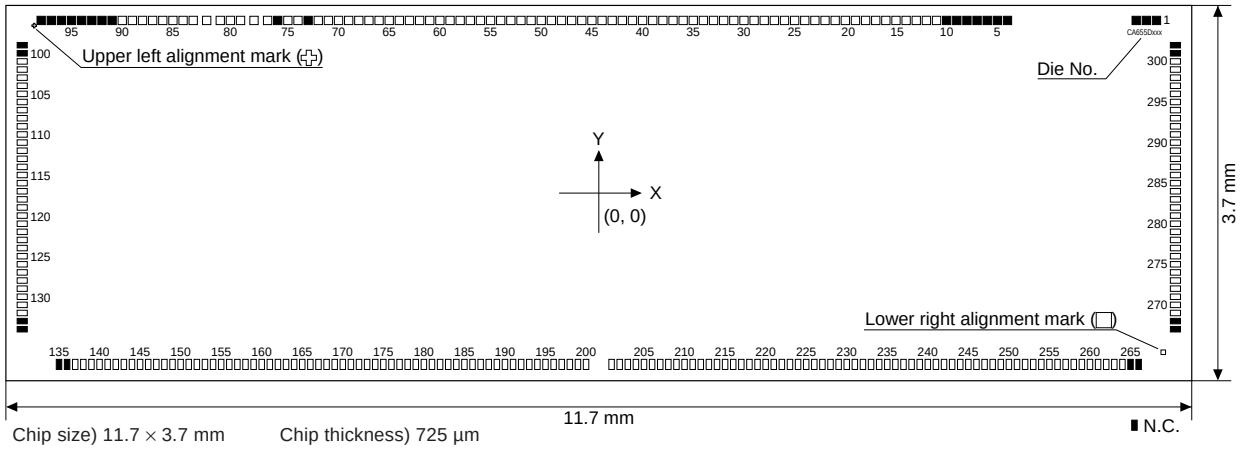
- Watchdog timer ..... Overflow cycle (1–4 seconds) and output signal (NMI or reset) are selectable*1
- Supply voltage detection (SVD) circuit .... 13 value programmable (1.8V to 2.7V)
- Reset voltage detection (RVD) circuit ..... Supply voltage level reset (1.6V, power-on reset function) with enable/disable option*1
- Interrupt ..... External interrupt: Input port interrupt (with noise rejector) 1 system (8 types)
  Internal interrupt: Timer interrupt 5 systems (20 types)
  Serial interface interrupt 2 systems (6 types)
- Supply voltage ..... 1.8V to 3.6V (internal voltage V_{D1} = 1.8V)
- Current consumption (Typ.) ..... SLEEP mode: 0.7µA
  HALT mode (32kHz OSC1 crystal, LCD OFF): 2µA
  HALT mode (32kHz OSC1 CR, LCD OFF): 7µA
  Run mode (32kHz OSC1 crystal, LCD OFF): 5µA
  Run mode (2MHz OSC3 CR, LCD OFF): 350µA
  Run mode (8MHz OSC3 ceramic, LCD OFF): 800µA
  RVD circuit operating current (V_{DD} = 3.6V): 1.5µA
  SVD circuit operating current (V_{DD} = 3.6V): 5µA
  LCD circuit operating current
  (V_{DD} = 3.0V, OSC1 = 32kHz, triple boosted, V_{C5} = 8V)
  White screen displayed: 50µA
  Checker pattern displayed: 120µA
- Supply form ..... AU-bump chip or TCM*2

*1: Can be selected with mask option
*2: TCM (Tape Carrier Module): FPC (Flexible Printed Circuit) modules that include peripheral circuit parts as well as the IC main unit

■ BLOCK DIAGRAM



■ PAD LAYOUT DIAGRAM



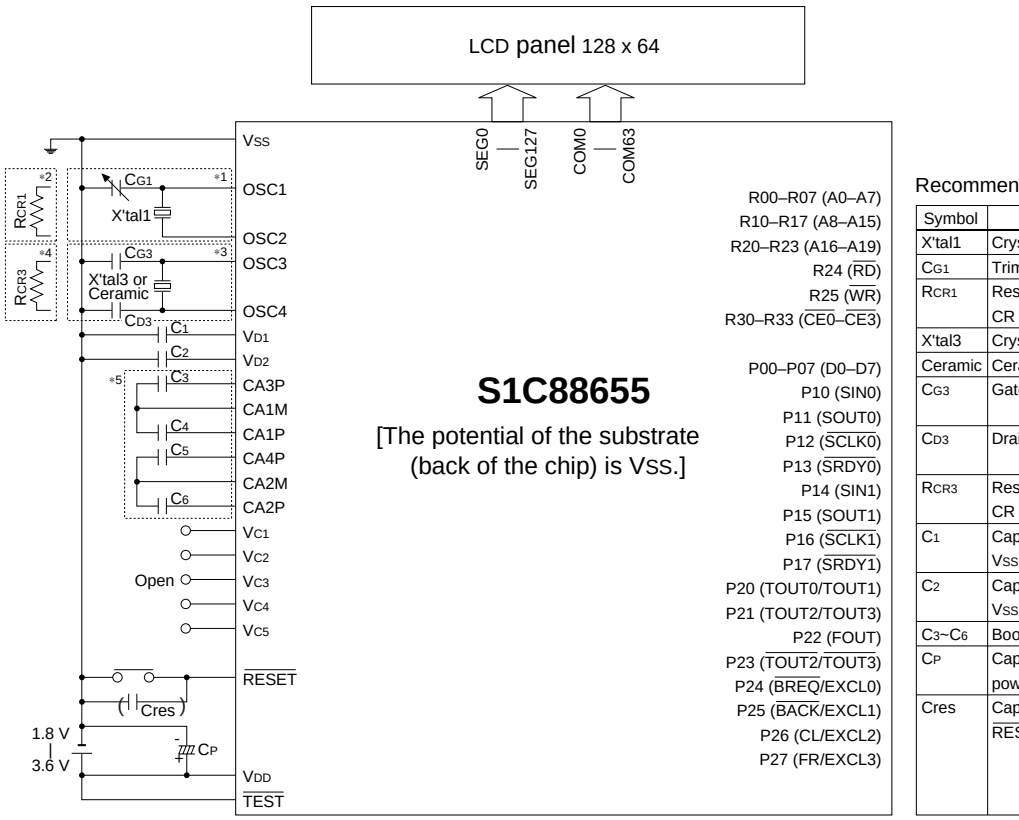
Chip size) 11.7 × 3.7 mm Chip thickness) 725 µm
Pad size) No. 1–98: 82 × 82 µm, No. 99–134: 100 × 54 µm, No. 135–266: 54 × 100 µm, No. 267–302: 100 × 54 µm
Bump pitch) No. 1–98: 100 µm (Min.), No. 99–302: 80 µm (Min.) Bump height) 22.5 µm
Alignment mark coordinates) Upper left corner: (-5560, 1660), Lower right corner: (5569, -1569)

■ PIN DESCRIPTION

Pad name	Pad No.	In/Out	Init*	Function
V_{DD}	11, 38, 74	–	–	Power supply (+) terminal
V_{SS}	14, 21, 75, 85	–	–	Power supply (GND) terminal
V_{D1}	15	–	–	Internal logic and oscillation system voltage regulator output terminal
V_{D2}	80, 84	–	–	LCD circuit power voltage booster output terminal
V_{C1}–V_{C5}	86–90	–	–	LCD drive voltage output terminals
CA1P, CA1M, CA2P, CA2M, CA3P, CA4P	79, 78, 83, 82, 77, 81	–	–	LCD voltage booster capacitor connection terminals
OSC1	13	I	I	OSC1 oscillation input terminal (select crystal/CR oscillation by mask option)
OSC2	12	O	O	OSC1 oscillation output terminal
OSC3	17	I	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation by mask option)
OSC4	16	O	O	OSC3 oscillation output terminal
MCU/$\overline{MPU}$	19	I	I (Pull-up)	MCU/MPU mode setup terminal
R00–R07/A0–A7	47–54	O	O (H)	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	55–62	O	O (H)	Output terminals (R10–R17) or address bus (A8–A15)
R20–R23/A16–A19	63–66	O	O (H)	Output terminals (R20–R23) or address bus (A16–A19)
R24/$\overline{RD}$	67	O	O (H)	Output terminal (R24) or read signal output terminal ($\overline{RD}$)
R25/$\overline{WR}$	68	O	O (H)	Output terminal (R25) or write signal output terminal ($\overline{WR}$)
R30–R33/$\overline{CE0}$–$\overline{CE3}$	69–72	O	O (H)	Output terminals (R30–R33) or chip enable signal output terminals ($\overline{CE0}$–$\overline{CE3}$)
P00–P07/D0–D7	46–39	I/O	I (Pull-up)	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN0	37	I/O	I (Pull-up)	I/O terminal (P10) or serial I/F Ch. 0 data input terminal (SIN0)
P11/SOUT0	36	I/O	I (Pull-up)	I/O terminal (P11) or serial I/F Ch. 0 data output terminal (SOUT0)
P12/$\overline{SCLK0}$	35	I/O	I (Pull-up)	I/O terminal (P12) or serial I/F Ch. 0 clock I/O terminal ($\overline{SCLK0}$)
P13/$\overline{SRDY0}$	34	I/O	I (Pull-up)	I/O terminal (P13) or serial I/F Ch. 0 ready signal output terminal ($\overline{SRDY0}$)
P14/SIN1	33	I/O	I (Pull-up)	I/O terminal (P14) or serial I/F Ch. 1 data input terminal (SIN1)
P15/SOUT1	32	I/O	I (Pull-up)	I/O terminal (P15) or serial I/F Ch. 1 data output terminal (SOUT1)
P16/$\overline{SCLK1}$	31	I/O	I (Pull-up)	I/O terminal (P16) or serial I/F Ch. 1 clock I/O terminal ($\overline{SCLK1}$)
P17/$\overline{SRDY1}$	30	I/O	I (Pull-up)	I/O terminal (P17) or serial I/F Ch. 1 ready signal output terminal ($\overline{SRDY1}$)
P20/TOUT0/TOUT1	29	I/O	I (Pull-up)	I/O terminal (P20) or programmable timer underflow signal output terminal (TOUT0/TOUT1)
P21/TOUT2/TOUT3	28	I/O	I (Pull-up)	I/O terminal (P21) or programmable timer underflow signal output terminal (TOUT2/TOUT3)
P22/FOUT	27	I/O	I (Pull-up)	I/O terminal (P22) or clock output terminal (FOUT)
P23/$\overline{TOUT2}$/$\overline{TOUT3}$	26	I/O	I (Pull-up)	I/O terminal (P23) or programmable timer underflow inverted signal output terminal ($\overline{TOUT2}$/$\overline{TOUT3}$)
P24/BREQ/EXCL0	25	I/O	I (Pull-up)	I/O terminal (P24), bus request signal input terminal ($\overline{BREQ}$) or programmable timer external clock input terminal (EXCL0)
P25/$\overline{BACK}$/EXCL1	24	I/O	I (Pull-up)	I/O terminal (P25), bus acknowledge signal output terminal ($\overline{BACK}$) or programmable timer external clock input terminal (EXCL1)
P26/$\overline{CL}$/EXCL2	23	I/O	I (Pull-up)	I/O terminal (P26), LCD clock output terminal (CL) or programmable timer external clock input terminal (EXCL2)
P27/FR/EXCL3	22	I/O	I (Pull-up)	I/O terminal (P27), LCD frame signal output terminal (FR) or programmable timer external clock input terminal (EXCL3)
COM0–COM63	132–101, 269–300	O	O (L)	LCD common output terminals
SEG0–SEG127	137–264	O	O (L)	LCD segment output terminals
$\overline{RESET}$	20	I	I (Pull-up)	Initial reset input terminal
$\overline{TEST}$	18	I	I (Pull-up)	Test input terminal

* (Pull-up): Pulled up (Hi-Z when Gate Direct is selected by mask option), (H): HIGH level output, (L): LOW level output

■ BASIC EXTERNAL CONNECTION DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz
C_{G1}	Trimmer capacitor	0–25 pF
R_{CR1}	Resistor for CR oscillation	1.5 MΩ
X'tal3	Crystal oscillator	4 MHz
Ceramic	Ceramic oscillator	4 MHz
C_{G3}	Gate capacitor	15 pF (Crystal) 30 pF (Ceramic)
C_{D3}	Drain capacitor	15 pF (Crystal) 30 pF (Ceramic)
R_{CR3}	Resistor for CR oscillation	39 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{D2}	1.0–4.7 µF
C_3~C_6	Booster capacitor	1.0–4.7 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF (Not required when the reset voltage detection circuit is used.)

∗1: OSC1 = Crystal oscillation ∗2: OSC1 = CR oscillation
∗3: OSC3 = Crystal or Ceramic oscillation ∗4: OSC3 = CR oscillation
∗5: Example for $V_{D2} = 5 \times V_{DD}$ ($V_{D2} > V_{C5}$)
The external circuit configuration depends on the supply voltage and LCD drive voltage values.

Note: The above table is simply an example, and is not guaranteed to work.

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