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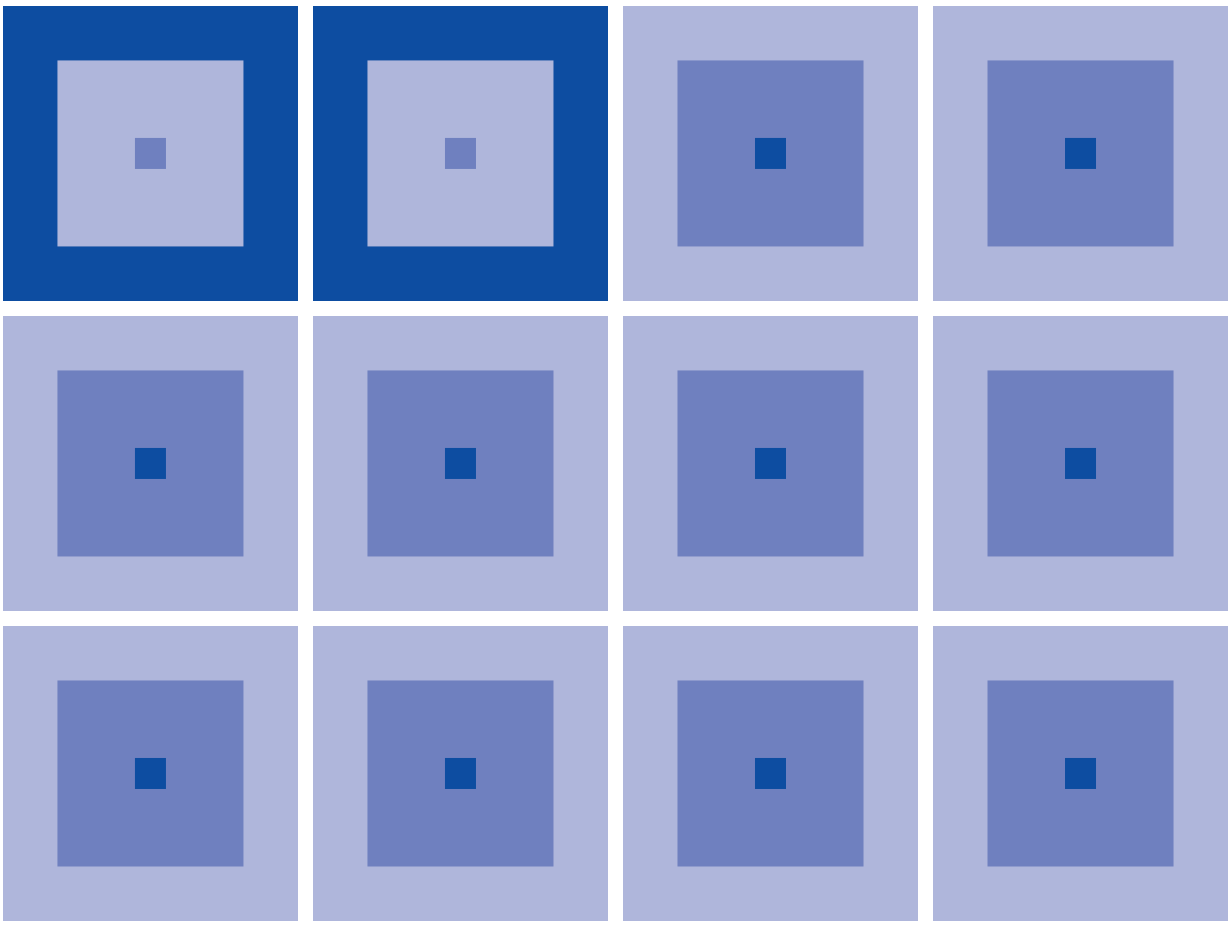
CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

S1C88655

Technical Manual

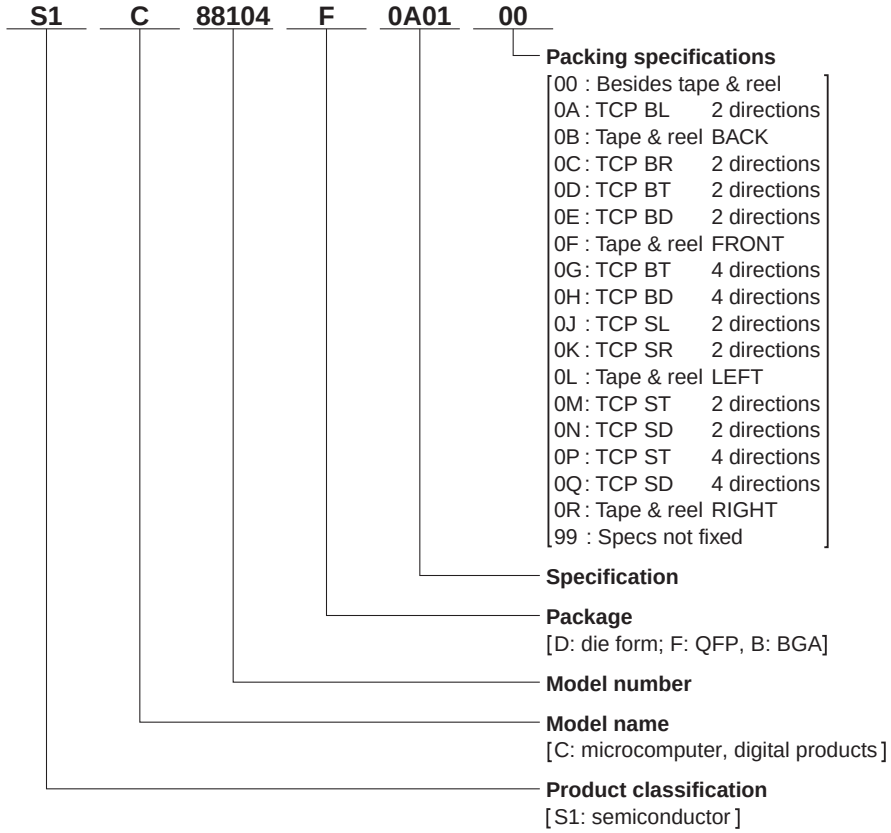
S1C88655 Technical Hardware



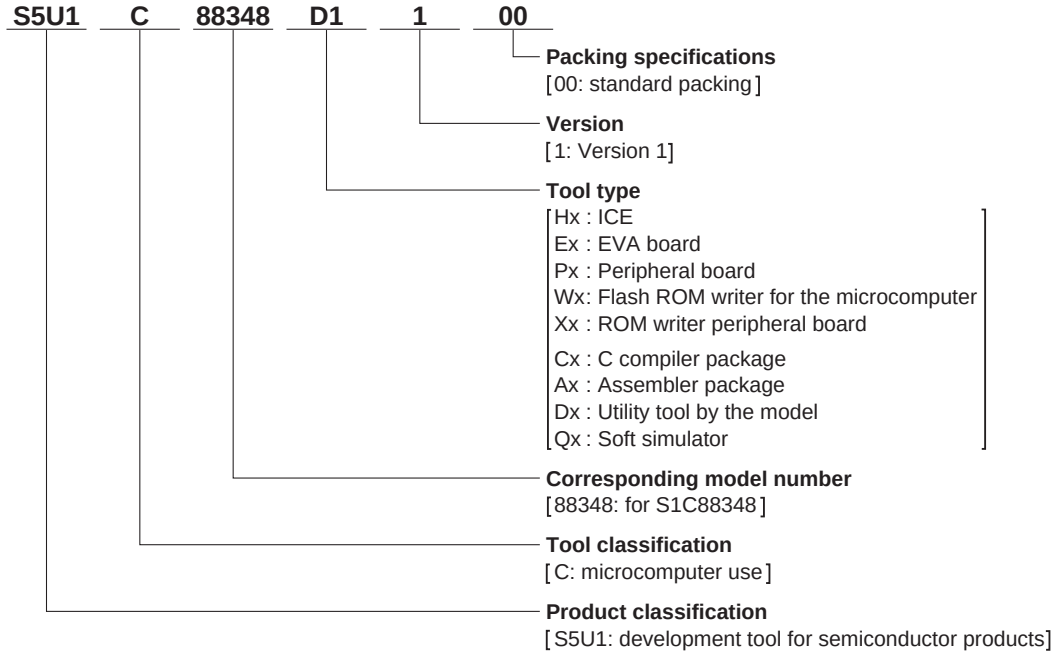
SEIKO EPSON CORPORATION

Configuration of product number

Devices



Development tools



Contents

1 INTRODUCTION

The S1C88655 is an 8-bit microcomputer for portable equipment with an LCD display that has a built-in LCD controller / driver and a font data ROM.
The LCD controller / driver contains an LCD drive power supply circuit and can drive a maximum of 128 × 64-dot LCD panel. The S1C88655 has a built-in large-capacity ROM that can store various font data*.
This microcomputer features low-voltage (1.8 V) and high-speed (8.2 MHz) operations as well as low-current consumption, for instance, 2 µA in standby mode (HALT mode with 32-kHz crystal oscillation).

The S1C88655 is suitable for display modules such as PDAs and data banks that require a general-purpose LCD driver in conventional systems as well as portable CD / MD players and solid audio equipment with low-power and a small-footprint.

* Fonts supported
1) 12 × 12-dot Japanese font
   (JIS level-1 and level-2, other characters)
2) 12 × 12-dot Korean font
   (KSX1001)

Please contact Seiko Epson for more information on the fonts provided.

1.1 Features

Table 1.1.1 lists the features of the S1C88655.

Table 1.1.1 Main features

Core CPU	S1C88 (MODEL3) CMOS 8-bit core CPU
Main (OSC3) oscillation circuit	Crystal oscillation circuit/ceramic oscillation circuit 8.2 MHz (Max.), or CR oscillation circuit 2.2 MHz (Max.)*1
Sub (OSC1) oscillation circuit	Crystal oscillation circuit 32.768 kHz (Typ.), or CR oscillation circuit 200 kHz (Max.)*1
Instruction set	608 types (usable for multiplication and division instructions)
Min. instruction execution time	0.244 µsec/8.2 MHz (2 clock)
Internal ROM capacity	48K bytes/program ROM 512K bytes/font data ROM Can be used for a program and data ROM when no font data is stored.
Internal RAM capacity	8K bytes/RAM 2K bytes/display data RAM (8192 bits per screen × 2)
Bus line	Address bus: 20 bits Data bus: 8 bits $\overline{CE}$ signal: 4 bits (1MB addressing range × 4) $\overline{WR}$ signal: 1 bit $\overline{RD}$ signal: 1 bit These pins can be used as general-purpose ports when not used for the bus.
Output port	0–3 bits (when the external bus is used) 26 bits (when the external bus is not used)
I/O port	16 bits (when the external bus is used) CMOS or Schmitt inputs*1 24 bits (when the external bus is not used) With or without pull-up resistors*1
Serial interface	2 channels Clock synchronous system or asynchronous system is selectable.
Timer	Programmable timer: 4 channels of 16-bit (8-bit × 2) timers (with PWM waveform, SIF and LCD driver clock output functions) Clock timer: 1 channel
LCD driver	Dot matrix type, 128 segments × 64 commons Built-in LCD power supply circuit that multiplies the source voltage by a factor of 2, 3, 4, or 5
Watchdog timer	Overflow cycle (1 to 4 seconds) and output signal (NMI or reset) are selectable*1
Supply voltage detection (SVD) circuit	13 values programmable (1.8–2.7 V)
Reset voltage detection (RVD) circuit	Supply voltage level reset (1.6 V, power-on reset function) with enable/disable option*1
Interrupt	External interrupt: Input interrupt (with noise rejector) 1 system (8 types) Internal interrupt: Timer interrupt 5 systems (20 types) Serial interface interrupt 2 systems (6 types)
Supply voltage	1.8–3.6 V (internal voltage V_{D1} = 1.8 V)
Current consumption	SLEEP mode: 0.7 µA (Typ.) HALT mode: 2 µA (Typ.) 32 kHz OSC1 crystal, LCD OFF 7 µA (Typ.) 32 kHz OSC1 CR, LCD OFF Run mode: 5 µA (Typ.) 32 kHz OSC1 crystal, LCD OFF 350 µA (Typ.) 2 MHz OSC3 CR, LCD OFF 800 µA (Typ.) 8 MHz OSC3 ceramic, LCD OFF RVD circuit operating current: 1.5 µA (Typ.) V_{DD} = 3.6 V SVD circuit operating current: 5 µA (Typ.) V_{DD} = 3.6 V LCD driver circuit operating current: 50 µA (Typ.) V_{DD} = 3.0 V, OSC1 = 32 kHz, triple boosted, V_{C5} = 8 V, white screen displayed 120 µA (Typ.) V_{DD} = 3.0 V, OSC1 = 32 kHz, triple boosted, V_{C5} = 8 V, checker pattern displayed
Supply form	AU-bump chip or TCM*2

*1 Selectable by mask option
*2 TCM (Tape Carrier Module): FPC (Flexible Printed Circuit) modules that include peripheral circuit parts as well as the IC main unit

1.2 Block Diagram

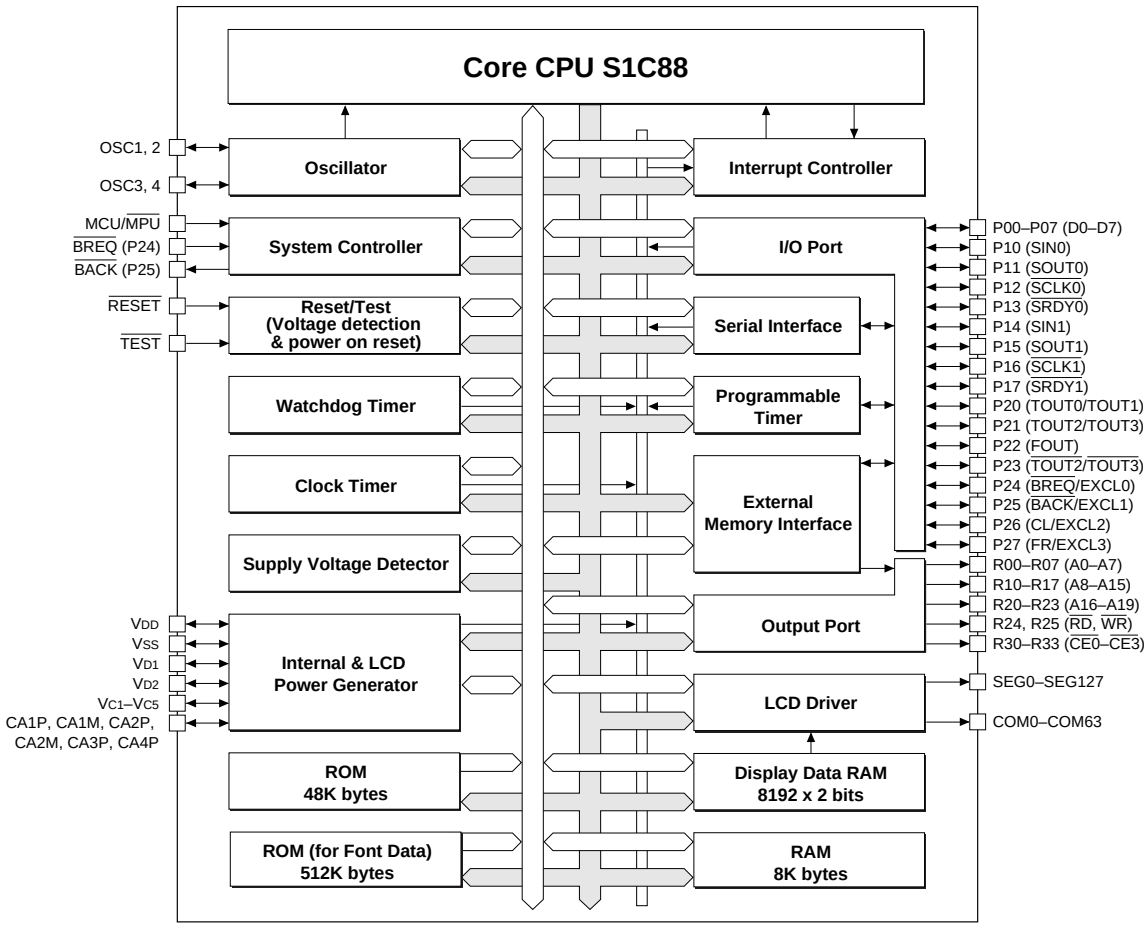
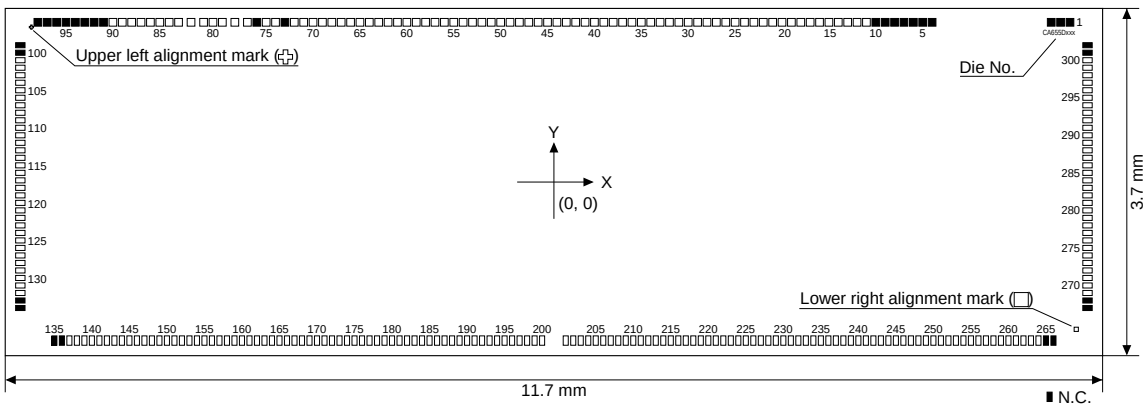


Fig. 1.2.1 S1C88655 block diagram

1.3 Pad Layout

1.3.1 Diagram of pad layout



Chip size) 11.7 × 3.7 mm Chip thickness) 725 µm
Pad size) No. 1–98: 82 × 82 µm, No. 99–134: 100 × 54 µm, No. 135–266: 54 × 100 µm, No. 267–302: 100 × 54 µm
Bump pitch) No. 1–98: 100 µm (Min.), No. 99–302: 80 µm (Min.) Bump height) 22.5 µm
Alignment mark coordinates) Upper left corner: (-5560, 1660), Lower right corner: (5569, -1569)

Fig. 1.3.1.1 Pad layout

1.3.2 Pad coordinates

Table 1.3.2.1 Pad coordinates (Unit: µm)

Pad		Coordinates		Pad		Coordinates		Pad		Coordinates		Pad		Coordinates	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	(N.C.)	5,502	1,702	77	CA3P	-3,268	1,702	153	SEG16	-3,886	-1,689	229	SEG92	2,366	-1,689
2	(N.C.)	5,402	1,702	78	CA1M	-3,402	1,702	154	SEG17	-3,806	-1,689	230	SEG93	2,446	-1,689
3	(N.C.)	5,302	1,702	79	CA1P	-3,535	1,702	155	SEG18	-3,726	-1,689	231	SEG94	2,526	-1,689
4	(N.C.)	4,032	1,702	80	V_{D2}	-3,635	1,702	156	SEG19	-3,646	-1,689	232	SEG95	2,606	-1,689
5	(N.C.)	3,932	1,702	81	CA4P	-3,735	1,702	157	SEG20	-3,566	-1,689	233	SEG96	2,686	-1,689
6	(N.C.)	3,832	1,702	82	CA2M	-3,869	1,702	158	SEG21	-3,486	-1,689	234	SEG97	2,766	-1,689
7	(N.C.)	3,732	1,702	83	CA2P	-4,002	1,702	159	SEG22	-3,406	-1,689	235	SEG98	2,846	-1,689
8	(N.C.)	3,632	1,702	84	V_{D2}	-4,102	1,702	160	SEG23	-3,326	-1,689	236	SEG99	2,926	-1,689
9	(N.C.)	3,532	1,702	85	V_{SS}	-4,202	1,702	161	SEG24	-3,246	-1,689	237	SEG100	3,006	-1,689
10	(N.C.)	3,432	1,702	86	V_{C1}	-4,302	1,702	162	SEG25	-3,166	-1,689	238	SEG101	3,086	-1,689
11	V_{DD}	3,332	1,702	87	V_{C2}	-4,402	1,702	163	SEG26	-3,086	-1,689	239	SEG102	3,166	-1,689
12	OSC2	3,232	1,702	88	V_{C3}	-4,502	1,702	164	SEG27	-3,006	-1,689	240	SEG103	3,246	-1,689
13	OSC1	3,132	1,702	89	V_{C4}	-4,602	1,702	165	SEG28	-2,926	-1,689	241	SEG104	3,326	-1,689
14	V_{SS}	3,032	1,702	90	V_{C5}	-4,702	1,702	166	SEG29	-2,846	-1,689	242	SEG105	3,406	-1,689
15	V_{D1}	2,932	1,702	91	(N.C.)	-4,802	1,702	167	SEG30	-2,766	-1,689	243	SEG106	3,486	-1,689
16	OSC4	2,832	1,702	92	(N.C.)	-4,902	1,702	168	SEG31	-2,686	-1,689	244	SEG107	3,566	-1,689
17	OSC3	2,732	1,702	93	(N.C.)	-5,002	1,702	169	SEG32	-2,606	-1,689	245	SEG108	3,646	-1,689
18	$\overline{\text{TEST}}$	2,632	1,702	94	(N.C.)	-5,102	1,702	170	SEG33	-2,526	-1,689	246	SEG109	3,726	-1,689
19	MCU/$\overline{\text{MPU}}$	2,532	1,702	95	(N.C.)	-5,202	1,702	171	SEG34	-2,446	-1,689	247	SEG110	3,806	-1,689
20	$\overline{\text{RESET}}$	2,432	1,702	96	(N.C.)	-5,302	1,702	172	SEG35	-2,366	-1,689	248	SEG111	3,886	-1,689
21	V_{SS}	2,332	1,702	97	(N.C.)	-5,402	1,702	173	SEG36	-2,286	-1,689	249	SEG112	3,966	-1,689
22	P27/FR/EXCL3	2,232	1,702	98	(N.C.)	-5,502	1,702	174	SEG37	-2,206	-1,689	250	SEG113	4,046	-1,689
23	P26/CL/EXCL2	2,132	1,702	99	(N.C.)	-5,689	1,458	175	SEG38	-2,126	-1,689	251	SEG114	4,126	-1,689
24	P25/$\overline{\text{BACK}}$/EXCL1	2,032	1,702	100	(N.C.)	-5,689	1,378	176	SEG39	-2,046	-1,689	252	SEG115	4,206	-1,689
25	P24/$\overline{\text{BREQ}}$/EXCL0	1,932	1,702	101	COM31	-5,689	1,298	177	SEG40	-1,966	-1,689	253	SEG116	4,286	-1,689
26	P23/$\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$	1,832	1,702	102	COM30	-5,689	1,218	178	SEG41	-1,886	-1,689	254	SEG117	4,366	-1,689
27	P22/FOUT	1,732	1,702	103	COM29	-5,689	1,138	179	SEG42	-1,806	-1,689	255	SEG118	4,446	-1,689
28	P21/TOUT2/TOUT3	1,632	1,702	104	COM28	-5,689	1,058	180	SEG43	-1,726	-1,689	256	SEG119	4,526	-1,689
29	P20/TOUT0/TOUT1	1,532	1,702	105	COM27	-5,689	978	181	SEG44	-1,646	-1,689	257	SEG120	4,606	-1,689
30	P17/$\overline{\text{SRDY1}}$	1,432	1,702	106	COM26	-5,689	898	182	SEG45	-1,566	-1,689	258	SEG121	4,686	-1,689
31	P16/$\overline{\text{SCLK1}}$	1,332	1,702	107	COM25	-5,689	818	183	SEG46	-1,486	-1,689	259	SEG122	4,766	-1,689
32	P15/SOUT1	1,232	1,702	108	COM24	-5,689	738	184	SEG47	-1,406	-1,689	260	SEG123	4,846	-1,689
33	P14/SIN1	1,132	1,702	109	COM23	-5,689	658	185	SEG48	-1,326	-1,689	261	SEG124	4,926	-1,689
34	P13/$\overline{\text{SRDY0}}$	1,032	1,702	110	COM22	-5,689	578	186	SEG49	-1,246	-1,689	262	SEG125	5,006	-1,689
35	P12/$\overline{\text{SCLK0}}$	932	1,702	111	COM21	-5,689	498	187	SEG50	-1,166	-1,689	263	SEG126	5,086	-1,689
36	P11/SOUT0	832	1,702	112	COM20	-5,689	418	188	SEG51	-1,086	-1,689	264	SEG127	5,166	-1,689
37	P10/SIN0	732	1,702	113	COM19	-5,689	338	189	SEG52	-1,006	-1,689	265	(N.C.)	5,246	-1,689
38	V_{DD}	632	1,702	114	COM18	-5,689	258	190	SEG53	-926	-1,689	266	(N.C.)	5,326	-1,689
39	P07/D7	532	1,702	115	COM17	-5,689	178	191	SEG54	-846	-1,689	267	(N.C.)	5,689	-1,342
40	P06/D6	432	1,702	116	COM16	-5,689	98	192	SEG55	-766	-1,689	268	(N.C.)	5,689	-1,262
41	P05/D5	332	1,702	117	COM15	-5,689	18	193	SEG56	-686	-1,689	269	COM32	5,689	-1,182
42	P04/D4	232	1,702	118	COM14	-5,689	-62	194	SEG57	-606	-1,689	270	COM33	5,689	-1,102
43	P03/D3	132	1,702	119	COM13	-5,689	-142	195	SEG58	-526	-1,689	271	COM34	5,689	-1,022
44	P02/D2	32	1,702	120	COM12	-5,689	-222	196	SEG59	-446	-1,689	272	COM35	5,689	-942
45	P01/D1	-68	1,702	121	COM11	-5,689	-302	197	SEG60	-366	-1,689	273	COM36	5,689	-862
46	P00/D0	-168	1,702	122	COM10	-5,689	-382	198	SEG61	-286	-1,689	274	COM37	5,689	-782
47	R00/A0	-268	1,702	123	COM9	-5,689	-462	199	SEG62	-206	-1,689	275	COM38	5,689	-702
48	R01/A1	-368	1,702	124	COM8	-5,689	-542	200	SEG63	-126	-1,689	276	COM39	5,689	-622
49	R02/A2	-468	1,702	125	COM7	-5,689	-622	201	SEG64	126	-1,689	277	COM40	5,689	-542
50	R03/A3	-568	1,702	126	COM6	-5,689	-702	202	SEG65	206	-1,689	278	COM41	5,689	-462
51	R04/A4	-668	1,702	127	COM5	-5,689	-782	203	SEG66	286	-1,689	279	COM42	5,689	-382
52	R05/A5	-768	1,702	128	COM4	-5,689	-862	204	SEG67	366	-1,689	280	COM43	5,689	-302
53	R06/A6	-868	1,702	129	COM3	-5,689	-942	205	SEG68	446	-1,689	281	COM44	5,689	-222
54	R07/A7	-968	1,702	130	COM2	-5,689	-1,022	206	SEG69	526	-1,689	282	COM45	5,689	-142
55	R10/A8	-1,068	1,702	131	COM1	-5,689	-1,102	207	SEG70	606	-1,689	283	COM46	5,689	-62
56	R11/A9	-1,168	1,702	132	COM0	-5,689	-1,182	208	SEG71	686	-1,689	284	COM47	5,689	18
57	R12/A10	-1,268	1,702	133	(N.C.)	-5,689	-1,262	209	SEG72	766	-1,689	285	COM48	5,689	98
58	R13/A11	-1,368	1,702	134	(N.C.)	-5,689	-1,342	210	SEG73	846	-1,689	286	COM49	5,689	178
59	R14/A12	-1,468	1,702	135	(N.C.)	-5,326	-1,689	211	SEG74	926	-1,689	287	COM50	5,689	258
60	R15/A13	-1,568	1,702	136	(N.C.)	-5,246	-1,689	212	SEG75	1,006	-1,689	288	COM51	5,689	338
61	R16/A14	-1,668	1,702	137	SEG0	-5,166	-1,689	213	SEG76	1,086	-1,689	289	COM52	5,689	418
62	R17/A15	-1,768	1,702	138	SEG1	-5,086	-1,689	214	SEG77	1,166	-1,689	290	COM53	5,689	498
63	R20/A16	-1,868	1,702	139	SEG2	-5,006	-1,689	215	SEG78	1,246	-1,689	291	COM54	5,689	578
64	R21/A17	-1,968	1,702	140	SEG3	-4,926	-1,689	216	SEG79	1,326	-1,689	292	COM55	5,689	658
65	R22/A18	-2,068	1,702	141	SEG4	-4,846	-1,689	217	SEG80	1,406	-1,689	293	COM56	5,689	738
66	R23/A19	-2,168	1,702	142	SEG5	-4,766	-1,689	218	SEG81	1,486	-1,689	294	COM57	5,689	818
67	R24/$\overline{\text{RD}}$	-2,268	1,702	143	SEG6	-4,686	-1,689	219	SEG82	1,566	-1,689	295	COM58	5,689	898
68	R25/$\overline{\text{WR}}$	-2,368	1,702	144	SEG7	-4,606	-1,689	220	SEG83	1,646	-1,689	296	COM59	5,689	978
69	R30/$\overline{\text{CE0}}$	-2,468	1,702	145	SEG8	-4,526	-1,689	221	SEG84	1,726	-1,689	297	COM60	5,689	1,058
70	R31/$\overline{\text{CE1}}$	-2,568	1,702	146	SEG9	-4,446	-1,689	222	SEG85	1,806	-1,689	298	COM61	5,689	1,138
71	R32/$\overline{\text{CE2}}$	-2,668	1,702	147	SEG10	-4,366	-1,689	223	SEG86	1,886	-1,689	299	COM62	5,689	1,218
72	R33/$\overline{\text{CE3}}$	-2,768	1,702	148	SEG11	-4,286	-1,689	224	SEG87	1,966	-1,689	300	COM63	5,689	1,298
73	(N.C.)	-2,868	1,702	149	SEG12	-4,206	-1,689	225	SEG88	2,046	-1,689	301	(N.C.)	5,689	1,378
74	V_{DD}	-2,968	1,702	150	SEG13	-4,126	-1,689	226	SEG89	2,126	-1,689	302	(N.C.)	5,689	1,458
75	V_{SS}	-3,068	1,702	151	SEG14	-4,046	-1,689	227	SEG90	2,206	-1,689	–	–	–	–
76	(N.C.)	-3,168	1,702	152	SEG15	-3,966	-1,689	228	SEG91	2,286	-1,689	–	–	–	–

1.3.3 Pad description

Table 1.3.3.1 Pad description

Pad name	Pad No.	In/Out	Init*	Function
V_{DD}	11, 38, 74	–	–	Power supply (+) terminal
V_{SS}	14, 21, 75, 85	–	–	Power supply (GND) terminal
V_{D1}	15	–	–	Internal logic and oscillation system voltage regulator output terminal
V_{D2}	80, 84	–	–	LCD circuit power voltage booster output terminal
V_{C1}–V_{C5}	86–90	–	–	LCD drive voltage output terminals
CA1P, CA1M, CA2P, CA2M, CA3P, CA4P	79, 78, 83, 82, 77, 81	–	–	LCD voltage booster capacitor connection terminals
OSC1	13	I	I	OSC1 oscillation input terminal (select crystal/CR oscillation by mask option)
OSC2	12	O	O	OSC1 oscillation output terminal
OSC3	17	I	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation by mask option)
OSC4	16	O	O	OSC3 oscillation output terminal
MCU/$\overline{\text{MPU}}$	19	I	I (Pull-up)	MCU/MPU mode setup terminal
R00–R07/A0–A7	47–54	O	O (H)	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	55–62	O	O (H)	Output terminals (R10–R17) or address bus (A8–A15)
R20–R23/A16–A19	63–66	O	O (H)	Output terminals (R20–R23) or address bus (A16–A19)
R24/$\overline{\text{RD}}$	67	O	O (H)	Output terminal (R24) or read signal output terminal ($\overline{\text{RD}}$)
R25/$\overline{\text{WR}}$	68	O	O (H)	Output terminal (R25) or write signal output terminal ($\overline{\text{WR}}$)
R30–R33/$\overline{\text{CE0}}$–$\overline{\text{CE3}}$	69–72	O	O (H)	Output terminals (R30–R33) or chip enable signal output terminals ($\overline{\text{CE0}}$–$\overline{\text{CE3}}$)
P00–P07/D0–D7	46–39	I/O	I (Pull-up)	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN0	37	I/O	I (Pull-up)	I/O terminal (P10) or serial I/F Ch. 0 data input terminal (SIN0)
P11/SOUT0	36	I/O	I (Pull-up)	I/O terminal (P11) or serial I/F Ch. 0 data output terminal (SOUT0)
P12/$\overline{\text{SCLK0}}$	35	I/O	I (Pull-up)	I/O terminal (P12) or serial I/F Ch. 0 clock I/O terminal ($\overline{\text{SCLK0}}$)
P13/$\overline{\text{SRDY0}}$	34	I/O	I (Pull-up)	I/O terminal (P13) or serial I/F Ch. 0 ready signal output terminal ($\overline{\text{SRDY0}}$)
P14/SIN1	33	I/O	I (Pull-up)	I/O terminal (P14) or serial I/F Ch. 1 data input terminal (SIN1)
P15/SOUT1	32	I/O	I (Pull-up)	I/O terminal (P15) or serial I/F Ch. 1 data output terminal (SOUT1)
P16/$\overline{\text{SCLK1}}$	31	I/O	I (Pull-up)	I/O terminal (P16) or serial I/F Ch. 1 clock I/O terminal ($\overline{\text{SCLK1}}$)
P17/$\overline{\text{SRDY1}}$	30	I/O	I (Pull-up)	I/O terminal (P17) or serial I/F Ch. 1 ready signal output terminal ($\overline{\text{SRDY1}}$)
P20/TOUT0/TOUT1	29	I/O	I (Pull-up)	I/O terminal (P20) or programmable timer underflow signal output terminal (TOUT0/TOUT1)
P21/TOUT2/TOUT3	28	I/O	I (Pull-up)	I/O terminal (P21) or programmable timer underflow signal output terminal (TOUT2/TOUT3)
P22/FOUT	27	I/O	I (Pull-up)	I/O terminal (P22) or clock output terminal (FOUT)
P23/$\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$	26	I/O	I (Pull-up)	I/O terminal (P23) or programmable timer underflow inverted signal output terminal ($\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$)
P24/$\overline{\text{BREQ}}$/EXCL0	25	I/O	I (Pull-up)	I/O terminal (P24), bus request signal input terminal ($\overline{\text{BREQ}}$) or programmable timer external clock input terminal (EXCL0)
P25/$\overline{\text{BACK}}$/EXCL1	24	I/O	I (Pull-up)	I/O terminal (P25), bus acknowledge signal output terminal ($\overline{\text{BACK}}$) or programmable timer external clock input terminal (EXCL1)
P26/CL/EXCL2	23	I/O	I (Pull-up)	I/O terminal (P26), LCD clock output terminal (CL) or programmable timer external clock input terminal (EXCL2)
P27/FR/EXCL3	22	I/O	I (Pull-up)	I/O terminal (P27), LCD frame signal output terminal (FR) or programmable timer external clock input terminal (EXCL3)
COM0–COM63	132–101, 269–300	O	O (L)	LCD common output terminals
SEG0–SEG127	137–264	O	O (L)	LCD segment output terminals
$\overline{\text{RESET}}$	20	I	I (Pull-up)	Initial reset input terminal
$\overline{\text{TEST}}$	18	I	I (Pull-up)	Test input terminal

* (Pull-up): Pulled up (Hi-Z when Gate Direct is selected by mask option), (H): HIGH level output, (L): LOW level output

1.4 Mask Option

Mask options shown below are provided for the S1C88655.
Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. Multiple specifications are available in each option item as indicated in the Option List.

Select the specifications that meet the target system and check the appropriate box.
The option selection is done interactively on the screen during function option generator winfog execution, using this option list as reference. Mask pattern of the IC is finally generated based on the data created by the winfog. Refer to the "S5U1C88000C Manual II" for details on the winfog.

PERIPHERAL CIRCUIT BOARD option list

The following shows the options for configuring the Peripheral Circuit Board (S5U1C88000P1 with S5U1C88655P2) installed in the ICE (S5U1C88000H5). The selections do not affect the IC's mask option.

A OSC1 SYSTEM CLOCK

☐ 1. Internal Clock
☐ 2. User Clock

When User Clock is selected, input a clock to the OSC1 terminal. When Internal Clock is selected, the clock frequency is changed according to the oscillation circuit selected by the IC's mask option.

B OSC3 SYSTEM CLOCK

☐ 1. Internal Clock
☐ 2. User Clock

When User Clock is selected, input a clock to the OSC3 terminal. When Internal Clock is selected, the clock frequency is changed according to the oscillation circuit selected by the IC's mask option.

S1C88655 mask option list

The following shows the option list for generating the IC's mask pattern. Note that the Peripheral Circuit Board installed in the ICE does not support some options.

1 OSC1 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. CR

The specification of the OSC1 oscillation circuit can be selected from among two types: "Crystal oscillation" and "CR oscillation". Refer to Section 8.4, "OSC1 Oscillation Circuit", for details.

2 OSC3 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. Ceramic
☐ 3. CR

The specification of the OSC3 oscillation circuit can be selected from among three types: "Crystal oscillation", "Ceramic oscillation" and "CR oscillation". Refer to Section 8.3, "OSC3 Oscillation Circuit", for details.

3 INPUT PORT PULL UP RESISTOR

- $\overline{\text{MCU}}$ / $\overline{\text{MPU}}$ .... ☐ 1. With Resistor ☐ 2. Gate Direct
- $\overline{\text{RESET}}$ ..... ☐ 1. With Resistor ☐ 2. Gate Direct

This mask option can select whether the pull-up resistors for the $\overline{\text{MCU}}$ / $\overline{\text{MPU}}$ and $\overline{\text{RESET}}$ terminals are used or not.

4 I/O PORT PULL UP RESISTOR

- P00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P04 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P05 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P06 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P07 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P11 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P12 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P13 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P14 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P15 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P16 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P17 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P20 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P21 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P22 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P23 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P24 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P25 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P26 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- P27 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

This mask option can select whether the pull-up resistor for the I/O port terminal (it works during input mode) is used or not. It is possible to select for each bit of the I/O ports. Refer to Chapter 10, "I/O Ports (P Ports)", for details.

5 I/O PORT INPUT I/F LEVEL

- P10 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P11 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P12 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P13 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P14 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P15 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P16 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P17 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P20 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P21 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P22 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P23 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P24 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P25 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P26 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt
- P27 ..... ☐ 1. CMOS Level ☐ 2. CMOS Schmitt

This mask option can select the interface level of the I/O (P) port from either the CMOS level or CMOS Schmitt level. It is possible to select for each bit of the I/O ports. Refer to Chapter 10, "I/O Ports (P Ports)", for details.

6 RESET VOLTAGE DETECTOR

☐ 1. Not Use
☐ 2. Use

This mask option can select whether the built-in reset voltage detection circuit is used or not. Refer to Section 5.1.2, "Reset voltage detector", for details.

7 WATCHDOG TIMER OVERFLOW CYCLE

☐ 1. Not Use
☐ 2. 32768 / f_{OSC1}
(1-sec cycle when f_{OSC1} = 32 kHz)
☐ 3. 65536 / f_{OSC1}
(2-sec cycle when f_{OSC1} = 32 kHz)
☐ 4. 131072 / f_{OSC1}
(4-sec cycle when f_{OSC1} = 32 kHz)

This mask option can select a watchdog timer overflow cycle. Refer to Chapter 14, "Watchdog Timer", for details.

8 WATCHDOG TIMER OVERFLOW SIGNAL

☐ 1. Interrupt (NMI)
☐ 2. Reset

This mask option can select whether the watchdog timer overflow signal is used to generate NMI or reset. Refer to Chapter 14, "Watchdog Timer", for details.

2 CPU

This chapter explains the CPU and operating mode.

2.1 Core CPU

The S1C88655 contains the S1C88 8-bit core CPU, so its register configuration, command set and other core features are similar to other family processors incorporating the S1C88.
See the "S1C88 Core CPU Manual" for the S1C88.

2.1.1 CPU model

The S1C88655 employs the Model 3 S1C88 CPU which has a maximum address space of 1M bytes × 4.

2.1.2 CC (customized condition flag)

The S1C88655 does not use the customized condition flag (CC) in the core CPU. Accordingly, it cannot be used as a branching condition for the conditional branching instruction (JRS, CARS).

2.2 MCU Mode and MPU Mode

The chip operating mode can be set to one of two settings using the MCU / $\overline{\text{MPU}}$ terminal.

2.2.1 MCU mode

Setting MCU mode: MCU/$\overline{\text{MPU}}$ terminal = HIGH

Set to this mode when using the internal ROM. With respect to areas other than internal memory, external memory can even be expanded. See Chapter 3, "Memory Map", for the memory map.

In the MCU mode, during initial reset, only systems in internal memory are activated. The internal program ROM is normally fixed as the top portion of the common program memory area (logical space 0000H–7FFFH). Exception processing vectors are assigned in the internal program ROM. Furthermore, the application initialization routines that start with reset exception processing must likewise be written to the internal program ROM. Since bus and other settings which correlate with external expanded memory can be executed in software, this processing is executed in the initialization routine written to the internal program ROM. Once these bus mode settings are made, external memory can be accessed. See Chapter 6, "System Controller and Bus Control", for setting bus mode.

When accessing the internal memory in this mode, the chip enable ($\overline{\text{CE}}$) and read ($\overline{\text{RD}}$) / write ($\overline{\text{WR}}$) signals are not output to external memory, and the data bus (D0–D7) goes into high impedance status (or pull-up status).
Consequently, in cases where addresses overlap in external and internal memory, the areas in external memory will be unavailable.

2.2.2 MPU mode

Setting MPU mode: MCU/$\overline{\text{MPU}}$ terminal = LOW

The internal ROM area is released to an external device. The internal ROM then becomes unusable and when this area is accessed, chip enable ($\overline{\text{CE}}$) and read ($\overline{\text{RD}}$) / write ($\overline{\text{WR}}$) signals are output to external memory and the data bus (D0–D7) become active. These signals are not output to an external device when other areas of internal memory are accessed.

In the MPU mode, the system is activated by external memory.

When using this mode, the exception processing vectors and initialization routine must be assigned within the common area (000000H–007FFFH).

2.2.3 Mask option

You can select whether the built-in pull-up resistor for the MCU / $\overline{\text{MPU}}$ terminal is used or not by mask option.

Input port pull-up resistor
MCU / $\overline{\text{MPU}}$ ..... ☐ With resistor ☐ Gate direct

Notes:
- *Setting of MCU/$\overline{\text{MPU}}$ terminal is latched at the rising edge of a reset signal input from the $\overline{\text{RESET}}$ terminal. Therefore, if the setting is to be changed, the $\overline{\text{RESET}}$ terminal must be set to LOW level once again.*
- *The data bus while the CPU accesses to the internal memory can be select into high-impedance status or pulled up to high using the pull-up control register and mask option. See Chapter 10, "I/O Ports (P Ports)", for details.*

3 MEMORY MAP

This chapter explains the memory configuration of the S1C88655.

3.1 MCU Single Chip Mode

The S1C88655 should be placed in single chip mode when it is used as a single chip microcomputer without an externally expanded memory. Since this mode uses the internal ROM, the system can be operated only in MCU mode. The MPU mode does not allow the IC to be placed in single chip mode. This mode does not need an external bus, so the terminals normally set for the external bus can be used as general-purpose output ports or I/O ports. See Chapter 6, "System Controller and Bus Control", for how to set single chip mode.

3.2 MCU Expansion Mode

The S1C88655 must be placed in expansion mode when it is used with an externally expanded memory up to 1M bytes × 4.
The internal ROM is enabled in the MCU mode, so external memory can be assigned to the area from 100000H to 4FFFFFH. See Chapter 6, "System Controller and Bus Control", for how to set expansion mode.

3.3 MPU Expansion Mode

The internal ROM area is released in the MPU mode, so external memory can be assigned to the area from 000000H to 3FFFFFH. However, the area from 00C000H to 00FFFFH is assigned to the internal memory and cannot be used to access an external device.

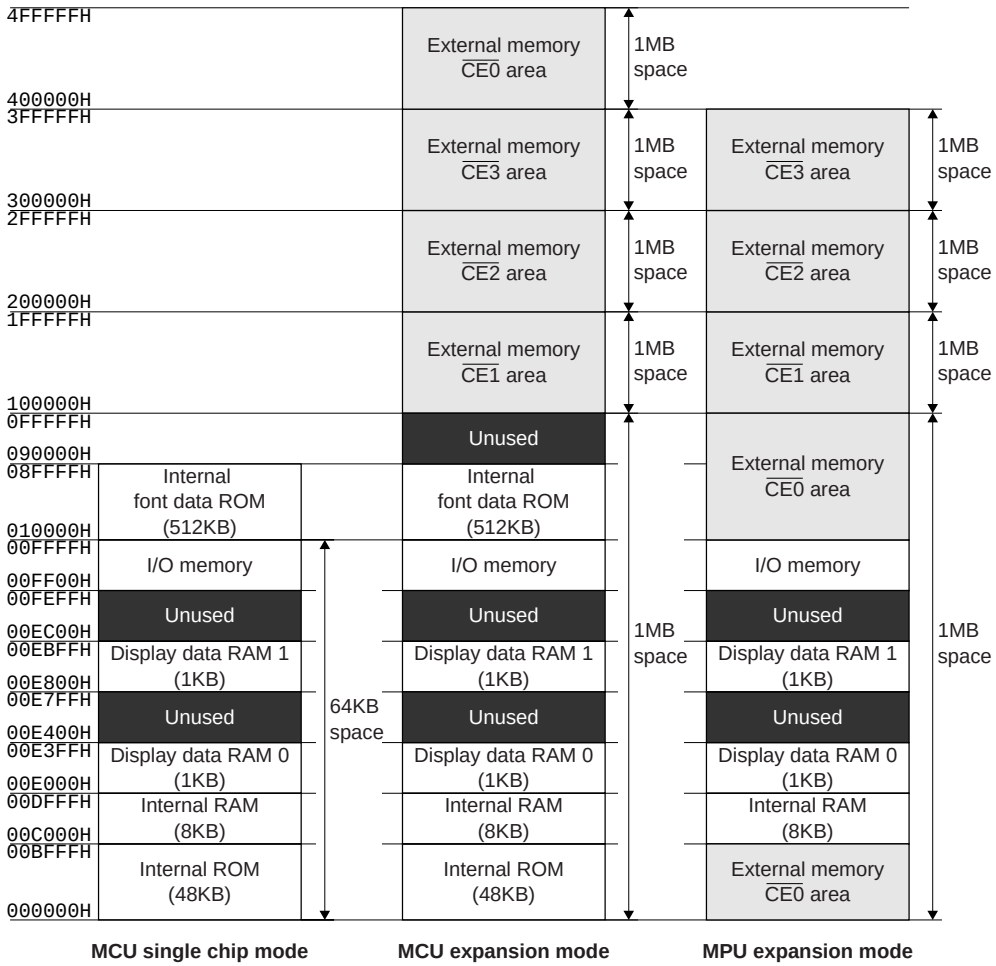


Fig. 3.1.1 Memory map

3.4 Internal Memory

The S1C88655 is equipped with a ROM and RAM as shown in Figure 3.1.1. Small-scale applications can be implemented in this chip alone.

3.4.1 Program ROM

The S1C88655 has a built-in 48K-byte program ROM. The ROM is allocated to 000000H–00BFFFH. This ROM areas can be released to external memory depending on the setting of the MCU/$\overline{\text{MPU}}$ terminal. (See Section 2.2, "MCU Mode and MPU Mode".)

3.4.2 RAM

The internal RAM capacity is 8K bytes and is allocated to 00C000H–00DFFFH.
Even when external memory which overlaps the internal RAM area is expanded, the RAM area is not released to external memory. Accesses to this area are always aimed at the internal RAM.

3.4.3 Display data RAM

The S1C88655 is equipped with an internal display data RAM which stores a display data for LCD driver. The display data RAM is allocated to 00E000H–00EBFFH. See Chapter 15, "LCD Driver", for details of the display data RAM. The display data RAM area cannot be released to external memory. Accesses to this area are always aimed at the display data RAM.

3.4.4 Font data ROM

The S1C88655 has a built-in ROM that can be used to store font data. The ROM capacity is 512K bytes and is allocated to 010000H–08FFFFH.
The entire ROM area when any font data is not used or the remaining area unused for font data can be used for a program and data storage area (see "Appendix B" for use of font data).
This ROM area can be released to external memory depending on the setting of the MCU/$\overline{\text{MPU}}$ terminal. (See Section 2.2, "MCU Mode and MPU Mode".)

3.5 I/O Memory

A memory mapped I/O method is employed in the S1C88655 for interfacing with the internal peripheral circuits. The peripheral circuit control bits and data registers are arranged in the data memory space, so normal memory access operations control the circuits and transfer data. The I/O memory is arranged in the area from 00FF00H to 00FFFFH. Even when external memory which overlaps the I/O memory area is expanded, the I/O memory area is not released to external memory. Accesses to this area are always aimed at the I/O memory.
The following shows the S1C88655 I/O memory map.

Table 3.5.1(a) I/O Memory map (00FF00H–00FF02H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00	D7	BUSMOD	Bus mode	Expansion	Single chip	0	R/W	
(MCU)	D6	CPUMOD	CPU mode	Maximum	Minimum	0	R/W	
	D5	–	–	–	–	–	–	Constantly "0" when
	D4	–	–	–	–	–	–	being read
	D3	CE3	$\overline{CE3}$ (R33)	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	In Single chip mode,
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	these setting are fixed
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	at DC output.
	D0	CE0	$\overline{CE0}$ (R30)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	0	R/W	
			$\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output					
00FF00	D7	BUSMOD	Bus mode	Expansion	–	1	R	Expansion mode only
(MPU)	D6	CPUMOD	CPU mode	Maximum	Minimum	0	R/W	
	D5	–	–	–	–	–	–	Constantly "0" when
	D4	–	–	–	–	–	–	being read
	D3	CE3	$\overline{CE3}$ (R33)	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30)	$\overline{CE0}$ enable	–	1	R	
			$\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output					
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5	< SP page allocatable address >	1	0	0	R/W	
	D4	SPP4	• Single chip mode: only 0 page	1	0	0	R/W	
	D3	SPP3	• Expansion mode: 0–27H page	1	0	0	R/W	
	D2	SPP2		1	0	0	R/W	
	D1	SPP1		1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	EBR	Bus release enable register P24	$\overline{BREQ}$	–	0	R/W	
			(P24 and P25 terminal specification) P25	$\overline{BACK}$	–			
	D6	WT2	Wait control register			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CLKCHG	CPU operating clock switch	OSC3	OSC1	1	R/W	∗1
	D1	SOSC3	OSC3 oscillation On/Off control	On	Off	1	R/W	∗2
	D0	SOSC1	OSC1 oscillation On/Off control	On	Off	1	R/W	∗3

WT2	WT1	WT0	Number of state
1	1	1	14
1	1	0	12
1	0	1	10
1	0	0	8
0	1	1	6
0	1	0	4
0	0	1	2
0	0	0	No wait

∗1 CLKCHG cannot be set to "0" when SOSC1 = "0" (OSC1 oscillation is OFF) and cannot be set to "1" when SOSC3 = "0" (OSC3 oscillation is OFF).

∗2 Cannot be turned OFF when the CPU is running with the OSC3 clock.

∗3 Cannot be turned OFF when the CPU is running with the OSC1 clock or the watchdog timer is enabled.

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the "00FF00H" and "00FF01H" addresses.

Table 3.5.1(b) I/O Memory map (00FF04H–00FF0AH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF04	D7	FOUTON	FOUT output control	On	Off	0	R/W	
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 1 1 1 f_{OSC3} / 8 1 1 0 f_{OSC3} / 4 1 0 1 f_{OSC3} / 2 1 0 0 f_{OSC3} / 1 0 1 1 f_{OSC1} / 8 0 1 0 f_{OSC1} / 4 0 0 1 f_{OSC1} / 2 0 0 0 f_{OSC1} / 1			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	–	–	–	–	–	–	Constantly "0" when being read
	D2	–	–	–	–	–	–	
	D1	–	–	–	–	–	–	
	D0	WDRST	Watchdog timer reset	Reset	No operation	–	W	
00FF08	D7	LCLK	CL output control	On	Off	0	R/W	
	D6	LFRM	FR output control	On	Off	0	R/W	
	D5	SEGREV	SEG output assignment control	Normal	Reverse	1	R/W	
	D4	COMREV	COM output assignment control	Normal	Reverse	1	R/W	
	D3	DSPAR	LCD display data RAM area selection	Display area 1	Display area 0	0	R/W	
	D2	DSPREV	Reverse display control	Normal	Reverse	1	R/W	
	D1	DSPC1	LCD display control DSPC1 DSPC0 Display 1 1 All dots ON 1 0 All dots OFF 0 1 Normal display 0 0 Display off			0	R/W	
	D0	DSPC0				0	R/W	
00FF09	D7	–	–	–	–	–	–	"0" when being read
	D6	LCDON	LCD driver circuit On/Off control	On	Off	0	R/W	
	D5	LBIAS	LCD bias selection	1/9 bias	1/7 bias	1	R/W	
	D4	VCON	$V_{C1–4}$ voltage generator On/Off control	On	Off	0	R/W	
	D3	VC5ON	V_{C5} voltage generator On/Off control	On	Off	0	R/W	
	D2	LBON	Supply voltage booster On/Off control	On	Off	0	R/W	
	D1	LCDCS1	Display timing generator control LCDCS1 LCDCS0 Source clock 1 1 P timer 5 1 0 f_{OSC1}/2 0 1 f_{OSC1}/1 0 0 Off			0	R/W	
	D0	LCDCS0				0	R/W	
00FF0A	D7	–	–	–	–	–	–	Constantly "0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	LRSEL2	V_{C5} voltage generator resistance ratio adjustment LRSEL2 LRSEL1 LRSEL0 Resistance ratio 1 1 1 Not allowed 1 1 0 8.69 1 0 1 8.13 1 0 0 7.20 0 1 1 6.46 0 1 0 5.60 0 0 1 4.84 0 0 0 4.06			0	R/W	
	D1	LRSEL1				0	R/W	
	D0	LRSEL0				0	R/W	

Table 3.5.1(c) I/O Memory map (00FF0BH–00FF15H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF0B	D7	–	–	–	–	–	–	Constantly "0" when
	D6	–	–	–	–	–	–	being read
	D5	LEV5	V_{C5} voltage control			0	R/W	
	D4	LEV4	LEV5 LEV4 LEV3 LEV2 LEV1 LEV0 Level			0	R/W	
	D3	LEV3	1 1 1 1 1 1 63			0	R/W	
	D2	LEV2	1 1 1 1 1 0 62			0	R/W	
	D1	LEV1	: : : : : : :			0	R/W	
	D0	LEV0	0 0 0 0 0 1 1 0 0 0 0 0 0 0			0	R/W	
00FF0C	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	SVDDT	SVD detection data	Low	Normal	0	R	
	D4	SVDON	SVD circuit On/Off	On	Off	0	R/W	
	D3	SVDS3	SVD criteria voltage setting			0	R/W	
	D2	SVDS2	SVDS3 SVDS2 SVDS1 SVDS0 Voltage (V)			0	R/W	
	D1	SVDS1	1 1 1 1 2.7 1 1 1 0 2.6			0	R/W	
	D0	SVDS0	1 1 0 1 2.5 : : : : : 0 0 1 1 1.8			0	R/W	
00FF10	D7	PSIF01	Serial interface 0 interrupt priority register	PSIF01 PSIF00		0	R/W	
	D6	PSIF00		PPT1 PPT0				
	D5	PPT1	Programmable timer 1–0 interrupt	PPT3 PPT2 Priority		0	R/W	
	D4	PPT0	priority register	PP21 PP20 level				
	D3	PPT3	Programmable timer 3–2 interrupt	1 1 Level 3		0	R/W	
	D2	PPT2	priority register	1 0 Level 2				
	D1	PP21	P20–P27 interrupt priority register	0 1 Level 1		0	R/W	
	D0	PP20		0 0 Level 0				
00FF11	D7	PPT5	Programmable timer 5–4 interrupt	PPT5 PPT4		0	R/W	
	D6	PPT4	priority register	PPT7 PPT6				
	D5	PPT7	Programmable timer 7–6 interrupt	PTM1 PTM0 Priority		0	R/W	
	D4	PPT6	priority register	PSIF11 PSIF10 level				
	D3	PTM1	Clock timer interrupt priority register	1 1 Level 3		0	R/W	
	D2	PTM0		1 0 Level 2				
	D1	PSIF11	Serial interface 1 interrupt priority register	0 1 Level 1		0	R/W	
	D0	PSIF10		0 0 Level 0				
00FF14	D7	EP27	P27 interrupt enable					
	D6	EP26	P26 interrupt enable					
	D5	EP25	P25 interrupt enable					
	D4	EP24	P24 interrupt enable	Interrupt	Interrupt			
	D3	EP23	P23 interrupt enable	enable	disable	0	R/W	
	D2	EP22	P22 interrupt enable					
	D1	EP21	P21 interrupt enable					
	D0	EP20	P20 interrupt enable					
00FF15	D7	ETC3	PTM3 compare match interrupt enable					
	D6	ETU3	PTM3 underflow interrupt enable					
	D5	ETC2	PTM2 compare match interrupt enable					
	D4	ETU2	PTM2 underflow interrupt enable	Interrupt	Interrupt			
	D3	ETC1	PTM1 compare match interrupt enable	enable	disable	0	R/W	
	D2	ETU1	PTM1 underflow interrupt enable					
	D1	ETU0	PTM0 underflow interrupt enable					
	D0	ETC0	PTM0 compare match interrupt enable					

Table 3.5.1(d) I/O Memory map (00FF16H–00FF1CH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF16	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	ESERR1	Serial I/F 1 (error) interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D4	ESREC1	Serial I/F 1 (receive) interrupt enable					
	D3	ESTRA1	Serial I/F 1 (transmit) interrupt enable					
	D2	ESERR0	Serial I/F 0 (error) interrupt enable			0	R/W	
	D1	ESREC0	Serial I/F 0 (receive) interrupt enable					
	D0	ESTRA0	Serial I/F 0 (transmit) interrupt enable					
00FF17	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	–	–	–	–	R	
	D3	ETM32	Clock timer 32 Hz interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable					
	D1	ETM2	Clock timer 2 Hz interrupt enable					
	D0	ETM1	Clock timer 1 Hz interrupt enable					
00FF18	D7	ETC7	PTM7 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU7	PTM7 underflow interrupt enable					
	D5	ETC6	PTM6 compare match interrupt enable					
	D4	ETU6	PTM6 underflow interrupt enable					
	D3	ETC5	PTM5 compare match interrupt enable					
	D2	ETU5	PTM5 underflow interrupt enable					
	D1	ETC4	PTM4 compare match interrupt enable					
	D0	ETU4	PTM4 underflow interrupt enable					
00FF1A	D7	FP27	P27 interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D6	FP26	P26 interrupt factor flag					
	D5	FP25	P25 interrupt factor flag					
	D4	FP24	P24 interrupt factor flag					
	D3	FP23	P23 interrupt factor flag					
	D2	FP22	P22 interrupt factor flag					
	D1	FP21	P21 interrupt factor flag					
	D0	FP20	P20 interrupt factor flag					
00FF1B	D7	FTC3	PTM3 compare match interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D6	FTU3	PTM3 underflow interrupt factor flag					
	D5	FTC2	PTM2 compare match interrupt factor flag					
	D4	FTU2	PTM2 underflow interrupt factor flag					
	D3	FTC1	PTM1 compare match interrupt factor flag					
	D2	FTU1	PTM1 underflow interrupt factor flag					
	D1	FTU0	PTM0 underflow interrupt factor flag					
	D0	FTC0	PTM0 compare match interrupt factor flag					
00FF1C	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	FSERR1	Serial I/F 1 (error) interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D4	FSREC1	Serial I/F 1 (receive) interrupt factor flag					
	D3	FSTRA1	Serial I/F 1 (transmit) interrupt factor flag					
	D2	FSERR0	Serial I/F 0 (error) interrupt factor flag			0	R/W	
	D1	FSREC0	Serial I/F 0 (receive) interrupt factor flag					
	D0	FSTRA0	Serial I/F 0 (transmit) interrupt factor flag					

Table 3.5.1(e) I/O Memory map (00FF1DH–00FF21H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF1D	D7	–	–	–	–	–	R	Constantly "0" when being read
	D6	–	–	–	–	–	R	
	D5	–	–	–	–	–	R	
	D4	–	–	–	–	–	R	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag	(R) Occurred	(R) Not occurred	0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag	(W) Reset	(W) No operation			
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					
00FF1E	D7	FTC7	PTM7 compare match interrupt factor flag	(R) Interrupt factor is occurred	(R) No interrupt factor is occurred	0	R/W	
	D6	FTU7	PTM7 underflow interrupt factor flag					
	D5	FTC6	PTM6 compare match interrupt factor flag					
	D4	FTU6	PTM6 underflow interrupt factor flag					
	D3	FTC5	PTM5 compare match interrupt factor flag					
	D2	FTU5	PTM5 underflow interrupt factor flag	(W) Reset	(W) No operation			
	D1	FTC4	PTM4 compare match interrupt factor flag					
	D0	FTU4	PTM4 underflow interrupt factor flag					
00FF20	D7	PRPRT1	Programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	Programmable timer 1 division ratio			0	R/W	
	D5	PST11				0	R/W	
	D4	PST10				0	R/W	
	D3	PRPRT0	Programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	Programmable timer 0 division ratio			0	R/W	
	D1	PST01				0	R/W	
	D0	PST00				0	R/W	
00FF21	D7	PRPRT3	Programmable timer 3 clock control	On	Off	0	R/W	
	D6	PST32	Programmable timer 3 division ratio			0	R/W	
	D5	PST31				0	R/W	
	D4	PST30				0	R/W	
	D3	PRPRT2	Programmable timer 2 clock control	On	Off	0	R/W	
	D2	PST22	Programmable timer 2 division ratio			0	R/W	
	D1	PST21				0	R/W	
	D0	PST20				0	R/W	

Programmable timer 1 division ratio

PST12	PST11	PST10	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 0 division ratio

PST02	PST01	PST00	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 3 division ratio

PST32	PST31	PST30	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Programmable timer 2 division ratio

PST22	PST21	PST20	(OSC3)	(OSC1)
1	1	1	fosc3 / 4096	fosc1 / 128
1	1	0	fosc3 / 1024	fosc1 / 64
1	0	1	fosc3 / 256	fosc1 / 32
1	0	0	fosc3 / 64	fosc1 / 16
0	1	1	fosc3 / 32	fosc1 / 8
0	1	0	fosc3 / 8	fosc1 / 4
0	0	1	fosc3 / 2	fosc1 / 2
0	0	0	fosc3 / 1	fosc1 / 1

Table 3.5.1(f) I/O Memory map (00FF23H–00FF27H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF23	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PRTF3	Programmable timer 3 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D2	PRTF2	Programmable timer 2 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D1	PRTF1	Programmable timer 1 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D0	PRTF0	Programmable timer 0 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
00FF24	D7	PRPRT5	Programmable timer 5 clock control	On	Off	0	R/W	
	D6	PST52	Programmable timer 5 division ratio			0	R/W	
	D5	PST51				0	R/W	
	D4	PST50				0	R/W	
	D3	PRPRT4	Programmable timer 4 clock control	On	Off	0	R/W	
	D2	PST42	Programmable timer 4 division ratio			0	R/W	
	D1	PST41				0	R/W	
	D0	PST40				0	R/W	
00FF25	D7	PRPRT7	Programmable timer 7 clock control	On	Off	0	R/W	
	D6	PST72	Programmable timer 7 division ratio			0	R/W	
	D5	PST71				0	R/W	
	D4	PST70				0	R/W	
	D3	PRPRT6	Programmable timer 6 clock control	On	Off	0	R/W	
	D2	PST62	Programmable timer 6 division ratio			0	R/W	
	D1	PST61				0	R/W	
	D0	PST60				0	R/W	
00FF27	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	–	–	–	–	R	
	D3	PRTF7	Programmable timer 7 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D2	PRTF6	Programmable timer 6 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D1	PRTF5	Programmable timer 5 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D0	PRTF4	Programmable timer 4 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	

PST52 PST51 PST50 (OSC3) (OSC1)

1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

PST42 PST41 PST40 (OSC3) (OSC1)

1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

PST72 PST71 PST70 (OSC3) (OSC1)

1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

PST62 PST61 PST60 (OSC3) (OSC1)

1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

Table 3.5.1(g) I/O Memory map (00FF30H–00FF35H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	
00FF32	D7	RDR07	PTM0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR06	PTM0 reload data D6					
	D5	RDR05	PTM0 reload data D5					
	D4	RDR04	PTM0 reload data D4					
	D3	RDR03	PTM0 reload data D3					
	D2	RDR02	PTM0 reload data D2					
	D1	RDR01	PTM0 reload data D1					
	D0	RDR00	PTM0 reload data D0 (LSB)					
00FF33	D7	RDR17	PTM1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR16	PTM1 reload data D6					
	D5	RDR15	PTM1 reload data D5					
	D4	RDR14	PTM1 reload data D4					
	D3	RDR13	PTM1 reload data D3					
	D2	RDR12	PTM1 reload data D2					
	D1	RDR11	PTM1 reload data D1					
	D0	RDR10	PTM1 reload data D0 (LSB)					
00FF34	D7	CDR07	PTM0 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR06	PTM0 compare data D6					
	D5	CDR05	PTM0 compare data D5					
	D4	CDR04	PTM0 compare data D4					
	D3	CDR03	PTM0 compare data D3					
	D2	CDR02	PTM0 compare data D2					
	D1	CDR01	PTM0 compare data D1					
	D0	CDR00	PTM0 compare data D0 (LSB)					
00FF35	D7	CDR17	PTM1 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR16	PTM1 compare data D6					
	D5	CDR15	PTM1 compare data D5					
	D4	CDR14	PTM1 compare data D4					
	D3	CDR13	PTM1 compare data D3					
	D2	CDR12	PTM1 compare data D2					
	D1	CDR11	PTM1 compare data D1					
	D0	CDR10	PTM1 compare data D0 (LSB)					

Table 3.5.1(h) I/O Memory map (00FF36H–00FF3BH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF36	D7	PTM07	PTM0 data D7 (MSB)	High	Low	1	R	
	D6	PTM06	PTM0 data D6					
	D5	PTM05	PTM0 data D5					
	D4	PTM04	PTM0 data D4					
	D3	PTM03	PTM0 data D3					
	D2	PTM02	PTM0 data D2					
	D1	PTM01	PTM0 data D1					
	D0	PTM00	PTM0 data D0 (LSB)					
00FF37	D7	PTM17	PTM1 data D7 (MSB)	High	Low	1	R	
	D6	PTM16	PTM1 data D6					
	D5	PTM15	PTM1 data D5					
	D4	PTM14	PTM1 data D4					
	D3	PTM13	PTM1 data D3					
	D2	PTM12	PTM1 data D2					
	D1	PTM11	PTM1 data D1					
	D0	PTM10	PTM1 data D0 (LSB)					
00FF38	D7	MODE16_B	PTM2–3 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_B	External clock 1 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	RPTOUT2	PTM2 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT2	PTM2 clock output control	On	Off	0	R/W	
	D2	PTRUN2	PTM2 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET2	PTM2 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL2	PTM2 input clock selection	External clock	Internal clock	0	R/W	
00FF39	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	RPTOUT3	PTM3 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT3	PTM3 clock output control	On	Off	0	R/W	
	D2	PTRUN3	PTM3 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET3	PTM3 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL3	PTM3 input clock selection	External clock	Internal clock	0	R/W	
00FF3A	D7	RDR27	PTM2 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR26	PTM2 reload data D6					
	D5	RDR25	PTM2 reload data D5					
	D4	RDR24	PTM2 reload data D4					
	D3	RDR23	PTM2 reload data D3					
	D2	RDR22	PTM2 reload data D2					
	D1	RDR21	PTM2 reload data D1					
	D0	RDR20	PTM2 reload data D0 (LSB)					
00FF3B	D7	RDR37	PTM3 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR36	PTM3 reload data D6					
	D5	RDR35	PTM3 reload data D5					
	D4	RDR34	PTM3 reload data D4					
	D3	RDR33	PTM3 reload data D3					
	D2	RDR32	PTM3 reload data D2					
	D1	RDR31	PTM3 reload data D1					
	D0	RDR30	PTM3 reload data D0 (LSB)					

Table 3.5.1(i) I/O Memory map (00FF3CH–00FF41H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF3C	D7	CDR27	PTM2 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR26	PTM2 compare data D6					
	D5	CDR25	PTM2 compare data D5					
	D4	CDR24	PTM2 compare data D4					
	D3	CDR23	PTM2 compare data D3					
	D2	CDR22	PTM2 compare data D2					
	D1	CDR21	PTM2 compare data D1					
	D0	CDR20	PTM2 compare data D0 (LSB)					
00FF3D	D7	CDR37	PTM3 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR36	PTM3 compare data D6					
	D5	CDR35	PTM3 compare data D5					
	D4	CDR34	PTM3 compare data D4					
	D3	CDR33	PTM3 compare data D3					
	D2	CDR32	PTM3 compare data D2					
	D1	CDR31	PTM3 compare data D1					
	D0	CDR30	PTM3 compare data D0 (LSB)					
00FF3E	D7	PTM27	PTM2 data D7 (MSB)	High	Low	1	R	
	D6	PTM26	PTM2 data D6					
	D5	PTM25	PTM2 data D5					
	D4	PTM24	PTM2 data D4					
	D3	PTM23	PTM2 data D3					
	D2	PTM22	PTM2 data D2					
	D1	PTM21	PTM2 data D1					
	D0	PTM20	PTM2 data D0 (LSB)					
00FF3F	D7	PTM37	PTM3 data D7 (MSB)	High	Low	1	R	
	D6	PTM36	PTM3 data D6					
	D5	PTM35	PTM3 data D5					
	D4	PTM34	PTM3 data D4					
	D3	PTM33	PTM3 data D3					
	D2	PTM32	PTM3 data D2					
	D1	PTM31	PTM3 data D1					
	D0	PTM30	PTM3 data D0 (LSB)					
00FF40	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	–	–	–	0	R	
	D3	–	–	–	–	0	R	
	D2	–	–	–	–	0	R	
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz					
	D5	TMD5	Clock timer data 4 Hz					
	D4	TMD4	Clock timer data 8 Hz					
	D3	TMD3	Clock timer data 16 Hz					
	D2	TMD2	Clock timer data 32 Hz					
	D1	TMD1	Clock timer data 64 Hz					
	D0	TMD0	Clock timer data 128 Hz					

Table 3.5.1(j) I/O Memory map (00FF48H–00FF4BH)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF48	D7	STPB0	SIF0 stop bit selection		2 bits	1 bit	0	R/W	Only for asynchronous mode
	D6	EPR0	SIF0 parity enable register		With parity	Non parity	0	R/W	
	D5	PMD0	SIF0 parity mode selection		Odd	Even	0	R/W	
	D4	SCS01	SIF0 clock source selection SCS01 SCS00 Clock source 1 1 Programmable timer				0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS00	1 0 fOSC3 / 4 0 1 fOSC3 / 8 0 0 fOSC3 / 16				0	R/W	
	D2	SMD01	SIF0 mode selection SMD01 SMD00 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD00	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF0	SIF0 enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	SDP0	SIF0 data input/output permutation selection		MSB first	LSB first	0	R/W	
	D6	FER0	SIF0 framing error flag	R	Error	No error	0	R/W	Only for asynchronous mode
				W	Reset (0)	No operation			
	D5	PER0	SIF0 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER0	SIF0 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG0	SIF0 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN0	SIF0 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG0	SIF0 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN0	SIF0 transmit enable		Enable	Disable	0	R/W	
00FF4A	D7	TXD07	SIF0 transmit data D7 (MSB)		High	Low	X	R/W	
	D6	TXD06	SIF0 transmit data D6						
	D5	TXD05	SIF0 transmit data D5						
	D4	TXD04	SIF0 transmit data D4						
	D3	TXD03	SIF0 transmit data D3						
	D2	TXD02	SIF0 transmit data D2						
	D1	TXD01	SIF0 transmit data D1						
	D0	TXD00	SIF0 transmit data D0 (LSB)						
00FF4B	D7	RXD07	SIF0 receive data D7 (MSB)		High	Low	X	R	
	D6	RXD06	SIF0 receive data D6						
	D5	RXD05	SIF0 receive data D5						
	D4	RXD04	SIF0 receive data D4						
	D3	RXD03	SIF0 receive data D3						
	D2	RXD02	SIF0 receive data D2						
	D1	RXD01	SIF0 receive data D1						
	D0	RXD00	SIF0 receive data D0 (LSB)						

Table 3.5.1(k) I/O Memory map (00FF4CH–00FF4FH)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF4C	D7	STPB1	SIF1 stop bit selection		2 bits	1 bit	0	R/W	Only for asynchronous mode
	D6	EPR1	SIF1 parity enable register		With parity	Non parity	0	R/W	
	D5	PMD1	SIF1 parity mode selection		Odd	Even	0	R/W	
	D4	SCS11	SIF1 clock source selection SCS11 SCS10 Clock source 1 1 Programmable timer				0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS10	1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16				0	R/W	
	D2	SMD11	SIF1 mode selection SMD11 SMD10 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD10	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF1	SIF1 enable register		Serial I/F	I/O port	0	R/W	
00FF4D	D7	SDP1	SIF1 data input/output permutation selection		MSB first	LSB first	0	R/W	
	D6	FER1	SIF1 framing error flag	R	Error	No error	0	R/W	Only for asynchronous mode
				W	Reset (0)	No operation			
	D5	PER1	SIF1 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER1	SIF1 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG1	SIF1 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN1	SIF1 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG1	SIF1 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN1	SIF1 transmit enable		Enable	Disable	0	R/W	
00FF4E	D7	TXD17	SIF1 transmit data D7 (MSB)		High	Low	X	R/W	
	D6	TXD16	SIF1 transmit data D6						
	D5	TXD15	SIF1 transmit data D5						
	D4	TXD14	SIF1 transmit data D4						
	D3	TXD13	SIF1 transmit data D3						
	D2	TXD12	SIF1 transmit data D2						
	D1	TXD11	SIF1 transmit data D1						
	D0	TXD10	SIF1 transmit data D0 (LSB)						
00FF4F	D7	RXD17	SIF1 receive data D7 (MSB)		High	Low	X	R	
	D6	RXD16	SIF1 receive data D6						
	D5	RXD15	SIF1 receive data D5						
	D4	RXD14	SIF1 receive data D4						
	D3	RXD13	SIF1 receive data D3						
	D2	RXD12	SIF1 receive data D2						
	D1	RXD11	SIF1 receive data D1						
	D0	RXD10	SIF1 receive data D0 (LSB)						

Table 3.5.1(l) I/O Memory map (00FF50H–00FF55H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF50	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register					
	D5	IOC05	P05 I/O control register					
	D4	IOC04	P04 I/O control register					
	D3	IOC03	P03 I/O control register					
	D2	IOC02	P02 I/O control register					
	D1	IOC01	P01 I/O control register					
	D0	IOC00	P00 I/O control register					
00FF51	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register					
	D5	IOC15	P15 I/O control register					
	D4	IOC14	P14 I/O control register					
	D3	IOC13	P13 I/O control register					
	D2	IOC12	P12 I/O control register					
	D1	IOC11	P11 I/O control register					
	D0	IOC10	P10 I/O control register					
00FF52	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data					
	D5	P05D	P05 I/O port data					
	D4	P04D	P04 I/O port data					
	D3	P03D	P03 I/O port data					
	D2	P02D	P02 I/O port data					
	D1	P01D	P01 I/O port data					
	D0	P00D	P00 I/O port data					
00FF53	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data					
	D5	P15D	P15 I/O port data					
	D4	P14D	P14 I/O port data					
	D3	P13D	P13 I/O port data					
	D2	P12D	P12 I/O port data					
	D1	P11D	P11 I/O port data					
	D0	P10D	P10 I/O port data					
00FF54	D7	PULP07	P07 pull-up control register	On	Off	1	R/W	
	D6	PULP06	P06 pull-up control register					
	D5	PULP05	P05 pull-up control register					
	D4	PULP04	P04 pull-up control register					
	D3	PULP03	P03 pull-up control register					
	D2	PULP02	P02 pull-up control register					
	D1	PULP01	P01 pull-up control register					
	D0	PULP00	P00 pull-up control register					
00FF55	D7	PULP17	P17 pull-up control register	On	Off	1	R/W	
	D6	PULP16	P16 pull-up control register					
	D5	PULP15	P15 pull-up control register					
	D4	PULP14	P14 pull-up control register					
	D3	PULP13	P13 pull-up control register					
	D2	PULP12	P12 pull-up control register					
	D1	PULP11	P11 pull-up control register					
	D0	PULP10	P10 pull-up control register					

Table 3.5.1(m) I/O Memory map (00FF60H–00FF68H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF60	D7	IOC27	P27 I/O control register	Output	Input	0	R/W	
	D6	IOC26	P26 I/O control register					
	D5	IOC25	P25 I/O control register					
	D4	IOC24	P24 I/O control register					
	D3	IOC23	P23 I/O control register					
	D2	IOC22	P22 I/O control register					
	D1	IOC21	P21 I/O control register					
	D0	IOC20	P20 I/O control register					
00FF62	D7	P27D	P27 I/O port data	High	Low	1	R/W	
	D6	P26D	P26 I/O port data					
	D5	P25D	P25 I/O port data					
	D4	P24D	P24 I/O port data					
	D3	P23D	P23 I/O port data					
	D2	P22D	P22 I/O port data					
	D1	P21D	P21 I/O port data					
	D0	P20D	P20 I/O port data					
00FF64	D7	PULP27	P27 pull-up control register	On	Off	1	R/W	
	D6	PULP26	P26 pull-up control register					
	D5	PULP25	P25 pull-up control register					
	D4	PULP24	P24 pull-up control register					
	D3	PULP23	P23 pull-up control register					
	D2	PULP22	P22 pull-up control register					
	D1	PULP21	P21 pull-up control register					
	D0	PULP20	P20 pull-up control register					
00FF66	D7	PCP27	P27 input comparison register	Interrupt occurred at falling edge	Interrupt occurred at rising edge	1	R/W	
	D6	PCP26	P26 input comparison register					
	D5	PCP25	P25 input comparison register					
	D4	PCP24	P24 input comparison register					
	D3	PCP23	P23 input comparison register					
	D2	PCP22	P22 input comparison register					
	D1	PCP21	P21 input comparison register					
	D0	PCP20	P20 input comparison register					
00FF68	D7	–	–	–	–	0	R	"0" when being read
	D6	CTP22H	P24–P27 port chattering-eliminate setup (Input level check time)			0	R/W	
	D5	CTP21H				0	R/W	
	D4	CTP20H				0	R/W	
	D3	–	–	–	–	0	R	"0" when being read
	D2	CTP22L	P20–P23 port chattering-eliminate setup (Input level check time)			0	R/W	
	D1	CTP21L				0	R/W	
	D0	CTP20L				0	R/W	

P24–P27 port chattering-eliminate setup (Input level check time)

CTP22H	CTP21H	CTP20H	Check time [sec]
1	1	1	4/fOSC3
1	1	0	2/fOSC3
1	0	1	1/fOSC3
1	0	0	4096/fOSC1
0	1	1	2048/fOSC1
0	1	0	512/fOSC1
0	0	1	128/fOSC1
0	0	0	None

P20–P23 port chattering-eliminate setup (Input level check time)

CTP22L	CTP21L	CTP20L	Check time [sec]
1	1	1	4/fOSC3
1	1	0	2/fOSC3
1	0	1	1/fOSC3
1	0	0	4096/fOSC1
0	1	1	2048/fOSC1
0	1	0	512/fOSC1
0	0	1	128/fOSC1
0	0	0	None

Table 3.5.1(n) I/O Memory map (00FF70H–00FF75H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF70	D7	HZR07	R07 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR06	R06 high impedance control					
	D5	HZR05	R05 high impedance control					
	D4	HZR04	R04 high impedance control					
	D3	HZR03	R03 high impedance control					
	D2	HZR02	R02 high impedance control					
	D1	HZR01	R01 high impedance control					
	D0	HZR00	R00 high impedance control					
00FF71	D7	HZR17	R17 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR16	R16 high impedance control					
	D5	HZR15	R15 high impedance control					
	D4	HZR14	R14 high impedance control					
	D3	HZR13	R13 high impedance control					
	D2	HZR12	R12 high impedance control					
	D1	HZR11	R11 high impedance control					
	D0	HZR10	R10 high impedance control					
00FF72	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	HZR25	R25 high impedance control	High impedance	Complementary	0	R/W	
	D4	HZR24	R24 high impedance control					
	D3	HZR23	R23 high impedance control					
	D2	HZR22	R22 high impedance control					
	D1	HZR21	R21 high impedance control					
	D0	HZR20	R20 high impedance control					
00FF73	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	–	–	–	–	0	R	
	D4	–	–	–	–	0	R	
	D3	HZR33	R33 high impedance control	High impedance	Complementary	0	R/W	
	D2	HZR32	R32 high impedance control					
	D1	HZR31	R31 high impedance control					
	D0	HZR30	R30 high impedance control					
00FF74	D7	R07D	R07 output port data	High	Low	1	R/W	
	D6	R06D	R06 output port data					
	D5	R05D	R05 output port data					
	D4	R04D	R04 output port data					
	D3	R03D	R03 output port data					
	D2	R02D	R02 output port data					
	D1	R01D	R01 output port data					
	D0	R00D	R00 output port data					
00FF75	D7	R17D	R17 output port data	High	Low	1	R/W	
	D6	R16D	R16 output port data					
	D5	R15D	R15 output port data					
	D4	R14D	R14 output port data					
	D3	R13D	R13 output port data					
	D2	R12D	R12 output port data					
	D1	R11D	R11 output port data					
	D0	R10D	R10 output port data					

Table 3.5.1(o) I/O Memory map (00FF76H–00FF83H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF76	D7	–	R/W register	1	0	1	R/W	Reserved register
	D6	–	R/W register	1	0	1	R/W	
	D5	R25D	R25 output port data	High	Low	1	R/W	
	D4	R24D	R24 output port data					
	D3	R23D	R23 output port data					
	D2	R22D	R22 output port data					
	D1	R21D	R21 output port data					
	D0	R20D	R20 output port data					
00FF77	D7	–	R/W register	1	0	1	R/W	Reserved register
	D6	–	R/W register	1	0	1	R/W	
	D5	–	R/W register	1	0	1	R/W	
	D4	–	R/W register	1	0	1	R/W	
	D3	R33D	R33 output port data	High	Low	1	R/W	
	D2	R32D	R32 output port data					
	D1	R31D	R31 output port data					
	D0	R30D	R30 output port data					
00FF80	D7	MODE16_C	PTM4–5 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_C	External clock 2 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN4	PTM4 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET4	PTM4 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL4	PTM4 input clock selection	External clock	Internal clock	0	R/W	
00FF81	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN5	PTM5 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET5	PTM5 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL5	PTM5 input clock selection	External clock	Internal clock	0	R/W	
00FF82	D7	RDR47	PTM4 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR46	PTM4 reload data D6					
	D5	RDR45	PTM4 reload data D5					
	D4	RDR44	PTM4 reload data D4					
	D3	RDR43	PTM4 reload data D3					
	D2	RDR42	PTM4 reload data D2					
	D1	RDR41	PTM4 reload data D1					
	D0	RDR40	PTM4 reload data D0 (LSB)					
00FF83	D7	RDR57	PTM5 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR56	PTM5 reload data D6					
	D5	RDR55	PTM5 reload data D5					
	D4	RDR54	PTM5 reload data D4					
	D3	RDR53	PTM5 reload data D3					
	D2	RDR52	PTM5 reload data D2					
	D1	RDR51	PTM5 reload data D1					
	D0	RDR50	PTM5 reload data D0 (LSB)					

Table 3.5.1(p) I/O Memory map (00FF84H–00FF89H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF84	D7	CDR47	PTM4 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR46	PTM4 compare data D6					
	D5	CDR45	PTM4 compare data D5					
	D4	CDR44	PTM4 compare data D4					
	D3	CDR43	PTM4 compare data D3					
	D2	CDR42	PTM4 compare data D2					
	D1	CDR41	PTM4 compare data D1					
	D0	CDR40	PTM4 compare data D0 (LSB)					
00FF85	D7	CDR57	PTM5 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR56	PTM5 compare data D6					
	D5	CDR55	PTM5 compare data D5					
	D4	CDR54	PTM5 compare data D4					
	D3	CDR53	PTM5 compare data D3					
	D2	CDR52	PTM5 compare data D2					
	D1	CDR51	PTM5 compare data D1					
	D0	CDR50	PTM5 compare data D0 (LSB)					
00FF86	D7	PTM47	PTM4 data D7 (MSB)	High	Low	1	R	
	D6	PTM46	PTM4 data D6					
	D5	PTM45	PTM4 data D5					
	D4	PTM44	PTM4 data D4					
	D3	PTM43	PTM4 data D3					
	D2	PTM42	PTM4 data D2					
	D1	PTM41	PTM4 data D1					
	D0	PTM40	PTM4 data D0 (LSB)					
00FF87	D7	PTM57	PTM5 data D7 (MSB)	High	Low	1	R	
	D6	PTM56	PTM5 data D6					
	D5	PTM55	PTM5 data D5					
	D4	PTM54	PTM5 data D4					
	D3	PTM53	PTM5 data D3					
	D2	PTM52	PTM5 data D2					
	D1	PTM51	PTM5 data D1					
	D0	PTM50	PTM5 data D0 (LSB)					
00FF88	D7	MODE16_D	PTM6–7 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_D	External clock 3 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN6	PTM6 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET6	PTM6 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL6	PTM6 input clock selection	External clock	Internal clock	0	R/W	
00FF89	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN7	PTM7 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET7	PTM7 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL7	PTM7 input clock selection	External clock	Internal clock	0	R/W	

Table 3.5.1(q) I/O Memory map (00FF8AH–00FF8FH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF8A	D7	RDR67	PTM6 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR66	PTM6 reload data D6					
	D5	RDR65	PTM6 reload data D5					
	D4	RDR64	PTM6 reload data D4					
	D3	RDR63	PTM6 reload data D3					
	D2	RDR62	PTM6 reload data D2					
	D1	RDR61	PTM6 reload data D1					
	D0	RDR60	PTM6 reload data D0 (LSB)					
00FF8B	D7	RDR77	PTM7 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR76	PTM7 reload data D6					
	D5	RDR75	PTM7 reload data D5					
	D4	RDR74	PTM7 reload data D4					
	D3	RDR73	PTM7 reload data D3					
	D2	RDR72	PTM7 reload data D2					
	D1	RDR71	PTM7 reload data D1					
	D0	RDR70	PTM7 reload data D0 (LSB)					
00FF8C	D7	CDR67	PTM6 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR66	PTM6 compare data D6					
	D5	CDR65	PTM6 compare data D5					
	D4	CDR64	PTM6 compare data D4					
	D3	CDR63	PTM6 compare data D3					
	D2	CDR62	PTM6 compare data D2					
	D1	CDR61	PTM6 compare data D1					
	D0	CDR60	PTM6 compare data D0 (LSB)					
00FF8D	D7	CDR77	PTM7 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR76	PTM7 compare data D6					
	D5	CDR75	PTM7 compare data D5					
	D4	CDR74	PTM7 compare data D4					
	D3	CDR73	PTM7 compare data D3					
	D2	CDR72	PTM7 compare data D2					
	D1	CDR71	PTM7 compare data D1					
	D0	CDR70	PTM7 compare data D0 (LSB)					
00FF8E	D7	PTM67	PTM6 data D7 (MSB)	High	Low	1	R	
	D6	PTM66	PTM6 data D6					
	D5	PTM65	PTM6 data D5					
	D4	PTM64	PTM6 data D4					
	D3	PTM63	PTM6 data D3					
	D2	PTM62	PTM6 data D2					
	D1	PTM61	PTM6 data D1					
	D0	PTM60	PTM6 data D0 (LSB)					
00FF8F	D7	PTM77	PTM7 data D7 (MSB)	High	Low	1	R	
	D6	PTM76	PTM7 data D6					
	D5	PTM75	PTM7 data D5					
	D4	PTM74	PTM7 data D4					
	D3	PTM73	PTM7 data D3					
	D2	PTM72	PTM7 data D2					
	D1	PTM71	PTM7 data D1					
	D0	PTM70	PTM7 data D0 (LSB)					

4 POWER SUPPLY

This chapter explains the operating voltage and the configuration and control of the S1C88655 internal power supply circuit.

4.1 Operating Voltage

The S1C88655 operating power voltage is as follows:

1.8 V to 3.6 V

Supply a voltage within the above range to between the V_{DD} (+) and V_{SS} (GND) terminals.

Note: The S1C88655 has three V_{DD} terminals and four V_{SS} terminals. These terminals must be connected to V_{DD} or V_{SS}. Do not leave the terminals open.

4.2 Internal Power Supply Circuit

The S1C88655 has a built-in power supply circuit as shown in Figure 4.2.1 that generates all the voltages required for the internal circuits from the supply voltage within the range described above.

Notes:
- *Be sure not to use the voltages output from the V_{D1}, V_{D2}, and V_{C1}–V_{C5} terminals for driving external circuits.*
- *Voltage within the range of 2.0 to 3.6 V should be supplied to V_{DD} when generating the V_{C1} to V_{C5} voltages. If V_{DD} = 1.8–2.0 V, the V_{C1} to V_{C5} voltages will be generated higher than those described in Chapter 19, "Electrical Characteristics".*

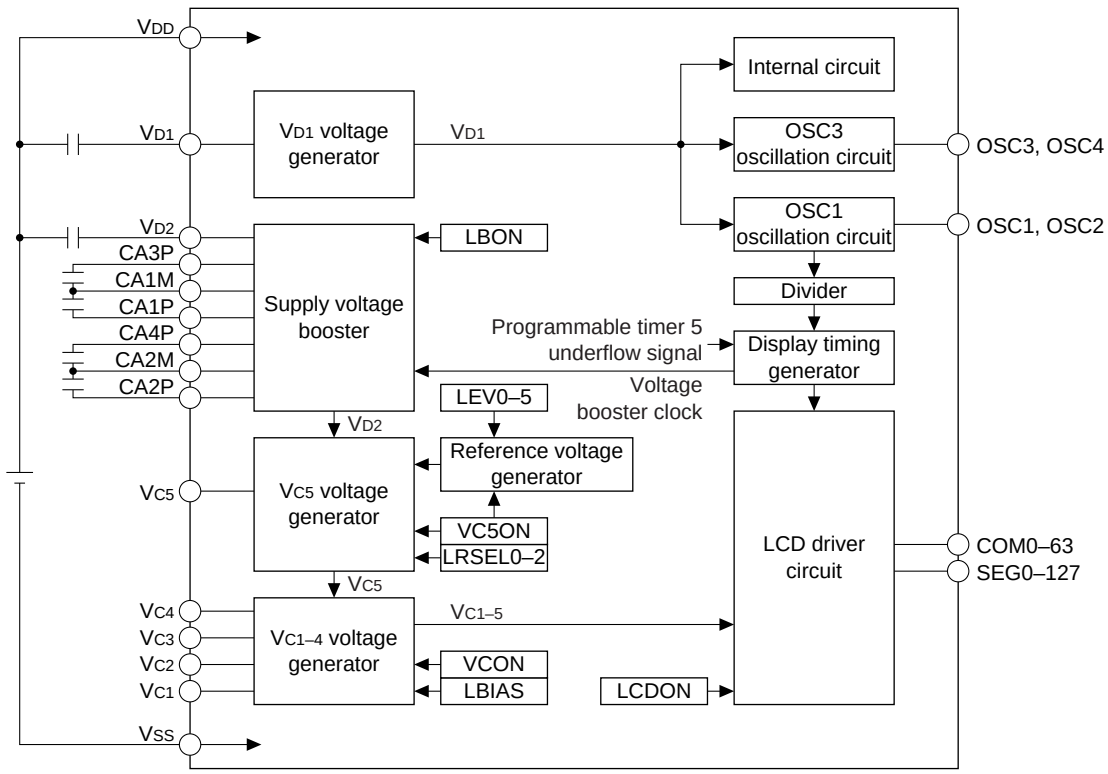


Fig. 4.2.1 Configuration of internal power supply circuit

4.2.1 V_{D1} voltage generator

The V_{D1} voltage generator outputs the V_{D1} operating voltage for the internal logic and oscillation circuits. The V_{D1} voltage value is fixed at 1.8 V (Typ.).

4.2.2 Supply voltage booster circuit

The V_{D2} voltage is used to drive the V_{C5} voltage generator and $V_{C1–4}$ voltage generator that generates the LCD drive voltages. The supply voltage booster circuit generates the V_{D2} voltage by double, triple, quadruple, or quintuple boosting the supply voltage V_{DD}. The boost ratio can be configured with the external circuit as shown in Figure 4.2.2.1. Select a boost ratio according to the V_{DD} voltage value so that the V_{D2} voltage level is higher than the desired V_{C5}.

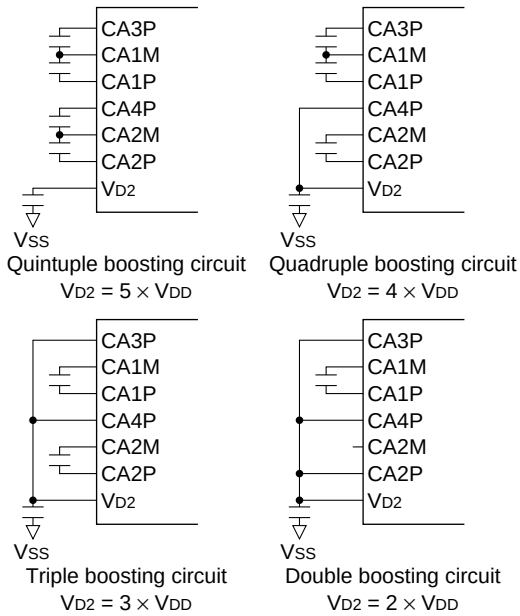


Fig. 4.2.2.1 External connection for supply voltage booster circuit

Notes:
- *Make sure that the V_{D2} voltage does not exceed the absolute maximum rating (see Chapter 19, "Electrical Characteristics") when setting the boosting ratio.*
- *The capacitances depend on the load of the LCD panel to drive. Select component values so that the LCD drive voltages are stabilized as much as possible.*
- *Current consumption varies according to the boosting ratio. See Chapter 19, "Electrical Characteristics".*

The supply voltage booster circuit is activated by writing "1" to the supply voltage booster ON / OFF control register LBON and is deactivated by writing "0". However, the LCD display timing generator must be turned ON to supply the voltage booster clock to the supply voltage booster circuit before turning the circuit ON.

4.2.3 V_{C5} voltage generator

The V_{C5} voltage generator generates the LCD drive voltage V_{C5} from the V_{D2} voltage output by the supply voltage booster circuit. The V_{C5} voltage generator includes a 64-level programmable voltage control and a software adjustable resistor with 7 different resistances to provide a 64 × 7-voltage fine adjustment function. This function is used to adjust the contrast of the LCD panel.

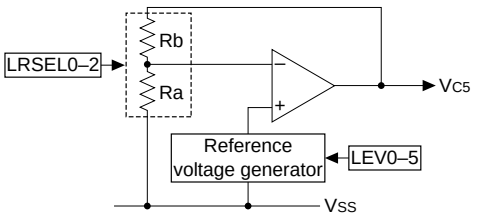


Fig. 4.2.3.1 Configuration of V_{C5} voltage generator

The programmable voltage control can be adjusted within level 0 to level 63 using the V_{C5} voltage control register LEV0–LEV5. The resistance ratio "(Ra + Rb) / Ra" can be selected as listed in Table 4.2.3.1 using the V_{C5} voltage generator resistance ratio adjustment register LRSEL0–LRSEL2.

Table 4.2.3.1 Adjusting resistance ratio in V_{C5} voltage generator

LRSEL2	LRSEL1	LRSEL0	(Ra+Rb)/Ra
1	1	1	Not allowed
1	1	0	8.69
1	0	1	8.13
1	0	0	7.20
0	1	1	6.46
0	1	0	5.60
0	0	1	4.84
0	0	0	4.06

See Chapter 19, "Electrical Characteristics", for the V_{C5} voltage adjustment values.

The V_{C5} voltage generator is activated by writing "1" to the V_{C5} voltage generator ON / OFF control register VC5ON and is deactivated by writing "0".

4.2.4 $V_{C1–4}$ voltage generator

The $V_{C1–4}$ voltage generator generates the LCD drive voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4} by dividing the V_{C5} voltage output from the V_{C5} voltage generator with resistors. These voltages are supplied to the LCD driver circuit via a voltage follower circuit. Furthermore, the LCD bias select register LBIAS is provided to select the LCD bias ratio from 1 / 7 bias or 1 / 9 bias.

See Chapter 19, "Electrical Characteristics", for the voltage values.

The $V_{C1–4}$ voltage generator is activated by writing "1" to the $V_{C1–4}$ voltage generator ON / OFF control register VCON and is deactivated by writing "0".

4.2.5 LCD drive power supply circuit control procedure

The supply voltage booster circuit, V_{C5} voltage generator, and $V_{C1–4}$ voltage generator should be activated in the procedure as shown in Figure 4.2.5.1.

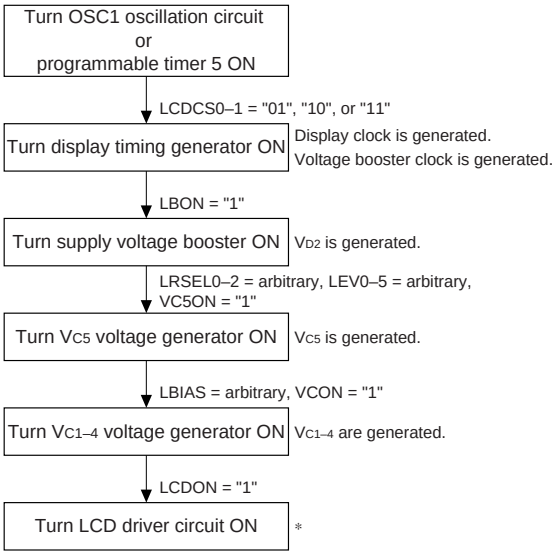


Fig. 4.2.5.1 LCD drive power supply circuit control procedure

* Setting the LCDON register to "1" starts supplying the V_{C1}–V_{C5} voltages to the LCD driver to enable display controls. Furthermore, the LCD driver generates the CL and FR signals. However, the DSPC0 and DSPC1 registers must be configured to start the LCD display.

While the LCD display is turned OFF, the LCD drive power supply circuit can be deactivated to reduce current consumption. In this case, turn each circuit OFF in the reverse order of Figure 4.2.5.1 except hardware reset.

See chapters "8 Oscillation Circuits", "13 Programmable Timer", and "15 LCD Driver" for controlling the OSC1 oscillation circuit, programmable timer, and display timing generator.

4.3 Details of Control Registers

Table 4.3.1 shows the control bits of the power supply circuit.

Table 4.3.1 Power supply control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF09	D7	–	–	–	–	–	–	"0" when being read
	D6	LCDON	LCD driver circuit On/Off control	On	Off	0	R/W	
	D5	LBIAS	LCD bias selection	1/9 bias	1/7 bias	1	R/W	
	D4	VCON	$V_{C1–4}$ voltage generator On/Off control	On	Off	0	R/W	
	D3	VC5ON	V_{C5} voltage generator On/Off control	On	Off	0	R/W	
	D2	LBON	Supply voltage booster On/Off control	On	Off	0	R/W	
	D1	LCDCS1	Display timing generator control LCDCS1 / LCDCS0 / Source clock 1 / 1 / P timer 5			0	R/W	
	D0	LCDCS0	1 / 0 / f_{OSC1}/2 0 / 1 / f_{OSC1}/1 0 / 0 / Off			0	R/W	
00FF0A	D7	–	–	–	–	–	–	Constantly "0" when
	D6	–	–	–	–	–	–	being read
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	LRSEL2	V_{C5} voltage generator resistance ratio adjustment LRSEL2 / LRSEL1 / LRSEL0 / Resistance ratio 1 / 1 / 1 / Not allowed			0	R/W	
	D1	LRSEL1	1 / 1 / 0 / 8.69 1 / 0 / 1 / 8.13 1 / 0 / 0 / 7.20			0	R/W	
	D0	LRSEL0	0 / 1 / 1 / 6.46 0 / 1 / 0 / 5.60 0 / 0 / 1 / 4.84 0 / 0 / 0 / 4.06			0	R/W	
00FF0B	D7	–	–	–	–	–	–	Constantly "0" when
	D6	–	–	–	–	–	–	being read
	D5	LEV5	V_{C5} voltage control			0	R/W	
	D4	LEV4	LEV5 LEV4 LEV3 LEV2 LEV1 LEV0 Level 1 1 1 1 1 1 63			0	R/W	
	D3	LEV3	1 1 1 1 1 0 62			0	R/W	
	D2	LEV2	: : : : : : :			0	R/W	
	D1	LEV1	0 0 0 0 0 1 1			0	R/W	
	D0	LEV0	0 0 0 0 0 0 0			0	R/W	

LBON: 00FF09H•D2

Controls the supply voltage booster circuit.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to LBON, the supply voltage booster circuit goes ON and outputs V_{D2} by boosting the V_{DD} in the boosting ratio set using the CAxx terminals. The V_{D2} voltage is supplied to the V_{C5} voltage generator and $V_{C1–4}$ voltage generator that generates the LCD drive voltages. When "0" is written to LBON, the supply voltage booster circuit goes OFF.
At initial reset, LBON is set to "0" (OFF).

VC5ON: 00FF09H•D3

Controls the V_{C5} voltage generator.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to VC5ON, the V_{C5} voltage generator goes ON and outputs the LCD drive voltage V_{C5}. However, a V_{D2} voltage higher than the desired V_{C5} voltage level must be supplied from the supply voltage booster circuit before the V_{C5} voltage can be generated. When "0" is written to VC5ON, the V_{C5} voltage generator goes OFF.
At initial reset, VC5ON is set to "0" (OFF).

VCON: 00FF09H•D4

Controls the $V_{C1–4}$ voltage generator.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to VCON, the $V_{C1–4}$ voltage generator goes ON and outputs the LCD drive voltages V_{C1}–V_{C4}. However, the V_{C5} voltage must be supplied from the V_{C5} voltage generator before these voltages can be generated. When "0" is written to VCON, the $V_{C1–4}$ voltage generator goes OFF.
At initial reset, VCON is set to "0" (OFF).

Note: While the LCD panel is turned OFF, the LCD drive power supply circuit should be turned OFF to reduce current consumption using LBON, VC5ON, and VCON.

LBIAS: 00FF09H•D5

Selects the bias ratio for LCD drive.

When "1" is written: 1/9 bias
When "0" is written: 1/7 bias
Reading: Valid

When "1" is written to LBIAS, 1/9 bias is selected and when "0" is written, 1/7 bias is selected. This setting controls the $V_{C1–4}$ voltage generator outputs.
At initial reset LBIAS is set to "1" (1/9 bias).

LRSEL0–LRSEL2: 00FF0AH•D0–D2

Selects a resistance ratio to adjust the output voltage of the V_{C5} voltage generator.

Table 4.3.2 Adjusting resistance ratio in V_{C5} voltage generator

LRSEL2	LRSEL1	LRSEL0	(Ra+Rb)/Ra
1	1	1	Not allowed
1	1	0	8.69
1	0	1	8.13
1	0	0	7.20
0	1	1	6.46
0	1	0	5.60
0	0	1	4.84
0	0	0	4.06

At initial reset, LRSEL is set to "0".

LEV0–LEV5: 00FF0BH•D0–D5

Adjusts the reference voltage for the V_{C5} voltage generator in 64 levels (0 to 63). The contrast of the LCD panel can be adjusted with both this register and the LRSEL0–LRSEL2 register. See Chapter 19, "Electrical Characteristics", for relationship between the setting values and the V_{C5} voltage values.
At initial reset, LEV is set to "0".

4.4 Precautions

(1) Be sure not to use the voltages output from the V_{D1} and V_{D2} terminals for driving external circuits.
The V_{C1}–V_{C5} terminal outputs can only be used to drive a recommended LCD driver.

(2) The supply voltage booster circuit must be configured so that the V_{D2} voltage level is higher than the desired V_{C5}. However, make sure that the V_{D2} voltage does not exceed the absolute maximum rating (see Chapter 19, "Electrical Characteristics") when setting the boosting ratio.

5 INITIAL RESET

An initial reset must be applied to the S1C88655 to initialize the internal circuits. This chapter describes the internal initial reset circuits and default values of the CPU registers.

5.1 Configuration of Initial Reset Circuit

The S1C88655 handles two internal reset signals for system reset and CPU reset.

System reset

The system reset signal initializes all the I/O registers and counters. When a system reset is issued, the CPU reset is issued simultaneously also.
The following lists the causes of system reset:

(1) External initial reset via the $\overline{\text{RESET}}$ terminal

(2) Internal initial reset by the reset voltage detector (mask option)

CPU reset

The CPU reset signal resets only the CPU with the I/O register values maintained.
The cause of CPU reset is as follows:

(1) Internal initial reset by the watchdog timer overflow signal (mask option)

Figure 5.1.1 shows the configuration of the initial reset circuit.
The CPU and peripheral circuits enter an reset status when a cause of initial reset occurs. When the cause of the reset is canceled, the CPU starts reset exception processing. (See the "S1C88 Core CPU Manual".)
When this occurs, the reset exception processing vector, Bank 0, 000000H–000001H from the program memory is read out and the program (initialization routine) which begins at the readout address is executed.

5.1.1 $\overline{\text{RESET}}$ terminal

Initial reset can be done by externally inputting a LOW level to the $\overline{\text{RESET}}$ terminal.
Be sure to maintain the $\overline{\text{RESET}}$ terminal at LOW level for the regulation time after the power on to assure the initial reset. (See Chapter 19, "Electrical Characteristics".)
In addition, be sure to use the $\overline{\text{RESET}}$ terminal for the first initial reset after the power is turned on. However, it is not necessary to reset the IC using the $\overline{\text{RESET}}$ terminal when the internal reset circuit is enabled by mask option.
The $\overline{\text{RESET}}$ terminal is equipped with a pull-up resistor. You can select whether or not to use by mask option.

Input port pull-up resistor
$\overline{\text{RESET}}$ ..... ☐ With resistor ☐ Gate direct

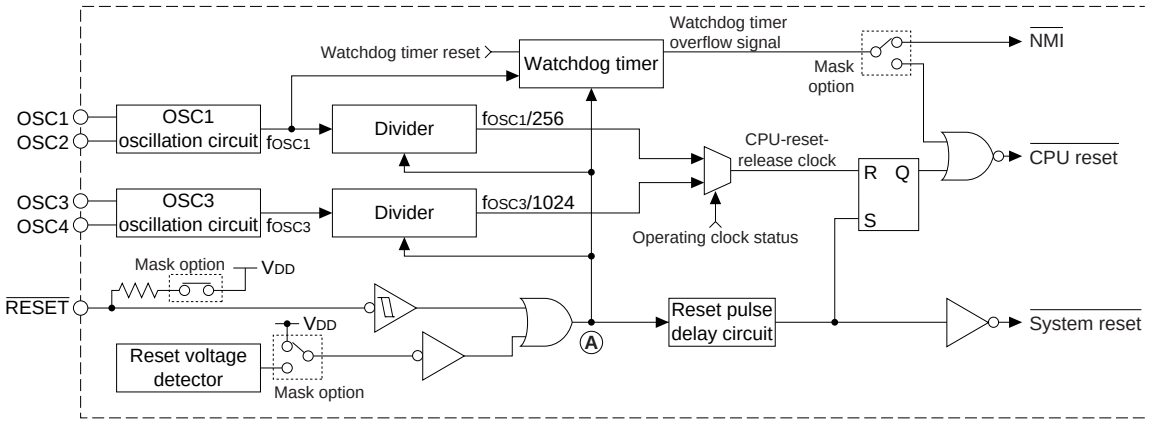


Fig. 5.1.1 Configuration of initial reset circuit

5.1.2 Reset voltage detector (RVD)

The S1C88655 has a built-in reset voltage detector that can be enabled by mask option. This circuit has a power-on reset function that issues a system reset when the power supply is turned OFF or the supply voltage drops as well as when the power supply is turned ON.

Reset voltage detector
☐ Not Use ☐ Use

When "Use" is selected by mask option, the reset voltage detector asserts the reset signal immediately after power is turned on until the supply voltage VDD reaches the reset release level. Furthermore, when the power is turned OFF or the supply voltage drops, the reset voltage detector asserts the reset signal after the supply voltage VDD drops under the reset level. There is a hysteresis error between the reset release level and the reset level. The reset voltage detector contains a function to hold reset status for a certain time to make sure the IC resets even if there is an instantaneous power interruption or a power surge. Note that current consumption increases when the reset voltage detector is used. See Chapter 19, "Electrical Characteristics", for the reset level, reset release level, hysteresis and current consumption.

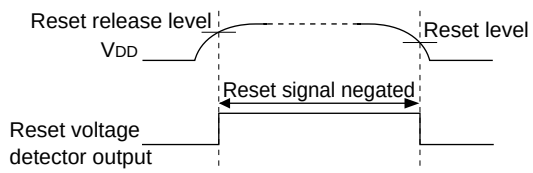


Fig. 5.1.2.1 Reset output from reset voltage detector

When the reset voltage detector is used, it is not necessary to perform initial reset using the $\overline{\text{RESET}}$ terminal. However, both the $\overline{\text{RESET}}$ terminal and the reset voltage detector can be used for initial reset.

5.1.3 Watchdog timer overflow signal

The watchdog timer overflow signal can be used as a CPU reset signal by mask option.

Watchdog timer overflow signal
☐ Interrupt(NMI) ☐ Reset

When "Reset" is selected, the watchdog timer overflow signal will reset only the CPU (it does not initialize the register values of the peripheral circuits). The reset signal output from the watchdog timer is negated without waiting for oscillation stabilization time.

5.1.4 Initial reset sequence

Even if the $\overline{\text{RESET}}$ terminal input or internal reset circuit negates the reset signal after power is turned on, the CPU's reset status continues (or the CPU does not starts up) until the oscillation stabilization waiting time (512 / fOSC3 sec.) has elapsed.
Figure 5.1.4.1 shows the operating sequence following initial reset release.
The CPU starts operating in synchronization with the OSC3 clock after reset status is released.

Note: The oscillation stabilization time described in this section does not include oscillation start time. Therefore the time interval until the CPU starts executing instructions after power is turned on or SLEEP status is cancelled may be longer than that indicated in the figure below.

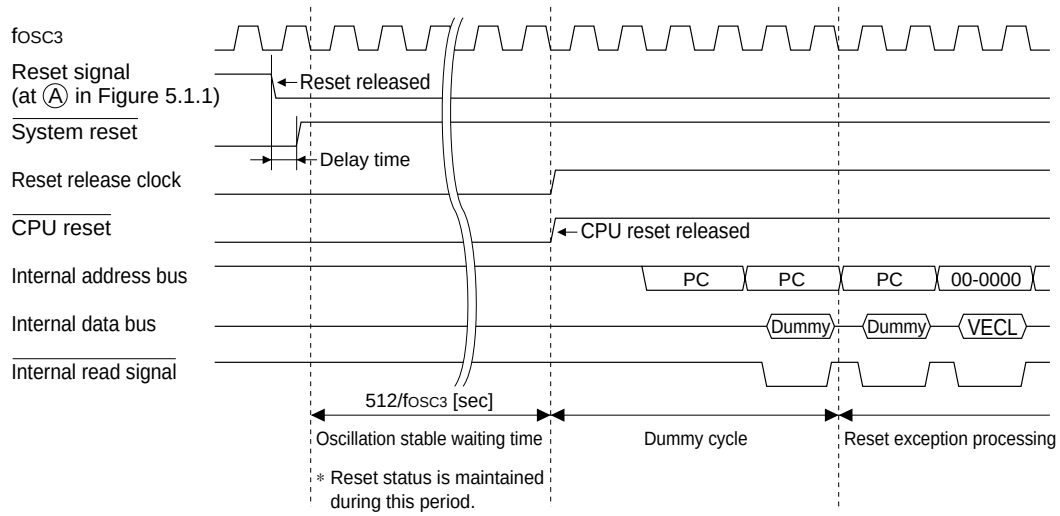


Fig. 5.1.4.1 Initial reset sequence

5.2 Initial Settings After Initial Reset

The CPU internal registers are initialized as follows during initial reset.

Table 5.2.1 Initial settings

Register name	Code	Bit length	Setting value
Data register A	A	8	Undefined
Data register B	B	8	Undefined
Index (data) register L	L	8	Undefined
Index (data) register H	H	8	Undefined
Index register IX	IX	16	Undefined
Index register IY	IY	16	Undefined
Program counter	PC	16	Undefined*
Stack pointer	SP	16	Undefined
Base register	BR	8	Undefined
Zero flag	Z	1	0
Carry flag	C	1	0
Overflow flag	V	1	0
Negative flag	N	1	0
Decimal flag	D	1	0
Unpack flag	U	1	0
Interrupt flag 0	I0	1	1
Interrupt flag 1	I1	1	1
New code bank register	NB	8	01H
Code bank register	CB	8	Undefined*
Expand page register	EP	8	00H
Expand page register for IX	XP	8	00H
Expand page register for IY	YP	8	00H

* Reset exception processing loads the preset values stored in 0 bank, 0000H–0001H into the PC. At the same time, 01H of the NB initial value is loaded into CB.

Initialize the registers which are not initialized at initial reset using software.

Since the internal RAM and display data RAM are not initialized at initial reset, be sure to initialize using software.

The respectively stipulated initializations are done for internal peripheral circuits. If necessary, the initialization should be done using software.
For initial values at initial reset, see Section 3.5, "I/O Memory", and peripheral circuit descriptions in the following chapters.

6 SYSTEM CONTROLLER AND BUS CONTROL

The system controller is a management unit which sets such items as the bus mode in accordance with memory system configuration factors. For the purposes of controlling the system, the following settings can be performed in software:

(1) Bus and CPU mode settings
(2) Chip enable ($\overline{CE}$) signal output settings
(3) WAIT state settings for external memory
(4) Page address setting of the stack pointer

Below is a description of the how these settings are to be made.

6.1 Configuration of External Bus

The S1C88655 has bus terminals that can address a maximum of 1M × 4 bytes and memory (and other) devices can be externally expanded according to the range of each bus mode described in the previous section.

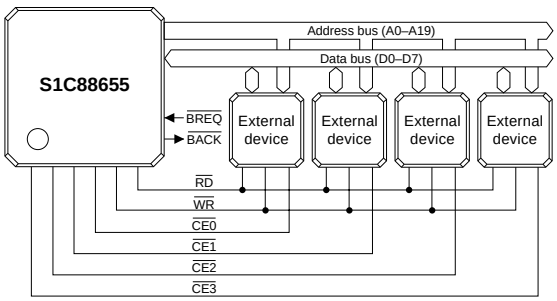


Fig. 6.1.1 External bus lines

■ Address bus

The S1C88655 possesses a 20-bit external address bus (A0–A19). The address bus terminals A0–A19 are shared with output ports R00–R07 (=A0–A7), R10–R17 (=A8–A15) and R20–R23 (=A16–A19), switching between these functions being determined by the bus mode setting.
When set as address bus, the data register and high impedance control register of each output port can be used as a general-purpose data register with read / write capabilities.

■ Data bus

The S1C88655 possesses an 8-bit external data bus (D0–D7). The data bus terminals D0–D7 are shared with I / O ports P00–P07, switching between these functions being determined by the bus mode setting.
When set as data bus, the data register and I / O control register of each I / O port can be used as a general-purpose data register with read / write capabilities.
The data bus can be pulled up to high during input mode using the built-in pull-up resistor. This pull-up resistor is enabled or disabled using the pull-up control register and mask option. See Chapter 10, "I / O Ports (P Ports)" for details.

■ Read ($\overline{RD}$)/write ($\overline{WR}$) signals

The read ($\overline{RD}$) / write ($\overline{WR}$) signal output terminals directed to external devices are shared respectively with the output ports R24 and R25, switching between these functions being determined by the bus mode setting.
When set as read ($\overline{RD}$) / write ($\overline{WR}$) signal output terminals, the data register and high impedance control register for each output port (R24, R25) can be used as a general-purpose data register with read / write capabilities.
The read ($\overline{RD}$) / write ($\overline{WR}$) signals are output only when an external memory is accessed When accessing the internal memory area, these signals are not output outside the IC.

■ Chip enable ($\overline{CE}$) signal

The S1C88655 is equipped with an address decoder which can output four different chip enable ($\overline{CE}$) signals. Consequently, four devices equipped with a chip enable ($\overline{CE}$) or chip select ($\overline{CS}$) terminal can be directly connected without any external address decoder circuit.

The four chip enable ($\overline{CE0}$–$\overline{CE3}$) signal output terminals are shared with the output ports R30–R33, either the chip enable ($\overline{CE}$) output or general-purpose output can be selected in each bit with software (except for single chip mode). When set for chip enable ($\overline{CE}$) output, the data register and high impedance control register for each output port can be used as a general-purpose data register with read / write capabilities.

The chip enable ($\overline{CE}$) signals are output only when an external memory is accessed. When accessing the internal memory area, these signals are not output to outside the IC.
See Table 6.3.1 for the address ranges that are assigned to the chip enable ($\overline{CE}$) signals.

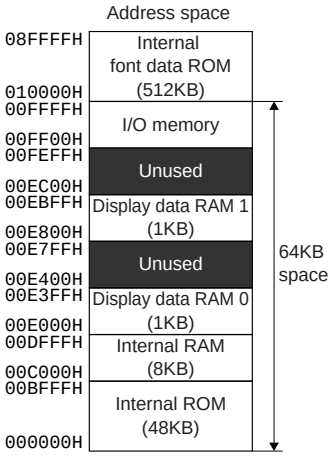
6.2 Bus Mode and CPU Mode

6.2.1 Bus mode

In order to set bus specifications to match the configuration of external expanded memory, two different bus modes described below are selectable using the bus mode setting register BUSMOD.
(1) Single chip mode (BUSMOD = "0")
(2) Expansion mode (BUSMOD = "1")

■ **Single chip mode**

The single chip mode setting applies when the S1C88655 is used as a single chip microcomputer without external expanded memory. Since this mode uses the internal ROM, the system can only be operated in the MCU mode. In the MPU mode, the system cannot be set to the single chip mode.
Since there is no need for an external bus line in this mode, terminals normally set for bus use can be used as general-purpose output ports or I/O ports.



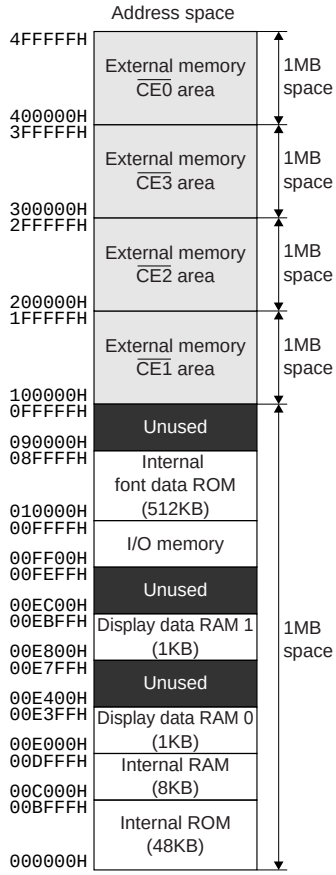
Pin configuration

Pin name	Function
R00 | R07	R00 | R07
R10 | R17	R10 | R17
R20 | R23	R20 | R23
R24	R24
R25	R25
R30	R30
R31	R31
R32	R32
R33	R33
P00 | P07	P00 | P07
P24	P24
P25	P25

Fig. 6.2.1.1 Memory map for single chip mode

■ **Expansion mode**

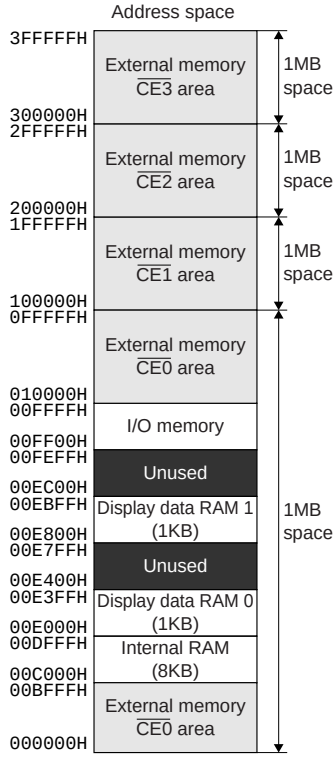
The expansion mode setting applies when the S1C88655 is used with up to 1M bytes × 4 of external expanded memory.
Because internal ROM is being used in the MCU mode, external devices can be assigned to the area from 100000H to 4FFFFFH.
Since the internal ROM area is released in the MPU mode, external devices can be assigned to the area from 000000H to 3FFFFFH. However, the area from 00C000H to 00FFFFH is assigned to internal memory and cannot be used to access an external device.



Pin configuration

Pin name	Function
R00 | R07	A0 | A7
R10 | R17	A8 | A15
R20 | R23	A16 | A19
R24	$\overline{RD}$
R25	$\overline{WR}$
R30	R30/$\overline{CE0}$
R31	R31/$\overline{CE1}$
R32	R32/$\overline{CE2}$
R33	R33/$\overline{CE3}$
P00 | P07	D0 | D7
P24	P24/$\overline{BREQ}$
P25	P25/$\overline{BACK}$

Fig. 6.2.1.2 Memory map for MCU expansion mode



Pin configuration

Pin name	Function
R00 | R07	A0 | A7
R10 | R17	A8 | A15
R20 | R23	A16 | A19
R24	$\overline{RD}$
R25	$\overline{WR}$
R30	$\overline{CE0}$
R31	R31/$\overline{CE1}$
R32	R32/$\overline{CE2}$
R33	R33/$\overline{CE3}$
P00 | P07	D0 | D7
P24	P24/$\overline{BREQ}$
P25	P25/$\overline{BACK}$

Fig. 6.2.1.3 Memory map for MPU expansion mode

6.2.2 CPU mode

The CPU allows software to select its operating mode from two types shown below according to the programming area size. Use the CPU mode setting register CPUMOD for selection.
(1) Minimum mode (CPUMOD = "0")
(2) Maximum mode (CPUMOD = "1")

■ Minimum mode

The program area is configured within 64K bytes in any one-bank. However, the bank to be used must be specified in the CB register and cannot be changed after an initialization. This mode does not push the CB register contents onto the stack when a subroutine is called. It makes it possible to economize on stack area usage.

■ Maximum mode

The program area can be configured exceeding 64K bytes. However the CB register must be setup when the program exceeds a bank boundary every 64K bytes. This mode pushes the CB register contents when a subroutine is called.

Table 6.2.2.1 lists the configuration of MCU / MPU mode, bus mode, and CPU mode.

■ Mode set after initial reset

At initial reset, the bus mode (CPU mode) is set as explained below.

In MCU mode:
At initial reset, the S1C88655 is set in single chip mode (minimum).
Accordingly, in MCU mode, even if a memory has been externally expanded, the system is activated by the program stored in the internal ROM.
In the system with externally expanded memory, perform the applicable bus mode settings during the initialization routine originating in the internal ROM.

In MPU mode:
At initial reset, the S1C88655 is set in expansion mode (minimum).
Therefore, the internal ROM will be disabled.

Table 6.2.2.1 Setting bus mode and CPU mode

MCU/$\overline{\text{MPU}}$ terminal	Setting value		Bus mode	CPU mode	Configuration of external memory
	BUSMOD	CPUMOD			
1 (MCU mode)	1	1	Expansion	Maximum	ROM+RAM>64K bytes (Program≥64K bytes)
	1	0		Minimum	ROM+RAM>64K bytes (Program<64K bytes)
	0	1	Single chip	Maximum	None (Program≥64K bytes)
	0	0		Minimum	None (Program<64K bytes)
0 (MPU mode)	1	1	Expansion	Maximum	ROM+RAM>64K bytes (Program≥64K bytes)
	1	0		Minimum	ROM+RAM>64K bytes (Program<64K bytes)
	0	1		Maximum	ROM+RAM>64K bytes (Program≥64K bytes)
	0	0		Minimum	ROM+RAM>64K bytes (Program<64K bytes)

6.3 Address Decoder ($\overline{CE}$) Settings

The S1C88655 is equipped with address decoders that can output a maximum of four chip enable signals ($\overline{CE0}$–$\overline{CE3}$) to external devices.
At initial reset, the $\overline{CE0}$–$\overline{CE3}$ terminals are set as output port terminals (R30–R33). For this reason, when operating in expansion mode, the ports to be used as $\overline{CE}$ signal output terminals must be configured. This setting is performed through software which writes "1" to registers CE0–CE3 corresponding the $\overline{CE}$ signals to be used.
However, in the MPU mode the R30 terminal is always configured as the $\overline{CE0}$ output port.
Table 6.3.1 shows the address range assigned to the four chip enable ($\overline{CE}$) signals.

Table 6.3.1 Address settings of $\overline{CE0}$–$\overline{CE3}$

Mode	$\overline{CE}$ signal	Address
MCU	$\overline{CE0}$	400000H–4FFFFFH
expansion	$\overline{CE1}$	100000H–1FFFFFH
mode	$\overline{CE2}$	200000H–2FFFFFH
	$\overline{CE3}$	300000H–3FFFFFH
MPU	$\overline{CE0}$	000000H–00BFFFH
expansion		010000H–0FFFFFH
mode	$\overline{CE1}$	100000H–1FFFFFH
	$\overline{CE2}$	200000H–2FFFFFH
	$\overline{CE3}$	300000H–3FFFFFH

The arrangement of memory space for external devices does not necessarily have to be continuous from a subordinate address and any of the chip enable signals can be used to assign areas in memory. However, in the MPU mode, program memory must be assigned to $\overline{CE0}$.
The $\overline{CE}$ signals are output only when the appointed external memory area is accessed and are not output when internal memory is accessed.

Note: The $\overline{CE}$ signals will be inactive status when the chip enters the standby mode (HALT mode or SLEEP mode).

6.4 WAIT State Settings

In order to insure accessing of external low speed devices during high speed operations, the S1C88655 is equipped with a WAIT function which prolongs access time. (See the "S1C88 Core CPU Manual" for details of the WAIT function.)

The number of wait states inserted can be selected from a choice of eight as shown in Table 6.4.1 using the WAIT state control register WT0–WT2.

Table 6.4.1 Setting number of WAIT states

WT2	WT1	WT0	Number of inserted states
1	1	1	14
1	1	0	12
1	0	1	10
1	0	0	8
0	1	1	6
0	1	0	4
0	0	1	2
0	0	0	No wait

* The length of one state is a 1/2 clock cycle.

WAIT states set in software are inserted between bus cycle states T3–T4.
Note, however, that WAIT states cannot be inserted when an internal register and internal memory are being accessed and when operating with the OSC1 oscillation circuit.
Consequently, WAIT state settings in single chip mode are meaningless.
Figures 6.4.1 and 6.4.2 show the memory read / write timing charts.

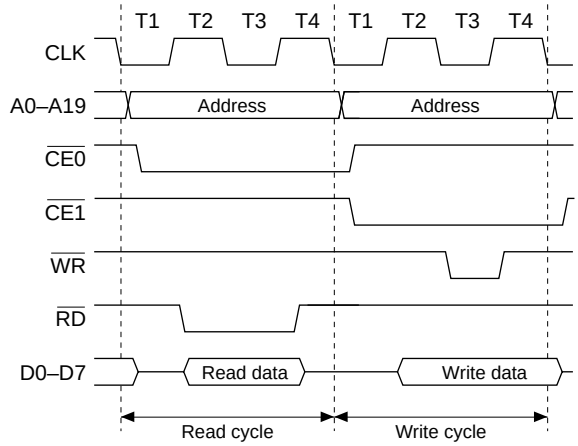


Fig. 6.4.1 Memory read/write cycle (no wait state)

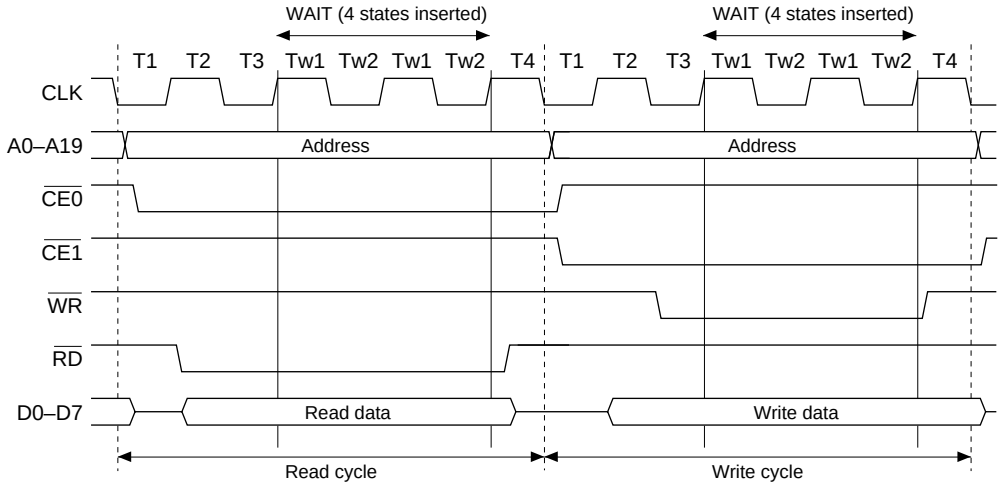


Fig. 6.4.2 Memory read/write cycle (with wait state)

6.5 Setting Bus Authority Release Request Signal

The S1C88655 is equipped with a bus authority release function on request from an external device so that DMA (Direct Memory Access) transfer can be conducted between external devices. The internal memory cannot be accessed by this function.

There are two terminals used for this function: the bus authority release request signal ($\overline{BREQ}$) input terminal and the bus authority release acknowledge signal ($\overline{BACK}$) output terminal.
The $\overline{BREQ}$ input terminal is shared with the P24 port and the $\overline{BACK}$ output terminal with the P25 port. At initial reset, these terminal facilities are set as I/O port terminals. The terminals can be altered to function as $\overline{BREQ}$/$\overline{BACK}$ terminals by writing "1" to register EBR. In the single chip mode, or when using a system which does not require bus authority release, EBR must be fixed at "0".

When the bus authority release request ($\overline{BREQ}$ = LOW) is received from an external device, the S1C88655 switches the address bus, data bus, $\overline{RD}$/$\overline{WR}$ signal, and $\overline{CE}$ signal lines to a high impedance state, outputs a LOW level from the $\overline{BACK}$ terminal and releases bus authority. As soon as a LOW level is output from the $\overline{BACK}$ terminal, the external device can use the external bus. When DMA is completed, the external device returns the $\overline{BREQ}$ terminal to HIGH and releases bus authority. Figure 6.5.1 shows the bus authority release sequence.

During bus authority release state, internal memory cannot be accessed from the external device. In cases where external memory has areas which overlap areas in internal memory, the external memory areas can be accessed accordance with the $\overline{CE}$ signal output by the external device.

Note: Be careful with the system, such that an external device does not become the bus master, other than during the bus release status. After setting the $\overline{BREQ}$ terminal to LOW level, hold the $\overline{BREQ}$ terminal at LOW level until the $\overline{BACK}$ terminal becomes LOW level. If the $\overline{BREQ}$ terminal is returned to HIGH level, before the $\overline{BACK}$ terminal becomes LOW level, the shift to the bus authorization release status will become indefinite.

6.6 Stack Page Setting

Although the stack area used to evacuate registers during subroutine calls can be arbitrarily moved to any area in data RAM using the stack pointer SP, its page address is set in registers SPP0–SPP7 in I/O memory.
At initial reset, SPP0–SPP7 are set to "00H" (page 0).

Since the internal RAM is arranged on page 0 (00C000H–00DFFFH), the stack area in single chip mode is inevitably located in page 0.
In order to place the stack area at the final address in internal RAM, the stack pointer SP is placed at an initial setting of "E000H". (SP is pre-decremented.)

In the expansion mode, to place the stack in external expanded RAM, set a corresponding page to SPP0–SPP7. The page addresses to which SPP0–SPP7 can be set are 00H–27H and must be within a RAM area.

* A page is each recurrent 64K division of data memory beginning at address zero.

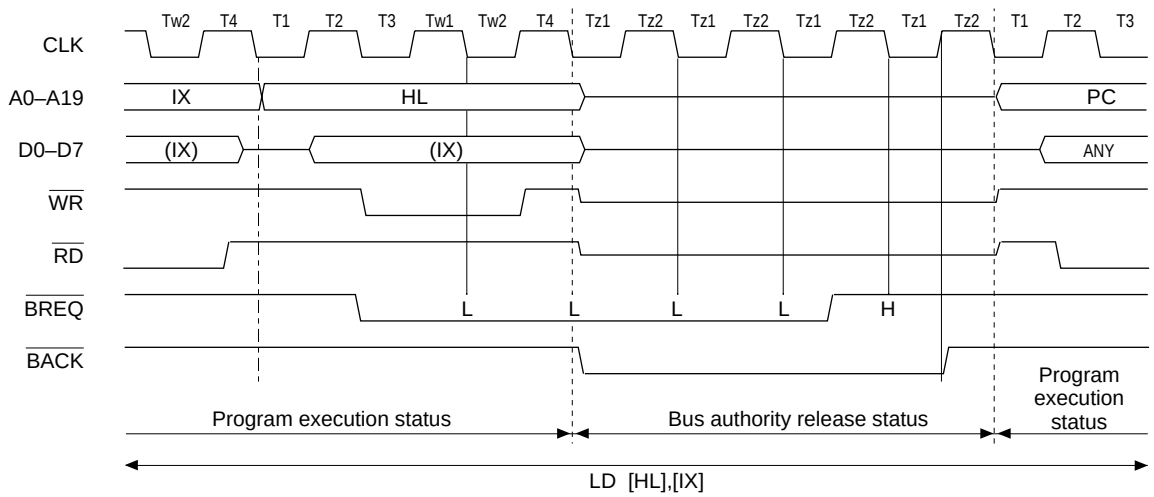


Fig. 6.5.1 Bus authority release sequence

6.7 Details of Control Registers

Table 6.7.1 shows the control bits for the system controller.

Table 6.7.1 System controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00 (MCU)	D7	BUSMOD	Bus mode	Expansion	Single chip	0	R/W	
	D6	CPUMOD	CPU mode	Maximum	Minimum	0	R/W	
	D5	–	–	–	–	–	–	Constantly "0" when being read
	D4	–	–	–	–	–	–	
	D3	CE3	$\overline{CE3}$ (R33)	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	In Single chip mode, these setting are fixed at DC output.
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30)	$\overline{CE0}$ enable	$\overline{CE0}$ disable	0	R/W	
			$\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output					
00FF00 (MPU)	D7	BUSMOD	Bus mode	Expansion	–	1	R	Expansion mode only
	D6	CPUMOD	CPU mode	Maximum	Minimum	0	R/W	
	D5	–	–	–	–	–	–	Constantly "0" when being read
	D4	–	–	–	–	–	–	
	D3	CE3	$\overline{CE3}$ (R33)	$\overline{CE3}$ enable	$\overline{CE3}$ disable	0	R/W	
	D2	CE2	$\overline{CE2}$ (R32)	$\overline{CE2}$ enable	$\overline{CE2}$ disable	0	R/W	
	D1	CE1	$\overline{CE1}$ (R31)	$\overline{CE1}$ enable	$\overline{CE1}$ disable	0	R/W	
	D0	CE0	$\overline{CE0}$ (R30)	$\overline{CE0}$ enable	–	1	R	
			$\overline{CE}$ signal output Enable/Disable Enable: $\overline{CE}$ signal output Disable: DC (R3x) output					
00FF01	D7	SPP7	Stack pointer page address (MSB)	1	0	0	R/W	
	D6	SPP6		1	0	0	R/W	
	D5	SPP5	< SP page allocatable address >	1	0	0	R/W	
	D4	SPP4	• Single chip mode: only 0 page	1	0	0	R/W	
	D3	SPP3	• Expansion mode: 0–27H page	1	0	0	R/W	
	D2	SPP2		1	0	0	R/W	
	D1	SPP1		1	0	0	R/W	
	D0	SPP0	(LSB)	1	0	0	R/W	
00FF02	D7	EBR	Bus release enable register (P24 and P25 terminal specification) P24	$\overline{BREQ}$	–	0	R/W	
			P25	$\overline{BACK}$	–			
	D6	WT2	Wait control register			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CLKCHG	CPU operating clock switch	OSC3	OSC1	1	R/W	∗1
	D1	SOSC3	OSC3 oscillation On/Off control	On	Off	1	R/W	∗2
	D0	SOSC1	OSC1 oscillation On/Off control	On	Off	1	R/W	∗3

WT2	WT1	WT0	Number of state
1	1	1	14
1	1	0	12
1	0	1	10
1	0	0	8
0	1	1	6
0	1	0	4
0	0	1	2
0	0	0	No wait

∗1 CLKCHG cannot be set to "0" when SOSC1 = "0" (OSC1 oscillation is OFF) and cannot be set to "1" when SOSC3 = "0" (OSC3 oscillation is OFF).

∗2 Cannot be turned OFF when the CPU is running with the OSC3 clock.

∗3 Cannot be turned OFF when the CPU is running with the OSC1 clock or the watchdog timer is enabled.

Note: All the interrupts including $\overline{NMI}$ are disabled, until you write the optional value into both the "00FF00H" and "00FF01H" addresses.

BUSMOD, CPUMOD: 00FF00H•D7, D6

Bus mode and CPU mode are set as shown in Table 6.7.2.

Table 6.7.2 Bus mode and CPU mode settings

MCU/$\overline{\text{MPU}}$ terminal	Setting value		Bus mode	CPU mode
	BUSMOD	CPUMOD		
1 (MCU mode)	1	1	Expansion	Maximum
	1	0		Minimum
	0	1	Single chip	Maximum
	0	0		Minimum
0 (MPU mode)	1	1	Expansion	Maximum
	1	0		Minimum
	0	1		Maximum
	0	0		Minimum

The single chip mode configuration is only possible when this IC is used in the MCU mode. The single chip mode setting is incompatible with the MPU mode, since this mode does not utilize internal ROM.
At initial reset, in the MCU mode the unit is set to single chip (minimum) mode and in the MPU mode the expansion (minimum) mode is used to select the applicable mode.

CE0–CE3: 00FF00H•D0–D3

Sets the $\overline{\text{CE}}$ output terminals being used.

When "1" is written: $\overline{\text{CE}}$ output enable
When "0" is written: $\overline{\text{CE}}$ output disable
Reading: Valid

$\overline{\text{CE}}$ output is enabled when a "1" is written to registers CE0–CE3 which correspond to the $\overline{\text{CE}}$ output being used. A "0" written to any of the registers disables $\overline{\text{CE}}$ signal output from that terminal and it reverts to its alternate function as an output port terminal (R30–R33).
In the MPU mode, CE0 is fixed at "1" as a read-only register.
At initial reset, register CE0 is set to "0" in the MCU mode and in the MPU mode, "1" is set in the register. Registers CE1–CE3 are set to "0" regardless of the MCU / MPU mode setting.

Note: To avoid a malfunction from an interrupt generated before the bus configuration is initialized, all interrupts including $\overline{\text{NMI}}$ are masked until you write an optional value into address "00FF00H".

SPP0–SPP7: 00FF01H

Sets the page address of stack area.
In single chip mode, set page address to "00H". In expansion mode, it can be set to any value within the range "00H"–"27H".
Since a carry and borrow from / to the stack pointer SP is not reflected in register SPP, the upper limit on continuous use of the stack area is 64K bytes.
At initial reset, this register is set to "00H" (page 0).

Note: To avoid a malfunction from an interrupt generated before the bus configuration is initialized, all interrupts including $\overline{\text{NMI}}$ are disabled, until you write an optional value into "00FF01H" address. Furthermore, to avoid generating an interrupt while the stack area is being set, all interrupts including $\overline{\text{NMI}}$ are disabled in one instruction execution period after writing to address "00FF01H".

WT0–WT2: 00FF02H•D4–D6

How WAIT state settings are performed.
The number of WAIT states to be inserted based on register settings is as shown in Table 6.7.3.

Table 6.7.3 Setting WAIT states

WT2	WT1	WT0	Number of inserted states
1	1	1	14
1	1	0	12
1	0	1	10
1	0	0	8
0	1	1	6
0	1	0	4
0	0	1	2
0	0	0	No wait

* The length of one state is a 1/2 clock cycle.

At initial reset, this register is set to "0" (no wait).

EBR: 00FF02H•D7

Sets the $\overline{\text{BREQ}}$ / $\overline{\text{BACK}}$ terminals function.

When "1" is written: $\overline{\text{BREQ}}$ / $\overline{\text{BACK}}$ enabled
When "0" is written: $\overline{\text{BREQ}}$ / $\overline{\text{BACK}}$ disabled
Reading: Valid

How $\overline{\text{BREQ}}$ and $\overline{\text{BACK}}$ terminal functions are set. Writing "1" to EBR enables $\overline{\text{BREQ}}$ / $\overline{\text{BACK}}$ input / output. Writing "0" sets the $\overline{\text{BREQ}}$ terminal as the P24 port terminal and the $\overline{\text{BACK}}$ terminal as the P25 port terminal.
At initial reset, EBR is set to "0" ($\overline{\text{BREQ}}$ / $\overline{\text{BACK}}$ disabled).

6.8 Precautions

(1) All the interrupts including $\overline{\text{NMI}}$ are masked, until you write the optional value into both the "00FF00H" and "00FF01H" addresses. Consequently, even if you do not change the content of this address (You use the initial value, as is.), you should still be sure to perform the writing operation using the initialization routine.

(2) When setting stack fields, including page addresses as well, you should write them in the order of the register SPP ("00FF01H") and the stack pointer SP.

Example: When setting the "178000H" address

```
LD    EP, #00H
LD    HL, #0FF01H
LD    [HL], #17H
LD    SP, #8000H
```

During this period the interrupts (including $\overline{\text{NMI}}$) are masked.

7 INTERRUPT AND STANDBY STATUS

■ Types of interrupts

4 systems and 34 types of interrupts have been provided for the S1C88655.

External interrupt
- P20–P27 input interrupt (8 types)

Internal interrupt
- Clock timer interrupt (4 types)
- Programmable timer interrupt (16 types)
- Serial interface interrupt (6 types)

Each interrupt source provides an interrupt factor flag that indicates occurrence of an interrupt factor and an interrupt enable register that enables / disables interrupt requests for controlling interrupt generation. In addition, an interrupt priority register has been provided for each interrupt system allowing interrupt handler routines to set the priority of each interrupt system to 3 levels.
Figure 7.1 shows the configuration of the interrupt circuit.
Refer to the explanations of the respective peripheral circuits for details on each interrupt.

■ HALT mode

When the program executes the HALT instruction, the S1C88655 enters HALT mode.
Since the CPU stops operating in HALT mode, power consumption can be reduced with only peripheral circuit operation.
The HALT mode is cancelled by initial reset or an interrupt request, and the CPU restarts program execution from an exception handler routine.
See the "S1C88 Core CPU Manual" for the HALT mode and reactivation sequence.

■ SLEEP mode

When the program executes the SLP instruction, the S1C88655 enters SLEEP mode.
Since the CPU and peripheral circuits stop operating completely in SLEEP mode, power consumption can be reduced even more than in HALT mode.
The SLEEP mode is cancelled by initial reset or an input interrupt from the port. The CPU reactivates after waiting 128 / f_{OSC1} or 512 / f_{OSC3} seconds of oscillation stabilization time (the oscillation stabilization time varies depending on the operating clock being used when the SLP instruction is executed). At this time, the CPU restarts program execution from an exception handler routine (input interrupt routine).

Note: The oscillation becomes unstable for a while after SLEEP status is cancelled, the wait time for restarting the CPU may be longer than 128/f_{OSC1} or 512/f_{OSC3} seconds.

7.1 Interrupt Generation Conditions

The interrupt factor flags that indicate occurrence of their respective interrupt factors are provided for the previously indicated 4 systems and 34 types of interrupts. They will be set to "1" when the corresponding interrupt factor occurs.
In addition, interrupt enable registers with a 1 to 1 correspondence to each of the interrupt factor flags are provided. An interrupt is enabled when "1" is written and interrupt is disabled when "0" is written.

The CPU manages the enable / disable of interrupt requests at the interrupt priority level. An interrupt priority register that sets the priority level is provided for each of the interrupts of the 4 systems and the CPU accepts only interrupts above the level that has been indicated with the interrupt flags (I0 and I1).
Consequently, the following three conditions are necessary for the CPU to accept the interrupt.

(1) The interrupt factor flag has been set to "1" by generation of an interrupt factor.

(2) The interrupt enable register corresponding to the above has been set to "1".

(3) The interrupt priority register corresponding to the above has been set to a priority level higher than the interrupt flag (I0 and I1) setting.

The CPU initially samples the interrupt for the first op-code fetch cycle of each instruction. Thereupon, the CPU shifts to the exception processing when the above mentioned conditions have been established.
See the "S1C88 Core CPU Manual" for the exception processing sequence.

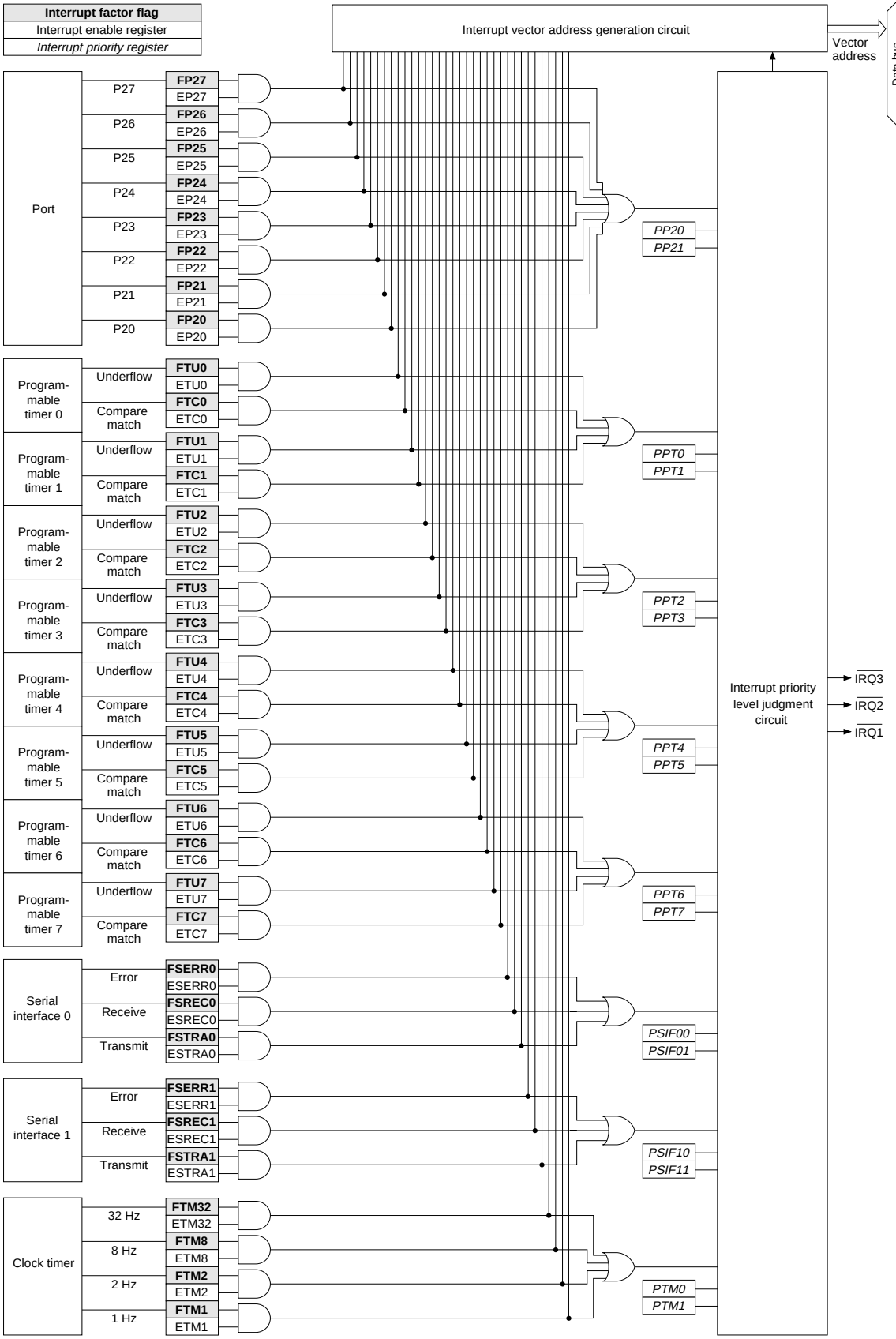


Fig. 7.1 Configuration of interrupt circuit

7.2 Interrupt Factor Flag

Table 7.2.1 shows the correspondence between the factors generating an interrupt and the interrupt factor flags.
The corresponding interrupt factor flags are set to "1" by generation of the respective interrupt factors. The corresponding interrupt factor can be confirmed by reading the flags through software.
Interrupt factor flag that has been set to "1" is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are reset to "0".

Note: When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

Table 7.2.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
P27 input (falling edge or rising edge specified with PCP27)	FP27	00FF1AH·D7
P26 input (falling edge or rising edge specified with PCP26)	FP26	00FF1AH·D6
P25 input (falling edge or rising edge specified with PCP25)	FP25	00FF1AH·D5
P24 input (falling edge or rising edge specified with PCP24)	FP24	00FF1AH·D4
P23 input (falling edge or rising edge specified with PCP23)	FP23	00FF1AH·D3
P22 input (falling edge or rising edge specified with PCP22)	FP22	00FF1AH·D2
P21 input (falling edge or rising edge specified with PCP21)	FP21	00FF1AH·D1
P20 input (falling edge or rising edge specified with PCP20)	FP20	00FF1AH·D0
Programmable timer 0 compare match	FTC0	00FF1BH·D0
Programmable timer 0 underflow	FTU0	00FF1BH·D1
Programmable timer 1 underflow	FTU1	00FF1BH·D2
Programmable timer 1 compare match	FTC1	00FF1BH·D3
Programmable timer 2 underflow	FTU2	00FF1BH·D4
Programmable timer 2 compare match	FTC2	00FF1BH·D5
Programmable timer 3 underflow	FTU3	00FF1BH·D6
Programmable timer 3 compare match	FTC3	00FF1BH·D7
Programmable timer 4 underflow	FTU4	00FF1EH·D0
Programmable timer 4 compare match	FTC4	00FF1EH·D1
Programmable timer 5 underflow	FTU5	00FF1EH·D2
Programmable timer 5 compare match	FTC5	00FF1EH·D3
Programmable timer 6 underflow	FTU6	00FF1EH·D4
Programmable timer 6 compare match	FTC6	00FF1EH·D5
Programmable timer 7 underflow	FTU7	00FF1EH·D6
Programmable timer 7 compare match	FTC7	00FF1EH·D7
Serial interface 0 receiving error (in asynchronous mode)	FSERR0	00FF1CH·D2
Serial interface 0 receiving completion	FSREC0	00FF1CH·D1
Serial interface 0 transmitting completion	FSTRA0	00FF1CH·D0
Serial interface 1 receiving error (in asynchronous mode)	FSERR1	00FF1CH·D5
Serial interface 1 receiving completion	FSREC1	00FF1CH·D4
Serial interface 1 transmitting completion	FSTRA1	00FF1CH·D3
Clock timer 32 Hz signal (falling edge)	FTM32	00FF1DH·D3
Clock timer 8 Hz signal (falling edge)	FTM8	00FF1DH·D2
Clock timer 2 Hz signal (falling edge)	FTM2	00FF1DH·D1
Clock timer 1 Hz signal (falling edge)	FTM1	00FF1DH·D0

7.3 Interrupt Enable Register

The interrupt enable register has a 1 to 1 correspondence with each interrupt factor flag and enable / disable of interrupt requests can be set.

When "1" is written to the interrupt enable register, an interrupt request is enabled, and is disabled when "0" is written.

This register also permits reading, thus making it possible to confirm that a status has been set.
At initial reset, the interrupt enable registers are set to "0" and shifts to the interrupt disable status.
Table 7.3.1 shows the correspondence between the interrupt enable registers and the interrupt factor flags.

Table 7.3.1 Interrupt enable registers and interrupt factor flags

Interrupt	Interrupt factor flag		Interrupt enable register	
P27 input	FP27	00FF1AH·D7	EP27	00FF14H·D7
P26 input	FP26	00FF1AH·D6	EP26	00FF14H·D6
P25 input	FP25	00FF1AH·D5	EP25	00FF14H·D5
P24 input	FP24	00FF1AH·D4	EP24	00FF14H·D4
P23 input	FP23	00FF1AH·D3	EP23	00FF14H·D3
P22 input	FP22	00FF1AH·D2	EP22	00FF14H·D2
P21 input	FP21	00FF1AH·D1	EP21	00FF14H·D1
P20 input	FP20	00FF1AH·D0	EP20	00FF14H·D0
Timer 0 compare match	FTC0	00FF1BH·D0	ETC0	00FF15H·D0
Timer 0 underflow	FTU0	00FF1BH·D1	ETU0	00FF15H·D1
Timer 1 underflow	FTU1	00FF1BH·D2	ETU1	00FF15H·D2
Timer 1 compare match	FTC1	00FF1BH·D3	ETC1	00FF15H·D3
Timer 2 underflow	FTU2	00FF1BH·D4	ETU2	00FF15H·D4
Timer 2 compare match	FTC2	00FF1BH·D5	ETC2	00FF15H·D5
Timer 3 underflow	FTU3	00FF1BH·D6	ETU3	00FF15H·D6
Timer 3 compare match	FTC3	00FF1BH·D7	ETC3	00FF15H·D7
Timer 4 underflow	FTU4	00FF1EH·D0	ETU4	00FF18H·D0
Timer 4 compare match	FTC4	00FF1EH·D1	ETC4	00FF18H·D1
Timer 5 underflow	FTU5	00FF1EH·D2	ETU5	00FF18H·D2
Timer 5 compare match	FTC5	00FF1EH·D3	ETC5	00FF18H·D3
Timer 6 underflow	FTU6	00FF1EH·D4	ETU6	00FF18H·D4
Timer 6 compare match	FTC6	00FF1EH·D5	ETC6	00FF18H·D5
Timer 7 underflow	FTU7	00FF1EH·D6	ETU7	00FF18H·D6
Timer 7 compare match	FTC7	00FF1EH·D7	ETC7	00FF18H·D7
Serial interface 0 receiving error	FSERR0	00FF1CH·D2	ESERR0	00FF16H·D2
Serial interface 0 receiving completion	FSREC0	00FF1CH·D1	ESREC0	00FF16H·D1
Serial interface 0 transmitting completion	FSTRA0	00FF1CH·D0	ESTRA0	00FF16H·D0
Serial interface 1 receiving error	FSERR1	00FF1CH·D5	ESERR1	00FF16H·D5
Serial interface 1 receiving completion	FSREC1	00FF1CH·D4	ESREC1	00FF16H·D4
Serial interface 1 transmitting completion	FSTRA1	00FF1CH·D3	ESTRA1	00FF16H·D3
Clock timer 32 Hz	FTM32	00FF1DH·D3	ETM32	00FF17H·D3
Clock timer 8 Hz	FTM8	00FF1DH·D2	ETM8	00FF17H·D2
Clock timer 2 Hz	FTM2	00FF1DH·D1	ETM2	00FF17H·D1
Clock timer 1 Hz	FTM1	00FF1DH·D0	ETM1	00FF17H·D0

7.4 Interrupt Priority Register and Interrupt Priority Level

Table 7.4.1 Interrupt priority register

Interrupt	Interrupt priority register	
P20–P27 input interrupt	PP20, PP21	00FF10·D0, D1
Programmable timer interrupt 1–0	PPT0, PPT1	00FF10·D4, D5
Programmable timer interrupt 3–2	PPT2, PPT3	00FF10·D2, D3
Programmable timer interrupt 5–4	PPT4, PPT5	00FF11·D6, D7
Programmable timer interrupt 7–6	PPT6, PPT7	00FF11·D4, D5
Serial interface 0 interrupt	PSIF00, PSIF01	00FF10·D6, D7
Serial interface 1 interrupt	PSIF10, PSIF11	00FF11·D0, D1
Clock timer interrupt	PTM0, PTM1	00FF11·D2, D3

The interrupt priority registers shown in Table 7.4.1 are provided for each system of interrupts and the interrupt priority levels for the CPU can be set to the optional priority level (0–3). As a result, it is possible to have multiple interrupts that match the system's interrupt processing priority levels.

The interrupt priority level between each system can optionally be set to three levels by the interrupt priority register. However, when more than one system is set to the same priority level, they are processed according to the default priority level.

Table 7.4.2 Setting of interrupt priority level

P*1	P*0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, the interrupt priority registers are all set to "0" and each interrupt is set to level 0. Furthermore, the priority levels in each system have been previously decided and they cannot be changed.

The CPU can mask each interrupt by setting the interrupt flags (I0 and I1). The relation between the interrupt priority level of each system and interrupt flags is shown in Table 7.4.3, and the CPU accepts only interrupts above the level indicated by the interrupt flags.

The $\overline{NMI}$ (watchdog timer) that has level 4 priority, is always accepted regardless of the setting of the interrupt flags.

Table 7.4.3 Interrupt mask setting of CPU

I1	I0	Acceptable interrupt
1	1	Level 4 ($\overline{NMI}$)
1	0	Level 4, Level 3 ($\overline{IRQ3}$)
0	1	Level 4, Level 3, Level 2 ($\overline{IRQ2}$)
0	0	Level 4, Level 3, Level 2, Level 1 ($\overline{IRQ1}$)

After an interrupt has been accepted, the interrupt flags are written to the level of that interrupt. However, interrupt flags after an $\overline{NMI}$ has been accepted are written to level 3 (I0 = I1 = "1").

Table 7.4.4 Interrupt flags after acceptance of interrupt

Accepted interrupt priority level		I1	I0
Level 4	($\overline{NMI}$)	1	1
Level 3	($\overline{IRQ3}$)	1	1
Level 2	($\overline{IRQ2}$)	1	0
Level 1	($\overline{IRQ1}$)	0	1

The set interrupt flags are reset to their original value on return from the interrupt processing routine. Consequently, multiple interrupts up to 3 levels can be controlled by the initial settings of the interrupt priority registers alone. Additional multiplexing can be realized by rewriting the interrupt flags and interrupt enable register in the interrupt processing routine.

Note: Beware. If the interrupt flags have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

7.5 Exception Processing Vectors

When the CPU accepts an interrupt request, it starts exception processing following completion of the instruction being executed. In exception processing, the following operations branch the program.

(1) In the minimum mode, the program counter (PC) and system condition flag (SC) are moved to stack and in the maximum mode, the code bank register (CB), PC and SC are moved.

(2) The branch destination address is read from the exception processing vector corresponding to each exception processing (interrupt) factor and is placed in the PC.

An exception vector is 2 bytes of data in which the top address of each exception (interrupt) processing routine has been stored and the vector addresses correspond to the exception processing factors as shown in Table 7.5.1.

Note: An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the top portion of an exception processing routine must be described within the common area (000000H–007FFFH).

Table 7.5.1 Vector address and exception processing correspondence

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	P27 input interrupt	
000008H	P26 input interrupt	
00000AH	P25 input interrupt	
00000CH	P24 input interrupt	
00000EH	P23 input interrupt	
000010H	P22 input interrupt	
000012H	P21 input interrupt	
000014H	P20 input interrupt	
000016H	PTM 3 compare match interrupt	
000018H	PTM 3 underflow interrupt	
00001AH	PTM 2 compare match interrupt	
00001CH	PTM 2 underflow interrupt	
00001EH	PTM 1 compare match interrupt	
000020H	PTM 1 underflow interrupt	
000022H	PTM 0 underflow interrupt	
000024H	PTM 0 compare match interrupt	
000026H	Serial I/F 0 error interrupt	
000028H	Serial I/F 0 receiving complete interrupt	
00002AH	Serial I/F 0 transmitting complete interrupt	
00002CH	Serial I/F 1 error interrupt	
00002EH	Serial I/F 1 receiving complete interrupt	
000030H	Serial I/F 1 transmitting complete interrupt	
000032H	Clock timer 32 Hz interrupt	
000034H	Clock timer 8 Hz interrupt	
000036H	Clock timer 2 Hz interrupt	
000038H	Clock timer 1 Hz interrupt	
00003AH	PTM 7 compare match interrupt	
00003CH	PTM 7 underflow interrupt	
00003EH	PTM 6 compare match interrupt	
000040H	PTM 6 underflow interrupt	
000042H	PTM 5 compare match interrupt	
000044H	PTM 5 underflow interrupt	
000046H	PTM 4 compare match interrupt	↓
000048H	PTM 4 underflow interrupt	Low
00004AH	System reserved (cannot be used)	No priority rating
00004CH : 0000FEH	Software interrupt	

7.6 Details of Control Registers

Table 7.6.1 shows the interrupt control bits.

Table 7.6.1(a) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF10	D7	PSIF01	Serial interface 0 interrupt priority register	PSIF01 PSIF00		0	R/W	
	D6	PSIF00						
	D5	PPT1	Programmable timer 1–0 interrupt	PPT1 PPT0		0	R/W	
	D4	PPT0	priority register	PPT3 PPT2	Priority			
	D3	PPT3	Programmable timer 3–2 interrupt	PP21 PP20	level	0	R/W	
	D2	PPT2	priority register	1 1	Level 3			
	D1	PP21	P20–P27 interrupt priority register	1 0	Level 2	0	R/W	
	D0	PP20		0 1	Level 1			
				0 0	Level 0			
00FF11	D7	PPT5	Programmable timer 5–4 interrupt	PPT5 PPT4		0	R/W	
	D6	PPT4	priority register	PPT7 PPT6				
	D5	PPT7	Programmable timer 7–6 interrupt	PTM1 PTM0	Priority	0	R/W	
	D4	PPT6	priority register	PSIF11 PSIF10	level			
	D3	PTM1	Clock timer interrupt priority register	1 1	Level 3	0	R/W	
	D2	PTM0		1 0	Level 2			
	D1	PSIF11	Serial interface 1 interrupt priority register	0 1	Level 1	0	R/W	
	D0	PSIF10		0 0	Level 0			
00FF14	D7	EP27	P27 interrupt enable					
	D6	EP26	P26 interrupt enable					
	D5	EP25	P25 interrupt enable					
	D4	EP24	P24 interrupt enable	Interrupt	Interrupt	0	R/W	
	D3	EP23	P23 interrupt enable	enable	disable			
	D2	EP22	P22 interrupt enable					
	D1	EP21	P21 interrupt enable					
	D0	EP20	P20 interrupt enable					
00FF15	D7	ETC3	PTM3 compare match interrupt enable					
	D6	ETU3	PTM3 underflow interrupt enable					
	D5	ETC2	PTM2 compare match interrupt enable					
	D4	ETU2	PTM2 underflow interrupt enable	Interrupt	Interrupt	0	R/W	
	D3	ETC1	PTM1 compare match interrupt enable	enable	disable			
	D2	ETU1	PTM1 underflow interrupt enable					
	D1	ETU0	PTM0 underflow interrupt enable					
	D0	ETC0	PTM0 compare match interrupt enable					
00FF16	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	ESERR1	Serial I/F 1 (error) interrupt enable					
	D4	ESREC1	Serial I/F 1 (receive) interrupt enable			0	R/W	
	D3	ESTRA1	Serial I/F 1 (transmit) interrupt enable	Interrupt	Interrupt			
	D2	ESERR0	Serial I/F 0 (error) interrupt enable	enable	disable			
	D1	ESREC0	Serial I/F 0 (receive) interrupt enable			0	R/W	
	D0	ESTRA0	Serial I/F 0 (transmit) interrupt enable					
00FF17	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	–	–	–	–	R	
	D3	ETM32	Clock timer 32 Hz interrupt enable					
	D2	ETM8	Clock timer 8 Hz interrupt enable	Interrupt	Interrupt	0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable	enable	disable			
	D0	ETM1	Clock timer 1 Hz interrupt enable					

Table 7.6.1(b) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF18	D7	ETC7	PTM7 compare match interrupt enable	Interrupt enable	Interrupt disable	0	R/W	
	D6	ETU7	PTM7 underflow interrupt enable					
	D5	ETC6	PTM6 compare match interrupt enable					
	D4	ETU6	PTM6 underflow interrupt enable					
	D3	ETC5	PTM5 compare match interrupt enable					
	D2	ETU5	PTM5 underflow interrupt enable					
	D1	ETC4	PTM4 compare match interrupt enable					
	D0	ETU4	PTM4 underflow interrupt enable					
00FF1A	D7	FP27	P27 interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D6	FP26	P26 interrupt factor flag					
	D5	FP25	P25 interrupt factor flag					
	D4	FP24	P24 interrupt factor flag					
	D3	FP23	P23 interrupt factor flag					
	D2	FP22	P22 interrupt factor flag					
	D1	FP21	P21 interrupt factor flag					
	D0	FP20	P20 interrupt factor flag					
00FF1B	D7	FTC3	PTM3 compare match interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D6	FTU3	PTM3 underflow interrupt factor flag					
	D5	FTC2	PTM2 compare match interrupt factor flag					
	D4	FTU2	PTM2 underflow interrupt factor flag					
	D3	FTC1	PTM1 compare match interrupt factor flag					
	D2	FTU1	PTM1 underflow interrupt factor flag					
	D1	FTU0	PTM0 underflow interrupt factor flag					
	D0	FTC0	PTM0 compare match interrupt factor flag					
00FF1C	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	FSERR1	Serial I/F 1 (error) interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D4	FSREC1	Serial I/F 1 (receive) interrupt factor flag					
	D3	FSTRA1	Serial I/F 1 (transmit) interrupt factor flag					
	D2	FSERR0	Serial I/F 0 (error) interrupt factor flag			0	R/W	
	D1	FSREC0	Serial I/F 0 (receive) interrupt factor flag					
	D0	FSTRA0	Serial I/F 0 (transmit) interrupt factor flag					
00FF1D	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	–	–	–	–	R	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag	(R) Occurred (W) Reset	(R) Not occurred (W) No operation	0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag					
	D1	FTM2	Clock timer 2 Hz interrupt factor flag					
	D0	FTM1	Clock timer 1 Hz interrupt factor flag					
00FF1E	D7	FTC7	PTM7 compare match interrupt factor flag	(R) Interrupt factor is occurred (W) Reset	(R) No interrupt factor is occurred (W) No operation	0	R/W	
	D6	FTU7	PTM7 underflow interrupt factor flag					
	D5	FTC6	PTM6 compare match interrupt factor flag					
	D4	FTU6	PTM6 underflow interrupt factor flag					
	D3	FTC5	PTM5 compare match interrupt factor flag					
	D2	FTU5	PTM5 underflow interrupt factor flag					
	D1	FTC4	PTM4 compare match interrupt factor flag					
	D0	FTU4	PTM4 underflow interrupt factor flag					

*P*0, P*1: 00FF10H–00FF11H*

These are the interrupt priority registers used to set the priority level of each interrupt system.
Table 7.6.2 shows the correspondence between the register and interrupt system.

Table 7.6.2 Interrupt priority registers

Register		Interrupt system
PP20, PP21	(00FF10·D0, D1)	P20–P27 input
PPT0, PPT1	(00FF10·D4, D5)	Programmable timers 1–0
PPT2, PPT3	(00FF10·D2, D3)	Programmable timers 3–2
PPT4, PPT5	(00FF11·D6, D7)	Programmable timers 5–4
PPT6, PPT7	(00FF11·D4, D5)	Programmable timers 7–6
PSIF00, PSIF01	(00FF10·D6, D7)	Serial interface 0
PSIF10, PSIF11	(00FF11·D0, D1)	Serial interface 1
PTM0, PTM1	(00FF11·D2, D3)	Clock timer

Table 7.6.3 shows the interrupt priority level that can be set by these registers.

Table 7.6.3 Setting interrupt priority level

P*1	P*0	Interrupt priority level	
1	1	Level 3	($\overline{IRQ3}$)
1	0	Level 2	($\overline{IRQ2}$)
0	1	Level 1	($\overline{IRQ1}$)
0	0	Level 0	(None)

To generate an interrupt, the priority level of the interrupt system must be set higher than the level set with the CPU's interrupt flag (I0, I1) using the interrupt priority register.
Furthermore, when two or more interrupts occur at the same time, the interrupt that has the highest priority set using this register is processed first. If they have the same priority level, the priority order set to the interrupt vectors (see Table 7.5.1) are applied.
At initial reset, the interrupt priority registers are set to "0" (level 0).

E: 00FF14H–00FF18H*

These are the interrupt enable registers that enable or disable to generate an interrupt to the CPU.
Table 7.6.4 shows the correspondence between the register and interrupt factor.

Table 7.6.4 Interrupt enable registers

Register		Interrupt factor
EP27	(00FF14H·D7)	P27 input
EP26	(00FF14H·D6)	P26 input
EP25	(00FF14H·D5)	P25 input
EP24	(00FF14H·D4)	P24 input
EP23	(00FF14H·D3)	P23 input
EP22	(00FF14H·D2)	P22 input
EP21	(00FF14H·D1)	P21 input
EP20	(00FF14H·D0)	P20 input
ETC0	(00FF15H·D0)	PTM 0 compare match
ETU0	(00FF15H·D1)	PTM 0 underflow
ETU1	(00FF15H·D2)	PTM 1 underflow
ETC1	(00FF15H·D3)	PTM 1 compare match
ETU2	(00FF15H·D4)	PTM 2 underflow
ETC2	(00FF15H·D5)	PTM 2 compare match
ETU3	(00FF15H·D6)	PTM 3 underflow
ETC3	(00FF15H·D7)	PTM 3 compare match
ETU4	(00FF18H·D0)	PTM 4 underflow
ETC4	(00FF18H·D1)	PTM 4 compare match
ETU5	(00FF18H·D2)	PTM 5 underflow
ETC5	(00FF18H·D3)	PTM 5 compare match
ETU6	(00FF18H·D4)	PTM 6 underflow
ETC6	(00FF18H·D5)	PTM 6 compare match
ETU7	(00FF18H·D6)	PTM 7 underflow
ETC7	(00FF18H·D7)	PTM 7 compare match
ESERR0	(00FF16H·D2)	Serial I/F 0 receiving error
ESREC0	(00FF16H·D1)	Serial I/F 0 receiving completion
ESTRA0	(00FF16H·D0)	Serial I/F 0 transmitting completion
ESERR1	(00FF16H·D5)	Serial I/F 1 receiving error
ESREC1	(00FF16H·D4)	Serial I/F 1 receiving completion
ESTRA1	(00FF16H·D3)	Serial I/F 1 transmitting completion
ETM32	(00FF17H·D3)	Clock timer 32 Hz
ETM8	(00FF17H·D2)	Clock timer 8 Hz
ETM2	(00FF17H·D1)	Clock timer 2 Hz
ETM1	(00FF17H·D0)	Clock timer 1 Hz

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

When the interrupt enable register is set to "1", the corresponding interrupt is enabled. When the interrupt enable register is set to "0", the interrupt is disabled.
At initial reset, the interrupt enable register is set to "0" (interrupt disabled).

F∗: 00FF1AH–00FF1EH

These are the interrupt factor flags that indicate occurrence of interrupt factors.
Table 7.6.5 shows the correspondence between the flag and interrupt factor.

Table 7.6.5 Interrupt factor flags

Flag		Interrupt factor
FP27	(00FF1AH·D7)	P27 input
FP26	(00FF1AH·D6)	P26 input
FP25	(00FF1AH·D5)	P25 input
FP24	(00FF1AH·D4)	P24 input
FP23	(00FF1AH·D3)	P23 input
FP22	(00FF1AH·D2)	P22 input
FP21	(00FF1AH·D1)	P21 input
FP20	(00FF1AH·D0)	P20 input
FTC0	(00FF1BH·D0)	PTM 0 compare match
FTU0	(00FF1BH·D1)	PTM 0 underflow
FTU1	(00FF1BH·D2)	PTM 1 underflow
FTC1	(00FF1BH·D3)	PTM 1 compare match
FTU2	(00FF1BH·D4)	PTM 2 underflow
FTC2	(00FF1BH·D5)	PTM 2 compare match
FTU3	(00FF1BH·D6)	PTM 3 underflow
FTC3	(00FF1BH·D7)	PTM 3 compare match
FTU4	(00FF1EH·D0)	PTM 4 underflow
FTC4	(00FF1EH·D1)	PTM 4 compare match
FTU5	(00FF1EH·D2)	PTM 5 underflow
FTC5	(00FF1EH·D3)	PTM 5 compare match
FTU6	(00FF1EH·D4)	PTM 6 underflow
FTC6	(00FF1EH·D5)	PTM 6 compare match
FTU7	(00FF1EH·D6)	PTM 7 underflow
FTC7	(00FF1EH·D7)	PTM 7 compare match
FSERR0	(00FF1CH·D2)	Serial I/F 0 receiving error
FSREC0	(00FF1CH·D1)	Serial I/F 0 receiving completion
FSTRA0	(00FF1CH·D0)	Serial I/F 0 transmitting completion
FSERR1	(00FF1CH·D5)	Serial I/F 1 receiving error
FSREC1	(00FF1CH·D4)	Serial I/F 1 receiving completion
FSTRA1	(00FF1CH·D3)	Serial I/F 1 transmitting completion
FTM32	(00FF1DH·D3)	Clock timer 32 Hz
FTM8	(00FF1DH·D2)	Clock timer 8 Hz
FTM2	(00FF1DH·D1)	Clock timer 2 Hz
FTM1	(00FF1DH·D0)	Clock timer 1 Hz

When "1" is read: Occurred
When "0" is read: Not occurred

When "1" is written: Resets factor flag
When "0" is written: Invalid

The interrupt factor flag is set to "1" when the interrupt generation condition is met.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt factor.

To accept the subsequent interrupt after an interrupt has generated, resetting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag must be reset. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

Refer to the explanations on the respective peripheral circuits for details of the interrupt factor.

7.7 Precautions

(1) When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

(2) Beware. If the interrupt flags (I0 and I1) have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the front portion of an exception processing routine must be described within the common area (000000H–007FFFH).

(4) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

8 OSCILLATION CIRCUITS

8.1 Configuration of Oscillation Circuits

The S1C88655 is twin clock system with two internal oscillation circuits (OSC1 and OSC3). The OSC3 oscillation circuit generates the main-clock to run the CPU and some peripheral circuits in high speed, and the OSC1 oscillation circuit generates the sub-clock for low-power operation. Figure 8.1.1 shows the configuration of the oscillation circuit.

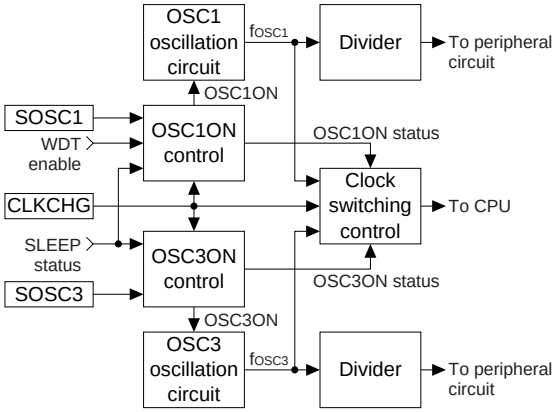


Fig. 8.1.1 Configuration of oscillation circuits

At initial reset, the OSC3 oscillation circuit is selected for the CPU operating clock source. Turning the OSC3 oscillation circuit ON / OFF and switching of the system clock between OSC3 and OSC1 are controlled in software. The OSC3 oscillation circuit is utilized when the CPU and some peripheral circuits must be operated in high speed. Otherwise, OSC1 should be used to generate the operating clock with the OSC3 oscillation circuit stopped in order to reduce current consumption.

8.2 Mask Option

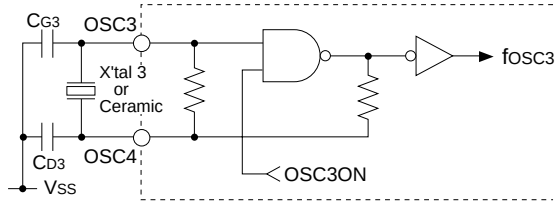
OSC1 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ CR oscillation circuit

OSC3 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ Ceramic oscillation circuit
- ☐ CR oscillation circuit

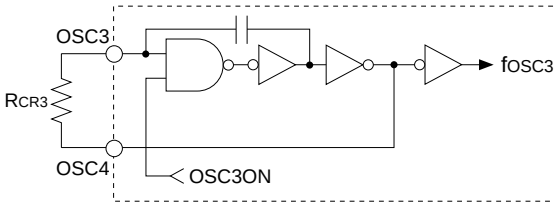
The OSC1 oscillator types can be selected from crystal and CR by mask option. The OSC3 oscillator types can be selected from crystal, ceramic, and CR by mask option.

8.3 OSC3 Oscillation Circuit

The OSC3 oscillation circuit generates the system clock to operate the CPU and some peripheral circuits in high speed.
The OSC3 oscillator types can be selected from crystal, ceramic, and CR by mask option.
Figure 8.3.1 shows the configuration of the OSC3 oscillation circuit.



(1) Crystal/ceramic oscillation circuit



(2) CR oscillation circuit

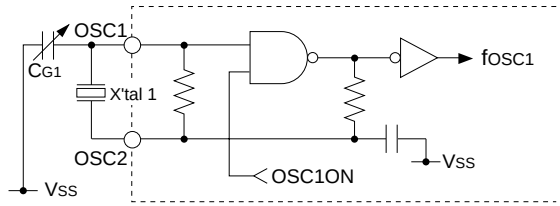
Fig. 8.3.1 OSC3 oscillation circuit

When crystal or ceramic is selected, the crystal or ceramic oscillation circuit are configured by connecting a crystal oscillator (X'tal 3) / ceramic oscillator (Ceramic) between the OSC3 and OSC4 terminals, and connecting two capacitors (C_{G3}, C_{D3}) between the OSC3 terminal and V_{SS} and between the OSC4 terminal and V_{SS}, respectively.
When CR is selected, the CR oscillation circuit is configured simply by connecting a resistor (R_{CR3}) between OSC3 and OSC4 terminals.

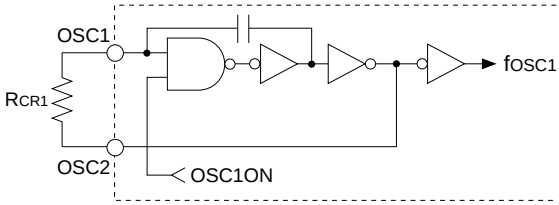
The OSC3 oscillation circuit can be turned ON or OFF using the OSC3 oscillation ON / OFF control register SOSC3. When the system does not need to run at high speed, current consumption can be reduced by turning the OSC3 oscillation OFF after switching the CPU clock to OSC1. While the OSC3 clock is used as the system clock, the OSC3 oscillation circuit cannot be stopped.
Also the OSC3 oscillation circuit stops when the SLP instruction is executed.

8.4 OSC1 Oscillation Circuit

The OSC1 oscillation circuit generates the system clock which is utilized during low speed operation (low power mode) of the CPU and peripheral circuits. Furthermore, even when OSC3 is utilized as the system clock, OSC1 continues to generate the source clock for the clock timer and watchdog timer.
The OSC1 oscillator types can be selected from crystal and CR by mask option.
Figure 8.4.1 shows the configuration of the OSC1 oscillation circuit.



(1) Crystal oscillation circuit



(2) CR oscillation circuit

Fig. 8.4.1 OSC1 oscillation circuit

When crystal is selected, a crystal oscillation circuit can be easily configured by connecting a crystal oscillator (X'tal 1) between the OSC1 and OSC2 terminals along with a trimmer capacitor (C_{G1}) between the OSC1 terminal and V_{SS}.
When CR is selected, the CR oscillation circuit is configured simply by connecting a resistor (R_{CR1}) between OSC1 and OSC2 terminals.

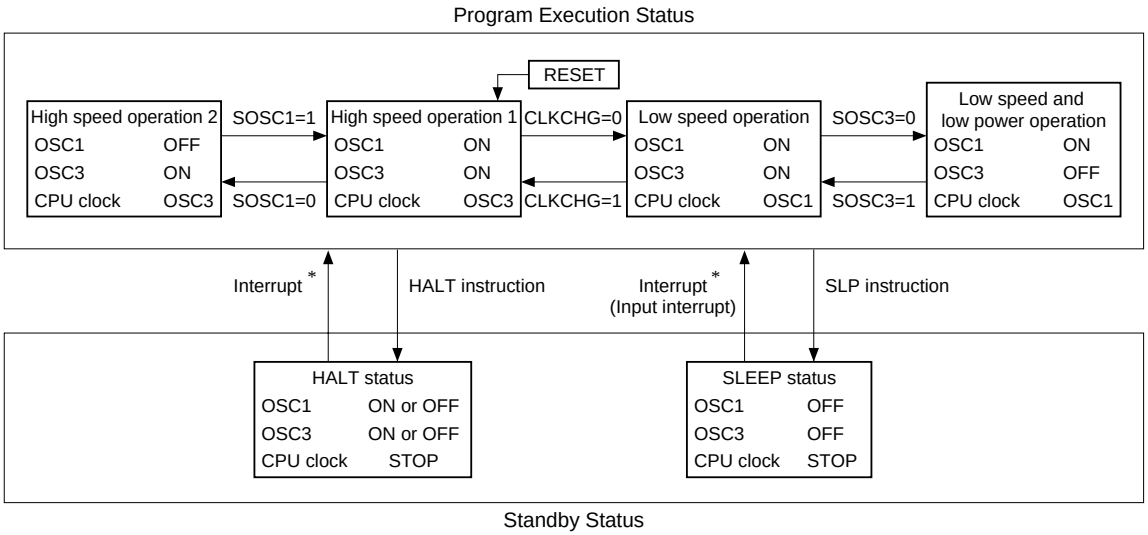
The OSC1 oscillation circuit can be turned ON or OFF using the OSC1 oscillation ON / OFF control register SOSC1. If the system does not need the OSC1 clock when it is running with OSC3 clock, current consumption can be reduced by turning the OSC1 oscillation OFF. When the watchdog timer that uses the OSC1 clock is enabled, the OSC1 oscillation circuit cannot be stopped.
Also the OSC1 oscillation circuit stops when the SLP instruction is executed.

8.5 Switching the CPU Clock

Either OSC1 or OSC3 can be selected as the system clock for running the CPU with software.
The system can save power by turning the OSC3 oscillation circuit OFF while the CPU is running with the OSC1 clock. When the system needs high speed operation, turn the OSC3 oscillation circuit ON and switch the system clock from OSC1 to OSC3. In this case, since several msec to several tens of msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON, you should switch over the clock after stabilization time has elapsed.
When switching over from the OSC3 to the OSC1, turn the OSC3 oscillation circuit OFF immediately following the clock changeover.
When switching the system clock from OSC3 to OSC1 immediately after the power is turned ON, it is necessary to wait for the OSC1 oscillation to stabilize before the clock can be switched. The OSC3 oscillation may take several tens of msec to several seconds until it has completely stabilized. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 19, "Electrical Characteristics".)

Figure 8.5.1 indicates the status transition diagram for the clock changeover.

Note: Be sure to wait long enough that the OSC1 oscillation has stabilized completely before switching the operating clock to OSC1 or starting the timer that uses the OSC1 clock after the OSC1 oscillation circuit is turned ON.
The CPU may start operating before the OSC1 oscillation has stabilized when both the OSC1 and OSC3 oscillation circuits are turned ON since the OSC3 oscillation circuit is able to stabilize in a shorter time than the OSC1 oscillation circuit.



* The return destination from the standby status becomes the program execution status prior to shifting to the standby status.

Fig. 8.5.1 Status transition diagram for the clock changeover

8.6 Clock Output (FOUT)

In order for the S1C88655 to provide a clock to an external device, a FOUT signal (oscillation clock fOSC1 or fOSC3 dividing clock) can be output from the P22 port terminal.
The FOUT signal output is controlled by the register FOUTON. When FOUTON is set to "1", the FOUT signal is output from the P22 port terminal, when "0" is set, the port is set to the status according to the P22 port registers. While the FOUT signal is output (FOUTON is "1"), settings of the I/O control register IOC22 and data register P22D become invalid.
The frequency of the FOUT signal can be selected from among eight settings as shown in Table 8.6.1 using the registers FOUT0–FOUT2.

Table 8.6.1 FOUT frequency setting

FOUT2	FOUT1	FOUT0	FOUT frequency
1	1	1	fOSC3 / 8
1	1	0	fOSC3 / 4
1	0	1	fOSC3 / 2
1	0	0	fOSC3 / 1
0	1	1	fOSC1 / 8
0	1	0	fOSC1 / 4
0	0	1	fOSC1 / 2
0	0	0	fOSC1 / 1

fOSC1: OSC1 oscillation frequency
fOSC3: OSC3 oscillation frequency

When the selected clock source is not activated, the oscillation circuit must be turned ON before starting the FOUT output. An oscillation stabilization waiting time is required after the OSC3 or OSC1 oscillation circuit is turned ON. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the oscillation, before outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 19, "Electrical Characteristics".)
Since the FOUT signal is generated asynchronously from the register FOUTON, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 8.6.1 shows the output waveform of the FOUT signal.

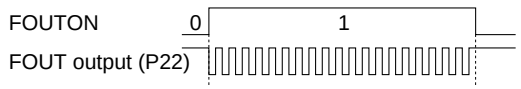


Fig. 8.6.1 Output waveform of FOUT signal

See Chapter 10, "I/O Ports (P Ports)", for the P22 port registers.

8.7 Details of Control Registers

Table 8.7.1 shows the control bits for the oscillation circuits.

Table 8.7.1 Oscillation circuit control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF02	D7	EBR	Bus release enable register P24 (P24 and P25 terminal specification) P25	$\overline{BREQ}$ $\overline{BACK}$	– –	0	R/W	
	D6	WT2	Wait control register WT2 WT1 WT0 Number of state 1 1 1 14 1 1 0 12 1 0 1 10 1 0 0 8 0 1 1 6 0 1 0 4 0 0 1 2 0 0 0 No wait			0	R/W	
	D5	WT1				0	R/W	
	D4	WT0				0	R/W	
	D3	–	–	–	–	–	–	"0" when being read
	D2	CLKCHG	CPU operating clock switch	OSC3	OSC1	1	R/W	∗1
	D1	SOSC3	OSC3 oscillation On/Off control	On	Off	1	R/W	∗2
	D0	SOSC1	OSC1 oscillation On/Off control	On	Off	1	R/W	∗3
00FF04	D7	FOUTON	FOUT output control	On	Off	0	R/W	
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 1 1 1 f_{OSC3} / 8 1 1 0 f_{OSC3} / 4 1 0 1 f_{OSC3} / 2 1 0 0 f_{OSC3} / 1 0 1 1 f_{OSC1} / 8 0 1 0 f_{OSC1} / 4 0 0 1 f_{OSC1} / 2 0 0 0 f_{OSC1} / 1			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	–	–	–	–	–	–	Constantly "0" when
	D2	–	–	–	–	–	–	being read
	D1	–	–	–	–	–	–	
	D0	WDRST	Watchdog timer reset	Reset	No operation	–	W	

∗1 CLKCHG cannot be set to "0" when SOSC1 = "0" (OSC1 oscillation is OFF) and cannot be set to "1" when SOSC3 = "0" (OSC3 oscillation is OFF).

∗2 Cannot be turned OFF when the CPU is running with the OSC3 clock.

∗3 Cannot be turned OFF when the CPU is running with the OSC1 clock or the watchdog timer is enabled.

SOSC1: 00FF02H•D0

Turns the OSC1 oscillation circuit ON or OFF.

When "1" is written: OSC1 oscillation ON
When "0" is written: OSC1 oscillation OFF
Reading: Valid

If the system does not need the OSC1 clock when it is running with OSC3 clock, set SOSC1 to "0" to reduce current consumption. When the system is running with the OSC1 clock or the watchdog timer that uses the OSC1 clock is enabled, the OSC1 oscillation circuit cannot be stopped. Also the OSC1 oscillation circuit stops when the SLP instruction is executed.
At initial reset, SOSC1 is set to "1" (OSC1 oscillation ON).

SOSC3: 00FF02H•D1

Turns the OSC3 oscillation circuit ON or OFF.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When the CPU and some peripheral circuits are to be operated at high speed, set SOSC3 to "1". Otherwise, it should be set to "0" in order to reduce current consumption. When the system is running with the OSC3 clock, the OSC3 oscillation circuit cannot be stopped. Also the OSC3 oscillation circuit stops when the SLP instruction is executed.
At initial reset, SOSC3 is set to "1" (OSC3 oscillation ON).

CLKCHG: 00FF02H•D2

Selects the operating clock for the CPU.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The CPU runs with the OSC3 clock when CLKCHG is set to "1" or with the OSC1 clock when it is set to "0". However, CLKCHG cannot be set to "0" when SOSC1 = "0" (OSC1 oscillation is OFF) and cannot be set to "1" when SOSC3 = "0" (OSC3 oscillation is OFF).
At initial reset, CLKCHG is set to "1" (OSC3 clock).

FOUTON: 00FF04H•D7

Controls the FOUT (f_{OSC1} / f_{OSC3} dividing clock) signal output.

When "1" is written: FOUT signal output
When "0" is written: P22 port
Reading: Valid

FOUTON is the output control register for FOUT signal. When "1" is set, the FOUT signal is output from the P22 port terminal and when "0" is set, the port is set to the status according to the P22 port registers. While the FOUT signal is output (FOUTON is "1"), settings of the I/O control register IOC22 and data register P22D become invalid.
At initial reset, FOUTON is set to "0" (P22 port).

FOUT0–FOUT2: 00FF04H•D4–D6

FOUT signal frequency is set as shown in Table 8.7.2.

Table 8.7.2 FOUT frequency settings

FOUT2	FOUT1	FOUT0	FOUT frequency
1	1	1	f_{OSC3} / 8
1	1	0	f_{OSC3} / 4
1	0	1	f_{OSC3} / 2
1	0	0	f_{OSC3} / 1
0	1	1	f_{OSC1} / 8
0	1	0	f_{OSC1} / 4
0	0	1	f_{OSC1} / 2
0	0	0	f_{OSC1} / 1

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

At initial reset, this register is set to "0" (f_{OSC1} / 1).

8.8 Precautions

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.
- CPU operating clock OSC1
- OSC3 oscillation circuit OFF
  (When the OSC3 clock is not necessary for some peripheral circuits.)

(2) An oscillation stabilization time is required when the oscillation circuit starts oscillating. Therefore, be sure to wait long enough before switching the CPU clock or outputting the FOUT clock after the oscillation circuit is turned ON. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 19, "Electrical Characteristics".)

(3) When switching the clock from OSC3 to OSC1, be sure to turn OSC3 oscillation OFF with separate instructions. The same applies when switching the clock from OSC1 to OSC3 and turning OSC1 OFF. Using a single instruction to process simultaneously may cause a malfunction of the CPU.

(4) Since the FOUT output signal is generated asynchronously from the output control register (FOUTON), when the signals is turned ON or OFF by the output control register settings, a hazard of a 1/2 cycle or less is generated.

(5) If the SLP instruction is executed when the FOUT signal is being output, an unstable clock will be output when the system wakes up from SLEEP status. Therefore, stop the FOUT output before executing the SLP instruction.

9 OUTPUT PORTS (R PORTS)

9.1 Configuration of Output Ports

The S1C88655 is equipped with 26 bits of output ports (R00–R07, R10–R17, R20–R25, R30–R33). Depending on the bus mode setting, the configuration of the output ports may vary as shown in the table below.

Table 9.1.1 Configuration of output ports

Terminal	Bus mode	
	Single chip	Expansion
R00	Output port R00	Address A0
R01	Output port R01	Address A1
R02	Output port R02	Address A2
R03	Output port R03	Address A3
R04	Output port R04	Address A4
R05	Output port R05	Address A5
R06	Output port R06	Address A6
R07	Output port R07	Address A7
R10	Output port R10	Address A8
R11	Output port R11	Address A9
R12	Output port R12	Address A10
R13	Output port R13	Address A11
R14	Output port R14	Address A12
R15	Output port R15	Address A13
R16	Output port R16	Address A14
R17	Output port R17	Address A15
R20	Output port R20	Address A16
R21	Output port R21	Address A17
R22	Output port R22	Address A18
R23	Output port R23	Address A19
R24	Output port R24	$\overline{RD}$ signal
R25	Output port R25	$\overline{WR}$ signal
R30	Output port R30	Output port R30/$\overline{CE0}$ signal
R31	Output port R31	Output port R31/$\overline{CE1}$ signal
R32	Output port R32	Output port R32/$\overline{CE2}$ signal
R33	Output port R33	Output port R33/$\overline{CE3}$ signal

Only the configuration of the output ports in single chip mode will be discussed here. With respect to bus control, see Chapter 6, "System Controller and Bus Control".

Figure 9.1.1 shows the basic structure of the output ports.

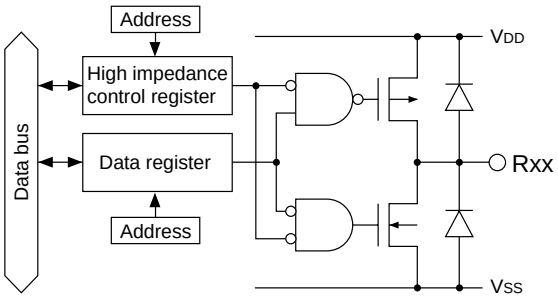


Fig. 9.1.1 Structure of output ports

In expansion mode, the data registers and high impedance control registers of the output ports used for bus function can be used as general-purpose registers with read / write capabilities. This will not in any way affect bus signal output.
The output specification of each output port is as complementary output with high impedance control in software possible.

9.2 High Impedance Control

The output port can be set into high impedance with software.
This makes it possible to share output signal lines with an other external device.

A high impedance control register HZRxx is provided to control each port status. When a high impedance control register HZRxx is set to "1", the corresponding output port terminal becomes high impedance state and when set to "0", it becomes complementary output.

9.3 DC Output

As Figure 9.1.1 shows, when "1" is written to the output port data register, the output terminal goes HIGH (V_{DD}) and when "0" is written it goes LOW (V_{SS}). When the port is in high impedance state, the data written to the data register is output from the terminal at the instant when output is switched to complementary.

9.4 Details of Control Registers

Table 9.4.1 shows the output port control bits.

Table 9.4.1(a) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF70	D7	HZR07	R07 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR06	R06 high impedance control					
	D5	HZR05	R05 high impedance control					
	D4	HZR04	R04 high impedance control					
	D3	HZR03	R03 high impedance control					
	D2	HZR02	R02 high impedance control					
	D1	HZR01	R01 high impedance control					
	D0	HZR00	R00 high impedance control					
00FF71	D7	HZR17	R17 high impedance control	High impedance	Complementary	0	R/W	
	D6	HZR16	R16 high impedance control					
	D5	HZR15	R15 high impedance control					
	D4	HZR14	R14 high impedance control					
	D3	HZR13	R13 high impedance control					
	D2	HZR12	R12 high impedance control					
	D1	HZR11	R11 high impedance control					
	D0	HZR10	R10 high impedance control					
00FF72	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	HZR25	R25 high impedance control	High impedance	Complementary	0	R/W	
	D4	HZR24	R24 high impedance control					
	D3	HZR23	R23 high impedance control					
	D2	HZR22	R22 high impedance control					
	D1	HZR21	R21 high impedance control					
	D0	HZR20	R20 high impedance control					
00FF73	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	–	–	–	–	0	R	
	D4	–	–	–	–	0	R	
	D3	HZR33	R33 high impedance control	High impedance	Complementary	0	R/W	
	D2	HZR32	R32 high impedance control					
	D1	HZR31	R31 high impedance control					
	D0	HZR30	R30 high impedance control					
00FF74	D7	R07D	R07 output port data	High	Low	1	R/W	
	D6	R06D	R06 output port data					
	D5	R05D	R05 output port data					
	D4	R04D	R04 output port data					
	D3	R03D	R03 output port data					
	D2	R02D	R02 output port data					
	D1	R01D	R01 output port data					
	D0	R00D	R00 output port data					
00FF75	D7	R17D	R17 output port data	High	Low	1	R/W	
	D6	R16D	R16 output port data					
	D5	R15D	R15 output port data					
	D4	R14D	R14 output port data					
	D3	R13D	R13 output port data					
	D2	R12D	R12 output port data					
	D1	R11D	R11 output port data					
	D0	R10D	R10 output port data					

Table 9.4.1(b) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF76	D7	–	R/W register	1	0	1	R/W	Reserved register
	D6	–	R/W register	1	0	1	R/W	
	D5	R25D	R25 output port data	High	Low	1	R/W	
	D4	R24D	R24 output port data					
	D3	R23D	R23 output port data					
	D2	R22D	R22 output port data					
	D1	R21D	R21 output port data					
	D0	R20D	R20 output port data					
00FF77	D7	–	R/W register	1	0	1	R/W	Reserved register
	D6	–	R/W register	1	0	1	R/W	
	D5	–	R/W register	1	0	1	R/W	
	D4	–	R/W register	1	0	1	R/W	
	D3	R33D	R33 output port data	High	Low	1	R/W	
	D2	R32D	R32 output port data					
	D1	R31D	R31 output port data					
	D0	R30D	R30 output port data					

HZR00–HZR07: 00FF70H
HZR10–HZR17: 00FF71H
HZR20–HZR25: 00FF72H•D0–D5
HZR30–HZR33: 00FF73H•D0–D3

Sets the output terminals to a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

HZRxx is the high impedance control register that corresponds to each output port terminal.
When "1" is set to the HZRxx register, the corresponding output port terminal becomes high impedance state and when "0" is set, it becomes complementary output.
At initial reset, this register is set to "0" (complementary).

The high impedance control registers set for bus signal output can be used as general-purpose registers with read / write capabilities which do not affect the output terminals.

R00D–R07D: 00FF74H
R10D–R17D: 00FF75H
R20D–R25D: 00FF76H•D0–D5
R30D–R33D: 00FF77H•D0–D3

Sets the data output from the output port terminal Rxx.

When "1" is written: HIGH level output
When "0" is written: LOW level output
Reading: Valid

RxxD is the data register for each output port.
When "1" is set, the corresponding output port terminal goes HIGH (V_{DD}) , and when "0" is set, it goes LOW (V_{SS}).
At initial reset, this register is set to "1" (HIGH level output).

The output data registers set for bus signal output can be used as general-purpose registers with read / write capabilities which do not affect the output terminals.

10 I/O PORTS (P PORTS)

10.1 Configuration of I/O Ports

The S1C88655 is equipped with 24 bits of I/O ports (P00–P07, P10–P17, P20–P27).
Figure 10.1.1 shows the structure of an I/O port.

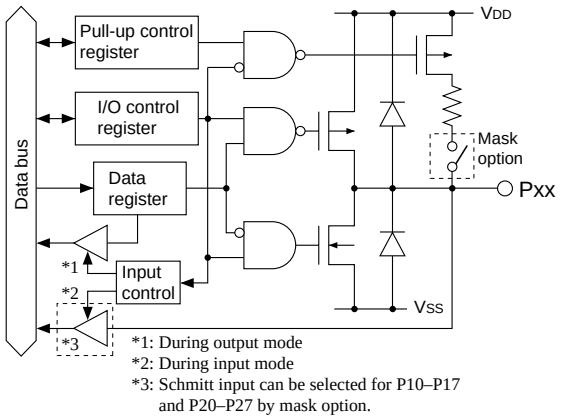


Fig. 10.1.1 Structure of I/O port

An I/O control register is provided for each I/O port to set the port into input or output mode.

The I/O port terminals are shared with other functions shown below and are software configurable.

Table 10.1.1 Terminal shared function

Port	Shared functions	
P00	Data bus (D0)	I/O
P01	Data bus (D1)	I/O
P02	Data bus (D2)	I/O
P03	Data bus (D3)	I/O
P04	Data bus (D4)	I/O
P05	Data bus (D5)	I/O
P06	Data bus (D6)	I/O
P07	Data bus (D7)	I/O
P10	Serial I/F 0 data input (SIN0)	I
P11	Serial I/F 0 data output (SOUT0)	O
P12	Serial I/F 0 clock input/output ($\overline{\text{SCLK0}}$)	I or O
P13	Serial I/F 0 ready signal output ($\overline{\text{SRDY0}}$)	O
P14	Serial I/F 1 data input (SIN1)	I
P15	Serial I/F 1 data output (SOUT1)	O
P16	Serial I/F 1 clock input/output ($\overline{\text{SCLK1}}$)	I or O
P17	Serial I/F 1 ready signal output ($\overline{\text{SRDY1}}$)	O
P20	PTM 0/1 output (TOUT0/TOUT1)	O
P21	PTM 2/3 output (TOUT2/TOUT3)	O
P22	Clock output (FOUT)	O
P23	PTM 2/3 inverted output ($\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$)	O
P24	1) Bus release request signal input ($\overline{\text{BREQ}}$)	I
	2) PTM 0 external clock input (EXCL0)	I
P25	1) Bus release ACK signal output ($\overline{\text{BACK}}$)	O
	2) PTM 1 external clock input (EXCL1)	I
P26	1) LCD clock output (CL)	O
	2) PTM 2 external clock input (EXCL2)	I
P27	1) LCD frame signal output (FR)	O
	2) PTM 3 external clock input (EXCL3)	I

P00–P07: D0–D7

The P00–P07 terminals are shared with the data bus D0–D7. When the bus mode is set to expansion mode, they function as the data bus terminals and cannot be used for general-purpose inputs/outputs. In single chip mode, they can be used as the P00–P07 I/O ports. See Chapter 6, "System Controller and Bus Control", for the bus mode and the data bus.
When these terminals are used as the data bus, the data registers and I/O control registers of the I/O ports can be used as general-purpose registers that do not affect the terminal status. The pull-up control registers are effective for the data bus.

P10–P13: SIN0, SOUT0, $\overline{\text{SCLK0}}$, $\overline{\text{SRDY0}}$
P14–P17: SIN1, SOUT1, $\overline{\text{SCLK1}}$, $\overline{\text{SRDY1}}$

The P10–P13 and P14–P17 terminals are shared with the inputs/outputs of the serial interface. Some terminals may be used as the I/O ports depending on the transfer mode to be set even if the serial interface is used. See Chapter 11, "Serial Interface", for details.
The data registers and I/O control registers of the ports used for serial input/output can be used as general-purpose registers that do not affect the terminal status. The pull-up control registers are effective for the input terminals.

P20: TOUT0/TOUT1
P21: $\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$
P23: $\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$

The P20, P21, and P23 terminals are shared with the programmable timer (PWM) outputs. See Section 13.6, "Setting TOUT Outputs", for details.
When using the terminal for a timer output, set the port to output mode and set the output level when the timer output is disabled to the data register.
The data register, I/O control register, and pull-up control register of the port while the timer output is enabled do not affect the terminal status.

P22: FOUT

The P22 terminal is shared with the clock output. See Section 8.6, "Clock Output (FOUT)", for the clock output function.
When using the terminal for the clock output, set the P22 port to output mode and set the output level when the clock output is disabled to the data register.
The data register, I/O control register, and pull-up control register of the port while the clock output is enabled do not affect the terminal status.

P24, P25: $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$

The P24 and P25 terminals are shared with the $\overline{\text{BREQ}}$ signal input and $\overline{\text{BACK}}$ signal output, respectively. See Section 6.5, "Setting Bus Authority Release Request Signal", for the $\overline{\text{BREQ}}$ and $\overline{\text{BACK}}$ signals.
The data registers and I/O control registers of the ports can be used as general-purpose registers that do not affect the terminal status.
The P24 pull-up control register is effective when used for the $\overline{\text{BREQ}}$ signal input.

P26, P27: CL, FR

The P26 and P27 terminals are shared with the CL and FR signal outputs, respectively. See Chapter 15, "LCD Driver", for the CL and FR signals.
When using the terminals for CL/FR outputs, set the ports to output mode and set the output level when the CL/FR outputs are disabled to the data registers.
The data register, I/O control register, and pull-up control register of the ports while the CL/FR outputs are enabled do not affect the terminal status.

P24–P27: EXCL0–EXCL3

The P24–P27 terminals can also be used for external clock inputs for the programmable timers. See Chapter 13, "Programmable Timer", for the EXCL input.
When using the terminal for EXCL input, set the port to input mode. In this case, the terminal (P24–P27) functions as an I/O port. Therefore, the pull-up control register is effective.

This chapter explains the functions when the terminals are used as general-purpose I/O ports.

10.2 Mask Option

I/O port pull-up resistors

P00	☐ With resistor	☐ Gate direct
P01	☐ With resistor	☐ Gate direct
P02	☐ With resistor	☐ Gate direct
P03	☐ With resistor	☐ Gate direct
P04	☐ With resistor	☐ Gate direct
P05	☐ With resistor	☐ Gate direct
P06	☐ With resistor	☐ Gate direct
P07	☐ With resistor	☐ Gate direct
P10	☐ With resistor	☐ Gate direct
P11	☐ With resistor	☐ Gate direct
P12	☐ With resistor	☐ Gate direct
P13	☐ With resistor	☐ Gate direct
P14	☐ With resistor	☐ Gate direct
P15	☐ With resistor	☐ Gate direct
P16	☐ With resistor	☐ Gate direct
P17	☐ With resistor	☐ Gate direct
P20	☐ With resistor	☐ Gate direct
P21	☐ With resistor	☐ Gate direct
P22	☐ With resistor	☐ Gate direct
P23	☐ With resistor	☐ Gate direct
P24	☐ With resistor	☐ Gate direct
P25	☐ With resistor	☐ Gate direct
P26	☐ With resistor	☐ Gate direct
P27	☐ With resistor	☐ Gate direct

I/O port input interface level

P10	☐ CMOS level	☐ CMOS Schmitt
P11	☐ CMOS level	☐ CMOS Schmitt
P12	☐ CMOS level	☐ CMOS Schmitt
P13	☐ CMOS level	☐ CMOS Schmitt
P14	☐ CMOS level	☐ CMOS Schmitt
P15	☐ CMOS level	☐ CMOS Schmitt
P16	☐ CMOS level	☐ CMOS Schmitt
P17	☐ CMOS level	☐ CMOS Schmitt
P20	☐ CMOS level	☐ CMOS Schmitt
P21	☐ CMOS level	☐ CMOS Schmitt
P22	☐ CMOS level	☐ CMOS Schmitt
P23	☐ CMOS level	☐ CMOS Schmitt
P24	☐ CMOS level	☐ CMOS Schmitt
P25	☐ CMOS level	☐ CMOS Schmitt
P26	☐ CMOS level	☐ CMOS Schmitt
P27	☐ CMOS level	☐ CMOS Schmitt

I/O ports P00–P07, P10–P17, and P20–P27 are equipped with a pull-up resistor which goes ON in the input mode. Whether this resistor is used or not can be selected for each port (one bit unit). Furthermore, the interface level for each port in P10–P17 and P20–P27 can be selected from CMOS level and CMOS Schmitt level.

10.3 Input/Output Mode

The I/O port Pxx is set either to input or output modes by writing data to the I/O control register IOCxx which corresponds to each bit.

To set an I/O port to input mode, write "0" to the I/O control register.
The I/O port , which is set to input mode, will go to a high impedance state and functions as an input port.
Readout in input mode consists simply of a direct readout of the input terminal state: the data being "1" when the input terminal is at HIGH (V_{DD}) level and "0" when it is at LOW (V_{SS}) level.
When the built-in pull-up resistor is enabled with the software, the port terminal will be pulled-up to high during input mode.
Even in input mode, data can be written to the data registers without affecting the terminal state.

To set an I/O port to output mode, write "1" to the I/O control register. The I/O port, which is set to output mode, functions as an output port.
When port output data is "1", a HIGH (V_{DD}) level is output and when it is "0", a LOW (V_{SS}) level is output. Readout in output mode consists of the contents of the data register.
At initial reset, I/O control registers are set to "0" (I/O ports are set to input mode).

10.4 Pull-up Control

When "With resistor" is selected by mask option, the software can enable and disable the pull-up resistor for each port (1-bit units).
The pull-up resistor becomes effective by writing "1" to the pull-up control register PULPxx that corresponds to each port, and the Pxx terminal is pulled up during the input mode. When "0" has been written, no pull-up is done. When "Gate direct" is selected by mask option, the corresponding pull-up control register is disconnected from the input line, so it can be used as a general-purpose register. When the port is set in the output mode, the setting of the pull-up control register becomes invalid (no pull-up is done during output).
At initial reset, the pull-up control registers are set to "1" (pulled up).

When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

For unused ports, select "With resistor" and enable pull-up using the pull-up control registers.

10.5 Interrupt Function

The P20–P27 ports provide the input interrupt function. The condition for issuing an interrupt can be set for each terminal in software. When the interrupt generation condition set for a terminal is met, the interrupt factor flag FP20–FP27 corresponding to the terminal is set at "1" and an interrupt is generated.
Interrupt can be prohibited by setting the interrupt enable registers EP20–EP27 for the corresponding interrupt factor flags.
Furthermore, the priority level for input interrupt can be set at the desired level (0–3) using the interrupt priority registers PP20–PP21.
For details on the interrupt control registers for the above and on operations subsequent to interrupt generation, see Chapter 7, "Interrupt and Standby Status".

The exception processing vectors for each interrupt factor are set as follows:

P27 input interrupt: 000006H
P26 input interrupt: 000008H
P25 input interrupt: 00000AH
P24 input interrupt: 00000CH
P23 input interrupt: 00000EH
P22 input interrupt: 000010H
P21 input interrupt: 000012H
P20 input interrupt: 000014H

Figure 10.5.1 shows the configuration of the input interrupt circuit.

Note: When a port is placed in output mode or configured for the shared port function other than general-purpose DC input, disable interrupts from the port.

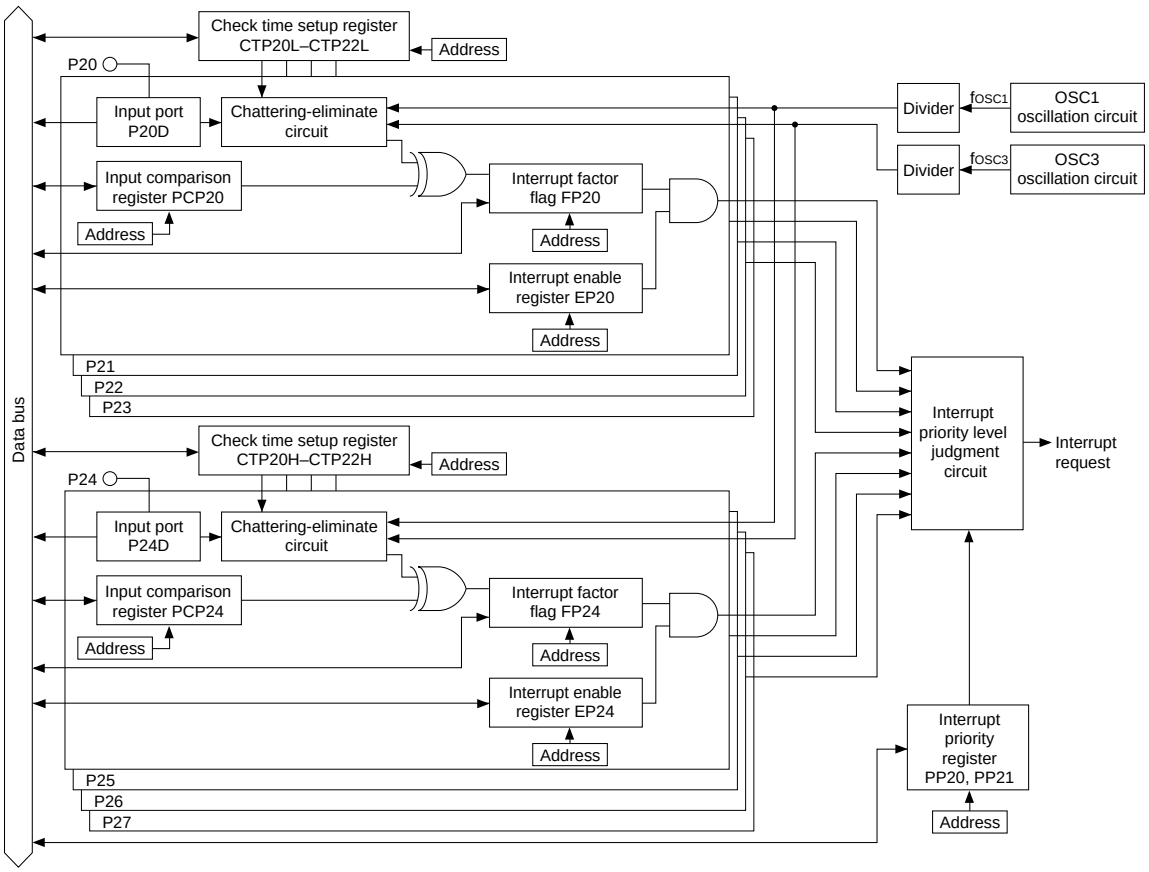


Fig. 10.5.1 Configuration of input interrupt circuit

The input comparison register PCP selects whether the interrupt for each input port will be generated on the rising edge or the falling edge of input. When the P2x input signal changes to the status set by the input comparison register PCP2x, the interrupt factor flag FP2x is set to "1" and an interrupt occurs.
The input port has a chattering-eliminate circuit that checks input level to avoid unnecessary interrupt generation due to chattering. There are two separate chattering-eliminate circuits for P20–P23 and P24–P27 and they can be set up individually. The CTP20x–CTP22x registers allow selection of signal level check time as shown in Table 10.5.1.

Table 10.5.1 Setting the input level check time

CTP22x	CTP21x	CTP20x	Check time	(*)
1	1	1	4/fOSC3	(2 µs)
1	1	0	2/fOSC3	(1 µs)
1	0	1	1/fOSC3	(0.5 µs)
1	0	0	4096/fOSC1	(128 ms)
0	1	1	2048/fOSC1	(64 ms)
0	1	0	512/fOSC1	(16 ms)
0	0	1	128/fOSC1	(4 ms)
0	0	0	None	–

*: When OSC1 = 32 kHz, OSC3 = 2 MHz

Notes:
- *Input interrupts cannot be accepted in SLEEP mode if the CPU enters SLEEP mode when the chattering-eliminate circuit is active. The chattering-eliminate circuit should be turned OFF (CTP2x = "000") before executing the SLP instruction.*
- *Be sure to disable interrupts before changing the contents of the CTP2x register. Unnecessary interrupts may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EP2x.*
- *The chattering-eliminate check time means the maximum pulse width that can be eliminated. The valid interrupt input needs a pulse width of the set check time (minimum) to twice that of the check time (maximum).*
- *The internal signal may oscillate if the rise / fall time of the input signal is too long because the input signal level transition to the threshold level duration of time is too long. This causes the input interrupt to malfunction, therefore setup the input signal so that the rise/fall time is 25 nsec or less.*

10.6 Details of Control Registers

Table 10.6.1 shows the I/O port control bits.

Table 10.6.1(a) I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF50	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register					
	D5	IOC05	P05 I/O control register					
	D4	IOC04	P04 I/O control register					
	D3	IOC03	P03 I/O control register					
	D2	IOC02	P02 I/O control register					
	D1	IOC01	P01 I/O control register					
	D0	IOC00	P00 I/O control register					
00FF51	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register					
	D5	IOC15	P15 I/O control register					
	D4	IOC14	P14 I/O control register					
	D3	IOC13	P13 I/O control register					
	D2	IOC12	P12 I/O control register					
	D1	IOC11	P11 I/O control register					
	D0	IOC10	P10 I/O control register					
00FF52	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data					
	D5	P05D	P05 I/O port data					
	D4	P04D	P04 I/O port data					
	D3	P03D	P03 I/O port data					
	D2	P02D	P02 I/O port data					
	D1	P01D	P01 I/O port data					
	D0	P00D	P00 I/O port data					
00FF53	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data					
	D5	P15D	P15 I/O port data					
	D4	P14D	P14 I/O port data					
	D3	P13D	P13 I/O port data					
	D2	P12D	P12 I/O port data					
	D1	P11D	P11 I/O port data					
	D0	P10D	P10 I/O port data					
00FF54	D7	PULP07	P07 pull-up control register	On	Off	1	R/W	
	D6	PULP06	P06 pull-up control register					
	D5	PULP05	P05 pull-up control register					
	D4	PULP04	P04 pull-up control register					
	D3	PULP03	P03 pull-up control register					
	D2	PULP02	P02 pull-up control register					
	D1	PULP01	P01 pull-up control register					
	D0	PULP00	P00 pull-up control register					
00FF55	D7	PULP17	P17 pull-up control register	On	Off	1	R/W	
	D6	PULP16	P16 pull-up control register					
	D5	PULP15	P15 pull-up control register					
	D4	PULP14	P14 pull-up control register					
	D3	PULP13	P13 pull-up control register					
	D2	PULP12	P12 pull-up control register					
	D1	PULP11	P11 pull-up control register					
	D0	PULP10	P10 pull-up control register					

Table 10.6.1(b) I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF60	D7	IOC27	P27 I/O control register	Output	Input	0	R/W	
	D6	IOC26	P26 I/O control register					
	D5	IOC25	P25 I/O control register					
	D4	IOC24	P24 I/O control register					
	D3	IOC23	P23 I/O control register					
	D2	IOC22	P22 I/O control register					
	D1	IOC21	P21 I/O control register					
	D0	IOC20	P20 I/O control register					
00FF62	D7	P27D	P27 I/O port data	High	Low	1	R/W	
	D6	P26D	P26 I/O port data					
	D5	P25D	P25 I/O port data					
	D4	P24D	P24 I/O port data					
	D3	P23D	P23 I/O port data					
	D2	P22D	P22 I/O port data					
	D1	P21D	P21 I/O port data					
	D0	P20D	P20 I/O port data					
00FF64	D7	PULP27	P27 pull-up control register	On	Off	1	R/W	
	D6	PULP26	P26 pull-up control register					
	D5	PULP25	P25 pull-up control register					
	D4	PULP24	P24 pull-up control register					
	D3	PULP23	P23 pull-up control register					
	D2	PULP22	P22 pull-up control register					
	D1	PULP21	P21 pull-up control register					
	D0	PULP20	P20 pull-up control register					
00FF66	D7	PCP27	P27 input comparison register	Interrupt occurred at falling edge	Interrupt occurred at rising edge	1	R/W	
	D6	PCP26	P26 input comparison register					
	D5	PCP25	P25 input comparison register					
	D4	PCP24	P24 input comparison register					
	D3	PCP23	P23 input comparison register					
	D2	PCP22	P22 input comparison register					
	D1	PCP21	P21 input comparison register					
	D0	PCP20	P20 input comparison register					
00FF68	D7	–	–	–	–	0	R	"0" when being read
	D6	CTP22H	P24–P27 port chattering-eliminate setup (Input level check time)			0	R/W	
	D5	CTP21H				0	R/W	
	D4	CTP20H				0	R/W	
	D3	–	–	–	–	0	R	"0" when being read
	D2	CTP22L	P20–P23 port chattering-eliminate setup (Input level check time)			0	R/W	
	D1	CTP21L				0	R/W	
	D0	CTP20L				0	R/W	

P24–P27 port chattering-eliminate setup (Input level check time)

CTP22H	CTP21H	CTP20H	Check time [sec]
1	1	1	4/fOSC3
1	1	0	2/fOSC3
1	0	1	1/fOSC3
1	0	0	4096/fOSC1
0	1	1	2048/fOSC1
0	1	0	512/fOSC1
0	0	1	128/fOSC1
0	0	0	None

P20–P23 port chattering-eliminate setup (Input level check time)

CTP22L	CTP21L	CTP20L	Check time [sec]
1	1	1	4/fOSC3
1	1	0	2/fOSC3
1	0	1	1/fOSC3
1	0	0	4096/fOSC1
0	1	1	2048/fOSC1
0	1	0	512/fOSC1
0	0	1	128/fOSC1
0	0	0	None

P00D–P07D: 00FF52H
P10D–P17D: 00FF53H
P20D–P27D: 00FF62H

These registers are used to read Pxx I/O port terminal data and to set output data.

When writing data:

When "1" is written: HIGH level
When "0" is written: LOW level

When the I/O port is set to output mode, the data written is output as is to the I/O port terminal. In terms of port data, when "1" is written, the port terminal goes to HIGH (V_{DD}) level and when "0" is written to a LOW (V_{SS}) level.
Even when the port is in input mode, data can still be written in.

When reading out data:

When "1" is read: HIGH level ("1")
When "0" is read: LOW level ("0")

When an I/O port is in input mode, the voltage level being input to the port terminal is read out. When terminal voltage is HIGH (V_{DD}), it is read as a "1", and when it is LOW (V_{SS}), it is read as a "0". Furthermore, in output mode, the contents of the data register are read out.
At initial reset, this register is set to "1" (HIGH level).

Note: The data registers of the ports that are configured to the data bus and serial interface outputs can be used as general-purpose registers that do not affect the terminal input/output status.

IOC00–IOC07: 00FF50H
IOC10–IOC17: 00FF51H
IOC20–IOC27: 00FF60H

Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOCxx is the I/O control register which corresponds to each I/O port (in bit units). Writing "1" to the IOCxx register will set the corresponding I/O port Pxx to output mode, and writing "0" will set it to input mode.
When the special output is used, "1" must always be set for the I/O control registers of I/O ports which will become output terminals.
At initial reset, this register is set to "0" (input mode).

Note: The I/O control registers of the ports that are configured to the data bus and serial interface inputs/outputs can be used as general-purpose registers that do not affect the terminal input/output status.

PULP00–PULP07: 00FF54H
PULP10–PULP17: 00FF55H
PULP20–PULP27: 00FF64H

Enables pull-up during input mode.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

PULPxx is the pull-up control register corresponding to each I/O port (in bit units). When "Gate direct" is selected by mask option, the corresponding pull-up control register is disconnected from the input line, so it can be used as a general-purpose register.
By writing "1" to the PULPxx register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.
At initial reset, these registers are all set to "1", so the pull-up function is enabled.

Note: The pull-up control registers of the ports that are configured to the serial interface outputs can be used as general-purpose registers that do not affect the pull-up control. The pull-up control registers of the port that are configured to the data bus and serial interface inputs function the same as the I/O port.

PCP20–PCP27: 00FF66H

Sets the interrupt generation condition (interrupt generation timing) for input port terminals P20–P27.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

PCP2x is the input comparison register which corresponds to the input port P2x. When PCP2x is set to "1", interrupts from the P2x port are generated at the falling edge of the input signal. When PCP2x is set to "0", interrupts are generated at the rising edge.
At initial reset, this register is set to "1" (falling edge).

CTP20L–CTP22L: 00FF68H•D0–D2

Sets the input level check time of the chattering-eliminate circuit for the P20–P23 port interrupts as shown in Table 10.6.2.

Table 10.6.2 Setting the input level check time

CTP22L	CTP21L	CTP20L	Input level check time [sec]
1	1	1	4/fOSC3
1	1	0	2/fOSC3
1	0	1	1/fOSC3
1	0	0	4096/fOSC1
0	1	1	2048/fOSC1
0	1	0	512/fOSC1
0	0	1	128/fOSC1
0	0	0	None

Be sure to disable interrupts before changing the contents of this register. Unnecessary interrupts may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EP2x.
At initial reset, this register is set to "0" (None).

CTP20H–CTP22H: 00FF58H•D4–D6

Sets the input level check time of the chattering-eliminate circuit for the P24–P27 input port interrupts as shown in Table 10.6.3.

Table 10.6.3 Setting the input level check time

CTP22H	CTP21H	CTP20H	Input level check time [sec]
1	1	1	4/fOSC3
1	1	0	2/fOSC3
1	0	1	1/fOSC3
1	0	0	4096/fOSC1
0	1	1	2048/fOSC1
0	1	0	512/fOSC1
0	0	1	128/fOSC1
0	0	0	None

Be sure to disable interrupts before changing the contents of this register. Unnecessary interrupt may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EP2x.
At initial reset, this register is set to "0" (None).

10.7 Precautions

(1) When changing the port terminal in which the pull-up resistor is enabled from LOW level to HIGH, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = RIN x (CIN + load capacitance on the board) x 1.6 [sec]

RIN: Pull up resistance Max. value
CIN: Terminal capacitance Max. value

(2) Be sure to disable interrupts before changing the contents of the CTP2x register. Unnecessary interrupts may occur if the register is changed when the corresponding input port interrupts have been enabled by the interrupt enable register EP2x.

11 SERIAL INTERFACE

11.1 Configuration of Serial Interface

The S1C88655 incorporates a full duplex serial interface (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software. When the clock synchronous system is selected, 8-bit data transfer is possible. When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software. Figure 11.1.1 shows the configuration of the serial interface.

Note: Ch. 0 and Ch. 1 have the same circuit configuration and functions. The signal and control bit names are suffixed by a 0 or 1 to indicate the channel number, enabling discrimination between channels 0 and 1. In this manual, however, channel numbers 0 and 1 are replaced with "x" unless discrimination is necessary, because explanations are common to both channels.

11.2 Switching Terminal Functions

The serial interface Ch. 0 input/output terminals, SIN0, SOUT0, $\overline{\text{SCLK0}}$, and $\overline{\text{SRDY0}}$ are shared with the I/O ports P10–P13. Also Ch. 1 input/output terminals, SIN1, SOUT1, $\overline{\text{SCLK1}}$, and $\overline{\text{SRDY1}}$ are shared with the I/O ports P14–P17. In order to utilize these terminals for the serial interface input/output terminals, "1" must be written to the ESIFx register. At initial reset, these terminals are set as I/O port terminals.

The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 11.2.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P10	SIN0
P11	SOUT0
P12	$\overline{\text{SCLK0}}$
P13	$\overline{\text{SRDY0}}$
P14	SIN1
P15	SOUT1
P16	$\overline{\text{SCLK1}}$
P17	$\overline{\text{SRDY1}}$

* The terminals used may vary depending on the transfer mode.

The serial interface terminals are configured according to the transfer mode set using the registers SMDx0 and SMDx1. SINx and SOUTx are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. $\overline{\text{SCLKx}}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. $\overline{\text{SRDYx}}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal. When asynchronous system is selected, since $\overline{\text{SCLKx}}$ and $\overline{\text{SRDYx}}$ are superfluous, the I/O port terminals P12 (P16) and P13 (P17) can be used as I/O ports. In the same way, when clock synchronous master mode is selected, since $\overline{\text{SRDYx}}$ is superfluous, the I/O port terminal P13 (P17) can be used as an I/O port.

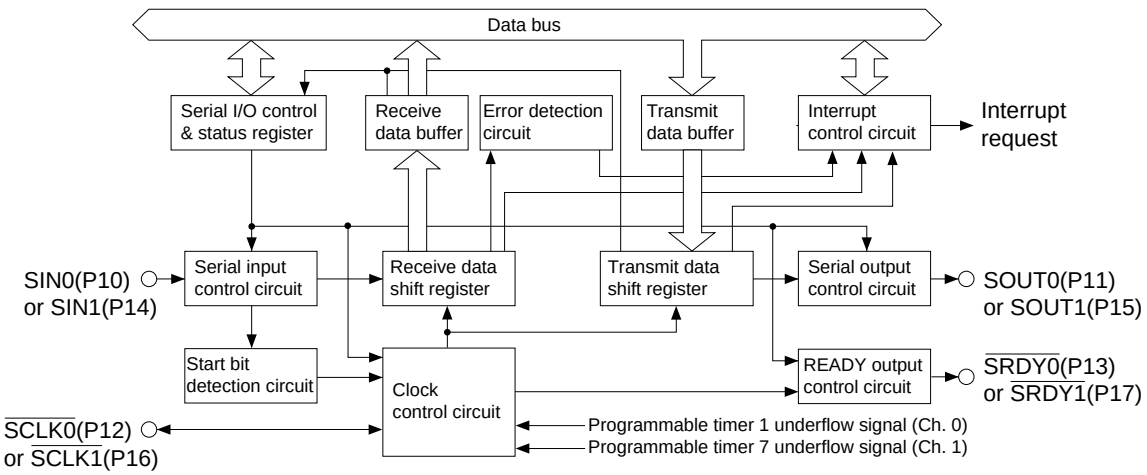


Fig. 11.1.1 Configuration of serial interface

11.3 Transfer Modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMDx0 and SMDx1 as shown in the table below.

Table 11.3.1 Transfer modes

SMDx1	SMDx0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 11.3.2 Terminal settings corresponding to each transfer mode

Mode	SINx	SOUTx	$\overline{\text{SCLKx}}$	$\overline{\text{SRDYx}}$
Asynchronous 8-bit	Input	Output	P12/P16	P13/P17
Asynchronous 7-bit	Input	Output	P12/P16	P13/P17
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P13/P17

At initial reset, transfer mode is set to clock synchronous master mode.

■ Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and clock synchronous 8-bit serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the $\overline{\text{SCLKx}}$ terminal which enables control of the external (slave side) serial I/O device. Since the $\overline{\text{SRDYx}}$ terminal is not utilized in this mode, it can be used as an I/O port.
Figure 11.3.1(a) shows the connection example of input/output terminals in the clock synchronous master mode.

■ Clock synchronous slave mode

In this mode, a synchronous clock from the external (master side) serial input/output device is utilized and clock synchronous 8-bit serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the $\overline{\text{SCLKx}}$ terminal and is utilized by this interface as the synchronous clock.
Furthermore, the $\overline{\text{SRDYx}}$ signal indicating the transmit-receive ready status is output from the $\overline{\text{SRDYx}}$ terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCSx0 and SCSx1 used to select the clock source are invalid.
Figure 11.3.1(b) shows the connection example of input/output terminals in the clock synchronous slave mode.

■ Asynchronous 7-bit mode

In this mode, asynchronous 7-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the $\overline{\text{SCLKx}}$ terminal is not used. Furthermore, since the $\overline{\text{SRDYx}}$ terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 11.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

■ Asynchronous 8-bit mode

In this mode, asynchronous 8-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the $\overline{\text{SCLKx}}$ terminal is not used. Furthermore, since the $\overline{\text{SRDYx}}$ terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 11.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

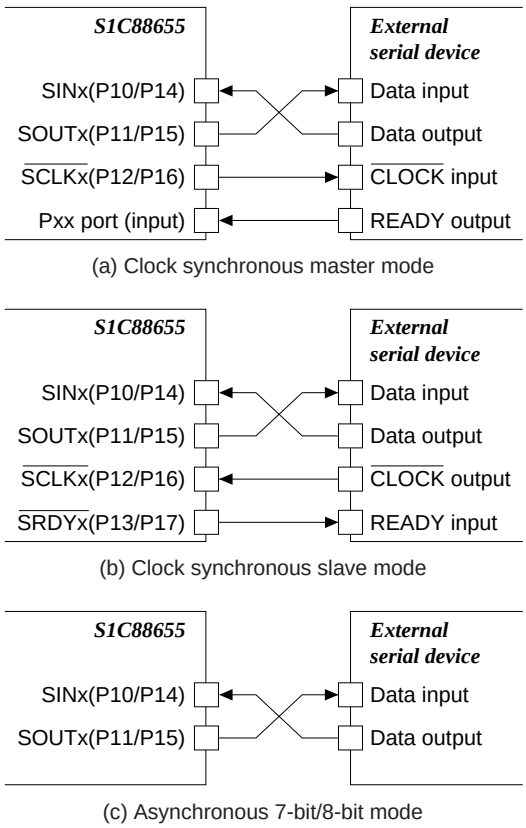


Fig. 11.3.1 Connection examples of serial interface I/O terminals

11.4 Clock Source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCSx0 and SCSx1 as shown in table below.

Table 11.4.1 Clock source

SCSx1	SCSx0	Clock source
1	1	Programmable timer 1 (Ch. 0)
		Programmable timer 7 (Ch. 1)
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

This register setting is invalid in clock synchronous slave mode and the external clock input from the $\overline{SCLKx}$ terminal is used.

When the "programmable timer " is selected, the underflow signal of the programmable timer 1 for Ch. 0 or timer 7 for Ch. 1 is divided by 2 and the divided signal is used as the clock source.
With respect to the transfer rate setting, see Chapter 13, "Programmable Timer".
At initial reset, the synchronous clock is set to "f_{OSC3} / 16".

Whichever clock is selected, the signal is further divided by 16 and then used as the synchronous clock.
Furthermore, external clock input is used as is for $\overline{SCLKx}$ in clock synchronous slave mode.

When the divided signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 19, "Electrical Characteristics".)
At initial reset, the OSC3 oscillation circuit is set to ON status.

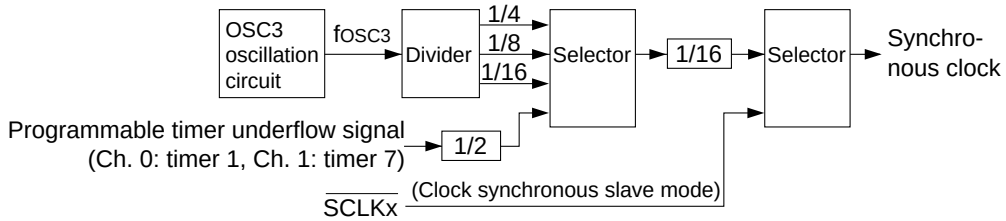


Fig. 11.4.1 Division of the synchronous clock

11.5 Transmit/Receive Control

Below is a description of the registers which handle transmit / receive control. With respect to transmit / receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

■ Shift register and transmit/received data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.
In the transmit section, a transmit data buffer is installed separate from the shift register. When data transmission is started, the data in the transmit data buffer is converted to serial through the shift register and output from the SOUTx terminal. Data can be written to the transmit data buffer asynchronously with the serial output, this allows highly efficient continuous data transfer.
In the reception section, a received data buffer is installed separate from the shift register.
Data being received are input to the SINx terminal and is converted to parallel through the shift register and written to the received data buffer.
Since the received data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

■ Transmit enable register and transmit control bit

For transmitting control, use the transmit enable register TXENx and transmit control bit TXTRGx.
The transmit enable register TXENx is used to set the transmitting enable / disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLKx}}$ terminal is also enabled.
The transmit control bit TXTRGx is used as the trigger to start transmitting data.
Prepare data transmission by writing data to the transmit data buffer and write "1" to TXTRGx. Then the data in the transmit data buffer is loaded to the transmit data shift register and data transmission begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.
In addition, TXTRGx can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.
When not transmitting, set TXENx to "0" to disable transmitting status.

■ Receive enable register and receive control bit

For receiving control, use the receive enable register RXENx and receive control bit RXTRGx.
Receive enable register RXENx is used to set receiving enable / disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLKx}}$ terminal is also enabled.
With the above setting, receiving begins and serial data input from the SINx terminal goes to the shift register.
The operation of the receive control bit RXTRGx is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit RXTRGx is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRGx to start receiving. (When "1" is written to RXTRGx in slave mode, $\overline{\text{SRDYx}}$ switches to "0".)
In an asynchronous system, RXTRGx is used to prepare for next data receiving. After reading the received data from the received data buffer, write "1" into RXTRGx to signify that the received data buffer is empty. If "1" is not written into RXTRGx, the overrun error flag OERx will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRGx.)
In addition, RXTRGx can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRGx is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.
When you do not receive, set RXENx to "0" to disable receiving status.

11.6 Operation of Clock Synchronous Transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCSx0 and SCSx1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the SCLKx terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the SCLKx terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line (SCLKx) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

The transfer data length is fixed at 8 bits. Data can be switched using a register whether it is transmitted/received from LSB (bit 0) or MSB (bit 7).

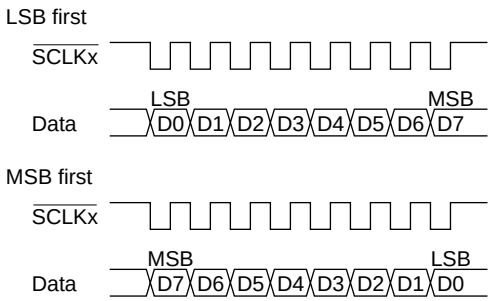


Fig. 11.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "11.8 Interrupt Function".

■ Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXENx and the receive enable register RXENx. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input/output ports SINx, SOUTx, SCLKx and SRDYx are set as I/O port terminals P10–P13 (P14–P17) at initial reset, "1" must be written to the serial interface enable register ESIFx in order to set these terminals for serial interface use.

(3) Setting of transfer mode
Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMDx0 and SMDx1.

Master mode: SMDx0 = "0", SMDx1 = "0"
Slave mode: SMDx0 = "1", SMDx1 = "0"

(4) Clock source selection
In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCSx0 and SCSx1. (See Table 11.4.1.)
This selection is not necessary in the slave mode.

Since all the registers mentioned in (2)–(4) are assigned to the same address, it's possible to set them all with one instruction. The parity enable register EPRx is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control
When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See Chapter 13, "Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See Chapter 8, "Oscillation Circuits".)

(6) Serial data input/output permutation
The S1C88655 provides the data input/output permutation select register SDPx to select whether the serial data bits are transferred from the LSB or MSB. The SDPx register should be set before writing data to TXDx0–TXDx7.

■ Data transmit procedure

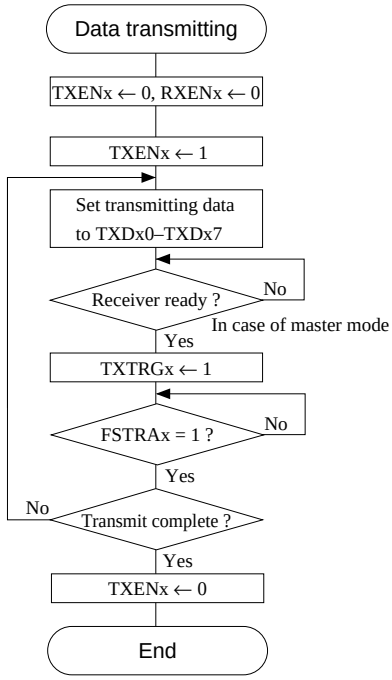


Fig. 11.6.2 Transmit procedure in clock synchronous mode

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXENx and the receive enable register RXENx to reset the serial interface.

(2) Write "1" in the transmit enable register TXENx to set into the transmitting enable status.

(3) Write the transmitting data into TXDx0–TXDx7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRGx and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{SCLKx}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLKx}$ terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUTx terminal. When the final bit (MSB when "LSB first" is selected, or LSB when "MSB first" is selected) is output, the SOUTx terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag FSTRAx is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXENx, when the transmitting is completed.

■ Data receive procedure

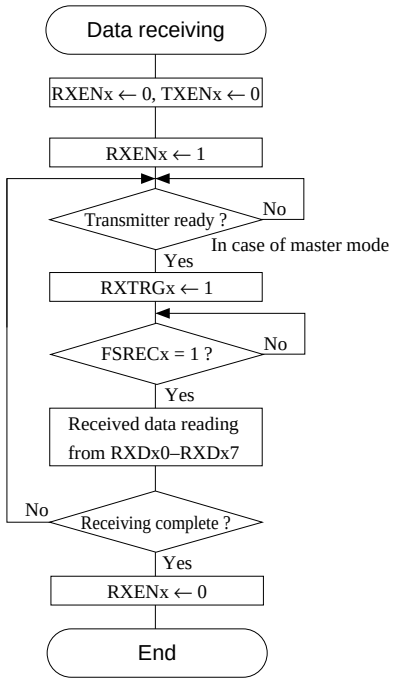


Fig. 11.6.3 Receiving procedure in clock synchronous mode

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXENx and transmit enable register TXENx to reset the serial interface.

(2) Write "1" in the receive enable register RXENx to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRGx and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{SCLKx}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLKx}$ terminal. The received data input from the SINx terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the received data buffer and the receiving complete interrupt factor flag FSRECx is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from RXDx0–RXDx7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXENx, when the receiving is completed.

■ Transmit/receive ready ($\overline{SRDYx}$) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an $\overline{SRDYx}$ signal is output to indicate whether or not this serial interface can transmit/receive to the master side (external serial input/output device). This signal is output from the $\overline{SRDYx}$ terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (LOW level) and becomes "1" (HIGH level) when there is a BUSY status, such as during transmit/receive operation.
The $\overline{SRDYx}$ signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRGx or the receive control bit RXTRGx and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge).
When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I/O port. At this time, since the $\overline{SRDYx}$ terminal is not set and instead P13 (P17) functions as the I/O port, you can apply this port for said control.

■ Timing chart

The timing chart for the clock synchronous system transmission is shown in Figure 11.6.4.

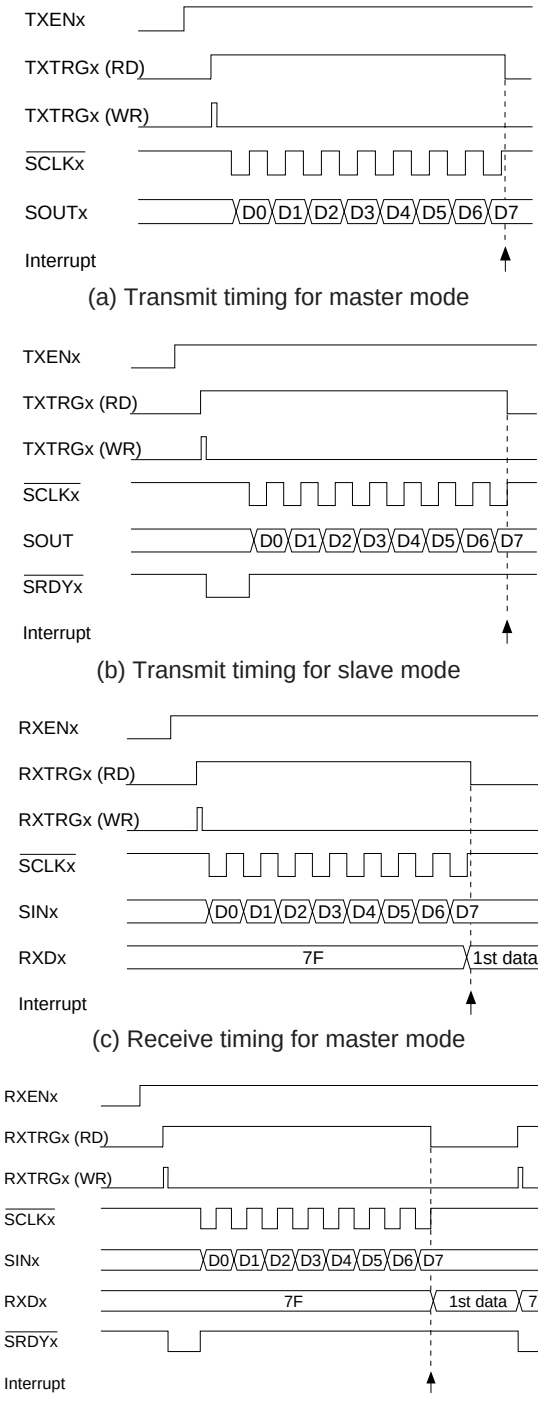
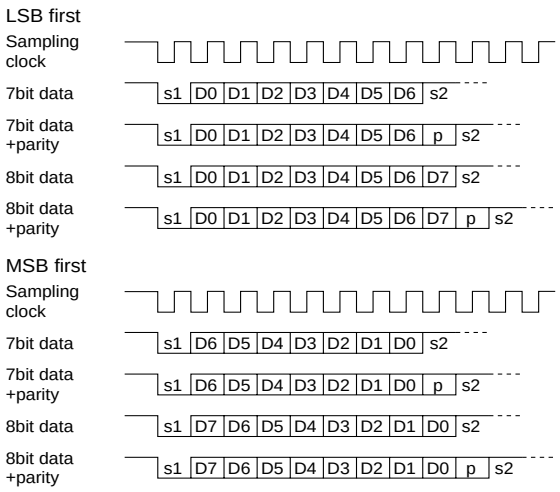


Fig. 11.6.4 Timing chart (clock synchronous system transmission, LSB first)

11.7 Operation of Asynchronous Transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start / stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.
For transfer data in the asynchronous 7-bit mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the asynchronous 8-bit mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit length is fixed at 1 bit. For the stop bit length, either 1 bit or 2 bits can be selected using the stop bit select register STPBx. Whether data is transmitted / received from LSB (bit 0) or MSB (bit 7) it can be switched using the data input / output permutation select register SDPx.



s1 : Start bit (Low level, 1 bit)
s2 : Stop bit (High level, 1 bit or 2 bits)
p : Parity bit

Fig. 11.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "11.8 Interrupt Function" for the serial interface interrupts.

■ Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXENx and the receive enable register RXENx. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input / output terminals SINx and SOUTx are set as I / O port terminals P10 (P14) and P11 (P15) at initial reset, "1" must be written to the serial interface enable register ESIFx in order to set these terminals for serial interface use.
$\overline{\text{SCLKx}}$ and $\overline{\text{SRDYx}}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I / O port terminals P12 (P16) and P13 (P17).

(3) Setting of transfer mode

Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMDx0 and SMDx1.

7-bit mode: SMDx0 = "0", SMDx1 = "1"
8-bit mode: SMDx0 = "1", SMDx1 = "1"

(4) Parity bit selection

When checking and adding parity bits, write "1" into the parity enable register EPRx to set to "with parity check". As a result of this setting, in the asynchronous 7-bit mode, it has a 7 bits data + parity bit configuration and in the asynchronous 8-bit mode it has an 8 bits data + parity bit configuration. In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMDx.
When "0" is written to the EPRx register to select "without parity check" in the asynchronous 7-bit mode, data configuration is set to 7 bits data (no parity) and in the asynchronous 8-bit mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection

Select the clock source by writing data to the two bits of the clock source selection registers SCSx0 and SCSx1. (See Table 11.4.1.)

Since all the registers mentioned in (2)–(5) are assigned to the same address, it's possible to set them all with one instruction.

(6) Clock source control

When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See Chapter 13, "Programmable Timer".)

When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See Chapter 8, "Oscillation Circuits".)

(7) Stop bit length selection

The stop bit length can be configured to 1 bit or 2 bits using the stop bit select register STPBx.

Table 11.7.1 Stop bit and parity bit settings

STPBx	EPRx	PMDx	Settings	
			Stop bit	Parity bit
1	1	1	2 bits	Odd
		0	2 bits	Even
	0	–	2 bits	Non parity
0	1	1	1 bit	Odd
		0	1 bit	Even
	0	–	1 bit	Non parity

(8) Serial data input/output permutation

The S1C88655 provides the data input/output permutation select register SDPx to select whether the serial data bits are transferred from the LSB or MSB. The SDPx register should be set before writing data to TXDx0–TXDx7.

■ Data transmit procedure

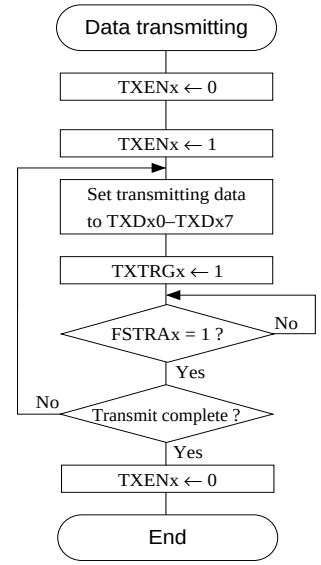


Fig. 11.7.2 Transmit procedure in asynchronous mode

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXENx to reset the serial interface.

(2) Write "1" in the transmit enable register TXENx to set into the transmitting enable status.

(3) Write the transmitting data into TXDx0–TXDx7. Also, when 7-bit data is selected, the TXDx7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRGx and start transmitting. This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUTx terminal in synchronize to its falling edge. The transmitting data set to the shift register is shifted one bit at a time at each falling edge of the clock thereafter and is output from the SOUTx terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output. The transmitting complete interrupt factor flag FSTRAx is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point. Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXENx, when the transmitting is completed.

■ Data receive procedure

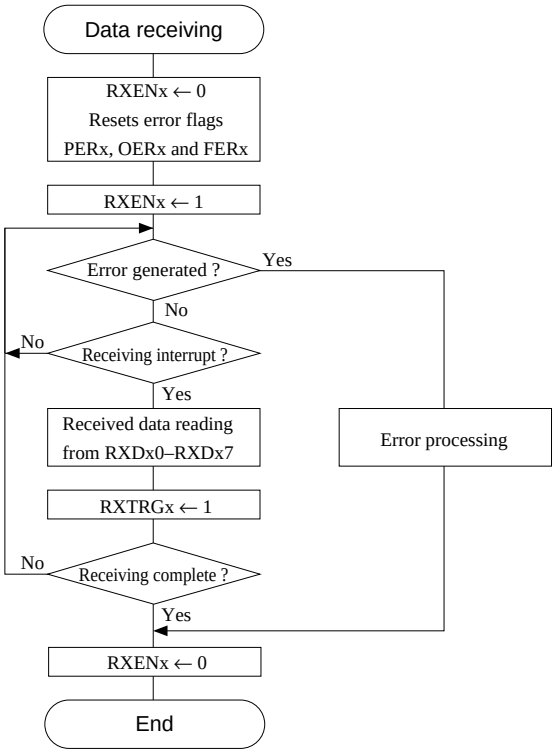


Fig. 11.7.3 Receiving procedure in asynchronous mode

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXENx to set the receiving disable status and to reset the respective PERx, OERx, FERx flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXENx to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SINx terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag FSERRx is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the received data buffer and the receiving complete interrupt flag FSRECx is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag FSRECx is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the received data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from RXDx0–RXDx7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRGx to inform that the receive data has been read out. When the following data is received prior to writing "1" to RXTRGx, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXENx, when the receiving is completed.

■ Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error
When writing "1" to the EPRx register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.
The parity check is performed when data received in the shift register is transferred to the received data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMDx register match. When it does not match, it is recognized as an parity error and the parity error flag PERx and the error interrupt factor flag FSERRx are set to "1".
When interrupt has been enabled, an error interrupt is generated at this point.
The PERx flag is reset to "0" by writing "1".
Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.
The received data at this point cannot assured because of the parity error.

(2) Framing error

In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FERx and the error interrupt factor flag FSERRx are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
The FERx flag is reset to "0" by writing "1".
Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

When the next data is received before "1" is written to RXTRGx, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OERx and the error interrupt factor flag FSERRx are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OERx flag is reset to "0" by writing "1" into it.
Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.
Furthermore, when the timing for writing "1" to RXTRGx and the timing for the received data transfer to the received data buffer overlap, it will be recognized as an overrun error.

■ Timing chart

Figure 11.7.4 show the asynchronous transfer timing chart.

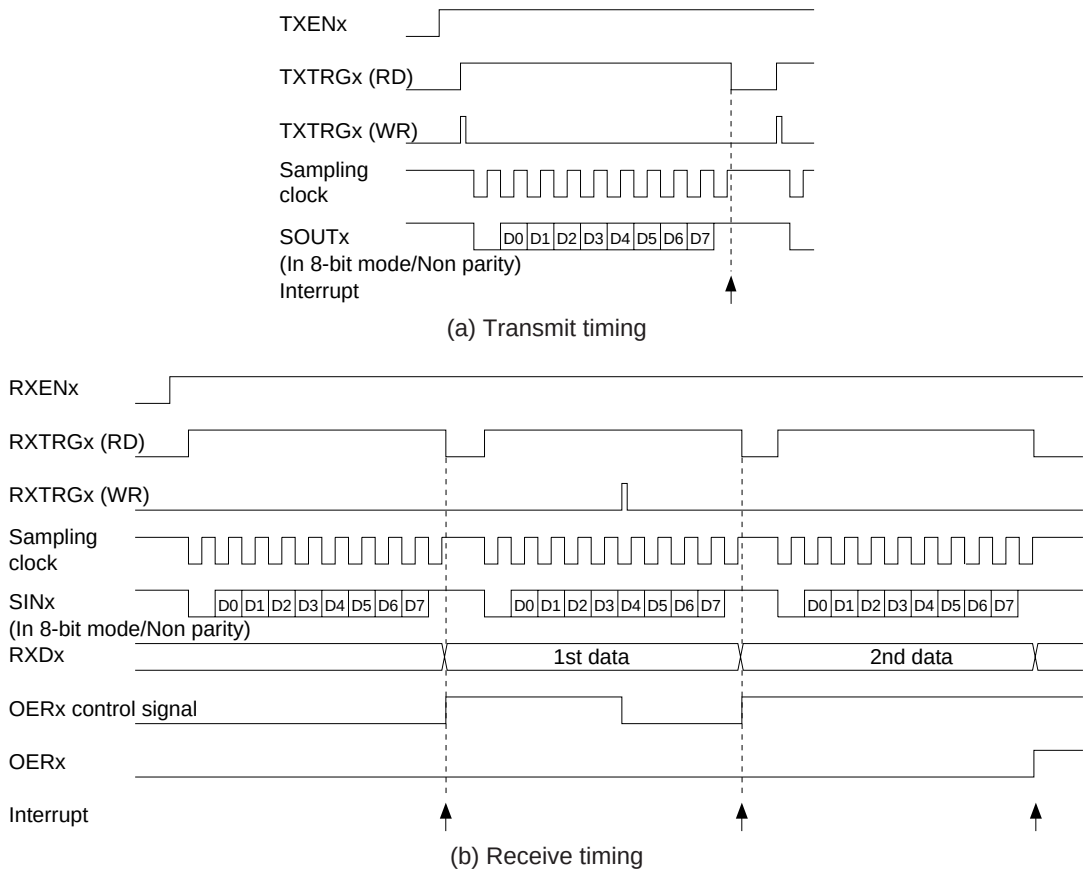


Fig. 11.7.4 Timing chart (asynchronous transfer, LSB first, stop bit = 1 bit)

11.8 Interrupt Function

This serial interface includes a function that generates the below indicated three types of interrupts.

- **Transmitting complete interrupt**
- **Receiving complete interrupt**
- **Error interrupt**

The interrupt factor flag FSxxx and the interrupt enable register ESxxx for the respective interrupt factors are provided and then the interrupt enable/disable can be selected by the software. In addition, a priority level of the serial interface interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSIFx0 and PSIFx1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see Chapter 7, "Interrupt and Standby Status".
Figure 11.8.1 shows the configuration of the serial interface interrupt circuit.

■ Transmitting complete interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag FSTRAx to "1". When set in this manner, if the corresponding interrupt enable register ESTRAx is set to "1" and the corresponding interrupt priority registers PSIFx0 and PSIFx1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESTRAx and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSTRAx is set to "1".
The interrupt factor flag FSTRAx is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting start (writing "1" to TXTRGx) can be controlled by generation of this interrupt factor.
The exception processing vector address is set as follows:

Ch. 0 transmitting complete interrupt: 00002AH
Ch. 1 transmitting complete interrupt: 000030H

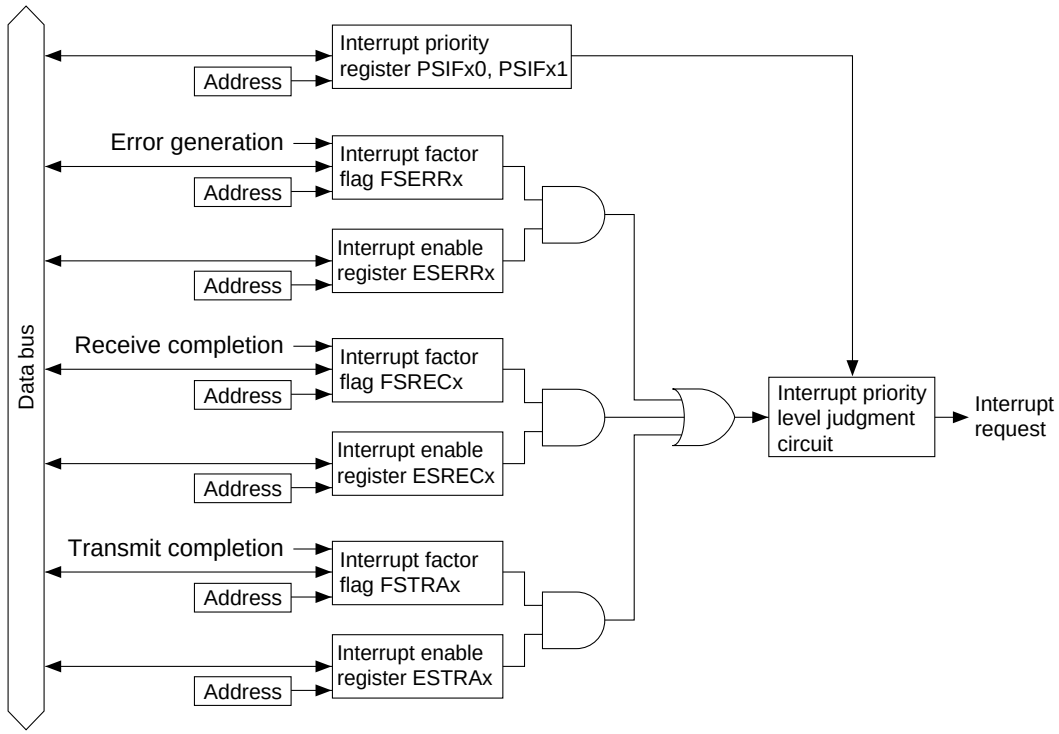


Fig. 11.8.1 Configuration of serial interface interrupt circuit

■ Receiving complete interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the received data buffer and it sets the interrupt factor flag FSRECx to "1". When set in this manner, if the corresponding interrupt enable register ESRECx is set to "1" and the corresponding interrupt priority registers PSIFx0 and PSIFx1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESRECx and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSRECx is set to "1".
The interrupt factor flag FSRECx is reset to "0" by writing "1".

The generation of this interrupt factor permits the received data to be read.

Also, the interrupt factor flag is set to "1" when a parity error or framing error is generated.

The exception processing vector address is set as follows:

Ch. 0 receiving complete interrupt: 000028H
Ch. 1 receiving complete interrupt: 00002EH

■ Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag FSERRx to "1". When set in this manner, if the corresponding interrupt enable register ESERRx is set to "1" and the corresponding interrupt priority registers PSIFx0 and PSIFx1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written in the interrupt enable register ESERRx and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSERRx is set to "1".
The interrupt factor flag FSERRx is reset to "0" by writing "1".

Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PERx (parity error), OERx (overrun error) and FERx (framing error).

The exception processing vector address is set as follows:

Ch. 0 receive error interrupt: 000026H
Ch. 1 receive error interrupt: 00002CH

11.9 Details of Control Registers

Table 11.9.1 show the serial interface control bits.

Table 11.9.1(a) Serial interface control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF48	D7	STPB0	SIF0 stop bit selection	2 bits	1 bit	0	R/W	Only for asynchronous mode
	D6	EPR0	SIF0 parity enable register	With parity	Non parity	0	R/W	
	D5	PMD0	SIF0 parity mode selection	Odd	Even	0	R/W	
	D4	SCS01	SIF0 clock source selection SCS01 SCS00 Clock source 1 1 Programmable timer			0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS00	1 0 fOSC3 / 4 0 1 fOSC3 / 8 0 0 fOSC3 / 16			0	R/W	
	D2	SMD01	SIF0 mode selection SMD01 SMD00 Mode 1 1 Asynchronous 8-bit			0	R/W	
	D1	SMD00	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master			0	R/W	
	D0	ESIF0	SIF0 enable register	Serial I/F	I/O port	0	R/W	
00FF49	D7	SDP0	SIF0 data input/output permutation selection	MSB first	LSB first	0	R/W	
	D6	FER0	SIF0 framing error flag R	Error	No error	0	R/W	Only for asynchronous mode
			W	Reset (0)	No operation			
	D5	PER0	SIF0 parity error flag R	Error	No error	0	R/W	
			W	Reset (0)	No operation			
	D4	OER0	SIF0 overrun error flag R	Error	No error	0	R/W	
			W	Reset (0)	No operation			
	D3	RXTRG0	SIF0 receive trigger/status R	Run	Stop	0	R/W	
			W	Trigger	No operation			
	D2	RXEN0	SIF0 receive enable	Enable	Disable	0	R/W	
	D1	TXTRG0	SIF0 transmit trigger/status R	Run	Stop	0	R/W	
			W	Trigger	No operation			
	D0	TXEN0	SIF0 transmit enable	Enable	Disable	0	R/W	
00FF4A	D7	TXD07	SIF0 transmit data D7 (MSB)	High	Low	X	R/W	
	D6	TXD06	SIF0 transmit data D6					
	D5	TXD05	SIF0 transmit data D5					
	D4	TXD04	SIF0 transmit data D4					
	D3	TXD03	SIF0 transmit data D3					
	D2	TXD02	SIF0 transmit data D2					
	D1	TXD01	SIF0 transmit data D1					
	D0	TXD00	SIF0 transmit data D0 (LSB)					
00FF4B	D7	RXD07	SIF0 receive data D7 (MSB)	High	Low	X	R	
	D6	RXD06	SIF0 receive data D6					
	D5	RXD05	SIF0 receive data D5					
	D4	RXD04	SIF0 receive data D4					
	D3	RXD03	SIF0 receive data D3					
	D2	RXD02	SIF0 receive data D2					
	D1	RXD01	SIF0 receive data D1					
	D0	RXD00	SIF0 receive data D0 (LSB)					

Table 11.9.1(b) Serial interface control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF4C	D7	STPB1	SIF1 stop bit selection		2 bits	1 bit	0	R/W	Only for asynchronous mode
	D6	EPR1	SIF1 parity enable register		With parity	Non parity	0	R/W	
	D5	PMD1	SIF1 parity mode selection		Odd	Even	0	R/W	
	D4	SCS11	SIF1 clock source selection SCS11 SCS10 Clock source 1 1 Programmable timer				0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS10	1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16				0	R/W	
	D2	SMD11	SIF1 mode selection SMD11 SMD10 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD10	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF1	SIF1 enable register		Serial I/F	I/O port	0	R/W	
00FF4D	D7	SDP1	SIF1 data input/output permutation selection		MSB first	LSB first	0	R/W	
	D6	FER1	SIF1 framing error flag	R	Error	No error	0	R/W	Only for asynchronous mode
				W	Reset (0)	No operation			
	D5	PER1	SIF1 parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER1	SIF1 overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG1	SIF1 receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN1	SIF1 receive enable		Enable	Disable	0	R/W	
	D1	TXTRG1	SIF1 transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN1	SIF1 transmit enable		Enable	Disable	0	R/W	
00FF4E	D7	TXD17	SIF1 transmit data D7 (MSB)		High	Low	X	R/W	
	D6	TXD16	SIF1 transmit data D6						
	D5	TXD15	SIF1 transmit data D5						
	D4	TXD14	SIF1 transmit data D4						
	D3	TXD13	SIF1 transmit data D3						
	D2	TXD12	SIF1 transmit data D2						
	D1	TXD11	SIF1 transmit data D1						
	D0	TXD10	SIF1 transmit data D0 (LSB)						
00FF4F	D7	RXD17	SIF1 receive data D7 (MSB)		High	Low	X	R	
	D6	RXD16	SIF1 receive data D6						
	D5	RXD15	SIF1 receive data D5						
	D4	RXD14	SIF1 receive data D4						
	D3	RXD13	SIF1 receive data D3						
	D2	RXD12	SIF1 receive data D2						
	D1	RXD11	SIF1 receive data D1						
	D0	RXD10	SIF1 receive data D0 (LSB)						

ESIF0: 00FF48H•D0
ESIF1: 00FF4CH•D0

Configures the serial interface terminals.

When "1" is written: Serial input / output terminal
When "0" is written: I / O port terminal
Reading: Valid

The ESIFx is the serial interface enable register and P10–P13 (P14–P17) terminals become serial input / output terminals (SINx, SOUTx, $\overline{\text{SCLKx}}$, $\overline{\text{SRDYx}}$) when "1" is written, and they become I / O port terminals when "0" is written.
Also, see Table 11.3.2 for the terminal settings according to the transfer modes.
At initial reset, ESIFx is set to "0" (I / O port).

SMD00, SMD01: 00FF48H•D1, D2
SMD10, SMD11: 00FF4CH•D1, D2

Set the transfer modes according to Table 11.9.2.

Table 11.9.2 Transfer mode settings

SMDx1	SMDx0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

SMDx0 and SMDx1 can also read out.
At initial reset, this register is set to "0" (clock synchronous master mode).

SCS00, SCS01: 00FF48H•D3, D4
SCS10, SCS11: 00FF4CH•D3, D4

Select the clock source according to Table 11.9.3.

Table 11.9.3 Clock source selection

SCSx1	SCSx0	Clock source
1	1	Programmable timer 1 (Ch. 0) Programmable timer 7 (Ch. 1)
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

SCSx0 and SCSx1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid.
At initial reset, this register is set to "0" (f_{OSC3} / 16).

PMD0: 00FF48H•D5
PMD1: 00FF4CH•D5

Selects odd parity / even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

When "1" is written to PMDx, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPRx. When "0" has been written to EPRx, the parity setting by PMDx becomes invalid.
At initial reset, PMDx is set to "0" (even parity).

EPR0: 00FF48H•D6
EPR1: 00FF4CH•D6

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPRx, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPRx setting becomes invalid in the clock synchronous mode.
At initial reset, EPRx is set to "0" (non parity).

STPB0: 00FF48H•D7
STPB1: 00FF4CH•D7

Selects the stop bit length for asynchronous data transfer.

When "1" is written: 2 bits
When "0" is written: 1 bit
Reading: Valid

STPBx is the stop bit select register that is effective in asynchronous mode. When "1" is written to STPBx, the stop bit length is set to 2 bits, and when "0" is written, it is set to 1 bit.
In clock synchronous mode, no start / stop bits can be added to transfer data. Therefore, setting STPBx becomes invalid.
At initial reset, STPBx is set to "0" (1 bit).

TXEN0: 00FF49H•D0
TXEN1: 00FF4DH•D0

Sets the serial interface to the transmitting enable status.

When "1" is written: Transmitting enable
When "0" is written: Transmitting disable
Reading: Valid

When "1" is written to TXENx, the serial interface shifts to the transmitting enable status and shifts to the transmitting disable status when "0" is written. Set TXENx to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, TXENx is set to "0" (transmitting disable).

TXTRG0: 00FF49H•D1
TXTRG1: 00FF4DH•D1

Functions as the transmitting start trigger and the operation status indicator (transmitting / stop status).

When "1" is read: During transmitting
When "0" is read: During stop

When "1" is written: Transmitting start
When "0" is written: Invalid

Starts the transmitting when "1" is written to TXTRGx after writing the transmitting data.
TXTRGx can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRGx is set to "0" (during stop).

RXEN0: 00FF49H•D2
RXEN1: 00FF4DH•D2

Sets the serial interface to the receiving enable status.

When "1" is written: Receiving enable
When "0" is written: Receiving disable
Reading: Valid

When "1" is written to RXENx, the serial interface shifts to the receiving enable status and shifts to the receiving disable status when "0" is written.
Set RXENx to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, RXENx is set to "0" (receiving disable).

RXTRG0: 00FF49H•D3
RXTRG1: 00FF4DH•D3

Functions as the receiving start trigger or preparation for the following data receiving and the operation status indicator (during receiving / during stop).

When "1" is read: During receiving
When "0" is read: During stop

When "1" is written: Receiving start / following data receiving preparation
When "0" is written: Invalid

RXTRGx has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRGx in the clock synchronous system, is used as the trigger for the receiving start.
Writes "1" into RXTRGx to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{\text{SRDYx}}$ becomes "0" at the point where "1" has been written into the RXTRGx.)

RXTRGx is used in the asynchronous system for preparation of the following data receiving. Reads the received data located in the received data buffer and writes "1" into RXTRGx to inform that the received data buffer has shifted to empty. When "1" has not been written to RXTRGx, the overrun error flag OERx is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRGx, an overrun error occurs.)

In addition, RXTRGx can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRGx is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRGx is set to "0" (during stop).

OER0: 00FF49H•D4
OER1: 00FF4DH•D4

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OERx is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when the receiving of data has been completed prior to the writing of "1" to RXTRGx in the asynchronous mode.
OERx is reset to "0" by writing "1".
At initial reset and when RXENx is "0", OERx is set to "0" (no error).

PER0: 00FF49H•D5
PER1: 00FF4DH•D5

Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PERx is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, if data that does not match the parity is received, a parity error is generated.
PERx is reset to "0" by writing "1".
At initial reset and when RXENx is "0", PERx is set to "0" (no error).

FER0: 00FF49H•D6
FER1: 00FF4DH•D6

Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FERx is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving of the asynchronous mode has become "0", a framing error is generated.
FERx is reset to "0" by writing "1".
At initial reset and when RXENx is "0", FERx is set to "0" (no error).

SDP0: 00FF49H•D7
SDP1: 00FF4DH•D7

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, SDPx is set to "0" (LSB first).

TXD00–TXD07: 00FF4AH
TXD10–TXD17: 00FF4EH

Write the transmitting data into the transmit shift register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to starting transmitting.
In the case of continuous transmitting, wait for the transmitting complete interrupt, then write the data.
The TXDx7 becomes invalid for the asynchronous 7-bit mode.
Converted serial data for which the bits set at "1" as HIGH (V_{DD}) level and for which the bits set at "0" as LOW (V_{SS}) level are output from the SOUTx terminal.
At initial reset, transmitting data is undefined.

RXD00–RXD07: 00FF4BH
RXD10–RXD17: 00FF4FH

The received data can be read out.

When "1" is read: HIGH level
When "0" is read: LOW level

The data from the received data buffer can be read out. Since the sift register is provided separately from this buffer, reading can be done during the receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.) Read the data after waiting for the receiving complete interrupt.
When performing parity check in the asynchronous 7-bit mode, "0" is loaded into the 8th bit (RXDx7) that corresponds to the parity bit.
The serial data input from the SINx terminal is level converted, making the HIGH (V_{DD}) level bit "1" and the LOW (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

11.10 Precautions

(1) Be sure to initialize the serial interface mode in the transmitting / receiving disable status (TXENx = RXENx = "0").

(2) Do not perform double trigger (writing "1") to TXTRGx (RXTRGx) when the serial interface is in the transmitting (receiving) operation. Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXENx = RXENx = "0".)

(3) In the clock synchronous mode, since one clock line ($\overline{SCLKx}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.) Consequently, be sure not to write "1" to RXTRGx (TXTRGx) when TXTRGx (RXTRGx) is "1".

(4) When a parity error or framing error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag FSERRx is set to "1" prior to the receiving complete interrupt factor flag FSRECx for the time indicated in Table 11.10.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag FSRECx to "0" by providing a wait time in error processing routines and similar routines. When an overrun error is generated, the receiving complete interrupt factor flag FSRECx is not set to "1" and a receiving complete interrupt is not generated.

Table 11.10.1 Time difference between FSERRx and FSRECx on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 19, "Electrical Characteristics".)
At initial reset, the OSC3 oscillation circuit is set to ON status.

12 CLOCK TIMER

12.1 Configuration of Clock Timer

The S1C88655 has built in a clock timer that uses the OSC1 oscillation circuit as clock source. The clock timer is composed of an 8-bit binary counter that uses the 256 Hz signal (when f_{OSC1} = 32.768 kHz) dividing f_{OSC1} as its input clock and can read the data of each bit (128–1 Hz) by software. Normally, this clock timer is used for various timing functions such as clocks.
The configuration of the clock timer is shown in Figure 12.1.1.

Note: The frequency values described in this chapter assumes that the OSC1 oscillation frequency (f_{OSC1}) is 32.768 kHz. If f_{OSC1} is not 32.768 kHz, this timer cannot be used for clocking.

12.2 Interrupt Function

The clock timer can generate an interrupt by each of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals.
The configuration of the clock timer interrupt circuit is shown in Figure 12.2.1.

Interrupts are generated by respectively setting the corresponding interrupt factor flags FTM32, FTM8, FTM2 and FTM1 at the falling edge of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals to "1". Interrupt can be prohibited by the setting the interrupt enable registers ETM32, ETM8, ETM2 and ETM1 corresponding to each interrupt factor flag.
In addition, a priority level of the clock timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PTM0 and PTM1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see Chapter 7, "Interrupt and Standby Status".

The exception processing vector addresses for each interrupt factor are respectively set as shown below.

32 Hz interrupt: 000032H
8 Hz interrupt: 000034H
2 Hz interrupt: 000036H
1 Hz interrupt: 000038H

Figure 12.2.2 shows the timing chart for the clock timer.

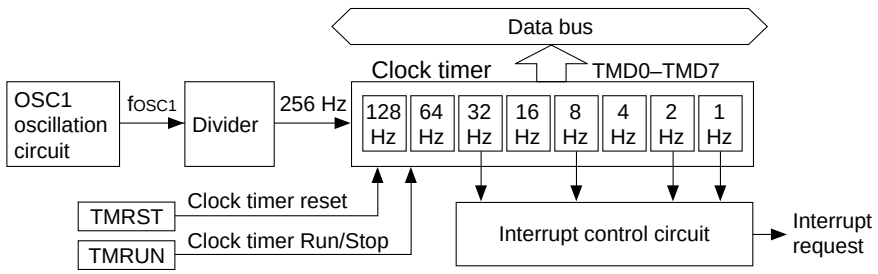


Fig. 12.1.1 Configuration of clock timer

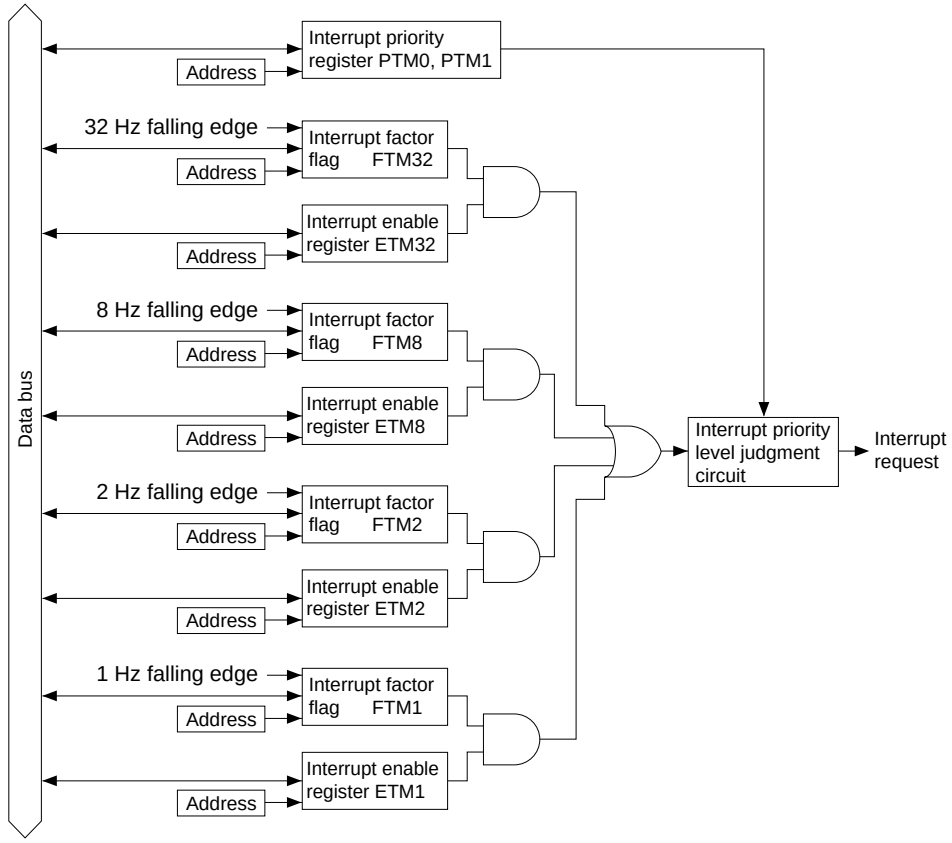


Fig. 12.2.1 Configuration of clock timer interrupt circuit

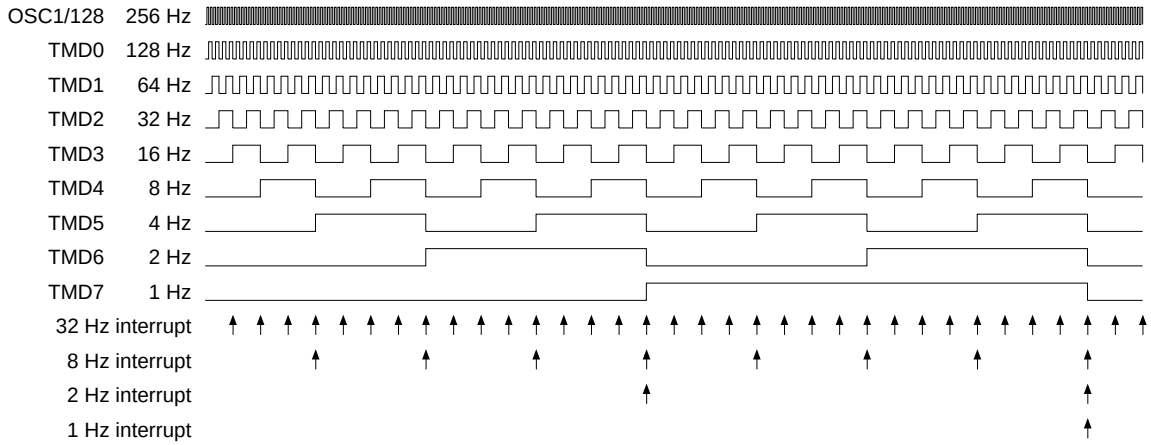


Fig. 12.2.2 Timing chart of clock timer

12.3 Details of Control Registers

Table 12.3.1 shows the clock timer control bits.

Table 12.3.1 Clock timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	–	–	–	0	R	
	D3	–	–	–	–	0	R	
	D2	–	–	–	–	0	R	
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz					
	D5	TMD5	Clock timer data 4 Hz					
	D4	TMD4	Clock timer data 8 Hz					
	D3	TMD3	Clock timer data 16 Hz					
	D2	TMD2	Clock timer data 32 Hz					
	D1	TMD1	Clock timer data 64 Hz					
	D0	TMD0	Clock timer data 128 Hz					

TMD0–TMD7: 00FF41H

The clock timer data can be read out.
Each bit of TMD0–TMD7 and frequency correspondence are as follows:

TMD0: 128 Hz TMD4: 8 Hz
TMD1: 64 Hz TMD5: 4 Hz
TMD2: 32 Hz TMD6: 2 Hz
TMD3: 16 Hz TMD7: 1 Hz

Since the TMD0–TMD7 is exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

TMRST: 00FF40H•D1

Resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to the TMRST.
When the clock timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the TMRST.
Since the TMRST is exclusively for writing, it always becomes "0" during reading.

TMRUN: 00FF40H•D0

Controls RUN / STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer starts up-counting by writing "1" to the TMRUN and stops by writing "0".
In the STOP status, the count data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the TMRUN is set to "0" (STOP).

12.4 Precautions

(1) The clock timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to the TMRUN, the timer shifts to STOP status when the counter is incremented "1". The TMRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 12.4.1 shows the timing chart of the RUN / STOP control.

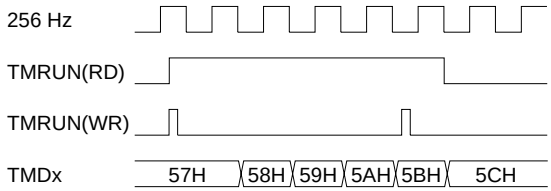


Fig. 12.4.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the clock timer is in the RUN status (TMRUN = "1"). The clock timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (TMRUN = "0") prior to executing the SLP instruction.

13 PROGRAMMABLE TIMER

13.1 Configuration of Programmable Timer

The S1C88655 has four built-in 16-bit programmable timer systems. Each system timer consists of a 16-bit presettable down counter, and can be used as 16-bit × 1 channel or 8-bit × 2 channels of programmable timer. Furthermore, they function as event counters using the input port terminal. Figures 13.1.1 and 13.1.2 show the configuration of the 16-bit programmable timers.
Two 8-bit down counters, the reload data register and compare data register corresponding to each down counter are arranged in the 16-bit programmable timer.
The reload data register is used to set an initial value to the down counter.
The compare data register stores data for comparison with the content of the down counter.
By setting these registers, a PWM waveform is generated and it can be output to external devices as the TOUT0, 1, 2 or 3 signal. Furthermore, the serial interface clock is generated from the underflow signal of Timer 1 for serial interface Ch. 0 or Timer 7 for Ch. 1. The Timer 5 underflow signal can be used to set the source clock for the display timing generator.

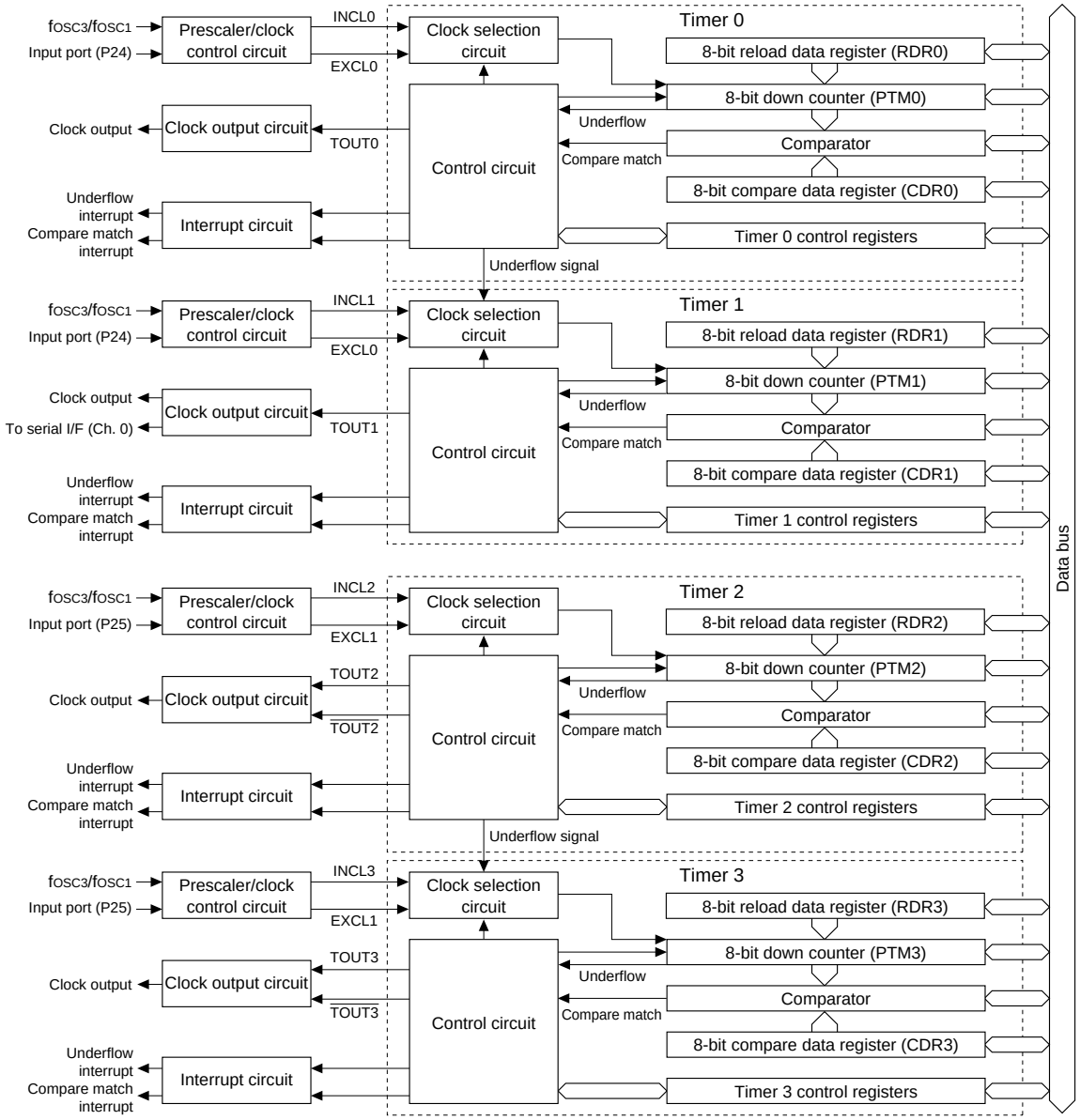


Fig. 13.1.1 Configuration of 16-bit programmable timer (Timers 1–3)

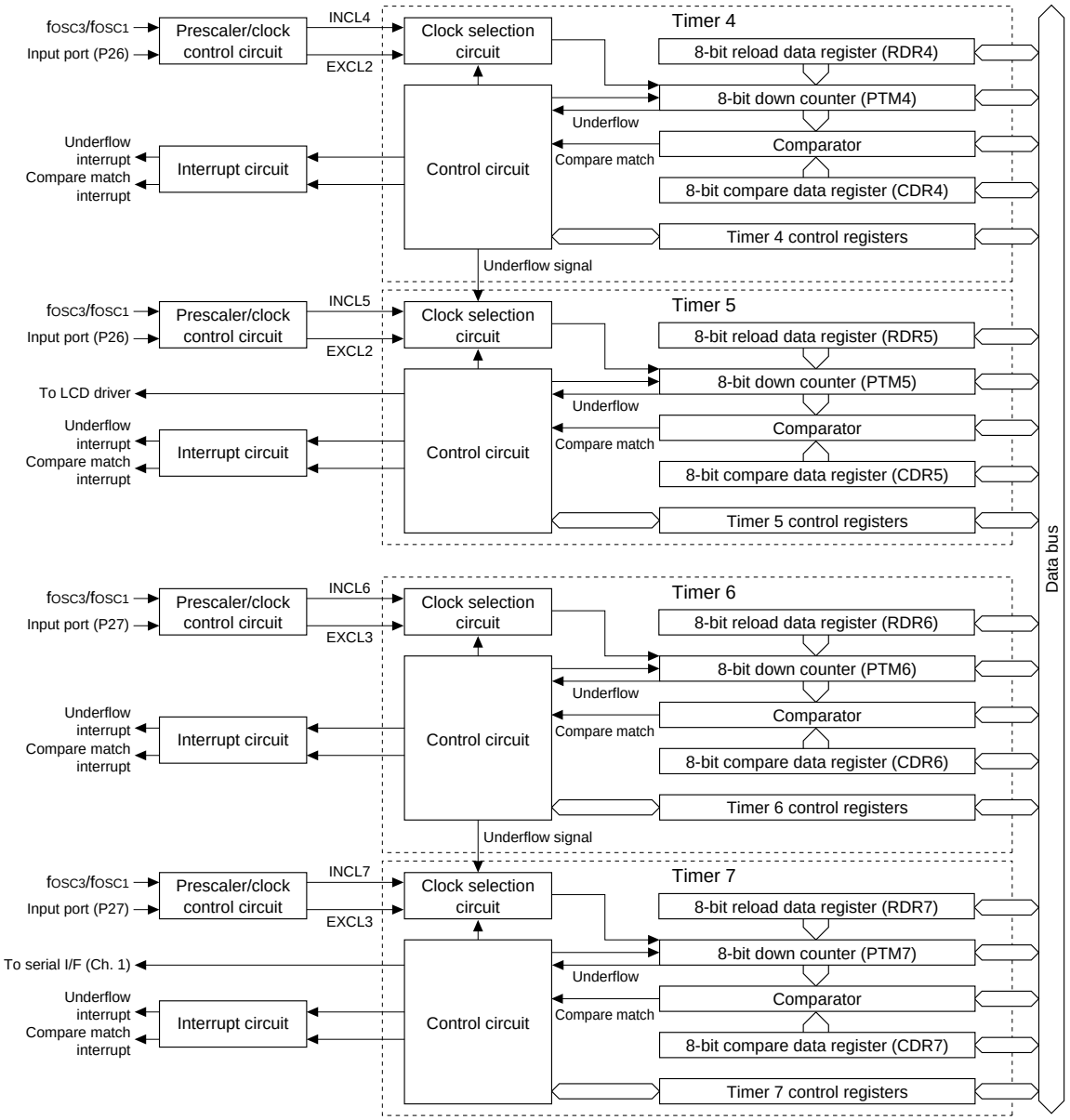


Fig. 13.1.2 Configuration of 16-bit programmable timer (Timers 4–7)

13.2 Operation Mode

Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, or Timers 6 and 7 can be used as two channels of 8-bit timers or one channel of 16-bit timer. Two kinds of operation modes are provided corresponding to this configuration, and it can be selected by the 8/16-bit mode selection registers MODE16_A (for Timer 0–1) through MODE16_D (for Timer 6–7). When "0" is set to the MODE16_A register, Timers 0 and 1 enter the 8-bit mode (8-bit × 2 channels) and when "1" is set, they enter the 16-bit mode (16-bit × 1 channel).
In the 8-bit mode, Timers 0 and 1 can be controlled individually.

In the 16-bit mode, the underflow signal of Timer 0 is used as the input clock of Timer 1 so that the down counters operate as a 16-bit counter.
The timer in the 16-bit mode is controlled with the control registers for Timer 0 except for the clock output.
MODE16_B through MODE16_D have the same function.

Figure 13.2.1 shows the timer configuration depending on the operation mode and Table 13.2.1 shows the configuration of the control registers.

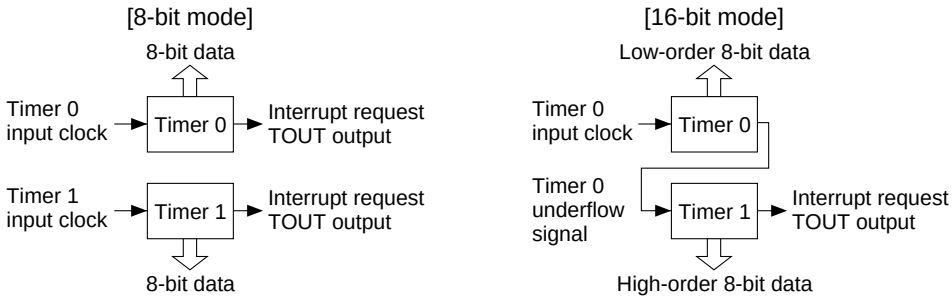


Fig. 13.2.1 Counter configuration in 8- and 16-bit mode (example of Timers 0 and 1)

Table 13.2.1(a) Control registers in 8-bit mode (example of Timers 0 and 1)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	

Table 13.2.1(b) Control registers in 16-bit mode (example of Timers 0 and 1)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	Reserved register
	D3	PTOUT0	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	
00FF31	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	
	D1	PSET1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	W	"0" when being read
	D0	CKSEL1	Invalid (fixed at "0")	Invalid	Fixed at "0"	0	R/W	

Note: The register names contain a timer number (0–7) to identify the timer to which the register belongs. The following explanation uses "x" instead of the timer number except when it is required. For example, PTRUNx represents PTRUN0 through PTRUN7. Furthermore, a pair of timers are described as Timer(L) and Timer(H) in explanations for 16-bit mode.
Timer(L) = Timer 0, Timer 2, Timer 4 or Timer 6
Timer(H) = Timer 1, Timer 3, Timer 5 or Timer 7

This is used for register names.

13.3 Setting of Input Clock

The clock to be input to the counter can be selected from either the internal clock or external clock by the input clock selection register (CKSEL) provided for each timer. The internal clock is an output of the prescaler. The external clock is used for the event counter function. A signal from the I/O port is used as the count clock.
Table 13.3.1 shows the input clock selection register and input clock of each timer.

Table 13.3.1 Input clock selection

Timer	Register setting	Input clock
Timer 0	CKSEL0 = "0"	INCL0 (Prescaler)
	CKSEL0 = "1"	EXCL0 (P24 input)
Timer 1	CKSEL1 = "0"	INCL1 (Prescaler)
	CKSEL1 = "1"	EXCL0 (P24 input)
Timer 2	CKSEL2 = "0"	INCL2 (Prescaler)
	CKSEL2 = "1"	EXCL1 (P25 input)
Timer 3	CKSEL3 = "0"	INCL3 (Prescaler)
	CKSEL3 = "1"	EXCL1 (P25 input)
Timer 4	CKSEL4 = "0"	INCL4 (Prescaler)
	CKSEL4 = "1"	EXCL2 (P26 input)
Timer 5	CKSEL5 = "0"	INCL5 (Prescaler)
	CKSEL5 = "1"	EXCL2 (P26 input)
Timer 6	CKSEL6 = "0"	INCL6 (Prescaler)
	CKSEL6 = "1"	EXCL3 (P27 input)
Timer 7	CKSEL7 = "0"	INCL7 (Prescaler)
	CKSEL7 = "1"	EXCL3 (P27 input)

When the external clock is selected, a signal from the I/O port is input to the programmable timer. An noise rejector is incorporated in the external clock input circuit and it can be enabled/disabled using the external clock noise rejector select registers PTNREN_A through PTNREN_D corresponding to the EXCL0 through EXCL3 inputs. Writing "1" to PTNREN_A (–D) enables the noise rejector for the external clock EXCL0 (–3). The noise rejector regards pulses less than a 16/f_{OSC1} seconds in width as noise and rejects them. The external clock must have a pulse width at least double the rejected width.

Note: An external clock cannot be input when the OSC1 oscillation circuit is OFF. When using the noise rejector, be sure to turn the OSC1 oscillation circuit ON.

When PTNREN_A (–D) is "0", the external clock bypasses the noise rejector.

When the internal clock is used, select a source clock and a division ratio of the prescaler to set the clock frequency for each timer.
The source clock is specified using the source clock selection register PRTFx provided for each timer. When "1" is written to PRTFx, the OSC1 clock is selected as the source clock for Timer x. When "0" is written, the OSC3 clock is selected. The OSC3 oscillation circuit must be on before the OSC3 can be used. See Chapter 8, "Oscillation Circuits" for the controlling of the OSC3 oscillation circuit.

The prescaler provides the division ratio selection register PSTx0–PSTx2 for each timer. Note that the division ratio varies depending on the selected source clock.

Table 13.3.2 Division ratio and control registers

Register			Dividing ratio	
PSTx2	PSTx1	PSTx0	(OSC3)	(OSC1)
1	1	1	f_{OSC3}/4096	f_{OSC1}/128
1	1	0	f_{OSC3}/1024	f_{OSC1}/64
1	0	1	f_{OSC3}/256	f_{OSC1}/32
1	0	0	f_{OSC3}/64	f_{OSC1}/16
0	1	1	f_{OSC3}/32	f_{OSC1}/8
0	1	0	f_{OSC3}/8	f_{OSC1}/4
0	0	1	f_{OSC3}/2	f_{OSC1}/2
0	0	0	f_{OSC3}/1	f_{OSC1}/1

The set clock is output to Timer x by writing "1" to the clock control register PRPRTx.

When the 16-bit mode is selected, the programmable timer operates with the clock input to Timer(L), and Timer(H) inputs the Timer(L) underflow signal as the clock. Therefore, the setting of Timer(H) input clock is invalid.

13.4 Operation and Control of Timer

Reload data register and setting of initial value

The reload data register (RDRx) is used to set an initial value of the down counter.
In the 8-bit mode, RDRx is used as an 8-bit register separated for each timer.
In the 16-bit mode, the RDR(L) register is handled as low-order 8 bits of reload data, and the RDR(H) register is as high-order 8 bits.

The reload data register can be read and written, and all the registers are set to FFH at initial reset.

Data written in this register is loaded into the down counter, and a down counting starts from the value. The down counter is preset, in the following two cases:

1) When software presets

The software preset can be done using the preset control bits PSETx corresponding to Timer x. When the preset control bit is set to "1", the content of the reload data register is loaded into the down counter at that point.
In the 16-bit mode, a 16-bit reload data is loaded all at one time by setting PSET(L). In this case, writing to PSET(H) is invalid.

2) When down counter has underflowed during a count

Since the down counter presets the reload data by the underflow, the underflow period is decided according to the value set in the reload data register. This underflow generates an interrupt, and controls the clock (TOUTx signal) output.

Compare data register

The programmable timer has a built-in data comparator so that count data can be compared with an optional value. The compare data register (CDRx) is used to set the value to be compared.
In the 8-bit mode, CDRx is used as an 8-bit register separated for each timer.
In the 16-bit mode, the CDR(L) register is handled as low-order 8 bits of compare data, and the CDR(H) register is as high-order 8 bits.

The compare data register can be read and written, and all the registers are set to 00H at initial reset.

The programmable timer compares count data with the compare data register (CDRx), and generates a compare match signal when they become the same value. This compare match signal generates an interrupt, and controls the clock (TOUTx signal) output.

Timer operation

Timer is equipped with PTRUNx register which controls the RUN / STOP of the timer. Timer x starts down counting by writing "1" to the PTRUNx register. However, it is necessary to control the input clock and to preset the reload data before starting a count.

When "0" is written to PTRUNx register, clock input is prohibited, and the count stops.
This RUN / STOP control does not affect data in the counter. The data in the counter is maintained during count deactivation, so it is possible to resume counting from the data.

In the 8-bit mode, the timers can be controlled individually by the PTRUNx register.
In the 16-bit mode, the PTRUN(L) register controls a pair of timers as a 16-bit timer. In this case, control of the PTRUN(H) register is invalid.

The buffers PTMx is attached to the counter, and reading is possible in optional timing.

When the counter agrees with the data set in the compare data register during down counting, the timer generates a compare match interrupt.
And, when the counter underflows, an underflow interrupt is generated, and the initial value set in the reload data register is loaded to the counter. The interrupt generated does not stop the down counting.
After an underflow interrupt is generated, the counter continues counting from the initial value reloaded.

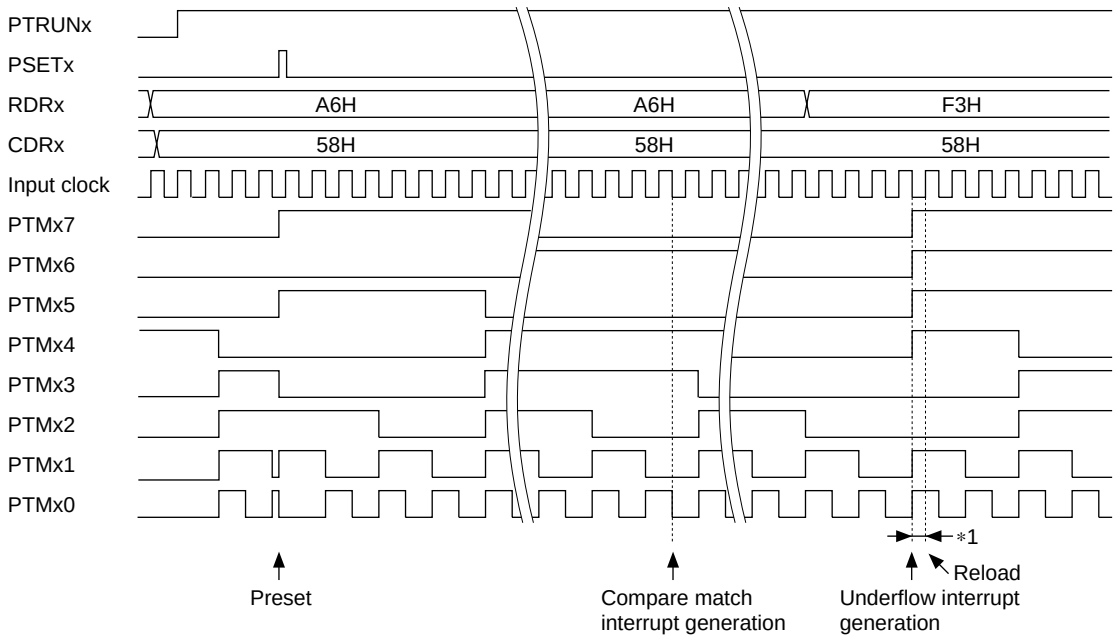


Fig. 13.4.1 Basic operation timing of counter (an example of 8-bit mode)

Note: The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ∗1 in the figure).
To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ∗1. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

13.5 Interrupt Function

The 16-bit programmable timer can generate an interrupt with the compare match signal and underflow signal of each timer.
Figure 13.5.1 shows the configuration of the 16-bit programmable timer interrupt circuit.

The compare match signal and underflow signal of each timer set the corresponding interrupt factor flag to "1". At that point, the interrupt is generated. The interrupt can also be prohibited by setting the interrupt enable register to correspond with the interrupt factor flag.
Furthermore, the priority level of the interrupt for the CPU can be set to an optional level (0–3) using the interrupt priority register.
Table 13.5.1 shows the interrupt factor flags, interrupt enable registers and interrupt priority registers corresponding to the interrupt factors.

In the 8-bit mode, the compare match interrupt factor flag and underflow interrupt factor flag are individually set to "1" by the timers.

In the 16-bit mode, the interrupt factor flags of Timer(H) are set to "1" by the compare match and underflow in 16 bits.

Refer to Chapter 7, "Interrupt and Standby Status", for details of the interrupt control registers and operations subsequent to interrupt generation.

The exception processing vector addresses for the 16-bit programmable timer interrupt are set as follows:

Timer 0 compare match interrupt:	000024H
Timer 0 underflow interrupt:	000022H
Timer 1 underflow interrupt:	000020H
Timer 1 compare match interrupt:	00001EH
Timer 2 underflow interrupt:	00001CH
Timer 2 compare match interrupt:	00001AH
Timer 3 underflow interrupt:	000018H
Timer 3 compare match interrupt:	000016H
Timer 4 underflow interrupt:	000048H
Timer 4 compare match interrupt:	000046H
Timer 5 underflow interrupt:	000044H
Timer 5 compare match interrupt:	000042H
Timer 6 underflow interrupt:	000040H
Timer 6 compare match interrupt:	00003EH
Timer 7 underflow interrupt:	00003CH
Timer 7 compare match interrupt:	00003AH

Table 13.5.1 Interrupt control registers

Interrupt factor		Interrupt factor flag		Interrupt enable register		Interrupt priority register	
		Name	Address·Dx	Name	Address·Dx	Name	Address·Dx
Timer 0	Compare match	FTC0	00FF1BH·D0	ETC0	00FF15H·D0	PPT0	00FF10H·D2
	Counter underflow	FTU0	00FF1BH·D1	ETU0	00FF15H·D1	PPT1	00FF10H·D3
Timer 1	Counter underflow	FTU1	00FF1BH·D2	ETU1	00FF15H·D2		
	Compare match	FTC1	00FF1BH·D3	ETC1	00FF15H·D3		
Timer 2	Counter underflow	FTU2	00FF1BH·D4	ETU2	00FF15H·D4	PPT2	00FF10H·D4
	Compare match	FTC2	00FF1BH·D5	ETC2	00FF15H·D5	PPT3	00FF10H·D5
Timer 3	Counter underflow	FTU3	00FF1BH·D6	ETU3	00FF15H·D6		
	Compare match	FTC3	00FF1BH·D7	ETC3	00FF15H·D7		
Timer 4	Counter underflow	FTU4	00FF1EH·D0	ETU4	00FF18H·D0	PPT4	00FF11H·D4
	Compare match	FTC4	00FF1EH·D1	ETC4	00FF18H·D1	PPT5	00FF11H·D5
Timer 5	Counter underflow	FTU5	00FF1EH·D2	ETU5	00FF18H·D2		
	Compare match	FTC5	00FF1EH·D3	ETC5	00FF18H·D3		
Timer 6	Counter underflow	FTU6	00FF1EH·D4	ETU6	00FF18H·D4	PPT6	00FF11H·D6
	Compare match	FTC6	00FF1EH·D5	ETC6	00FF18H·D5	PPT7	00FF11H·D7
Timer 7	Counter underflow	FTU7	00FF1EH·D6	ETU7	00FF18H·D6		
	Compare match	FTC7	00FF1EH·D7	ETC7	00FF18H·D7		

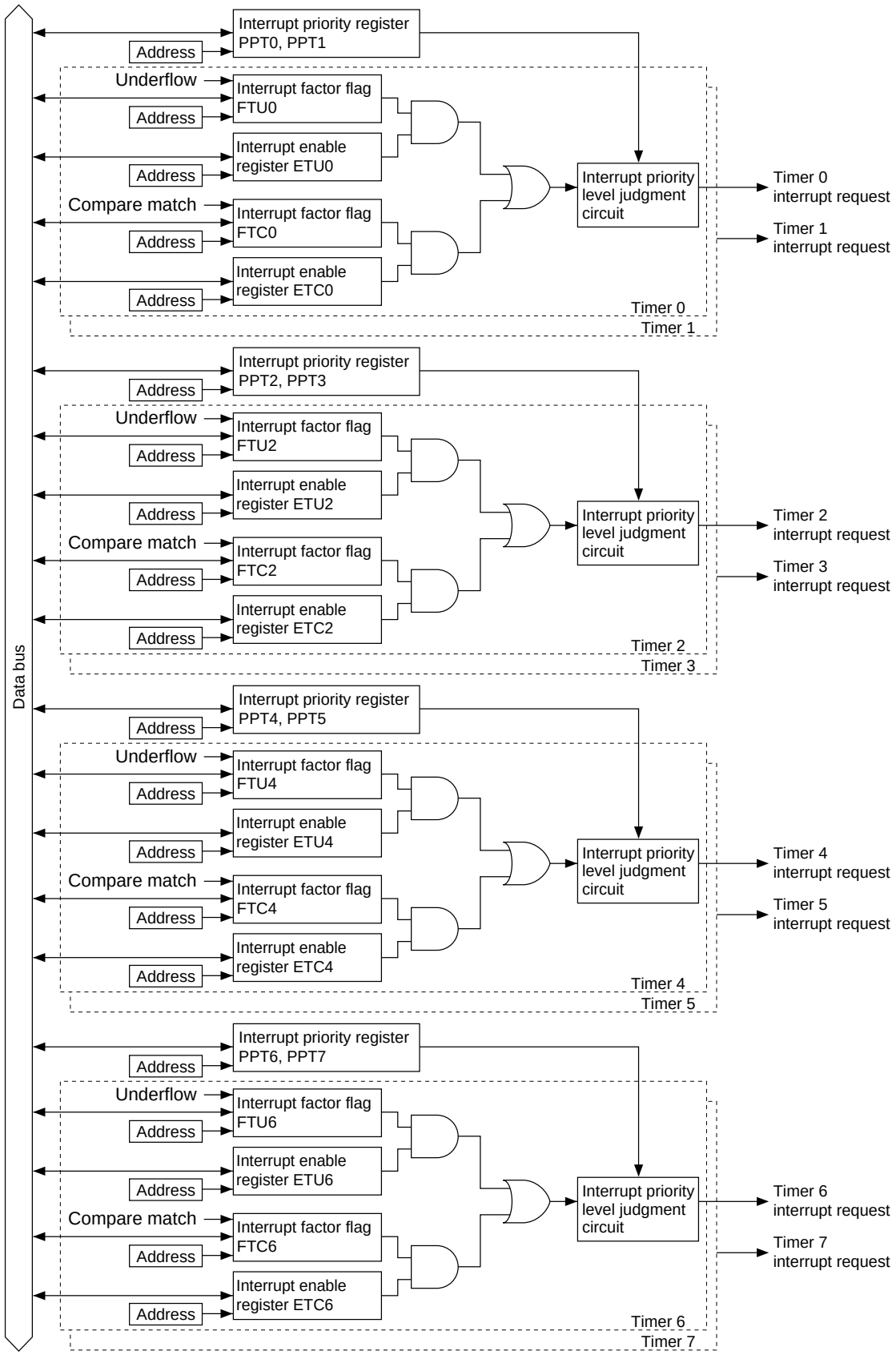


Fig. 13.5.1 Configuration of 16-bit programmable timer interrupt circuit

13.6 Setting TOUT Outputs

The 16-bit programmable timer can generate TOUT signals with the underflow and compare match signals of each timer. The TOUT signal generated in the 16-bit programmable timer can be output from the I/O port terminal shown in Table 13.6.1 so that a clock is supplied for external devices or it can be used as a PWM waveform output.

Table 13.6.1 TOUT output terminal

Timer	Output clock name	Output terminal
Timer 0	TOUT0	P20
Timer 1	TOUT1	P20
Timer 2	TOUT2	P21
	$\overline{\text{TOUT2}}$	P23
Timer 3	TOUT3	P21
	$\overline{\text{TOUT3}}$	P23

The TOUT signal rises at the falling edge of the underflow signal and falls at the falling edge of the compare match signal. $\overline{\text{TOUT}}$ is the inverted TOUT signal. Therefore, it is possible to change the frequency and duty ratio of the TOUT signal by setting the reload data register (RDR) and compare data register (CDR).

However, it needs a condition setting: RDR > CDR, CDR ≠ 0. In the case of RDR ≤ CDR, TOUT signal is fixed at "1".

The TOUT output can be controlled ON and OFF using the clock output control register PTOUTx of each timer and the $\overline{\text{TOUT}}$ output can be controlled using the inverted clock output control register RPTOUTx of Timer 2 or Timer 3.
When PTOUTx (RPTOUTx) is set to "1", the TOUTx ($\overline{\text{TOUTx}}$) signal is output from the corresponding port terminal, when "0" is set, the port is set for DC output. When PTOUTx (RPTOUTx) is "1", settings of the I/O control register IOC20/IOC21/IOC23 and data register P20D/P21D/P23D become invalid.

Note: If PTOUT0 and PTOUT1 are set to "1" at the same time, PTOUT1 is effective. Similarly, if PTOUT2 (RPTOUT2) and PTOUT3 (RPTOUT3) are set to "1", PTOUT3 (RPTOUT3) is effective.

In the 16-bit mode, the output is controlled by the control register PTOUT(H) for Timer(H). The clock is output from Timer(H).

Since the TOUTx ($\overline{\text{TOUTx}}$) signal is generated asynchronously from the register PTOUTx (RPTOUTx), when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 13.6.1 shows the output waveform of TOUT signal.

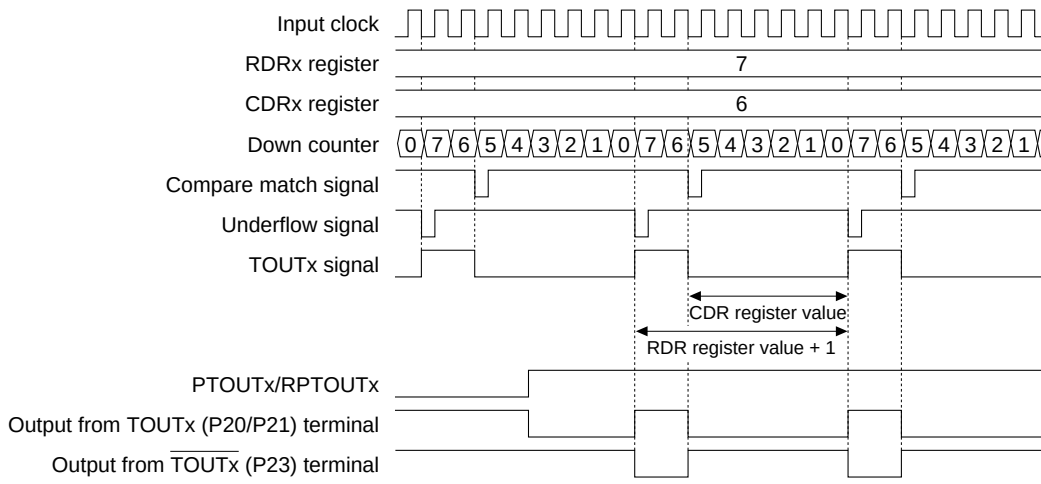


Fig. 13.6.1 Output waveform of TOUT signal

13.7 Setting Transfer Rate of Serial Interface

The underflow signals of Timer 1 and Timer 7 can be used as the source clock for serial interface Ch. 0 and Ch.1, respectively. The transfer rate is set using the registers PST1x and RDR1x for Ch. 0 or PST7x and RDR7x for Ch. 1. (since only the underflow signal is used as the serial interface clock source, the CDR1x or CDR7x register value does not affect the transfer rates. It can be set to any value).

Since the underflow signal of Timer is divided by 32 in the serial interface, the value set in the register RDR1x or RDR7x which corresponds to the transfer rate is shown in the following expression:

$$RDR = \frac{fdiv}{32 \times bps} - 1$$

RDR: RDR1x or RDR7x set value
fdiv: Input clock frequency (setting of PST1x or PST7x)
bps: Transfer rate

Table 13.7.1 Example of transfer rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings							
	f_{OSC3} = 2.4576 MHz		f_{OSC3} = 3.0720 MHz		f_{OSC3} = 3.6864 MHz		f_{OSC3} = 4.3008 MHz	
	PST1x PST7x	RDR1x RDR7x	PST1x PST7x	RDR1x RDR7x	PST1x PST7x	RDR1x RDR7x	PST1x PST7x	RDR1x RDR7x
19,200	00H	03H	00H	04H	00H	05H	00H	06H
9,600	00H	07H	00H	09H	00H	0BH	00H	0DH
4,800	00H	0FH	00H	13H	00H	17H	00H	1BH
2,400	00H	1FH	00H	27H	00H	2FH	00H	37H
1,200	00H	3FH	00H	4FH	00H	5FH	00H	6FH
600	00H	7FH	00H	9FH	00H	BFH	00H	DFH
300	02H	1FH	03H	09H	01H	BFH	01H	DFH
150	02H	3FH	03H	13H	02H	5FH	02H	6FH

∗ Since the underflow signal only is used as the clock source, the CDR1x or CDR7x register value does not affect the transfer rates.

13.8 Setting Clock for LCD Driver Display Timing Generator

The underflow signal of Timer 5 can be used as the source clock for the display timing generator in the LCD driver. This makes it possible to set the frame frequency minutely.
The frequency is set up using the registers PST5x and RDR5x (since only the underflow signal is used as the source clock, the CDR5x register value does not affect the frame signal. It can be set to any value).
The Timer 5 underflow signal is divided by 2 before supplying to the display timing generator, so set a value represented by the following expressions to the register RDR5x.

$$RDR5x = \frac{fdiv}{2 \times f_{CL}} - 1$$

or

$$RDR5x = \frac{fdiv}{2 \times 64 \times f_{FR}} - 1$$

fdiv: Input clock frequency (setting of PST5x)
f_{CL}: Display timing generator source clock frequency (Hz)
f_{FR}: Frame frequency (Hz)

13.9 Details of Control Register

Table 13.9.1 shows the programmable timer control bits.

Table 13.9.1(a) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PRPRT1	Programmable timer 1 clock control	On	Off	0	R/W	
	D6	PST12	Programmable timer 1 division ratio PST12 PST11 PST10 (OSC3) (OSC1) 1 1 1 fosc3 / 4096 fosc1 / 128 1 1 0 fosc3 / 1024 fosc1 / 64 1 0 1 fosc3 / 256 fosc1 / 32 1 0 0 fosc3 / 64 fosc1 / 16 0 1 1 fosc3 / 32 fosc1 / 8 0 1 0 fosc3 / 8 fosc1 / 4 0 0 1 fosc3 / 2 fosc1 / 2 0 0 0 fosc3 / 1 fosc1 / 1			0	R/W	
	D5	PST11				0	R/W	
	D4	PST10				0	R/W	
	D3	PRPRT0	Programmable timer 0 clock control	On	Off	0	R/W	
	D2	PST02	Programmable timer 0 division ratio PST02 PST01 PST00 (OSC3) (OSC1) 1 1 1 fosc3 / 4096 fosc1 / 128 1 1 0 fosc3 / 1024 fosc1 / 64 1 0 1 fosc3 / 256 fosc1 / 32 1 0 0 fosc3 / 64 fosc1 / 16 0 1 1 fosc3 / 32 fosc1 / 8 0 1 0 fosc3 / 8 fosc1 / 4 0 0 1 fosc3 / 2 fosc1 / 2 0 0 0 fosc3 / 1 fosc1 / 1			0	R/W	
	D1	PST01				0	R/W	
	D0	PST00				0	R/W	
00FF21	D7	PRPRT3	Programmable timer 3 clock control	On	Off	0	R/W	
	D6	PST32	Programmable timer 3 division ratio PST32 PST31 PST30 (OSC3) (OSC1) 1 1 1 fosc3 / 4096 fosc1 / 128 1 1 0 fosc3 / 1024 fosc1 / 64 1 0 1 fosc3 / 256 fosc1 / 32 1 0 0 fosc3 / 64 fosc1 / 16 0 1 1 fosc3 / 32 fosc1 / 8 0 1 0 fosc3 / 8 fosc1 / 4 0 0 1 fosc3 / 2 fosc1 / 2 0 0 0 fosc3 / 1 fosc1 / 1			0	R/W	
	D5	PST31				0	R/W	
	D4	PST30				0	R/W	
	D3	PRPRT2	Programmable timer 2 clock control	On	Off	0	R/W	
	D2	PST22	Programmable timer 2 division ratio PST22 PST21 PST20 (OSC3) (OSC1) 1 1 1 fosc3 / 4096 fosc1 / 128 1 1 0 fosc3 / 1024 fosc1 / 64 1 0 1 fosc3 / 256 fosc1 / 32 1 0 0 fosc3 / 64 fosc1 / 16 0 1 1 fosc3 / 32 fosc1 / 8 0 1 0 fosc3 / 8 fosc1 / 4 0 0 1 fosc3 / 2 fosc1 / 2 0 0 0 fosc3 / 1 fosc1 / 1			0	R/W	
	D1	PST21				0	R/W	
	D0	PST20				0	R/W	
00FF23	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PRTF3	Programmable timer 3 source clock selection	fosc1	fosc3	0	R/W	
	D2	PRTF2	Programmable timer 2 source clock selection	fosc1	fosc3	0	R/W	
	D1	PRTF1	Programmable timer 1 source clock selection	fosc1	fosc3	0	R/W	
	D0	PRTF0	Programmable timer 0 source clock selection	fosc1	fosc3	0	R/W	

Table 13.9.1(b) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF24	D7	PRPRT5	Programmable timer 5 clock control	On	Off	0	R/W	
	D6	PST52	Programmable timer 5 division ratio			0	R/W	
	D5	PST51				0	R/W	
	D4	PST50				0	R/W	
	D3	PRPRT4	Programmable timer 4 clock control	On	Off	0	R/W	
	D2	PST42	Programmable timer 4 division ratio			0	R/W	
	D1	PST41				0	R/W	
	D0	PST40				0	R/W	
00FF25	D7	PRPRT7	Programmable timer 7 clock control	On	Off	0	R/W	
	D6	PST72	Programmable timer 7 division ratio			0	R/W	
	D5	PST71				0	R/W	
	D4	PST70				0	R/W	
	D3	PRPRT6	Programmable timer 6 clock control	On	Off	0	R/W	
	D2	PST62	Programmable timer 6 division ratio			0	R/W	
	D1	PST61				0	R/W	
	D0	PST60				0	R/W	
00FF27	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	–	–	–	–	–	R	
	D4	–	–	–	–	–	R	
	D3	PRTF7	Programmable timer 7 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D2	PRTF6	Programmable timer 6 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D1	PRTF5	Programmable timer 5 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
	D0	PRTF4	Programmable timer 4 source clock selection	f_{OSC1}	f_{OSC3}	0	R/W	
00FF30	D7	MODE16_A	PTM0–1 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_A	External clock 0 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT0	PTM0 clock output control	On	Off	0	R/W	
	D2	PTRUN0	PTM0 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET0	PTM0 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL0	PTM0 input clock selection	External clock	Internal clock	0	R/W	

PST52 PST51 PST50 (OSC3) (OSC1)

PST52	PST51	PST50	(OSC3)	(OSC1)
1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

PST42 PST41 PST40 (OSC3) (OSC1)

PST42	PST41	PST40	(OSC3)	(OSC1)
1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

PST72 PST71 PST70 (OSC3) (OSC1)

PST72	PST71	PST70	(OSC3)	(OSC1)
1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

PST62 PST61 PST60 (OSC3) (OSC1)

PST62	PST61	PST60	(OSC3)	(OSC1)
1	1	1	f_{OSC3} / 4096	f_{OSC1} / 128
1	1	0	f_{OSC3} / 1024	f_{OSC1} / 64
1	0	1	f_{OSC3} / 256	f_{OSC1} / 32
1	0	0	f_{OSC3} / 64	f_{OSC1} / 16
0	1	1	f_{OSC3} / 32	f_{OSC1} / 8
0	1	0	f_{OSC3} / 8	f_{OSC1} / 4
0	0	1	f_{OSC3} / 2	f_{OSC1} / 2
0	0	0	f_{OSC3} / 1	f_{OSC1} / 1

Table 13.9.1(c) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF31	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	PTOUT1	PTM1 clock output control	On	Off	0	R/W	
	D2	PTRUN1	PTM1 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET1	PTM1 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL1	PTM1 input clock selection	External clock	Internal clock	0	R/W	
00FF32	D7	RDR07	PTM0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR06	PTM0 reload data D6					
	D5	RDR05	PTM0 reload data D5					
	D4	RDR04	PTM0 reload data D4					
	D3	RDR03	PTM0 reload data D3					
	D2	RDR02	PTM0 reload data D2					
	D1	RDR01	PTM0 reload data D1					
	D0	RDR00	PTM0 reload data D0 (LSB)					
00FF33	D7	RDR17	PTM1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR16	PTM1 reload data D6					
	D5	RDR15	PTM1 reload data D5					
	D4	RDR14	PTM1 reload data D4					
	D3	RDR13	PTM1 reload data D3					
	D2	RDR12	PTM1 reload data D2					
	D1	RDR11	PTM1 reload data D1					
	D0	RDR10	PTM1 reload data D0 (LSB)					
00FF34	D7	CDR07	PTM0 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR06	PTM0 compare data D6					
	D5	CDR05	PTM0 compare data D5					
	D4	CDR04	PTM0 compare data D4					
	D3	CDR03	PTM0 compare data D3					
	D2	CDR02	PTM0 compare data D2					
	D1	CDR01	PTM0 compare data D1					
	D0	CDR00	PTM0 compare data D0 (LSB)					
00FF35	D7	CDR17	PTM1 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR16	PTM1 compare data D6					
	D5	CDR15	PTM1 compare data D5					
	D4	CDR14	PTM1 compare data D4					
	D3	CDR13	PTM1 compare data D3					
	D2	CDR12	PTM1 compare data D2					
	D1	CDR11	PTM1 compare data D1					
	D0	CDR10	PTM1 compare data D0 (LSB)					
00FF36	D7	PTM07	PTM0 data D7 (MSB)	High	Low	1	R	
	D6	PTM06	PTM0 data D6					
	D5	PTM05	PTM0 data D5					
	D4	PTM04	PTM0 data D4					
	D3	PTM03	PTM0 data D3					
	D2	PTM02	PTM0 data D2					
	D1	PTM01	PTM0 data D1					
	D0	PTM00	PTM0 data D0 (LSB)					

Table 13.9.1(d) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF37	D7	PTM17	PTM1 data D7 (MSB)	High	Low	1	R	
	D6	PTM16	PTM1 data D6					
	D5	PTM15	PTM1 data D5					
	D4	PTM14	PTM1 data D4					
	D3	PTM13	PTM1 data D3					
	D2	PTM12	PTM1 data D2					
	D1	PTM11	PTM1 data D1					
	D0	PTM10	PTM1 data D0 (LSB)					
00FF38	D7	MODE16_B	PTM2–3 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_B	External clock 1 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	RPTOUT2	PTM2 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT2	PTM2 clock output control	On	Off	0	R/W	
	D2	PTRUN2	PTM2 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET2	PTM2 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL2	PTM2 input clock selection	External clock	Internal clock	0	R/W	
00FF39	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	–	–	–	–	0	R	
	D4	RPTOUT3	PTM3 inverted clock output control	On	Off	0	R/W	
	D3	PTOUT3	PTM3 clock output control	On	Off	0	R/W	
	D2	PTRUN3	PTM3 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET3	PTM3 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL3	PTM3 input clock selection	External clock	Internal clock	0	R/W	
00FF3A	D7	RDR27	PTM2 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR26	PTM2 reload data D6					
	D5	RDR25	PTM2 reload data D5					
	D4	RDR24	PTM2 reload data D4					
	D3	RDR23	PTM2 reload data D3					
	D2	RDR22	PTM2 reload data D2					
	D1	RDR21	PTM2 reload data D1					
	D0	RDR20	PTM2 reload data D0 (LSB)					
00FF3B	D7	RDR37	PTM3 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR36	PTM3 reload data D6					
	D5	RDR35	PTM3 reload data D5					
	D4	RDR34	PTM3 reload data D4					
	D3	RDR33	PTM3 reload data D3					
	D2	RDR32	PTM3 reload data D2					
	D1	RDR31	PTM3 reload data D1					
	D0	RDR30	PTM3 reload data D0 (LSB)					
00FF3C	D7	CDR27	PTM2 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR26	PTM2 compare data D6					
	D5	CDR25	PTM2 compare data D5					
	D4	CDR24	PTM2 compare data D4					
	D3	CDR23	PTM2 compare data D3					
	D2	CDR22	PTM2 compare data D2					
	D1	CDR21	PTM2 compare data D1					
	D0	CDR20	PTM2 compare data D0 (LSB)					

Table 13.9.1(e) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF3D	D7	CDR37	PTM3 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR36	PTM3 compare data D6					
	D5	CDR35	PTM3 compare data D5					
	D4	CDR34	PTM3 compare data D4					
	D3	CDR33	PTM3 compare data D3					
	D2	CDR32	PTM3 compare data D2					
	D1	CDR31	PTM3 compare data D1					
	D0	CDR30	PTM3 compare data D0 (LSB)					
00FF3E	D7	PTM27	PTM2 data D7 (MSB)	High	Low	1	R	
	D6	PTM26	PTM2 data D6					
	D5	PTM25	PTM2 data D5					
	D4	PTM24	PTM2 data D4					
	D3	PTM23	PTM2 data D3					
	D2	PTM22	PTM2 data D2					
	D1	PTM21	PTM2 data D1					
	D0	PTM20	PTM2 data D0 (LSB)					
00FF3F	D7	PTM37	PTM3 data D7 (MSB)	High	Low	1	R	
	D6	PTM36	PTM3 data D6					
	D5	PTM35	PTM3 data D5					
	D4	PTM34	PTM3 data D4					
	D3	PTM33	PTM3 data D3					
	D2	PTM32	PTM3 data D2					
	D1	PTM31	PTM3 data D1					
	D0	PTM30	PTM3 data D0 (LSB)					
00FF80	D7	MODE16_C	PTM4–5 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_C	External clock 2 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN4	PTM4 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET4	PTM4 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL4	PTM4 input clock selection	External clock	Internal clock	0	R/W	
00FF81	D7	–	–	–	–	0	R	Constantly "0" when being read
	D6	–	–	–	–	0	R	
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN5	PTM5 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET5	PTM5 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL5	PTM5 input clock selection	External clock	Internal clock	0	R/W	
00FF82	D7	RDR47	PTM4 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR46	PTM4 reload data D6					
	D5	RDR45	PTM4 reload data D5					
	D4	RDR44	PTM4 reload data D4					
	D3	RDR43	PTM4 reload data D3					
	D2	RDR42	PTM4 reload data D2					
	D1	RDR41	PTM4 reload data D1					
	D0	RDR40	PTM4 reload data D0 (LSB)					

Table 13.9.1(f) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF83	D7	RDR57	PTM5 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR56	PTM5 reload data D6					
	D5	RDR55	PTM5 reload data D5					
	D4	RDR54	PTM5 reload data D4					
	D3	RDR53	PTM5 reload data D3					
	D2	RDR52	PTM5 reload data D2					
	D1	RDR51	PTM5 reload data D1					
	D0	RDR50	PTM5 reload data D0 (LSB)					
00FF84	D7	CDR47	PTM4 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR46	PTM4 compare data D6					
	D5	CDR45	PTM4 compare data D5					
	D4	CDR44	PTM4 compare data D4					
	D3	CDR43	PTM4 compare data D3					
	D2	CDR42	PTM4 compare data D2					
	D1	CDR41	PTM4 compare data D1					
	D0	CDR40	PTM4 compare data D0 (LSB)					
00FF85	D7	CDR57	PTM5 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR56	PTM5 compare data D6					
	D5	CDR55	PTM5 compare data D5					
	D4	CDR54	PTM5 compare data D4					
	D3	CDR53	PTM5 compare data D3					
	D2	CDR52	PTM5 compare data D2					
	D1	CDR51	PTM5 compare data D1					
	D0	CDR50	PTM5 compare data D0 (LSB)					
00FF86	D7	PTM47	PTM4 data D7 (MSB)	High	Low	1	R	
	D6	PTM46	PTM4 data D6					
	D5	PTM45	PTM4 data D5					
	D4	PTM44	PTM4 data D4					
	D3	PTM43	PTM4 data D3					
	D2	PTM42	PTM4 data D2					
	D1	PTM41	PTM4 data D1					
	D0	PTM40	PTM4 data D0 (LSB)					
00FF87	D7	PTM57	PTM5 data D7 (MSB)	High	Low	1	R	
	D6	PTM56	PTM5 data D6					
	D5	PTM55	PTM5 data D5					
	D4	PTM54	PTM5 data D4					
	D3	PTM53	PTM5 data D3					
	D2	PTM52	PTM5 data D2					
	D1	PTM51	PTM5 data D1					
	D0	PTM50	PTM5 data D0 (LSB)					
00FF88	D7	MODE16_D	PTM6–7 8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D6	PTNREN_D	External clock 3 noise rejector selection	Enable	Disable	0	R/W	
	D5	–	–	–	–	0	R	"0" when being read
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN6	PTM6 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET6	PTM6 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL6	PTM6 input clock selection	External clock	Internal clock	0	R/W	

Table 13.9.1(g) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF89	D7	–	–	–	–	0	R	Constantly "0" when
	D6	–	–	–	–	0	R	being read
	D5	–	–	–	–	0	R	
	D4	–	R/W register	1	0	0	R/W	Reserved register
	D3	–	R/W register	1	0	0	R/W	
	D2	PTRUN7	PTM7 Run/Stop control	Run	Stop	0	R/W	
	D1	PSET7	PTM7 preset	Preset	No operation	0	W	"0" when being read
	D0	CKSEL7	PTM7 input clock selection	External clock	Internal clock	0	R/W	
00FF8A	D7	RDR67	PTM6 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR66	PTM6 reload data D6					
	D5	RDR65	PTM6 reload data D5					
	D4	RDR64	PTM6 reload data D4					
	D3	RDR63	PTM6 reload data D3					
	D2	RDR62	PTM6 reload data D2					
	D1	RDR61	PTM6 reload data D1					
	D0	RDR60	PTM6 reload data D0 (LSB)					
00FF8B	D7	RDR77	PTM7 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RDR76	PTM7 reload data D6					
	D5	RDR75	PTM7 reload data D5					
	D4	RDR74	PTM7 reload data D4					
	D3	RDR73	PTM7 reload data D3					
	D2	RDR72	PTM7 reload data D2					
	D1	RDR71	PTM7 reload data D1					
	D0	RDR70	PTM7 reload data D0 (LSB)					
00FF8C	D7	CDR67	PTM6 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR66	PTM6 compare data D6					
	D5	CDR65	PTM6 compare data D5					
	D4	CDR64	PTM6 compare data D4					
	D3	CDR63	PTM6 compare data D3					
	D2	CDR62	PTM6 compare data D2					
	D1	CDR61	PTM6 compare data D1					
	D0	CDR60	PTM6 compare data D0 (LSB)					
00FF8D	D7	CDR77	PTM7 compare data D7 (MSB)	High	Low	0	R/W	
	D6	CDR76	PTM7 compare data D6					
	D5	CDR75	PTM7 compare data D5					
	D4	CDR74	PTM7 compare data D4					
	D3	CDR73	PTM7 compare data D3					
	D2	CDR72	PTM7 compare data D2					
	D1	CDR71	PTM7 compare data D1					
	D0	CDR70	PTM7 compare data D0 (LSB)					
00FF8E	D7	PTM67	PTM6 data D7 (MSB)	High	Low	1	R	
	D6	PTM66	PTM6 data D6					
	D5	PTM65	PTM6 data D5					
	D4	PTM64	PTM6 data D4					
	D3	PTM63	PTM6 data D3					
	D2	PTM62	PTM6 data D2					
	D1	PTM61	PTM6 data D1					
	D0	PTM60	PTM6 data D0 (LSB)					

Table 13.9.1(h) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF8F	D7	PTM77	PTM7 data D7 (MSB)	High	Low	1	R	
	D6	PTM76	PTM7 data D6					
	D5	PTM75	PTM7 data D5					
	D4	PTM74	PTM7 data D4					
	D3	PTM73	PTM7 data D3					
	D2	PTM72	PTM7 data D2					
	D1	PTM71	PTM7 data D1					
	D0	PTM70	PTM7 data D0 (LSB)					

MODE16_A: 00FF30H•D7
MODE16_B: 00FF38H•D7
MODE16_C: 00FF80H•D7
MODE16_D: 00FF88H•D7

Selects either the 8 / 16 bit mode.

When "1" is written: 16 bits × 1 channel
When "0" is written: 8 bits × 2 channels
Reading: Valid

MODE16_A, MODE16_B, MODE16_C and MODE16_D are the 8 / 16-bit mode selection registers corresponding to Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, and Timers 6 and 7, respectively. Select whether Timer(L) and Timer(H) are used as 2 channels independent 8-bit timers or as 1 channel combined 16-bit timer.
When "0" is written to the MODE16_A (–D) register, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected.
At initial reset, this register is set to "0" (8-bit × 2 channels).

PTNREN_A: 00FF30H•D6
PTNREN_B: 00FF38H•D6
PTNREN_C: 00FF80H•D6
PTNREN_D: 00FF88H•D6

Enables / disables the noise rejector in the external clock input circuit.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

Writing "1" to PTNREN_A (–D) enables the noise rejector for the external clock EXCL0 (–3). The noise rejector regards pulses less than a 16 / f_{OSC1} seconds in width as noise and rejects them.
When PTNREN_A (–D) is "0", the external clock bypasses the noise rejector.
At initial reset, this register is set to "0" (disabled).

CKSEL0: 00FF30H•D0
CKSEL1: 00FF31H•D0
CKSEL2: 00FF38H•D0
CKSEL3: 00FF39H•D0
CKSEL4: 00FF80H•D0
CKSEL5: 00FF81H•D0
CKSEL6: 00FF88H•D0
CKSEL7: 00FF89H•D0

Selects the input clock for each timer.

When "1" is written: External clock
When "0" is written: Internal clock
Reading: Valid

The clock to be input to each timer is selected from either the external clock (input signal of input port) or the internal clock (prescaler output clock).

When "0" is written to the CKSELx register, the internal clock (prescaler output INCLx) is selected as the input clock for Timer x.
When "1" is written, the external clock (EXCL0 (P24 input) for Timers 0 and 1, EXCL1 (P25 input) for Timers 2 and 3, EXCL2 (P26 input) for Timers 4 and 5, EXCL3 (P27 input) for Timers 6 and 7) is selected and the timer functions as an event counter.
In the 16-bit mode, the setting of the CKSEL(H) register is invalid.
At initial reset, this register is set to "0" (internal clock).

PRTF0: 00FF23H•D0
PRTF1: 00FF23H•D1
PRTF2: 00FF23H•D2
PRTF3: 00FF23H•D3
PRTF4: 00FF27H•D0
PRTF5: 00FF27H•D1
PRTF6: 00FF27H•D2
PRTF7: 00FF27H•D3

Selects the source clock for each timer (when internal clock is used).

When "1" is written: f_{OSC1}
When "0" is written: f_{OSC3}
Reading: Valid

When "1" is written to the PRTFx register, the OSC1 clock is selected as the source clock for Timer x.
When "0" is written, the OSC3 clock is selected.
At initial reset, this register is set to "0" (f_{OSC3}).

PST00–PST02: 00FF20H•D0–D2
PST10–PST12: 00FF20H•D4–D6
PST20–PST22: 00FF21H•D0–D2
PST30–PST32: 00FF21H•D4–D6
PST40–PST42: 00FF24H•D0–D2
PST50–PST52: 00FF24H•D4–D6
PST60–PST62: 00FF25H•D0–D2
PST70–PST72: 00FF25H•D4–D6

Selects the input clock for each timer (when internal clock is used).
It can be selected from 8 types of division ratio shown in Tables 13.9.1(a) and (b).
This register can also be read.
At initial reset, this register is set to "0".

PRPRT0: 00FF20H•D3
PRPRT1: 00FF20H•D7
PRPRT2: 00FF21H•D3
PRPRT3: 00FF21H•D7
PRPRT4: 00FF24H•D3
PRPRT5: 00FF24H•D7
PRPRT6: 00FF25H•D3
PRPRT7: 00FF25H•D7

Controls the clock supply of each timer (when internal clock is used).

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to the PRPRTx register, the clock that is selected with the PSTx register is output to Timer x.
When "0" is written, the clock is not output.
At initial reset, the this register is set to "0" (OFF).

RDR00–RDR07: 00FF32H
RDR10–RDR17: 00FF33H
RDR20–RDR27: 00FF3AH
RDR30–RDR37: 00FF3BH
RDR40–RDR47: 00FF82H
RDR50–RDR57: 00FF83H
RDR60–RDR67: 00FF8AH
RDR70–RDR77: 00FF8BH

Sets the initial value for the counter of each timer. Each counter loads the reload data set in this register and counts using it as the initial value.
The reload data set in this register is loaded into the counter when "1" is written to PSETx, or when a counter underflow occurs.
This register can also be read.
At initial reset, this register is set to "FFH".

CDR00–CDR07: 00FF34H
CDR10–CDR17: 00FF35H
CDR20–CDR27: 00FF3CH
CDR30–CDR37: 00FF3DH
CDR40–CDR47: 00FF84H
CDR50–CDR57: 00FF85H
CDR60–CDR67: 00FF8CH
CDR70–CDR77: 00FF8DH

Sets the compare data for each timer.
The timer compares the data set in this register with the corresponding counter data, and outputs the compare match signals when they are the same. The compare match signal controls the interrupt and the TOUT output waveform.
This register can also be read.
At initial reset, this register is set to "00H".

PTM00–PTM07: 00FF36H
PTM10–PTM17: 00FF37H
PTM20–PTM27: 00FF3EH
PTM30–PTM37: 00FF3FH
PTM40–PTM47: 00FF86H
PTM50–PTM57: 00FF87H
PTM60–PTM67: 00FF8EH
PTM70–PTM77: 00FF8FH

The counter data of each timer can be read.
Data can be read at any given time. However, in the 16-bit mode, reading PTM(L) does not latch the Timer(H) counter data in PTM(H). To avoid generating a borrow from Timer(L) to Timer(H), read the counter data after stopping the timer by writing "0" to PTRUN(L).
PTMx can only be read, so writing operation is invalid.
At initial reset, PTMx is set to "FFH".

PSET0: 00FF30H•D1
PSET1: 00FF31H•D1
PSET2: 00FF38H•D1
PSET3: 00FF39H•D1
PSET4: 00FF80H•D1
PSET5: 00FF81H•D1
PSET6: 00FF88H•D1
PSET7: 00FF89H•D1

Presets the reload data to the counter.

When "1" is written: Preset
When "0" is written: Invalid
Reading: Always "0"

Writing "1" to PSETx presets the reload data in the RDRx register to the counter of Timer x. When the counter of Timer x is in RUN status, the counter restarts immediately after presetting.
In the case of STOP status, the counter maintains the preset data.
No operation results when "0" is written.
In the 16-bit mode, writing "1" to PSET(H) is invalid because 16-bit data is preset by PSET(L) only.
PSETx is only for writing, and it is always "0" during reading.

PTRUN0: 00FF30H•D2
PTRUN1: 00FF31H•D2
PTRUN2: 00FF38H•D2
PTRUN3: 00FF39H•D2
PTRUN4: 00FF80H•D2
PTRUN5: 00FF81H•D2
PTRUN6: 00FF88H•D2
PTRUN7: 00FF89H•D2

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter of Timer x starts down-counting by writing "1" to the PTRUNx register and stops by writing "0".
In STOP status, the counter data is maintained until it is preset or the counter restarts. When STOP status changes to RUN status, the counter resumes counting from the data maintained.
In the 16-bit mode, the timers are controlled with the PTRUN(L) register, and the PTRUN(H) register is fixed at "0".
At initial reset, this register is set to "0" (STOP).

PTOUT0: 00FF30H•D3
PTOUT1: 00FF31H•D3
PTOUT2: 00FF38H•D3
PTOUT3: 00FF39H•D3

Controls the output of the TOUT signal.

When "1" is written: TOUT signal output
When "0" is written: DC output
Reading: Valid

The PTOUTx is the output control register for the TOUTx signal (Timer x output clock). When PTOUT0 or PTOUT1 is set to "1", the TOUT0 or TOUT1 signal is output from the P20 port terminal. When PTOUT2 or PTOUT3 is set to "1", the TOUT2 or TOUT3 signal is output from the P21 port terminal. When "0" is set, P20 / P21 is set for DC output.
At this time, settings of the I / O control register IOC20 / IOC21 and data register P20D / P21D become invalid.
In the 16-bit mode, the timers are controlled with the PTOUT(H) register, and the PTOUT(L) register is fixed at "0".
At initial reset, this register is set to "0" (DC output).

Note: If PTOUT0 and PTOUT1 are set to "1" at the same time, PTOUT1 is effective. Similarly, if PTOUT2 and PTOUT3 are set to "1", PTOUT3 is effective. Furthermore, if the programmable timer is set in 16-bit mode, the TOUT0 and TOUT2 signals cannot be output.

RPTOUT2: 00FF38H•D4
RPTOUT3: 00FF39H•D4

Controls the output of the $\overline{\text{TOUT}}$ signal.

When "1" is written: $\overline{\text{TOUT}}$ signal output
When "0" is written: DC output
Reading: Valid

The RPTOUTx is the output control register for the $\overline{\text{TOUTx}}$ signal (Timer x inverted output clock). When RPTOUT2 or RPTOUT3 is set to "1", the $\overline{\text{TOUT2}}$ or $\overline{\text{TOUT3}}$ signal is output from the P23 port terminal. When "0" is set, P23 is set for DC output.
At this time, settings of the I / O control register IOC23 and data register P23D become invalid.
In the 16-bit mode, the timers are controlled with the RPTOUT3 register, and the RPTOUT2 register is fixed at "0".
At initial reset, this register is set to "0" (DC output).

Note: If RPTOUT2 and RPTOUT3 are set to "1" at the same time, RPTOUT3 is effective.

13.10 Precautions

(1) The programmable timer actually enters into RUN or STOP status at the falling edge of the input clock after writing to the PTRUNx register. Consequently, when "0" is written to PTRUNx, the timer stops after counting once more (+1). PTRUNx is read as "1" until the timer actually stops.
Figure 13.10.1 shows the timing chart at the RUN / STOP control.

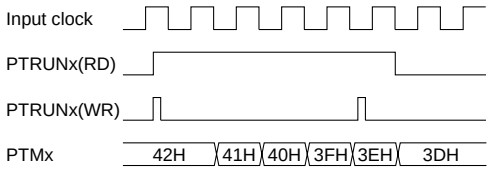


Fig. 13.10.1 Timing chart at RUN/STOP control

(2) When the SLP instruction is executed while the programmable timer is running (PTRUNx = "1"), the timer stops counting during SLEEP status. When SLEEP status is canceled, the timer starts counting. However, the operation becomes unstable immediately after SLEEP status is canceled. Therefore, when shifting to SLEEP status, stop the 16-bit programmable timer (PTRUNx = "0") prior to executing the SLP instruction.
Same as above, the TOUT signal output should be disabled (PTOUTx = "0") so that an unstable clock is not output to the clock output port terminal.

(3) In the 16-bit mode, reading PTM(L) does not latch the Timer(H) counter data in PTM(H). To avoid generating a borrow from Timer(L) to Timer(H), read the counter data after stopping the timer by writing "0" to PTRUN(L).

(4) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

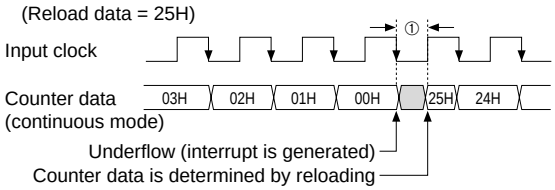


Fig. 13.10.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

14 WATCHDOG TIMER

14.1 Configuration of Watchdog Timer

The S1C88655 has a built-in watchdog timer that uses the OSC1 oscillation circuit as its clock source. The watchdog timer provides a mask option to select an overflow cycle or to disable the watchdog timer. The overflow signal can generate a non-maskable interrupt (NMI) or CPU reset, this is also selectable by mask option
Figure 14.1.1 shows the block diagram of the watchdog timer.

When the watchdog timer is used, it must be reset periodically with software. If the watchdog timer is not reset within the selected overflow period, it generates a non-maskable interrupt or CPU reset to the CPU.
Place a watchdog timer reset routine at a path where the CPU executes periodically, such as a main loop or timer interrupt handler routine, to detect program runaway as if the watchdog timer reset routine is not executed.
The watchdog timer is active in HALT mode. Therefore, if HALT state continues for longer than the selected period, the CPU starts exception processing. The watchdog timer stops in SLEEP mode.

Note: The overflow cycle has an error of less than128/fOSC1 seconds according to the watchdog timer reset timings.

14.2 Mask Option

The watchdog timer overflow cycle can be selected by mask option.

Watchdog timer overflow cycle
- ☐ Not use
- ☐ 32768 / fOSC1 (1-sec cycle when fOSC1 = 32 kHz)
- ☐ 65536 / fOSC1 (2-sec cycle when fOSC1 = 32 kHz)
- ☐ 131072 / fOSC1 (4-sec cycle when fOSC1 = 32 kHz)

When "Not use" is selected, the watchdog timer does not activate as no clock is supplied. In this case, the OSC1 oscillation circuit can be stopped by software control (see Chapter 8, "Oscillation Circuits").
When "32768 / fOSC1", "65536 / fOSC1", or "131072 / fOSC1" is selected, the watchdog overflow cycle is configured to 1 second, 2 seconds or 4 seconds, respectively. In this case, the OSC1 oscillation circuit cannot be stopped by software control since the OSC1 clock is always required.

Furthermore, mask option allows selection of either NMI or CPU reset to be generated by the watchdog timer overflow signal.

Watchdog timer overflow signal
- ☐ Interrupt (NMI)
- ☐ Reset

When "Interrupt (NMI)" is selected, the watchdog timer overflow signal will be sent to the $\overline{\text{NMI}}$ (level 4) input of the core CPU. This interrupt cannot be disabled and the $\overline{\text{NMI}}$ exception occurs in priority over other interrupts. See the "S1C88 Core CPU Manual" for more information on the $\overline{\text{NMI}}$ exception processing. The $\overline{\text{NMI}}$ exception processing vector address is set at 000004H.
The CPU reset signal resets only the CPU and does not initialize the peripheral circuit registers (see Chapter 5, "Initial Reset"). The reset exception processing vector address is set at 000000H.

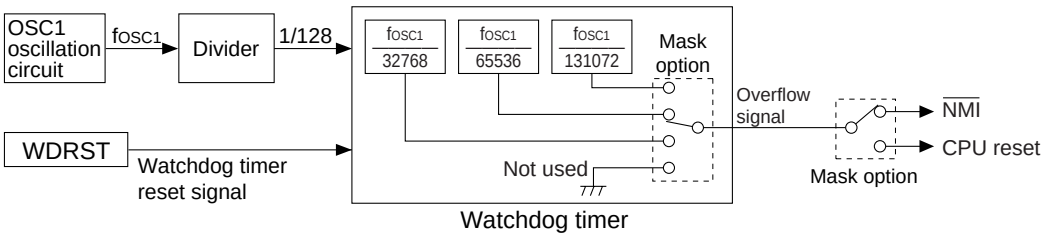


Fig. 14.1.1 Watchdog timer block diagram

14.3 Details of Control Register

Table 14.3.1 shows the control bit for the watchdog timer.

Table 14.3.1 Watchdog timer control bit

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF04	D7	FOUTON	FOUT output control	On	Off	0	R/W	
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	–	–	–	–	–	–	Constantly "0" when being read
	D2	–	–	–	–	–	–	
	D1	–	–	–	–	–	–	
	D0	WDRST	Watchdog timer reset	Reset	No operation	–	W	

FOUT2	FOUT1	FOUT0	Frequency
1	1	1	f_{OSC3} / 8
1	1	0	f_{OSC3} / 4
1	0	1	f_{OSC3} / 2
1	0	0	f_{OSC3} / 1
0	1	1	f_{OSC1} / 8
0	1	0	f_{OSC1} / 4
0	0	1	f_{OSC1} / 2
0	0	0	f_{OSC1} / 1

WDRST: 00FF04H•D0

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" to WDRST, the watchdog timer is reset, after which it is immediately restarted.
Writing "0" will mean no operation.
Since WDRST is for writing only, it is constantly set to "0" during readout.

14.4 Precautions

(1) When the watchdog timer is used, the software must reset it within the cycles selected by mask option.

(2) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

15 LCD DRIVER

15.1 Configuration of LCD Driver

The S1C88655 has a built-in dot matrix LCD driver that can drive an LCD panel with a maximum of 8,192 dots (128 segments × 64 commons). Figure 15.1.1 shows the configuration of the LCD driver and the drive power supply.

15.2 LCD Power Supply

The on-chip power supply circuit generates the LCD drive voltages V_{C1}–V_{C5}. See Chapter 4, "Power Supply" for controlling the power supply circuit. Note that the LCD power supply should be turned ON in the procedure shown below (in the reverse order to turn OFF).

1. Turn the clock source for the display timing generator ON. (OSC1 oscillation circuit or programmable timer 5)
2. Turn the display timing generator ON.
3. Turn the supply voltage booster circuit ON.
4. Turn the V_{C5} voltage generator ON.
5. Turn the $V_{C1–4}$ voltage generator ON.
6. Turn the LCD driver circuit ON.

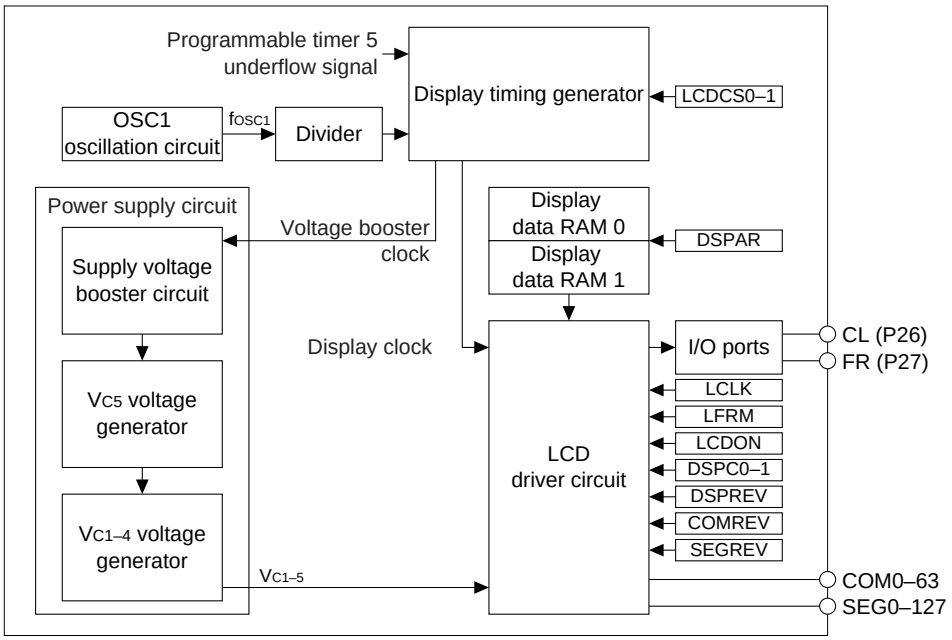


Fig. 15.1.1 Configuration of LCD driver

15.3 Display Timing Generator

15.3.1 Generating frame signal

This LCD driver has a display timing generator included to generate the LCD display clock and the supply voltage booster clock. The configuration of the circuit block is shown in Figure 15.3.1.1.
The display timing generator control register LCDCS0–LCDCS1 is used to turn the circuit ON / OFF and to select the source clock.

Table 15.3.1.1 Controlling display timing generator

LCDCS1	LCDCS0	Source clock (f_{LCD})
1	1	Programmable timer 5 underflow signal
1	0	f_{OSC1}/2
0	1	f_{OSC1}/1
0	0	OFF

Setting LCDCS0–LCDCS1 to "00" stops supplying the clock to the display timing generator, as a result the display timing generator stops outputting the voltage booster and display clocks. When a source clock (f_{LCD}) is selected, the display timing generator starts generating the voltage booster and display clocks.

The source clock can be selected from the OSC1 divided clocks (f_{OSC1} / 1, f_{OSC1} / 2) or the underflow signal of the programmable timer 5.
When the LCDON register is set to "1", the LCD driver divides the display clock to generate the CL and FR signals.
The display clock frequency f_{CL} and the frame frequency f_{FR} can be expressed by the following equation,

$f_{CL} = f_{LCD}/8$
$f_{FR} = f_{CL}/64 = f_{LCD}/512$

where f_{LCD} represents the frequency of the selected source clock.

The following shows the frame frequency when an OSC1 divided clock is selected as the source clock (when f_{OSC1} = 32.768 kHz):
64 Hz when f_{OSC1} / 1 is selected
32 Hz when f_{OSC1} / 2 is selected

Use of the programmable timer 5 allows fine adjustment of the frame frequency. See Section 13.8, "Setting Clock for LCD Driver Display Timing Generator", for setting the programmable timer.
f_{FR} represents a frame frequency and the LCD alternating signal (FR) cycle is two frames, so the FR signal cycle is f_{FR} / 2.
Setup f_{FR} to approximately 60 to 80 Hz as a guide.

The LCD driver circuit generates 1 / 64 duty LCD drive waveforms as shown in Figure 15.3.1.2 based on the timing generated by the display timing generator.

Note: The display timing generator also outputs the voltage booster clock to generate the LCD drive voltages. Therefore, be sure to select a source clock before turning the on-chip power supply circuit ON.

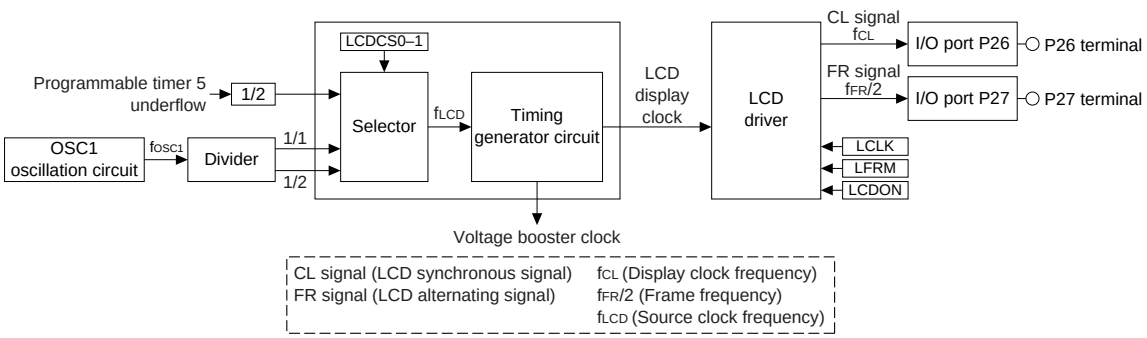


Fig. 15.3.1.1 Display timing generator

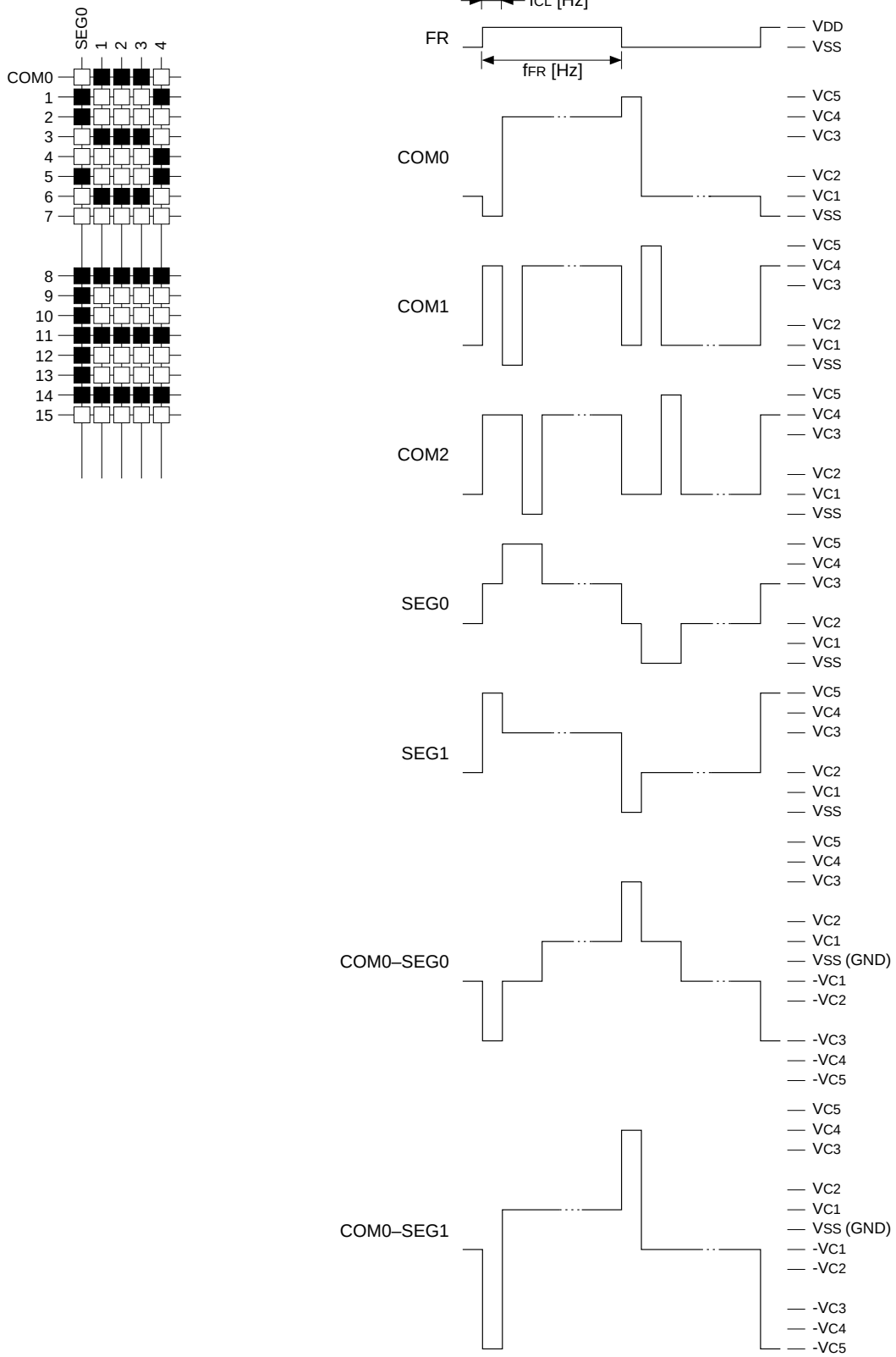


Fig. 15.3.1.2 LCD drive waveform (1/64 duty)

15.3.2 CL, FR signal outputs

The CL signal (LCD synchronous clock) and FR signal (LCD alternating signal) that are generated by the display timing generator can be output externally from the P26 and P27 port terminals, respectively. This makes it possible to monitor the f_{CL} and f_{FR} settings.
The LCLK register is used for output control of the CL signal (source clock selected using LCDCS). When LCLK is set to "1", the CL signal is output from the P26 terminal.
The LFRM register is used for output control of the FR signal. When LFRM is set to "1", the FR signal is output from the P27 terminal.
Figure 15.3.2.1 shows the output waveforms of the CL and FR signals.
Since these signals are generated asynchronously with the LCLK and LFRM registers, hazard may occur on the waveforms when the signal is turned ON / OFF using the register.

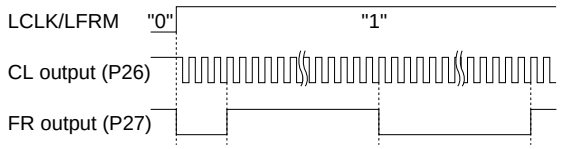


Fig. 15.3.2.1 CL and FR signal output waveforms

When LCLK or LFRM is set to "1", the data register (P26D, P27D) and I / O control register (IOC26, IOC27) of the I / O port P26 or P27 are not effective. When LCLK or LFRM is set to "0", the P26 or P27 terminal functions as an I / O port.

Note: The LCDON register must be set to "1" to generate the CL and FR signals.

15.4 Display Data RAM

The S1C88655 has a built-in 2K-byte display data RAM (8192 bits per screen × 2). The display data RAM is allocated to address E000H–EF7FH.

Two screen areas are reserved in the display data RAM and the area to be displayed can be selected using the display data RAM area select register DSPAR. When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.

The memory allocation for the SEG and COM terminals can be reversed using the SEGREV and COMREV registers, respectively.

The correspondence between the display data RAM bits and the common / segment terminals are shown in Figures 15.4.1 and 15.4.2.

When "1" is written to the display data RAM bit, the corresponding dot on the LCD panel goes ON and when "0" is written, it goes OFF. Since display data RAM is designed to permit reading / writing, it can be controlled in bit units by logical operation instructions and other means (read, modify and write instructions).
Even when external memory has expanded into the display data RAM area, this area is not released to external memory. Access to this area is always via display data RAM.

Address	0H								1H								···	EH								FH								COM	COM
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	···	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	(normal)*3	(reverse)*4
00E00xH	■	■	■	■		■	■	■				■	■	■			···																	0	63
00E01xH	■					■			■		■						···																	1	62
00E02xH	■					■			■		■						···																	2	61
00E03xH	■	■	■	■		■	■	■				■	■				···																	3	60
00E04xH	■					■								■			···																	4	59
00E05xH	■					■								■			···																	5	58
00E06xH	■	■	■	■		■				■	■	■					···																	6	57
00E07xH																	···																	7	56
00E08xH	■	■	■														···																	8	55
00E09xH	■			■													···																	9	54
00E0AxH	■			■													···																	10	53
00E0BxH	■	■	■														···																	11	52
00E0CxH	■																···																	12	51
00E0DxH	■																···																	13	50
00E0ExH	■																···																	14	49
00E0FxH																	···																	15	48
00E10xH		■	■	■													···																	16	47
00E11xH	■																···																	17	46
00E12xH	■																···																	18	45
00E13xH		■	■														···																	19	44
00E14xH				■													···																	20	43
00E15xH				■													···																	21	42
00E16xH	■	■	■														···																	22	41
00E17xH																	···																	23	40
00E18xH		■	■														···																	24	39
00E19xH	■			■													···																	25	38
00E1AxH	■			■													···																	26	37
00E1BxH	■			■													···																	27	36
00E1CxH	■			■													···																	28	35
00E1DxH	■			■													···																	29	34
00E1ExH		■	■														···																	30	33
00E1FxH																	···																	31	32
00E20xH	■			■													···																	32	31
00E21xH	■			■													···																	33	30
00E22xH	■	■		■													···																	34	29
00E23xH	■		■	■													···																	35	28
00E24xH	■			■													···																	36	27
00E25xH	■			■													···																	37	26
00E26xH	■			■													···																	38	25
00E27xH																	···																	39	24
00E28xH																	···																	40	23
00E29xH																	···																	41	22
00E2AxH																	···																	42	21
00E2BxH																	···																	43	20
00E2CxH																	···																	44	19
00E2DxH																	···																	45	18
00E2ExH																	···																	46	17
00E2FxH																	···																	47	16
00E30xH																	···																	48	15
00E31xH																	···																	49	14
00E32xH																	···																	50	13
00E33xH																	···																	51	12
00E34xH																	···																	52	11
00E35xH																	···																	53	10
00E36xH																	···																	54	9
00E37xH																	···																	55	8
00E38xH																	···																	56	7
00E39xH																	···																	57	6
00E3AxH																	···																	58	5
00E3BxH																	···																	59	4
00E3CxH																	···																	60	3
00E3DxH																	···																	61	2
00E3ExH																	···																	62	1
00E3FxH																	···																	63	0
SEG(normal)*1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	···	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127		
SEG(reverse)*2	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	···	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Display area 0

*1: SEGREV = "1" *2: SEGREV = "0" *3: COMREV = "1" *4: COMREV = "0"

Fig. 15.4.1 Display data RAM map (display area 0)

Address	0H								1H								···	EH								FH								COM	COM
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	···	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	(normal)*3	(reverse)*4
00E80xH	■	■	■	■		■	■	■				■	■	■			···																	0	63
00E81xH	■					■			■			■					···																	1	62
00E82xH	■					■			■			■					···																	2	61
00E83xH	■	■	■	■		■	■	■				■	■				···																	3	60
00E84xH	■					■								■			···																	4	59
00E85xH	■					■								■			···																	5	58
00E86xH	■	■	■	■		■						■	■	■			···																	6	57
00E87xH																	···																	7	56
00E88xH	■	■	■														···																	8	55
00E89xH	■			■													···																	9	54
00E8AxH	■			■													···																	10	53
00E8BxH	■	■	■														···																	11	52
00E8CxH	■																···																	12	51
00E8DxH	■																···																	13	50
00E8ExH	■																···																	14	49
00E8FxH																	···																	15	48
00E90xH		■	■	■													···																	16	47
00E91xH	■																···																	17	46
00E92xH	■																···																	18	45
00E93xH		■	■														···																	19	44
00E94xH				■													···																	20	43
00E95xH				■													···																	21	42
00E96xH	■	■	■														···																	22	41
00E97xH																	···																	23	40
00E98xH		■	■														···																	24	39
00E99xH	■			■													···																	25	38
00E9AxH	■			■													···																	26	37
00E9BxH	■			■													···																	27	36
00E9CxH	■			■													···																	28	35
00E9DxH	■			■													···																	29	34
00E9ExH		■	■														···																	30	33
00E9FxH																	···																	31	32
00EA0xH	■			■													···																	32	31
00EA1xH	■			■													···																	33	30
00EA2xH	■	■		■													···																	34	29
00EA3xH	■		■	■													···																	35	28
00EA4xH	■			■													···																	36	27
00EA5xH	■			■													···																	37	26
00EA6xH	■			■													···																	38	25
00EA7xH																	···																	39	24
00EA8xH																	···																	40	23
00EA9xH																	···																	41	22
00EAAxH																	···																	42	21
00EABxH																	···																	43	20
00EACxH																	···																	44	19
00EADxH																	···																	45	18
00EAExH																	···																	46	17
00EAFxH																	···																	47	16
00EB0xH																	···																	48	15
00EB1xH																	···																	49	14
00EB2xH																	···																	50	13
00EB3xH																	···																	51	12
00EB4xH																	···																	52	11
00EB5xH																	···																	53	10
00EB6xH																	···																	54	9
00EB7xH																	···																	55	8
00EB8xH																	···																	56	7
00EB9xH																	···																	57	6
00EBAxH																	···																	58	5
00EBBxH																	···																	59	4
00EBCxH																	···																	60	3
00EBDxH																	···																	61	2
00EBExH																	···																	62	1
00EBFxH																	···																	63	0
SEG(normal)*1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	···	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127		
SEG(reverse)*2	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	···	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Display area 1

*1: SEGREV = "1" *2: SEGREV = "0" *3: COMREV = "1" *4: COMREV = "0"

Fig. 15.4.2 Display data RAM map (display area 1)

15.5 Display Control

The display status by the built-in LCD driver and the contrast can be controlled with software.
The LCD display status can be selected by the LCD display control registers DSPC0 and DSPC1. Relationship between the register values and display statuses is shown in Table 15.5.1.

Table 15.5.1 LCD display control

DSPC1	DSPC0	LCD display
1	1	All dots ON
1	0	All dots OFF
0	1	Normal display
0	0	Display OFF

■ Display ON/OFF

When DSPC0–DSPC1 are set to "01", the LCD drive waveforms are output from the COM and SEG terminals. When DSPC0–DSPC1 are set to "00", the COM and SEG terminals output V_{SS} (GND), as a result the display turns OFF. At initial reset, display is turned OFF (DSPC0–DSPC1 = "00").

■ All dots ON

When DSPC0–DSPC1 are set to "11", all the dots on the LCD panel are lit with dynamic drive. In this case, all the SEG terminals output an ON waveform (V_{C5} or V_{SS}). This software control does not affect the contents of the display data RAM.

■ All dots OFF

When DSPC0–DSPC1 are set to "10", all the dots on the LCD panel go out with dynamic drive. In this case, all the SEG terminals output an OFF waveform (V_{C3} or V_{C2}) and all the COM terminals output an OFF waveform (V_{C4} and V_{C1}). This software control does not affect the contents of the display data RAM.

■ Reverse display

The display on the LCD panel in normal display mode (DSPC0–DSPC1 = "01") can be reversed (black pixels are turned white and vice versa) by setting the reverse display control register DSPREV to "0". Normal screen appears when DSPREV = "1". This software control does not affect the contents of the display data RAM. At initial reset, reverse display is disabled (DSPREV = "1").
If reverse display (DSPREV = "0") and all dots ON (DSPC0–DSPC1 = "11") are specified simultaneously, the display is reversed (all dots are lit).
If reverse display (DSPREV = "0") and all dots OFF (DSPC0–DSPC1 = "10") are specified simultaneously, the display is not reversed (all dots go out).

■ Contrast adjustment

The LCD contrast can be adjusted by controlling the V_{C5} voltage in the power supply circuit. See Chapter 4, "Power Supply", for controlling V_{C5} and Chapter 19, "Electrical Characteristics", for adjustable range of the LCD drive voltage.

15.6 Details of Control Registers

Table 15.6.1 shows the LCD driver control bits.

Table 15.6.1 LCD driver control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF08	D7	LCLK	CL output control	On	Off	0	R/W	
	D6	LFRM	FR output control	On	Off	0	R/W	
	D5	SEGREV	SEG output assignment control	Normal	Reverse	1	R/W	
	D4	COMREV	COM output assignment control	Normal	Reverse	1	R/W	
	D3	DSPAR	LCD display data RAM area selection	Display area 1	Display area 0	0	R/W	
	D2	DSPREV	Reverse display control	Normal	Reverse	1	R/W	
	D1	DSPC1	LCD display control DSPC1 DSPC0 Display 1 1 All dots on			0	R/W	
	D0	DSPC0	1 0 All dots off 0 1 Normal display 0 0 Display off			0	R/W	
00FF09	D7	–	–	–	–	–	–	"0" when being read
	D6	LCDON	LCD driver circuit On/Off control	On	Off	0	R/W	
	D5	LBIAS	LCD bias selection	1/9 bias	1/7 bias	1	R/W	
	D4	VCON	V_{C1-4} voltage generator On/Off control	On	Off	0	R/W	
	D3	VC5ON	V_{C5} voltage generator On/Off control	On	Off	0	R/W	
	D2	LBON	Supply voltage booster On/Off control	On	Off	0	R/W	
	D1	LCDCS1	Display timing generator control LCDCS1 LCDCS0 Source clock 1 1 P timer 5			0	R/W	
	D0	LCDCS0	1 0 $f_{OSC1}/2$ 0 1 $f_{OSC1}/1$ 0 0 Off			0	R/W	

LCDCS0, LCDCS1: 00FF09H•D0, D1

Controls the display timing generator.

Table 15.6.2 Controlling display timing generator

LCDCS1	LCDCS0	Source clock (f_{LCD})
1	1	Programmable timer 5 underflow signal
1	0	$f_{OSC1}/2$
0	1	$f_{OSC1}/1$
0	0	OFF

Setting LCDCS0–LCDCS1 to "00" stops supplying the clock to the display timing generator, as a result all the LCD output signals go to a V_{SS} level. When a source clock is selected, the display timing generator inputs the clock as the CL signal and starts generating the frame (FR) signal.
The display timing generator also outputs the voltage booster clock to generate the LCD drive voltages. Therefore, be sure to select a source clock before turning the on-chip power supply circuit ON.
At initial reset, LCDCS is set to "00" (OFF).

LCDON: 00FF09H•D6

Turns the LCD driver circuit ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When LCDON is set to "1", the LCD driver circuit activates and allows display controls. However, the LCD drive voltages must be supplied to the LCD driver circuit before setting LCDON to "1" (see Chapter 4, "Power Supply").
When LCDON is set to "0", the LCD driver circuit deactivates and display controls will be ineffective.
At initial reset, LCDON is set to "0" (OFF).

DSPC0, DSPC1: 00FF08H•D0, D1

Controls the LCD display.

Table 15.6.3 LCD display control

DSPC1	DSPC0	LCD display
1	1	All dots ON
1	0	All dots OFF
0	1	Normal display
0	0	Display OFF

The four settings mentioned above can be made without changing the display memory data.
At initial reset, this register is set to "00" (display OFF).

DSPREV: 00FF08H•D2

Reverses the display.

When "1" is written: Normal display
When "0" is written: Reverse display
Reading: Valid

When DSPREV is set to "0", the display on the LCD panel is reversed (black pixels are turned white and vice versa). Normal screen appears when DSPREV = "1". This software control does not affect the contents of the display data RAM.
This control is effective when normal display or all dots ON (DSPC0–DSPC1 = "01" or "11") is selected. When all dots OFF (DSPC0–DSPC1 = "10") is selected, display is not reversed (all dots go out).
At initial reset, DSPREV is set to "1" (normal display).

DSPAR: 00FF08H•D3

Selects the display area.

When "1" is written: Display area 1
When "0" is written: Display area 0
Reading: Valid

An area to be displayed is selected from two areas in the display data RAM.
When DSPAR is set to "0", display area 0 is selected and when set to "1", display area 1 is selected.
See Figures 15.4.1 and 15.4.2 for the display areas.
At initial reset, DSPAR is set to "0" (display area 0).

COMREV: 00FF08H•D4

Reverses the memory allocation for the COM terminals.

When "1" is written: Normal (ascending order)
When "0" is written: Reversed (descending order)
Reading: Valid

See Figures 15.4.1 and 15.4.2 for correspondence between the display data RAM and COM terminals.
At initial reset, COMREV is set to "1" (normal).

SEGREV: 00FF08H•D5

Reverses the memory allocation for the SEG terminals.

When "1" is written: Normal (ascending order)
When "0" is written: Reversed (descending order)
Reading: Valid

See Figures 15.4.1 and 15.4.2 for correspondence between the display data RAM and SEG terminals.
At initial reset, SEGREV is set to "1" (normal).

LFRM: 00FF08H•D6

Controls the FR signal output.

When "1" is written: FR signal output ON
When "0" is written: FR signal output OFF
Reading: Valid

When LFRM is set to "1", the FR signal is output from the P27 terminal. When LFRM is set to "0", the P27 terminal functions as an I/O port.
At initial reset, LFRM is set to "0" (FR signal output OFF).

LCLK: 00FF08H•D7

Controls the CL signal output.

When "1" is written: CL signal output ON
When "0" is written: CL signal output OFF
Reading: Valid

When LCLK is set to "1", the CL signal is output from the P26 terminal. When LCLK is set to "0", the P26 terminal functions as an I/O port.
At initial reset, LCLK is set to "0" (CL signal output OFF).

15.7 Precautions

(1) The display timing generator outputs the voltage booster clock to generate the LCD drive voltages. Therefore, be sure to select a source clock using the LCDCS register before turning the on-chip power supply circuit ON.

(2) Since the CL and FR signals are generated asynchronously with the LCLK and LFRM registers, hazard may occur on the waveforms when the signal is turned ON / OFF using the register.

(3) Be sure to set LCDCS0–1, LCDON, VCON, VC5ON and LBON to OFF before executing the SLP instruction. Also note that a hazard may occur if LCDCS0–1 is changed when LCLK and LFRM is ON.

16 SUPPLY VOLTAGE DETECTION (SVD) CIRCUIT

16.1 Configuration of SVD Circuit

The S1C88655 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON / OFF and the SVD criteria voltage setting can be done with software.
Figure 16.1.1 shows the configuration of the SVD circuit.

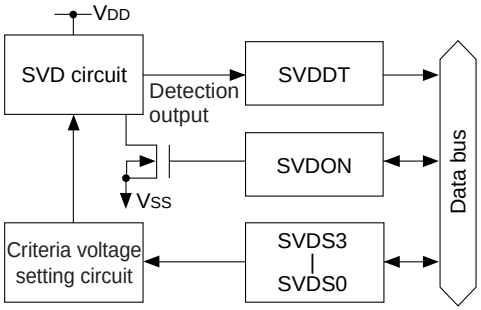


Fig. 16.1.1 Configuration of SVD circuit

16.2 SVD Operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 13 types shown in Table 16.2.1 by the SVDS3–SVDS0 registers.

Table 16.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	2.7
1	1	1	0	2.6
1	1	0	1	2.5
1	1	0	0	2.4
1	0	1	1	2.3
1	0	1	0	2.2
1	0	0	1	2.1
1	0	0	0	2.05
0	1	1	1	2.0
0	1	1	0	1.95
0	1	0	1	1.9
0	1	0	0	1.85
0	0	1	1	1.8
0	0	1	0	–
0	0	0	1	–
0	0	0	0	–

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.
To obtain a stable detection result, the SVD circuit must be ON for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

16.3 Details of Control Register

Table 16.3.1 shows the SVD circuit control bits.

Table 16.3.1 SVD circuit control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF0C	D7	–	–	–	–	–	R	Constantly "0" when
	D6	–	–	–	–	–	R	being read
	D5	SVDDT	SVD detection data	Low	Normal	0	R	
	D4	SVDON	SVD circuit On/Off	On	Off	0	R/W	
	D3	SVDS3	SVD criteria voltage setting			0	R/W	
	D2	SVDS2	SVDS3 SVDS2 SVDS1 SVDS0 Voltage (V) 1 1 1 1 2.7 1 1 1 0 2.6			0	R/W	
	D1	SVDS1	1 1 0 1 2.5			0	R/W	
	D0	SVDS0	: : : : : 0 0 1 1 1.8			0	R/W	

SVDS3–SVDS0: 00FF0CH•D3–D0

Criteria voltage for SVD is set as shown in Table 16.2.1.
At initial reset, this register is set to "0".

SVDON: 00FF0CH•D4

Controls the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a supply voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least 500 µsec.
At initial reset, this register is set to "0".

SVDDT: 00FF0CH•D5

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

16.4 Precautions

(1) To obtain a stable detection result, the SVD circuit must be ON for at least 500 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 500 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

17 SUMMARY OF NOTES

17.1 Notes for Low Current Consumption

The S1C88655 can turn circuits, which consume a large amount of power, ON or OFF by control registers.
You can reduce power consumption by creating a program that operates the minimum necessary circuits using these control registers.

Next, which circuit systems' operation can be controlled and their control registers (instructions) are explained. You should refer to these when programming.

See Chapter 19, "Electrical Characteristics", for the current consumption.

Refer to "Precautions" in each peripheral section for precautions of each peripheral circuit.

Table 17.1.1 Circuit systems and control registers

Circuit type	Control register (Instruction)	Status at time of initial resetting
CPU	HALT and SLP instructions	Operation status
Oscillation circuit	CLKCHG	OSC3 clock (CLKCHG = "1")
	SOSC3	OSC3 oscillation ON (SOSC3 = "1")
	SOSC1	OSC1 oscillation ON (SOSC1 = "1")
Power supply circuit	LBON	Supply voltage booster circuit OFF (LBON = "0")
	VC5ON	V_{C5} voltage generator OFF (VC5ON = "0")
	VCON	$V_{C1–4}$ voltage generator ON (VCON = "1")
LCD driver circuit	LCDON	LCD driver circuit OFF (LCDON = "0")
	DSPC0–1	Display OFF (DSPC0–1 = "0")
SVD circuit	SVDON	OFF status (SVDON = "0")

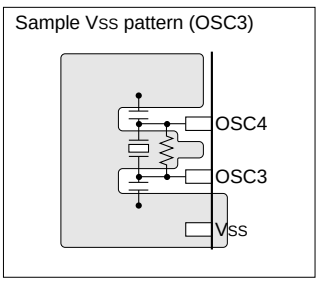
17.2 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 / OSC3 and VDD, please keep enough distance between OSC1 / OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

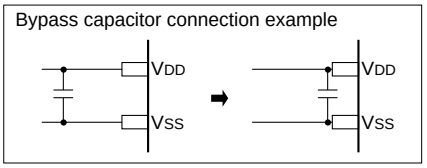
- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor of the $\overline{\text{RESET}}$ terminal is used, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

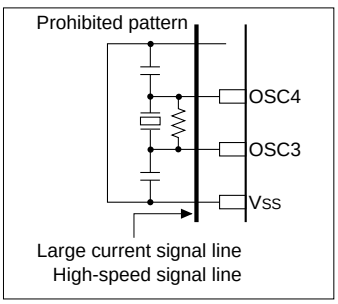
  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1 and VD2 terminals, such as capacitors and resistors, should be connected in the shortest line.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

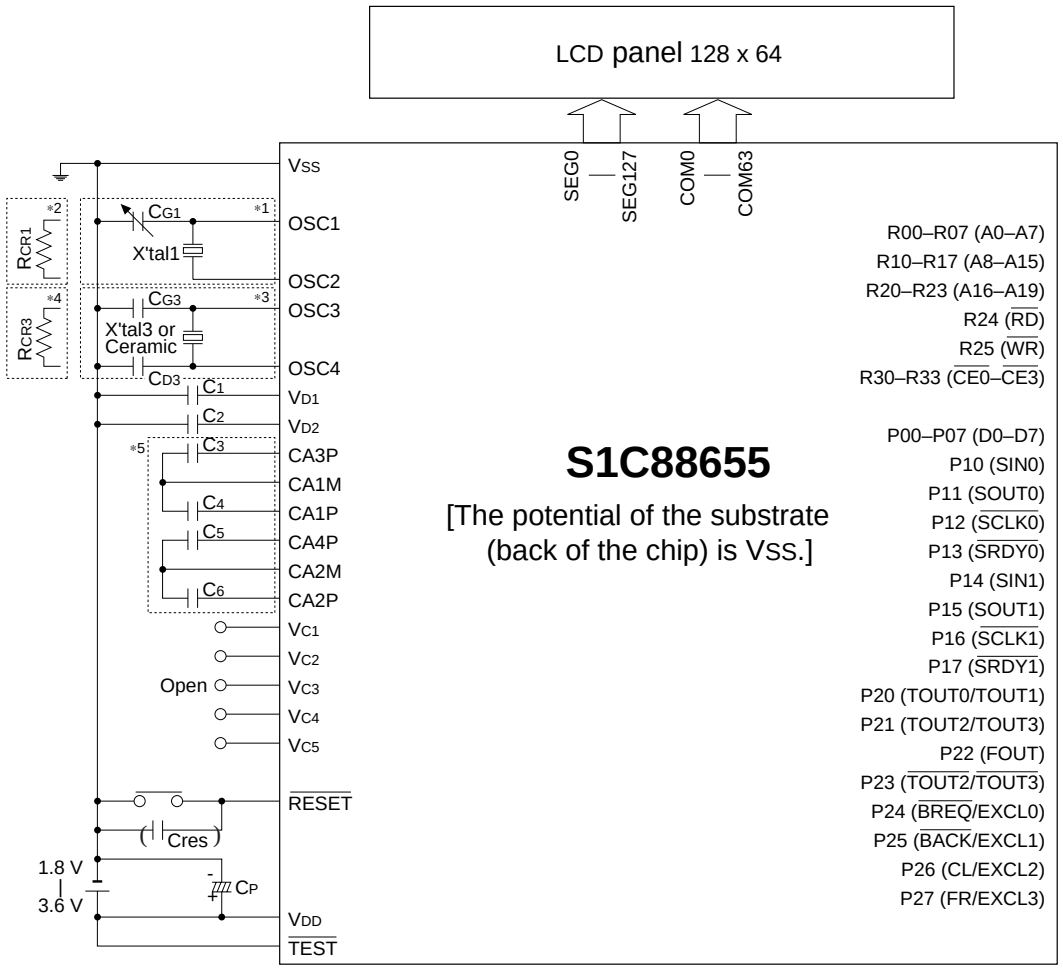
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

18 BASIC EXTERNAL WIRING DIAGRAM



∗1: OSC1 = Crystal oscillation ∗2: OSC1 = CR oscillation
∗3: OSC3 = Crystal or Ceramic oscillation ∗4: OSC3 = CR oscillation
∗5: Example for $V_{D2} = 5 \times V_{DD}$ ($V_{D2} > V_{C5}$)
The external circuit configuration depends on the supply voltage and LCD drive voltage values.

Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz
C_{G1}	Trimmer capacitor	0–25 pF
R_{CR1}	Resistor for CR oscillation	1.5 MΩ
X'tal3	Crystal oscillator	4 MHz
Ceramic	Ceramic oscillator	4 MHz
C_{G3}	Gate capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
C_{D3}	Drain capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)

Symbol	Name	Recommended value
R_{CR3}	Resistor for CR oscillation	39 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{D2}	1.0–4.7 µF
C_3–C_6	Booster capacitor	1.0–4.7 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF (Not required when the reset voltage detection circuit is used.)

Note: The above table is simply an example, and is not guaranteed to work.

19 ELECTRICAL CHARACTERISTICS

19.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +4.7	V	
Liquid crystal power voltage	V_{D2}, V_{C5}		-0.3 to +24.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	1
Operating temperature	Topr		-20 to +70	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10 sec (lead section)	–	

Note) 1 In case of plastic package.

19.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	V_{DD}		1.8		3.6	V	
Operating frequency	f_{OSC1}	Crystal/CR oscillation	30	32.768	200	kHz	
	f_{OSC3}	CR oscillation	0.2		2.2	MHz	
		Crystal/ceramic oscillation	0.2		8.2	MHz	
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{D2} and V_{SS}	C_2		1.0		4.7	µF	1
Capacitor between CA3P and CA1M	C_3		1.0		4.7	µF	1
Capacitor between CA1P and CA1M	C_4		1.0		4.7	µF	1
Capacitor between CA4P and CA2M	C_5		1.0		4.7	µF	1
Capacitor between CA2P and CA2M	C_6		1.0		4.7	µF	1

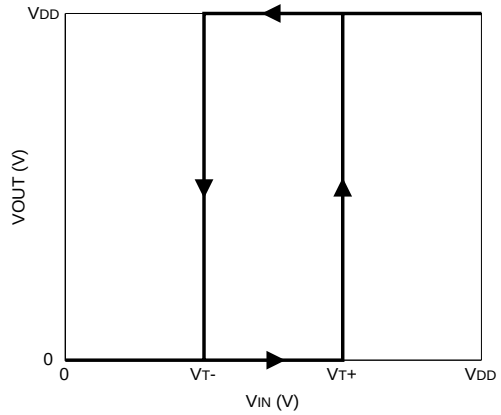
Note) 1 When LCD drive power is not used, the capacitor is not necessary.
Configuration of C_3–C_6 is different depending on the boosting ratio.

19.3 DC Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage	V_{IH}	Pxx	0.8V_{DD}		V_{DD}	V	1
Low level input voltage	V_{IL}	Pxx	0		0.2V_{DD}	V	1
High level schmitt input voltage (1)	V_{T1+}	$\overline{RESET}$, MCU/$\overline{MPU}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage (1)	V_{T1-}	$\overline{RESET}$, MCU/$\overline{MPU}$	0.1V_{DD}		0.5V_{DD}	V	
High level schmitt input voltage (2)	V_{T2+}	Pxx	0.5V_{DD}		0.9V_{DD}	V	2
Low level schmitt input voltage (2)	V_{T2-}	Pxx	0.1V_{DD}		0.5V_{DD}	V	2
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9 V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1 V_{DD}	0.5			mA	
Input leak current	I_{LI}	Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	100		500	kΩ	3
Input terminal capacitance	C_{IN}	Pxx V_{IN} = 0 V, f = 1 MHz, Ta = 25°C			15	pF	

Note) 1 When CMOS level is selected by mask option.
2 When CMOS Schmitt level is selected by mask option.
3 When addition of pull-up resistor is selected by mask option.



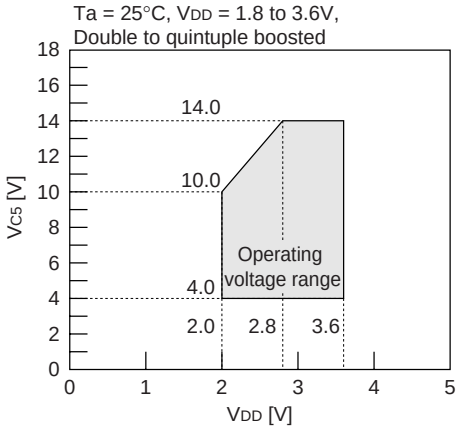
19.4 Analog Circuit Characteristics

■ LCD drive circuit

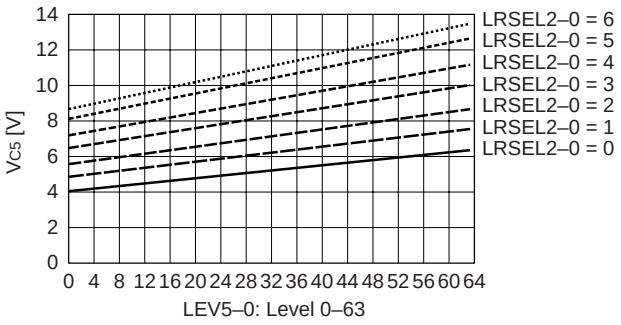
Unless otherwise specified: V_{DD} = 2.0 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Voltage booster circuit operating voltage	V_{DD}	Double boosted	2.0	–	3.6	V	
		Triple boosted	2.0	–	3.6	V	
		Quadruple boosted	2.0	–	3.6	V	
		Quintuple boosted	2.0	–	3.6	V	
V_{D2} voltage range	V_{D2}		–	–	18	V	
$V_{C1–5}$ voltage range (for 1/9 bias)	V_{C5}	Set using LRSEL0–2 and LEV0–5.	Typ.×0.93	4.0–14.0	Typ.×1.07	V	1
	V_{C4}		–	0.889×V_{C5}	–	V	
	V_{C3}		–	0.778×V_{C5}	–	V	
	V_{C2}		–	0.222×V_{C5}	–	V	
	V_{C1}		–	0.111×V_{C5}	–	V	
$V_{C1–5}$ voltage range (for 1/7 bias)	V_{C5}	Set using LRSEL0–2 and LEV0–5.	Typ.×0.93	4.0–14.0	Typ.×1.07	V	1
	V_{C4}		–	0.857×V_{C5}	–	V	
	V_{C3}		–	0.714×V_{C5}	–	V	
	V_{C2}		–	0.286×V_{C5}	–	V	
	V_{C1}		–	0.143×V_{C5}	–	V	

Note) 1 See the plot below for the V_{C5} voltage adjustable range.



Operating voltage range



V_{C5} output voltage adjustment range (Typ.)

■ SVD circuit

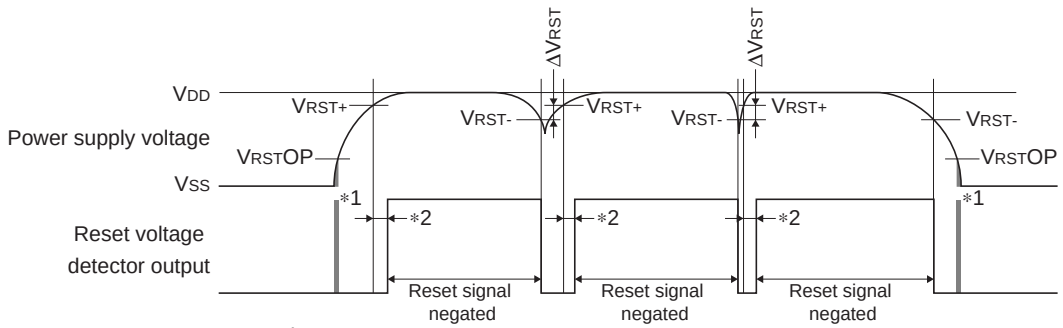
Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	SVDS0–3 = "0"		–		V	
		SVDS0–3 = "1"		–		V	
		SVDS0–3 = "2"		–		V	
		SVDS0–3 = "3"		1.8		V	
		SVDS0–3 = "4"		1.85		V	
		SVDS0–3 = "5"		1.9		V	
		SVDS0–3 = "6"		1.95		V	
		SVDS0–3 = "7"		2.0		V	
		SVDS0–3 = "8"		2.05		V	
		SVDS0–3 = "9"	Typ.×0.91	2.1	Typ.×1.09	V	
		SVDS0–3 = "10"		2.2		V	
		SVDS0–3 = "11"		2.3		V	
		SVDS0–3 = "12"		2.4		V	
		SVDS0–3 = "13"		2.5		V	
		SVDS0–3 = "14"		2.6		V	
		SVDS0–3 = "15"		2.7		V	
SVD circuit response time	t_{SVD}				500	µs	

■ RVD circuit

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Reset detection voltage	V_{RST+}	V_{DD} = L → H (Reset release level)	Typ.×0.91	1.3	Typ.×1.09	V	
	V_{RST-}	V_{DD} = H → L (Reset level)		1.25		V	
Hysteresis voltage	ΔV_{RST}	V_{DD} = L → H → L	20	50	80	mV	
Operation limit voltage	V_{RSTOP}			0.65	1.0	V	



∗1 Unsteady reset range

∗2 Reset hold range (Reset status is held for a certain time after the power supply voltage exceeds the reset release level.)

19.5 Power Current Consumption

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, C_1 = 0.1 µF, C_2–C_6 = 1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Current consumption in SLEEP mode	I_{SLP}	OSC1 = OFF, OSC3 = OFF		0.7	1.5	µA	
Current consumption in HALT mode	I_{HALT1}	OSC1 = 32 kHz Crystal, OSC3 = OFF		2	4	µA	
	I_{HALT2}	OSC1 = 32 kHz CR, OSC3 = OFF		7	11	µA	
	I_{HALT3}	OSC1 = OFF, OSC3 = 8 MHz Ceramic		150	300	µA	
	I_{HALT4}	OSC1 = OFF, OSC3 = 2 MHz CR		200	400	µA	
Current consumption during execution	I_{EXE1}	OSC1 = 32 kHz Crystal, OSC3 = OFF		5	8	µA	
	I_{EXE2}	OSC1 = 32 kHz CR, OSC3 = OFF		10	15	µA	
	I_{EXE3}	OSC1 = OFF, OSC3 = 8 MHz Ceramic		800	1200	µA	
	I_{EXE4}	OSC1 = OFF, OSC3 = 2 MHz CR		350	550	µA	
RVD circuit current	I_{RVD}	V_{DD} = 3.6 V		1.5	3	µA	1
SVD circuit current	I_{SVD}	V_{DD} = 3.6 V		5	10	µA	2
LCD driver circuit current	I_{LCD1}	V_{DD} = 2.0 V, Quintuple boosted, V_{C5} = 8 V, White screen displayed		80	120	µA	3
	I_{LCD2}	V_{DD} = 2.0 V, Quintuple boosted, V_{C5} = 8 V, Checker pattern displayed		200	300	µA	3
	I_{LCD3}	V_{DD} = 3.0 V, Triple boosted, V_{C5} = 8 V, White screen displayed		50	75	µA	3
	I_{LCD4}	V_{DD} = 3.0 V, Triple boosted, V_{C5} = 8 V, Checker pattern displayed		120	180	µA	3

Note) 1 This value is added to the current consumption in SLEEP mode/in HALT mode/during execution when the reset voltage detector is selected by mask option.

2 This value is added to the current consumption in SLEEP mode/in HALT mode/during execution when the SVD circuit is active.
SVDON = "1", SVDS0–3 = "Fh"

3 This value is added to the current consumption in SLEEP mode/in HALT mode/during execution when the LCD driver circuit is active.
LCDCS0–1 = "01", LBON = "1", VC5ON = "1", LBIAS = "1", DSPC0–1 = "01", LRSEL0–2 and LEV0–5 = arbitrarily

19.6 AC Characteristics

■ Operating range

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency	f_{OSC1}	V_{DD} = 1.8 to 3.6 V	30	32.768	200	kHz	
	f_{OSC3}		0.2		8.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	10	61	67	µs	
		2-cycle instruction	20	122	133	µs	
		3-cycle instruction	30	183	200	µs	
		4-cycle instruction	40	244	267	µs	
		5-cycle instruction	50	305	333	µs	
		6-cycle instruction	60	366	400	µs	
Instruction execution time (during operation with OSC3 clock)	tcy	1-cycle instruction	0.24		10	µs	
		2-cycle instruction	0.49		20	µs	
		3-cycle instruction	0.73		30	µs	
		4-cycle instruction	0.98		40	µs	
		5-cycle instruction	1.22		50	µs	
		6-cycle instruction	1.46		60	µs	

■ External memory access

• Read cycle

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	tc+tl-50+n•tc/2			ns	1
Address hold time in read cycle	trah	th-40			ns	
Read signal pulse width	trp	tc-10+n•tc/2			ns	1
Data input set-up time in read cycle	trds	150			ns	
Data input hold time in read cycle	trdh	0			ns	

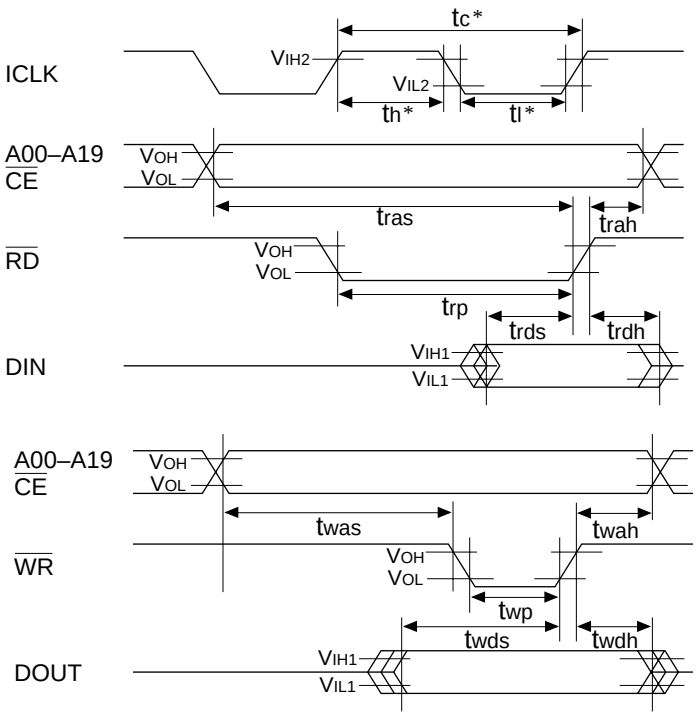
Note) 1 Substitute the number of states for wait insertion in n.

• Write cycle

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	tc-90			ns	
Address hold time in write cycle	twah	th-40			ns	
Write signal pulse width	twp	tl-20+n•tc/2			ns	1
Data output set-up time in write cycle	twds	tc-90+n•tc/2			ns	1
Data output hold time in write cycle	twdh	th-40		th+40	ns	

Note) 1 Substitute the number of states for wait insertion in n.



* In the case of crystal oscillation and ceramic oscillation: th = 0.5tc ± 0.05tc, tl = tc - th (1/tc: oscillation frequency)

* In the case of CR oscillation: th = 0.5tc ± 0.10tc, tl = tc - th (1/tc: oscillation frequency)

■ Serial interface

• Clock synchronous master mode

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	ns	
Receiving data input set-up time	tsms	250			ns	
Receiving data input hold time	tsmh	100			ns	

• Clock synchronous slave mode

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	ns	
Receiving data input set-up time	tsss	100			ns	
Receiving data input hold time	tssh	100			ns	

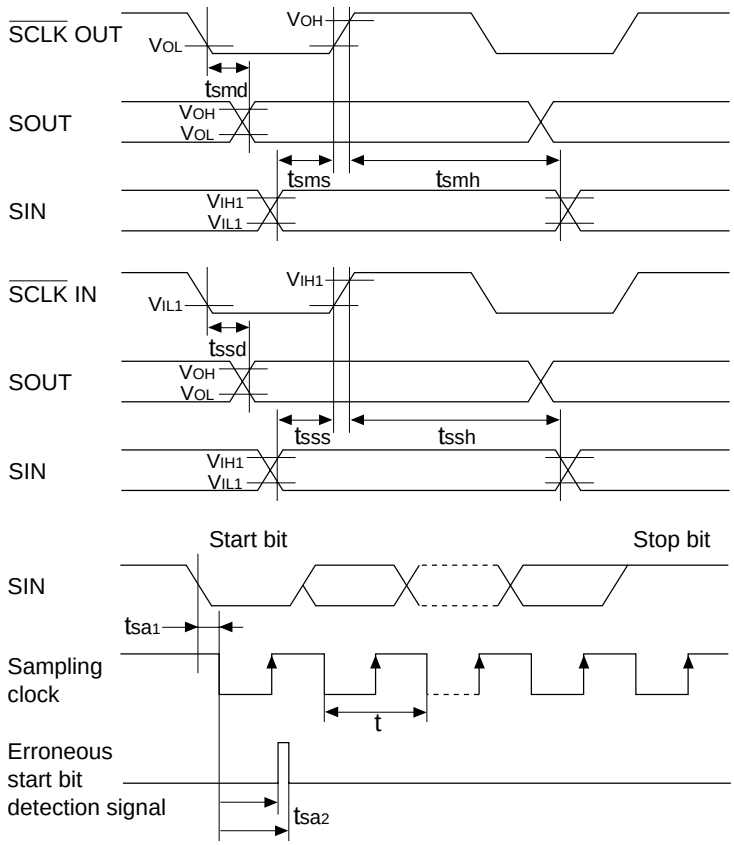
• Asynchronous system

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	s	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	s	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

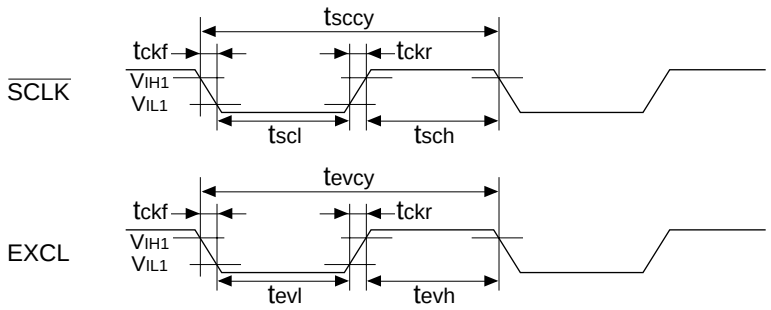


■ Input clock

• $\overline{\text{SCLK}}$, EXCL input clock

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

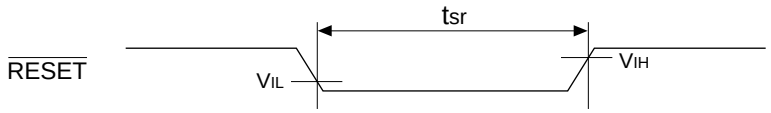
Item		Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	tsccy	2			µs	
	"H" pulse width	tsch	1			µs	
	"L" pulse width	tscl	1			µs	
EXCL input clock time (with noise rejector)	Cycle time	tevcy	64/f_{OSC1}			s	
	"H" pulse width	tevh	32/f_{OSC1}			s	
	"L" pulse width	tevl	32/f_{OSC1}			s	
EXCL input clock time (without noise rejector)	Cycle time	tevcy	2			µs	
	"H" pulse width	tevh	1			µs	
	"L" pulse width	tevl	1			µs	
Input clock rising time		tckr			25	ns	
Input clock falling time		tckf			25	ns	



• $\overline{\text{RESET}}$ input clock

Condition: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.5V_{DD}, V_{IL} = 0.1V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µs	



19.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or crystal oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

■ OSC1 (Crystal)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = C-002RX (R_1 = 30 kΩ (Typ.), C_L = 12.5 pF)*, C_{G1} = 25 pF, C_{D1} = Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	s	
External gate capacitance	C_{G1}	Including board capacitance	0		25	pF	
Built-in drain capacitance	C_{D1}	In case of the chip		10		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 0 to 25 pF	25			ppm	

* C-002RX Made by EPSON TOYOCOM

■ OSC1 (CR)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

■ OSC3 (Crystal)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = CA-301*, R_F = 1 MΩ, C_{G3} = C_{D3} = 15 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				10	ms	1

* CA-301 Made by EPSON TOYOCOM

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G3} and C_{D3}.

■ OSC3 (Ceramic)

Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C,
Ceramic oscillator = KBR-4.0MSB/KBR-8.0MSB*, R_F = 1 MΩ, C_{G3} = C_{D3} = 30 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				1	ms	1

* KBR-4.0MSB/KBR-8.0MSB Made by Kyocera

Note) 1 The ceramic oscillation start time changes by the ceramic oscillator to be used, C_{G3} and C_{D3}.

■ OSC3 (CR)

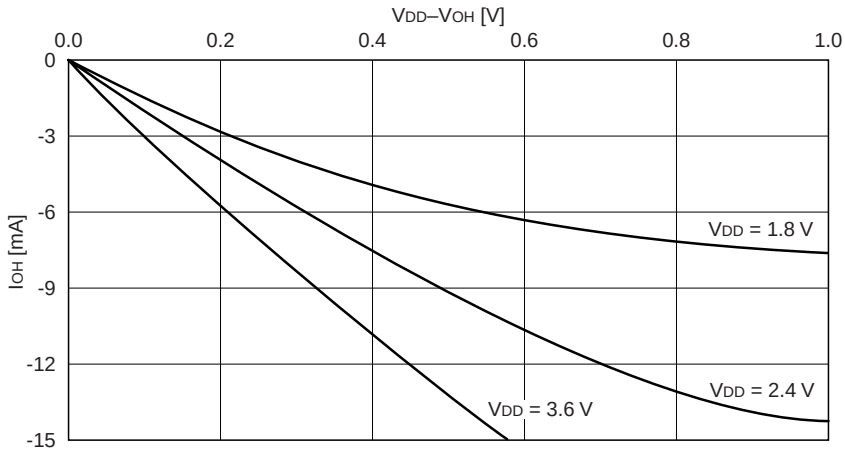
Unless otherwise specified: V_{DD} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

19.8 Characteristics Curves (reference value)

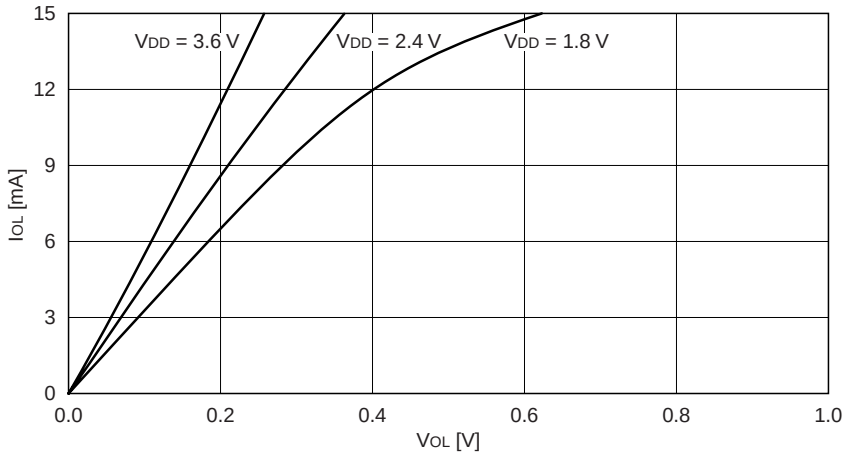
■ High level output current characteristic

Ta = 70°C, Max. value



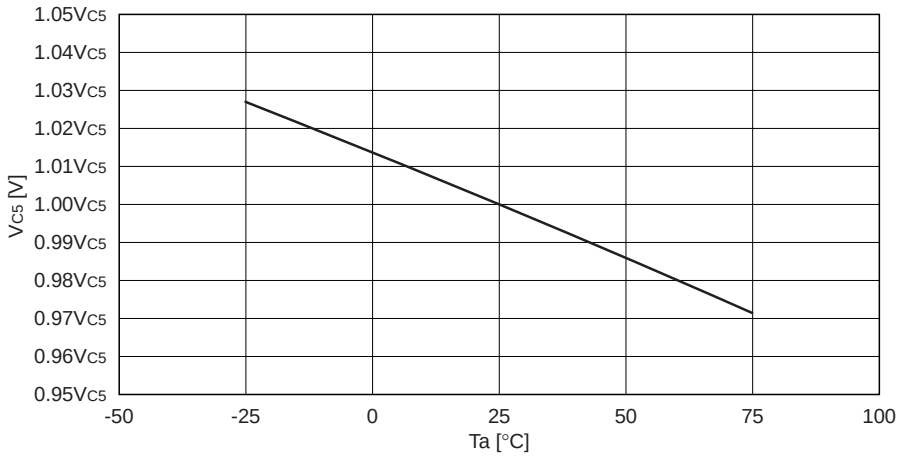
■ Low level output current characteristic

Ta = 70°C, Min. value

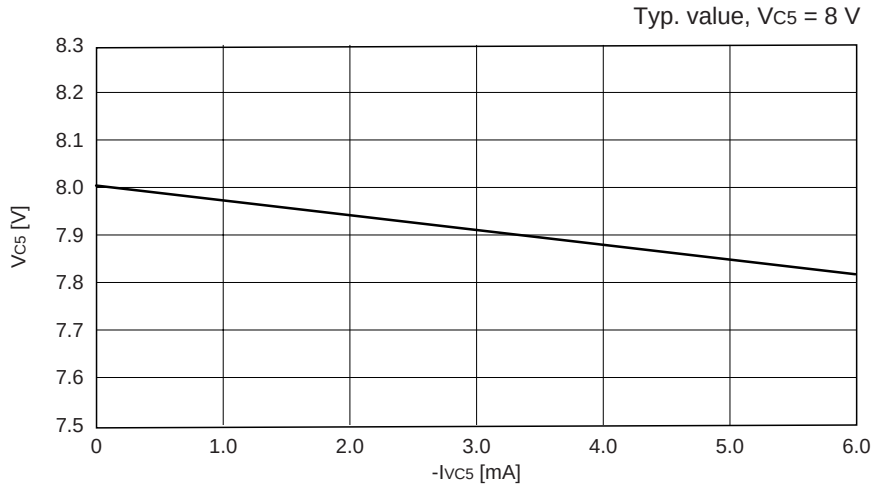


■ VC5 voltage - temperature characteristic

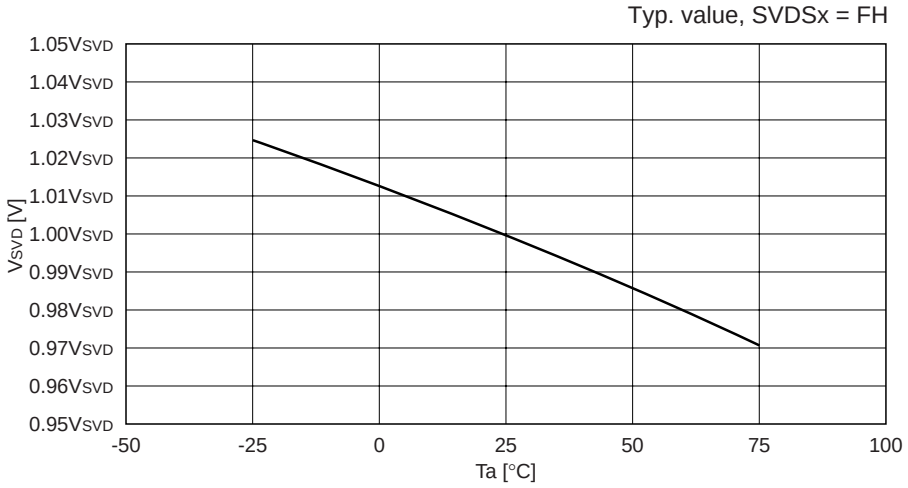
Typ. value, VC5 = 8 V



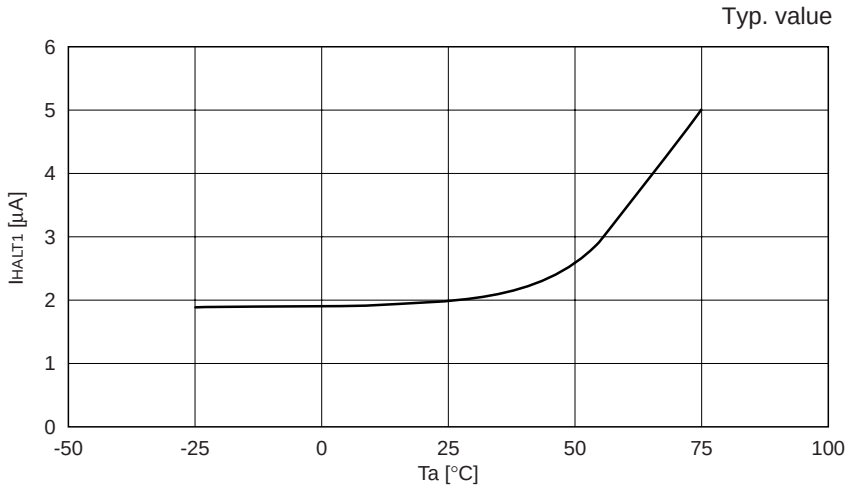
■ V_{C5} voltage - load characteristic



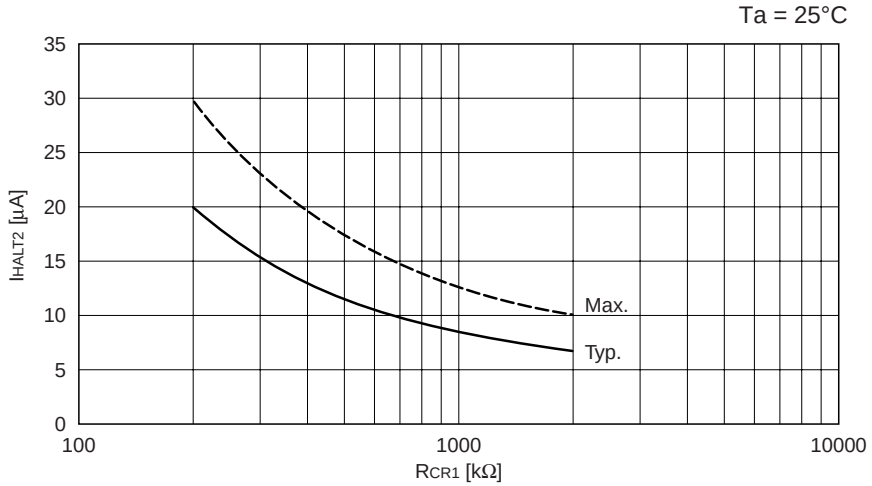
■ SVD voltage - temperature characteristic



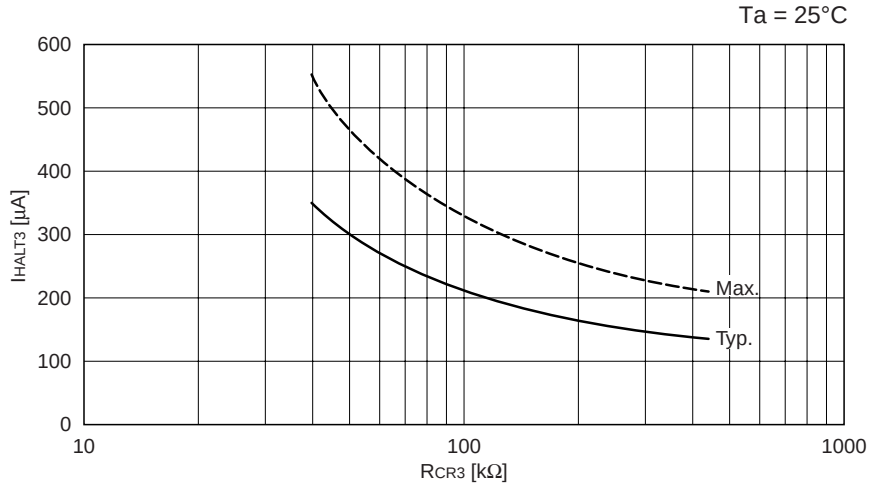
■ In HALT status current consumption - temperature characteristic (During operation with OSC1) <Crystal oscillation, f_{OSC1} = 32.768 kHz>



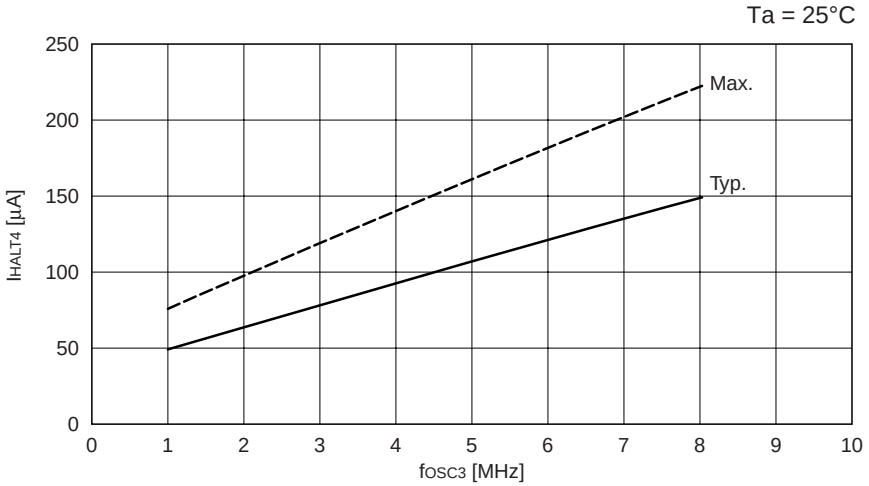
■ **In HALT status current consumption - resistance characteristic (During operation with OSC1) <CR oscillation>**



■ **In HALT status current consumption - resistance characteristic (During operation with OSC3) <CR oscillation>**

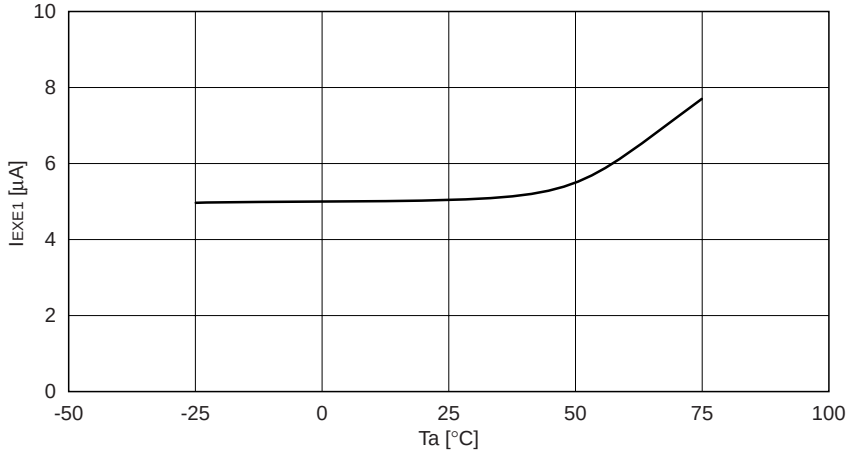


■ **In HALT status current consumption - frequency characteristic (During operation with OSC3) <Crystal oscillation/Ceramic oscillation>**



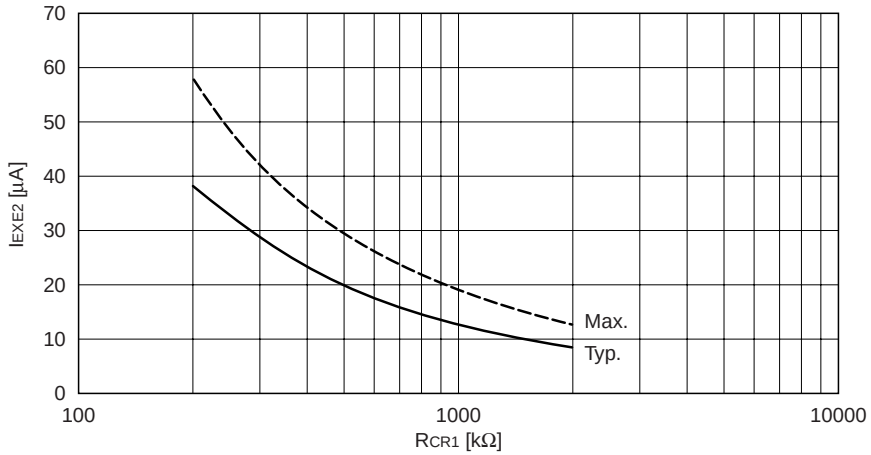
■ **In executed status current consumption - temperature characteristic (During operation with OSC1) <Crystal oscillation, f_{OSC1} = 32.768 kHz>**

Typ. value



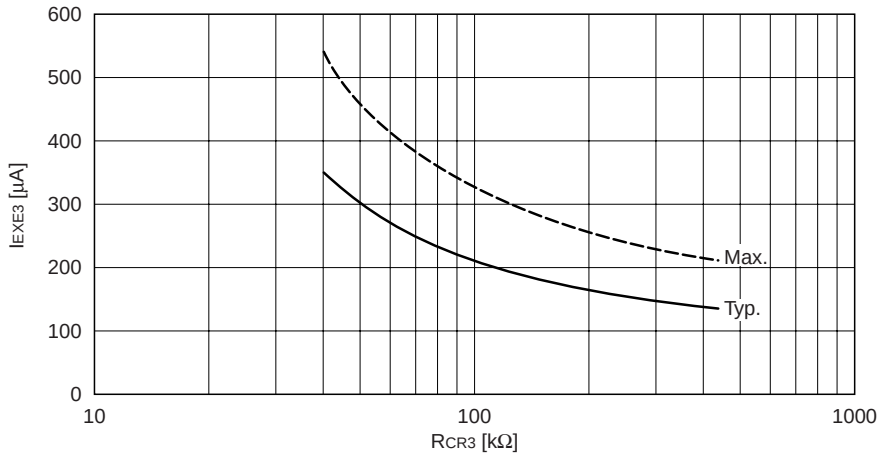
■ **In executed status current consumption - resistance characteristic (During operation with OSC1) <CR oscillation>**

Ta = 25°C



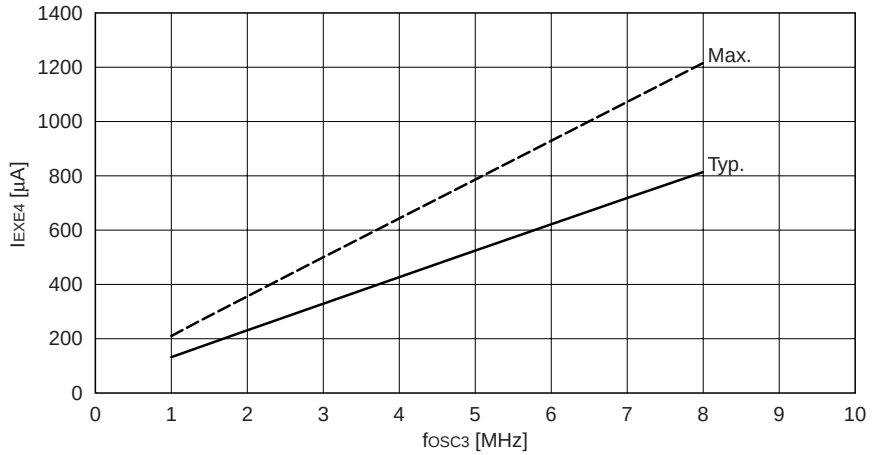
■ **In executed status current consumption - resistance characteristic (During operation with OSC3) <CR oscillation>**

Ta = 25°C



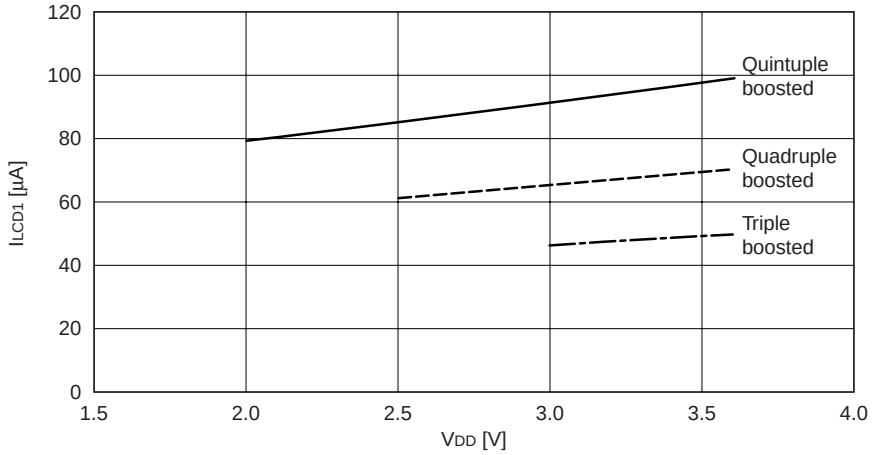
■ In executed status current consumption - frequency characteristic (During operation with OSC3) <Crystal oscillation/Ceramic oscillation>

Ta = 25°C

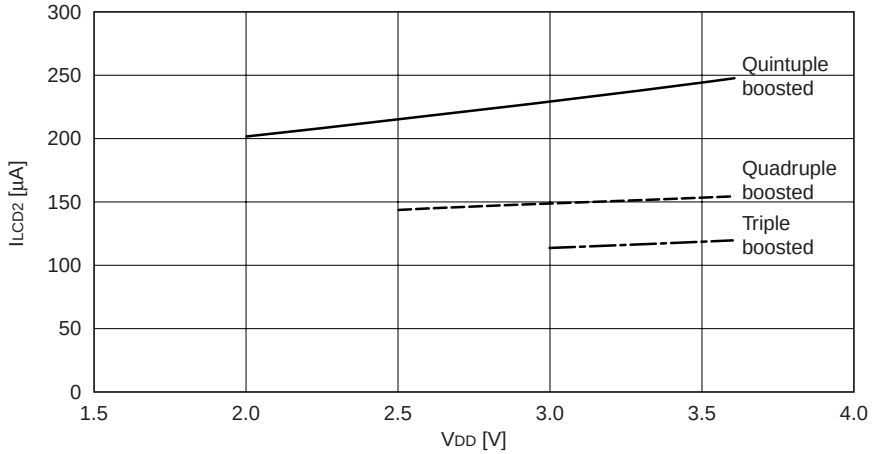


■ LCD driver circuit current - power voltage characteristic

Ta = 25°C, Typ. value, V_{C5} = 8 V, white screen displayed



Ta = 25°C, Typ. value, V_{C5} = 8 V, checker pattern displayed

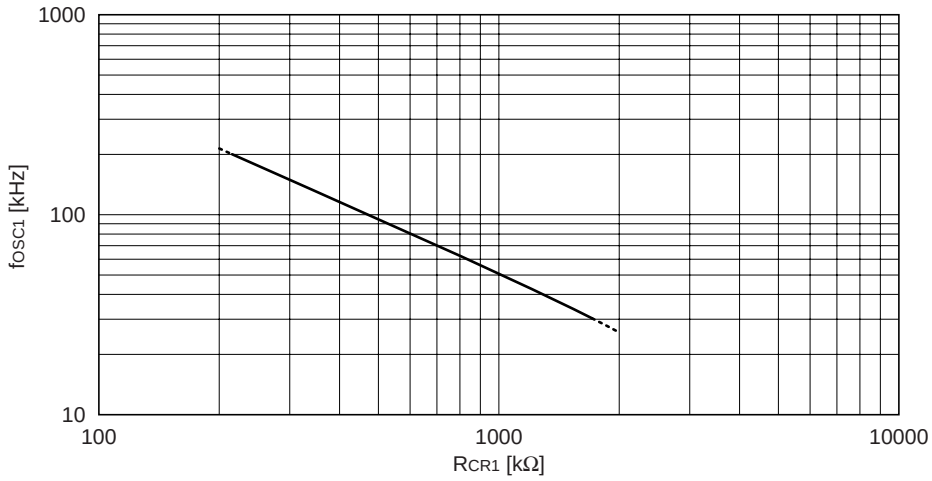


■ CR oscillation frequency characteristic

Note: Oscillation frequency changes depending on the conditions (components used, board pattern, etc.). In particular, the OSC3 oscillation frequency changes extensively depending on the product form and board capacitance. Therefore, select the resistance value after evaluating the actual product. (The OSC3 resistance value should be set to $R_{CR3} \geq 15$ kΩ.)

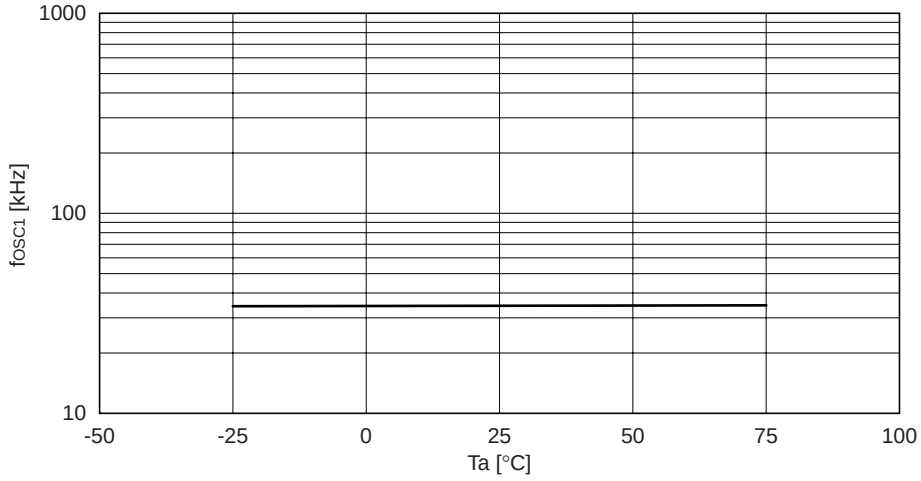
• OSC1 oscillation frequency - resistor characteristic

Ta = 25°C, Typ. value



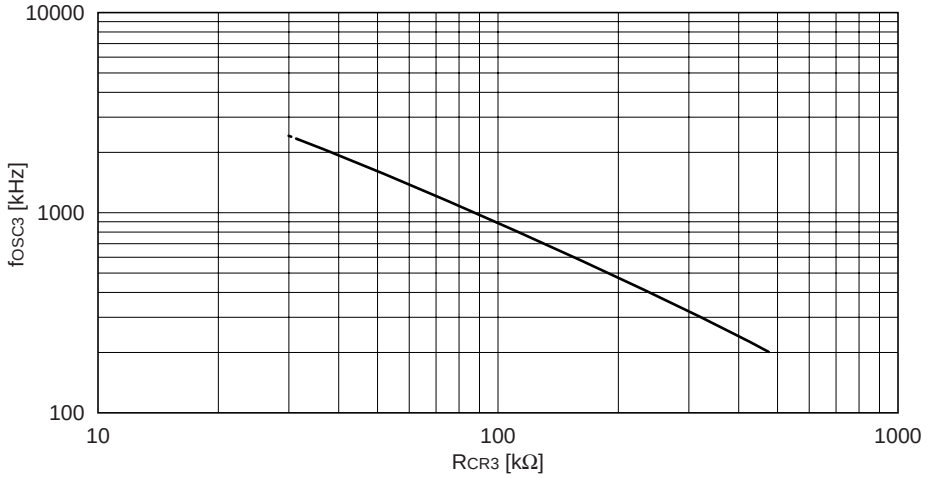
• OSC1 oscillation frequenc - temperature characteristic

Typ. value, R_{CR1} = 1500 kΩ



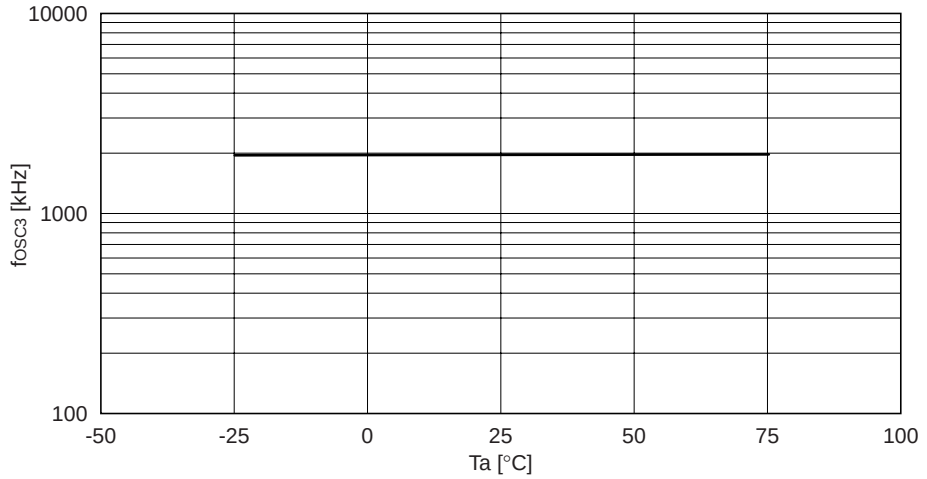
- **OSC3 oscillation frequency - resistor characteristic**

Ta = 25°C, Typ. value



- **OSC3 oscillation frequenc - temperature characteristic**

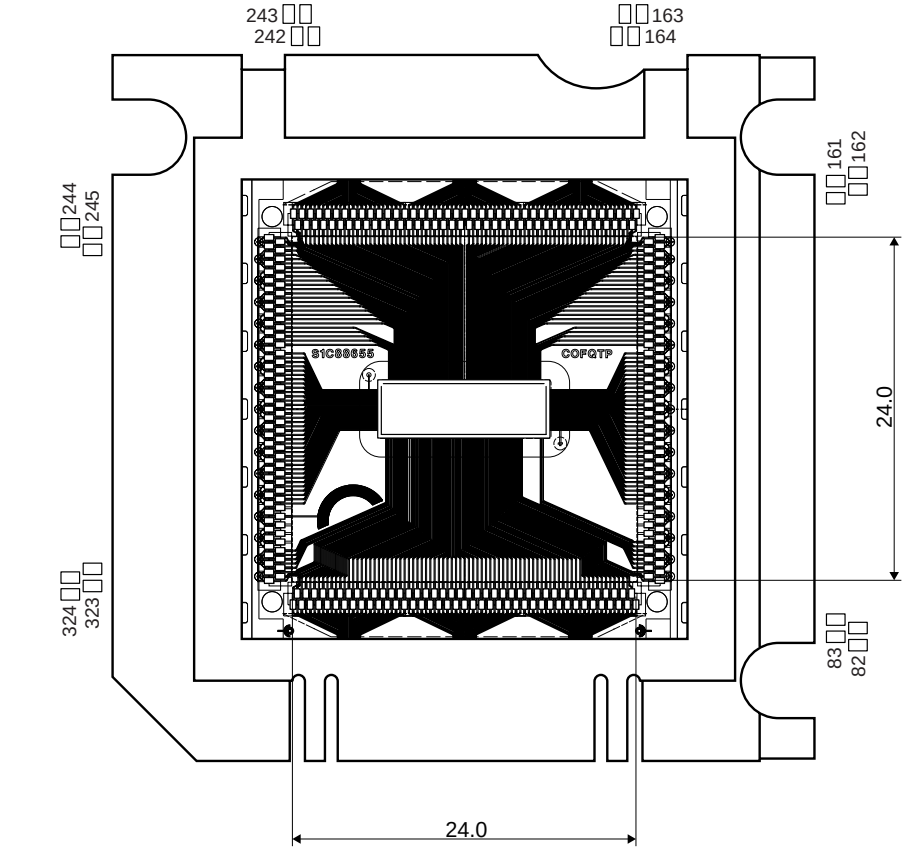
Typ. value, R_{CR3} = 39 kΩ

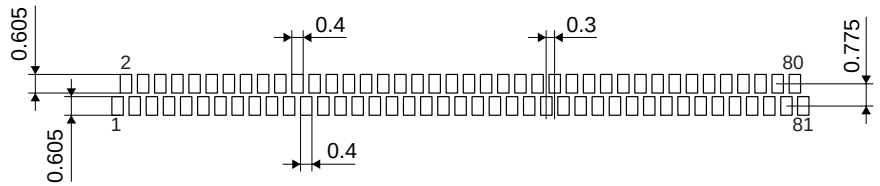


20 PACKAGE FOR TEST SAMPLES

S1C88655COFQTP

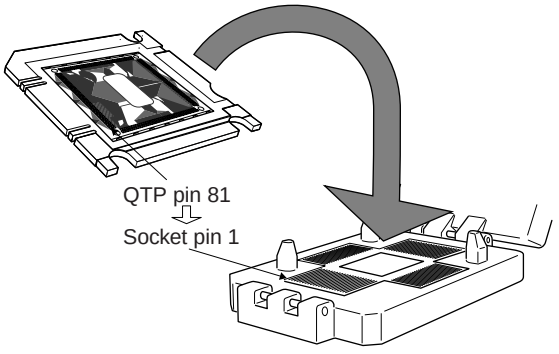
(Unit: mm)





Inserting QTP into the socket

Make sure the orientation of the carrier when inserting it into the socket.



Note: The analog characteristic values evaluated using a test sample may differ from those of the actual product due to the parasitic capacitance on the board and other conditions.

S1C88655COFQTP pin - pad correspondence table

IC Pad	Name	QTP pin No.	Socket pin No.	IC Pad	Name	QTP pin No.	Socket pin No.	IC Pad	Name	QTP pin No.	Socket pin No.	IC Pad	Name	QTP pin No.	Socket pin No.
–	–	81	1	91	(N.C.)	324	82	161	SEG24	243	163	241	SEG104	162	244
11	V_{DD}	80	2	92	(N.C.)	323	83	162	SEG25	242	164	242	SEG105	161	245
12	OSC2	79	3	93	(N.C.)	322	84	163	SEG26	241	165	243	SEG106	160	246
13	OSC1	78	4	94	(N.C.)	321	85	164	SEG27	240	166	244	SEG107	159	247
14	V_{SS}	77	5	95	(N.C.)	320	86	165	SEG28	239	167	245	SEG108	158	248
15	V_{D1}	76	6	96	(N.C.)	319	87	166	SEG29	238	168	246	SEG109	157	249
16	OSC4	75	7	97	(N.C.)	318	88	167	SEG30	237	169	247	SEG110	156	250
17	OSC3	74	8	98	(N.C.)	317	89	168	SEG31	236	170	248	SEG111	155	251
18	$\overline{TEST}$	73	9	–	–	316	90	169	SEG32	235	171	249	SEG112	154	252
19	MCU/$\overline{MPU}$	72	10	–	–	315	91	170	SEG33	234	172	250	SEG113	153	253
20	$\overline{RESET}$	71	11	–	–	314	92	171	SEG34	233	173	251	SEG114	152	254
21	V_{SS}	70	12	–	–	313	93	172	SEG35	232	174	252	SEG115	151	255
22	P27/FR/EXCL3	69	13	–	–	312	94	173	SEG36	231	175	253	SEG116	150	256
23	P26/CL/EXCL2	68	14	–	–	311	95	174	SEG37	230	176	254	SEG117	149	257
24	P25/$\overline{BACK}$/EXCL1	67	15	–	–	310	96	175	SEG38	229	177	255	SEG118	148	258
25	P24/$\overline{BREQ}$/EXCL0	66	16	–	–	309	97	176	SEG39	228	178	256	SEG119	147	259
26	P23/$\overline{TOUT2}$/$\overline{TOUT3}$	65	17	–	–	308	98	177	SEG40	227	179	257	SEG120	146	260
27	P22/FOUT	64	18	–	–	307	99	178	SEG41	226	180	258	SEG121	145	261
28	P21/TOUT2/TOUT3	63	19	99	(N.C.)	306	100	179	SEG42	225	181	259	SEG122	144	262
29	P20/TOUT0/TOUT1	62	20	100	(N.C.)	305	101	180	SEG43	224	182	260	SEG123	143	263
30	P17/$\overline{SRDY1}$	61	21	101	COM31	304	102	181	SEG44	223	183	261	SEG124	142	264
31	P16/$\overline{SCLK1}$	60	22	102	COM30	303	103	182	SEG45	222	184	262	SEG125	141	265
32	P15/SOUT1	59	23	103	COM29	302	104	183	SEG46	221	185	263	SEG126	140	266
33	P14/SIN1	58	24	104	COM28	301	105	184	SEG47	220	186	264	SEG127	139	267
34	P13/$\overline{SRDY0}$	57	25	105	COM27	300	106	185	SEG48	219	187	265	(N.C.)	138	268
35	P12/$\overline{SCLK0}$	56	26	106	COM26	299	107	186	SEG49	218	188	266	(N.C.)	137	269
36	P11/SOUT0	55	27	107	COM25	298	108	187	SEG50	217	189	–	–	136	270
37	P10/SIN0	54	28	108	COM24	297	109	188	SEG51	216	190	267	(N.C.)	135	271
38	V_{DD}	53	29	109	COM23	296	110	189	SEG52	215	191	268	(N.C.)	134	272
39	P07/D7	52	30	110	COM22	295	111	190	SEG53	214	192	269	COM32	133	273
40	P06/D6	51	31	111	COM21	294	112	191	SEG54	213	193	270	COM33	132	274
41	P05/D5	50	32	112	COM20	293	113	192	SEG55	212	194	271	COM34	131	275
42	P04/D4	49	33	113	COM19	292	114	193	SEG56	211	195	272	COM35	130	276
43	P03/D3	48	34	114	COM18	291	115	194	SEG57	210	196	273	COM36	129	277
44	P02/D2	47	35	115	COM17	290	116	195	SEG58	209	197	274	COM37	128	278
45	P01/D1	46	36	116	COM16	289	117	196	SEG59	208	198	275	COM38	127	279
46	P00/D0	45	37	117	COM15	288	118	197	SEG60	207	199	276	COM39	126	280
47	R00/A0	44	38	118	COM14	287	119	198	SEG61	206	200	277	COM40	125	281
48	R01/A1	43	39	119	COM13	286	120	199	SEG62	205	201	278	COM41	124	282
49	R02/A2	42	40	120	COM12	285	121	200	SEG63	204	202	279	COM42	123	283
50	R03/A3	41	41	121	COM11	284	122	–	–	203	203	280	COM43	122	284
51	R04/A4	40	42	122	COM10	283	123	201	SEG64	202	204	281	COM44	121	285
52	R05/A5	39	43	123	COM9	282	124	202	SEG65	201	205	282	COM45	120	286
53	R06/A6	38	44	124	COM8	281	125	203	SEG66	200	206	283	COM46	119	287
54	R07/A7	37	45	125	COM7	280	126	204	SEG67	199	207	284	COM47	118	288
55	R10/A8	36	46	126	COM6	279	127	205	SEG68	198	208	285	COM48	117	289
56	R11/A9	35	47	127	COM5	278	128	206	SEG69	197	209	286	COM49	116	290
57	R12/A10	34	48	128	COM4	277	129	207	SEG70	196	210	287	COM50	115	291
58	R13/A11	33	49	129	COM3	276	130	208	SEG71	195	211	288	COM51	114	292
59	R14/A12	32	50	130	COM2	275	131	209	SEG72	194	212	289	COM52	113	293
60	R15/A13	31	51	131	COM1	274	132	210	SEG73	193	213	290	COM53	112	294
61	R16/A14	30	52	132	COM0	273	133	211	SEG74	192	214	291	COM54	111	295
62	R17/A15	29	53	133	(N.C.)	272	134	212	SEG75	191	215	292	COM55	110	296
63	R20/A16	28	54	134	(N.C.)	271	135	213	SEG76	190	216	293	COM56	109	297
64	R21/A17	27	55	–	–	270	136	214	SEG77	189	217	294	COM57	108	298
65	R22/A18	26	56	135	(N.C.)	269	137	215	SEG78	188	218	295	COM58	107	299
66	R23/A19	25	57	136	(N.C.)	268	138	216	SEG79	187	219	296	COM59	106	300
67	R24/$\overline{RD}$	24	58	137	SEG0	267	139	217	SEG80	186	220	297	COM60	105	301
68	R25/$\overline{WR}$	23	59	138	SEG1	266	140	218	SEG81	185	221	298	COM61	104	302
69	R30/$\overline{CE0}$	22	60	139	SEG2	265	141	219	SEG82	184	222	299	COM62	103	303
70	R31/$\overline{CE1}$	21	61	140	SEG3	264	142	220	SEG83	183	223	300	COM63	102	304
71	R32/$\overline{CE2}$	20	62	141	SEG4	263	143	221	SEG84	182	224	301	(N.C.)	101	305
72	R33/$\overline{CE3}$	19	63	142	SEG5	262	144	222	SEG85	181	225	302	(N.C.)	100	306
73	(N.C.)	18	64	143	SEG6	261	145	223	SEG86	180	226	–	–	99	307
74	V_{DD}	17	65	144	SEG7	260	146	224	SEG87	179	227	–	–	98	308
75	V_{SS}	16	66	145	SEG8	259	147	225	SEG88	178	228	–	–	97	309
76	(N.C.)	15	67	146	SEG9	258	148	226	SEG89	177	229	–	–	96	310
77	CA3P	14	68	147	SEG10	257	149	227	SEG90	176	230	–	–	95	311
78	CA1M	13	69	148	SEG11	256	150	228	SEG91	175	231	–	–	94	312
79	CA1P	12	70	149	SEG12	255	151	229	SEG92	174	232	–	–	93	313
80	V_{D2}	11	71	150	SEG13	254	152	230	SEG93	173	233	–	–	92	314
81	CA4P	10	72	151	SEG14	253	153	231	SEG94	172	234	1	(N.C.)	91	315
82	CA2M	9	73	152	SEG15	252	154	232	SEG95	171	235	2	(N.C.)	90	316
83	CA2P	8	74	153	SEG16	251	155	233	SEG96	170	236	3	(N.C.)	89	317
84	V_{D2}	7	75	154	SEG17	250	156	234	SEG97	169	237	4	(N.C.)	88	318
85	V_{SS}	6	76	155	SEG18	249	157	235	SEG98	168	238	5	(N.C.)	87	319
86	V_{C1}	5	77	156	SEG19	248	158	236	SEG99	167	239	6	(N.C.)	86	320
87	V_{C2}	4	78	157	SEG20	247	159	237	SEG100	166	240	7	(N.C.)	85	321
88	V_{C3}	3	79	158	SEG21	246	160	238	SEG101	165	241	8	(N.C.)	84	322
89	V_{C4}	2	80	159	SEG22	245	161	239	SEG102	164	242	9	(N.C.)	83	323
90	V_{C5}	1	81	160	SEG23	244	162	240	SEG103	163	243	10	(N.C.)	82	324

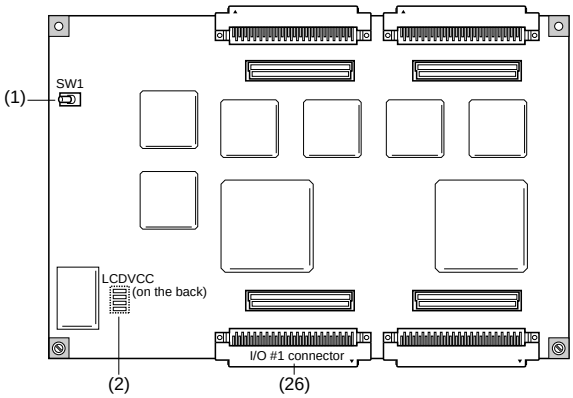
APPENDIX A PERIPHERAL CIRCUIT BOARD FOR S1C88655

(S5U1C88000P1 + S5U1C88655P2 + S5U1C88655T1)

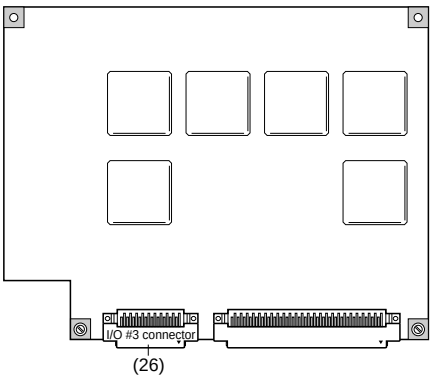
This manual describes how to use the Peripheral Circuit Board for S1C88655 (S5U1C88000P1 + S5U1C88655P2 + S5U1C88655T1). This circuit board is used to provide emulation functions when it is installed in the ICE (S5U1C88000H5), a debugging tool for the 8-bit Single Chip Microcomputer S1C88 Family.
The explanation assumes that the S1C88655 circuit data has been downloaded into the S1C88 Family Peripheral Circuit Board (S5U1C88000P1).
For how to download circuit data into the S5U1C88000P1 and specifications of the boards, refer to Sections A.4 and A.6, respectively. For details on ICE functions and how to operate the debugger, refer to the separately prepared manuals.

A.1 Names and Functions of Each Part

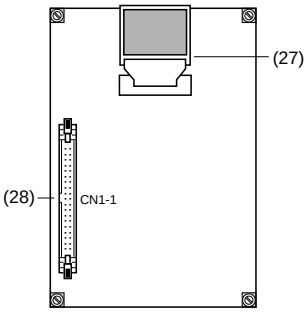
The following explains the names and functions of each part of the S5U1C88000P1, S5U1C88655P2 and S5U1C88655T1.



Main board (S5U1C88000P1)



Add-on board (S5U1C88655P2)



* The LCD panel (demonstration) board (S5U1C88655T1) is required when debugging displays on LCD using the peripheral circuit board for S1C88655.

LCD panel (demonstration) board (S5U1C88655T1)

Fig. A.1.1 Board layout

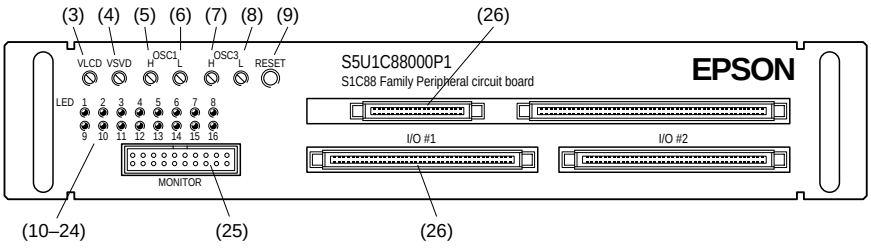


Fig. A.1.2 Panel layout (S5U1C88000P1)

(1) SW1

When downloading circuit data, set this switch to the "3" position. Otherwise, set to position "1".

(2) LCDVCC (on the back of the S5U1C88000P1 board)

Unused.
However, make sure that the switches are set as a combination as shown in the table below.

Table A.1.1 Setting LCDVCC

LCDVCC			
1	2	3	4
ON	OFF	OFF	ON
OFF	ON	OFF	OFF
OFF	OFF	ON	OFF
OFF	OFF	OFF	ON

(3) VLCD control

Unused.

(4) VSVD control

This control is used for varying the power supply voltage to confirm the supply voltage detection (SVD) function. (Refer to Section A.5.2, "Differences from Actual IC".)

(5) OSC1 H control

This control is used for coarse adjustment of the OSC1 CR oscillation frequency.

(6) OSC1 L control

This control is used for fine adjustment of the OSC1 CR oscillation frequency.

(7) OSC3 H control

This control is used for coarse adjustment of the OSC3 CR oscillation frequency.

(8) OSC3 L control

This control is used for fine adjustment of the OSC3 CR oscillation frequency.

(9) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(10) LED 1 (MPU/MCU)

Indicates the MPU or MCU mode.
Lit: MPU mode
Not lit: MCU mode

(11) LED 2 (BUSMOD), LED 3 (CPUMOD)

Indicates the bus and CPU modes (BUSMOD / CPUMOD register settings).

Table A.1.2 Bus and CPU modes

BUSMOD	CPUMOD	Bus mode	CPU mode
Lit	Lit	Expansion	Maximum
Lit	Not lit		Minimum
Not lit	Lit	Single chip	Maximum
Not lit	Not lit		Minimum

(12) LED 4 (CLKCHG)

Indicates the CPU operating clock.
Lit: OSC3 (CLKCHG register = "1")
Not lit: OSC1 (CLKCHG register = "0")

(13) LED 5 (SOSC1)

Indicates the OSC1 oscillation status.
Lit: OSC1 oscillation is on (SOSC1 register = "1")
Not lit: OSC1 oscillation is off (SOSC1 register = "0")

(14) LED 6 (SOSC3)

Indicates the OSC3 oscillation status.
Lit: OSC3 oscillation is on (SOSC3 register = "1")
Not lit: OSC3 oscillation is off (SOSC3 register = "0")

(15) LED 7 (SVDON)

Indicates the SVD circuit status.
Lit: SVD circuit is on (SVDON register = "1")
Not lit: SVD circuit is off (SVDON register = "0")

(16) LED 8 (LBON)

Indicates the supply voltage booster circuit status.
Lit: Supply voltage booster circuit is on (LBON register = "1")
Not lit: Supply voltage booster circuit is off (LBON register = "0")

(17) LED 9 (VC5ON)

Indicates the V_{C5} voltage generator status.
Lit: V_{C5} voltage generator is on (VC5ON register = "1")
Not lit: V_{C5} voltage generator is off (VC5ON register = "0")

(18) LED 10 (VCON)

Indicates the $V_{C1–4}$ voltage generator status.
Lit: $V_{C1–4}$ voltage generator is on (VCON register = "1")
Not lit: $V_{C1–4}$ voltage generator is off (VCON register = "0")

(19) LED 11 (LCDON)

Indicates the LCD driver circuit status.
Lit: LCD driver circuit is on (LCDON register = "1")
Not lit: LCD driver circuit is off (LCDON register = "0")

(20) LED 12 (HALT/SLEEP)

Indicates the CPU status.
Lit: HALT or SLEEP
Not lit: RUN

(21) LED 13

Unused.

(22) LED 14 (OSC1 operating clock)

The OSC1 operating clock is connected to this LED. The corresponding monitor pin (pin 14) can be used to check the OSC1 clock frequency.

(23) LED 15 (OSC3 operating clock)

The OSC3 operating clock is connected to this LED. The corresponding monitor pin (pin 15) can be used to check the OSC3 clock frequency.

(24) LED 16 (FPGA configuration)

If the FPGA on the S5U1C88000P1 includes circuit data, this LED lights when the power is turned on. If this LED does not light at power-up, a circuit data must be written to the FPGA before debugging can be started (turn the power on again after writing data).

(25) LED signal monitor connector

This connector provides the signals that drive the LEDs shown above for monitoring. The signals listed below are output from the connector pins. The signal level is high when the LED is lit and is low when the LED is not lit.

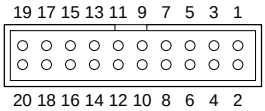


Fig. A.1.3 LED signal monitor connector

Pin 1: LED 1 (MPU/MCU mode)
Pin 2: LED 2 (Bus mode)
Pin 3: LED 3 (CPU mode)
Pin 4: LED 4 (CPU operating clock)
Pin 5: LED 5 (OSC1 oscillation status)
Pin 6: LED 6 (OSC3 oscillation status)
Pin 7: LED 7 (SVD circuit status)
Pin 8: LED 8 (Supply voltage booster circuit status)
Pin 9: LED 9 (V_{C5} voltage generator status)
Pin 10: LED 10 ($V_{C1–4}$ voltage generator status)
Pin 11: LED 11 (LCD driver circuit status)
Pin 12: LED 12 (HALT/SLEEP, RUN status)
Pin 14: LED 14 (OSC1 operating clock)
Pin 15: LED 15 (OSC3 operating clock)

Pin 18: OSC1 CR oscillation frequency monitor pin
Pin 19: OSC3 CR oscillation frequency monitor pin

Pins 13, 16, 17 and 20 are not used.
The CR oscillation clock is connected to pins 18 and 19. (The CR oscillation circuit on this board always operates even if crystal oscillation is selected by mask option and regardless of the SOSC1/3 register status.) These pins can be used to monitor CR oscillation when adjusting the oscillation frequency.

(26) I/O #1, I/O #3 connectors

These are the connectors for connecting the I/O and LCD panel board. The I/O cables (80-pin/40-pin × 2 flat type, 40-pin/20-pin × 2 flat type) are used to connect to the target system.

(27) LCD module (standard TCM)

This is a 128 × 64-dot LCD panel module using the standard TCM (see Appendix C). This LCD module has included an actual S1C88655 device, note, however, that the chip is configured to work as only an LCD driver using the device test function (unreleased).

(28) ICE connector (CN1-1)

Connect between this connector and I/O #1 connector on the S5U1C88000P1 using the I/O cable (80-pin/40-pin × 2 flat type).

A.2 Installation

A.2.1 Installing S5U1C88655P2 to S5U1C88000P1

Aim the I/O connectors on the add-on board (S5U1C88655P2) at the front panel of the main board (S5U1C88000P1) and insert the four connectors on the back of the S5U1C88655P2 board into the corresponding connectors on the S5U1C88000P1 board.

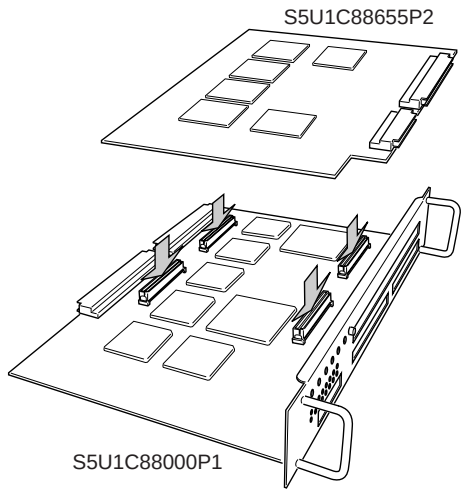


Fig. A.2.1.1 Installing S5U1C88655P2 to S5U1C88000P1

A.2.2 Installing into the ICE (S5U1C88000H5)

Insert the S5U1C88000P1 along by the lower guide rail of the ICE (S5U1C88000H5), until the connectors fit into the ICE back-panel connectors.

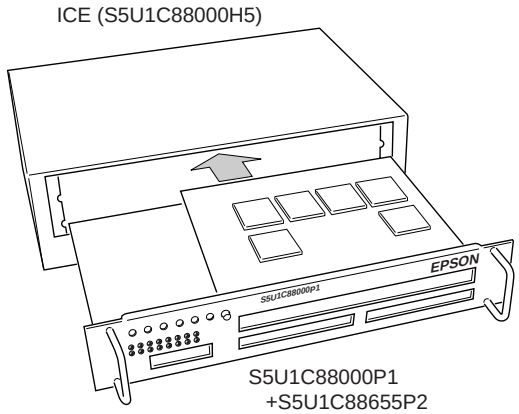


Fig. A.2.2.1 Installing into the ICE (S5U1C88000H5)

Note: The S5U1C88000P1 and S5U1C88655P2 may fail to operate if they are not adequately mounted, so be sure to mount them securely.

A.3 Connecting to the Target System

This section explains how to connect the S5U1C88000P1 + S5U1C88655P2 to the target system and the LCD panel board (S5U1C88655T1).

Note: Turn the power of all equipment off before connecting or disconnecting cables.

Use the I/O cables (80-pin / 40-pin × 2 flat type, 40-pin / 20-pin × 2 flat type) to connect the target system to the I/O #1 and I/O #3 connectors of the front panel. Connect the 80-pin and 40-pin cable connectors to the I/O #1 and I/O #3 connectors, respectively, and the CN1-2 connector of the 40-pin × 2 cable and the 20-pin × 2 cable connectors (CN3-1 and CN3-2) to the target system.
The LCD panel board (S5U1C88655T1) is connected to the I/O #1 connector of the front panel using the CN1-1 connector of the 40-pin × 2 cable. Be careful as power (V_{DD}) is supplied to the I/O #1 and I/O #3 connectors.

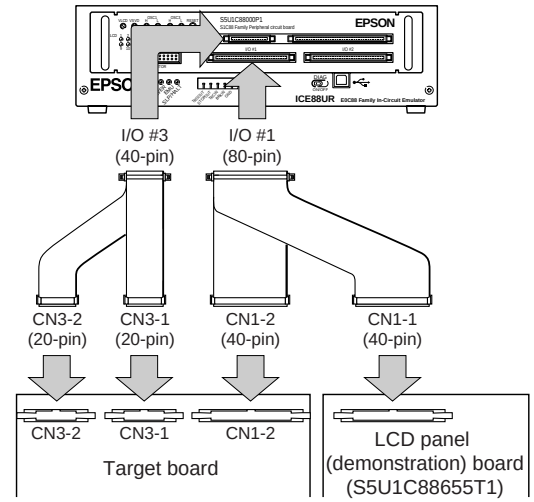


Fig. A.3.1 Connecting to the target system

The following shows the clock frequencies generated from the on-board crystal oscillation circuits:
OSC1 crystal oscillation circuit: 32.768 kHz
OSC3 crystal oscillation circuit: 4.9152 MHz

When CR oscillation is selected, the oscillation frequency can be adjusted using the controls on the front panel (OSC1H and OSC1L for adjusting OSC1, OSC3H and OSC3L for adjusting OSC3). Use a frequency counter or other equipment to be connected to the OSC1 CR oscillation frequency monitor pin (pin 18) on the monitor connector or OSC3 CR oscillation frequency monitor pin (pin 19) for monitoring the frequency during adjustment. Be sure of the frequency when using this monitor pin because the CR oscillation frequency is initially undefined.

Notes:
- *The LCD panel board operating clock frequency is limited to that of the connected LCD module (standard TCM).*
- *If the LCD panel is out of synchronization with the S5U1C88000P1 + S5U1C88655P2, reset the system using the RESET switch on the S5U1C88000P1.*

I/O connector pin assignment

Table A.3.1 I/O #1 connector

40-pin CN1-1		40-pin CN1-2	
No.	Pin name	No.	Pin name
1	VDD (3.3 V)	1	R10/A8
2	VDD (3.3 V)	2	R11/A9
3	VSS	3	R12/A10
4	VSS	4	R13/A11
5	DMTAD0	5	R14/A12
6	DMTAD1	6	R15/A13
7	DMTAD2	7	R16/A14
8	DMTAD3	8	R17/A15
9	DMTAD4	9	R20/A16
10	DMTAD5	10	R21/A17
11	DMTAD6	11	R22/A18
12	DMTAD7	12	R23/A19
13	DMTAD8	13	R24/$\overline{RD}$
14	DMTAD9	14	R25/$\overline{WR}$
15	DMTAD10	15	R30/$\overline{CE0}$
16	DMTAD11	16	R31/$\overline{CE1}$
17	DMTAD12	17	R32/$\overline{CE2}$
18	DMTAD13	18	R33/$\overline{CE3}$
19	DMTAD14	19	N.C.
20	DMTAD15	20	GND_IN
21	N.C.	21	OSC3EX
22	DMTEB0	22	GND_IN
23	DMTEB1	23	OSC1EX
24	DMTEB2	24	GND_IN
25	DMTEB3	25	N.C.
26	DMTEB4	26	N.C.
27	DMTEB5	27	N.C.
28	DMTEB6	28	N.C.
29	DMTEB7	29	N.C.
30	N.C.	30	N.C.
31	DMT_XRESET	31	N.C.
32	N.C.	32	N.C.
33	DMT_PK	33	N.C.
34	DMT_PL	34	N.C.
35	DMT_I/O0	35	N.C.
36	DMT_I/O1	36	N.C.
37	DMT_I/O2	37	N.C.
38	DMT_I/O3	38	N.C.
39	DMT_DBS0	39	N.C.
40	DMT_DBS1	40	N.C.

Table A.3.2 I/O #3 connector

20-pin CN3-1		20-pin CN3-2	
No.	Pin name	No.	Pin name
1	P20/TOUT0/TOUT1	1	VSS
2	P21/TOUT2/TOUT3	2	VSS
3	P22/FOUT	3	P00/D0
4	P23/$\overline{TOUT2}$/$\overline{TOUT3}$	4	P01/D1
5	P24/$\overline{BREQ}$/EXCL0	5	P02/D2
6	P25/$\overline{BACK}$/EXCL1	6	P03/D3
7	P26/CL/EXCL2	7	P04/D4
8	P27/FR/EXCL3	8	P05/D5
9	$\overline{RESET}$	9	P06/D6
10	MCU/$\overline{MPU}$	10	P07/D7
11	N.C.	11	VDD (3.3 V)
12	N.C.	12	VDD (3.3 V)
13	R00/A0	13	P10/SIN0
14	R01/A1	14	P11/SOUT0
15	R02/A2	15	P12/$\overline{SCLK0}$
16	R03/A3	16	P13/$\overline{SRDY0}$
17	R04/A4	17	P14/SIN1
18	R05/A5	18	P15/SOUT1
19	R06/A6	19	P16/$\overline{SCLK1}$
20	R07/A7	20	P17/$\overline{SRDY1}$

Note: The pin names of the CN1-1 connector indicates the internal signals connected to the connector. This connector must be used to connect the LCD panel (demonstration) board (S5U1C88655T1).

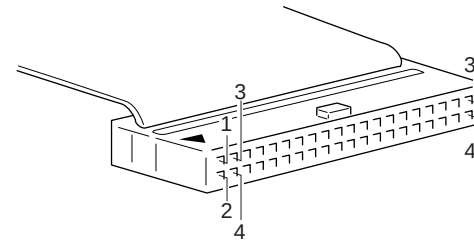


Fig. A.3.2 CN1-1/CN1-2 pin layout

A.4 Downloading Circuit Data to the S5U1C88000P1

This board (S5U1C88000P1) comes with the FPGA that contains factory inspection data, therefore the circuit data for the model to be used should be downloaded. The following explains the downloading procedure.

1) Set the switch "SW1"*1 on this board to the "3" position.
2) Install this board to the ICE (S5U1C88000H5) as shown in Section A.2.2.
3) Connect the ICE to the host PC. Then turn the host PC and ICE on.
4) Invoke the debugger included in the ICE or assembler package. For how to use the ICE and debugger, refer to the manuals supplied with the ICE and assembler package.
5) Download the circuit data file (.mcs) corresponding to the model by entering the following commands in the command window.

`>XFER`		(erase all)
`>XFWR`	<*file name*>	(download the specified file)*2
`>XFCP`	<*file name*>	(compare the specified file and downloaded data)

6) Terminate the debugger and then turn the ICE off.
7) Remove this board from the ICE and set the switch "SW1" on the board to the "1" position.
8) Install this board to the ICE again.
9) Turn the ICE on and invoke the debugger again. Debugging can be started here.

*1 See Figure A.1.1, "Board layout", for the location of SW1.
*2 The downloading takes about 5 minutes.

A.5 Precautions

Take the following precautions when using the Peripheral Circuit Board for S1C88655.

A.5.1 Precaution for operation

(1) Turn the power of all equipment off before connecting or disconnecting cables.

(2) The mask option data must be loaded before debugging can be started.

A.5.2 Differences from actual IC

Caution is called for due to the following function and property related differences with the actual IC. If these precautions are overlooked, it may not operate on the actual IC, even if it operates on the ICE in which the Peripheral Circuit Board for S1C88655 has been installed.

(1) I/O differences

Interface power voltage

This board and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter or similar circuit on the target system side to accommodate the required interface voltage.

Drive capability of each output port

The drive capability of each output port on this board is higher than that of the actual IC. When designing the application system and software, refer to Chapter 19, "Electrical Characteristics", to confirm the drive capability of each output port.

Input port characteristics

The AC characteristic of the input terminal is different from that of the actual IC and it affects the input interrupt function. Therefore, evaluate the operation in the actual IC if the rise / fall time of the input signal is long.

Protective diode of each port

All I / O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between this board and the target system are set to +3.3 V. Therefore, this board and the target system cannot be interfaced with a voltage exceeding V_{DD} even if the output ports are configured with open-drain output.

Pull-up resistance value

The pull-up resistance values on this board are set to 100 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 19, "Electrical Characteristics".
Note that when using pull-up resistors to pull the input terminals high, the input terminals may require a certain period to reach a valid high level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since rise delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by this board differs significantly from that of the actual IC. Inspecting the LEDs on the S5U1C88000P1 front panel may help keep track of approximate current consumption. The following factors / components greatly affect device current consumption:

Those which can be verified by LEDs and monitor pins

a) Run and Halt execution ratio
(verified by LEDs and monitor pins on the ICE)
b) CPU operating clock change control
(LED 4: monitor pin 4)
c) OSC1 oscillation on / off control
(LED 5: monitor pin 5)
d) OSC3 oscillation on / off control
(LED 6: monitor pin 6)
e) SVD circuit on / off control
(LED 7: monitor pin 7)
f) Supply voltage booster circuit
(LED 8: monitor pin 8)
g) V_{C5} voltage generator
(LED 9: monitor pin 9)
h) $V_{C1–4}$ voltage generator
(LED 10: monitor pin 10)
i) LCD control
(LED 11: monitor pin 11)
j) SLEEP and HALT execution ratio
(LED 12: monitor pin 12)
k) OSC1 operating clock
(LED 14: monitor pin 14)
l) OSC3 operating clock
(LED 15: monitor pin 15)

Those that can only be counteracted by system or software

m) Current consumed by the internal pull-up resistors
n) Input ports in a floating state

(3) Functional precautions

SVD circuit

- The SVD function is realized by artificially varying the power supply voltage using the VSVD control on the front panel of the S5U1C88000P1.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. The delay time on this board differs from that of the actual IC. Refer to Chapter 19, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- The evaluation voltages supported in this board are different from those of the actual IC. When debugging the SVD operation using this board, evaluate the SVD results as levels not voltages.

Oscillation circuit

- The OSC1 crystal oscillation frequency is fixed at 32.768 kHz.
- The OSC1 CR oscillation frequency can be adjusted in the range of approx. 20 kHz to 500 kHz using the control on the S5U1C88000P1 front panel. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 19, "Electrical Characteristics", to select the appropriate operating frequency.
- The OSC3 crystal oscillation frequency is fixed at 4.9152 MHz.
- The OSC3 CR oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz using the control on the S5U1C88000P1 front panel. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 19, "Electrical Characteristics", to select the appropriate operating frequency.
- The Peripheral Circuit Board for S1C88655 does not include the OSC3 ceramic oscillation circuit. When ceramic oscillation circuit is selected by mask option, the Peripheral Circuit Board for S1C88655 uses the on-board crystal oscillation circuit.
- When using an external clock, adjust the external clock (amplitude: 3.3 V ±5%, duty: 50% ±10%) and input to the OSC1EX or OSC3EX terminal with V_{SS} as GND. Moreover, the GND_IN terminals adjacent to the OSC1EX and OSC3EX terminals should be connected to the GND line in order to stabilize the clock waveforms.

- This board can operate normally even when the CPU clock is switched to OSC3 (CLKCHG = "1") immediately after the OSC3 oscillation control circuit is turned on (SOSC3 = "1") without a wait time inserted. In the actual IC, an oscillation stability wait time is required before switching the CPU clock after the OSC3 oscillation is turned on. Refer to Chapter 19, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- This board can operate normally even when the CPU clock is switched to OSC1 (CLKCHG = "0") immediately after the OSC1 oscillation control circuit is turned on (SOSC1 = "1") without a wait time inserted. In the actual IC, an oscillation stability wait time is required before switching the CPU clock after the OSC1 oscillation is turned on. Refer to Chapter 19, "Electrical Characteristics", when setting the appropriate wait time for the actual IC.
- This board starts operating without waiting for an oscillation start time after SLEEP status is cancelled.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with this board, may not function properly with the actual IC.
- This board contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, this board can operate with the OSC3 circuit.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on this board differs from that of the actual IC.

Access to undefined address space

If any undefined space in the S1C88655's internal ROM / RAM or I / O is accessed for data read or write operations, the read / written value is indeterminate. Additionally, it is important to remain aware that the indeterminate state differs between the Peripheral Circuit Board for S1C88655 and the actual IC.

Reset circuit

Keep in mind that the operation sequence from when the ICE with this board installed is powered on until the time at which the program starts running differs from the sequence of the actual IC. This is because this board becomes capable of operating as a debugging system after the user program and optional data are downloaded.

Internal power supply circuit

The LCD drive voltage on this board is different from that on the actual IC.

Function option

- Input interface level
  The actual IC allows selection of the input interface level for P10–P17 and P20–P27 either COMS level or CMOS Schmitt level by a function option. This board supports CMOS level only and selection of the function option using Winfog does not affect the interface level of this board.

(4) Notes on model support

Parameter file

The ROM, RAM and I / O spaces in the ICE with this board installed are configured when the debugger on the personal computer starts up using the parameter file (88655.par) provided for each model.
The parameter file allows the user to modify its contents according to the ROM and RAM spaces actually used. Do not configure areas other than below when using the IC in single chip maximum mode.

ROM area:	0000H to BFFFH
	10000H to 8FFFFH
RAM area:	C000H to E3FFH
	E800H to EBFFH
Stack area:	C000H to DFFFH

Access disable area

When using this board for development of an S1C88655 application, be sure not to read and write from / to I / O memory addresses FF22H and FFC0H to FFDDH. Furthermore, do not change the initial values when writing to bit D4 of address FF23H.

A.6 Product Specifications

A.6.1 S5U1C88000P1 specifications

S5U1C88000P1

Dimensions (mm):
247.5 (wide) × 165 (depth) × 44.6 (height)
Weight:
Approx. 500 g
Power supply:
DC 5 V ± 5%, less than 1 A
(supplied from ICE main unit)

I/O connection cable (80-pin/40-pin x 2, 2 cables)

S5U1C88000P1 connector (80-pin):
KEL 8830E-080-170L, or equivalent
Cable connector (80-pin):
KEL 8822E-080-171 × 1
Cable connector (40-pin):
3M 7940-6500SC × 2
Cable:
40-pin flat cable × 2
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

Monitor signal cable

S5U1C88000P1 connector:
3M 7610-5002SC, or equivalent
Cable connector (10-pin):
3M 7910-6500SC × 1
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

Accessories

40-pin connector for the target system:
3M 3432-6002LCSC × 4

A.6.2 S5U1C88655P2 specifications

S5U1C88655P2

Dimensions (mm):
184 (W) × 152 (D) × 20 (H)

I/O cable (100-pin/50-pin x 2)

S5U1C88655P2 connector (100-pin):
KEL 8830E-100-170L-F
Cable connector (100-pin):
KEL 8822E-100-171-F × 1
Cable connector (50-pin):
Connector 3M 7950-6500SC × 2
Strain relief 3M 3448-7950 × 2
Cable:
50-pin flat cable × 1
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

I/O cable (40-pin/20-pin x 2)

S5U1C88655P2 connector (40-pin):
KEL 8830E-040-170L-F
Cable connector (40-pin):
KEL 8822E-040-171-F × 1
Cable connector (20-pin):
Connector 3M 7920-6500SC × 2
Strain relief 3M 3448-7920 × 2
Cable:
20-pin flat cable × 1
Interface:
CMOS interface (3.3 V)
Length:
Approx. 40 cm

Accessories

50-pin connector for the target system:
3M 3433-6002LCPL × 2
20-pin connector for the target system:
3M 3428-6002LCPL × 2

A.6.3 S5U1C88655T1 specifications

S5U1C88655T1

Dimensions (mm):
100 (W) × 150 (D) × 38 (H)

S5U1C88655T1 connector

3M 3433-6002LCPL

Interface

CMOS interface (3.3 V)

APPENDIX B USING FONT DATA

Font packages that can be used to display on LCD are provided for the S1C88655.
The package contains a sample program that runs on the S1C88-Family microcomputer to display this font data on an LCD, an application note for the sample program, and a bitmap utility that can be used to create custom font data.
The font data is supplied in an object file format (assembler output file identified by the extension .obj) to enable it to be embedded in the S1C88-Family microcomputer programs. Simply by linking this object file to the created application program, the font data can be used easily.

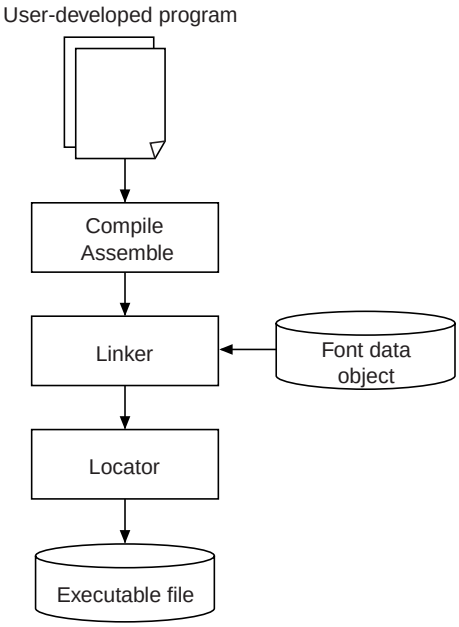
Notes: • *Before the font data included with the package and the typefaces shown in the manual can be used, a contract for a license to use the typefaces must be concluded between Seiko Epson and the purchaser.*

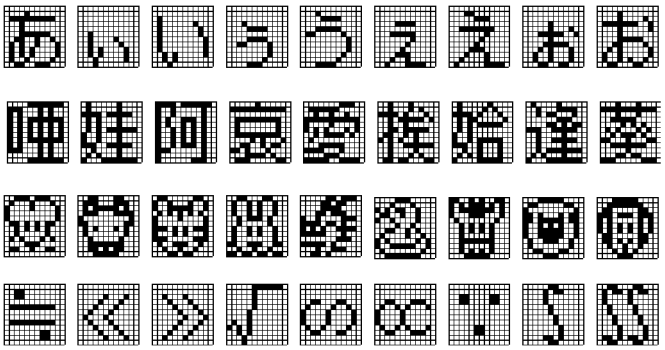
• *The programs necessary to obtain font data from the character codes and display the font data on an LCD must be created by the user.*

List of font packages

- **S5U1C88655R1**
  12 × 12-dot Japanese font
  (JIS level-1 and level-2, other characters)
- **S5U1C88655R3**
  12 × 12-dot Korean font
  (KSX1001)

Please contact Seiko Epson for other font packages.





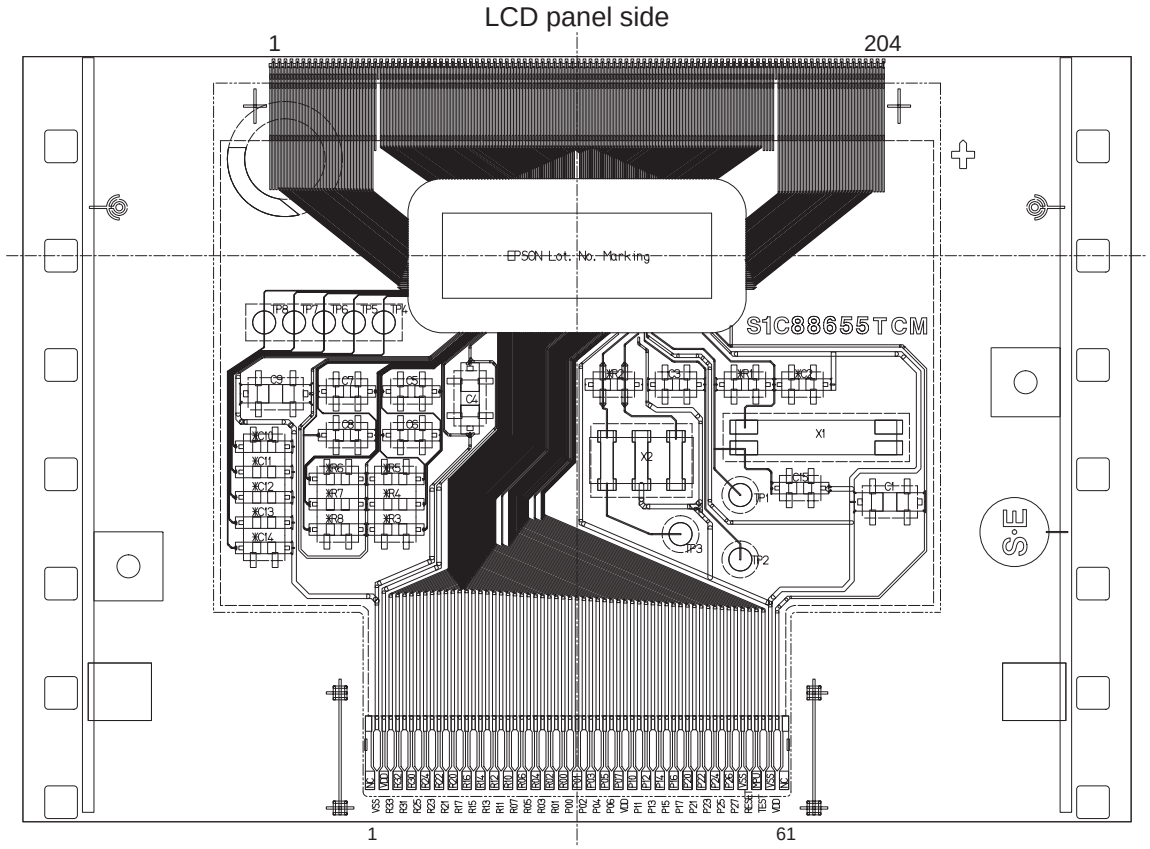
APPENDIX C TCM

TCM is a packaging method that mounts constituents such as IC and SMT (Surface Mount Technology) parts on an FPC (Flexible Printed Circuit) tape. Using a flexible FPC tape, which is adequate to narrow space mounting, as a printed-circuit board makes it possible to reduce size, weight and profile of the products. TCM is provided as the standard packaging form for the S1C88655 and the standard TCM has been released. Furthermore, Seiko Epson accepts orders for developing custom TCMs with the product specifications implemented. Please contact us for details of the standard TCM specifications and custom TCM development.

S1C88655 standard TCM specifications

1. OSC1 oscillation circuit
   CR (R_{CR1} = 1.5 MΩ)
2. OSC3 oscillation circuit
   CR (R_{CR3} = 39 kΩ)
3. Input port pull-up resistors
   $\overline{RESET}$ With pull-up resistor
   MCU / $\overline{MPU}$ With pull-up resistor
4. I/O port pull-up resistors
   P00–07, 10–17, 20–27 With pull-up resistor
5. I/O port input interface level
   P10–13, 20–23 CMOS Schmitt level
   P14–17, 24–27 CMOS level
6. Reset voltage detector
   Used
7. Watchdog timer overflow cycle
   32768 / f_{OSC1}
8. Watchdog timer overflow signal
   Interrupt (NMI)
9. Voltage booster
   Quintuple boosting circuit configuration
10. LCD panel size
    128 × 64
11. LCD panel specifications
    A panel with V_{C5} = 7 V and 1/9 bias specifications is recommended.

Standard TCM outline drawing (die-cut pattern before assembly)



∗ Recommended FPC connectors: FH23 series (Hirose Electric Co., LTD.)

Standard TCM pin layout

LCD panel side (upper side)

No.	Name	No.	Name	No.	Name	No.	Name
1	N.C.	52	SEG15	103	SEG66	154	SEG117
2	N.C.	53	SEG16	104	SEG67	155	SEG118
3	N.C.	54	SEG17	105	SEG68	156	SEG119
4	COM31	55	SEG18	106	SEG69	157	SEG120
5	COM30	56	SEG19	107	SEG70	158	SEG121
6	COM29	57	SEG20	108	SEG71	159	SEG122
7	COM28	58	SEG21	109	SEG72	160	SEG123
8	COM27	59	SEG22	110	SEG73	161	SEG124
9	COM26	60	SEG23	111	SEG74	162	SEG125
10	COM25	61	SEG24	112	SEG75	163	SEG126
11	COM24	62	SEG25	113	SEG76	164	SEG127
12	COM23	63	SEG26	114	SEG77	165	N.C.
13	COM22	64	SEG27	115	SEG78	166	N.C.
14	COM21	65	SEG28	116	SEG79	167	N.C.
15	COM20	66	SEG29	117	SEG80	168	N.C.
16	COM19	67	SEG30	118	SEG81	169	COM32
17	COM18	68	SEG31	119	SEG82	170	COM33
18	COM17	69	SEG32	120	SEG83	171	COM34
19	COM16	70	SEG33	121	SEG84	172	COM35
20	COM15	71	SEG34	122	SEG85	173	COM36
21	COM14	72	SEG35	123	SEG86	174	COM37
22	COM13	73	SEG36	124	SEG87	175	COM38
23	COM12	74	SEG37	125	SEG88	176	COM39
24	COM11	75	SEG38	126	SEG89	177	COM40
25	COM10	76	SEG39	127	SEG90	178	COM41
26	COM9	77	SEG40	128	SEG91	179	COM42
27	COM8	78	SEG41	129	SEG92	180	COM43
28	COM7	79	SEG42	130	SEG93	181	COM44
29	COM6	80	SEG43	131	SEG94	182	COM45
30	COM5	81	SEG44	132	SEG95	183	COM46
31	COM4	82	SEG45	133	SEG96	184	COM47
32	COM3	83	SEG46	134	SEG97	185	COM48
33	COM2	84	SEG47	135	SEG98	186	COM49
34	COM1	85	SEG48	136	SEG99	187	COM50
35	COM0	86	SEG49	137	SEG100	188	COM51
36	N.C.	87	SEG50	138	SEG101	189	COM52
37	SEG0	88	SEG51	139	SEG102	190	COM53
38	SEG1	89	SEG52	140	SEG103	191	COM54
39	SEG2	90	SEG53	141	SEG104	192	COM55
40	SEG3	91	SEG54	142	SEG105	193	COM56
41	SEG4	92	SEG55	143	SEG106	194	COM57
42	SEG5	93	SEG56	144	SEG107	195	COM58
43	SEG6	94	SEG57	145	SEG108	196	COM59
44	SEG7	95	SEG58	146	SEG109	197	COM60
45	SEG8	96	SEG59	147	SEG110	198	COM61
46	SEG9	97	SEG60	148	SEG111	199	COM62
47	SEG10	98	SEG61	149	SEG112	200	COM63
48	SEG11	99	SEG62	150	SEG113	201	N.C.
49	SEG12	100	SEG63	151	SEG114	202	N.C.
50	SEG13	101	SEG64	152	SEG115	203	N.C.
51	SEG14	102	SEG65	153	SEG116	204	N.C.

FPC connector side (lower side)

No.	Name	No.	Name
1	N.C.	52	P25
2	V_{SS}	53	P26
3	V_{DD}	54	P27
4	R33	55	V_{SS}
5	R32	56	$\overline{RESET}$
6	R31	57	MCU/$\overline{MPU}$
7	R30	58	$\overline{TEST}$
8	R25	59	V_{SS}
9	R24	60	V_{DD}
10	R23	61	N.C.
11	R22		
12	R21		
13	R20		
14	R17		
15	R16		
16	R15		
17	R14		
18	R13		
19	R12		
20	R11		
21	R10		
22	R07		
23	R06		
24	R05		
25	R04		
26	R03		
27	R02		
28	R01		
29	R00		
30	P00		
31	P01		
32	P02		
33	P03		
34	P04		
35	P05		
36	P06		
37	P07		
38	V_{DD}		
39	P10		
40	P11		
41	P12		
42	P13		
43	P14		
44	P15		
45	P16		
46	P17		
47	P20		
48	P21		
49	P22		
50	P23		
51	P24		

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