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S1R72005

Application Notes – Information on Differences from Previous Model

SEIKO EPSON CORPORATION

Rev.1.00

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Chapter 1 Overview

The **S1R72005B00A300** and **S1R72005F00A300** (hereafter referred to as the S1R72005#00A300) are an On-The-Go (OTG) device controller LSI conforming to USB 2.0-compliant Full Speed (12 Mbps) mode. Host functions, Peripheral functions, and the On-The-Go function are integrated on a single chip, enabling the LSI to operate as an OTG dual-role device.

The LSI presented here was developed from earlier Seiko Epson products, the S1R72005B00A100 and S1R72005F00A100, by redesigning their power supply for the I/O unit to allow provision of power separately for the USB interface and the CPU interface. Various functional improvements have been incorporated into the new product while maintaining near-100% software compatibility with the S1R72005#00A100.

This document provides differences in register specifications from the S1R72005#00A100. When reading this document, please refer to the other document titled "**S1R72005 Application Notes (Rev 1.21)**."

Note that differences from the S1R72005#00A100 are indicated in red in this document to facilitate software porting.

Chapter 2 Registers

2.1 Register Map

2.2 Detailed Description of Registers

2.2.4 Common Block

2.2.4.1 0x30 Macro Configuration (MacroConfig) – information on differences

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x30	MacroConfig	7:				00h
		6:				
		5:				
		4: COMPPwrDown	R/W	0: Normal	1: Internal 2.0V-comparator and 4.4V-comparator is powerdown	
		3:				
		2:				
		1:				
		0: ExtResMode	R/W	0: Use internal pull-up/pull down resistance	1: Use external pull-up/pull-down resistance	

This register sets the operation of the LSI's internal circuit.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 COMPPowerDown

This bit powers down the internal VBUS-2.0 V and VBUS-4.4 V comparators.

To minimize power consumption when the chip is inactive, set this register to 1.

0 – Operate normally

1 – Power down the VBUS-2.0 V and VBUS-4.4 V comparators

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 ExtResMode

This bit specifies whether the internal pull-up/pull-down resistors are used.

0 – Use the internal pull-up/pull-down resistors

1 – Use external pull-up/pull-down resistors

2.2.5.9 0x48 CPU Configuration0 (CPUConfig_0) – information on differences

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x48	CPUConfig_0	7:				00h
		6: WaitPortDisable	R/W	0: WAIT port enabled	1: WAIT port disabled	
		5: WaitMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		4: IntMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		3:				
		2: CPUEndian	R/W	0: CPU Big Endian	1: CPU Little Endian	
		1:				
		0: CPUBus8x16	R/W	0: CPU Bus 16bit Mode	1: CPU Bus 8bit Mode	

This register sets parameters involving the CPU interface.

The bits in this register and those in the CPUConfig_1 register are internally and one-for-one Boolean OR'd in the LSI. Thus, only one register needs to be set.

Bit 7 Reserved

Bit 6 WaitPortDisable

Setting this bit to 1 disables the xWAIT pin function (i.e., port is accessed in fixed cycles).

If the LSI is used with this bit set to 1, insert the appropriate cycles in the CPU bus cycle to meet the AC timing requirements stipulated in the S1R72005#00A300 hardware specifications.

0 – Output xWAIT

1 – Do not output xWAIT

Bit 5 WaitMode

This bit sets xWAIT pin output mode.

0 – xWAIT output in 0/Hi-Z mode

1 – xWAIT output in 0/1 mode

Bit 4 IntMode

This bit sets xINT pin output mode.

0 – xINT output in 0/Hi-Z mode

1 – xINT output in 0/1 mode

Bit 3 Reserved

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Bit 2 CPUEndian

This bit sets the CPU endian mode when the CPU bus is used as 16 bits wide.

This bit always applies, regardless of the LSI clock input condition.

0 – Support CPU access in big endian mode

1 – Support CPU access in little endian mode

Bit 1 Reserved

Bit 0 CPUBus8x16

To use the CPU bus as 8 bits wide, set this bit to 1.

If this bit is set to 1, the FIFOforCPU registers for each pipe and endpoint are functionally divided between the 8 low-order bits containing valid data and 8 high-order bits having no effect.

0 – Use the CPU bus in 16-bit mode

1 – Use the CPU bus in 8-bit mode

2.2.5.10 0x49 CPU Configuration1 (CPUConfig_1) – information on differences

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x49	CPUConfig_0	7:				00h
		6: WaitPortDisable	R/W	0: WAIT port enabled	1: WAIT port disabled	
		5: WaitMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		4: IntMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		3:				
		2: CPUEndian	R/W	0: CPU Big Endian	1: CPU Little Endian	
		1:				
		0: CPUBus8x16	R/W	0: CPU Bus 16bit Mode	1: CPU Bus 8bit Mode	

This register sets parameters involving the CPU interface.

The bits in this register and those in the CPUConfig_0 register are internally and one-for-one Boolean OR'd in the LSI. Thus, only one register needs to be set.

Bit 7 Reserved

Bit 6 WaitPortDisable

Setting this bit to 1 disables the xWAIT pin function (i.e., port is accessed in fixed cycles).

If the LSI is used with this bit set to 1, insert the appropriate cycles in the CPU bus cycle to meet the AC timing requirements stipulated in the S1R72005#00A300 hardware specifications.

0 – Output xWAIT

1 – Do not output xWAIT

Bit 5 WaitMode

This bit sets xWAIT pin output mode.

0 – xWAIT output in 0/Hi-Z mode

1 – xWAIT output in 0/1 mode

Bit 4 IntMode

This bit sets xINT pin output mode.

0 – xINT output in 0/Hi-Z mode

1 – xINT output in 0/1 mode

Bit 3 Reserved

(Continued to the next page)

(Continued from the preceding page)

Bit 2 CPUEndian

This bit sets the CPU endian mode when the CPU bus is used as 16 bits wide.

This bit always applies, regardless of the LSI clock input condition.

0 – Support CPU access in big endian mode

1 – Support CPU access in little endian mode

Bit 1 Reserved

Bit 0 CPUBus8x16

To use the CPU bus as 8 bits wide, set this bit to 1.

If this bit is set to 1, the FIFOforCPU registers for each pipe and endpoint are functionally divided between the 8 low-order bits containing valid data and 8 high-order bits having no effect.

0 – Use the CPU bus in 16-bit mode

1 – Use the CPU bus in 8-bit mode

2.2.12 ChannelE Register Block – information on differences

The contents of registers in the channel E register block (0xB0 to 0xBF) are identical to those in the channel A register block (0x70 to 0x7F). For more information on the channel E registers, refer to the description of channel A registers. In that case, please confirm that each register name is read as shown below.

aConfig_0／1	→	eConfig_0／1
aMaxPktSize_H／L	→	eMaxPktSize_H／L
PIPEaInterval	→	PIPEeInterval
PIPEaTranConfig	→	PIPEeTranConfig
PIPEaControl	→	PIPEeControl
PIPEaTotalSizeH／M／L	→	PIPEeTotalSizeH／M／L
EPaControl_0／1	→	EPeControl_0／1
aFIFOforCPU_H／L	→	eFIFOforCPU_H／L
aFIFOControl_0／1	→	eFIFOControl_0／1

In addition, register names including letters representing a channel (e.g., interrupt related registers) should be read in the same way as above.

Dummy pipe (PIPEe) settings during host operations required for the S1R72005#00A100 do not need to be set in the S1R72005#00A300.

Chapter 3 Known Problems and Solutions – information on differences

A problem encountered with the earlier S1R72005B00A100 and S1R72005F00A100 models wherein the host issues an unintended token has been resolved in the S1R72005B00A300 and S1R72005F00A300.

No corrective measures are required in software.

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Document Code: 410691100
First Issue: February 2004
Printed February 2006 in JAPAN