EPSON
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S1R72005B00A300/F00A300
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.0

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General Rules

- Scope of Application

The specifications given in this manual apply to the “S1R72005B00A300” and “S1R72005F00A300” USB On-The-Go controllers made by the Semiconductor Operations Division of Seiko Epson Corporation.

Table of Contents

1. Overview

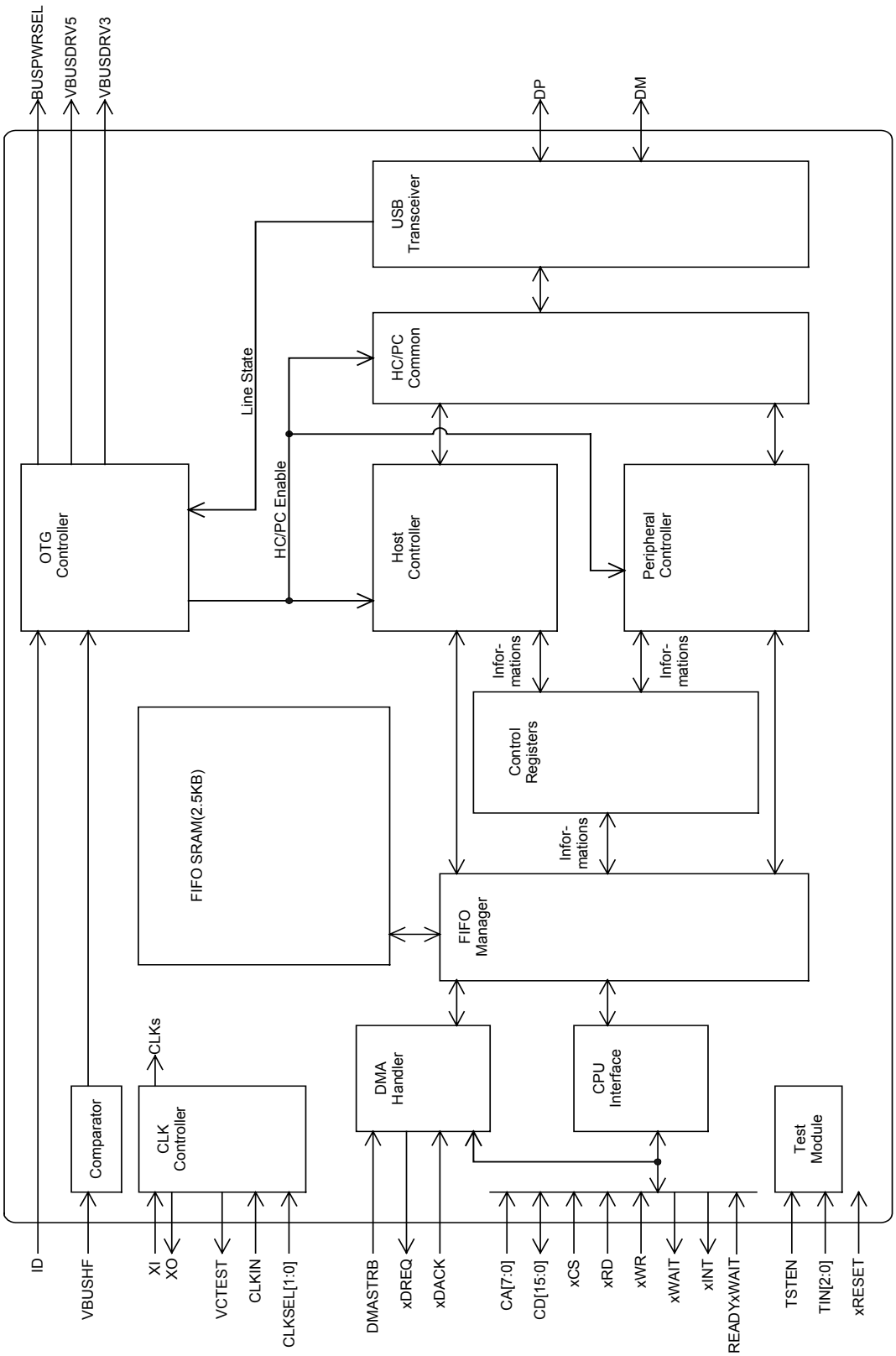
The LSI described in this manual is an On-The-Go device controller LSI compatible with USB 2.0-compliant Full Speed (12 Mbps) mode. Both the Host and Peripheral functions as well as the On-The-Go function are integrated onto a single chip, enabling the LSI to operate as a dual-role device.
In addition to providing universal connectivity between USB devices and a PC, the LSI offers a new feature that permits unprecedented flexibility in the ways in which a USB device can be connected to another USB device. It incorporates a CPU interface power supply (2.8 - 3.3 V) independent of the USB interface power supply (3.3 V), allowing connection to various external CPUs.

2. Features

- Incorporates Host, Peripheral, and On-The-Go functions on a single chip.
- Two I/O power supplies (USB 3.3 V and CPUIF 2.8 - 3.3 V).
- Compliant with the On-The-Go (Supplement to the USB 2.0) 1.0 standard.
- Supports USB 2.0 Full Speed (12 Mbps).
- Provides one On-The-Go port.
- Supports control, bulk, interrupt, and isochronous transfers.
- Controller interface for reduced CPU loads and high throughput during USB transfers.
- Supports Endpoint 0 and five general-purpose endpoints during peripheral operations.
- Built-in 2.5-Kbyte FIFO for data transfers.
- Uses a ring buffer-type FIFO.
- Incorporates a 16-bit wide, general-purpose CPU interface.
- Capable of operating as a 16-bit wide, general-purpose DMA slave (sharing buses with the CPU interface).
- Accepts a 12 MHz resonator for clock input (built-in oscillator circuit).
- Built-in frequency-multiplying PLL circuit.
- Also accepts 12 MHz, 27 MHz, or 48 MHz external clock input from a crystal oscillator.
- Sophisticated clock control for reduced power consumption.
- Housed in an 81-pin CSP or 64-pin QFP package.

* The LSI is not designed to be radiation-resistant.

3. Block Diagram



4. Pin Layout Diagram

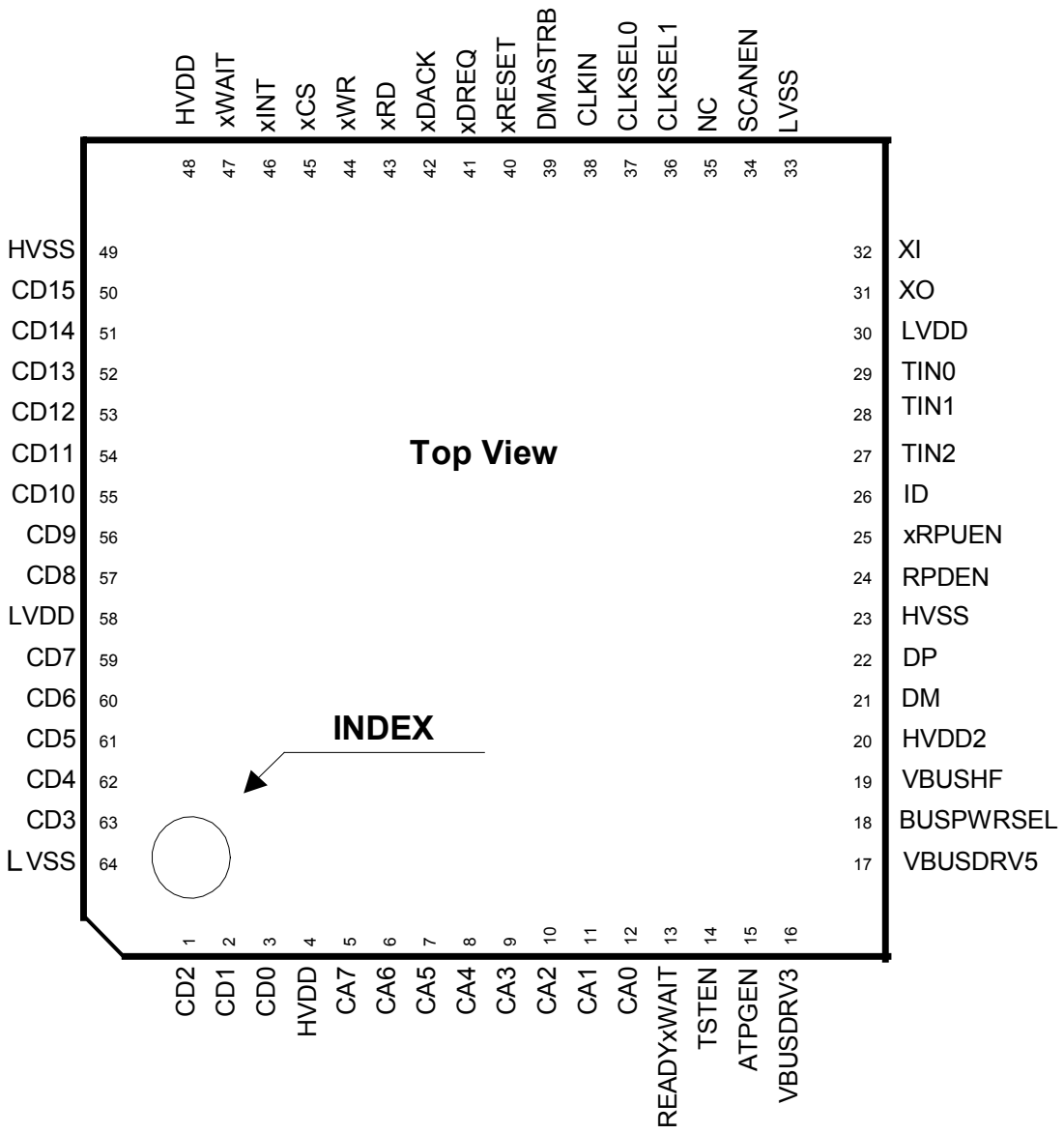
4.1 CSP Package

	1	2	3	4	5	6	7	8	9
J		VBUS DRV5	VBUSHF	DM	RPDEN	ID	LVDD	XI	
H	VBUS DRV3	READYx WAIT	BUS PWRSEL	DP	HVSS	TIN2	XO	TIN0	LVSS
G	TSTEN	ATPGEN	HVDD2			TIN1	CLKSEL 1	SCANEN	
F	CA2	CA1	CA0		XRPUEN			CLKIN	CLKSEL 0
E	CA3	CA4	CA5			COMPIN 22	DMA STRB	XRESET	XDREQ
D	CA7	CA6				COMPIN 10	XWR	XRD	XDACK
C	CD0	CD1	HVDD	CD6	CD10		CD13	XWAIT	XINT
B	CD2	CD5	CD3	CD7	CD9	CD11	CD15	XCS	HVDD
A		LVSS	CD4	LVDD	CD8	CD12	CD14	HVSS	

Bottom View

* The pins READYxWAIT and HVDD and HVDD2 have been modified from the S1R72005B00A100.

4.2 QFP Package



* The pins READYxWAIT and HVDD and HVDD2 have been modified from the S1R72005B00A100.

5. Description of Pin Functions

5.1 CPU Interface

Symbol	Pin Name	Pin Number		Pin Type	Description
		CSP	QFP		
DMASTRB	DMA Strobe	E7	39	I(Gated CMOS)	Strobe signal for burst DMA transfer If unused, connect this pin to GND (HVSS)
xDREQ	DMA Request	E9	41	O(3-state 3mA)	DMA transfer request This is initially in a Hi-Z state. Set the corresponding register to select active-low or active-high settings.
xDACK	DMA Acknowledge	D9	42	I (Gated CMOS)	DMA transfer enable
xRD	Read Strobe	D8	43	I (Gated CMOS)	CPU read strobe
xWR	Write Strobe	D7	44	I (Gated CMOS)	CPU write strobe
xCS	Chip Select	B8	45	I (CMOS)	Chip select signal
xINT	Interrupt signal	C9	46	O(3-state 3mA)	Interrupt signal to the CPU This is initially in a Hi-Z state. Set the corresponding register to select Hi-Z/0 or 1/0.
xWAIT	Wait signal	C8	47	O(3-state 3mA)	Wait signal to the CPU This is initially in a Hi-Z state. Set the corresponding register to select Hi-Z/0 or 1/0.
READYxWAIT	ReadySelect	H2	13	I (CMOS Schmitt)	Apply a high-level input to this pin if xWAIT signal is used in READY mode. This pin is already set, and its state cannot be changed during operations.
CD15 CD14 CD13 CD12 CD11 CD10 CD9 CD8 CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0	CPU Data	B7 A7 C7 A6 B6 C5 B5 A5 B4 C4 B2 A3 B3 B1 C2 C1	50 51 52 53 54 55 56 57 59 60 61 62 63 1 2 3	I/O (Gated CMOS 3mA)	CPU data bus This bus is initially directed for input. Register data is output from this bus during reads. During writes, register data is set by the CPU through this bus. Shared with the DMA data bus.
CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0	CPU Address	D1 D2 E3 E2 E1 F1 F2 F3	5 6 7 8 9 10 11 12	I(Gated CMOS)	CPU address bus This bus is used to specify a register address.

5.2 USB Interface

Symbol	Pin Name	Pin Number		Pin Type	Description
		CSP	QFP		
VBUSDRV3	VBUS Drive	H1	16	O (3mA)	VBUS 3.3 V drive enable 0: Disable; 1: Enable VBUS 3.3 V drive is initially disabled. If unused, leave this pin open.
VBUSDRV5	VBUS Drive	J2	17	O (3mA)	VBUS 5 V drive (max 8 mA) enable 0: Disable; 1: Enable VBUS 5 V drive is initially disabled.
BUSPWRSEL	VBUS Drive	H3	18	O (3mA)	VBUS 5 V drive (over 8 mA) enable 0: Disable; 1: Enable VBUS 5 V drive is initially disabled.
COMPIN10	1.0 V level detection signal	D6	—	I (CMOS with 120 KΩ pull-down)	VBUS/2 level detection result (1.0 V) 0: VBUS/2 < 1.0 V; 1: VBUS/2 ≥ 1.0 V When using the internal comparator, connect this pin to GND.
COMPIN22	2.2 V level detection signal	E6	—	I (CMOS with 120 ΩW pull-down)	VBUS/2 level detection result (2.2 V) 0: VBUS/2 < 2.2 V; 1: VBUS/2 ≥ 2.2 V When using the internal comparator, connect this pin to GND.
DM	USB negative-logic signal	J4	21	I/O (special)	USB data line D-
DP	USB positive-logic signal	H4	22	I/O (special)	USB data line D+
RPDEN	Rpd Enable	J5	24	O (3mA)	D+ pull-down enable 0: Disable; 1: Enable Leave this pin open when using the internal resistor.
xRPUEN	Rpu Enable	F5	25	O (3mA)	D+ pull-up enable 0: Enable; 1: Disable Leave this pin open when using the internal resistor.
ID	ID signal	J6	26	I (CMOS Schmitt with 120 KΩ pull-up)	ID signal 0: A-Device; 1: B-Device
VBUSHF	VBUS/2	J3	19	I (special)	VBUS/2 level Connect this pin to GND when using an external comparator.

5.3 System Related Pins

Symbol	Pin Name	Pin Number		Pin Type	Description
		CSP	QFP		
XO	Resonator output	H7	31	O (special)	Used for output from the internal oscillator circuit If unused, leave this pin open.
XI	Resonator input	J8	32	I (special)	Used for input to the internal oscillator circuit If unused, connect this pin to GND (LVSS) through a pull-down resistor.
CLKSEL1 CLKSEL0	Clock select	G7 F9	36 37	I (CMOS Schmitt)	This pin is used to select the resonator or external clock. CLKSEL[1:0] 00: 12 MHz resonator used 01: External 27 MHz clock input used 10: External 48 MHz clock input used 11: External 12 MHz clock input used
CLKIN	External clock input	F8	38	I(TTL)	External clock input If unused, connect this pin to GND (HVSS). When using external clock input, make sure clock oscillation is stabilized before the LSI emerges from the reset.
XRESET	Chip reset	E8	40	I (CMOS Schmitt with 120 KΩ pull-up)	Chip reset

5.4 Test Signal

Symbol	Pin Name	Pin Number		Pin Type	Description
		CSP	QFP		
TIN2 TIN1 TIN0	Test mode	H6 G6 H8	27 28 29	I (CMOS Schmitt with 120 KΩ pull-down)	Mode setup input pin 000: Normal Other: Internal test mode During normal use, connect this pin to GND (HVSS).
TSTEN	Test enable	G1	14	I (TEST I/O)	Test enable pin 0: Normal; 1: Test During normal use, connect this pin to GND (HVSS).
ATPGEN	Test ATPG	G2	15	I (CMOS Schmitt with 120 KΩ pull-down)	Test pin During normal use, connect this pin to GND (HVSS).
SCANEN	Test SCAN	G8	34	I (CMOS Schmitt with 120 KΩ pull-down)	Test pin During normal use, connect this pin to GND (HVSS).

5.5 Power Supply, GND, Other

Symbol	Pin Name	Pin Number		Pin Type	Description
		CSP	QFP		
HVDD	Power Supply for I/O Part	C3, B9	4, 48	P	2.8 - 3.3 V power supply pin for I/O
HVDD2	Power Supply for USB Part	G3	20	P	3.3 V power supply pin for the USB interface
HVSS	Ground for I/O Part	H5, A8	23, 49	P	Ground pin for I/O
LVDD	Power Supply for Logic part	J7, A4	30, 58	P	2.5 V power supply pin for the internal circuit
LVSS	Ground for Logic part	H9, A2	33, 64	P	Ground pin for the internal circuit
NC	None Connect	C6, D3, D4, D5, E4, E5, F4, F6, F7, G4, G5, G9, A1, A9, J1, J9	35	–	Unused pins Leave these pins open during normal use.

* The pins READYxWAIT and HVDD and HVDD2 have been modified from the S1R72005B00A100.

6. Functional Description

6.1 Host Controller (HC)

- Arbitrates between multiple transactions and performs time management in frames, transfer scheduling, and retransmission management.
- Performs transaction management.
- Generates and disassembles packets.
- Issues instructions for the generation of suspend, resume, and reset states.

6.2 Peripheral Controller (PC)

- Manages endpoint operation information via registers.
- Performs transaction management.
- Generates and disassembles packets.
- Issues instructions for the generation of remote wakeup signals.

6.3 OTG Controller

- Monitors USB data line status (including connect/disconnect status).
- Monitors VBUS levels.
- Monitors the ID.
- Controls VBUS start/stop to execute OTG operations, connects/disconnects pull-up and pull-down resistors (D+), and enables/disables the HC and PC.

6.4 HC/PC Common

- Issues instructions for the generation of USB data line status.
- Switches a USB Transceiver connection to the HC or PC.

6.5 USB Transceiver

- Processes parallel/serial conversion.
- Processes bit stuffing/unstuffing.
- Processes NRZI encoding/decoding.
- Transmits/receives USB data signals.
- Generates USB data line status.

6.6 Control Registers

- Includes a set of registers for transaction and endpoint control.

6.7 FIFO Manager

- Manages addresses for FIFO access by CPU/DMA and USB.
- Arbitrates FIFO access by CPU/DMA and USB.

6.8 FIFO SRAM

- Used as data transfer FIFO (total 2.5 Kbytes).

6.9 CPU I/F

- Controls PIO transfers.
- Generates interrupt signals to the CPU.

6.10 DMA Handler

- Controls DMA transfers (DMA slave).

6.11 CLK Controller

- Generates various internally used clocks from the frequency-multiplying PLL (when a resonator is used) or an external input clock.
- Controls the operation of clocks used in each circuit block.

6.12 Test Module

- Performs test to verify LSI internal operations.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

(VSS=0V)

Parameter	Symbol	Rated Value	Unit
Power Supply Voltage	HVDD*	-0.3 - 4.0	V
	HVDD2	-0.3 - 4.0	V
	LVDD*	-0.3 - 3.0	V
Input Voltage	HVI1	-0.3 - HVDD+0.5	V
	HVI2	-0.3 - HVDD2+0.5	V
	LVI	-0.3 - LVDD+0.5	V
Output Voltage	HVO1	-0.3 - HVDD+0.5	V
	HVo2	-0.3 - HVDD2+0.5	V
	LVO	-0.3 - LVDD+0.5	V
Output Current per Pin	IOUT	±30	mA
Storage Temperature	Tstg	-65 - 150	°C

*HVDD2, HVDD ≥ LVDD

7.2 Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	HVDD2	3.00	3.30	3.60	V
	HVDD	2.70	–	3.60	V
	LVDD	2.30	2.50	2.70	V
Input Voltage	HVI1	VSS	–	HVDD	V
	HVI2	VSS	–	HVDD	V
	LVI	VSS	–	LVDD	V
Ambient Temperature	Ta	-40	25	85	°C

7.3 D.C. Characteristics

D.C. Characteristics (under Recommended Operating Conditions) (1)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption						
Power Supply Current	IDDH	HVDD = 3.6V	-	-	10	mA
	IDDH2	HVDD2 = 3.6V	-	-	10	mA
	IDDL	LVDD = 2.7V	-	-	40	mA
Quiescent Current (quiescent current between HVDD and VSS)						
Power Supply Current	IDDSH	VIN = HVDD or HVDD2 or VSS HVDD = 3.6V LVDD = 2.7V	-	-	30	μA
Quiescent Current (quiescent current between HVDD2 and VSS)						
Power Supply Current	IDDSH2	VIN = HVDD or HVDD2 or VSS HVDD2 = 3.6V LVDD = 2.7V	-	-	30	μA
Quiescent Current (quiescent current between LVDD and VSS)						
Power Supply Current	IDDSL	VIN = HVDD or HVDD2 or VSS HVDD = 3.6V LVDD = 2.7V	-	-	60	μA
Input Leakage						
Input Leakage Current	IL	VIN = HVDD or HVDD2 or VSS HVDD = 3.6V HVDD = 3.6V LVDD = 2.7V HVIH = HVDD LVIL = LVDD VIL = VSS	-5	-	5	μA

D.C. Characteristics (under Recommended Operating Conditions) (2)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Characteristics (CMOS)	Pin name:	CA7..CA0, CD15..CD0, TSTEN, xCS, xDACK, xRD, xWR, DMASTRB, COMPIN10, COMPIN22				
High Level Input Voltage	VIH1H	HVDD = 3.6V	2.2	-	-	V
Low Level Input Voltage	VIL1H	HVDD = 2.7V	-	-	0.8	V
Schmitt Input Characteristics (CMOS)	Pin name:	xRESET, CLKSEL1, CLKSEL0, TIN2, TIN1, TIN0, SCANEN, ATPGEN				
High Level Trigger Voltage	VT1+	HVDD = 3.6V	1.4	-	2.7	V
Low Level Trigger Voltage	VT1-	HVDD = 2.7V	0.6	-	1.8	V
Hysteresis Voltage	△V1	HVDD = 2.7V	0.3	-	-	V
Schmitt Input Characteristics (CMOS)	Pin name:	ID				
High Level Trigger Voltage	VT2+	HVDD2 = 3.6V	1.4	-	2.7	V
Low Level Trigger Voltage	VT2-	HVDD2 = 3.0V	0.6	-	1.8	V
Hysteresis Voltage	△V2	HVDD2 = 3.0V	0.3	-	-	V
Input Characteristics (VLTTL)	Pin name:	CLKIN				
High Level Input Voltage	VIH2H	HVDD = 3.6V	2.0	-	-	V
Low Level Input Voltage	VIL2H	HVDD = 2.7V	-	-	0.8	V
Schmitt Input Characteristics (USB: FS)	Pin name:	DP, DM				
High Level Trigger Voltage	VT+(USB)	HVDD2 = 3.6V	1.1	-	1.8	V
Low Level Trigger Voltage	VT-(USB)	HVDD2 = 3.0V	1.0	-	1.5	V
Hysteresis Voltage	△V(USB)	HVDD2 = 3.0V	0.1	-	-	V
Input Characteristics (USB: FS differential input)	Pin name:	PD and DM in pairs				
Sensitivity of Differential Input		HVDD2 = 3.0V				
	VDS(USB)	Differential input voltage 0.8V - 2.5V	-	-	0.2	V
Input Pull-up Characteristics	Pin name:	xRESET				
~~Pull-up Resistance Value~~	~~RPU2~~	~~HVDD = 3.3V~~	~~60~~	~~120~~	~~288~~	~~kΩ~~
		~~VIH = VSS~~				
Input Pull-up Characteristics	Pin name:	ID				
Pull-up Resistance Value	RPU2	HVDD2 = 3.3V VIH = VSS	60	120	288	kΩ
Input Pull-down Characteristics	Pin name:	SCANEN, ATPGEN, TIN2, TIN1, TIN0, COMPIN10, COMPIN22				
Pull-down Resistance Value	RPD2	HVDD = 3.3V VIH = VSS	60	120	288	kΩ

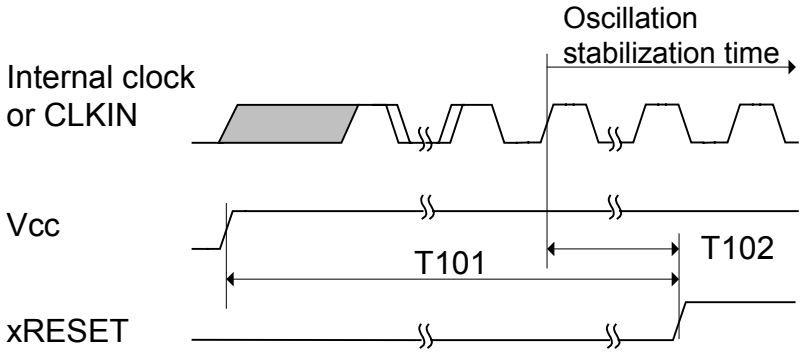
D.C. Characteristics (under Recommended Operating Conditions) (3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Characteristics	Pin name:	CD15..CD0, xINT, xWAIT, xDREQ				
High Level Output Voltage	VOH1H	HVDD = 2.7V IOH = -3mA	VDD-0.4	-	-	V
Low Level Output Voltage	VOL1H	HVDD = 2.7V IOL = 3mA	-	-	0.4	V
Output Characteristics	Pin name:	xRPUEN, RPDEN, VBUSDRV3, VBUSDRV5,BUSPWRSEL				
High Level Output Voltage	VOH1H	HVDD = 3.0V IOH = -3mA	VDD-0.4	-	-	V
Low Level Output Voltage	VOL1H	HVDD = 3.0V IOL = 3mA	-	-	0.4	V
Output Characteristics (USB: FS)	Pin name:	DP, DM				
High Level Output Voltage	VOH(USB)	HVDD = 3.0V	2.8	-	-	V
Low Level Output Voltage	VOL(USB)	HVDD = 3.6V	-	-	0.3	V
Output Characteristics	Pin name:	xRPUEN, RPDEN, VBUSDRV3, VBUSDRV5, BUSPWRSEL, CD15..CD0, xINT, xWAIT, xDREQ				
Off-State Leakage Current	IOZ1H	HVDD = 3.6V VOH = VDD VOL = VSS	-5	-	5	μA
Pin Capacitance	Pin name:	All input pins				
Input Pin Capacitance	CI	f = 1MHz VDD = VSS	-	-	8	pF
Pin Capacitance	Pin name:	All output pins				
Output Pin Capacitance	CO	f = 1MHz VDD = VSS	-	-	8	pF
Pin Capacitance	Pin name:	All input/output pins				
Input/Output Pin Capacitance	CIO	f = 1MHz VDD = VSS	-	-	8	pF

7.4 A.C. Characteristics

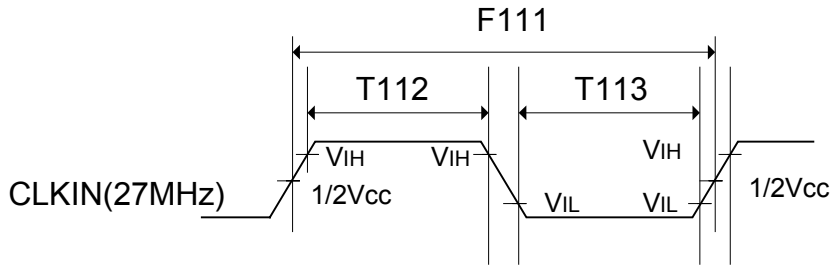
7.4.1 Clock Timing

7.4.1.1 Power-On Oscillation Stabilization Time



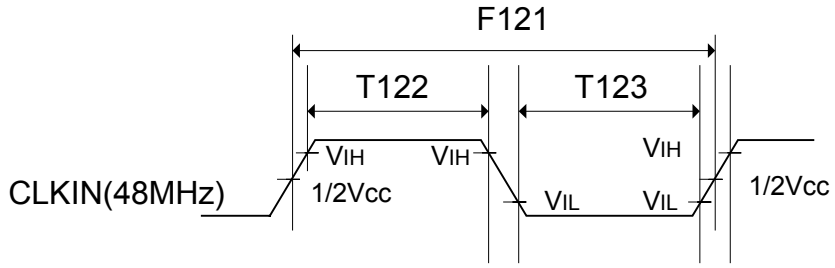
Symbol	Description	Min.	Typ.	Max.	Unit
T101	Power-on oscillation stabilization time	10	-	-	ms
T102	XRESET setup time	200	-	-	us

7.4.1.2 CLKIN (27 MHz) Clock Input Timing



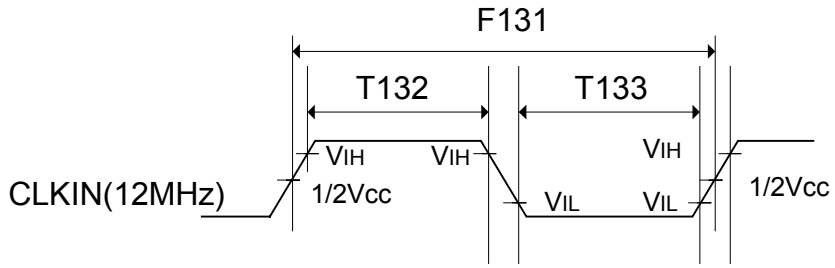
Symbol	Description	Min.	Typ.	Max.	Unit
F111	Clock input frequency	26.933	27.000	27.068	MHz
T112	Clock input high-level pulse width	12	-	23	ns
T113	Clock input low-level pulse width	12	-	23	ns

7.4.1.3 CLKIN (48 MHz) Clock Input Timing



Symbol	Description	Min.	Typ.	Max.	Unit
F121	Clock input frequency (center frequency)	47.880	48	48.120	MHz
T122	Clock input high-level pulse width	7	-	13	ns
T123	Clock input low-level pulse width	7	-	13	ns

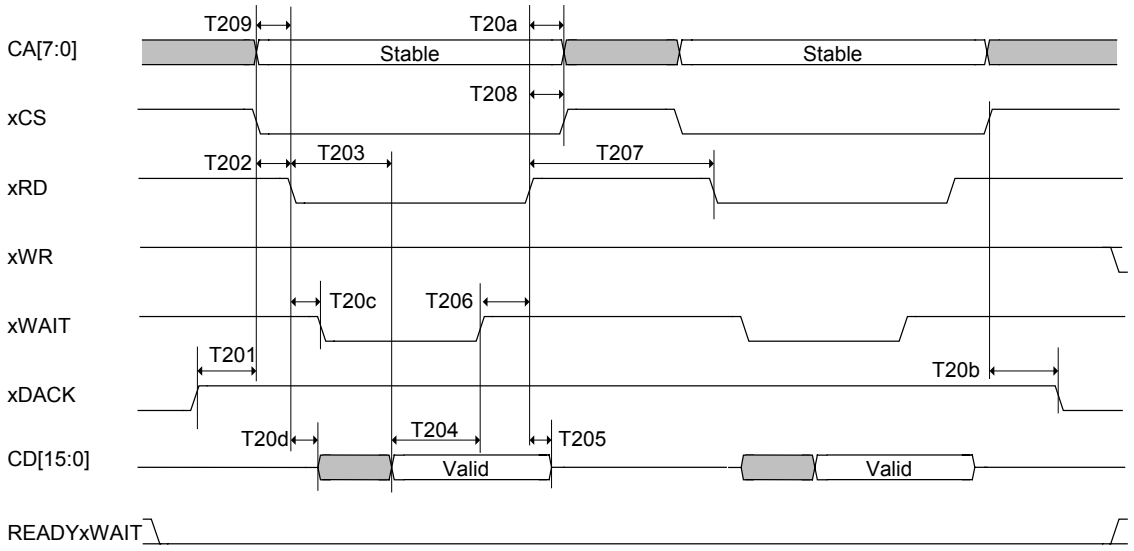
7.4.1.4 CLKIN (12 MHz) Clock Input Timing



Symbol	Description	Min.	Typ.	Max.	Unit
F131	Clock input frequency (center frequency)	11.970	12.000	12.030	MHz
T132	Clock input high-level pulse width	28	-	52	ns
T133	Clock input low-level pulse width	28	-	52	ns

7.4.2 CPU Interface Access Timing

7.4.2.1 Read Timing (External xWAIT Mode)

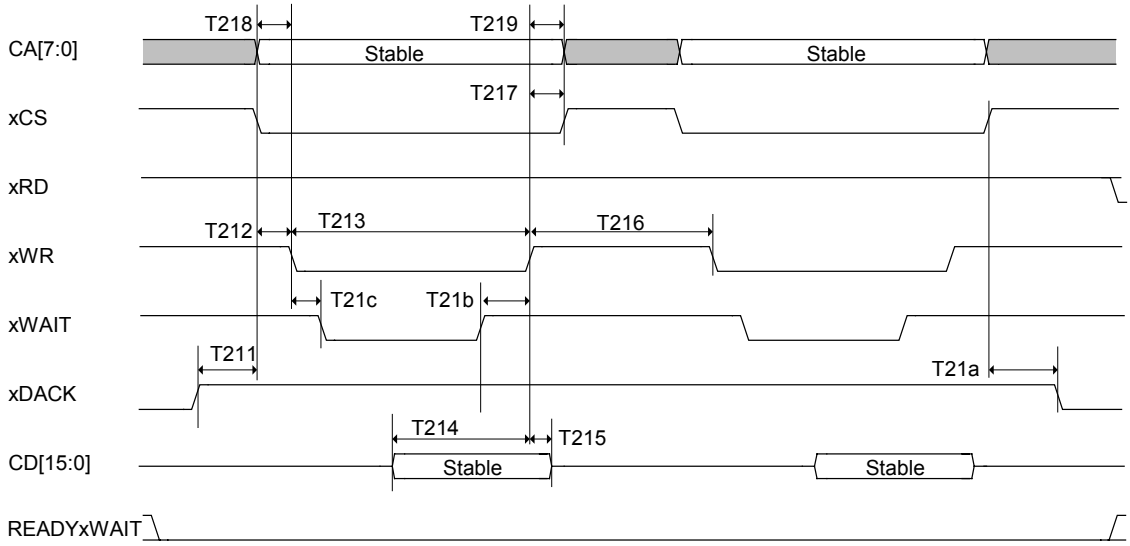


Symbol	Description	Min.	Typ.	Max.	Unit
T201	xCS assert time relative to xDACK negate	10	-	-	ns
T202	xRD assert time relative to xCS assert	0	-	-	ns
T203	CD valid data delay time relative to xRD assert (Note 1)	-	-	62.5	ns
T204	xWAIT negate time relative to CD output	20	-	-	ns
T205	CD output hold time relative to xRD negate	2.5	-	-	ns
T206	xRD negate time relative to xWAIT negate	0	-	-	ns
T207	xRD negate time	25	-	-	ns
T208	xCS negate time relative to xRD negate	0	-	-	ns
T209	CA setup time relative to xRD assert	0	-	-	ns
T20a	CA hold time relative to xRD negate	0	-	-	ns
T20b	xDACK assert time relative to xCS negate	10	-	-	ns
T20c	xWAIT assert time relative to xRD assert	-	-	8	ns
T20d	CD output delay time relative to xRD assert	-	-	8	ns

Note 1:

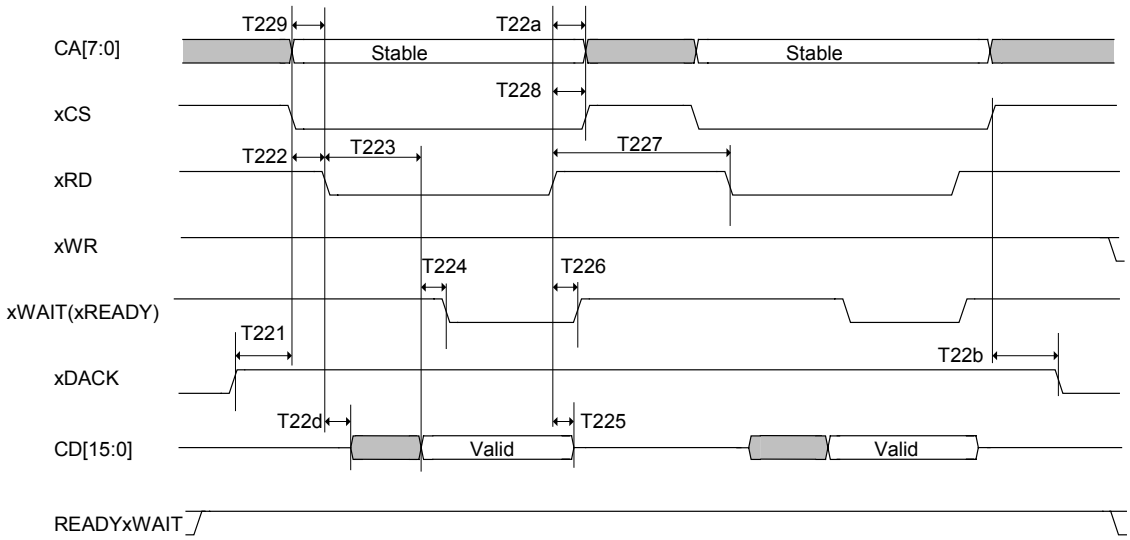
This delay is stipulated for ordinary register access (not including access to the “FIFOforCPU” register). The data output delay time may be extended during access to the FIFOforCPU register, depending on contention for access to internal FIFO memory.

7.4.2.2 Write Timing (External xWAIT Mode)



Symbol	Description	Min.	Typ.	Max.	Unit
T211	xCS assert time relative to xDACK negate	10	-	-	ns
T212	xWR assert time relative to xCS assert	0	-	-	ns
T213	xWR assert pulse width	32	-	-	ns
T214	CD setup time relative to xWR negate	10	-	-	ns
T215	CD hold time relative to xWR negate	0	-	-	ns
T216	xWR negate time	25	-	-	ns
T217	xCS negate time relative to xWR negate	0	-	-	ns
T218	CA setup time relative to xWR assert	0	-	-	ns
T219	CA hold time relative to xWR negate	0	-	-	ns
T21a	xDACK assert time relative to xCS negate	10	-	-	ns
T21b	xWR negate time relative to xWAIT negate	0	-	-	ns
T21c	xWAIT assert time relative to xWR assert (Note 2)	-	-	8	ns

7.4.2.3 Read Timing (External xREADY Mode)

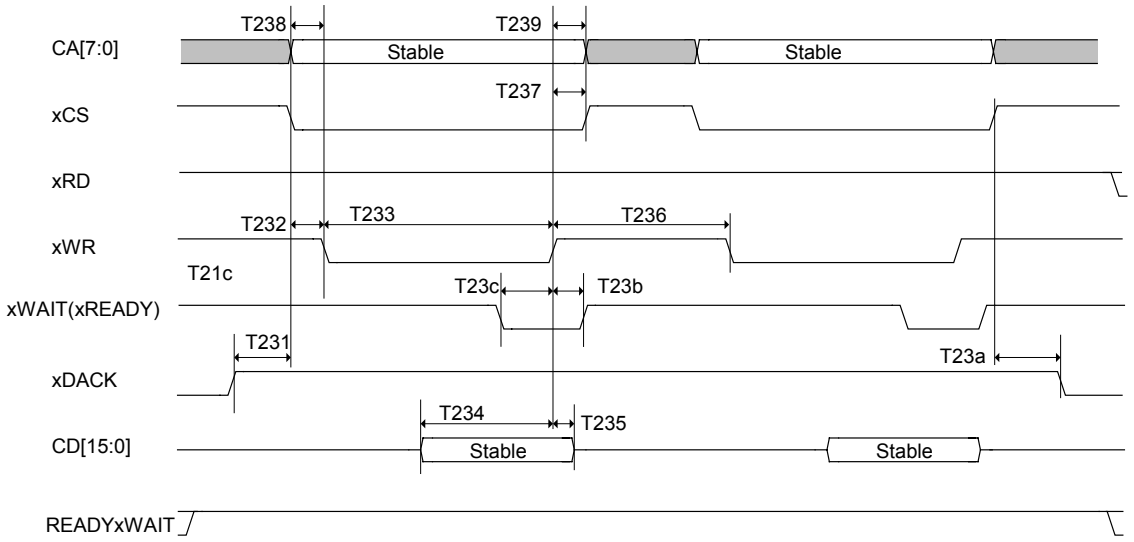


Symbol	Description	Min.	Typ.	Max.	Unit
T221	xCS assert time relative to xDACK negate	10	-	-	ns
T222	xRD assert time relative to xCS assert	0	-	-	ns
T223	CD valid data delay time relative to xRD assert (Note 1)	-	-	62.5	ns
T224	xREADY assert time relative to CD output	15	-	-	ns
T225	CD output hold time relative to xRD negate	2.5	-	-	ns
T226	xREADY negate time relative to xRD negate		-	8	ns
T227	xRD negate period	25	-	-	ns
T228	xCS negate time relative to xRD negate	0	-	-	ns
T229	CA setup time relative to xRD assert	0	-	-	ns
T22a	CA hold time relative to xRD negate	0	-	-	ns
T22b	xDACK assert time relative to xCS negate	10	-	-	ns
T22c	-	-	-	-	ns
T22d	CD output delay time relative to xRD assert	-	-	8	ns

Note 1:

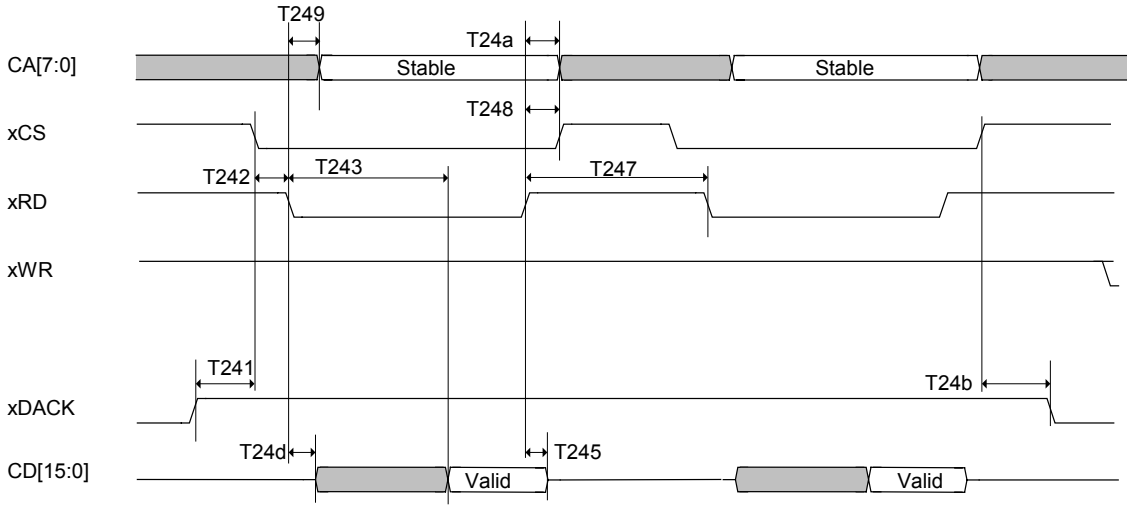
This delay is stipulated for ordinary register access (not including access to the “FIFOforCPU” register). The data output delay time may be extended during access of the FIFOforCPU register, depending on contention for access to internal FIFO memory.

7.4.2.4 Write Timing (External xREADY Mode)



Symbol	Description	Min.	Typ.	Max.	Unit
T231	xCS assert time relative to xDACK negate	10	-	-	ns
T232	xWR assert time relative to xCS assert	0	-	-	ns
T233	xWR assert pulse width	32	-	-	ns
T234	CD setup time relative to xWR negate	10	-	-	ns
T235	CD hold time relative to xWR negate	0	-	-	ns
T236	xWR negate period	25	-	-	ns
T237	xCS negate time relative to xWR negate	0	-	-	ns
T238	CA setup time relative to xWR assert	0	-	-	ns
T239	CA hold time relative to xWR negate	0	-	-	ns
T23a	xDACK assert time relative to xCS negate	10	-	-	ns
T23b	xREADY negate time relative to xWR negate	-	-	8	ns
T23c	xWR negate time relative to xREADY assert	0	-	-	ns

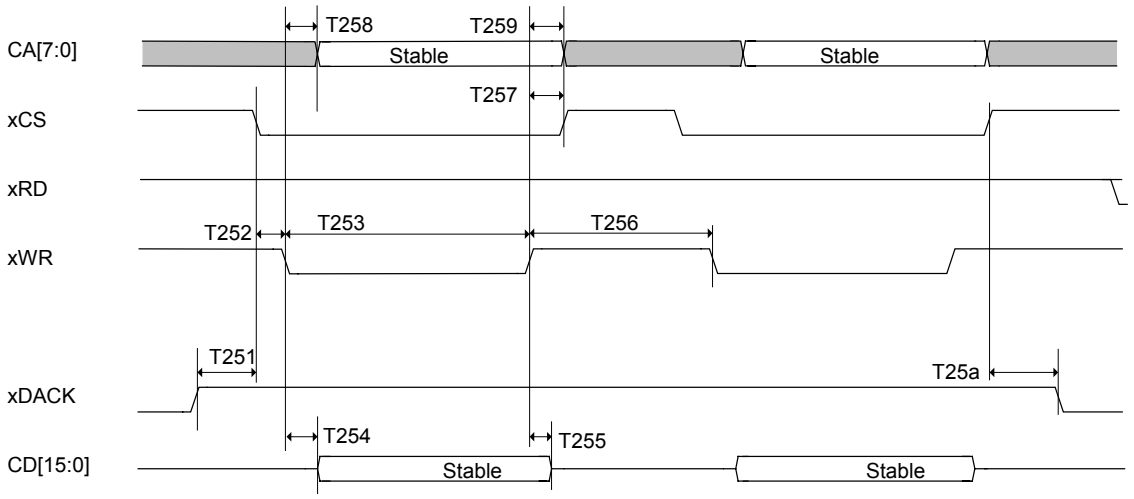
7.4.2.5 Read Timing (Fixed WAIT Mode)



Symbol	Description	Min.	Typ.	Max.	Unit
T241	xCS assert time relative to xDACK negate	10	-	-	ns
T242	xRD assert time relative to xCS assert	0	-	-	ns
T243	CD valid data output delay time relative to xRD assert	-	-	110	ns
T244	-	-	-	-	ns
T245	CD output hold time relative to xRD negate	2.5	-	-	ns
T246	-	-	-	-	ns
T247	xRD negate period	25	-	-	ns
T248	xCS negate time relative to xRD negate	0	-	-	ns
T249	CA valid delay time relative to xRD assert	-	-	10	ns
T24a	CA hold time relative to xRD negate	0	-	-	ns
T24b	xDACK assert time relative to xCS negate	10	-	-	ns
T24c	-	-	-	-	ns
T24d	CD output delay time relative to xRD assert	-	-	8	ns

- The S1R72005's CPUConfig register is used to select fixed WAIT mode.
- This LSI is designed to operate in external xWAIT mode after power-on reset.
- Since xWAIT is not output during access to the CPUConfig register, data can be written to the register from a CPU that does not have xWAIT.
- If the external WAIT pin is unused, the CPU must be assigned an appropriate software wait when accessing, to ensure that it can access this device with the above timing.

7.4.2.6 Write Timing (Fixed WAIT Mode)

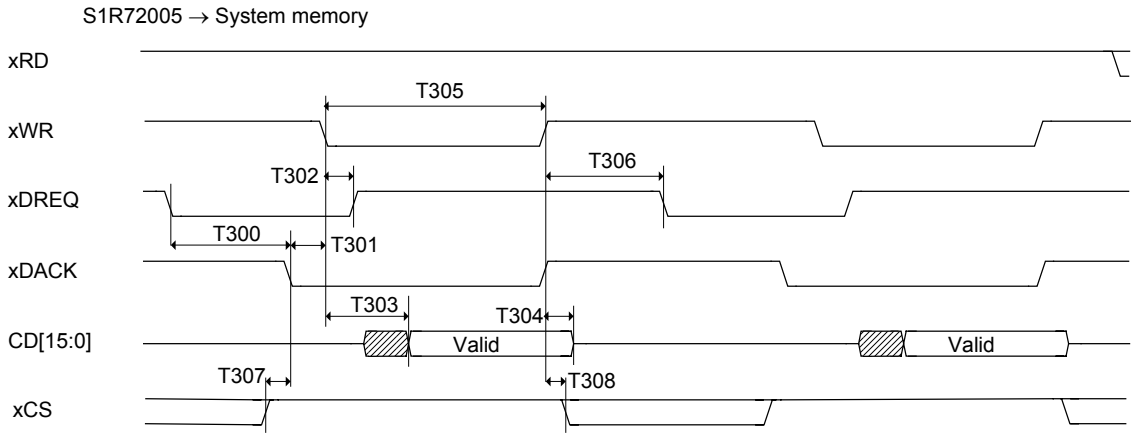


Symbol	Description	Min.	Typ.	Max.	Unit
T251	xCS assert time relative to xDACK negate	10	-	-	ns
T252	xWR assert time relative to xCS assert	0	-	-	ns
T253	xWR assert pulse width	110	-	-	ns
T254	CD valid delay time relative to xWR assert	-	-	20	ns
T255	CD hold time relative to xWR negate	0	-	-	ns
T256	xWR negate period	25	-	-	ns
T257	xCS negate time relative to xWR negate	0	-	-	ns
T258	CA valid delay time relative to xWR assert	0	-	-	ns
T259	CA hold time relative to xWR negate	0	-	-	ns
T25a	xDACK assert time relative to xCS negate	10	-	-	ns

- The S1R72005's CPUConfig register is used to select fixed WAIT mode.
- This LSI is designed to operate in external xWAIT mode after power-on reset.
- Since xWAIT is not output during access to the CPUConfig register, data can be written to the register from a CPU that does not have xWAIT.
- If the external WAIT pin is unused, the CPU must be assigned an appropriate software wait when accessing, to ensure that it can access this device with the above timing.

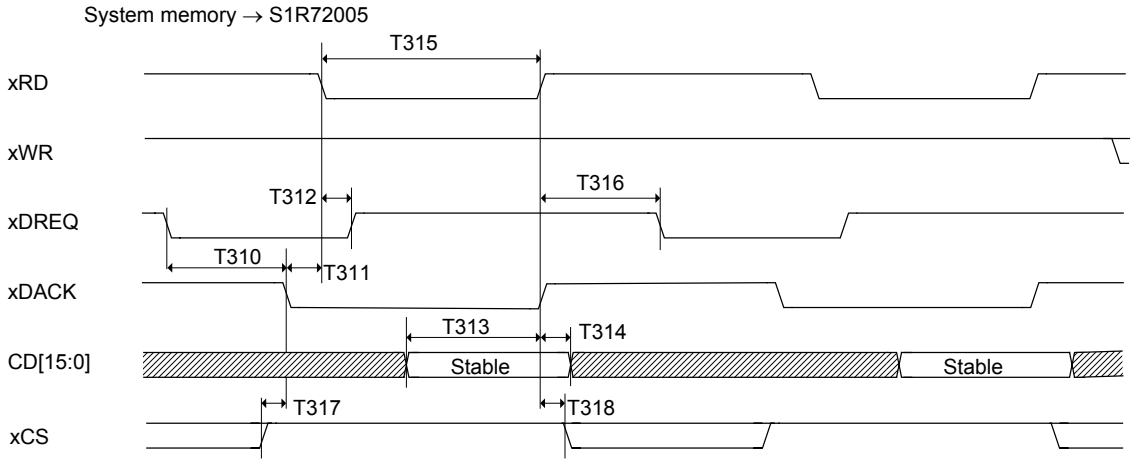
7.4.3 DMA Timing

7.4.3.1 xRD and xWR Strobe Mode (DMAOUT)



Symbol	Description	Min.	Typ.	Max.	Unit
T300	xDACK assert time relative to xDREQ assert	0	-	-	ns
T301	xWR assert time relative to xDACK assert	0	-	-	ns
T302	xDREQ negate time relative to xWR assert	-	-	10	ns
T303	Data output delay time relative to xWR assert	-	-	8	ns
T304	Data hold time relative to xWR negate	2	-	-	ns
T305	xWR assert pulse width	42	-	-	ns
T306	xDREQ assert time relative to xWR negate	160	-	-	ns
T307	xDACK assert time relative to xCS negate	0	-	-	ns
T308	xCS assert time relative to xDACK negate	0			ns

7.4.3.2 xRD and xWR Strobe Mode (DMAIN)

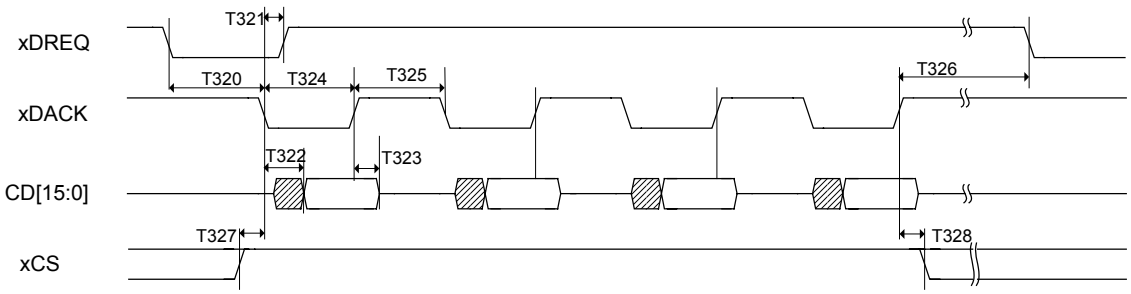


Symbol	Description	Min.	Typ.	Max.	Unit
T310	xDACK assert time relative to xDREQ assert	0	-	-	ns
T311	xRD assert time relative to xDACK assert	0	-	-	ns
T312	xDREQ negate time relative to xRD assert	-	-	10	ns
T313	Data setup time relative to xRD negate	10	-	-	ns
T314	Data hold time relative to xRD negate	0	-	-	ns
T315	xRD assert pulse width	42	-	-	ns
T316	xDREQ assert time relative to xRD negate	160	-	-	ns
T317	xDACK assert time relative to xCS negate	0	-	-	ns
T318	xCS assert time relative to xDACK negate	0	-	-	ns

7.4.3.3 DACK Strobe Mode (DMAOUT)

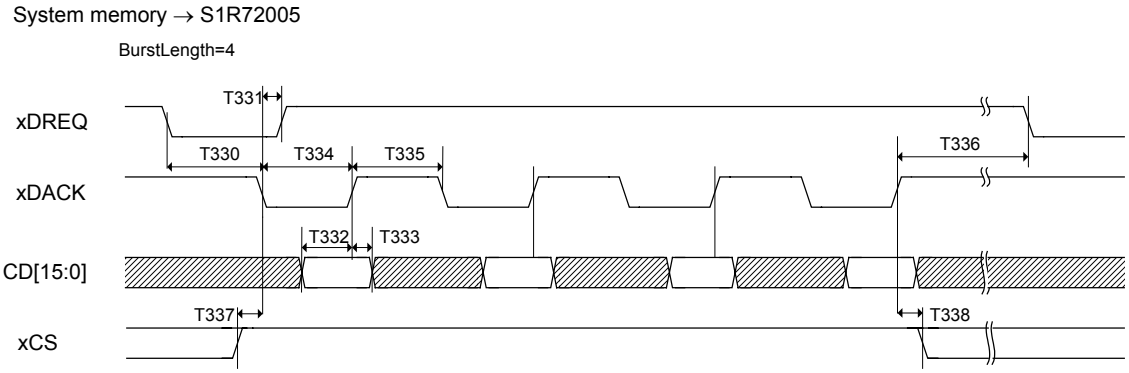
S1R72005 → System memory

BurstLength=4



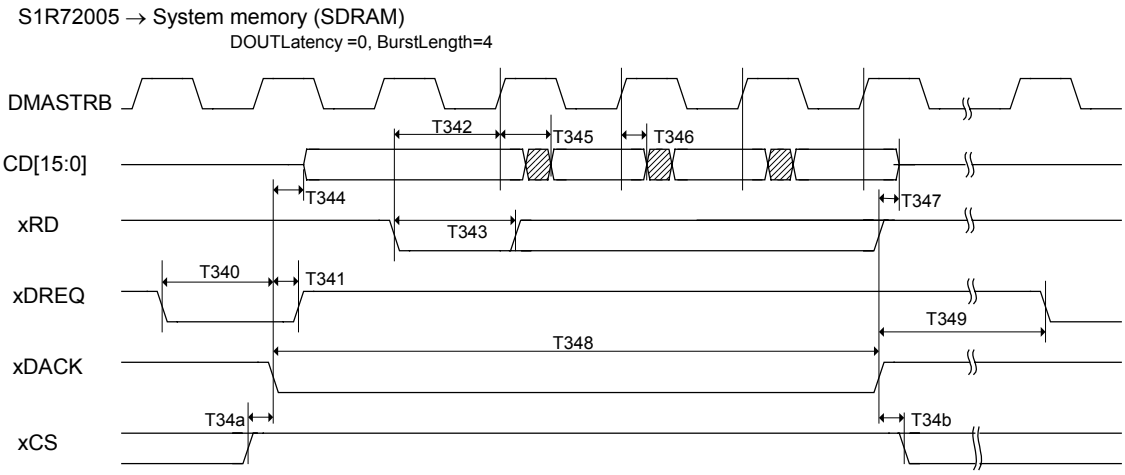
Symbol	Description	Min.	Typ.	Max.	Unit
T320	xDACK assert time relative to xDREQ assert	0	-	-	ns
T321	xDREQ negate time relative to xDACK assert	-	-	10	ns
T322	Data output delay time relative to xDACK assert	-	-	7	ns
T323	Data hold time relative to xDACK negate	2	-	-	ns
T324	xDACK assert pulse width	42	-	-	ns
T325	xDACK negate pulse width	42	-	-	ns
T326	xDREQ assert time relative to xDACK negate	160	-	-	ns
T327	xDACK assert time relative to xCS negate	0	-	-	ns
T328	xCS assert time relative to xDACK negate	0	-	-	ns

7.4.3.4 DACK Strobe Mode (DMAIN)



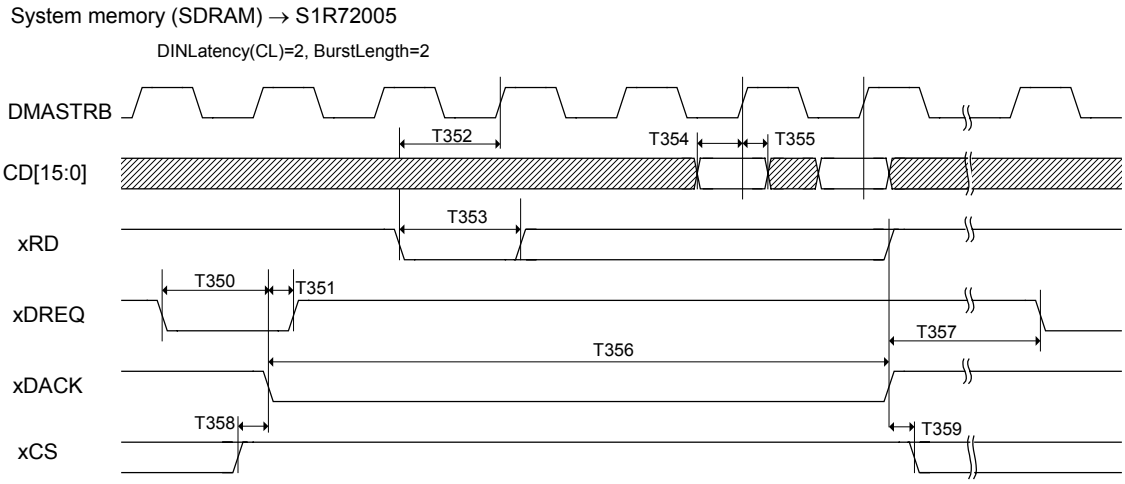
Symbol	Description	Min.	Typ.	Max.	Unit
T330	xDACK assert time relative to xDREQ assert	0	-	-	ns
T331	xDREQ negate time relative to xDACK assert	-	-	10	ns
T332	Data setup time relative to xDACK negate	10	-	-	ns
T333	Data hold time relative to xDACK negate	0	-	-	ns
T334	xDACK assert pulse width	42	-	-	ns
T335	xDACK negate pulse width	42	-	-	ns
T336	xDREQ assert time relative to xDACK negate	160	-	-	ns
T337	xDACK assert time relative to xCS negate	0	-	-	ns
T338	xCS assert time relative to xDACK negate	0	-	-	ns

7.4.3.5 DMASTRB SDRAM Mode (DMAOUT)



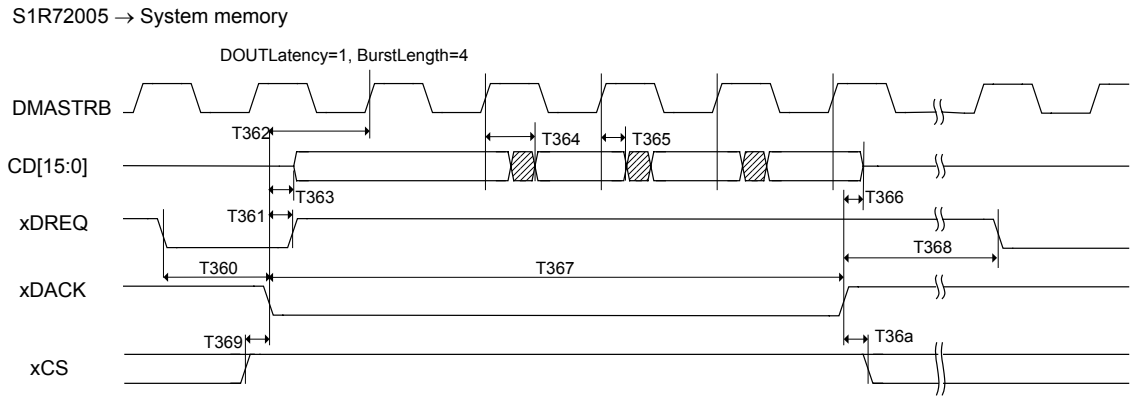
Symbol	Description	Min.	Typ.	Max.	Unit
T340	xDACK assert time relative to xDREQ assert	0	-	-	ns
T341	xDREQ negate time relative to xDACK assert	-	-	10	ns
T342	DMASTRB active edge time relative to xRD (~CAS) assert	3	-	-	ns
T343	xRD (~CAS) assert pulse width	1T (DMASTRB)	-	-	ns
T344	Data output delay time relative to xDACK assert	-	-	7	ns
T345	Data output delay time relative to DMASTRB active edge	-	-	9	ns
T346	Data hold time relative to DMASTRB active edge	4	-	-	ns
T347	Data hold time relative to xDACK negate	2	-	-	ns
T348	xDACK assert pulse width	42	-	-	ns
T349	xDREQ assert time relative to xDACK negate	160	-	-	ns
T34a	xDACK assert time relative to xCS negate	0	-	-	ns
T34b	xCS assert time relative to xDACK negate	0	-	-	ns

7.4.3.6 DMASTRB SDRAM Mode (DMAIN)



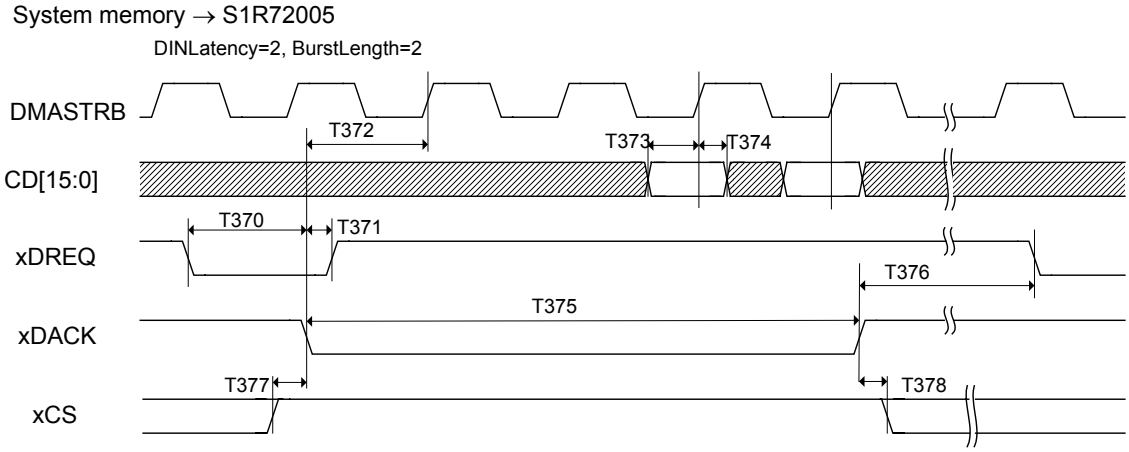
Symbol	Description	Min.	Typ.	Max.	Unit
T350	xDACK assert time relative to xDREQ assert	0	-	-	ns
T351	xDREQ negate time relative to xDACK assert	-	-	10	ns
T352	DMASTRB active edge time relative to xRD (~CAS) assert	3	-	-	ns
T353	xRD (~CAS) assert pulse width	1T (DMASTRB)	-	-	ns
T354	Data setup time relative to DMASTRB active edge	10	-	-	ns
T355	Data hold time relative to DMASTRB active edge	0	-	-	ns
T356	xDACK assert pulse width	42	-	-	ns
T357	xDREQ assert time relative to xDACK negate	160	-	-	ns
T358	xDACK assert time relative to xCS negate	0	-	-	ns
T359	xCS assert time relative to xDACK negate	0	-	-	ns

7.4.3.7 DMASTRB General-Purpose Mode (DMAOUT)



Symbol	Description	Min.	Typ.	Max.	Unit
T360	xDACK assert time relative to xDREQ assert	0	-	-	ns
T361	xDREQ negate time relative to xDACK assert	-	-	10	ns
T362	DMASTRB active edge time relative to xDACK assert	3	-	-	ns
T363	Data output delay time relative to xDACK assert	-	-	7	ns
T364	Data output delay time relative to DMASTRB active edge	-	-	9	ns
T365	Data hold time relative to DMASTRB active edge	4	-	-	ns
T366	Data hold time relative to xDACK negate	2	-	-	ns
T367	xDACK assert pulse width	42	-	-	ns
T368	xDREQ assert time relative to xDACK negate	160	-	-	ns
T369	xDACK assert time relative to xCS negate	0	-	-	ns
T36a	xCS assert time relative to xDACK negate	0	-	-	ns

7.4.3.8 DMASTRB General-Purpose Mode (DMAIN)



Symbol	Description	Min.	Typ.	Max.	Unit
T370	xDACK assert time relative to xDREQ assert	0	-	-	ns
T371	xDREQ negate time relative to xDACK assert	-	-	10	ns
T372	DMASTRB active edge time relative to xDACK assert	3	-	-	ns
T373	Data setup time relative to DMASTRB active edge	10	-	-	ns
T374	Data hold time relative to DMASTRB active edge	0	-	-	ns
T375	xDACK assert pulse width	42	-	-	ns
T376	xDREQ assert time relative to xDACK negate	160	-	-	ns
T377	xDACK assert time relative to xCS negate	0	-	-	ns
T378	xCS assert time relative to xDACK negate	0	-	-	ns

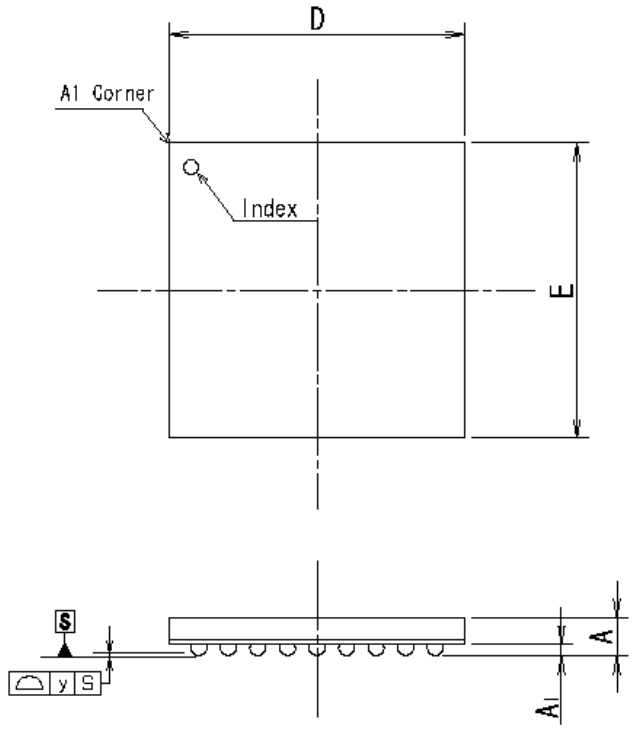
7.4.4 USB Interface Timing

Compliant with USB 2.0 standard.

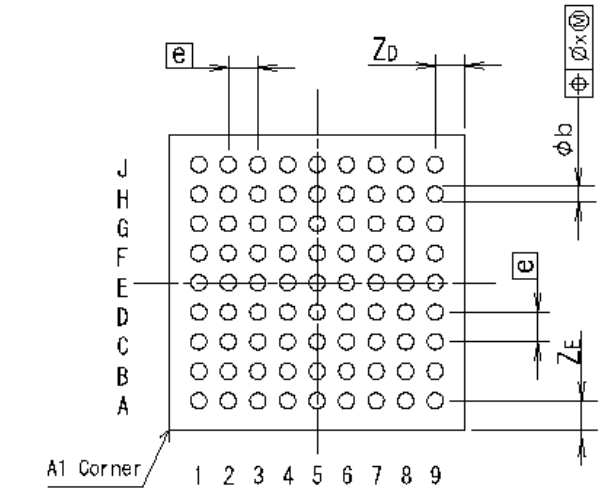
8. Package Dimensions

8.1 CSP Package

Top View



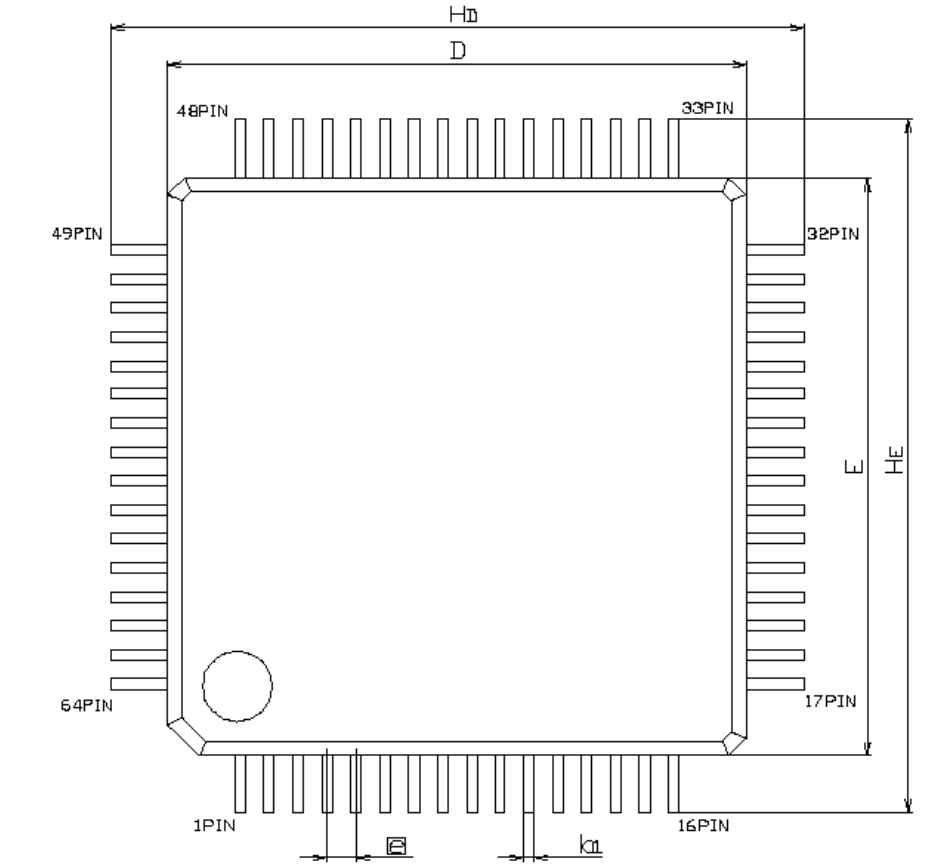
Bottom View

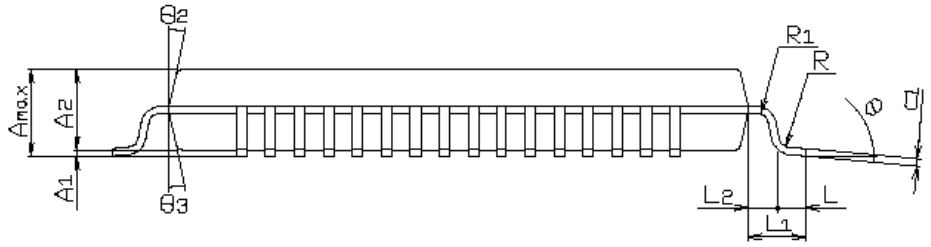


Symbol	Dimension in Millmeters		
	Min	Nom	Max
D	7.80	8.0	8.2
E	7.80	8.0	8.2
A			1.20
A1	0.25	0.30	0.35
e		0.80	
b	0.38	0.43	0.48
X			0.08
Y			0.10
ZD		0.80	
ZE		0.80	

1 = 1mm

8.2 QFP Package





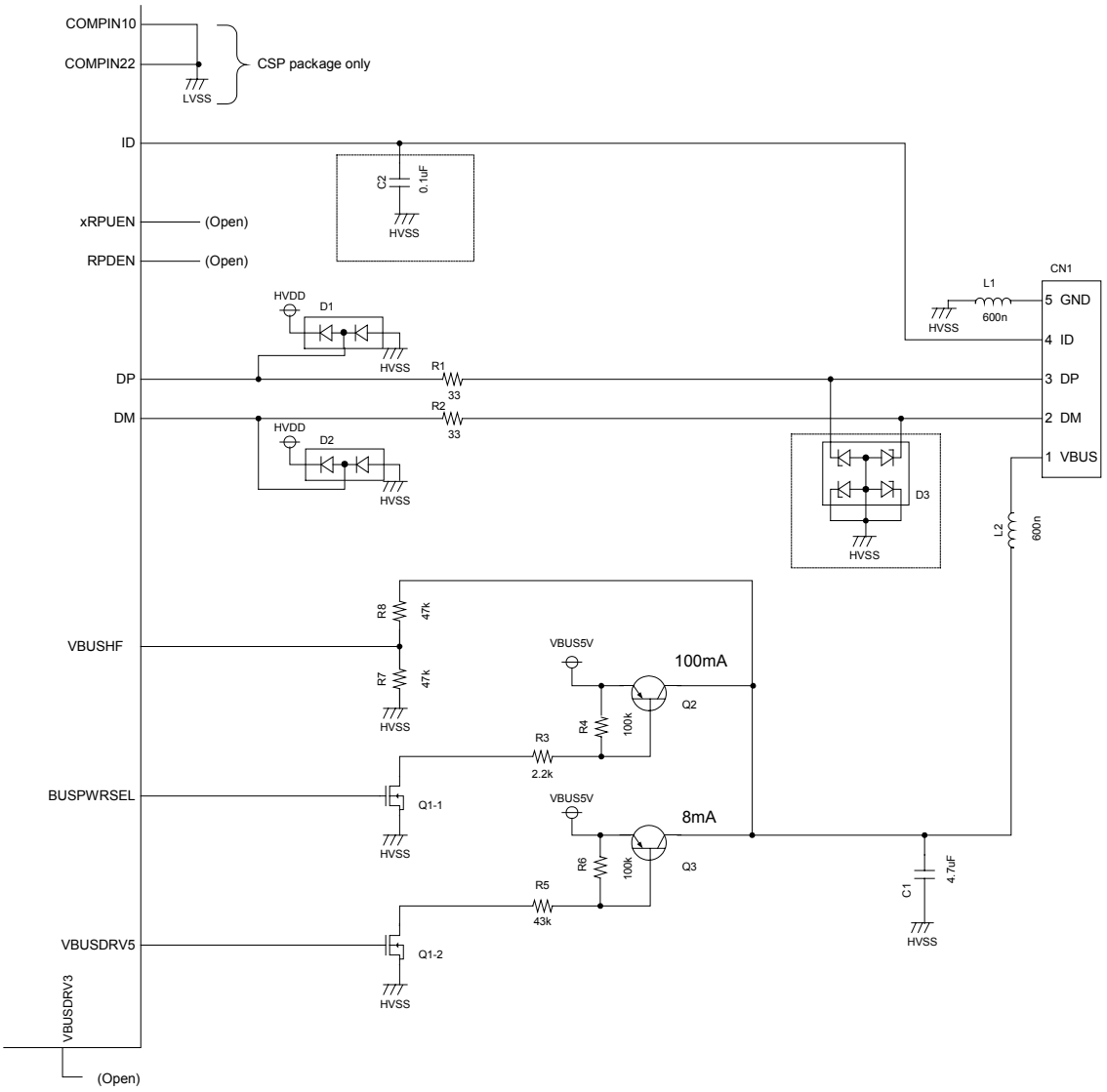
Symbol	Dimension in Millmeters		
	Min	Nom	Max
E	9.9	10	10.1
D	9.9	10	10.1
Amax			1.7
A1		0.1	
A2	1.3	1.4	1.5
e		0.5	
b1	0.13	0.18	0.28
c1	0.1	0.125	0.175
θ	0°		10°
L	0.3	0.5	0.7
L1		1	
L2		0.5	
HE	11.6	12	12.4
HD	11.6	12	12.4
θ2		12°	
θ3		12°	
R		0.2	
R1		0.2	

9. Connection Examples

For reference purposes, this section gives various examples of connecting an external peripheral circuit to the LSI.

Note: The connection examples given here are provided solely for reference. They are not guaranteed to be functional in your product. The user is solely responsible for selecting the circuit configuration and parts suitable for the product in question.

9.1 Example of an OTG Interface Pin Connection



Notes on Connections

- To protect against static electricity, always incorporate a protective circuit comprised of diodes D1 and D2. Choose the appropriate diodes by considering their characteristics and rated values.
- Consider using diode D3 for added protection against static electricity.

- Select C1 in the range from 1.0 µF to 6.5 µF.
- Consider using C2 to protect the ID pin from static electricity.
- The DP and DM lines must be as short as possible and of equal lengths.
- Avoid positioning any other lines next to or directly below the OTG interface wiring.

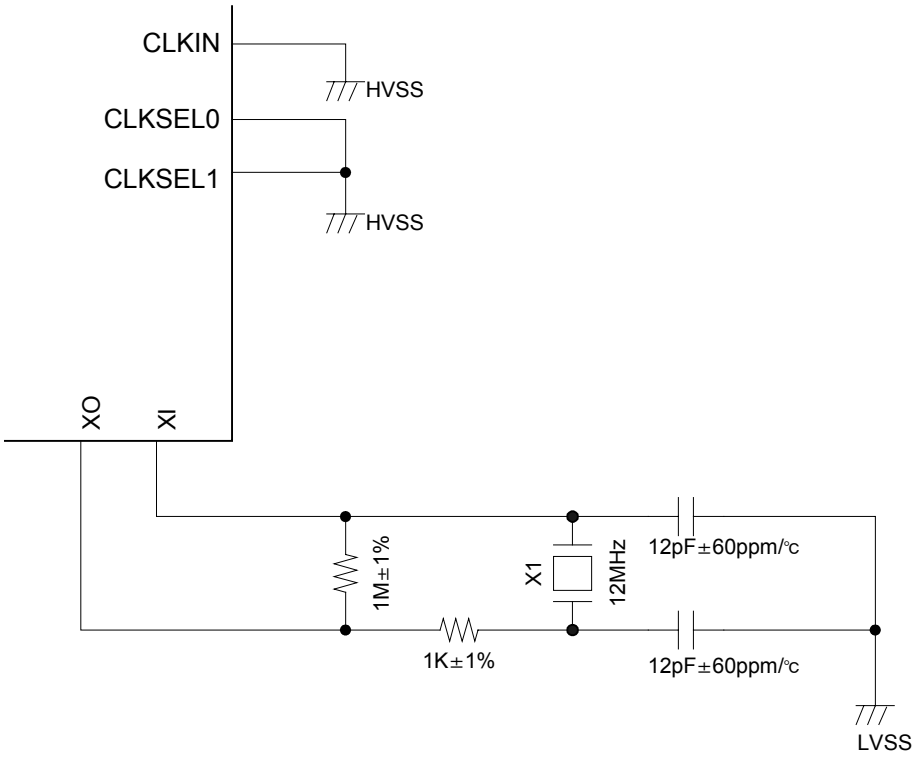
Example of Connected Parts

Note: The following part list is provided solely for reference. It does not constitute a guarantee of compatibility with your product. The user is responsible for selecting parts suitable for the product in question.

Item No.	Symbol	Part Name	Part Type Number	Specification (Constant)	Operating Temperature (°C)	Manufacturer	Quantity
1	C1	Ceramic Capacitor	GRM31MF11C475ZA12B	16V 4.7uF	-25 to 85	Murata Mfg.	1
2	C2	Ceramic Capacitor	GRM40F104Z50PT	0.1uF	-25 to 85	Murata Mfg.	1
3	L1, L2	EMI Filter	BLM21PG600SN1	600nH	-55 to 125	Murata Mfg.	2
4	R1, R2	Resistor	RK73H1JTD33F	33Ω	-55 to 125	KOA	2
5	R3	Resistor	RK73H1JTD2.2kD	2.2kΩ	-55 to 125	KOA	1
6	R4, R6	Resistor	RK73H1JTD100kD	100kΩ	-55 to 125	KOA	2
7	R5	Resistor	RK73H1JTD43kD	43kΩ	-55 to 125	KOA	1
8	R7, R8	Resistor	RK73H2BTD47kF	47kΩ	-55 to 125	KOA	2
9	Q1	FET	TPCS8205		-55 to 150	Toshiba	1
10	Q2, Q3	Transistor	2SA1121	PNP	-55 to 125	Hitachi	2
11	D1, D2	Diode	1SS396		-40 to 100	Toshiba	2
12	D3	Diode	NNCD5.6LG		-40 to 100	NEC	1
13	CN1	USBReceptacle	MNE20	USB miniAB	-	ACON	1

9.2 Example of a Clock Pin Connection

<When using a crystal resonator>

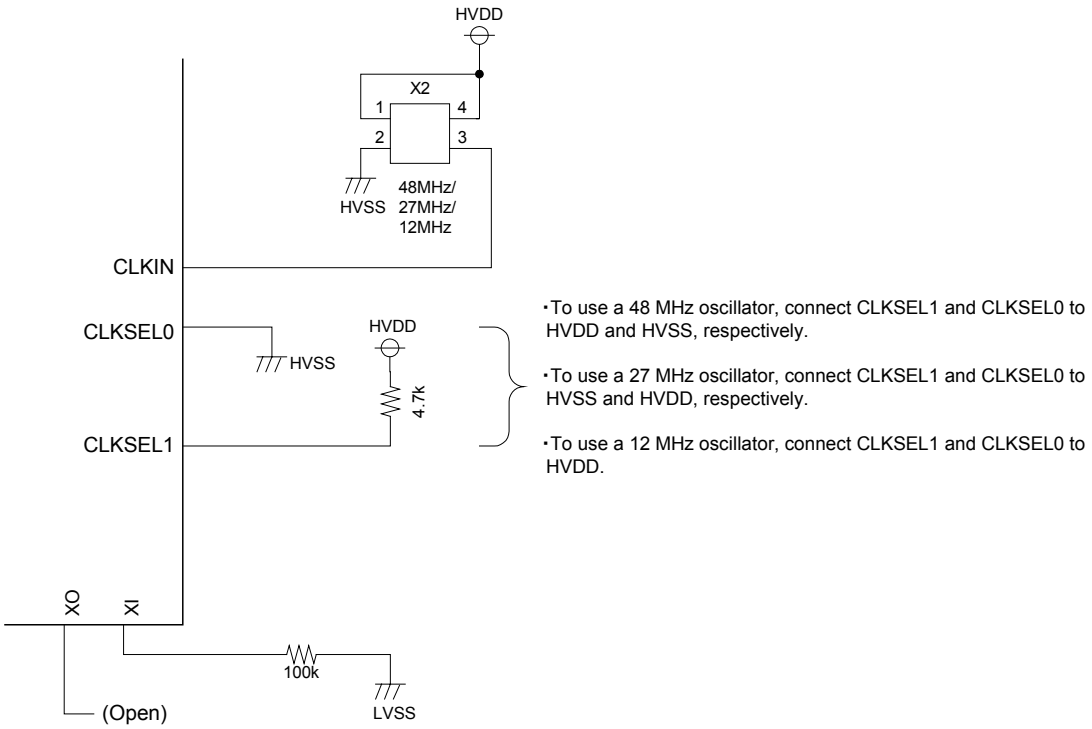


X1* : MA-406 12MHz 10pF 30ppm (EPSON)

Notes for Connections

- Do not wire any other lines next to or directly below the clock wiring.
- For XI and XO circuits and time constants, refer to a connection example for the crystal resonator X1 used in your product.
- Make sure the XI and XO circuits are wired by the shortest routes possible.

<When using a crystal oscillator (external clock input)>



X2* : Example for SG-615PCW 48 MHz ± 50 ppm (EPSON)

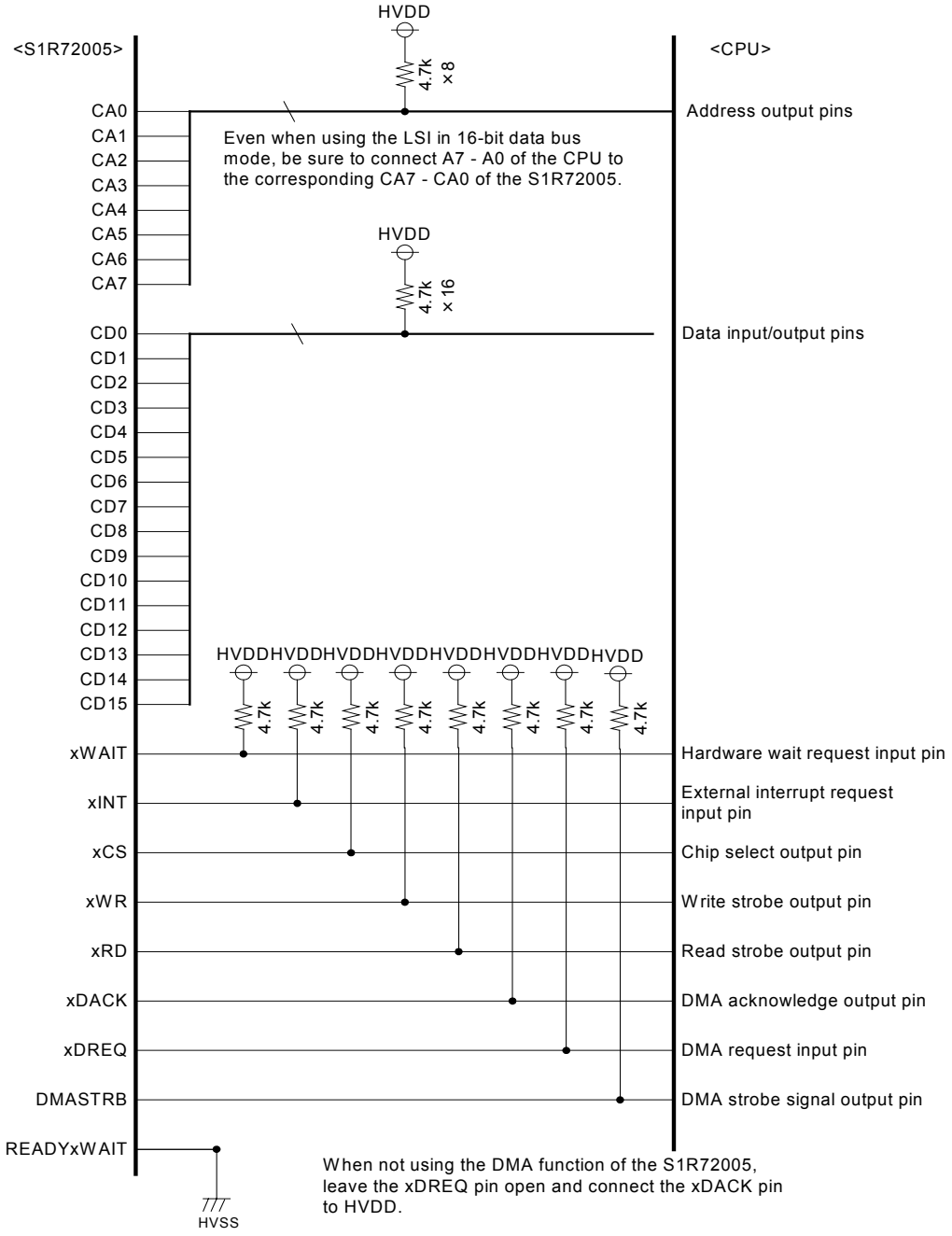
We recommend a crystal oscillator with center frequency ± 50 ppm or less.

PLL devices are not recommended, due to their excessive jitter.

Notes for Connections

- Avoid routing any other lines next to or directly below the clock wiring.
- For information on the CLKIN circuit, refer to a connection example given for the crystal oscillator X2 used in your product.
- Make sure the CLKIN circuit is wired by the shortest route possible.
- For the CLKIN input voltage, observe the HVI input voltage value specified as part of the required operating conditions.
- Make sure XI is wired by the shortest route possible.
- Make sure XO is wired by the shortest route possible, and leave it open.

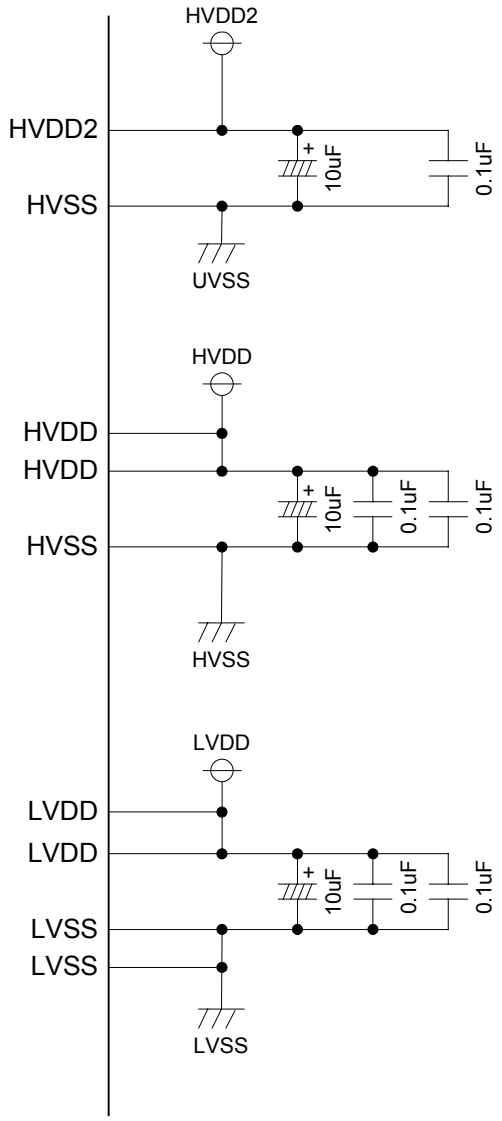
9.3 Example of a CPU Interface Pin Connection



Notes for Connections

- Always connect the READYxWAIT pin to either HVDD or HVSS, depending on the system in question.
- If your system requires pull-up resistors, use pull-up resistors having the appropriate resistance values.
- When not using the DMASTRB pin of the S1R72005, you must connect it to HVSS.
- If the data bus connects to an 8-bit CPU, use the 8 low-order bits of the bus in the S1R72005, connecting the 8 high-order bits to HVSS.

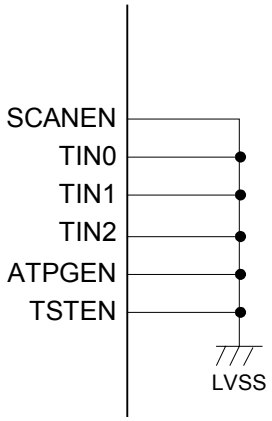
9.4 Example of Power Supply and Ground Pin Connections



Notes for Connections

- Make sure that HVSS and CPU I/O ground are accommodated by a common ground.
- Connect an exclusive capacitor (uppermost part in the above diagram) between the HVDD2 (G3 on CSP, pin 20 on QFP) and HVSS (H5 on CSP, pin 23 on QFP) located in the USB I/O block.

9.5 Example of Test Pin Connection



Notes for Connections

- Always make sure that all test input pins are connected to VSS, as shown above.

The application circuit examples in this manual are provided solely for reference. No guarantees are made with regard to their freedom from infringement of the patent rights of third parties. Seiko Epson rejects any liability should use of these application circuit examples result in patent infringement.

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