EPSON

S1C63558

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Low Current Consumption
- Wide-range Operating Voltage (2.2V to 5.5V)
- High Speed Operation in Low Voltage

■ DESCRIPTION

The S1C63558 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (5,120 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems), SVD circuit, a dot-matrix LCD driver that can drive a maximum 40 segments × 17 commons, DTMF/DP generator, FSK demodulator and sound generator built-in. The S1C63558 features high speed operation and low current consumption in an operating voltage range (2.2 V to 5.5 V), this makes it suitable for applications working with batteries. It is also suitable for caller ID and portable data bank systems because it has a large capacity of RAM built-in.

■ FEATURES

- OSC1 oscillation circuit ..... 32.768 kHz (Typ.) crystal oscillation circuit
- OSC3 oscillation circuit ..... 3.58 MHz (Typ.) ceramic oscillation circuit
- Instruction set ..... Basic instruction: 46 types (411 instructions with all)
  Addressing mode: 8 types
- Instruction execution time ..... During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec
  During operation at 3.58 MHz: 0.56 µsec 1.12 µsec 1.68 µsec
- ROM capacity ..... Code ROM: 8,192 words × 13 bits
  Data ROM: 2,048 words × 4 bits (= 8K bits)
- RAM capacity ..... Data memory: 5,120 words × 4 bits
  Display memory: 816 bits (192 words × 4 bits + 48 × 1 bit)
- Input port ..... 8 bits (Pull-up resistors may be supplemented ∗1)
- Output port ..... 12 bits (It is possible to switch the 8 bits to special output ∗2)
- I/O port ..... 16 bits (It is possible to switch the 2 bits to special output and the 4 bits to serial I/F input/output ∗2)
- Serial interface ..... 2 ch. (8-bit clock synchronous or asynchronous system is selectable)
- LCD driver ..... 40 segments × 8, 16 or 17 commons (∗2)
  /48 segments × 8 commons (∗1)
- Time base counter ..... 2 systems (Clock timer, stopwatch timer)
- Programmable timer ..... Built-in, 2 inputs × 8 bits, with event counter function
- Watchdog timer ..... Built-in
- DTMF generator ..... Built-in
- DP generator ..... Built-in
- FSK demodulator ..... Built-in (Compatible with ITU-T V.23/Bell 202)
- Sound generator ..... With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit ... 12 values, programmable (2.20 V to 3.30 V)
  (It is possible to switch 1 value to the external voltage detection ∗1)
- External interrupt ..... Input port interrupt: 2 systems
- Internal interrupt ..... Clock timer interrupt: 4 systems
  Stopwatch timer interrupt: 2 systems
  Programmable timer interrupt: 2 systems
  Serial interface interrupt: 6 systems
  Dialer interrupt: 1 system
  FSK interrupt: 2 systems

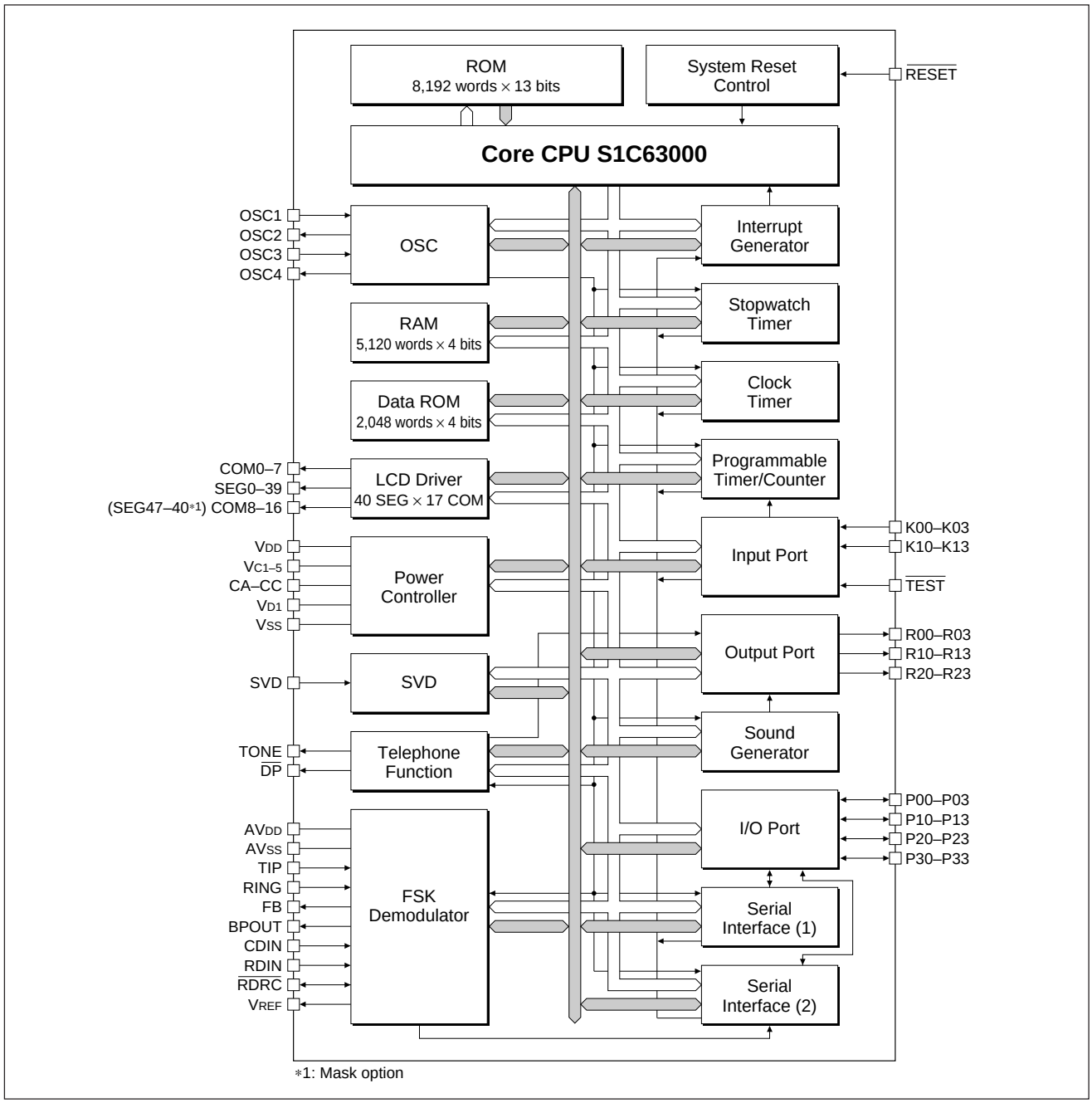
- Power supply voltage ..... 2.2 V to 5.5 V
- Operating temperature range ..... -20°C to 70°C
- Current consumption (Typ.) ..... Low-speed operation (OSC1: crystal oscillation):

During HALT (32 kHz)	3.0 V (LCD power OFF)	1.5 µA
	3.0 V (LCD power ON)	4 µA
During operation (32 kHz)	3.0 V (LCD power ON)	10 µA
High-speed operation (OSC3: ceramic oscillation):		
During operation (3.58 MHz)	3.0 V (LCD power ON)	600 µA
During FSK operation	5.5 V (LCD power ON)	1,800 µA

- Package ..... QFP15-128pin (plastic) or chip

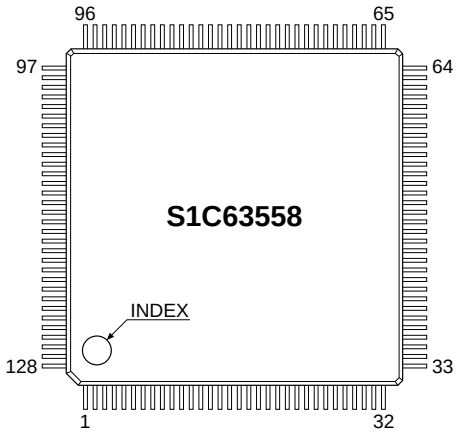
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP15-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	33	SEG4	65	N.C.	97	N.C.
2	SEG34	34	SEG3	66	R10	98	P00
3	SEG33	35	SEG2	67	R03	99	K13
4	SEG32	36	SEG1	68	R02	100	K12
5	SEG31	37	SEG0	69	R01	101	K11
6	SEG30	38	COM7	70	R00	102	K10
7	SEG29	39	COM6	71	CDIN	103	K03
8	SEG28	40	COM5	72	BPOUT	104	K02
9	SEG27	41	COM4	73	$\overline{RDRC}$	105	K01
10	SEG26	42	COM3	74	RDIN	106	K00
11	SEG25	43	COM2	75	V_{REF}	107	SVD
12	SEG24	44	COM1	76	AV_{SS}	108	V_{C1}
13	SEG23	45	COM0	77	FB	109	V_{C23}
14	SEG22	46	V_{SS}	78	RING	110	V_{C4}
15	SEG21	47	OSC1	79	TIP	111	V_{C5}
16	SEG20	48	OSC2	80	AV_{DD}	112	CC
17	SEG19	49	V_{D1}	81	P33	113	CB
18	SEG18	50	OSC3	82	P32	114	CA
19	SEG17	51	OSC4	83	P31	115	COM8/SEG47 *1
20	SEG16	52	V_{DD}	84	P30	116	COM9/SEG47 *1
21	SEG15	53	$\overline{RESET}$	85	P23	117	COM10/SEG46 *1
22	SEG14	54	$\overline{TEST}$	86	P22	118	COM11/SEG45 *1
23	SEG13	55	TONE	87	P21	119	COM12/SEG44 *1
24	SEG12	56	$\overline{DP}$	88	P20	120	COM13/SEG43 *1
25	SEG11	57	R23	89	P13	121	COM14/SEG42 *1
26	SEG10	58	R22	90	P12	122	COM15/SEG41 *1
27	SEG9	59	R21	91	P11	123	COM16/SEG40 *1
28	SEG8	60	R20	92	P10	124	SEG39
29	SEG7	61	R13	93	P03	125	SEG38
30	SEG6	62	R12	94	P02	126	SEG37
31	SEG5	63	R11	95	P01	127	SEG36
32	N.C.	64	N.C.	96	N.C.	128	SEG35

*1: Mask option

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
V_{DD}	52	–	Power (+) supply pin
V_{SS}	46	–	Power (–) supply pin
V_{D1}	49	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C5}	108–111	–	LCD system power supply pin (1/4 bias generated internally)
CA–CC	114–112	–	LCD system boosting/reducing capacitor connecting pin
OSC1	47	I	Crystal oscillation input pin
OSC2	48	O	Crystal oscillation output pin
OSC3	50	I	Ceramic oscillation input pin
OSC4	51	O	Ceramic oscillation output pin
K00–K03	106–103	I	Input port
K10–K13	102–99	I	Input port
P00–P03	98, 95–93	I/O	I/O port
P10–P13	92–89	I/O	I/O port (switching to serial I/F (1) input/output is possible by software)
P20	88	I/O	I/O port
P21	87	I/O	I/O port
P22	86	I/O	I/O port (switching to CL signal output is possible by software)
P23	85	I/O	I/O port (switching to FR signal output is possible by software)
P30–P33	84–81	I/O	I/O port (switching to serial I/F (2) input/output is possible by software)
R00	70	O	Output port (switching to XBZ signal output is possible by software)
R01	69	O	Output port (switching to BZ signal output is possible by software)
R02	68	O	Output port (switching to TOUT signal output is possible by software)
R03	67	O	Output port (switching to FOUT signal output is possible by software)
R10	66	O	Output port (switching to XTMUTE signal output is possible by software)

Pin name	Pin No.	I/O	Function
R11	63	O	Output port (switching to XRMUTE signal output is possible by software)
R12	62	O	Output port (switching to HDO signal output is possible by software)
R13	61	O	Output port (switching to HFO signal output is possible by software)
R20–R23	60–57	O	Output port
COM0–COM7	45–38	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
COM8–COM16 (SEG47–SEG40)	115–123	O	LCD common output pin or LCD segment output pin (mask option)
SEG0–SEG39	37–33, 31–2, 128–124	O	LCD segment output pin
SVD	107	I	SVD external voltage input pin
$\overline{DP}$	56	O	Dial pulse output pin
TONE	55	O	DTMF output pin
$\overline{RESET}$	53	I	Initial reset input pin
$\overline{TEST}$	54	I	Testing input pin
AV_{DD}	80	–	Power (+) supply pin for FSK demodulator
AV_{SS}	76	–	Power (-) supply pin for FSK demodulator
RDIN	74	I	Ring detection input pin
TIP	79	I	TIP input pin
RING	78	I	RING input pin
FB	77	O	Input amplifier output pin
BPOUT	72	O	Band-pass filter output pin
CDIN	71	I	Carrier detection input pin
$\overline{RDRC}$	73	I/O	I/O pin for connecting RC network
V_{REF}	75	O	Reference voltage output pin (1/2 V_{DD})

■ OPTION LIST

1 MULTIPLE KEY ENTRY RESET COMBINATION
- ☐ 1. Not Use
- ☐ 2. Use <K00, K01, K02, K03>
- ☐ 3. Use <K00, K01, K02>
- ☐ 4. Use <K00, K01>

2 MULTIPLE KEY ENTRY RESET TIME AUTHORIZE
- ☐ 1. Not Use
- ☐ 2. Use

3 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct

4 OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R01	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R02	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R03	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R10	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R11	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R12	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R13	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R20	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R21	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R22	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R23	☐ 1. Complementary	☐ 2. Nch-OpenDrain

5 I/O PORT OUTPUT SPECIFICATION

• P00	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P01	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P02	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P03	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P10	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P11	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P12	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P13	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P20	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P21	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P22	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P23	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P30	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P31	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P32	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P33	☐ 1. Complementary	☐ 2. Nch-OpenDrain

6 I/O PORT PULL UP RESISTOR

• P0x	☐ 1. With Resistor	☐ 2. Gate Direct
• P1x	☐ 1. With Resistor	☐ 2. Gate Direct
• P20	☐ 1. With Resistor	☐ 2. Gate Direct
• P21	☐ 1. With Resistor	☐ 2. Gate Direct
• P22	☐ 1. With Resistor	☐ 2. Gate Direct
• P23	☐ 1. With Resistor	☐ 2. Gate Direct
• P3x	☐ 1. With Resistor	☐ 2. Gate Direct

7 DP PORT OUTPUT SPECIFICATION

☐ 1. Complementary ☐ 2. Nch-OpenDrain

8 SVD EXTERNAL VOLTAGE DETECTION

☐ 1. Not Use
☐ 2. Use

9 LCD DRIVER SPECIFICATION

☐ 1. 40 seg ∗ 17 com
☐ 2. 48 seg ∗ 8 com

10 FSK INTERNAL FEEDBACK RESISTOR

☐ 1. Use
☐ 2. Not Use

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP15-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	OSC3 oscillation OFF	2.2		5.5	V
			OSC3 oscillation ON	2.2		5.5	V
			When DTMF is used	2.5		5.5	V
			When FSK is used	2.5		5.5	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
	f_{OSC3}	Ceramic oscillation		–	3.58	3.6	MHz
SVD terminal input voltage	SVD	SVD≤V_{DD}, V_{SS}=0V		0		5.5	V

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23, P30–33	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
High level input voltage (3)	V_{IH3}		RDIN, $\overline{RDRC}$	0.75·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		P00–03, P10–13, P20–23, P30–33	0		0.4	V
Low level input voltage (3)	V_{IL3}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
Low level input voltage (4)	V_{IL4}		RDIN, $\overline{RDRC}$	0		0.25·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13, RDIN, $\overline{RDRC}$ P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$, SVD	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, RDIN, $\overline{RDRC}$ P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$, SVD	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33			-1	mA
Low level output current	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, $\overline{RDRC}$ P00–03, P10–13, P20–23, P30–33	3			mA
Common output current	I_{OH2}	V_{OH2}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23, P30–33	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
High level input voltage (3)	V_{IH3}		RDIN, $\overline{RDRC}$	0.75·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		P00–03, P10–13, P20–23, P30–33	0		0.4	V
Low level input voltage (3)	V_{IL3}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
Low level input voltage (4)	V_{IL4}		RDIN, $\overline{RDRC}$	0		0.25·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13, RDIN, $\overline{RDRC}$ P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$, SVD	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, RDIN, $\overline{RDRC}$ P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$, SVD	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33			-3	mA
Low level output current	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, $\overline{RDRC}$ P00–03, P10–13, P20–23, P30–33	7.5			mA
Common output current	I_{OH2}	V_{OH2}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C23} ×0.95		1/2·V_{C23} -0.1	V
	V_{C23}	Connect 1 MΩ load resistor between V_{SS} and V_{C23} (without panel load)	LC0–3="0"		1.95		
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"	Typ.	2.16	Typ.	V
			LC0–3="8"	×0.88	2.19	×1.12	
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3/2·V_{C23} ×0.95		3/2·V_{C23}	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		2·V_{C23} ×0.95		2·V_{C23}	V
SVD voltage (Ta=25°C)	V_{SVD1}	SVDS0–3="0" (internal)			2.20		
		SVDS0–3="1"			2.20		
		SVDS0–3="2"			2.20		
		SVDS0–3="3"			2.20		
		SVDS0–3="4"			2.20		
		SVDS0–3="5"			2.30		
		SVDS0–3="6"			2.40		
		SVDS0–3="7"		Typ.	2.50	Typ.	V
		SVDS0–3="8"		×0.93	2.60	×1.07	
		SVDS0–3="9"			2.70		
		SVDS0–3="10"			2.80		
		SVDS0–3="11"			2.90		
		SVDS0–3="12"			3.00		
		SVDS0–3="13"			3.10		
		SVDS0–3="14"			3.20		
		SVDS0–3="15"			3.30		
SVD voltage (external) *3	V_{SVD2}	SVDS0–3="0" (external), Ta = 25°C		0.85	0.95	1.05	V
SVD circuit response time	t_{SVD}	Ta = 25°C				100	µS
Current consumption (Ta=25°C)	I_{OP}	During HALT (32 kHz crystal oscillation)	LCD power OFF *1, *2		1.5	3	µA
			LCD power ON *1, *2		4	8	µA
		During execution (32 kHz crystal oscillation)	LCD power ON *1, *2		10	19	µA
		During HALT (3.58 MHz ceramic oscillation)	LCD power ON *1		150	300	µA
		During execution (3.58 MHz ceramic oscillation)	LCD power ON *1		600	800	µA
		SVD circuit current (during supply voltage detection) V_{DD}=2.2 to 5.5 V		1		15	µA
		SVD circuit current (during external voltage detection) V_{DD}=2.2 to 5.5 V		0.5		6	µA
		DTMF circuit current V_{DD}=5.5 V *4			1.4	2.5	mA
		DTMF circuit current V_{DD}=3.0 V *4			1.2	2.0	mA
		FSK circuit current V_{DD}=5.5 V *4			1.8	2.5	mA
		FSK circuit current V_{DD}=3.0 V *4			1.0	1.5	mA

*1: Without panel load. The SVD circuit is OFF.
*2: OSCC = "0"
*3: Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.
*4: OSC3 oscillation current and CPU operating current with a 3.58 MHz clock are included.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	Δf/ΔV	V_{DD}=2.2 to 5.5V			10	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	5.5			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 3.58MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

● Serial Interface (1), (2) AC Characteristics

Clock Synchronous Master Mode (During 1 MHz Operation)

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

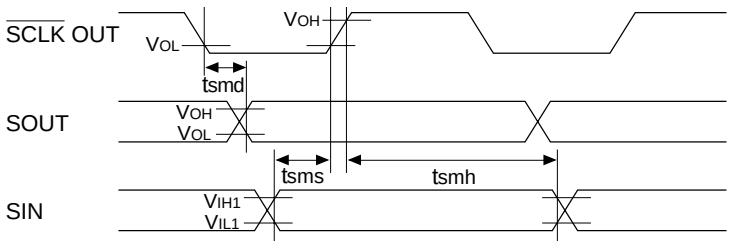
Clock Synchronous Slave Mode (During 1 MHz Operation)

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

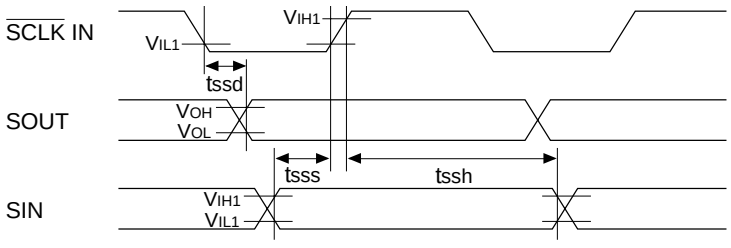
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>



<Slave mode>



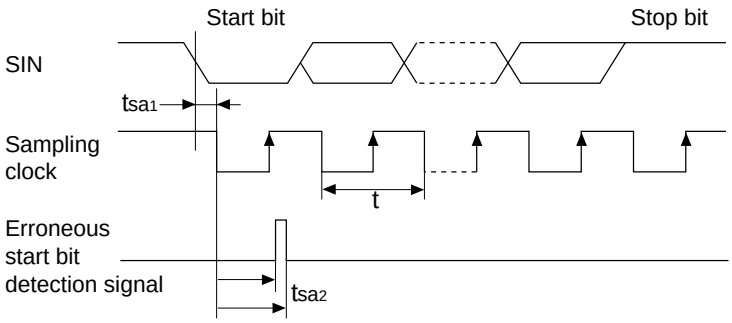
Asynchronous System

(Condition: V_{DD}=2.2 to 5.5V, V_{SS}=0V, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Start bit detection error time *1	t_{sa1}	0		t/16	S
Erroneous start bit detection range time *2	t_{sa2}	9t/16		10t/16	S

*1: Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

*2: Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started. When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)



● FSK Demodulator Characteristics

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	TRATE		1188	1200	1212	
Bell202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V0}		2068	2100	2132	Hz
Signal-to-noise ratio	SNR		20	–	–	dB
Band-pass filter gain *1	G_{BPF}	300Hz	–	9.2	–	dB
		1200Hz	–	42.7	–	dB
		1700Hz	–	42.8	–	dB
		2200Hz	–	42.7	–	dB
		3000Hz	–	22.4	–	dB
		4000Hz	–	3.7	–	dB
		≥10000Hz	–	-20.0	–	dB
Carrier detection ON sensitivity *2	CD_{ON}	V_{DD}=5.0V	–	-51	-48	dBm
Carrier detection OFF sensitivity *2	CD_{OFF}	V_{DD}=5.0V	-57	-54	–	dBm
Input clock frequency	f_{CLK}		-0.1%	3.579545	+0.1%	MHz
Input AC impedance	R_{IN}	V_{DD}=5.0V (between TIP/RING pin and V_{REF})	70	100	130	kΩ
FSKON set-up time	t_{SUP}		20	–	–	mS
Carrier detection response time	t_{CDON}		3	6.25	9	mS
	t_{CDOFF}		5	7.5	10	mS

*1: Value measured between TIP/RING pin and BPOUT pin

*2: The following expressions can be used to calculate the typical values (dBm) of CD_{ON} and CD_{OFF} when an external resistor R_{TR} (10kΩ Typ.) is connected in series with the TIP pin and the RING pin.

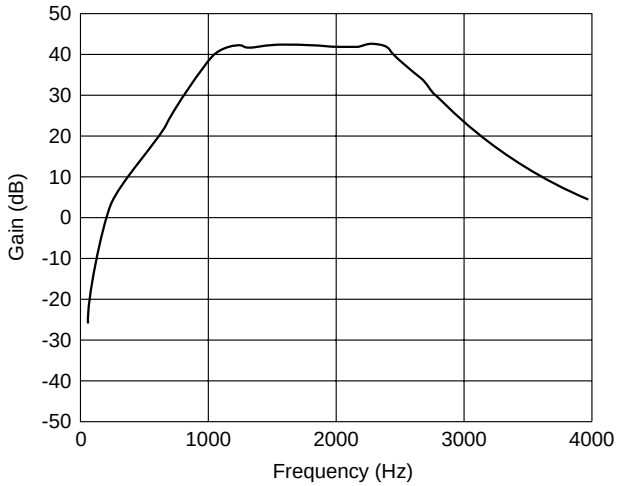
$$CD_{ON} = -51 + 20\log\left(\frac{V_{DD}}{5} \times \frac{100k}{R_{TR} + 100k}\right) [dBm] \quad CD_{OFF} = -54 + 20\log\left(\frac{V_{DD}}{5} \times \frac{100k}{R_{TR} + 100k}\right) [dBm]$$

In addition, the following expressions can be used to calculate the sensitivity of CD_{ON} and CD_{OFF} when an external feedback resistor is used for the input amplifier (mask option).

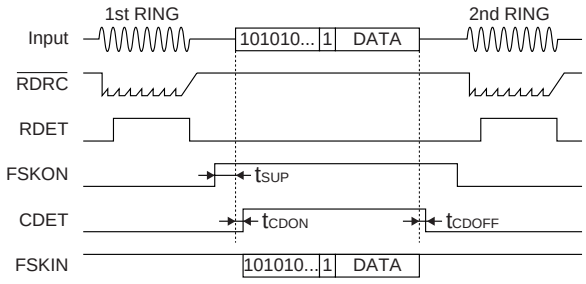
$$G_{Amp} = \frac{R_5}{R_1} = \frac{R_6}{R_2} \quad (R_1 = R_2, R_3 = R_4, R_5 = R_6)$$

$$CD_{ON} = -51 + 20\log\left(\frac{V_{DD}}{5} \times \frac{R_1}{R_5}\right) [dBm] \qquad CD_{OFF} = -54 + 20\log\left(\frac{V_{DD}}{5} \times \frac{R_1}{R_5}\right) [dBm]$$

Band-pass filter gain (Typ. value)



Timing chart



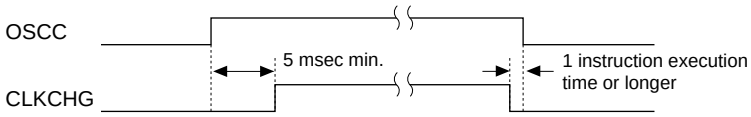
● Telephone Function Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Flash pause time	t_{FLP}		–	938	–	mS
Mute hold time	t_{MH}		–	4	–	mS
Make ratio	M/B	Selected by software	–	1/2 2/3	–	–
Dial puls rate	DR	Selected by software	–	10 20	–	pps
Make time	t_M	10pps, M/B=1/2	–	33.2	–	mS
		20pps, M/B=1/2	–	16.6	–	mS
		10pps, M/B=2/3	–	39.1	–	mS
		20pps, M/B=2/3	–	19.5	–	mS
Break time	t_B	10pps, M/B=1/2	–	66.4	–	mS
		20pps, M/B=1/2	–	33.2	–	mS
		10pps, M/B=2/3	–	58.6	–	mS
		20pps, M/B=2/3	–	29.3	–	mS
Tone output DC level	V_{TDC}		–	0.5(V_{DD}-V_{SS})	–	V
ROW single tone output voltage	V_R	V_{DD}=3V, R_L=10kΩ	–	92	–	mVrms
		V_{DD}=5.5V, R_L=10kΩ	–	168	–	mVrms
COL single tone output voltage	V_C	V_{DD}=3V, R_L=10kΩ	–	122	–	mVrms
		V_{DD}=5.5V, R_L=10kΩ	–	224	–	mVrms
Tone output voltage ratio	dB_{CR}	V_{DD}=3V, R_L=10kΩ	–	2.5	–	dB
		V_{DD}=5.5V, R_L=10kΩ	–	2.5	–	dB
Tone load resistor	R_{TL}	V_{DD}=2.5 to 5.5V	7	–	–	kΩ
Tone distortion ratio	THD	V_{DD}=2.5 to 5.5V, R_L=10kΩ	–	–	6	%
Tone output frequency	f_{ROW1}		–	701.32	–	Hz
	f_{ROW2}		–	771.45	–	Hz
	f_{ROW3}		–	857.17	–	Hz
	f_{ROW4}		–	935.10	–	Hz
	f_{COL1}		–	1215.88	–	Hz
	f_{COL2}		–	1331.68	–	Hz
	f_{COL3}		–	1471.85	–	Hz
	f_{COL4}		–	1645.01	–	Hz
Tone output time	t_{TD}		94	–	–	mS
Tone inter-digit pause time	t_{TIP}		–	94	–	mS
Tone output cycle	t_T	t_{TD}+t_{TIP}	188	–	–	mS

● Timing Chart

System clock switching

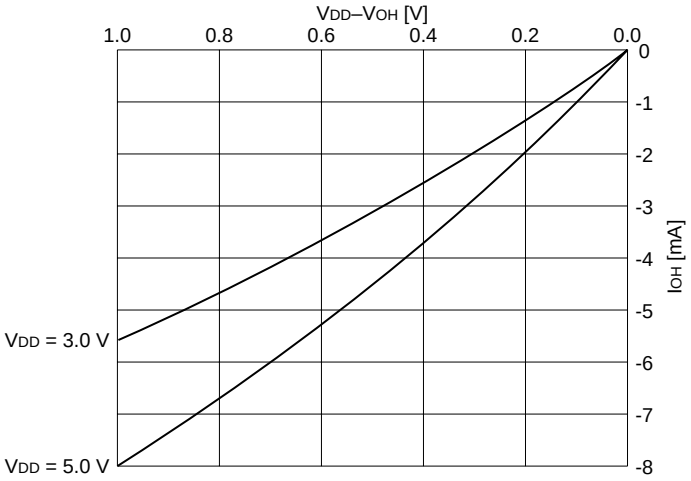


● Characteristic Curves (reference value)

Output current characteristics

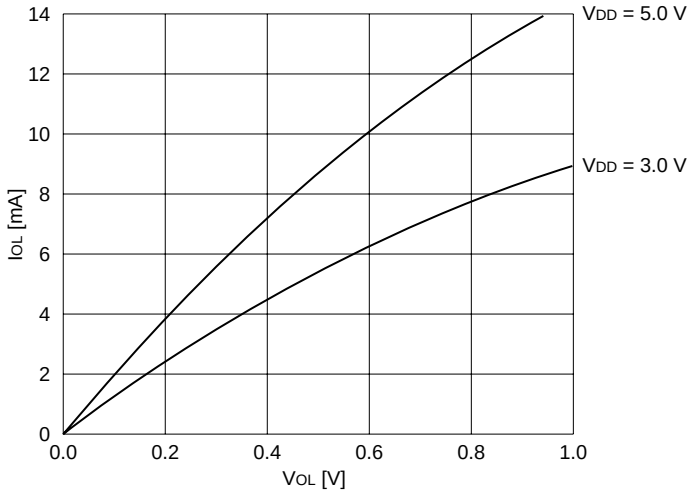
• High level output current (Pxx, Rxx, BZ)

Ta = 70˚C, Max. value



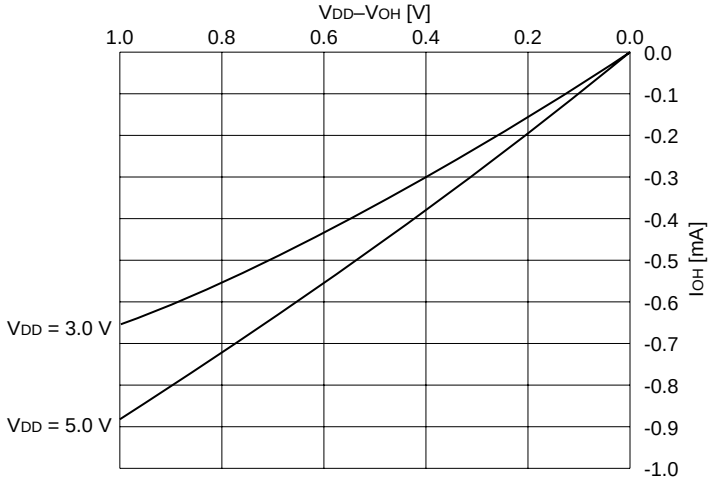
• Low level output current (Pxx, Rxx, BZ)

Ta = 70˚C, Min. value



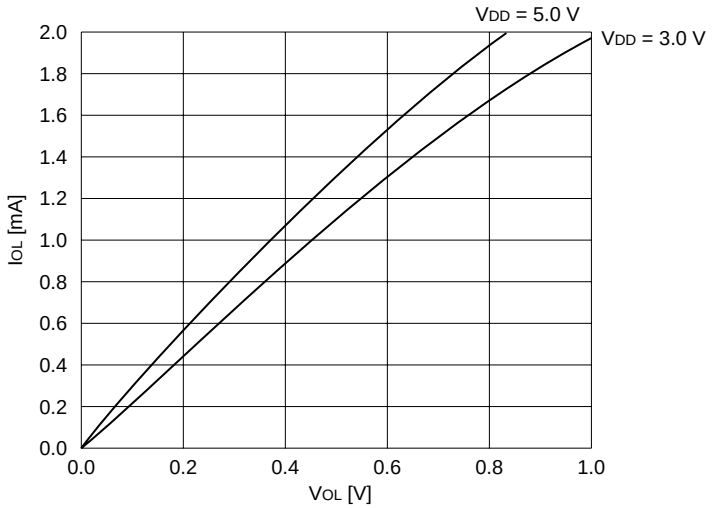
• **High level output current (SEGxx)**

Ta = 70˚C, Max. value



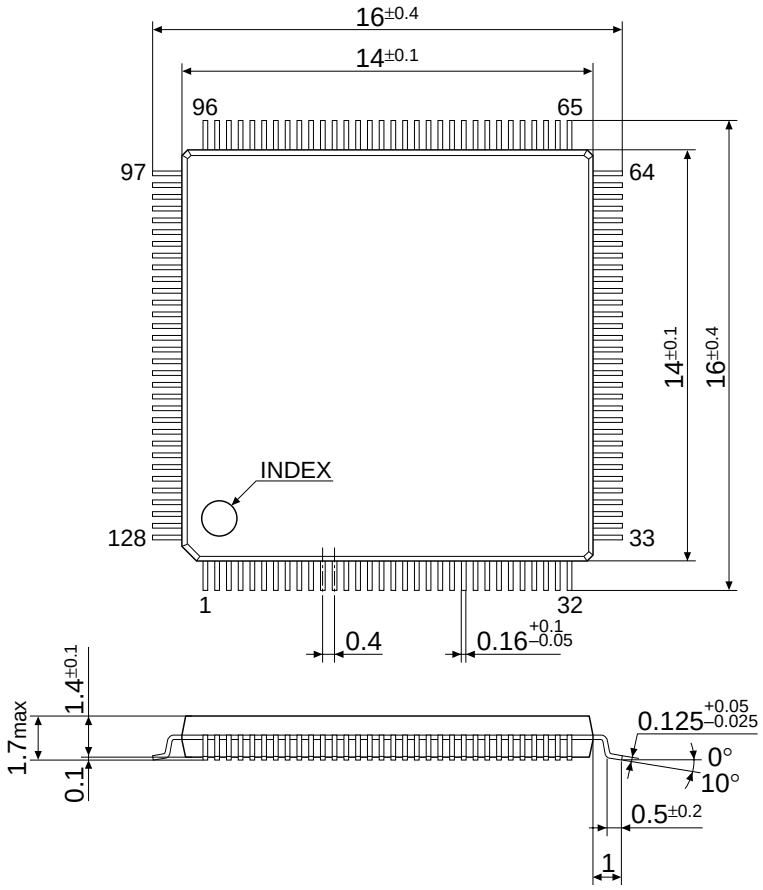
• **Low level output current (SEGxx)**

Ta = 70˚C, Min. value



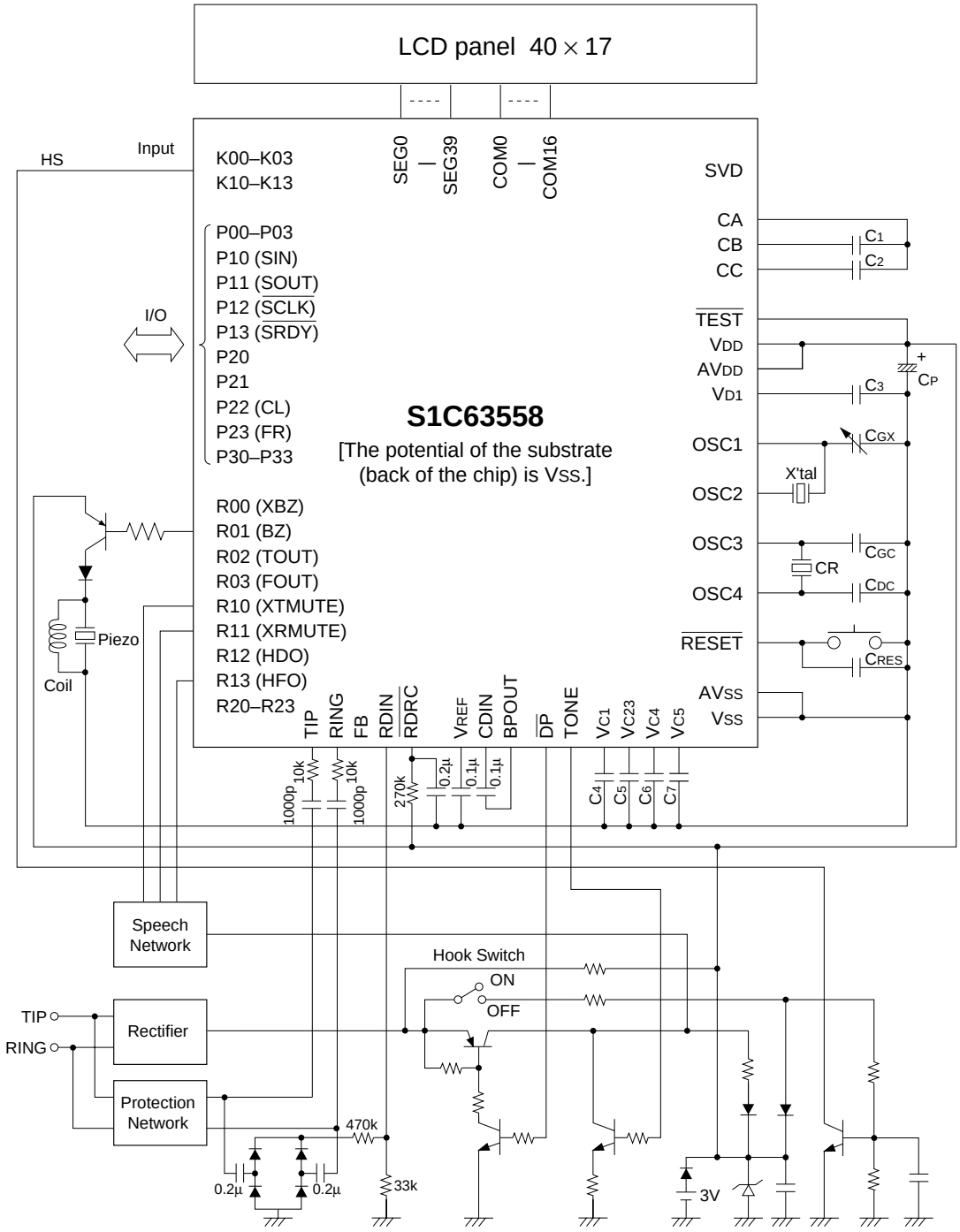
■ PACKAGE DIMENSIONS

Plastic QFP15-128pin



Unit: mm

■ BASIC EXTERNAL CONNECTION DIAGRAM

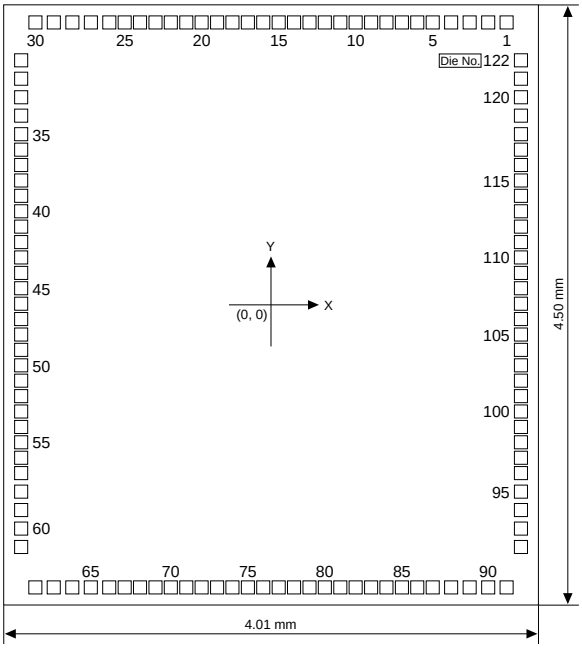


X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	3.58 MHz
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
C1–C7	Capacitor	0.2 µF
CP	Capacitor	10 µF
CRES	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PAD LAYOUT

● Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

● Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	R10	1767	2118	31	P00	-1874	1834	62	SEG34	-1767	-2118	92	SEG4	1874	-1815
2	R03	1629	2118	32	K13	-1874	1696	63	SEG33	-1629	-2118	93	SEG3	1874	-1677
3	R02	1490	2118	33	K12	-1874	1557	64	SEG32	-1490	-2118	94	SEG2	1874	-1538
4	R01	1351	2118	34	K11	-1874	1419	65	SEG31	-1351	-2118	95	SEG1	1874	-1400
5	R00	1213	2118	35	K10	-1874	1280	66	SEG30	-1213	-2118	96	SEG0	1874	-1261
6	CDIN	1097	2118	36	K03	-1874	1164	67	SEG29	-1097	-2118	97	COM7	1874	-1146
7	BPOUT	982	2118	37	K02	-1874	1049	68	SEG28	-982	-2118	98	COM6	1874	-1030
8	$\overline{RDRC}$	866	2118	38	K01	-1874	933	69	SEG27	-866	-2118	99	COM5	1874	-915
9	RDIN	751	2118	39	K00	-1874	818	70	SEG26	-751	-2118	100	COM4	1874	-799
10	V_{REF}	635	2118	40	SVD	-1874	702	71	SEG25	-635	-2118	101	COM3	1874	-684
11	AV_{SS}	520	2118	41	V_{C1}	-1874	587	72	SEG24	-520	-2118	102	COM2	1874	-568
12	FB	404	2118	42	V_{C23}	-1874	471	73	SEG23	-404	-2118	103	COM1	1874	-453
13	RING	289	2118	43	V_{C4}	-1874	356	74	SEG22	-289	-2118	104	COM0	1874	-337
14	TIP	173	2118	44	V_{C5}	-1874	240	75	SEG21	-173	-2118	105	V_{SS}	1874	-222
15	AV_{DD}	58	2118	45	CC	-1874	125	76	SEG20	-58	-2118	106	OSC1	1874	-106
16	P33	-58	2118	46	CB	-1874	9	77	SEG19	58	-2118	107	OSC2	1874	9
17	P32	-173	2118	47	CA	-1874	-106	78	SEG18	173	-2118	108	V_{D1}	1874	125
18	P31	-289	2118	48	COM8/SEG47 *1	-1874	-222	79	SEG17	289	-2118	109	OSC3	1874	240
19	P30	-404	2118	49	COM9/SEG47 *1	-1874	-337	80	SEG16	404	-2118	110	OSC4	1874	356
20	P23	-520	2118	50	COM10/SEG46 *1	-1874	-453	81	SEG15	520	-2118	111	V_{DD}	1874	471
21	P22	-635	2118	51	COM11/SEG45 *1	-1874	-568	82	SEG14	635	-2118	112	$\overline{RESET}$	1874	587
22	P21	-751	2118	52	COM12/SEG44 *1	-1874	-684	83	SEG13	751	-2118	113	$\overline{TEST}$	1874	702
23	P20	-866	2118	53	COM13/SEG43 *1	-1874	-799	84	SEG12	866	-2118	114	TONE	1874	818
24	P13	-982	2118	54	COM14/SEG42 *1	-1874	-915	85	SEG11	982	-2118	115	$\overline{DP}$	1874	933
25	P12	-1097	2118	55	COM15/SEG41 *1	-1874	-1030	86	SEG10	1097	-2118	116	R23	1874	1049
26	P11	-1213	2118	56	COM16/SEG40 *1	-1874	-1146	87	SEG9	1213	-2118	117	R22	1874	1164
27	P10	-1351	2118	57	SEG39	-1874	-1261	88	SEG8	1351	-2118	118	R21	1874	1280
28	P03	-1490	2118	58	SEG38	-1874	-1400	89	SEG7	1490	-2118	119	R20	1874	1419
29	P02	-1629	2118	59	SEG37	-1874	-1538	90	SEG6	1629	-2118	120	R13	1874	1557
30	P01	-1767	2118	60	SEG36	-1874	-1677	91	SEG5	1767	-2118	121	R12	1874	1696
–				61	SEG35	-1874	-1815	–				122	R11	1874	1834

*1: Mask option

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