EPSON

S1C05251

CAS + FSK IC

Low Voltage Operation Products

- ITU V.23 & Bell 202 FSK Receiver
- Bellcore "CPE Alerting Signal" Detection
- BT "Idle Tone Alert Signal" Detection
- Low Voltage Operation

■ DESCRIPTION

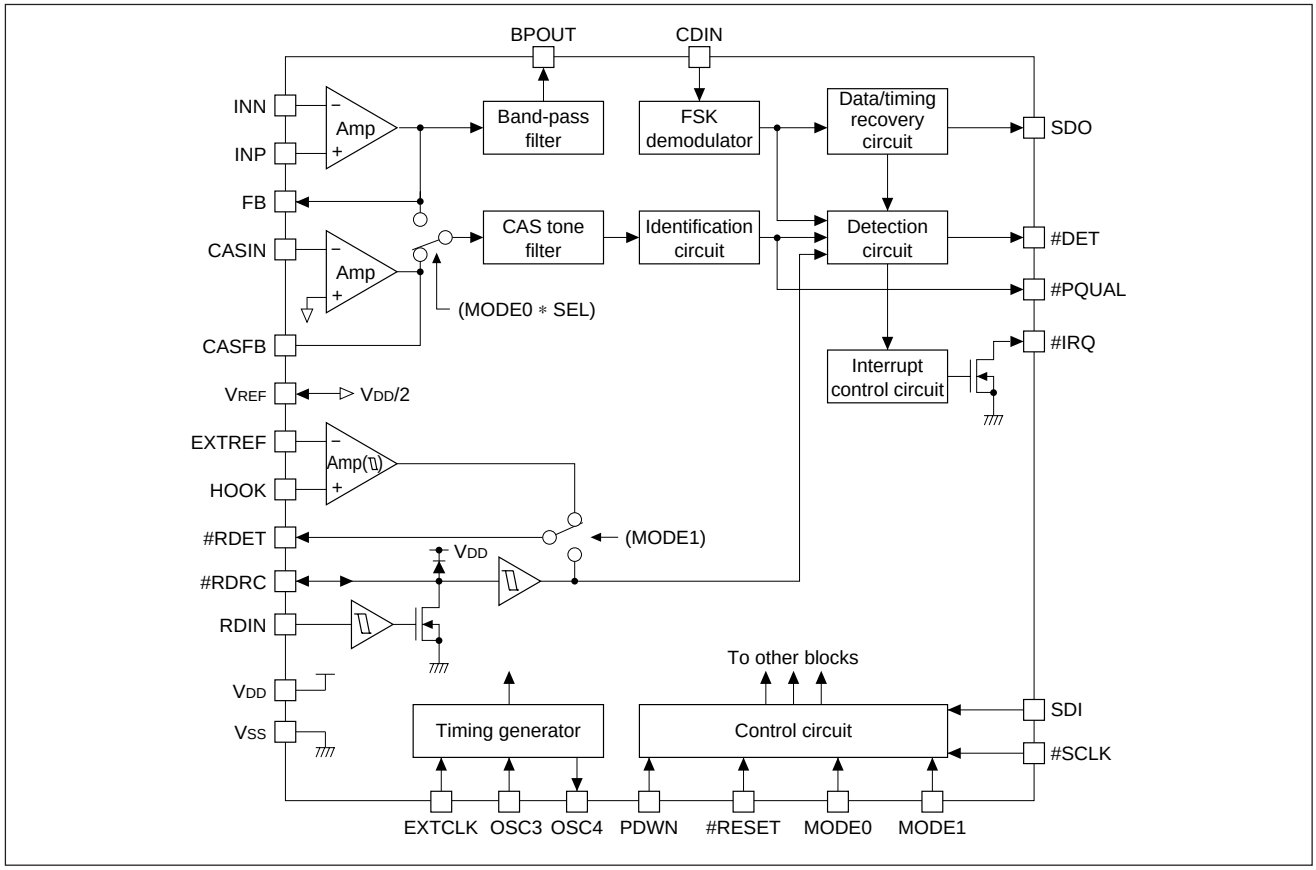
The S1C05251 (CAS + FSK IC), an upgraded version of the S1C05250, is a CMOS IC for calling number identification with the Call Waiting function. It provides an interface to various call information delivery services based on Bellcore GR-30-CORE, such as CND (Calling Number Delivery), CNAM (Calling Name Delivery), and CIDCW (Calling Identity on Call Waiting), as well as British Telecom's CLIP (Calling Line Identification Service) and Cable Communications Association's CDS (Caller Display Service). The S1C05251 incorporates power-down, ring detection, and carrier detection circuits, a synchronous receive data output function, and a clock-synchronized serial interface. All these features make it suitable for various applications such as those listed below.

- Calling number delivery service with a Call Waiting function
- Telephone sets and similar auxiliary equipment
- Telephone answering equipment
- Multifunction telephones
- Facsimiles
- Computer peripheral circuits
- Message waiting telephones

■ FEATURES

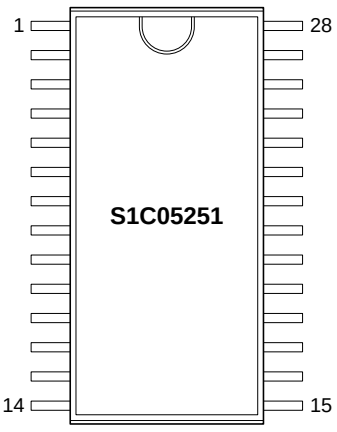
- Conforms to Bellcore GR-30-CORE and SR-TSV-002476 (same as S1C05250)
- Conforms to British Telecom SIN227 and SIN242 (same as S1C05250)
- Can detect Bellcore CPE alert signal (CAS) and British Telecom idle-tone alert signal using a programmable band-pass filter (same as S1C05250)
- FSK demodulation circuit based on ITU-T V.23 and BELL202 (same as S1C05250)
- Filter bypass mode to detect call progress mode (CPM) signal (same as S1C05250)
- Programmable alert-signal detection level (same as S1C05250)
- Carrier/ring detection output (same as S1C05250)
- FSK energy mode to detect FSK signal in power-down mode (new function for S1C05251)
- Supports CAS signal single-end input (new function for S1C05251)
- Off-hook detection (new function for S1C05251)
- Supports 3.57945 MHz crystal oscillator or external clock input (same as S1C05250)
- Serial-receive data output (same as S1C05250)
- Serial host interface (same as S1C05250)
- Power-down mode (same as S1C05250)
- Power supply voltage: 2.7 V to 5.5 V (same as S1C05250)
- Operating temperature range: -20°C to 70°C (same as S1C05250)
- Current consumption: 3 mA when operating (same as S1C05250)
  1 µA in zero-power mode (same as S1C05250)
  6 µA in FSK energy detection mode (new function for S1C05251)
- Shipping form: SOP2-28pin package (plastic), DIP-28pin package (ceramic) or chip (package for S1C05251)

■ BLOCK DIAGRAM

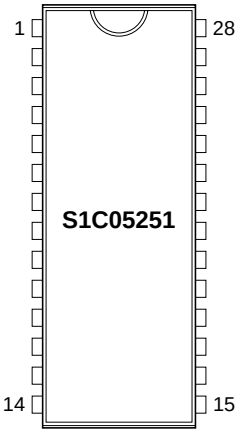


■ PIN CONFIGURATION

SOP2-28pin



DIP-28pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	INP	8	HOOK	15	OSC3	22	#IRQ
2	INN	9	RDIN	16	OSC4	23	#SCLK
3	FB	10	#RDRC	17	EXTCLK	24	SDI
4	CASIN	11	#RDET	18	MODE0	25	SDO
5	CASFB	12	PDWN	19	MODE1	26	CDIN
6	VREF	13	#RESET	20	#PQUAL	27	BPOUT
7	EXTREF	14	VSS	21	#DET	28	VDD

■ PIN DESCRIPTION

Note: The signal and pin names prefixed by # are those of active-low signals and pins.

Pin name	Pin No.	Type	Power-down state	Description
INP	1	Input Analog	Off/ Active	**+ Input:** Non-inverting amplifier input. This pin is connected to the telephone wire through an input gain-setting resistor and a DC cut capacitor. Under the power down mode, this pin is functionary disconnected from the internal circuitry when the MODE1 pin is set to low level. When the MODE1 pin is set to high level, this pin stays active to detect FSK signal energy to send wake up signal to the host through the #IRQ pin. Do not connect any external components to this pin except gain setting resistors to this pin. Excess load may cause improper operation of the circuit.
INN	2	Input Analog	Off/ Active	**- Input:** Inverting amplifier input. This pin is connected to the telephone wire through an input gain-setting resistor and a DC cut capacitor. Under the power down mode, this pin is functionary disconnected from the internal circuitry when the MODE1 pin is set to low level. When the MODE1 pin is set to high level, this pin stays active to detect FSK signal energy to send wake up signal to the host through the #IRQ pin. Do not connect any external components to this pin except gain setting resistors to this pin. Excess load may cause improper operation of the circuit.
FB	3	Output Analog	High-Z/ Active	**Amplifier Output:** A feed back resistor is connected between this pin and the INN pin to set gain. Under the power down mode, this output pin is set to high impedance when the MODE1 pin is set to low level. When the MODE1 pin is set to high level in power down, this pin stays active to detect FSK signal energy to send wake up signal to the host through the #DET pin. Do not connect any external components to this pin except a gain setting resistor to this pin. Excess load may cause improper operation of the circuit.
CASIN	4	Input Analog	Off	**CAS Tone Input:** CAS tone amplifier input. For the telephone application, this pin is connected to the output of telephone hybrid circuit through input gain-setting resistor and a DC cut capacitor. Under the power down mode, this pin is functionary disconnected from the internal circuitry. Do not connect any external components to this pin except gain setting resistors to this pin. Excess load may cause improper operation of the circuit.
CASFB	5	Output Analog	High-Z	**CAS Amplifier Output:** A feed back resistor is connected between this pin and the CASIN pin to set CAS gain. Under the power down mode, this output pin is set to high impedance. Do not connect any external components to this pin except a gain setting resistor to this pin. Excess load may cause improper operation of the circuit.
V_{REF}	6	Output Analog	High-Z/ V_{DD}/2 level	**Reference Voltage Output:** 1/2 V_{DD} voltage output. This pin must be bypassed to ground through 0.1 µF capacitor. During power down mode, this output pin is set to high impedance when the MODE1 pin is low level. When the MODE1 pin is set to high level in power down, this pin stays at V_{DD}/2. Do not connect any external components to this pin except a jumper to V_{REF} pin or a bypass capacitor to ground. Excess load may cause improper operation of the circuit.
EXTREF	7	Input Analog	Active	**External Reference Voltage Input:** External DC reference voltage is connected to this pin. This voltage set the off-hook detection threshold level.
HOOK	8	Input Analog	Active	**Off-Hook Detection Input:** Diode bridge output from the TIP/RING lines is connected to this pin through external resistor divider to detect off-hook/on-hook states.
RDIN	9	Schmitt trigger input	Active	**Ring Detect Input:** The attenuated ring signal is connected to this pin for the ring detection. This circuit is always active even if the device is in the power down mode.
#RDRC	10	Open-drain output Schmitt trigger input	Active	**Ring Detect RC Terminal:** RC network will be connected to this pin to set time delays for the ring signal detection. This circuit is always active even if the device is in the power down mode.
#RDET	11	Output	Active	**Ring Detect Output:** When the MODE1 pin is set to low level, this pin is connected from output of a Schmitt trigger buffer which input is connected to the #RDRC pin. Low level at this pin indicates that the ring signal is detected. When the MODE1 pin bit is set to high level, this pin is connected from output of a hook detect circuit which input is connected from the HOOK pin. High level at this pin indicates on-hook condition and low level at this pin indicates off-hook condition.
PDWN	12	Input	Active	**Power Down Input:** This pin must be kept at low level for the normal operation. When it is set to high level, the device enters the power down mode. During power down mode, the OSC4 pin is set to high level, and the V_{REF}, CASFB and FB pins are set to high impedance. (The FB and V_{REF} pins are set to high impedance only when the MODE1 pin is at low level.)
#RESET	13	Input	Active	**Reset Input:** When this pin is set to low level, all internal host registers are reset to their default conditions. This pin must be set to high level to write data to the internal registers.
V_{SS}	14	Power supply (-)		**Device Ground:** This pin is connected to the system ground.

Pin name	Pin No.	Type	Power-down state	Description
OSC3	15	Input	Off	**Crystal Oscillator/External Clock Input:** A crystal resonator is connected between this pin and the OSC4 pin. This pin may be driven from an external clock source. The proper value load capacitor must be connected between this pin and ground. During power down, this input pin is disconnected from internal circuits.
OSC4	16	Output	High level	**Crystal Oscillator Output:** A crystal or ceramic resonator is connected between this pin and OSC3 pin. This pin must be kept open when the OSC3 pin is driven from an external clock source. The proper value load capacitor must be connected between this pin and ground. During power down, this output pin is set to high level.
EXTCLK	17	Input	Active	**External Clock Input:** Typically 32.768 kHz clock signal is applied to this pin from the host device to enable pre-qualification logic used in FSK energy detection circuitry.
MODE0	18	Input	Active	**Mode0 Select Input:** This pin select CAS or FSK/CPM mode. When this pin is set to high level, CAS mode is selected. In this mode, CAS detection is enabled and the FSK function is disabled. The host device also can write internal registers through the SDI and #SCLK pin. Before writing data into registers, this pin must be set to low level once to synchronize the serial interface circuit for data writing sequence. When this pin is set to low level, FSK/CPM mode is selected. In this mode, CAS detection is disabled and the FSK/CPM function is enabled. The host device also can read the received data from the SDO pin under this mode.
MODE1	19	Input	Active	**Mode1 Select Input:** This pin enables FSK energy and off-hook detection mode. When this pin is set to high level, FSK energy and off-hook detection mode is enabled. When this pin is set to low level, FSK energy and off-hook detection mode is disabled.
#PQUAL	20	Output	High level	**Pre-qualification Output:** Early qualification output will be monitored at this pin. When no tones are detected, this pin stays at high level.
#DET	21	Output	Active	**Detection Output:** When the device is in the power down mode and the MODE1 pin is set to low level, low level at this pin indicates the presence of ring signal or phone line reversal. If the MODE1 pin is set to high level, low level at this pin indicates the presence of ring signal or FSK inbound signal. When in the power up mode and FSK mode is selected, low level at this pin indicates the presence of FSK inbound signal. If CPM mode is selected, pulses from this pin indicate the presence of CPM tone signal. If CAS mode is selected, low level at this pin indicates the presence of CAS tone signal.
#IRQ	22	Open-drain output	Active	**Interrupt Request Output:** When the device is in the power down mode, low level at this pin indicates the presence of ring signal or phone line reversal. When in the power up mode and FSK mode is selected, low level at this pin indicates that the received data is ready in the internal register for the host device to read. In this mode, this pin is set to high level after the first bit of the received data is read. If CPM mode is selected, low level at this pin indicates the presence of CPM. If CAS mode is selected, low level at this pin indicates that the CAS tone is detected. In this mode, this pin remains low level while CAS tones exist.
#SCLK	23	Input	Active	**Serial Clock Input:** The host device supplies a clock to this pin to write internal registers or to read received data. The received data changes its state at falling edge of the clock supplied by the host device.
SDI	24	Input	Active	**Serial Data Input:** The host device writes control bits through this pin.
SDO	25	Output	High level	**Serial Data Output:** The host device reads the serial receive data from this pin. If asynchronous mode is selected, the asynchronous format serial data appears at this pin. If synchronous mode is selected, the received serial data is read from this pin by the host device with the serial clock supplied to the #SCLK pin. During the power down, CPM or CAS mode, this output pin is set to high level.
CDIN	26	Input Analog	V_{REF}	**Capacitor Input:** A 0.1 µF capacitor is connected between this pin and the BPOUT pin. The FSK signal can be applied from the FB pin to this pin through this 0.1 µF capacitor to bypass the band pass filter for internal testing purpose. Do not connect any external components except this capacitor to this pin. Excess load may cause improper operation of the circuit.
BPOUT	27	Output Analog	High-Z	**Capacitor Output:** A 0.1 µF capacitor is connected between this pin and the CDIN pin. The band pass filter output is monitored at this pin for internal testing purpose. Do not connect any external components except this capacitor to this pin. Excess load may cause improper operation of the circuit.
V_{DD}	28	Power supply (+)		**Device Power Supply:** Positive power supply pin.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rated value	Unit
Power supply voltage	V_{DD}	-0.5 to 7	V
Input voltage	V_I	-0.3 to V_{DD}+0.3	V
Total output current	ΣI_{VDD}	±10	mA
Power dissipation	P_D	250	mW
Storage temperature	T_{STG}	-65 to 150	°C
Solder temperature	T_{SOL}	255	°C
Soldering time	t_{SOL}	10	Sec
Operating temperature	T_{OPR}	-20 to 70	°C
Electrostatic withstand voltage	V_E	EIAJ test (C=200pF): 250V or more MIL test (C=100pF, R=1.5kΩ): 1200V or more	V

The voltages are referenced to the V_{SS} pin as the ground level.

● Recommended Operating Conditions

Parameter	Symbol	Condition	Unit
Power supply voltage	V_{DD}	2.7 to 5.5	V
Crystal/clock frequency	f_{CLK}	3.579545	MHz
Crystal/clock frequency error	f_{ERR}	±0.01	%

The voltages are referenced to the V_{SS} pin as the ground level.

● DC Characteristics

(Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, EXTCLK	0.8V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		RDIN, #RDRC	0.7V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, EXTCLK	0		0.2V_{DD}	V
Low level input voltage (2)	V_{IL2}		RDIN, #RDRC	0		0.3V_{DD}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	RDIN, OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, #IRQ, EXTCLK, #RDRC (RDIN = Low)	0		0.5	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	RDIN, OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, #RDRC, #IRQ, EXTCLK	-0.5		0	µA
High level output current	I_{OH}	V_{OH}=0.9V_{DD}	SDO, #DET, #RDET, #PQUAL			-1.5	mA
Low level output current	I_{OL}	V_{OL}=0.1V_{DD}	SDO, #DET, #RDET, #PQUAL, #IRQ, #RDRC	2.5			mA
V_{REF} output voltage	V_{REF}				V_{DD}/2		V
Input impedance	R_{IN}		INP, INN, HOOK, EXTREF, CASIN	10			MΩ
	R_{CDIN}		CDIN	140	200	260	kΩ

● Current Consumption

(Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	Zero-power mode (PDWN=High)	V_{DD}=5V			1.0	µA
		FSK energy detection mode (PDWN=High)	V_{DD}=5V		6.0	8.0	µA
		Power up mode (no signal inputs)	V_{DD}=5V		3.0		mA
			V_{DD}=3V		1.8		mA

● Crystal Oscillation Characteristics

(Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, C_G=C_D=18pF, Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	3.579545MHz oscillator			20	msec

● FSK Demodulation Circuit Characteristics

FSK AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	TRATE		1188	1200	1212	Baud
Bell 202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell 202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V2}		2068	2100	2132	Hz
SN ratio	SNR		20	–	–	dB
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CDONFSK	V_{DD}=5V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-5dB	-47.2	-45.2	-43.2	dBV
		V_{DD}=3V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.2	-45.2	-43.2	dBV
Carrier-detect OFF sensitivity ∗1	CDOFFFSK	V_{DD}=5V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-5dB	-49.2	-47.2	-45.2	dBV
		V_{DD}=3V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.2	-47.2	-45.2	dBV

∗1: When the gain in the input amp is set to G_{AMP} (dB), the CDONFSK and CDOFFFSK values (Typ.) can be calculated from the equation below.

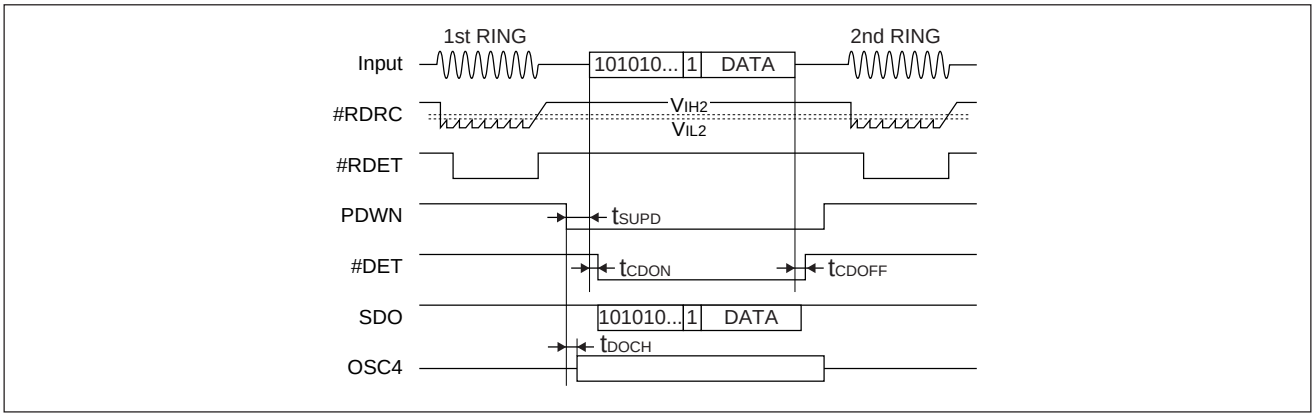
CD_{ONFSK} [dBm] = $-G_{AMP}$ - 48.0 + $20\log(\frac{V_{DD}}{5})$ [dBm], CD_{ONFSK} [dBV] = $-G_{AMP}$ - 50.2 + $20\log(\frac{V_{DD}}{5})$ [dBV]

CD_{OFFFSK} [dBm] = $-G_{AMP}$ - 50.0 + $20\log(\frac{V_{DD}}{5})$ [dBm], CD_{OFFFSK} [dBV] = $-G_{AMP}$ - 52.2 + $20\log(\frac{V_{DD}}{5})$ [dBV]

FSK switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PDWN fall → FSK	t_{SUPD}				20	msec
Carrier detect start time	t_{CDON}		5	10	15	msec
Data end → #DET rise	t_{CDOFF}		5	10	15	msec
PDWN rise → Oscillation start	t_{DOCH}	V_{DD}=5V		7	12	msec
		V_{DD}=3V		10	15	msec



FSK energy detection mode characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	TRATE		1188	1200	1212	Baud
Bell 202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell 202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V2}		2068	2100	2132	Hz
SN ratio	SNR		20	–	–	dB
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CDONFSK	V_{DD}=5V	-44.0	-41.0	-38.0	dBm
		Input amp gain (G_{AMP})=-5dB	-46.2	-43.2	-40.2	dBV
		V_{DD}=3V	-44.0	-41.0	-38.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-46.2	-43.2	-40.2	dBV

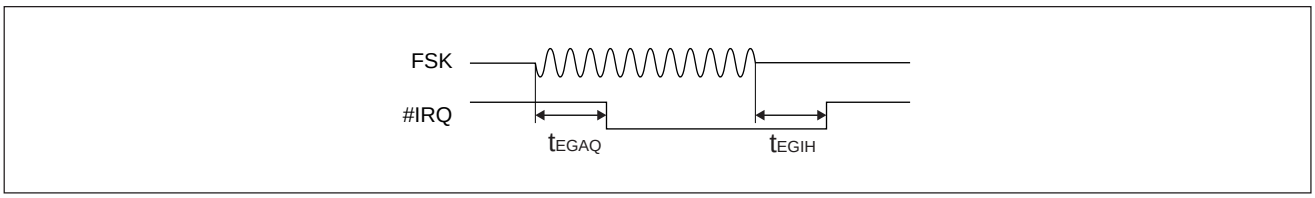
∗1: When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONFSK} value (Typ.) can be calculated from the equation below.

CD_{ONFSK} [dBm] = $-G_{AMP}$ - 46.0 + $20\log(\frac{V_{DD}}{5})$ [dBm], CD_{ONFSK} [dBV] = $-G_{AMP}$ - 48.2 + $20\log(\frac{V_{DD}}{5})$ [dBV]

FSK energy detection mode switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FSK energy detect capture time	t_{EGAQ}	V_{DD}=5V		12	20	msec
FSK end → #IRQ rise	t_{EGIH}	V_{DD}=5V		24	40	msec



● Dual-Tone (CAS) Detection Circuit Characteristics

CAS AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect sensitivity *1 (input level at TPI/RING)	CD_{ONTONE}	V_{DD}=5V, Bellcore mode Input amp gain (G_{AMP})=-5dB Tone filter gain=-4dB	-39.9	-35.9	-31.9	dBm
		V_{DD}=5V, BT mode *2 Input amp gain (G_{AMP})=-5dB Tone filter gain=-4dB	-48.1	-44.1	-40.1	dBV
		V_{DD}=3V, BT mode *2 Input amp gain (G_{AMP})=-9.4dB Tone filter gain=-4dB	-39.9	-35.9	-31.9	dBm
		V_{DD}=3V, BT mode *2 Input amp gain (G_{AMP})=-9.4dB Tone filter gain=-4dB	-48.1	-44.1	-40.1	dBV
Low tone frequency	f_{LTONE}	Bellcore (±0.5%)	2119.35	2130	2140.65	Hz
		BT line disconnected	2110	2130	2150	Hz
		BT line connected (±0.6%)	2117.22	2130	2142.78	Hz
High tone frequency	f_{HTONE}	Bellcore (±0.5%)	2736.25	2750	2763.75	Hz
		BT line disconnected	2720	2750	2780	Hz
		BT line connected (±0.6%)	2733.50	2750	2766.50	Hz

*1: When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONTONE} value (Typ.) can be calculated from the equation below. (When the internal tone filter gain = -4 dB)

$$CD_{ONTONE}\ [dBm] = -G_{AMP} - 40.9 + 20\log(\frac{V_{DD}}{5})\ [dBm],\quad CD_{ONTONE}\ [dBV] = -G_{AMP} - 49.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

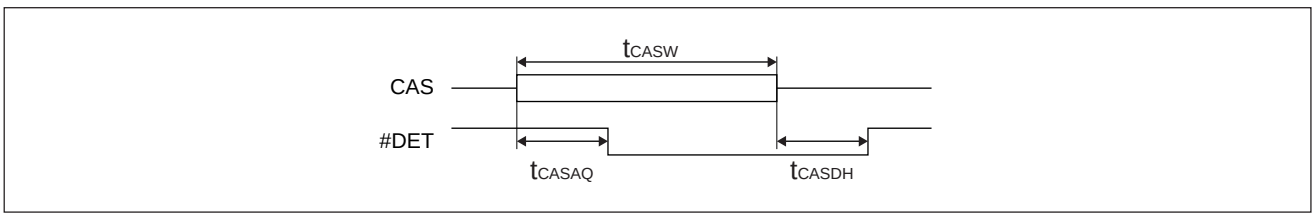
*2: BT mode is selected by setting the mode register (address = 0h) bit 2 to 1. By this setting, the gain in each dual-tone filter is raised +6 dB for adjustment to the British Telecom CD level.

CAS switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CAS detect capture time	t_{CASAQ}		2.8×(N+2)+16.9		msec
CAS end → #DET rise	t_{CASDH}		2.8×(31-N)+13.1		msec
CAS width	t_{CASW}	75	80	85	msec

N = TH0 × 16 + TL3 × 8 + TL2 × 4 + TL1 × 2 + TL0



● Call Progress Mode (CPM) Detection Circuit Characteristics

CPM AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect ON sensitivity *1 (input level at TPI/RING)	CD_{ONCPM}	V_{DD}=5V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-5dB	-47.2	-45.2	-43.2	dBV
		V_{DD}=3V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.2	-45.2	-43.2	dBV
Carrier-detect OFF sensitivity *1	CD_{OFFCPM}	V_{DD}=5V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-5dB	-49.2	-47.2	-45.2	dBV
		V_{DD}=3V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.2	-47.2	-45.2	dBV

*1: When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONCPM} and CD_{OFFCPM} values (Typ.) can be calculated from the equation below.

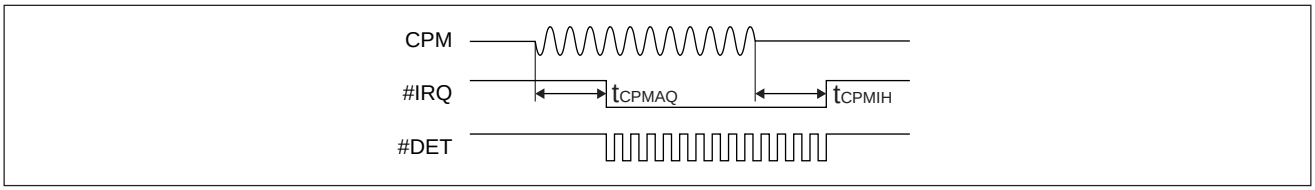
$$CD_{ONCPM}\ [dBm] = -G_{AMP} - 48.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{ONCPM}\ [dBV] = -G_{AMP} - 50.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

$$CD_{OFFCPM}\ [dBm] = -G_{AMP} - 50.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{OFFCPM}\ [dBV] = -G_{AMP} - 52.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

CPM switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CPM tone-detect capture time	t_{CPMAQ}		25		msec
CPM tone end → #IRQ rise	t_{CPMIH}		30		msec

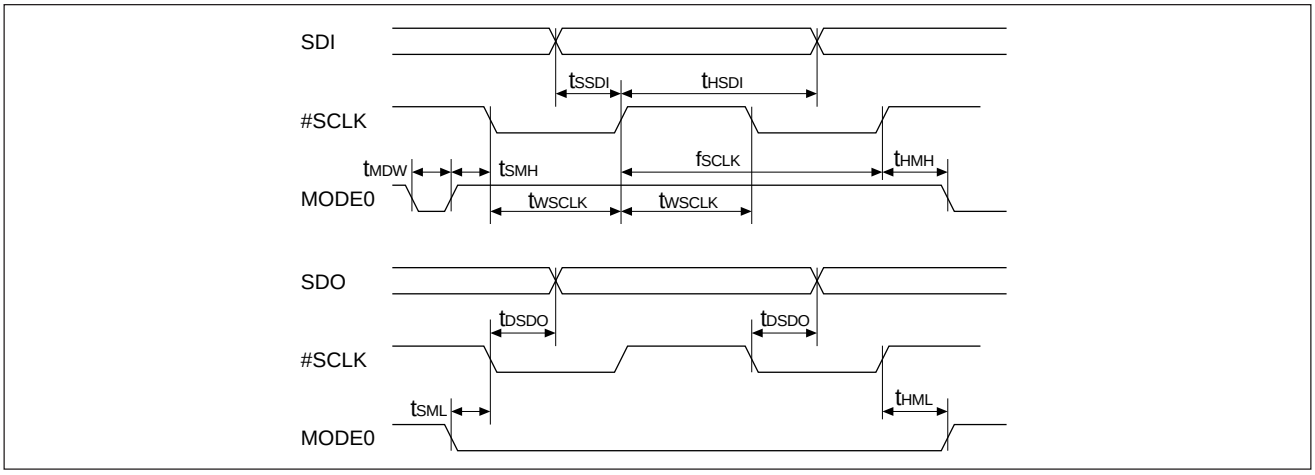


● Serial Interface Circuit Characteristics

Serial interface AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF)

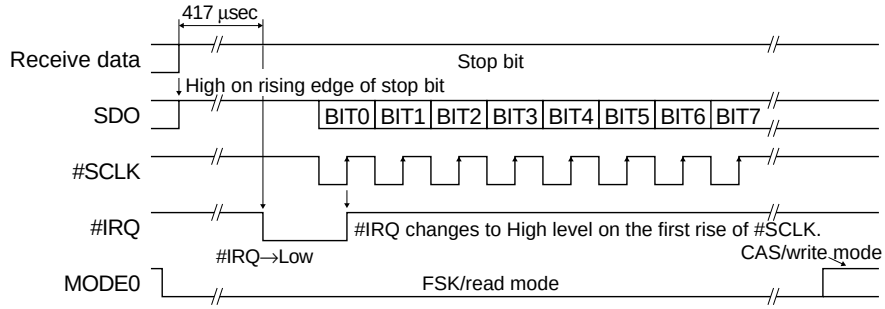
Parameter	Symbol	Min.	Typ.	Max.	Unit
#SCLK frequency	f_{SCLK}			1	MHz
#SCLK pulse width	t_{WSCLK}	400			nsec
SDI setup time	t_{SSDI}	250			nsec
SDI hold time	t_{HSDI}	500			nsec
SDO delay time	t_{DSDO}			250	nsec
MODE0 High setup time	t_{SMH}	1			µsec
MODE0 High hold time	t_{HMH}	1			µsec
MODE0 Low setup time	t_{SML}	1			µsec
MODE0 Low hold time	t_{HML}	1			µsec
MODE0 Low pulse width	t_{MDW}	1			µsec



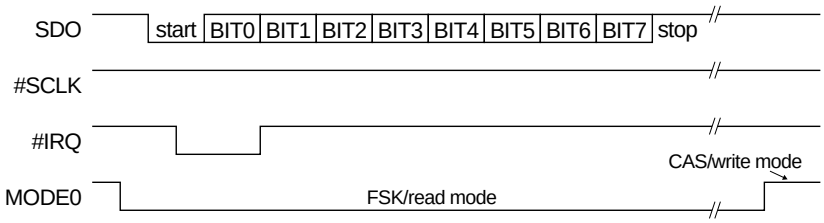
FSK demodulated data read mode

The FSK signal fed to the INP and INN pins is demodulated into 8-bit asynchronous (start-stop) data. The demodulated data is then sampled by the internal 8-bit shift register. When the data has been stored in the shift register, the #IRQ pin changes to Low level, indicating that the data can be read by the host CPU.
If the MODE pin is set to Low level and synchronoμs mode has been selected (MDR[0] = 1), the host CPU reads out the 8-bit data synchronously with the clock signal fed from the host CPU to the #SCLK pin. The figure below shows the timing at which this data is read. Each bit of the 8-bit data is output from the SDO pin synchronously with falling edges of the #SCLK clock signal, beginning with bit 0. The host CPU latches each bit into the internal logic at rising edges of the #SCLK clock signal.
If the MODE pin is set to Low level and asynchronous mode has been set (MDR[0] = 0), the data is output from the SDO pin at a transfer rate of 1,200 baud. The clock signal from the host CPU is unnecessary. The host CPU latches the data synchronously with the start bit.

<Data read timing in synchronous mode>

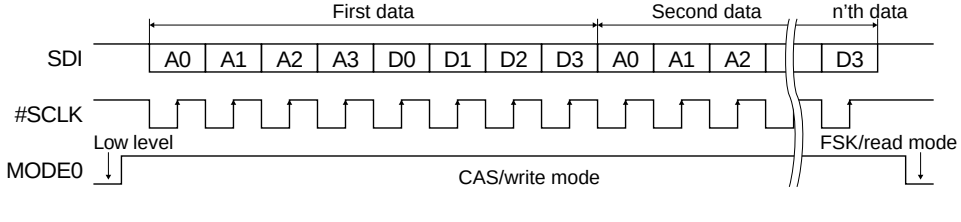


<Data read timing in asynchronous mode>



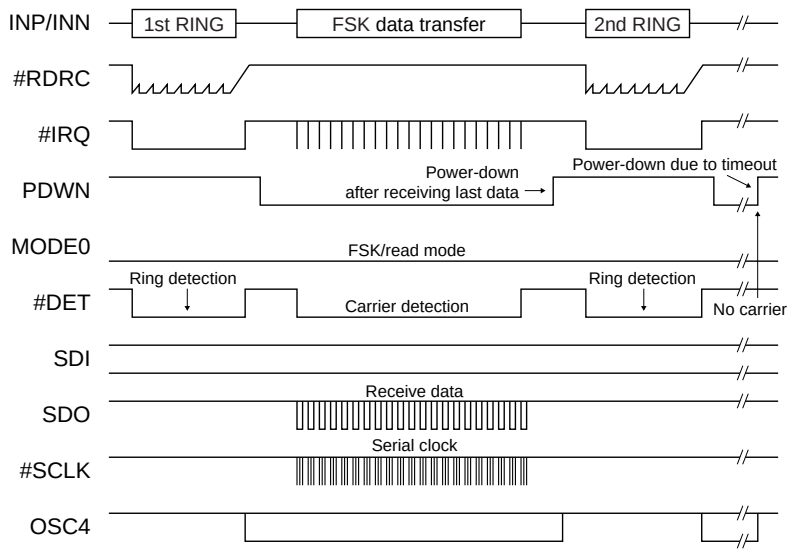
CAS detection circuit control-register write mode

The host CPU can write 4-bit data to the internal registers through the SDI pin in order to set each control bit. The host CPU must temporarily pull the MODE pin to Low level to initialize the write control circuit before it can write data. Then, after releasing the MODE pin back to High level, the host CPU must be held at High level while writing data to the internal register. The data input to the SDI pin is sampled at rising edges of the clock signal fed from the host CPU to the #SCLK pin. The first four bits of data sent from the host CPU are the address A[3:0] of the internal register to be accessed. The subsequent four bits are the data bits D[3:0] to be written to the specified register. The data is input beginning with the LSB.

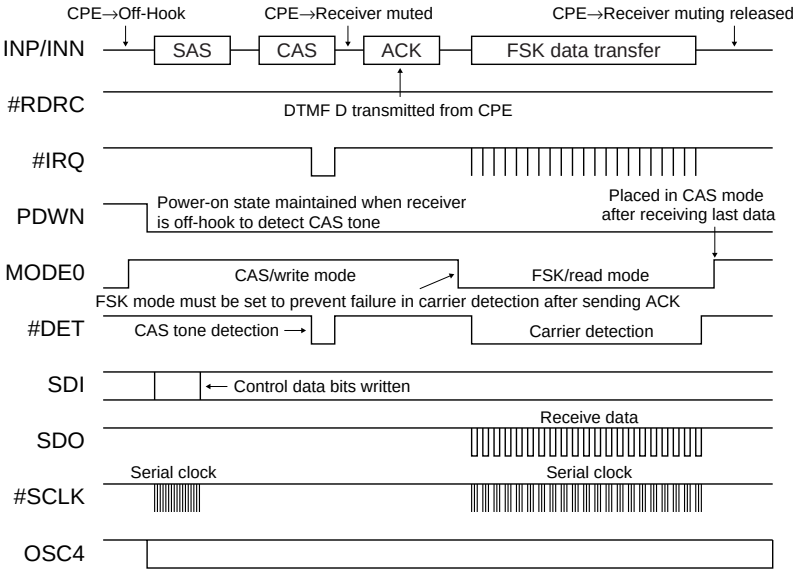


● S1C05251 Timing Chart

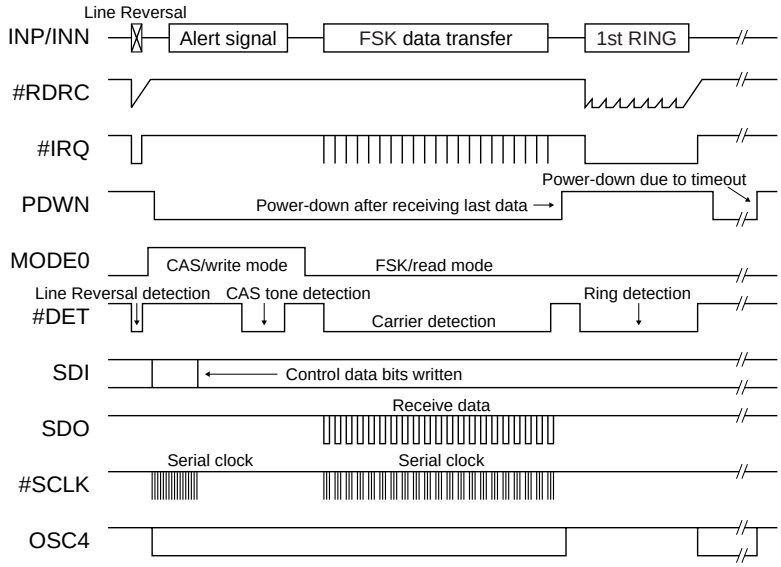
Bellcore on-hook data transfer



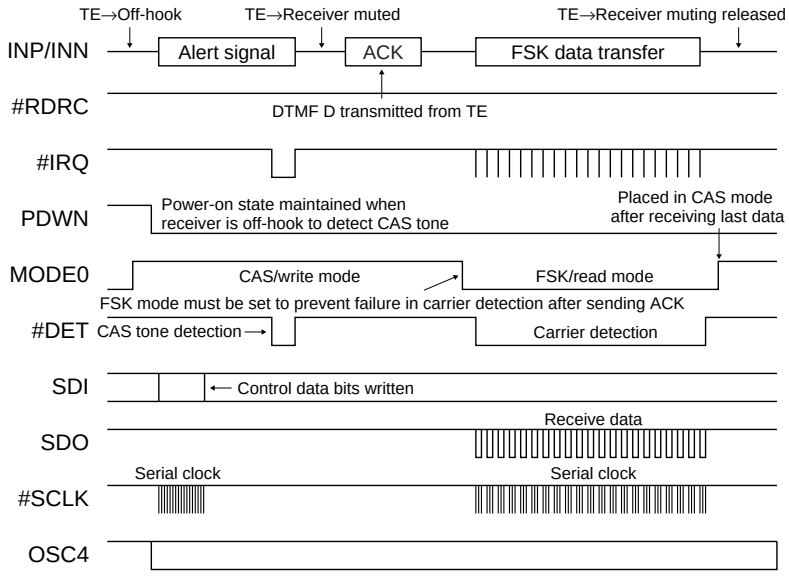
Bellcore off-hook data transfer



BT Idle State CLI service

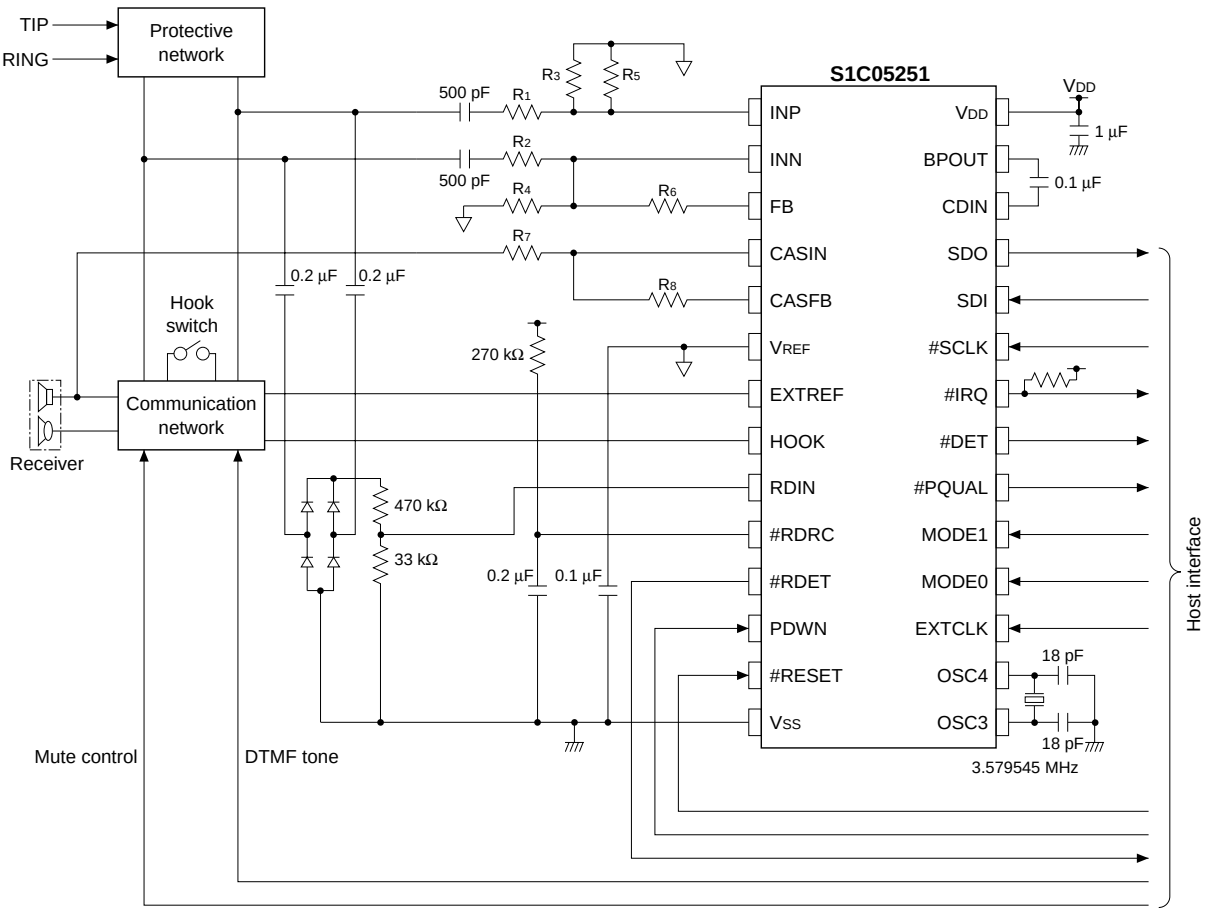


BT Loop State CLI service



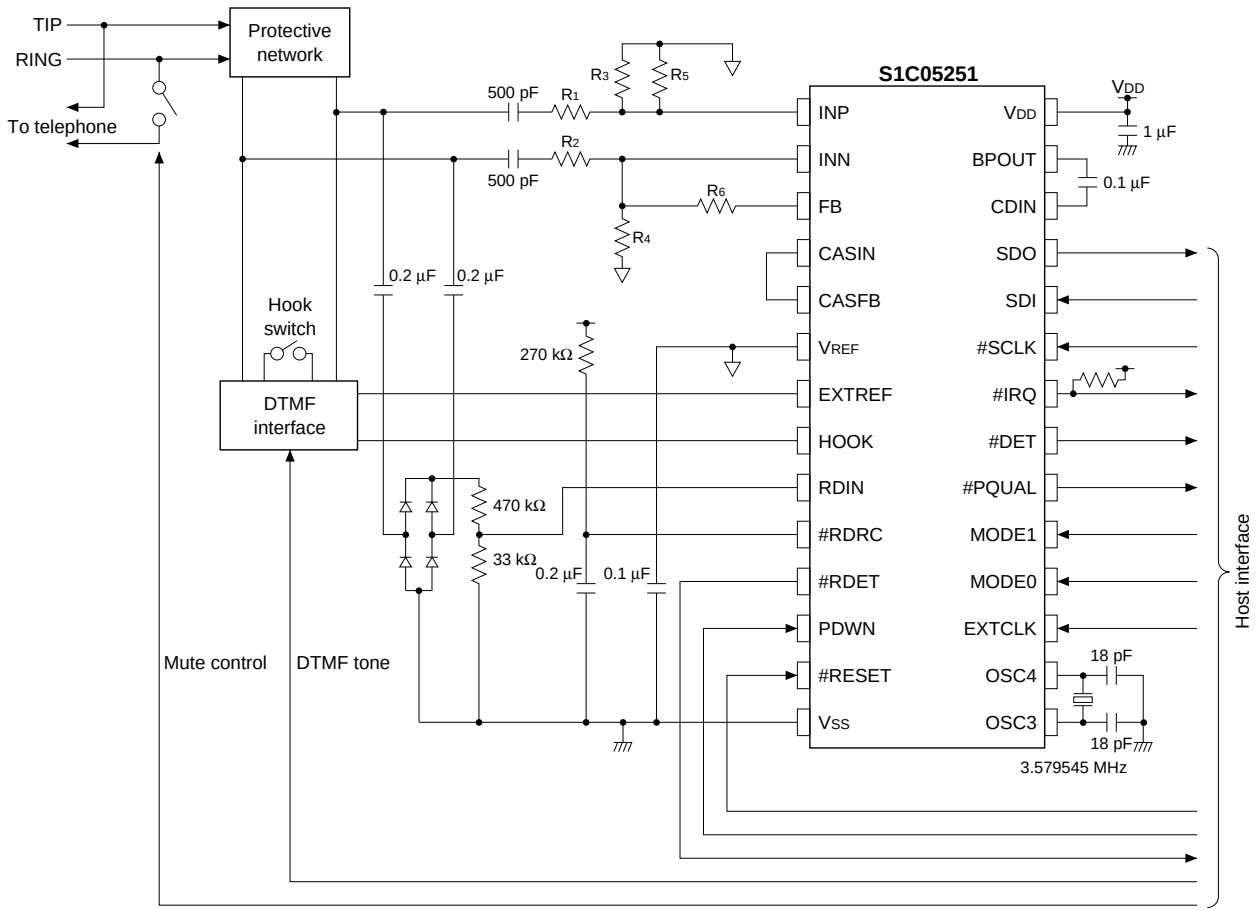
● External Wiring Diagram (Example)

Example of Bellcore-compatible telephone circuit



Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

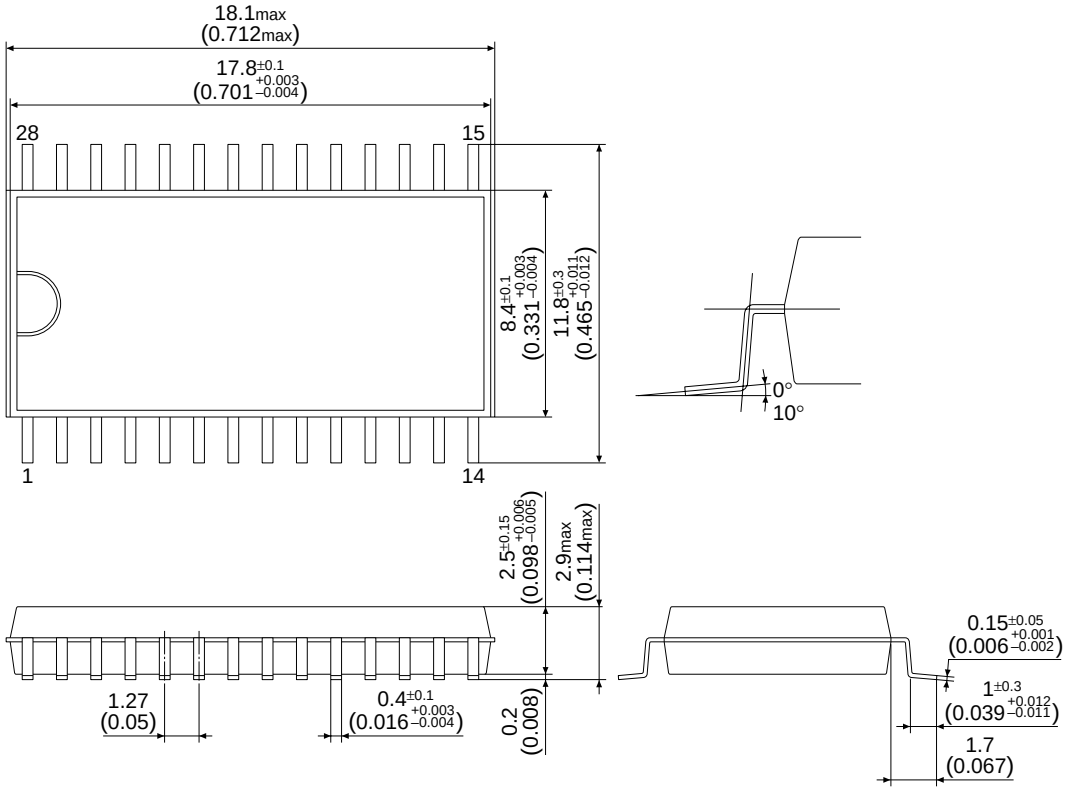
Example of Bellcore-compatible auxiliary circuit



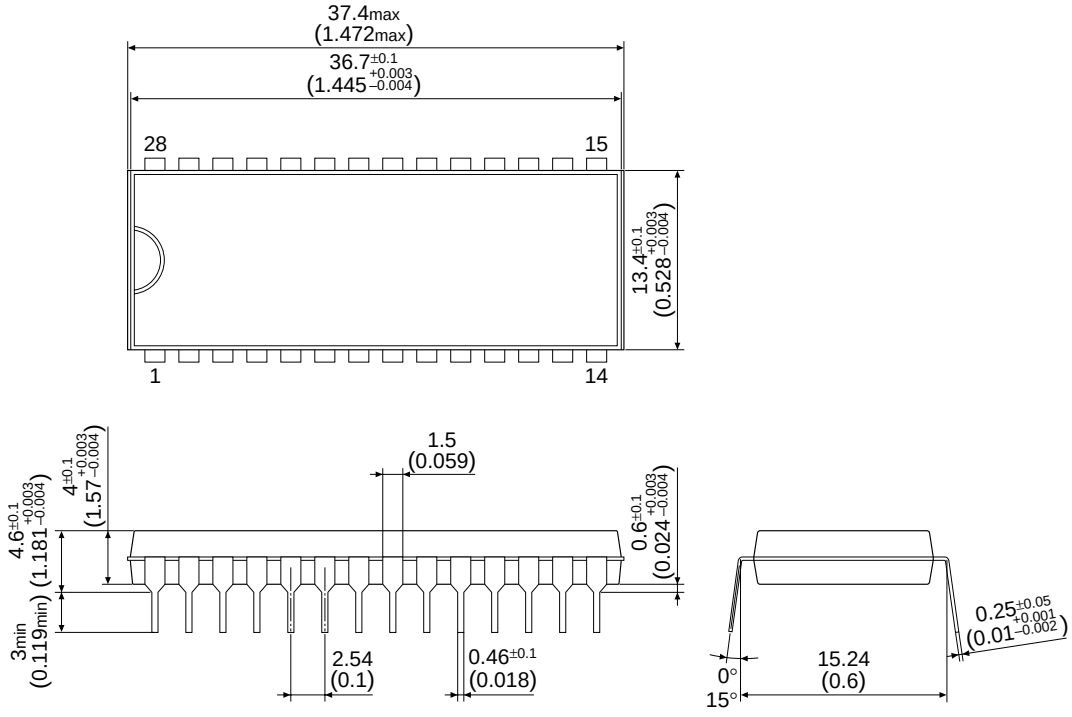
Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

■ PACKAGE DIMENSIONS

SOP2-28pin Plastic Package



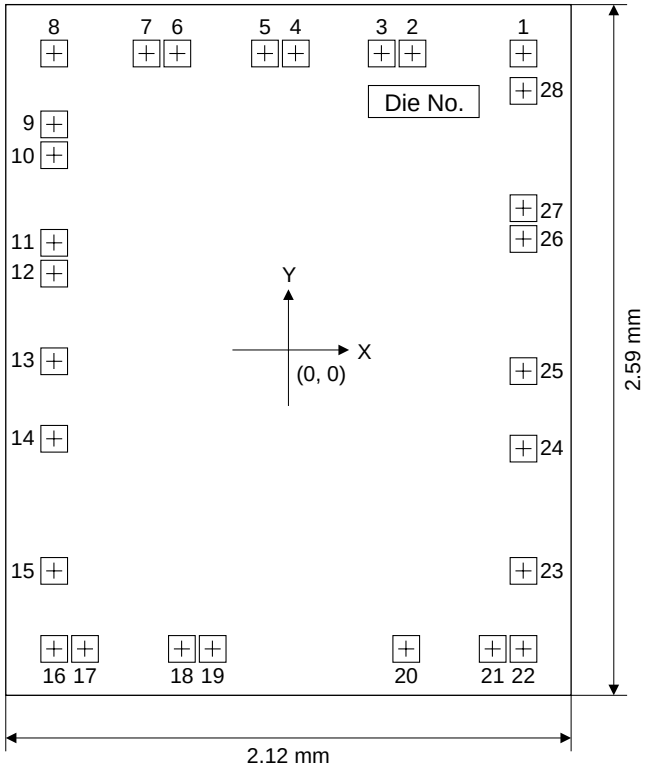
DIP-28pin Ceramic Package



Unit: mm (inch)

■ PAD LAYOUT

● Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

● Pad Coordinates

(Unit: µm)

Pad No.	Pad name	X coordinate	Y coordinate	Pad No.	Pad name	X coordinate	Y coordinate
1	SD0	879.9	1116.3	15	#RDET	-879.8	-823.8
2	CDIN	463.7	1116.3	16	PDWN	-879.8	-1116.4
3	BPOUT	348.2	1116.3	17	#RESET	-764.3	-1116.4
4	V_{DD}	26.1	1116.3	18	V_{SS}	-401.0	-1116.4
5	INP	-89.4	1116.3	19	OSC3	-285.5	-1116.4
6	INN	-418.1	1116.3	20	OSC4	440.3	-1116.4
7	FB	-533.6	1116.3	21	EXTCLK	764.4	-1116.4
8	CASIN	-879.8	1116.3	22	MODE0	879.9	-1116.4
9	CASFB	-879.8	850.5	23	MODE1	879.9	-823.8
10	V_{REF}	-879.8	735.0	24	#PQUAL	879.9	-365.3
11	EXTREF	-879.8	406.4	25	#DET	879.9	-74.7
12	HOOK	-879.8	290.9	26	#IRQ	879.9	420.8
13	RDIN	-879.8	-37.8	27	#SCLK	879.9	536.3
14	#RDRC	-879.8	-328.4	28	SDI	879.9	976.1

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