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S1C6P366

4-bit Single Chip Microcomputer

● Function Evaluation Flash built-in
● Compatible with S1C63358 and 158
● On-board writing supported

Low Voltage Operation Products

■ DESCRIPTION

The S1C6P366 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, rewritable PROM, RAM, serial interface, watchdog timer, programmable timer, time base counter (1 system), SVD circuit, a segment type LCD driver (32 segments × 4 commons), A/D converter and a special input port that can implement key position discrimination function using with the A/D converter. The S1C6P366 has a built-in large capacity PROM (16K × 13 bits) and RAM (2K × 4 bits) that are compatible with the S1C63358 and S1C63158, it can therefore be used for program development.

■ FEATURES

● OSC1 oscillation circuit .... 32.768 kHz (Typ.) crystal oscillation circuit
● OSC3 oscillation circuit .... 1.8 MHz (Typ.) CR or 4 MHz (Max.) ceramic oscillation circuit (∗1)
● Instruction set .... Basic instruction: 46 types (411 instructions with all)
Addressing mode: 8 types
● Instruction execution time .... At 32.768 kHz operation: Min. 61 µsec
At 4 MHz operation: Min. 0.5 µsec
● PROM capacity .... Code PROM: 16,384 words × 13 bits
Segment option PROM: 2,048 words × 4 bits
Programming method: Parallel or serial programming
(exclusive PROM writer is used)
Rewriting: 100 times
● RAM capacity .... Data memory: 2,048 words × 4 bits
Display memory: 32 words × 4 bits
● Input port .... 9 bits   8 bits (with pull-up resistors)
1 bit (for key position sensing interrupt by A/D)
● Output port .... 12 bits   (2 special outputs are available ∗2)
● I/O port .... 20 bits   (4 serial inputs/outputs are available ∗2)
(4 A/D inputs are available ∗2)
● Serial interface .... 1 port   (8-bit clock synchronous system)
● LCD driver .... 32 segments × 4, 3 or 2 commons (∗2), 1/3 bias drive
● Time base counter .... 1 system (clock timer)
● Programmable timer .... Built-in, 2 channels × 8 bits or 1 channel × 16 bits (∗2),
with event counter function
● Watchdog timer .... Built-in
● A/D converter .... 8-bit resolution
Maximum error: ±3 LSB, A/D clock: OSC1, OSC3 (2.7 V to 5.5 V)
● Buzzer output .... Buzzer frequency: 2 kHz or 4 kHz (∗2), 2 Hz interval output (∗2)
● Supply voltage detection (SVD) circuit .... 2 values, programmable (2.7 V, 2.8 V)
● External interrupt .... Input port interrupt: 2 systems
Key sensing interrupt: 1 system
● Internal interrupt .... Clock timer interrupt: 4 systems
Programmable timer interrupt: 2 systems
Serial interface interrupt: 1 system
A/D converter: 1 system

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● Power supply voltage .... 2.7 V to 5.5 V
● Operating temperature range .... -20°C to 70°C
● Current consumption (Typ.) .... Single clock:

	During HALT (32 kHz)	3.0 V (LCD power OFF)	2.5 µA
		3.0 V (LCD power ON)	37 µA
	During operation (32 kHz)	3.0 V (LCD power ON)	120 µA
	Twin clock:		
	During operation (4 MHz)	3.0 V (LCD power ON)	800 µA
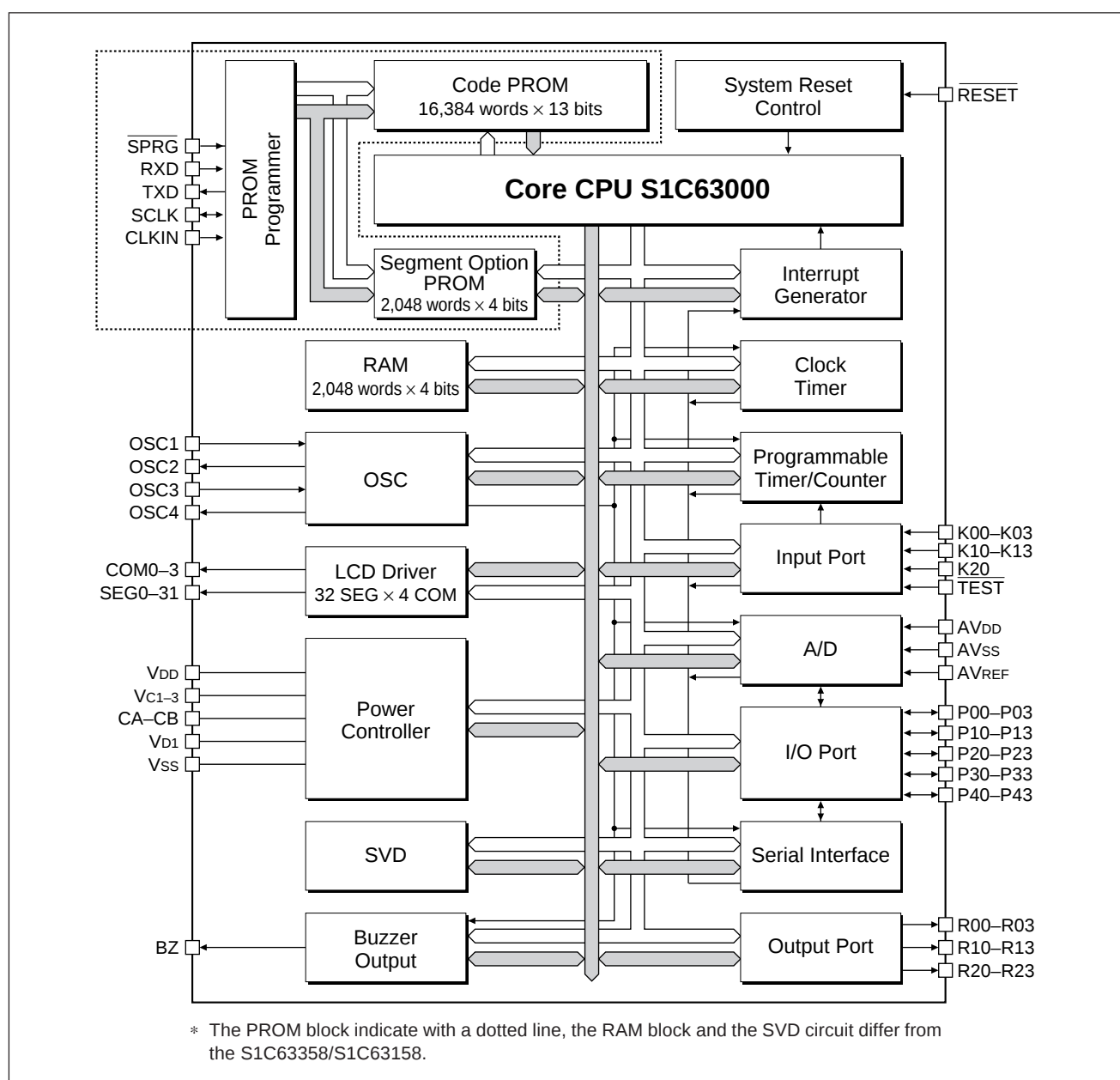
● Package .... QFP15-100pin (plastic) or chip

∗1: Can be selected with mask option   ∗2: Can be selected with software
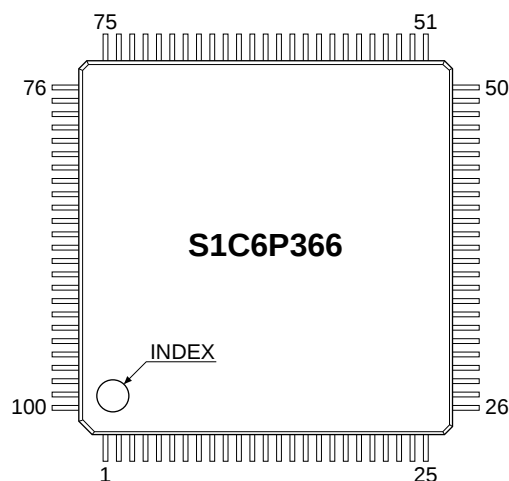
■ BLOCK DIAGRAM

∗ The PROM block indicate with a dotted line, the RAM block and the SVD circuit differ from the S1C63358/S1C63158.

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■ PIN CONFIGURATION

QFP15-100pin

No.	Pin name		No.	Pin name		No.	Pin name		No.	Pin name	
	S1C6P366	S1C63358		S1C6P366	S1C63358		S1C6P366	S1C63358		S1C6P366	S1C63358
1	SEG7	SEG7	26	CLKIN	N.C.	51	SCLK	N.C.	76	R13	R13
2	SEG8	SEG8	27	$\overline{\text{SPRG}}$	N.C.	52	P43	P43	77	R12	R12
3	SEG9	SEG9	28	COM0	COM0	53	P42	P42	78	R11	R11
4	SEG10	SEG10	29	COM1	COM1	54	P41	P41	79	R10	R10
5	SEG11	SEG11	30	COM2	COM2	55	P40	P40	80	R03	R03
6	SEG12	SEG12	31	COM3	COM3	56	P33	P33	81	R02	R02
7	SEG13	SEG13	32	CB	CB	57	P32	P32	82	R01	R01
8	SEG14	SEG14	33	CA	CA	58	P31	P31	83	R00	R00
9	SEG15	SEG15	34	V_{C3}	V_{C3}	59	P30	P30	84	BZ	BZ
10	SEG16	SEG16	35	V_{C2}	V_{C2}	60	P23	P23	85	K00	K00
11	SEG17	SEG17	36	V_{C1}	V_{C1}	61	P22	P22	86	K01	K01
12	SEG18	SEG18	37	V_{SS}	V_{SS}	62	P21	P21	87	K02	K02
13	SEG19	SEG19	38	OSC1	OSC1	63	P20	P20	88	K03	K03
14	SEG20	SEG20	39	OSC2	OSC2	64	P13	P13	89	K10	K10
15	SEG21	SEG21	40	V_{D1}	V_{D1}	65	P12	P12	90	K11	K11
16	SEG22	SEG22	41	OSC3	OSC3	66	P11	P11	91	K12	K12
17	SEG23	SEG23	42	OSC4	OSC4	67	P10	P10	92	K13	K13
18	SEG24	SEG24	43	V_{DD}	V_{DD}	68	P03	P03	93	K20	K20
19	SEG25	SEG25	44	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	69	P02	P02	94	SEG0	SEG0
20	SEG26	SEG26	45	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	70	P01	P01	95	SEG1	SEG1
21	SEG27	SEG27	46	AV_{REF}	AV_{REF}	71	P00	P00	96	SEG2	SEG2
22	SEG28	SEG28	47	AV_{DD}	AV_{DD}	72	R23	R23	97	SEG3	SEG3
23	SEG29	SEG29	48	AV_{SS}	AV_{SS}	73	R22	R22	98	SEG4	SEG4
24	SEG30	SEG30	49	RXD	N.C.	74	R21	R21	99	SEG5	SEG5
25	SEG31	SEG31	50	TXD	N.C.	75	R20	R20	100	SEG6	SEG6

N.C. : No Connection

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■ PIN DESCRIPTION

| Pin name	Pin No.	In/Out	Function
V_{DD}	43	–	Power (+) supply pin
V_{SS}	37	–	Power (–) supply pin
V_{D1}	40	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C3}	36–34	–	LCD system power supply pin 1/3 bias
CA, CB	33, 32	–	LCD system boosting/reducing capacitor connecting pin
OSC1	38	I	Crystal oscillation input pin
OSC2	39	O	Crystal oscillation output pin
OSC3	41	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	42	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	85–88	I	Input port
K10–K13	89–92	I	Input port
K20	93	I	Input port with control
P00–P03	71–68	I/O	I/O port
P10–P13	67–64	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	63–60	I/O	I/O port
P30–P33	59–56	I/O	I/O port
P40–P43	55–52	I/O	I/O port (can be used as A/D input)
R00	83	O	Output port
R01	82	O	Output port
R02	81	O	Output port (switching to TOUT output is possible by software)
R03	80	O	Output port (switching to FOUT output is possible by software)
R10–R13	79–76	O	Output port
R20–R23	75–72	O	Output port
COM0–COM3	28–31	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG31	94–100, 1–25	O	LCD segment output pin
AV_{DD}	47	–	Power (+) supply pin for A/D converter
AV_{SS}	48	–	Power (–) supply pin for A/D converter
AV_{REF}	46	–	Reference voltage for A/D converter
BZ	84	O	Buzzer output pin
$\overline{RESET}$	44	I	Initial reset input pin
$\overline{TEST}$	45	I	Testing input pin
RXD [*1]	49	I	Serial data input pin for Flash programming
TXD [*1]	50	O	Serial data output pin for Flash programming
SCLK [*1]	51	I/O	Serial clock input/output pin for Flash programming
CLKIN [*1]	26	I	Clock input pin for Flash programming
$\overline{SPRG}$ [*1]	27	I	Control pin for Flash programming
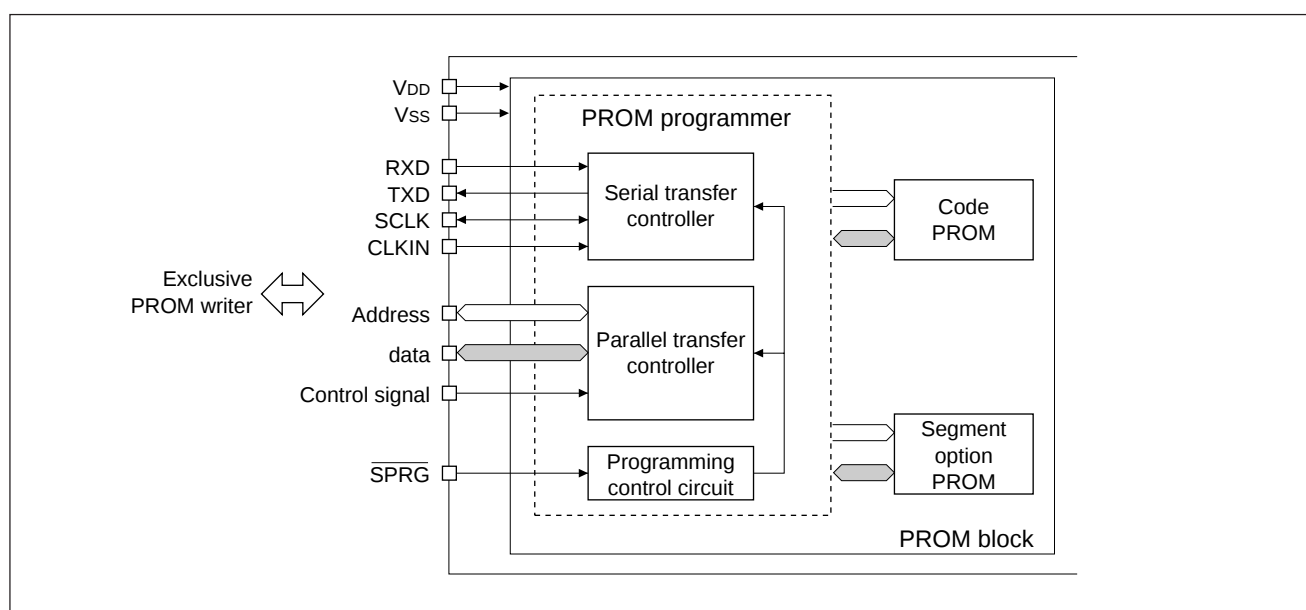
*1   N.C. in S1C63358
Refer to "PROM Programmer and Operating Mode", for the Flash programming pins.

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■ PROM PROGRAMMING AND OPERATING MODE

The S1C6P366 has built-in Flash EEPROMs as the code PROM and the segment option PROM that allow the developer to program the PROM data using the exclusive PROM writer (Universal ROM Writer II (S5U1C88000W1)). This chapter explains the PROM programmer that controls data writing and the writing mode.

● Configuration of PROM Programmer

The configuration of the PROM programmer is shown below.

The PROM programmer supports the following two writing modes.
1) Serial Programming
2) Parallel Programming

Serial programming mode uses the serial communication ports of the PROM writer and S1C6P366 to write data. This mode enables on-board programming by designing the target board with a serial writing function. In parallel programming mode, the on-chip PROM can be directly programmed using the exclusive PROM writer with the adaptor socket installed. Refer to "Operating Mode", for each programming method.

Terminals
The S1C6P366 provides the following terminals for programming the Flash EEPROM.

$\overline{\text{SPRG}}$: Flash programming control terminal (pull-up resistor built-in)
       When set to High ... Normal operation mode (The CPU executes the program in the Flash EEPROM.)
       When set to Low .... Programming mode (for writing data to the Flash EEPROM)
SCLK: Serial transfer clock input/output terminal for Serial Programming (pull-up resistor built-in)
RXD: Serial data input terminal for Serial Programming (pull-up resistor built-in)
TXD: Serial data output terminal for Serial Programming
CLKIN: PROM programmer clock input terminal (1 MHz; pull-up resistor built-in)

The five terminals above are provided exclusively for the Flash EEPROM. The S1C63358 and S1C63158 do not have these terminals.

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● **Operating Mode**

Three operating modes are available in the S1C6P366: one is for normal operation and the others are for programming.

The operating mode is decided by the terminal setting at power-on or initial reset.

When the $\overline{\text{SPRG}}$ terminal is set to Low, the S1C6P366 enters serial programming mode. To operate the S1C6P366 in normal operation mode (to execute the instruction written to the Flash EEPROM after programming), the $\overline{\text{SPRG}}$ terminal should be set to High or open.

The parallel programming including the mode switching and terminal settings is controlled by the exclusive PROM writer.

The following table lists the operating modes.

Operating mode	$\overline{\text{SPRG}}$ terminal
Normal mode	High or open
Serial programming mode	Set by PROM writer
Parallel programming mode	Set by PROM writer

Normal Operation Mode

In this mode, the S1C63000 core CPU and the peripheral circuits operate by the instructions programmed in the Flash EEPROM. Note that inspection data is written to the PROM at shipment.

In normal operation mode, set the terminals for programming the Flash EEPROM as as below. The board must be designed so that the terminal settings cannot be changed while the IC is operating.

Terminal	Setting
$\overline{\text{SPRG}}$	High or open
SCLK	High or open
RXD	High or open
TXD	Open
CLKIN	High or open

When the $\overline{\text{SPRG}}$ terminal is set to Low, the S1C6P366 starts operating in serial programming mode after power-on or an initial reset. Be sure not to change the $\overline{\text{SPRG}}$ terminal status during normal operation, because the operating mode may change according to the terminal status.

Serial Programming Mode

Serial programming mode writes data to the Flash EEPROM using a serial communication between the exclusive PROM writer (Universal ROM Writer II) and the S1C6P366. By providing a serial communication port on the target board, the S1C6P366 on the board can be programmed (on-board writing).

Terminal	Setting
$\overline{\text{SPRG}}$	Connected to PROM writer
SCLK	Connected to PROM writer
RXD	Connected to PROM writer
TXD	Connected to PROM writer
CLKIN	Connected to PROM writer

The serial programming is performed using the 1 MHz clock supplied from the PROM writer to the CLKIN terminal. Take noise measure into consideration so that noise does not affect the clock line input to the CLKIN terminal when designing the target board.

Parallel Programming Mode

The parallel programming can be performed by installing the S1C6P366 to the exclusive PROM writer via the adaptor socket. In this mode, it is not necessary to set up the programming terminals since it is controlled by the exclusive PROM writer.

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■ DIFFERENCES FROM THE MASK ROM MODELS

This section explains the differences in functions (except for the Flash EEPROM block) between the S1C6P366 and the mask ROM models (S1C63358 and S1C63158).

● Mask Option

The S1C6P366 cannot specify the S1C63358 and S1C63158 mask options individually. The following option combination is provided for the S1C6P366.

Note: Recommended LCD segment option data is include in the S5U1C6P366Y1 package. Modifying the LCD segment opotion is done at the user's own risk. For the LCD segment specifications, both the segment allocation and the output specification can be selected similarly to the S1C63358. Create segment option data using the segment option generator SOG63358 and write it to the segment option PROM in the S1C6P366. The selected option specifications are automatically set to each segment terminal.

Mask option		S1C6P366E (Type E)	S1C6P366F (Type F)
OSC1 oscillation circuit		Crystal (32.768 kHz)	Crystal (32.768 kHz)
OSC3 oscillation circuit		Ceramic	CR
Multiple key reset combination		Not used	Not used
Multiple key reset time authorize		Not used	Not used
Input port pull-up resistors	K00	With pull-up resistor	With pull-up resistor
	K01	With pull-up resistor	With pull-up resistor
	K02	With pull-up resistor	With pull-up resistor
	K03	With pull-up resistor	With pull-up resistor
	K10	With pull-up resistor	With pull-up resistor
	K11	With pull-up resistor	With pull-up resistor
	K12	With pull-up resistor	With pull-up resistor
	K13	With pull-up resistor	With pull-up resistor
	K20	With pull-up resistor	With pull-up resistor
Output port output specifications	R10–R13	Complementary output	Complementary output
	R20–R23	Complementary output	Complementary output
I/O port output specifications	P10–P13	Complementary output	Complementary output
	P20	Complementary output	Complementary output
	P21	Complementary output	Complementary output
	P22	Complementary output	Complementary output
	P23	Complementary output	Complementary output
	P30	Complementary output	Complementary output
	P31	Complementary output	Complementary output
	P32	Complementary output	Complementary output
	P33	Complementary output	Complementary output
	P40	Complementary output	Complementary output
	P41	Complementary output	Complementary output
	P42	Complementary output	Complementary output
	P43	Complementary output	Complementary output
I/O port pull-up resistors	P10–P13	With pull-up resistor	With pull-up resistor
	P20	With pull-up resistor	With pull-up resistor
	P21	With pull-up resistor	With pull-up resistor
	P22	With pull-up resistor	With pull-up resistor
	P23	With pull-up resistor	With pull-up resistor
	P30	With pull-up resistor	With pull-up resistor
	P31	With pull-up resistor	With pull-up resistor
	P32	With pull-up resistor	With pull-up resistor
	P33	With pull-up resistor	With pull-up resistor
	P40	No pull-up resistor	No pull-up resistor
	P41	No pull-up resistor	No pull-up resistor
	P42	No pull-up resistor	No pull-up resistor
	P43	No pull-up resistor	No pull-up resistor
LCD drive bias		1/3 bias (internal)	1/3 bias (internal)
Serial interface signal polarity		Negative polarity	Negative polarity
Buzzer output specification		Negative polarity	Negative polarity

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● **Pin Aassignment Comparison List (S1C6P366: QFP15-100pin, S1C63158: QFP12-48pin)**

| S1C6P366 | | S1C63158 | | S1C6P366 | | S1C63158 | | S1C6P366 | | S1C63158 | | S1C6P366 | | S1C63158 | |
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG7	–	–	26	**CLKIN**	–	– (∗1)	51	**SCLK**	–	– (∗1)	76	R13	30	R13
2	SEG8	–	–	27	$\overline{\text{SPRG}}$	–	– (∗1)	52	P43	14	P43	77	R12	31	R12
3	SEG9	–	–	28	COM0	–	–	53	P42	15	P42	78	R11	32	R11
4	SEG10	–	–	29	COM1	–	–	54	P41	16	P41	79	R10	33	R10
5	SEG11	–	–	30	COM2	–	–	55	P40	17	P40	80	R03	34	R03
6	SEG12	–	–	31	COM3	–	–	56	P33	–	–	81	R02	35	R02
7	SEG13	–	–	32	CB	11	CB	57	P32	–	–	82	R01	37	R01
8	SEG14	–	–	33	CA	12	CA	58	P31	–	–	83	R00	38	R00
9	SEG15	–	–	34	V_{C3}	–	–	59	P30	–	–	84	BZ	39	BZ
10	SEG16	–	–	35	V_{C2}	13	V_{C2}	60	P23	18	P23	85	K00	40	K00
11	SEG17	–	–	36	V_{C1}	–	–	61	P22	19	P22	86	K01	41	K01
12	SEG18	–	–	37	V_{SS}	1	V_{SS}	62	P21	20	P21	87	K02	42	K02
13	SEG19	–	–	38	OSC1	2	OSC1	63	P20	21	P20	88	K03	43	K03
14	SEG20	–	–	39	OSC2	3	OSC2	64	P13	22	P13	89	K10	44	K10
15	SEG21	–	–	40	V_{D1}	4	V_{D1}	65	P12	23	P12	90	K11	45	K11
16	SEG22	–	–	41	OSC3	5	OSC3	66	P11	24	P11	91	K12	46	K12
17	SEG23	–	–	42	OSC4	6	OSC4	67	P10	25	P10	92	K13	47	K13
18	SEG24	–	–	43	V_{DD}	7	V_{DD}	68	P03	26	P03	93	K20	48	K20
19	SEG25	–	–	44	$\overline{\text{RESET}}$	8	$\overline{\text{RESET}}$	69	P02	27	P02	94	SEG0	–	–
20	SEG26	–	–	45	$\overline{\text{TEST}}$	9	$\overline{\text{TEST}}$	70	P01	28	P01	95	SEG1	–	–
21	SEG27	–	–	46	AV_{REF}	10	V_{REF}	71	P00	29	P00	96	SEG2	–	–
22	SEG28	–	–	47	AV_{DD}	–	–	72	R23	–	–	97	SEG3	–	–
23	SEG29	–	–	48	AV_{SS}	–	–	73	R22	–	–	98	SEG4	–	–
24	SEG30	–	–	49	**RXD**	–	– (∗1)	74	R21	–	–	99	SEG5	–	–
25	SEG31	–	–	50	**TXD**	–	– (∗1)	75	R20	–	–	100	SEG6	–	–

∗1 : Pin for serial programming

● **Pin Aassignment Comparison List (S1C6P366: QFP15-100pin, S1C63158: QFP13-64pin)**

| S1C6P366 | | S1C63158 | | S1C6P366 | | S1C63158 | | S1C6P366 | | S1C63158 | | S1C6P366 | | S1C63158 | |
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG7	–	–	26	**CLKIN**	–	– (∗1)	51	**SCLK**	–	– (∗1)	76	R13	41	R13
2	SEG8	–	–	27	$\overline{\text{SPRG}}$	–	– (∗1)	52	P43	17	P43	77	R12	42	R12
3	SEG9	–	–	28	COM0	–	–	53	P42	18	P42	78	R11	43	R11
4	SEG10	–	–	29	COM1	–	–	54	P41	19	P41	79	R10	44	R10
5	SEG11	–	–	30	COM2	–	–	55	P40	20	P40	80	R03	45	R03
6	SEG12	–	–	31	COM3	–	–	56	P33	21	P33	81	R02	46	R02
7	SEG13	–	–	32	CB	13	CB	57	P32	22	P32	82	R01	52	R01
8	SEG14	–	–	33	CA	14	CA	58	P31	23	P31	83	R00	53	R00
9	SEG15	–	–	34	V_{C3}	–	–	59	P30	24	P30	84	BZ	54	BZ
10	SEG16	–	–	35	V_{C2}	15	V_{C2}	60	P23	25	P23	85	K00	55	K00
11	SEG17	–	–	36	V_{C1}	–	–	61	P22	26	P22	86	K01	56	K01
12	SEG18	–	–	37	V_{SS}	1	V_{SS}	62	P21	27	P21	87	K02	57	K02
13	SEG19	–	–	38	OSC1	2	OSC1	63	P20	28	P20	88	K03	58	K03
14	SEG20	–	–	39	OSC2	3	OSC2	64	P13	29	P13	89	K10	59	K10
15	SEG21	–	–	40	V_{D1}	4	V_{D1}	65	P12	30	P12	90	K11	60	K11
16	SEG22	–	–	41	OSC3	5	OSC3	66	P11	31	P11	91	K12	61	K12
17	SEG23	–	–	42	OSC4	6	OSC4	67	P10	32	P10	92	K13	62	K13
18	SEG24	–	–	43	V_{DD}	7	V_{DD}	68	P03	33	P03	93	K20	63	K20
19	SEG25	–	–	44	$\overline{\text{RESET}}$	8	$\overline{\text{RESET}}$	69	P02	34	P02	94	SEG0	–	–
20	SEG26	–	–	45	$\overline{\text{TEST}}$	9	$\overline{\text{TEST}}$	70	P01	35	P01	95	SEG1	–	–
21	SEG27	–	–	46	AV_{REF}	12	V_{REF}	71	P00	36	P00	96	SEG2	–	–
22	SEG28	–	–	47	AV_{DD}	10	AV_{DD}	72	R23	37	R23	97	SEG3	–	–
23	SEG29	–	–	48	AV_{SS}	11	AV_{SS}	73	R22	38	R22	98	SEG4	–	–
24	SEG30	–	–	49	**RXD**	–	– (∗1)	74	R21	39	R21	99	SEG5	–	–
25	SEG31	–	–	50	**TXD**	–	– (∗1)	75	R20	40	R20	100	SEG6	–	–

∗1 : Pin for serial programming

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● **Power Supply**

Since the S1C6P366 is produced using the Flash EEPROM process, the characteristics are different from those of the mask ROM models.

1) Operating voltage range

S1C6P366:   2.7 to 5.5V
S1C63358:   2.3 to 3.6V (Min. 0.9V when the OSC3 is not used)
S1C63158:   2.2 to 3.6V (Min. 0.9V when the OSC3 is not used)

The circuit blocks of the S1C6P366 except for the oscillation circuit and LCD driver (CPU, PROM, RAM and peripheral digital circuits) operate with the source voltage supplied between the V_{DD} and V_{SS} terminals. Therefore, the VDC register (I/O memory address: FF00H, data bit: D0) is invalidated and is used as a general-purpose register. Writing "1" or "0" to this register does not affect the V_{D1} output voltage level.

S1C63158

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	2.1 V	1.3 V	CPU operating voltage switch (1.3 V: OSC1, 2.1 V: OSC3)

S1C63358

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	2.25 V	1.35 V	CPU operating voltage switch (1.35 V: OSC1, 2.25 V: OSC3)

S1C6P366

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	(OSC3)	(OSC1)	(Operating voltage switch, CPU clock switch)

∗ In the S1C6P366, the V_{D1} level is fixed at 2.05V regard less of the VDC register value.

2) Operating mode of oscillation system voltage regulator

The operating mode range of the S1C6P366 is different from that of the S1C63358 and S1C63158 because the operable voltage range is different.

S1C63158

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.35	1.35–2.2	2.2–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	1.3	V_{C2} mode	Normal mode		Not allowed
	OSC3 (2 MHz)	2.1	Not allowed		Normal mode	Not allowed

S1C63358

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.4	1.4–2.3	2.3–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	1.3	V_{C2} mode	Normal mode		Not allowed
	OSC3 (4 MHz)	2.25	Not allowed		Normal mode	Not allowed

S1C6P366

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.4	1.4–2.7	2.7–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	2.05	Not allowed		Normal mode	
	OSC3 (4 MHz)	V_{DD}	Not allowed		Normal mode	

∗ The S1C6P366 does not enter the V_{C2} mode.
The internal circuits of the S1C63358 and S1C63158 operate with the oscillation system regulated voltage (V_{D1}). The S1C6P366 internal circuits operate with the supply voltage (V_{DD}).

3) Power supply terminal for the oscillation circuit (V$_{D1}$)

The V$_{D1}$ voltage that is generated by the internal voltage regulator is used only for the OSC1 oscillation circuit to stabilize the oscillation. As explained in Item 1 above, the VDC register (FF00H•D0) does not affect the V$_{D1}$ output voltage.

4) Operating mode of LCD system voltage regulator

The operable voltage range is different.

    S1C63358:   V$_{DD}$ = 0.9V to 1.4V   V$_{C1}$ = V$_{DD}$

                           V$_{DD}$ = 1.4V to 3.6V   V$_{C1}$ = 1.05V (Typ.)

    S1C6P366:   V$_{DD}$ = 2.7V to 5.5V   V$_{C1}$ = 1.05V (Typ.)

∗ The S1C6P366 operation is guaranteed within the above voltage range.

5) Operating mode of A/D converter power supply

The A/D converter operating mode range of the S1C6P366 is different from that of the S1C63358 and S1C63158 because the operable voltage range is different.

S1C63158

Circuit	Supply voltage V$_{DD}$ (V)		
	0.9–2.2	2.2–3.6	3.6–5.5
A/D converter	V$_{C2}$ mode	Normal mode	Not allowed

S1C63358
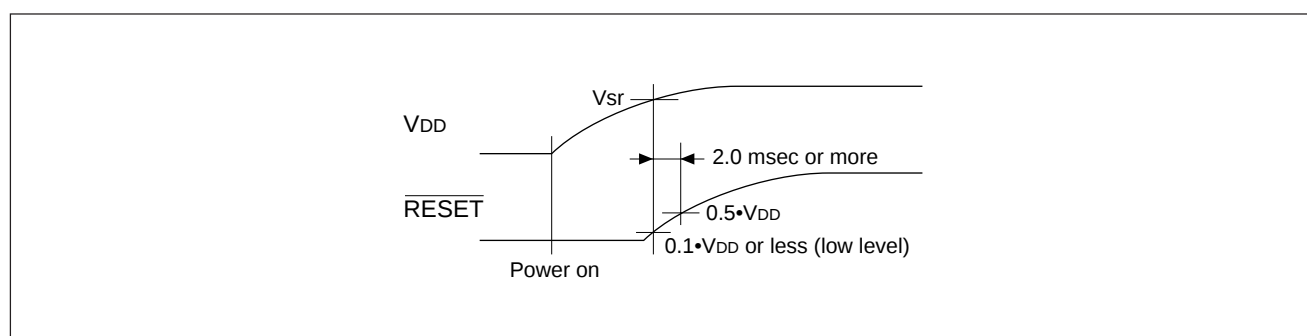
Circuit	Supply voltage V$_{DD}$ (V)		
	0.9–1.6	1.6–3.6	3.6–5.5
A/D converter	V$_{C2}$ mode	Normal mode	Not allowed

S1C6P366

Circuit	Supply voltage V$_{DD}$ (V)		
	0.9–2.7	2.7–3.6	3.6–5.5
A/D converter	Not allowed	Normal mode	

● **Initial Reset**

When the power is turned on, the reset terminal must be set at Low level until the supply voltage rises to the Vsr level.

The Vsr voltage level is different:

S1C63158:   Vsr = 1.3 V

S1C63358:   Vsr = 1.4 V

S1C6P366:   Vsr = 2.7 V

Furthermore, S1C6P366 uses the initial reset signal as a trigger for setting either the normal operation mode or the programming mode. Therefore, design the reset input circuit so that the IC will be reset for sure. Initial resetting during operation is the same as the S1C63358.

When resetting the IC in the normal operation mode, make sure to fix the $\overline{\text{SPRG}}$ terminal at High level or leave open.

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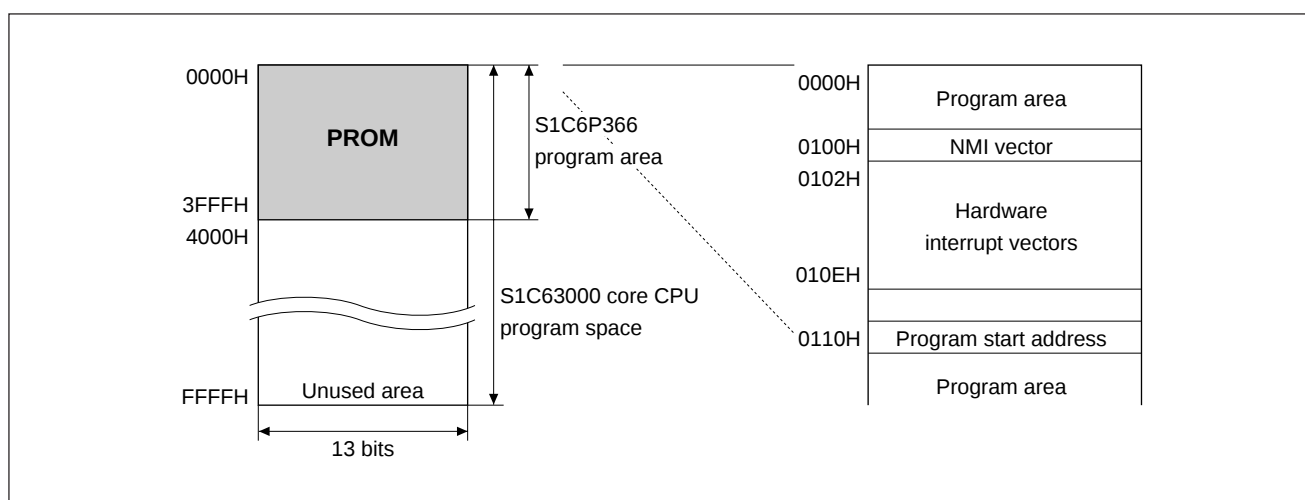
● **PROM, RAM**

The S1C6P366 employs a Flash EEPROM for the internal PROM. The Flash EEPROM can be rewritten up to 100 times. Rewriting data is done at the user's own risk.

1) Code PROM

The built-in code PROM is a Flash EEPROM for loading programs, and has a capacity of 16,384 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C6P366 is step 0000H to step 3FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

Note: Pay attention to the application program size since the code PROM of the S1C63358/S1C63158 is smaller (8,192 steps × 13 bits, 0000H–1FFFH) than that of the S1C6P366.
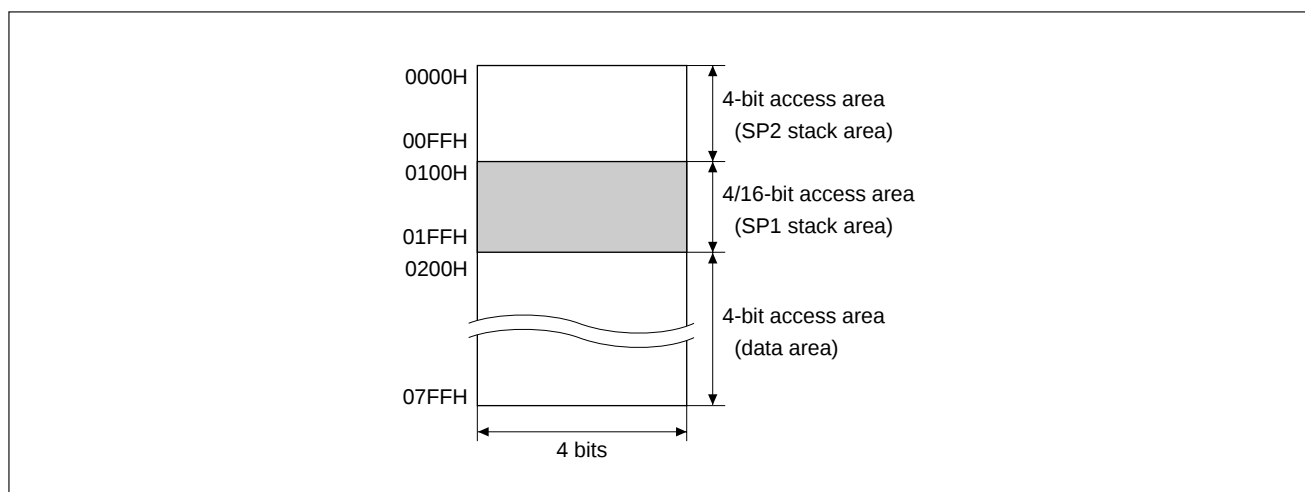
2) RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 2,048 words × 4 bits. The RAM area is assigned to addresses 0000H to 07FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data.
When programming, refer to the "Technical Manual" of the S1C63358 or S1C63158.

Note: Pay attention to the application data size since the RAM of the S1C63358/S1C63158 is smaller (512 words × 4 bits) than that of the S1C6P366.

S1C6P366

● **Oscillation Circuit**

In the S1C6P366, only crystal oscillation is available for the OSC1 oscillation circuit and either ceramic or CR oscillation is available for the OSC3 oscillation circuit. Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure to have enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

∗ The S1C6P366 has differences in its production process from the mask ROM models (S1C63358 and S1C63158). The constant must be decided according to the characteristics of the mask ROM model.

● **SVD Circuit**

The S1C6P366 has a built-in SVD (supply voltage detection) circuit the same as the S1C63358 and S1C63158. However, the detection levels are different from those of the S1C63358 and S1C63158. Furthermore, there is a great restriction on the operable detection levels in the S1C6P366. When using the SVD function, check the available detection level.

Detection level	S1C63158			S1C63358			S1C6P366		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
SVDS3–0 = "0"	0.95	1.05	1.15	0.95	1.05	1.15	Not allowed		
SVDS3–0 = "1"	1.05	1.10	1.15	1.02	1.10	1.18	Not allowed		
SVDS3–0 = "2"	1.10	1.15	1.20	1.07	1.15	1.23	Not allowed		
SVDS3–0 = "3"	1.15	1.20	1.25	1.12	1.20	1.28	Not allowed		
SVDS3–0 = "4"	1.20	1.25	1.30	1.16	1.25	1.34	Not allowed		
SVDS3–0 = "5"	1.25	1.30	1.35	1.21	1.30	1.39	Not allowed		
SVDS3–0 = "6"	1.35	1.40	1.45	1.30	1.40	1.50	Not allowed		
SVDS3–0 = "7"	1.55	1.60	1.65	1.49	1.60	1.71	Not allowed		
SVDS3–0 = "8"	1.90	1.95	2.00	1.81	1.95	2.09	Not allowed		
SVDS3–0 = "9"	1.95	2.00	2.05	1.86	2.00	2.14	Not allowed		
SVDS3–0 = "10"	2.00	2.05	2.10	1.91	2.05	2.19	Not allowed		
SVDS3–0 = "11"	2.05	2.10	2.15	1.95	2.10	2.25	Not allowed		
SVDS3–0 = "12"	2.15	2.20	2.25	2.05	2.20	2.35	Not allowed		
SVDS3–0 = "13"	2.25	2.30	2.35	2.14	2.30	2.46	Not allowed		
SVDS3–0 = "14"	2.45	2.50	2.55	2.33	2.50	2.68	2.50	2.70	2.90
SVDS3–0 = "15"	2.55	2.60	2.65	2.42	2.60	2.78	2.60	2.80	3.00

A criteria voltage can be set using the SVDS0–SVDS3 register (I/O memory address: FF04H).
Since the minimum operating voltage of the S1C6P366 is 2.7V, 2.7V or less criteria voltages are not available. Be aware that the SVD circuit in the S1C6P366 may not operate when a 2.7V or less criteria voltage is selected.
For the software control sequence of the SVD circuit, refer to the Technical Manual of the S1C63358 and S1C63158.

■ ELECTRICAL CHARACTERISTICS

Note: The electrical characteristics of the S1C6P366 are different from those of the S1C63358/S1C63158. The following characteristic values should be used as reference values when the S1C6P366 is used as a development tool.

● **Absolute Maximum Ratings**

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current ∗1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature ∗2	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	−
Permissible dissipation ∗3	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).
∗2: The storage temperature cannot guarantee data holding capability.
∗3: In case of plastic package (QFP15-100pin).

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● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Normal mode	2.7	3.0	5.5	V
	AV_{DD}	AV_{SS}=0V		2.7	3.0	5.5	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
	f_{OSC3}	CR oscillation			1800		kHz
		Ceramic oscillation				4100	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	0		0.5	μA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	-0.5		0	μA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	-16	-10	-5	μA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03, P10–13 P20–23, P30–33, P40–43, TXD, SCLK			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03, P10–13 P20–23, P30–33, P40–43, TXD, SCLK	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–3			-10	μA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			μA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–31			-10	μA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			μA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-220	μA
	I_{OL5}	V_{OL5}=0.1·V_{DD}		220			μA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	0		0.5	μA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	-0.5		0	μA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03, P10–13, P20–23 P30–33, P40–43, RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	μA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03, P10–13 P20–23, P30–33, P40–43, TXD, SCLK			-3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03, P10–13 P20–23, P30–33, P40–43, TXD, SCLK	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–3			-10	μA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			μA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–31			-10	μA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			μA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-660	μA
	I_{OL5}	V_{OL5}=0.1·V_{DD}		660			μA

S1C6P366

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2μF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C2} ×0.95		1/2·V_{C2} -0.1	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)		Typ. ×0.88	2.10	Typ. ×1.12	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3/2·V_{C2} ×0.95		3/2·V_{C2}	V
SVD voltage	V_{SVD}	SVDS0–3="0"		–	–	–	V
		SVDS0–3="1"		–	–	–	
		SVDS0–3="2"		–	–	–	
		SVDS0–3="3"		–	–	–	
		SVDS0–3="4"		–	–	–	
		SVDS0–3="5"		–	–	–	
		SVDS0–3="6"		–	–	–	
		SVDS0–3="7"		–	–	–	
		SVDS0–3="8"		–	–	–	
		SVDS0–3="9"		–	–	–	
		SVDS0–3="10"		–	–	–	
		SVDS0–3="11"		–	–	–	
		SVDS0–3="12"		–	–	–	
		SVDS0–3="13"		–	–	–	
		SVDS0–3="14"		2.50	2.70	2.90	
		SVDS0–3="15"		2.60	2.80	3.00	
SVD circuit response time	t_{SVD}					100	μS
Current consumption	I_{OP}	During HALT Normal mode LCD power OFF	32.768kHz		2.5	6	μA
		During HALT Normal mode *1 LCD power ON	32.768kHz		37	60	μA
		During execution Normal mode *1 LCD power ON	32.768kHz (Crystal oscillation)		120	200	μA
			1.8MHz (CR oscillation)		0.6	0.9	mA
			4MHz (Ceramic oscillation)		0.8	1.2	mA

*1: Without panel load. The SVD circuit and the A/D converter are OFF. AV_{REF} is open.

A/D Converter Characteristics

(Unless otherwise specified: AV_{DD}=V_{DD}=2.7 to 3.6V, AV_{SS}=V_{SS}=0V, Ta=-25 to 75°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Error		3.6V≤V_{DD}≤5.5V Fconv=OSC3/2 or OSC1	-3		3	LSB
		2.7V≤V_{DD}≤3.6V Fconv=OSC3/2 or OSC1	-3		3	LSB
Convertion time	t_{conv}	Fconv=OSC3/2=2MHz			10.5	μS
		Fconv=OSC1=32kHz			641	μS
Input voltage			AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		0.9		AV_{DD}	V
AV_{REF} resistance			15	50		kΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta}	t_{sta}≤3sec (V_{DD})	2.7			V
Oscillation stop voltage	V_{stp}	t_{stp}≤10sec (V_{DD})	2.7			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		18		pF
Frequency/voltage deviation	$\partial f/\partial V$	V_{DD}=2.7 to 5.5V			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	C_G=5 to 25pF		50		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	5.5			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

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OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=100pF, Ta=-20 to 70°C)
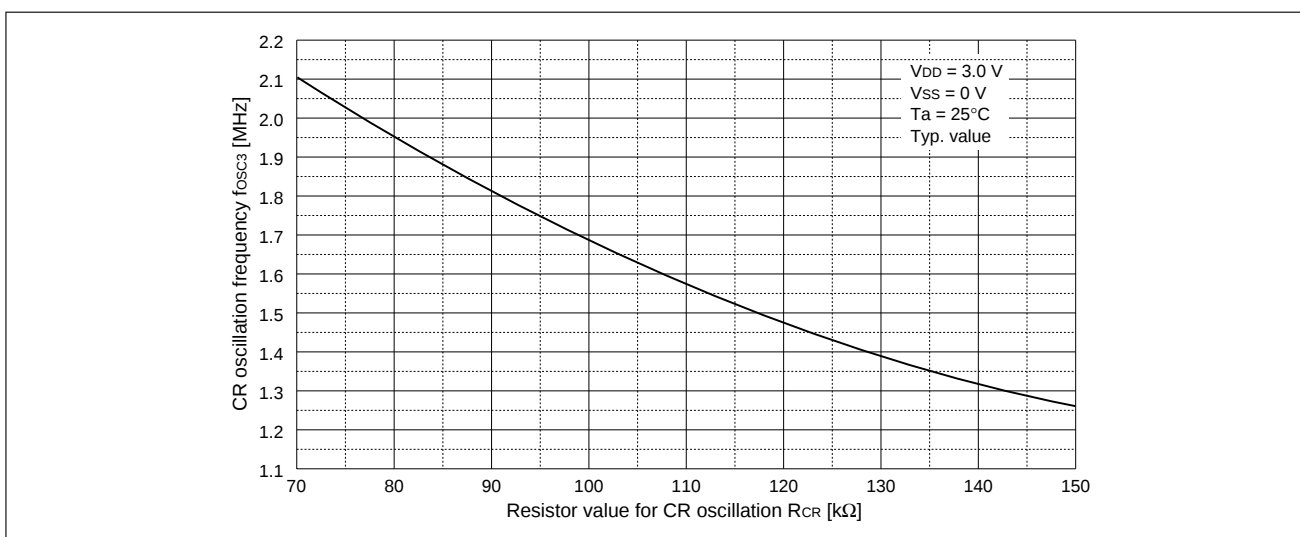
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.7			V
Oscillation start time	tsta	V_{DD}=2.7 to 5.5V			5	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.7			V

OSC3 CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR}=91kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1.8MHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.7			V
Oscillation start time	tsta	V_{DD}=2.7 to 5.5V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.7			V

OSC1 CR oscillation frequency-resistance characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.

● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	μS
Receiving data input set-up time	tsms	10			μS
Receiving data input hold time	tsmh	5			μS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})
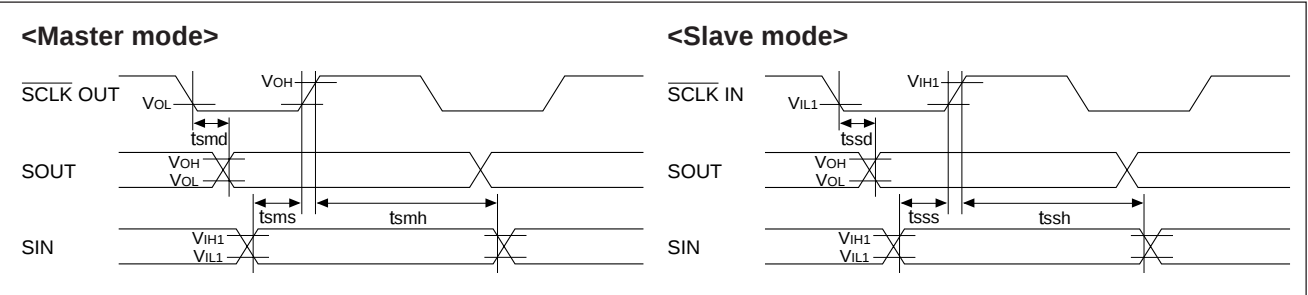
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	μS
Receiving data input set-up time	tsss	10			μS
Receiving data input hold time	tssh	5			μS

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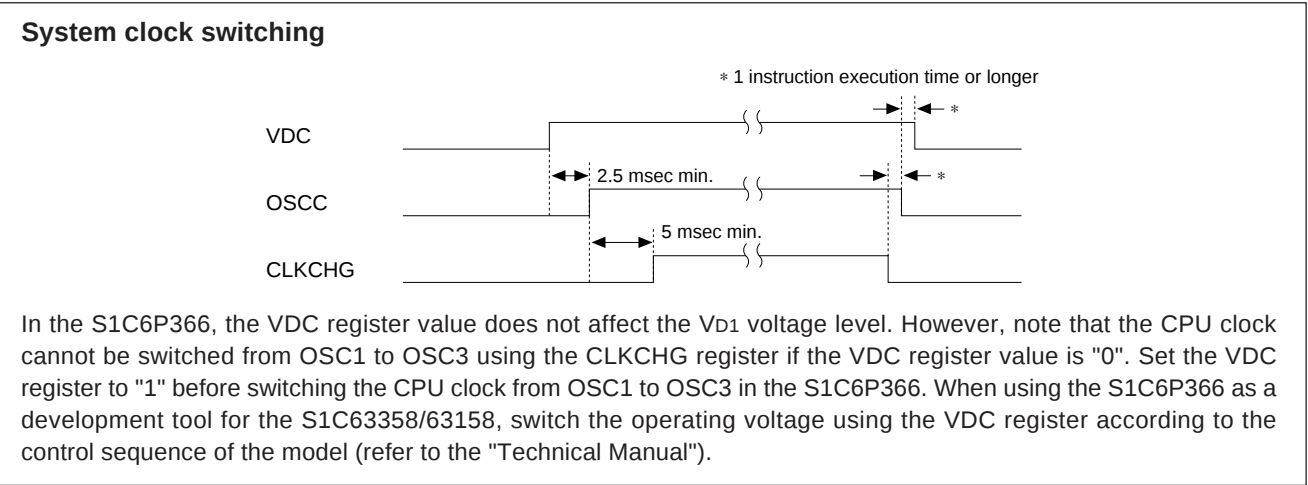
• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	t_{ssd}			500	nS
Receiving data input set-up time	t_{sss}	400			nS
Receiving data input hold time	t_{ssh}	200			nS

<Master mode>

SCLK OUT V_{OL} / V_{OH} t_{smd}

SOUT V_{OH} / V_{OL} t_{sms} t_{smh}

SIN V_{IH1} / V_{IL1}

<Slave mode>

SCLK IN V_{IL1} / V_{IH1} t_{ssd}

SOUT V_{OH} / V_{OL} t_{sss} t_{ssh}

SIN V_{IH1} / V_{IL1}

● **Timing Chart**

System clock switching

∗ 1 instruction execution time or longer

VDC

OSCC   2.5 msec min.   ∗

CLKCHG   5 msec min.
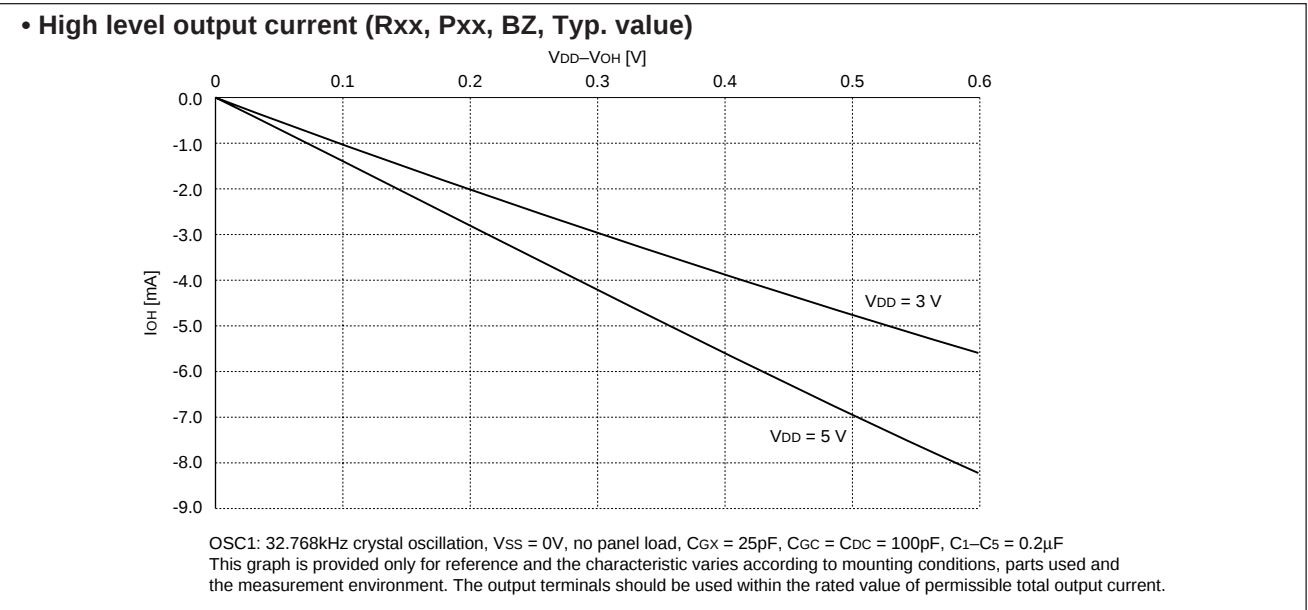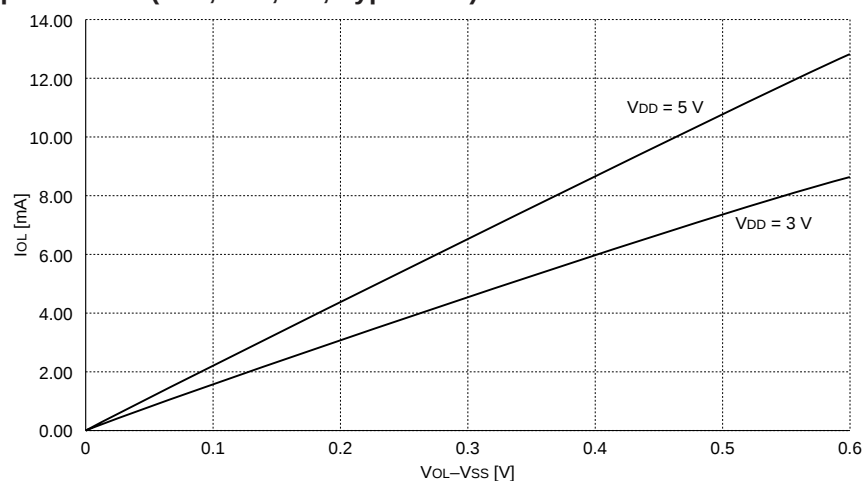
In the S1C6P366, the VDC register value does not affect the V_{D1} voltage level. However, note that the CPU clock cannot be switched from OSC1 to OSC3 using the CLKCHG register if the VDC register value is "0". Set the VDC register to "1" before switching the CPU clock from OSC1 to OSC3 in the S1C6P366. When using the S1C6P366 as a development tool for the S1C63358/63158, switch the operating voltage using the VDC register according to the control sequence of the model (refer to the "Technical Manual").

● **Characteristic Curves (reference value)**
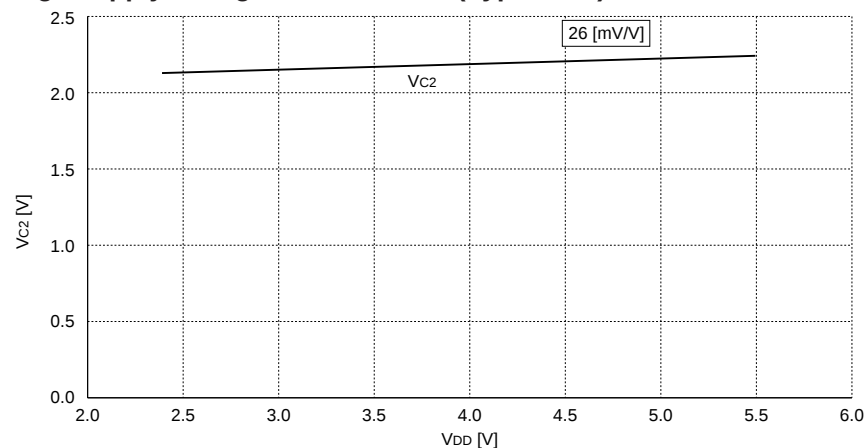
• High level output current (Rxx, Pxx, BZ, Typ. value)

V_{DD}–V_{OH} [V]

V_{DD} = 3 V

V_{DD} = 5 V

I_{OH} [mA]

OSC1: 32.768kHz crystal oscillation, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2μF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment. The output terminals should be used within the rated value of permissible total output current.

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• Low level output current (Rxx, Pxx, BZ, Typ. value)

OSC1: 32.768kHz crystal oscillation, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2μF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment. The output terminals should be used within the rated value of permissible total output current.

• V$_{C2}$ output voltage-temperature characteristic (Typ. value)
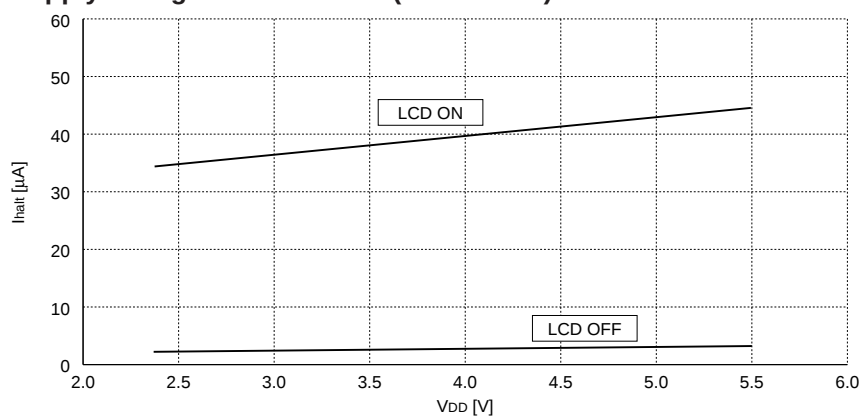
OSC1: 32.768kHz crystal oscillation, V_{DD} = 3V, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2μF
The LCD drive voltage output from the internal LCD drive power circuit varies depending on temperature. This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

• V$_{C2}$ output voltage-supply voltage characteristic (Typ. value)
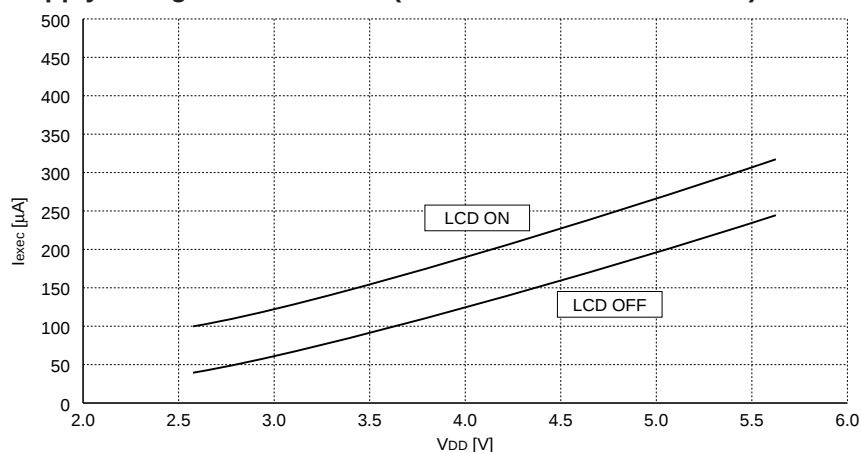
OSC1: 32.768kHz crystal oscillation, Ta =25°C, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2μF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

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• Power current-supply voltage characteristic (HALT state)
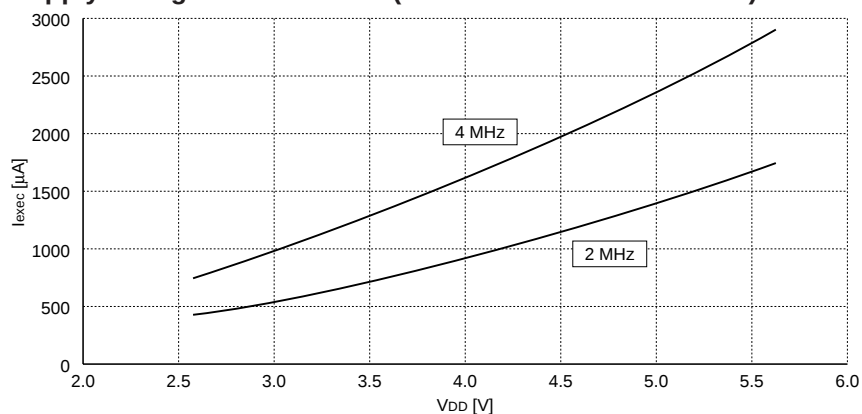
OSC1: 32.768kHz crystal oscillation, Ta =25°C, VSS = 0V, no panel load, CGX = 25pF, CGC = CDC = 100pF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

• Power current-supply voltage characteristic (RUN state with OSC1 clock)

OSC1: 32.768kHz crystal oscillation, Ta =25°C, VSS = 0V, no panel load, CGX = 25pF, CGC = CDC = 100pF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.
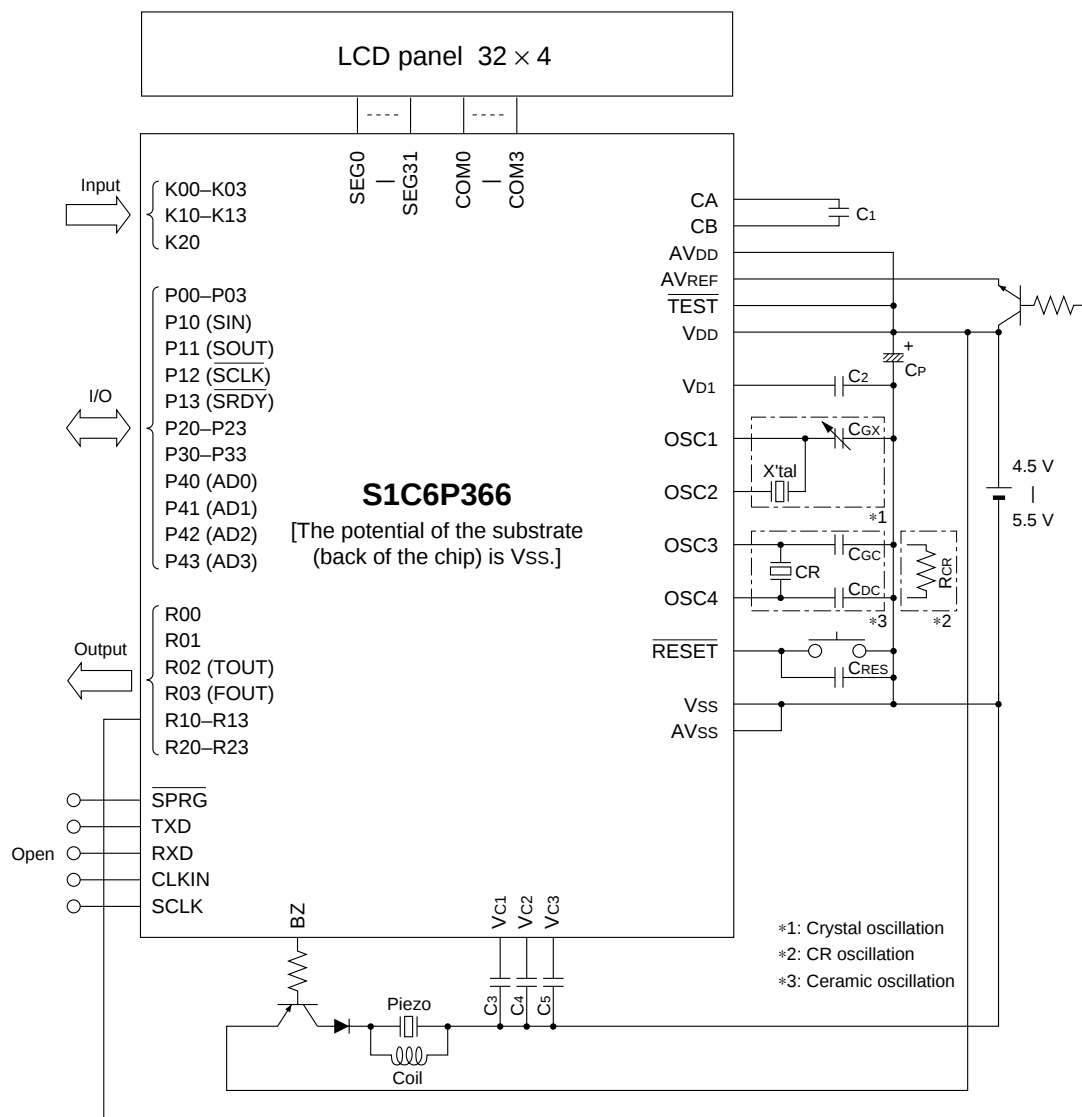
• Power current-supply voltage characteristic (RUN state with OSC3 clock)

OSC1: 32.768kHz crystal oscillation, Ta =25°C, VSS = 0V, no panel load, CGX = 25pF, CGC = CDC = 100pF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

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■ BASIC EXTERNAL CONNECTION DIAGRAM

• Normal operating mode <when used as S1C63358 OTP>

X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C_1–C_5	Capacitor	0.2 µF
C_P	Capacitor	3.3 µF
C_{RES}	$\overline{RESET}$ terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

• Normal operating mode <when used as S1C63158 OTP>

X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C_1–C_3	Capacitor	0.2 µF
C_P	Capacitor	3.3 µF
C_{RES}	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

• Serial programming mode (S1C88/S1C63 Serial Connector) <when used as S1C63358 OTP>

LCD panel 32 × 4

Input — K00–K03 / K10–K13 / K20

SEG0 — SEG31   COM0 — COM3

I/O —
P00–P03
P10 (SIN)
P11 (SOUT)
P12 ($\overline{\text{SCLK}}$)
P13 ($\overline{\text{SRDY}}$)
P20–P23
P30–P33
P40 (AD0)
P41 (AD1)
P42 (AD2)
P43 (AD3)

S1C6P366

[The potential of the substrate (back of the chip) is VSS.]

Output —
R00
R01
R02 (TOUT)
R03 (FOUT)
R10–R13
R20–R23

CA
CB
AVDD
AVREF
$\overline{\text{TEST}}$
VDD
VD1
OSC1
OSC2
OSC3
OSC4
VSS
AVSS

X'tal

CGX
CGC
CDC
RCR
CR

C1
C2
CP

*1
*2
*3

*1: Crystal oscillation
*2: CR oscillation
*3: Ceramic oscillation

Exclusive cable

1	VDD
2	VDD
3	CLK
4	VSS
5	SCLK
6	VSS
7	RXD
8	VSS
9	TXD
10	VSS
11	$\overline{\text{RESET}}$
12	VSS
13	$\overline{\text{SPRG}}$
14	VSS
15	Reserved
16	Reserved

← S1C88/S1C63 Serial Connector

CLKIN
SCLK
RXD
TXD
$\overline{\text{RESET}}$
$\overline{\text{SPRG}}$

CRES

BZ

Piezo
Coil

VC1 VC2 VC3
C3 C4 C5

X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C1–C5	Capacitor	0.2 μF
CP	Capacitor	3.3 μF
CRES	$\overline{\text{RESET}}$ terminal capacitor	0.1 μF

Note: The above table is simply an example, and is not guaranteed to work.

S1C6P366

• Serial programming mode (S1C88/S1C63 Serial Connector) <when used as S1C63158 OTP>
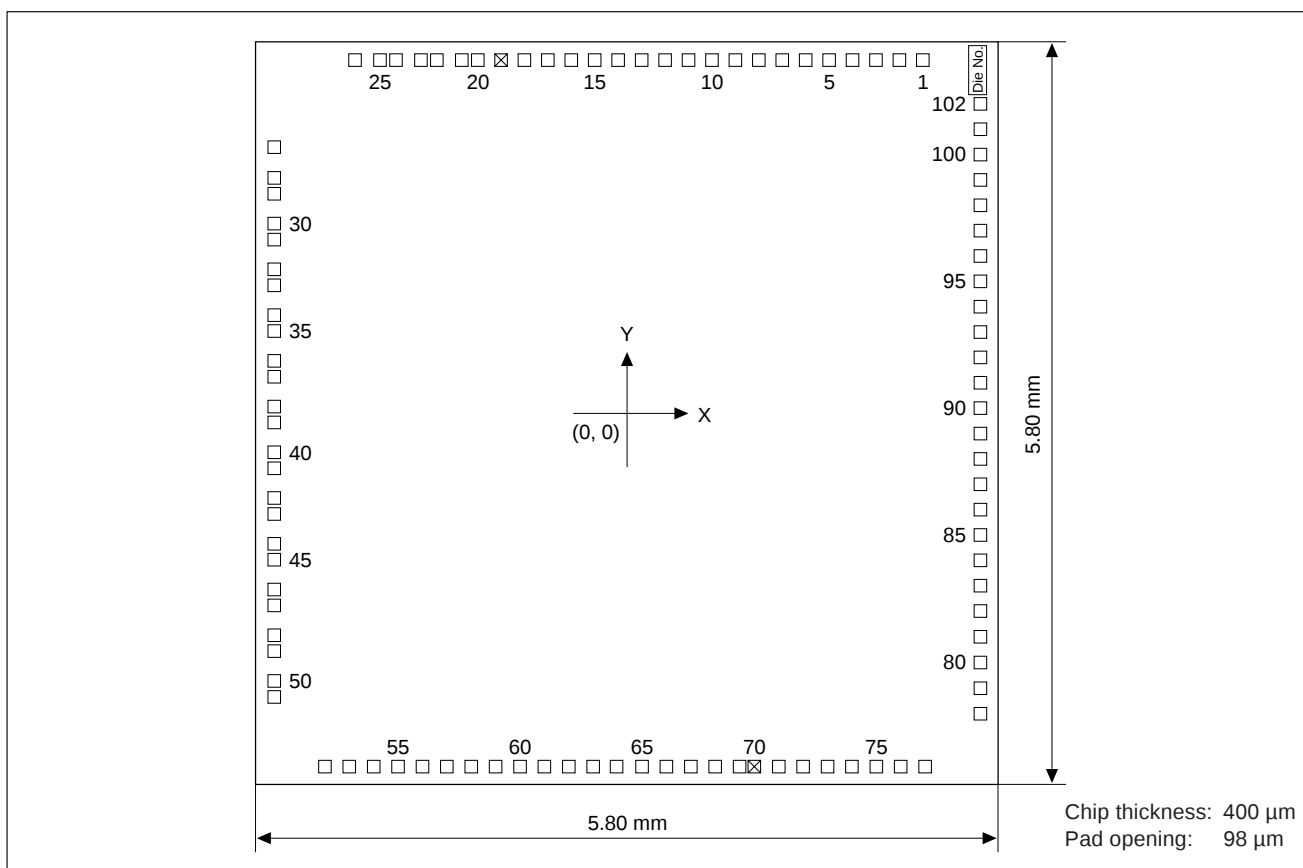
S1C6P366
[The potential of the substrate (back of the chip) is Vss.]

Input: K00–K03, K10–K13, K20

I/O: P00–P03, P10 (SIN), P11 (SOUT), P12 (SCLK), P13 (SRDY), P20–P23, P30–P33, P40 (AD0), P41 (AD1), P42 (AD2), P43 (AD3)

Output: R00, R01, R02 (TOUT), R03 (FOUT), R10–R13, R20–R23

Exclusive cable
1 VDD
2 VDD
3 CLK
4 Vss
5 SCLK
6 Vss
7 RXD
8 Vss
9 TXD
10 Vss
11 RESET
12 Vss
13 SPRG
14 Vss
15 Reserved
16 Reserved

← S1C88/S1C63 Serial Connector

∗1: Crystal oscillation
∗2: CR oscillation
∗3: Ceramic oscillation

X'tal	Crystal oscillator	32.768 kHz, C$_I$ (Max.) = 34 kΩ
C$_{GX}$	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
C$_{GC}$	Gate capacitor	100 pF
C$_{DC}$	Drain capacitor	100 pF
R$_{CR}$	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C$_1$–C$_3$	Capacitor	0.2 µF
C$_P$	Capacitor	3.3 µF
C$_{RES}$	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

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■ PAD LAYOUT

● Diagram of Pad Layout

Chip thickness: 400 μm
Pad opening: 98 μm

### ● Pad Coordinates

Unit: μm
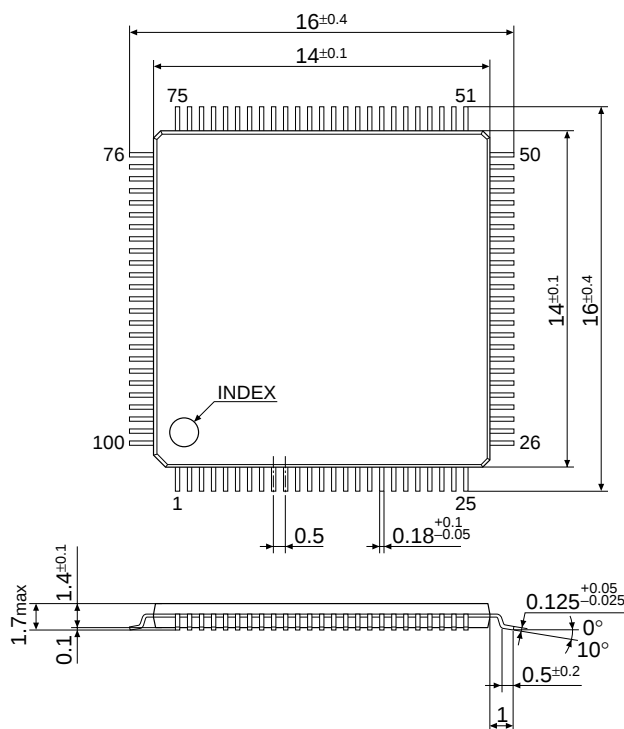
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	R13	2,309	2,759	27	SEG7	-2,757	2,079	53	$\overline{SPRG}$	-2,171	-2,759	79	P43	2,759	-2,147
2	R12	2,126	2,759	28	SEG8	-2,757	1,839	54	COM0	-1,980	-2,759	80	P42	2,759	-1,946
3	R11	1,943	2,759	29	SEG9	-2,757	1,715	55	COM1	-1,790	-2,759	81	P41	2,759	-1,745
4	R10	1,760	2,759	30	SEG10	-2,757	1,482	56	COM2	-1,599	-2,759	82	P40	2,759	-1,544
5	R03	1,577	2,759	31	SEG11	-2,757	1,357	57	COM3	-1,409	-2,759	83	P33	2,759	-1,346
6	R02	1,394	2,759	32	SEG12	-2,757	1,125	58	CB	-1,218	-2,759	84	P32	2,759	-1,148
7	R01	1,211	2,759	33	SEG13	-2,757	1,000	59	CA	-1,028	-2,759	85	P31	2,759	-950
8	R00	1,028	2,759	34	SEG14	-2,757	767	60	V_{C3}	-837	-2,759	86	P30	2,759	-752
9	BZ	845	2,759	35	SEG15	-2,757	643	61	V_{C2}	-647	-2,759	87	P23	2,759	-554
10	K00	662	2,759	36	SEG16	-2,757	410	62	V_{C1}	-456	-2,759	88	P22	2,759	-356
11	K01	479	2,759	37	SEG17	-2,757	286	63	V_{SS}	-266	-2,759	89	P21	2,759	-158
12	K02	296	2,759	38	SEG18	-2,757	53	64	OSC1	-83	-2,759	90	P20	2,759	41
13	K03	113	2,759	39	SEG19	-2,757	-71	65	OSC2	116	-2,759	91	P13	2,759	239
14	K10	-71	2,759	40	SEG20	-2,757	-304	66	V_{D1}	306	-2,759	92	P12	2,759	437
15	K11	-254	2,759	41	SEG21	-2,757	-429	67	OSC3	497	-2,759	93	P11	2,759	635
16	K12	-437	2,759	42	SEG22	-2,757	-661	68	OSC4	687	-2,759	94	P10	2,759	833
17	K13	-620	2,759	43	SEG23	-2,757	-786	69	V_{DD}	878	-2,759	95	P03	2,759	1,031
18	K20	-803	2,759	44	SEG24	-2,757	-1,019	70	N.C.	993	-2,759	96	P02	2,759	1,229
19	N.C.	-986	2,759	45	SEG25	-2,757	-1,143	71	$\overline{RESET}$	1,184	-2,759	97	P01	2,759	1,427
20	SEG0	-1,167	2,759	46	SEG26	-2,757	-1,376	72	$\overline{TEST}$	1,374	-2,759	98	P00	2,759	1,625
21	SEG1	-1,292	2,759	47	SEG27	-2,757	-1,500	73	AVREF	1,565	-2,759	99	R23	2,759	1,823
22	SEG2	-1,487	2,759	48	SEG28	-2,757	-1,733	74	AV_{DD}	1,755	-2,759	100	R22	2,759	2,021
23	SEG3	-1,611	2,759	49	SEG29	-2,757	-1,857	75	AVSS	1,946	-2,759	101	R21	2,759	2,219
24	SEG4	-1,806	2,759	50	SEG30	-2,757	-2,090	76	RXD	2,136	-2,759	102	R20	2,759	2,417
25	SEG5	-1,931	2,759	51	SEG31	-2,757	-2,215	77	TXD	2,327	-2,759				
26	SEG6	-2,126	2,759	52	CLKIN	-2,361	-2,759	78	SCLK	2,759	-2,346				

N.C. : No Connection

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S1C6P366

■ PACKAGE

Plastic QFP15-100pin

Unit: mm