MF1220-02

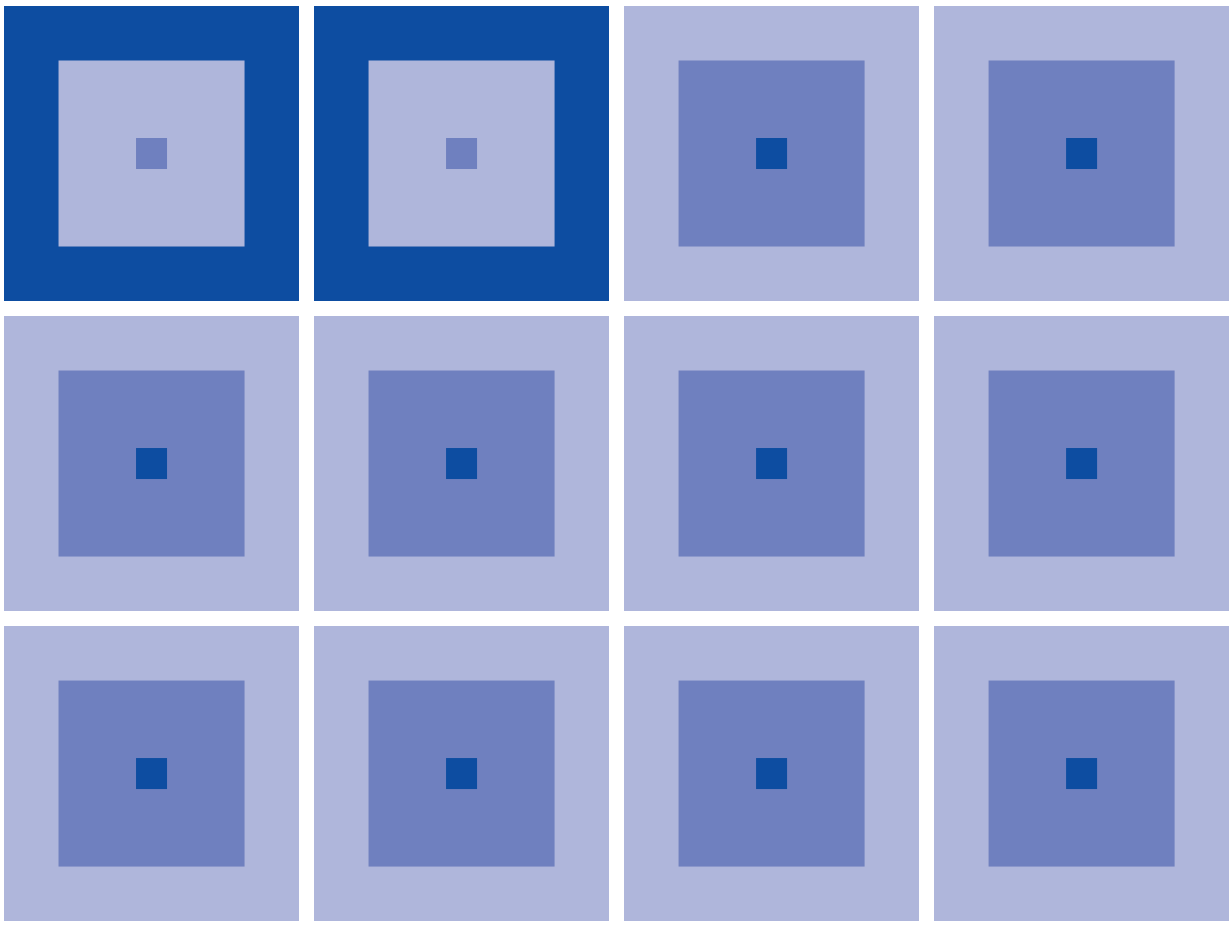
EPSON

CMOS CALLING NUMBER IDENTIFICATION RECEIVER IC

S1C05250

Technical Manual

S1C05250 Technical Hardware



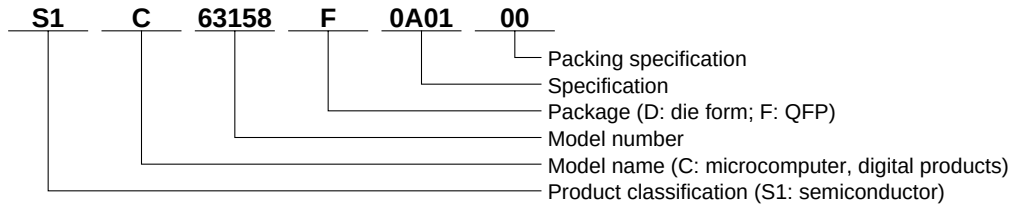
SEIKO EPSON CORPORATION

The information of the product number change

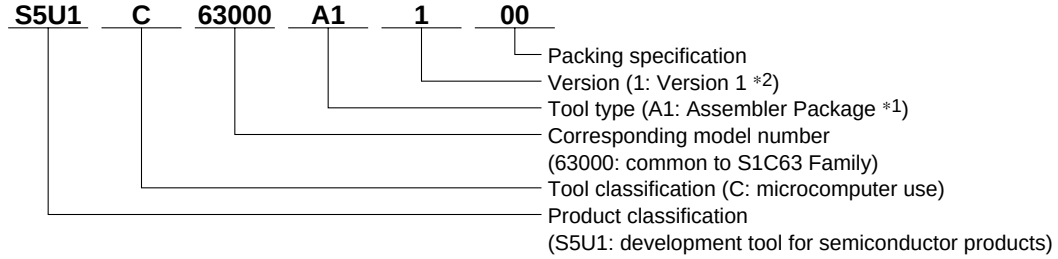
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C63 Family processors

Previous No.	New No.
E0C63158	S1C63158
E0C63256	S1C63256
E0C63358	S1C63358
E0C63P366	S1C6P366
E0C63404	S1C63404
E0C63406	S1C63406
E0C63408	S1C63408
E0C63F408	S1C6F408
E0C63454	S1C63454
E0C63455	S1C63455
E0C63458	S1C63458
E0C63466	S1C63466
E0C63P466	S1C6P466

Previous No.	New No.
E0C63467	S1C63467
E0C63557	S1C63557
E0C63558	S1C63558
E0C63567	S1C63567
E0C63F567	S1C6F567
E0C63658	S1C63658
E0C63666	S1C63666
E0C63F666	S1C6F666
E0C63A08	S1C63A08
E0C63B07	S1C63B07
E0C63B08	S1C63B08
E0C63B58	S1C63B58

S1C63 Family peripheral products

Previous No.	New No.
E0C5250	S1C05250
E0C5251	S1C05251

Comparison table between new and previous number of development tools

Development tools for the S1C63 Family

Previous No.	New No.
ADP63366	S5U1C63366X
ADP63466	S5U1C63466X
ASM63	S5U1C63000A
GAM63001	S5U1C63000G
ICE63	S5U1C63000H1
PRC63001	S5U1C63001P
PRC63002	S5U1C63002P
PRC63004	S5U1C63004P
PRC63005	S5U1C63005P
PRC63006	S5U1C63006P
PRC63007	S5U1C63007P
URS63366	S5U1C63366Y

Development tools for the S1C63/88 Family

Previous No.	New No.
ADS00002	S5U1C88000X1
GWH00002	S5U1C88000W2
URM00002	S5U1C88000W1

CONTENTS

1 Overview

The S1C05250 (CAS + FSK IC) is a CMOS IC for calling number identification with a Call Waiting function. It provides an interface to various call information delivery services based on Bellcore GR-30-CORE, such as CND (Calling Number Delivery), CNAM (Calling Name Delivery), and CIDCW (Calling Identity on Call Waiting), as well as British Telecom's CLIP (Calling Line Identification Service) and Cable Communications Association's CDS (Caller Display Service).

The S1C05250 incorporates power-down, ring detection, and carrier detection circuits, a synchronous receive data output function, and a clock-synchronized serial interface. All these features make it suitable for various applications such as those listed below.

- Calling number delivery service with a Call Waiting function
- Telephone sets and similar auxiliary equipment
- Telephone answering equipment
- Multifunction telephones
- Facsimiles
- Computer peripheral circuits

1.1 Features

- Conforms to Bellcore GR-30-CORE and SR-TSV-002476
- Conforms to British Telecom SIN227 and SIN242
- Can detect Bellcore CPE alert signal (CAS) and British Telecom idle-tone alert signal using a programmable band-pass filter
- FSK demodulation circuit based on ITU-T V.23 and BELL202
- Filter bypass mode to detect call progress mode (CPM) signal
- Programmable alert-signal detection level
- Carrier/ring detection output
- Supports 3.57945 MHz crystal oscillator or external clock input
- Serial-receive data output
- Serial host interface
- Power-down mode
- Power supply voltage: 2.7 V to 5.5 V
- Operating temperature range: -20°C to 70°C
- Current consumption: 3 mA when operating
  1 µA during power-down
- Shipping form: SOP1-24pin package (plastic) or chip

1.2 Block Diagram

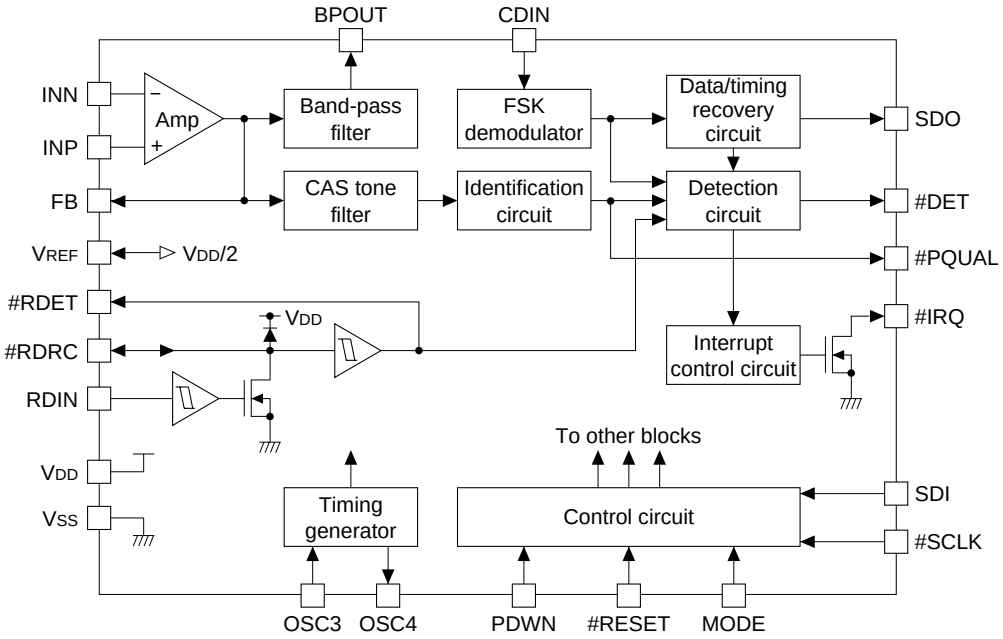
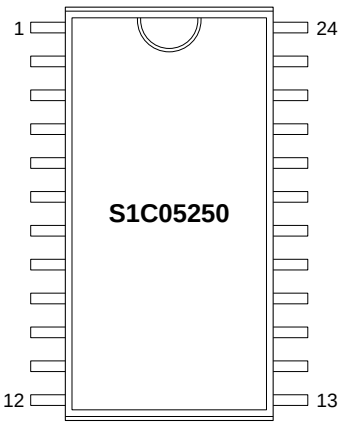


Figure 1.2.1 Block diagram

1.3 Pin Assignment

SOP1-24pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	INP	7	#RDET	13	OSC3	19	#SCLK
2	INN	8	PDWN	14	OSC4	20	SDI
3	FB	9	#RESET	15	N.C.	21	SDO
4	VREF	10	N.C.	16	#PQUAL	22	CDIN
5	RDIN	11	MODE	17	#DET	23	BPOUT
6	#RDRC	12	VSS	18	#IRQ	24	VDD

Figure 1.3.1 Pin assignment

1.4 Pin Description

Note: The signal and pin names prefixed by # in this manual are those of active-low signals and pins.

Table 1.4.1 Pin description

Pin name	Pin No.	Type	Power-down state	Description
INP	1	Input Analog	Off	Positive input: Non-inverted amp input Connect this pin to the RING side of the twisted-pair telephone line through an input-gain setting resistor and DC-decoupling capacitor. In power-down mode, this pin is disconnected from the internal circuit.
INN	2	Input Analog	Off	Negative input: Inverted amp input Connect this pin to the TIP side of the twisted-pair telephone line through an input-gain setting resistor and DC-decoupling capacitor. In power-down mode, this pin is disconnected from the internal circuit.
FB	3	Output Analog	High-Z	Amp output Connect a feedback resistor to set the gain between this pin and the INN pin. In power-down mode, this pin goes to a high-impedance state.
V_{REF}	4	Output Analog	V_{DD} level	Reference voltage output This pin outputs a voltage that is 1/2 of V_{DD}. Connect this pin to V_{SS} via a 0.1-µF capacitor. In power-down mode, this pin outputs a voltage equal to V_{DD}.
RDIN	5	Schmitt trigger input	Active	Ring detection input For ring detection, attenuate the ring signal before inputting it to this pin. This input circuit remains active even in power-down mode.
#RDRC	6	Open-drain output Schmitt trigger input	Active	Ring detection RC pin Connect an RC network to this pin and set the delay time for ring signal detection. This output circuit remains active even in power-down mode.
#RDET	7	Output	Active	Ring detection output This pin outputs the #RDRC signal after it is passed through a Schmitt trigger buffer. Upon detection of the ring signal, this pin changes to Low level.
PDWN	8	Input	Active	Power-down input This pin must be held at Low level during normal operation. When the pin is set to High level, the S1C05250 is placed in power-down mode. During power-down mode, each pin on the S1C05250 is placed in the state shown in this table.
#RESET	9	Input	Active	Reset input All of the internal registers are reset to the default state when the pin is set to Low level. Before any data can be written to the internal registers, this pin must be set to High level.
MODE	11	Input	Active	Mode selection input: Selects CAS mode or FSK/CPM mode CAS mode is selected by setting this input to High level, so that CAS detection is enabled while FSK function/CPM detection is disabled. Also, in this state, data can be written from the host device to the internal registers using the SDI and #SCLK pins. Note that before writing data to the internal registers, the serial interface must be synchronized to the data write sequence by temporarily setting this pin to Low level. FSK/CPM mode is selected by setting this input to Low level, in which case CAS detection is disabled and FSK function/CPM detection is enabled. In this state, the host device can read out receive data from the SDO pin.
V_{SS}	12	Power supply (-)		Negative power-supply pin Connect this pin to the ground line of the system.
OSC3	13	Input	Off	Crystal oscillator input/external clock input Connect a crystal resonator between this pin and the OSC4 pin and an appropriate capacitance between this pin and the V_{SS} pin. This pin can also be used for external clock input. In power-down mode, this pin is disconnected from the internal circuit.

Pin name	Pin No.	Type	Power-down state	Description
OSC4	14	Output	High level	Crystal oscillator output Connect a crystal resonator between this pin and the OSC3 pin and an appropriate capacitance between this pin and the VSS pin. When connecting external clock input to the OSC3 pin, leave this pin open. During power-down mode, this pin changes to High level.
#PQUAL	16	Output	High level	Prequalify output The prequalify status of the CAS tone can be monitored from this pin in CAS mode. This pin returns to High level when the CAS tone is not detected.
#DET	17	Output	Active	Detection output During power-down mode, this pin changes to Low level when a ring signal is input or pulled to Low level by the Line Reversal signal. During normal operation in FSK mode, this pin goes to Low level when an FSK signal is input. During normal operation in CPM mode, this pin outputs the input signal in pulse form at the amplitude level of VDD and VSS. By measuring the frequency of the pulse from the host side, the CPM (dial) tone can be identified. During normal operation in CAS mode, this pin goes to Low level when a CAS tone signal is input.
#IRQ	18	Open-drain output	Active	Interrupt request output In power-down mode, this pin changes to Low level when a ring signal is input or pulled to Low level by the Line Reversal signal. During normal operation in FSK mode, this pin changes to Low level when receive data is latched into the internal register and is ready to be read by the host. Then, when the host reads the first bit of the receive data, this pin returns to High level. During normal operation in CPM mode, this pin changes to Low level when a signal with a frequency of 200 Hz or above, such as the dial tone, is input. During normal operation in CAS mode, this pin changes to Low level when the CAS tone is detected. This pin is held at Low level while the CAS tone is being input.
#SCLK	19	Input	Active	Serial clock input When the host writes to the internal register or reads receive data, a clock signal is fed from the host into this pin. The receive data read out by the host is sequentially shifted at falling edges of the clock signal fed to this pin.
SDI	20	Input	Active	Serial data input When the host writes to the internal register, the write data is input from this pin.
SDO	21	Output	High level	Serial data output This pin outputs the receive data read out by the host. When asynchronous mode is selected, data in asynchronous mode is output. When synchronous mode is selected, data is output synchronously with the clock signal fed to the #SCLK pin by the host. In power-down, CPM, or CAS mode, this pin is held at High level.
BPOUT	22	Input Analog	VREF	Capacitor connecting pin Connect a 0.1-µF capacitor between this pin and the CDIN pin.
CDIN	23	Output Analog	High-Z	Capacitor connecting pin Connect a 0.1-µF capacitor between this pin and the BPOUT pin.
VDD	24	Power supply		Positive power supply
N.C.	10,15	Open		Unconnected

2 Power Supply Block and Initial Reset

2.1 Power Supply

The following shows the operating power supply voltage of the S1C05250.

Power supply voltage: 2.7 V to 5.5 V

The S1C05250 is operated in the above voltage range by a single power supply that is connected between VDD and VSS. The voltage required for internal operation (VREF = 1/2 VDD) is generated by the IC itself.

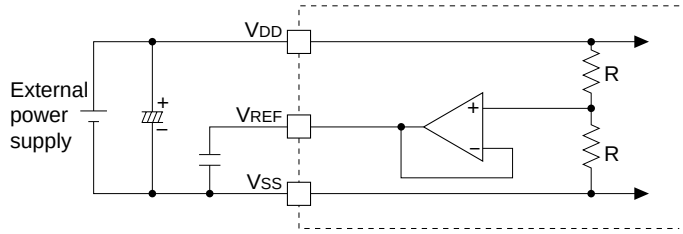


Figure 2.1.1 Power supply block

2.2 Initial Reset

The S1C05250 contains control registers that can be accessed by the external CPU through a serial interface. The control registers are initialized by an initial reset which is applied from the #RESET pin.

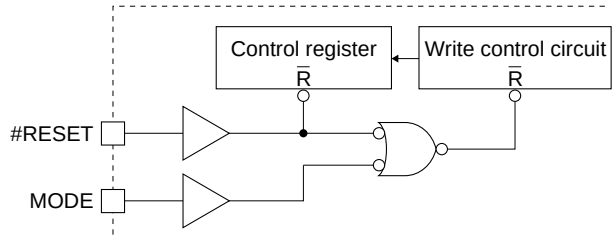


Figure 2.2.1 Initial reset circuit

Specifically, the control registers are reset by pulling the #RESET pin to Low level (VSS) from outside of the IC. Then, the reset state is eliminated by releasing the #RESET pin back to High level (VDD). Also, the write control circuit for the control register is reset when the #RESET pin or MODE pin is at Low level. Before data can be written to the control register, both #RESET and MODE must be at High level.

3 Functional Description

3.1 Register Description

The S1C05250 contains eight 4-bit registers that can be accessed by the CPU.
The CPU can access these CPU interface registers through the serial interface pins (SDI, #SCLK, and MODE) and control the mode of the S1C05250. The CPU uses the first four bits of transmit data to specify the address A[3:0] of the internal register to be accessed. The data is transmitted beginning with the LSB (A0). The four bits that follow the LSB are data bits D[3:0] which are the data to be written to the specified register. This data is also transmitted beginning with the LSB (D0).
Table 3.1.1 shows registers and control bit assignments.

Table 3.1.1 Register structure

Register name	Address A[3:0]	Initial value	Data bit			
			D3	D2	D1	D0
MDR	0000	0000	TEST	FSK/CPM	Bellcore/BT	ASYNC/SYNC
GLR	0001	0100	GL3	GL2	GL1	GL0
GHR	0010	0100	GH3	GH2	GH1	GH0
TLR	0011	0110	TL3	TL2	TL1	TL0
THR	0100	XXX1	X	X	X	TH0
AVR	0101	X011	X	AV2	AV1	AV0
WLR	0110	0001	WL3	WL2	WL1	WL0
WHR	0111	0001	WH3	WH2	WH1	WH0

Each register is detailed below.

MDR: Mode Register (Address = 0h)

Table 3.1.2 MDR register

Bit	Bit name	Initial value	Description
D0	ASYNC/SYNC	0	Asynchronous/synchronous mode selection This bit is used to select asynchronous or synchronous mode. ASYNC/SYNC bit — Mode 0 — Selects asynchronous mode 1 — Selects synchronous mode Asynchronous mode is selected by setting this bit to 0, in which case the 8-bit serial data output from the SDO pin is forwarded in asynchronous mode. Synchronous mode is selected by setting this bit to 1. When the FSK signal is received in FSK mode, serial data is output from the SDO pin and read by the CPU synchronously with the clock signal fed from the CPU to the #SCLK pin. Also, in synchronous mode, when the receive data is ready for output, the #IRQ pin changes to Low level, indicating that the CPU can read the data.
D1	Bellcore/BT	0	Bellcore/BT selection This bit is used to select Bellcore or BT (British Telecom) mode. Bellcore/BT bit — Mode 0 — Selects Bellcore mode 1 — Selects BT mode When this bit is set to 0, the gain in the dual-tone filter is set directly by the GLR and GHR registers. When this bit is set to 1, the value set by the GLR and GHR registers plus 6 dB is set as the gain in the dual-tone filter.
D2	FSK/CPM	0	CPM mode selection This bit is used to select FSK or CPM mode when the MODE pin is low. FSK/CPM bit — Mode 0 — Selects FSK mode 1 — Selects CPM mode If this bit is set to 1 when the MODE pin is held at Low level (FSK/CPM mode), the receive filter is bypassed, and when the CPM tone is input to the INP/INN pin, the #IRQ pin goes to Low level. Also, since the pulse generated from the CPM tone signal is output from the #DET pin, the CPM (dial) tone can be identified by measuring the frequency of the pulse. If this bit is set to 0 when the MODE pin is held at Low level (FSK/CPM mode), the FSK function is enabled. When the MODE pin is high (CAS mode), settings on this pin do not affect the device operation.
D3	TEST	0	Test mode selection This bit is used to test the IC. This bit normally must be fixed to 0.

GLR: Low-Tone Gain Setting Register (Address = 1h)

Table 3.1.3 GLR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	GL0 GL1 GL2 GL3	0100	Low-tone filter gain selection These bits control gain in the 2,130-Hz tone filter. GL3 GL2 Gain (dB) GL1 GL0 Gain (dB) 0 0 0 0 0 0 0 1 -4 0 1 -1 1 0 -8 1 0 -2 1 1 -12 1 1 -3 GL1 and GL0 change the gain in increments of 1 dB, whereas GL3 and GL2 change the gain in increments of 4 dB. The alert-tone detection level is attenuated (sensitivity is lowered) by an amount equal to the total gain set here.

GHR: High-Tone Gain Setting Register (Address = 2h)

Table 3.1.4 GHR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	GH0 GH1 GH2 GH3	0100	High-tone filter gain selection These bits control gain in the 2,750-Hz tone filter. GH3 GH2 Gain (dB) GH1 GH0 Gain (dB) 0 0 0 0 0 0 0 1 -4 0 1 -1 1 0 -8 1 0 -2 1 1 -12 1 1 -3 GH1 and GH0 change the gain in increments of 1 dB, whereas GH3 and GH2 change the gain in increments of 4 dB. The alert-tone detection level is attenuated (sensitivity is lowered) by an amount equal to the total gain set here.

TLR, THR: Detection Threshold Setting Registers (Address = 3h, 4h)

Table 3.1.5 TLR and THR registers

Bit	Bit name	Initial value	Description
D0 D1 D2 D3 D0 D1 D2 D3	TL0 TL1 TL2 TL3 TH0 X X X	0110 XXX1	CAS detection threshold selection These bits control the minimum duration of tone with which the CAS tone is identified. TH0 (THR register bit 0) is the MSB of the threshold set. TH0 TL3 TL2 TL1 TL0 Threshold value (msec) 0 0 0 0 0 5 0 0 0 0 1 9 0 0 0 1 0 12 0 0 0 1 1 16 0 0 1 0 0 19 0 0 1 0 1 21 0 0 1 1 0 23 0 0 1 1 1 26 0 1 0 0 0 29 0 1 0 0 1 32 0 1 0 1 0 34 0 1 0 1 1 36 0 1 1 0 0 39 0 1 1 0 1 43 0 1 1 1 0 46 0 1 1 1 1 48 1 0 0 0 0 50 1 0 0 0 1 53 1 0 0 1 0 56 1 0 0 1 1 59 1 0 1 0 0 61 1 0 1 0 1 64 **1 0 1 1 0 67** 1 0 1 1 1 70 1 1 0 0 0 73 **1 1 0 0 1 76** 1 1 0 1 0 78 1 1 0 1 1 81 1 1 1 0 0 84 1 1 1 0 1 87 1 1 1 1 0 90 1 1 1 1 1 Invalid (Cannot be set) The bit setting 10110 corresponds to Bellcore and British Telecom Loop State service; the bit setting 11001 corresponds to British Telecom Idle State service.

AVR: Average Divide-Ratio Select Register (Address = 5h)

Table 3.1.6 AVR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	AV0 AV1 AV2 X	X011	Average counter divide-ratio selection These bits control the frequency divide ratio of the internal average counter. Setting to 011 is recommended. AV2 AV1 AV0 Divide ratio 0 0 0 1/1 0 0 1 1/2 0 1 0 1/4 0 1 1 1/8 1 0 0 1/16 1 0 1 1/32 1 1 0 1/64

WLR: Low-Tone Record Window Select Register (Address = 6h)

Table 3.1.7 WLR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	WL0 WL1 WL2 WL3	0001	Low-tone window width selection These bits are used the low-tone record window width of the identification block. A tone can be identified when one cycle of it is within the specified range. WL3 WL2 WL1 WL0 Window width (%) 0 0 0 0 0.51, -0.50 **0 0 0 1 0.57, -0.56** **0 0 1 0 0.63, -0.62** 0 0 1 1 0.69, -0.68 0 1 0 0 0.75, -0.74 0 1 0 1 0.81, -0.80 0 1 1 0 0.87, -0.85 0 1 1 1 0.93, -0.91 1 0 0 0 0.99, -0.97 1 0 0 1 1.06, -1.03 1 0 1 0 1.12, -1.09 1 0 1 1 1.18, -1.15 **1 1 0 0 1.24, -1.20** 1 1 0 1 1.30, -1.26 1 1 1 0 1.36, -1.32 1 1 1 1 1.42, -1.38 Bit setting 0001 is Bellcore's default value. Bit setting 0010 corresponds to British Telecom Loop State service and setting 1100 corresponds to British Telecom Idle State service.

WHR: High-Tone Record Window Select Register (Address = 7h)

Table 3.1.8 WHR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	WH0 WH1 WH2 WH3	0001	High-tone window width selection These bits are used to select the high-tone record window width of the identification block. A tone can be identified when one cycle of it is within the specified range. WH3 WH2 WH1 WH0 Window width (%) 0 0 0 0 0.51, -0.49 **0 0 0 1 0.59, -0.56** **0 0 1 0 0.67, -0.64** 0 0 1 1 0.75, -0.71 0 1 0 0 0.83, -0.79 0 1 0 1 0.90, -0.86 0 1 1 0 0.98, -0.94 0 1 1 1 1.06, -1.02 1 0 0 0 1.14, -1.09 **1 0 0 1 1.22, -1.17** 1 0 1 0 1.30, -1.24 1 0 1 1 1.37, -1.32 1 1 0 0 1.45, -1.39 1 1 0 1 1.53, -1.46 1 1 1 0 1.61, -1.54 1 1 1 1 1.69, -1.61 Bit setting 0001 is Bellcore's default value. Bit setting 0010 corresponds to British Telecom Loop State service and setting 1001 corresponds to British Telecom Idle State service.

3.2 Input Amp Circuit

The amp at the input stage must have its circuit configured to allow gain to be set correctly. For this reason, it requires five to six external resistors.

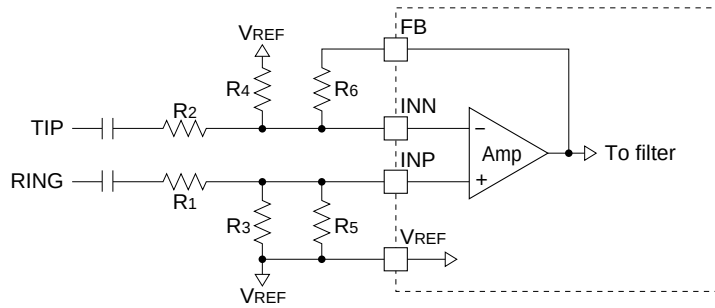


Figure 3.2.1 Input amp circuit

The gain in the input amp can be set depending on values R1 to R6 as shown below. Note that R3 and R5 may be replaced by one resistor.

$$G_{AMP} = \frac{R_5}{R_1} = \frac{R_6}{R_2} \text{ [times]} \qquad (When\ R_1 = R_2, R_3 = R_4, R_5 = R_6)$$

To set the FSK and CAS tone signal-detection levels, determine each resistance value with respect to VDD as shown below.

$$G_{AMP} = \frac{R_5}{R_1} = \frac{R_6}{R_2} = \frac{V_{DD}}{5} \times 0.562 \text{ [times]}$$

VDD is the power supply voltage fed to the VDD pin of the S1C05250. For R3 and R4, Seiko Epson recommends using a resistance of about 100 kΩ for noise prevention.
Tables 3.2.1 and 3.2.2 show typical resistance values and amp gain for the case where VDD = 5 V and VDD = 3 V, respectively.

Table 3.2.1 Resistance values and gain (VDD = 5 V)

Parameter	Value		Condition
	Bellcore	BT	
R1, R2	499 kΩ	499 kΩ	1%
R3, R4	100 kΩ	100 kΩ	1%
R5, R6	281 kΩ	281 kΩ	1%
Input amp gain	0.562 times (-5dB)	0.562 times (-5dB)	
FSK/CPM - CD ON level (Typ.)	-42.9 dBm	-45.1 dBV	
FSK/CPM - CD OFF level (Typ.)	-44.9 dBm	-47.1 dBV	
CAS - CD ON level (Typ.)	-35.8 dBm	-44.0 dBV	Tone filter gain = -4dB

Table 3.2.2 Resistance values and gain (VDD = 3 V)

Parameter	Value		Condition
	Bellcore	BT	
R1, R2	499 kΩ	499 kΩ	1%
R3, R4	100 kΩ	100 kΩ	1%
R5, R6	168 kΩ	168 kΩ	1%
Input amp gain	0.3372 times (-9.4dB)	0.3372 times (-9.4dB)	
FSK/CPM - CD ON level (Typ.)	-42.9 dBm	-45.1 dBV	
FSK/CPM - CD OFF level (Typ.)	-44.9 dBm	-47.1 dBV	
CAS - CD ON level (Typ.)	-35.8 dBm	-44.0 dBV	Tone filter gain = -4dB

3.3 Ring/Line Reversal Signal Detection

Figure 3.3.1 shows a typical circuit used to detect the Bellcore ring signal and British Telecom Line Reversal signal. When the S1C05250 is in power-down mode, this circuit detects the ring signal or Line Reversal signal. The Line Reversal or ring signal causes the voltage on the RDIN pin to rise, which drives the Schmitt rigger output high. This causes the Nch transistor to turn on and the #RDRC pin to change to Low level. Since the RDIN pin is normally at the Vss level, the #RDRC pin is at the High level. When the ring signal is input or the Line Reversal signal is generated, the capacitor of the #RDRC pin discharges, causing the #RDRC pin to change state from High to Low. The #RDET pin operates in the same way, except that in any mode other than power-down mode, the #RDET pin always responds to input on the RDIN pin.

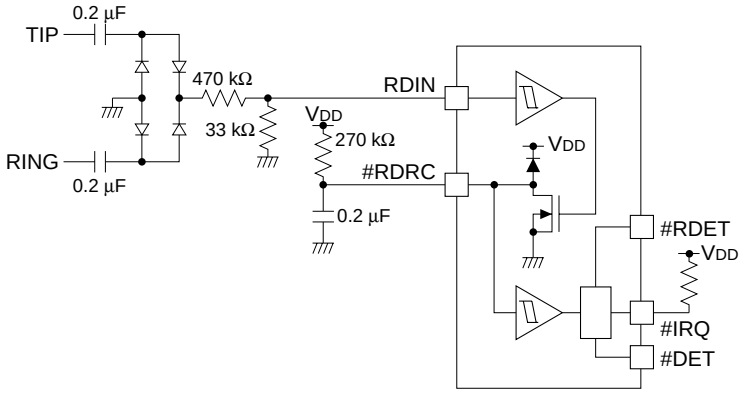


Figure 3.3.1 Ring/Line Reversal signal detection circuit

3.4 FSK Demodulation

The received FSK-modulated signal, after being processed by the band-pass filter, is demodulated by the FSK demodulation circuit. If the FSK signal is input when the PDWN pin is set to Low level and FSK mode has been selected by the host CPU, the #DET pin changes to Low level. The received data is read out from the SDO pin by the host CPU. Also, the #IRQ pin is driven Low each time one byte is received. This demodulation circuit supports a FSK-modulated signal that conforms to ITU-T V.23 or Bell202.

Table 3.4.1 FSK data characteristics

Parameter	Bellcore	BT
Mark frequency	1200 Hz ±1%	1300 Hz ±1.5%
Space frequency	2200 Hz ±1%	2100 Hz ±1.5%
Receive signal level	Mark: -32 dBm to -12 dBm Space: -36 dBm to -12 dBm	Mark: -40 dBV to -14 dBV Space: -36 dBV to -8 dBV
Signal distortion	≥ 25 dB	≥ 20 dB
Transfer rate	1200 baud ±1%	1200 baud ±1%

3.5 Dual-Tone Detection

Dual tones (Bellcore CPE alert signal (CAS), British Telecom tone alert signal) are detected using two tone filters and digital identification circuits. If dual tones are received when the PDWN pin is set low and CAS mode has been selected by the host CPU, the #DET pin and the #IRQ pin changes to Low level.

Table 3.5.1 Dual-tone characteristics

Parameter	Bellcore (CPE alert signal)	BT (tone alert signal)	
		Line disconnected	Line connected
Low tone frequency	2130 Hz ±0.5%	2130 Hz ±1.1%	2130 Hz ±0.6%
High tone frequency	2750 Hz ±0.5%	2750 Hz ±1.1%	2750 Hz ±0.6%
Receive signal level	-32 dBm to -14 dBm/tone, off-hook	-40 dBV to -2 dBV/tone, on-hook	-40 dBV to -8 dBV/tone, off-hook
Rejection signal level	≤ -45 dBm	≤ -46 dBV	
Receive tone twist	0 to 6 dB	0 to 7 dB	0 to 7 dB
Tone output time	75 msec to 85 msec	88 msec to 110 msec	80 msec to 85 msec
Simultaneous voice reception	Yes	No	Yes

4 Precautions on Mounting

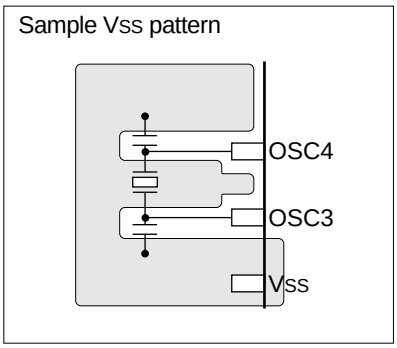
<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC3, OSC4 terminals, such as oscillators and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC3, OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



  (3) When supplying an external clock to the OSC3 terminal, the clock source should be connected to the OSC3 terminal in the shortest line.
  Furthermore, do not connect anything else to the OSC4 terminal.

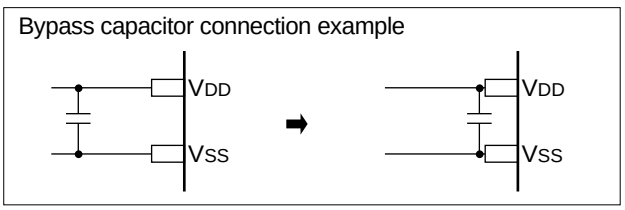
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC3 and VDD, please keep enough distance between OSC3 and VDD or other signals on the board pattern.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

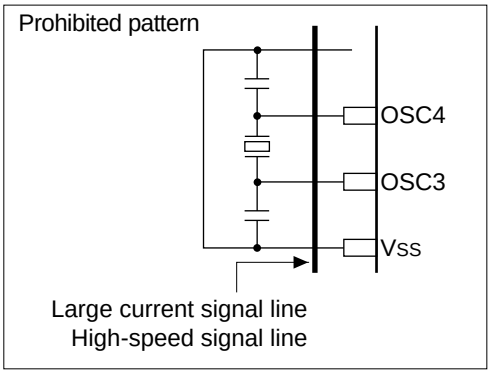
  (1) The power supply should be connected to the VDD, VSS and VREF terminals with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1.1 Absolute maximum ratings

Parameter	Symbol	Rated value	Unit
Power supply voltage	V_{DD}	-0.5 to 7	V
Input voltage	V_I	-0.3 to V_{DD}+0.3	V
Total output current	ΣI_{VDD}	±10	mA
Power dissipation	P_D	250	mW
Storage temperature	T_{STG}	-65 to 150	°C
Solder temperature	T_{SOL}	255	°C
Soldering time	t_{SOL}	10	Sec
Operating temperature	T_{OPR}	-20 to 70	°C
Electrostatic withstand voltage	V_E	EIAJ test (C=200pF): 150V or more MIL test (C=100pF, R=1.5kΩ): 1200V or more	V

The voltages are referenced to the V_{SS} pin as the ground level.

5.2 Recommended Operating Conditions

Table 5.2.1 Recommended operating conditions

Parameter	Symbol	Condition	Unit
Power supply voltage	V_{DD}	2.7 to 5.5	V
Crystal/clock frequency	f_{CLK}	3.579545	MHz
Crystal/clock frequency error	f_{ERR}	±0.01	%

The voltages are referenced to the V_{SS} pin as the ground level.

5.3 DC Characteristics

Table 5.3.1 DC characteristics

Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		OSC3, MODE, #SCLK, SDI, PDWN, #RESET	0.8V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		RDIN, #RDRC	0.7V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		OSC3, MODE, #SCLK, SDI, PDWN, #RESET	0		0.2V_{DD}	V
Low level input voltage (2)	V_{IL2}		RDIN, #RDRC	0		0.3V_{DD}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	RDIN, OSC3, MODE, #SCLK, SDI, PDWN, #RESET, #IRQ #RDRC (RDIN = Low)	0		0.5	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	RDIN, OSC3, MODE, #SCLK, SDI, PDWN, #RESET, #RDRC, #IRQ	-0.5		0	µA
High level output current	I_{OH}	V_{OH}=0.9V_{DD}	SDO, #DET, #RDET, #PQUAL			-1.5	mA
Low level output current	I_{OL}	V_{OL}=0.1V_{DD}	SDO, #DET, #RDET, #PQUAL, #IRQ, #RDRC	2.5			mA
V_{REF} output voltage	V_{REF}				V_{DD}/2		V
Input impedance	R_{IN}		INP, INN	10			MΩ
	R_{CDIN}		CDIN	140	200	260	kΩ

5.4 Current Consumption

Table 5.4.1 Current consumption

Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	During power-down (PDWN = High)				1.0	µA
		When operating (no signal input)	V_{DD}=5V		3.0		mA
			V_{DD}=3V		1.8		mA

5.5 Crystal Oscillation Characteristics

Table 5.5.1 Crystal oscillation characteristics

Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, C_G=C_D=18pF, Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	3.579545MHz oscillator			20	msec

5.6 FSK Demodulation Circuit Characteristics

5.6.1 FSK AC Characteristics

Table 5.6.1 FSK AC characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	TRATE		1188	1200	1212	Baud
Bell 202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell 202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V2}		2068	2100	2132	Hz
SN ratio	SNR		20	–	–	dB
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CDONFSK	V_{DD}=5V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-5dB	-47.1	-45.1	-43.1	dBV
		V_{DD}=3V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.1	-45.1	-43.1	dBV
Carrier-detect OFF sensitivity ∗1	CDOFFFSK	V_{DD}=5V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-5dB	-49.1	-47.1	-45.1	dBV
		V_{DD}=3V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.1	-47.1	-45.1	dBV

∗1 When the gain in the input amp is set to G_{AMP} (dB), the CDONFSK and CDOFFFSK values (Typ.) can be calculated from the equation below.

$$CD_{ONFSK}\ [dBm] = -G_{AMP} - 47.9 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{ONFSK}\ [dBV] = -G_{AMP} - 50.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

$$CD_{OFFFSK}\ [dBm] = -G_{AMP} - 49.9 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{OFFFSK}\ [dBV] = -G_{AMP} - 52.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

5.6.2 FSK Switching Characteristics

Table 5.6.2 FSK switching characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PDWN fall → FSK	tSUPD				20	msec
Carrier detect start time	tCDON		5	10	15	msec
Data end → #DET rise	tCDOFF		5	10	15	msec
PDWN rise → Oscillation start	tDOCH	V_{DD}=5V		7	12	msec
		V_{DD}=3V		10	15	msec

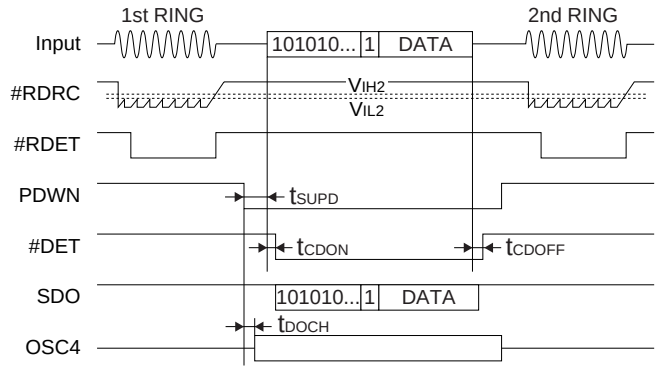


Figure 5.6.1 FSK switching characteristics

5.7 Dual-Tone (CAS) Detection Circuit Characteristics

5.7.1 CAS AC Characteristics

Table 5.7.1 CAS AC characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect sensitivity ∗1 (input level at TPI/RING)	CD_{ONTONE}	V_{DD}=5V, Bellcore mode Input amp gain (G_{AMP})=-5dB Tone filter gain=-4dB	-39.8	-35.8	-35.1	dBm
		V_{DD}=5V, BT mode ∗2 nput amp gain (G_{AMP})=-5dB Tone filter gain=-4dB	-48.0	-44.0	-40.0	dBV
		V_{DD}=3V, BT mode ∗2 nput amp gain (G_{AMP})=-9.4dB Tone filter gain=-4dB	-39.8	-35.8	-35.1	dBm
		V_{DD}=3V, BT mode ∗2 nput amp gain (G_{AMP})=-9.4dB Tone filter gain=-4dB	-48.0	-44.0	-40.0	dBV
Low tone frequency	f_{LTONE}	Bellcore (±0.5%)	2119.35	2130	2140.65	Hz
		BT line disconnected	2110	2130	2150	Hz
		BT line connected (±0.6%)	2117.22	2130	2142.78	Hz
High tone frequency	f_{HTONE}	Bellcore (±0.5%)	2736.25	2750	2763.75	Hz
		BT line disconnected	2720	2750	2780	Hz
		BT line connected (±0.6%)	2733.50	2750	2766.50	Hz

∗1 When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONTONE} value (Typ.) can be calculated from the equation below.
(When the internal tone filter gain = –4 dB)

$$CD_{ONTONE}\ [dBm] = -G_{AMP} - 40.8 + 20\log(\frac{V_{DD}}{5})\ [dBm],\quad CD_{ONTONE}\ [dBV] = -G_{AMP} - 49 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

∗2 BT mode is selected by setting the mode register (address = 0h) bit 2 to 1. By this setting, the gain in each dual-tone filter is raised +6 dB for adjustment to the British Telecom CD level.

5.7.2 CAS Switching Characteristics

Table 5.7.2 CAS switching characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Min.	Typ.	Max.	Unit
CAS detect capture time	t_{CASAQ}		2.8×(N+2)+16.9		msec
CAS end →#DET rise	t_{CASDH}		2.8×(31-N)+13.1		msec
CAS width	t_{CASW}	75	80	85	msec

N = TH0 × 16 + TL3 × 8 + TL2 × 4 + TL1 × 2 + TL0

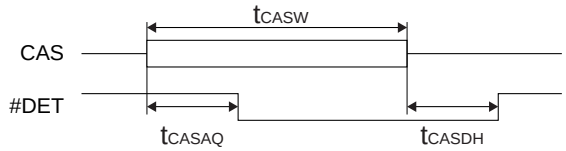


Figure 5.7.1 CAS switching characteristics

5.8 Call Progress Mode (CPM) Detection Circuit Characteristics

5.8.1 CPM AC Characteristics

Table 5.8.1 CPM AC characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CD_{ONCPM}	V_{DD}=5V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-5dB	-47.1	-45.1	-43.1	dBV
		V_{DD}=3V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.1	-45.1	-43.1	dBV
Carrier-detect OFF sensitivity ∗1	CD_{OFFCPM}	V_{DD}=5V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-5dB	-49.1	-47.1	-45.1	dBV
		V_{DD}=3V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.1	-47.1	-45.1	dBV

∗1 When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONCPM} and CD_{OFFCPM} values (Typ.) can be calculated from the equation below.

$$CD_{ONCPM}\ [dBm] = -G_{AMP} - 47.9 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{ONCPM}\ [dBV] = -G_{AMP} - 50.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

$$CD_{OFFCPM}\ [dBm] = -G_{AMP} - 49.9 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{OFFCPM}\ [dBV] = -G_{AMP} - 52.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

5.8.2 CPM Switching Characteristics

Table 5.8.2 CPM switching characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Min.	Typ.	Max.	Unit
CPM tone-detect capture time	t_{CPMAQ}		25		msec
CPM tone end → #IRQ rise	t_{CPMIH}		30		msec

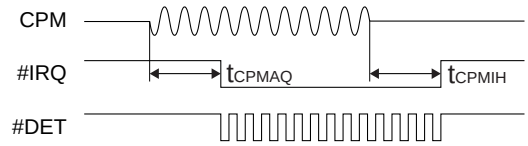


Figure 5.8.1 CPM switching characteristics

5.9 Serial Interface Circuit Characteristics

5.9.1 Serial Interface AC Characteristics

Table 5.9.1 Serial interface AC characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Min.	Typ.	Max.	Unit
#SCLK frequency	f_{SCLK}			1	MHz
#SCLK pulse width	t_{WSCLK}	400			nsec
SDI setup time	t_{SSDI}	250			nsec
SDI hold time	t_{HSDI}	500			nsec
SDO delay time	t_{DSDO}			250	nsec
MODE High setup time	t_{SMH}	1			µsec
MODE High hold time	t_{HMH}	1			µsec
MODE Low setup time	t_{SML}	1			µsec
MODE Low hold time	t_{HML}	1			µsec
MODE Low pulse width	t_{MDW}	1			µsec

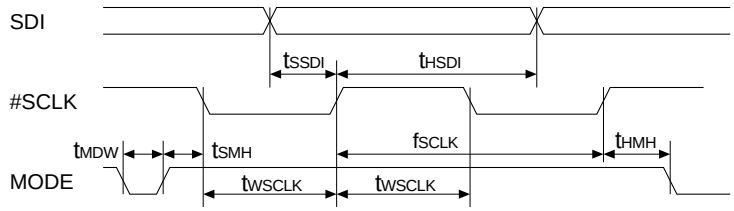


Figure 5.9.1 Serial interface input timing

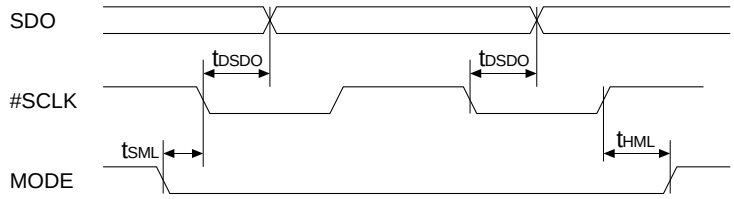


Figure 5.9.2 Serial interface output timing

5.9.2 FSK Demodulated Data Read Mode

The FSK signal fed to the INP and INN pins is demodulated into 8-bit asynchronous (start-stop) data. The demodulated data is then sampled by the internal 8-bit shift register. When the data has been stored in the shift register, the #IRQ pin changes to Low level, indicating that the data can be read by the host CPU.
If the MODE pin is set to Low level and synchronous mode has been selected (MDR[0] = 1), the host CPU reads out the 8-bit data synchronously with the clock signal fed from the host CPU to the #SCLK pin. Figure 5.9.3 shows the timing at which this data is read. Each bit of the 8-bit data is output from the SDO pin synchronously with falling edges of the #SCLK clock signal, beginning with bit 0. The host CPU latches each bit into the internal logic at rising edges of the #SCLK clock signal.
If the MODE pin is set to Low level and asynchronous mode has been set (MDR[0] = 0), the data is output from the SDO pin at a transfer rate of 1,200 baud. The clock signal from the host CPU is unnecessary. The host CPU latches the data synchronously with the start bit.

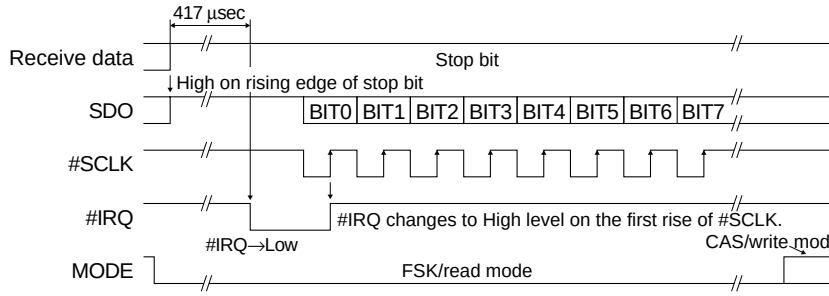


Figure 5.9.3 Data read timing in synchronous mode

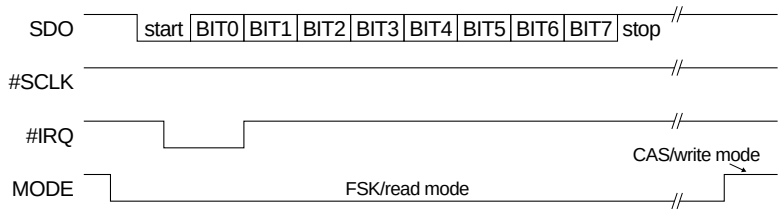


Figure 5.9.4 Data read timing in asynchronous mode

5.9.3 CAS Detection Circuit Control-Register Write Mode

The host CPU can write 4-bit data to the internal registers through the SDI pin in order to set each control bit. The host CPU must temporarily pull the MODE pin to Low level to initialize the write control circuit before it can write data. Then, after releasing the MODE pin back to High level, the host CPU must be held at High level while writing data to the internal register. The data input to the SDI pin is sampled at rising edges of the clock signal fed from the host CPU to the #SCLK pin. The first four bits of data sent from the host CPU are the address A[3:0] of the internal register to be accessed. The subsequent four bits are the data bits D[3:0] to be written to the specified register. The data is input beginning with the LSB.

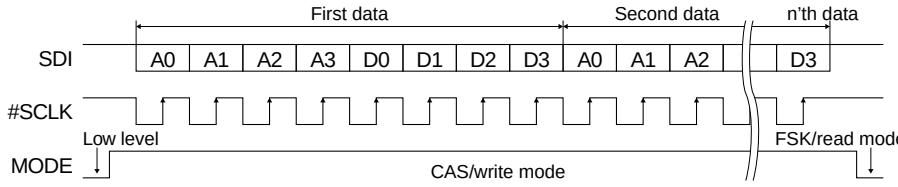


Figure 5.9.5 Data write timing

5.10 S1C05250 Timing Chart

5.10.1 Bellcore On-Hook Data Transfer

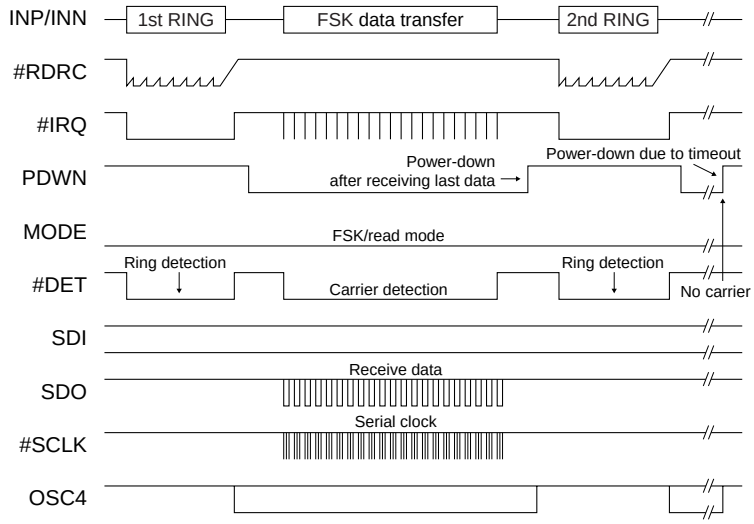


Figure 5.10.1 Bellcore on-hook data transfer timing chart

5.10.2 Bellcore Off-Hook Data Transfer

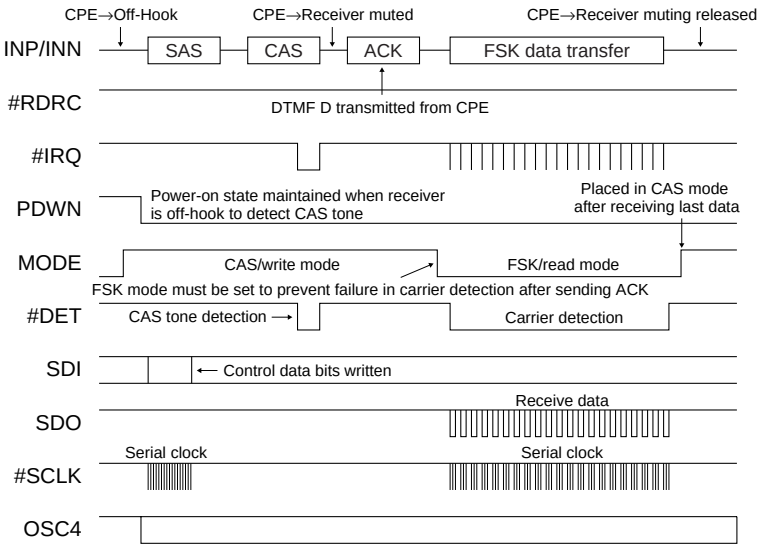


Figure 5.10.2 Bellcore off-hook data transfer timing chart

5.10.3 BT Idle State CLI Service

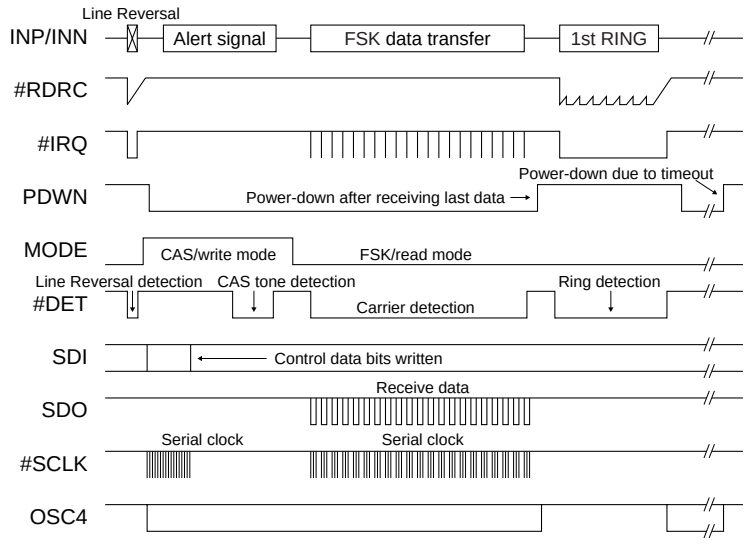


Figure 5.10.3 BT Idle State CLI service timing chart

5.10.4 BT Loop State CLI Service

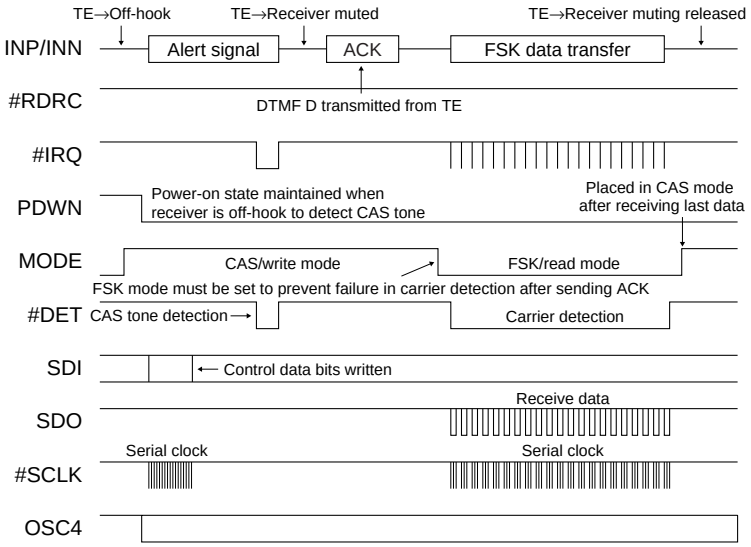


Figure 5.10.4 BT Loop State CLI service timing chart

5.11 External Wiring Diagram (Example)

5.11.1 Example of Bellcore-Compatible Telephone Circuit

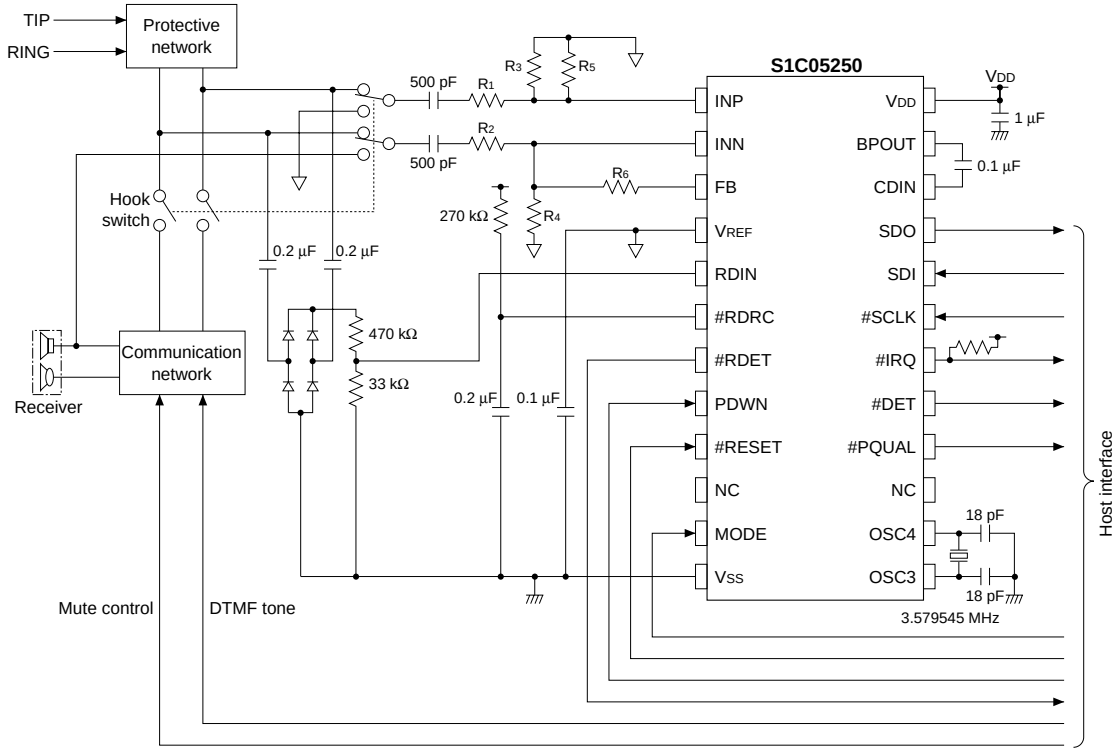


Figure 5.11.1 Example of Bellcore-compatible telephone circuit

Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

∗ See Section 3.2, "Input Amp Circuit", for the R1 to R6 values.

5.11.2 Example of Bellcore-Compatible Auxiliary Circuit

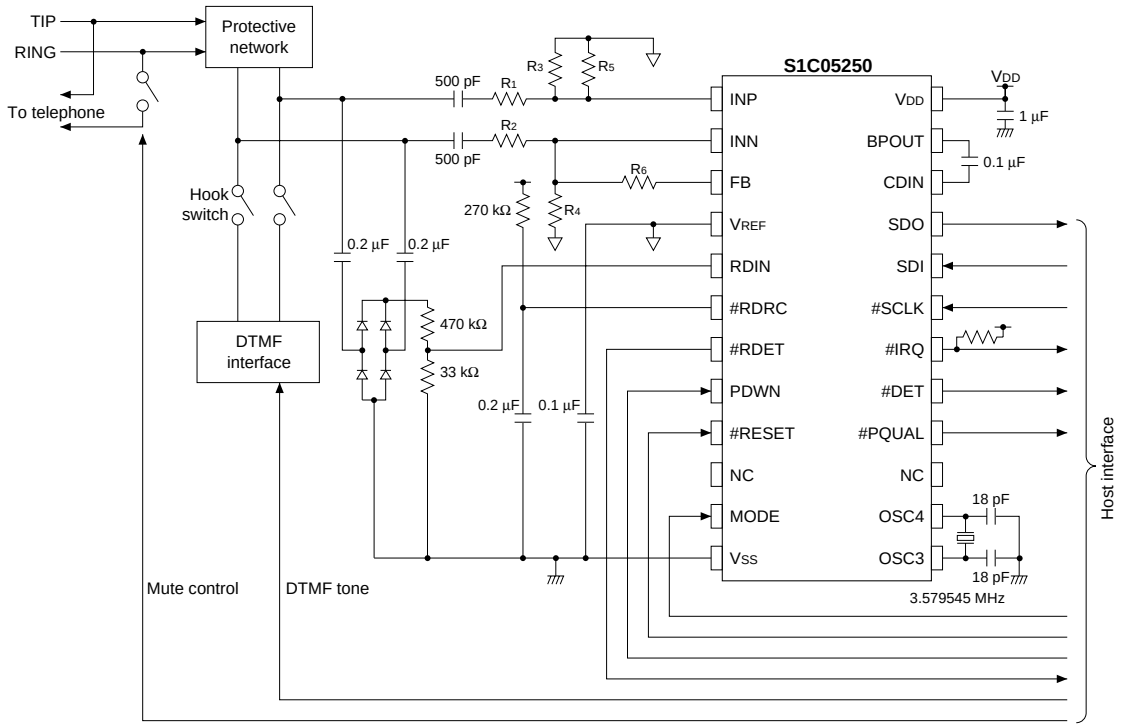


Figure 5.11.2 Example of Bellcore-compatible auxiliary circuit

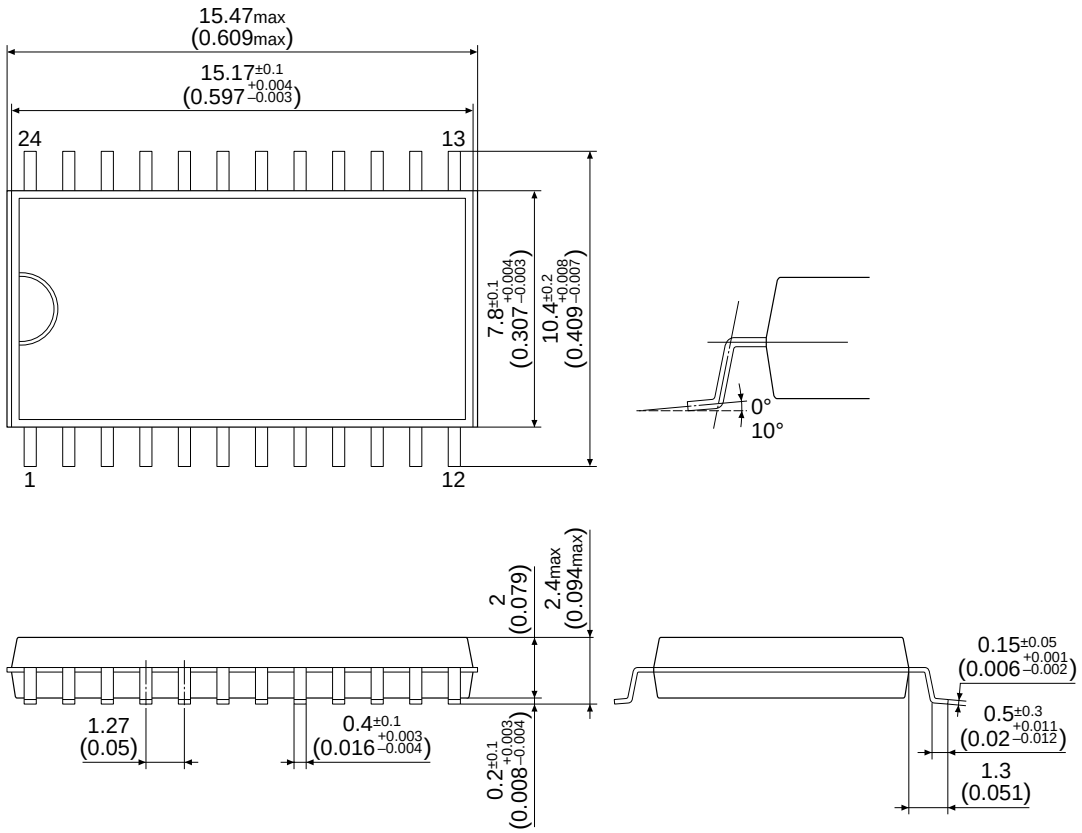
Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

∗ See Section 3.2, "Input Amp Circuit", for the R1 to R6 values.

6 Package

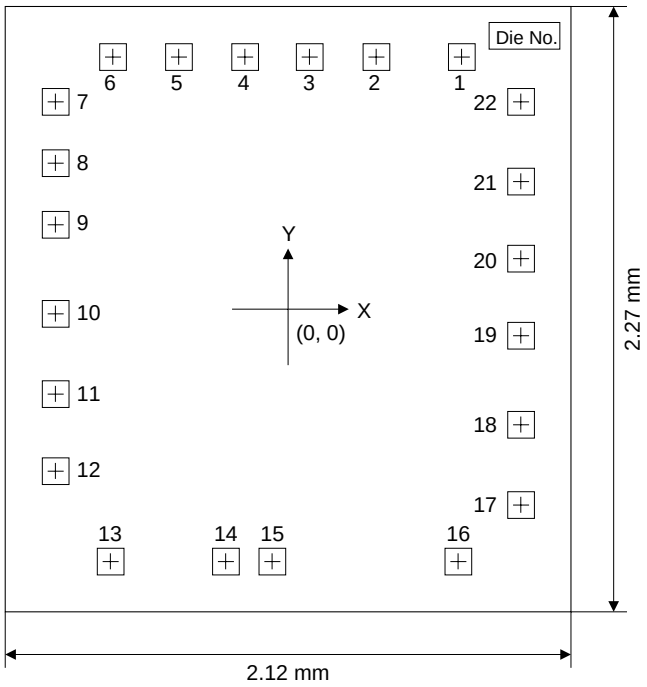
SOP1-24pin Plastic Package

Unit: mm (inch)



7 Pad Layout

7.1 Pad Layout Diagram



Chip thickness: 400 µm
Pad opening: 100 µm

7.2 Pad Coordinates

(Unit: µm)

Pad No.	Pad name	X coordinate	Y coordinate	Pad No.	Pad name	X coordinate	Y coordinate
1	CDIN	650	946	12	#RESET	-872	-607
2	BPOUT	330	946	13	MODE	-666	-946
3	V_{DD}	80	946	14	V_{SS}	-234	-946
4	INP	-162	946	15	OSC3	-60	-946
5	INN	-410	946	16	OSC4	637	-946
6	FB	-657	946	17	#PQUAL	872	-734
7	V_{REF}	-872	778	18	#DET	872	-433
8	RDIN	-872	548	19	#IRQ	872	-99
9	#RDRC	-872	317	20	#SCLK	872	190
10	#RDET	-872	-17	21	SDI	872	479
11	PDWN	-872	-318	22	SDO	872	778

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S1C05250
Technical Manual

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First issue October, 1999
Printed March, 2001 in Japan ⓂA