

8-bit Single Chip Microcomputer



- Original Architecture Core CPU
- Remote-control Carrier Output
- Dot-matrix LCD Driver
(51×32/66×17/67×16, 8 dots)

■ DESCRIPTION

The S1C88848 microcomputer features the S1C88 (Model 3) CMOS 8-bit core CPU along with ROM, RAM, a remote-control carrier output, a dot-matrix LCD controller/driver that allows driving of up to 1,632 pixels, three different timers and a serial interface with optional asynchronization or clock synchronization. The S1C88848 is fully operable over a wide range of voltages, and can perform stable operations even at low voltage (1.8 V Min.). Like all the devices in the S1C Family, this microcomputer has low current consumption (1.7 μ A at standby mode). The S1C88848 also contains the SVD circuit for detecting drop of battery voltage, and is most suitable for remote controllers for home electric appliances.

■ FEATURES

- Core CPU S1C88 (MODEL3) CMOS 8-bit core CPU
- Main (OSC3) oscillation circuit Crystal oscillation circuit/ceramic oscillation circuit/CR oscillation circuit 8.2MHz (Max.) (*1) (start clock source)
- Sub (OSC1) oscillation circuit Crystal oscillation circuit/CR oscillation circuit 32.768kHz (Typ.) (*1)
- Instruction set..... 608 types (usable for multiplication and division instructions)
- Min. instruction execution time 0.244 μ sec/8.2MHz (2-clock)
- Internal ROM capacity 48K bytes
- Internal RAM capacity RAM: 1.5K bytes
Display memory: 402 bytes
- Input port 10 bits (2 bits can be configured for event counter external clock inputs)
Internal pull-up resistors are available (*1)
- Output port 5 bits (can be configured for buzzer*2, TOUT*2, FOUT*2 and infrared remote-control carrier*1 outputs)
SEG40–SEG50 are usable as DC output ports (*1)
- I/O port 8 bits (4 bits can be configured for serial interface inputs/outputs *2)
Internal pull-up resistors are available (*1)
- LCD driver Dot matrix type
51 segments \times 32 commons (*1, *2)
66 segments \times 17 commons (*1)
67 segments \times 16 commons (*1, *2)
67 segments \times 8 commons (*1)
Built-in LCD power supply circuit (booster type, 5 or 4 potentials)
- Remote controller Infrared remote-control carrier output or DC output
- Serial interface 1 ch. (optional clock synchronous system or asynchronous system *2)
- Programmable timer 16-bit \times 2 ch. or 8-bit \times 4 ch. (*2), with event counter function
- Clock timer 8-bit \times 1 ch.
- Stopwatch timer 8-bit \times 1 ch.

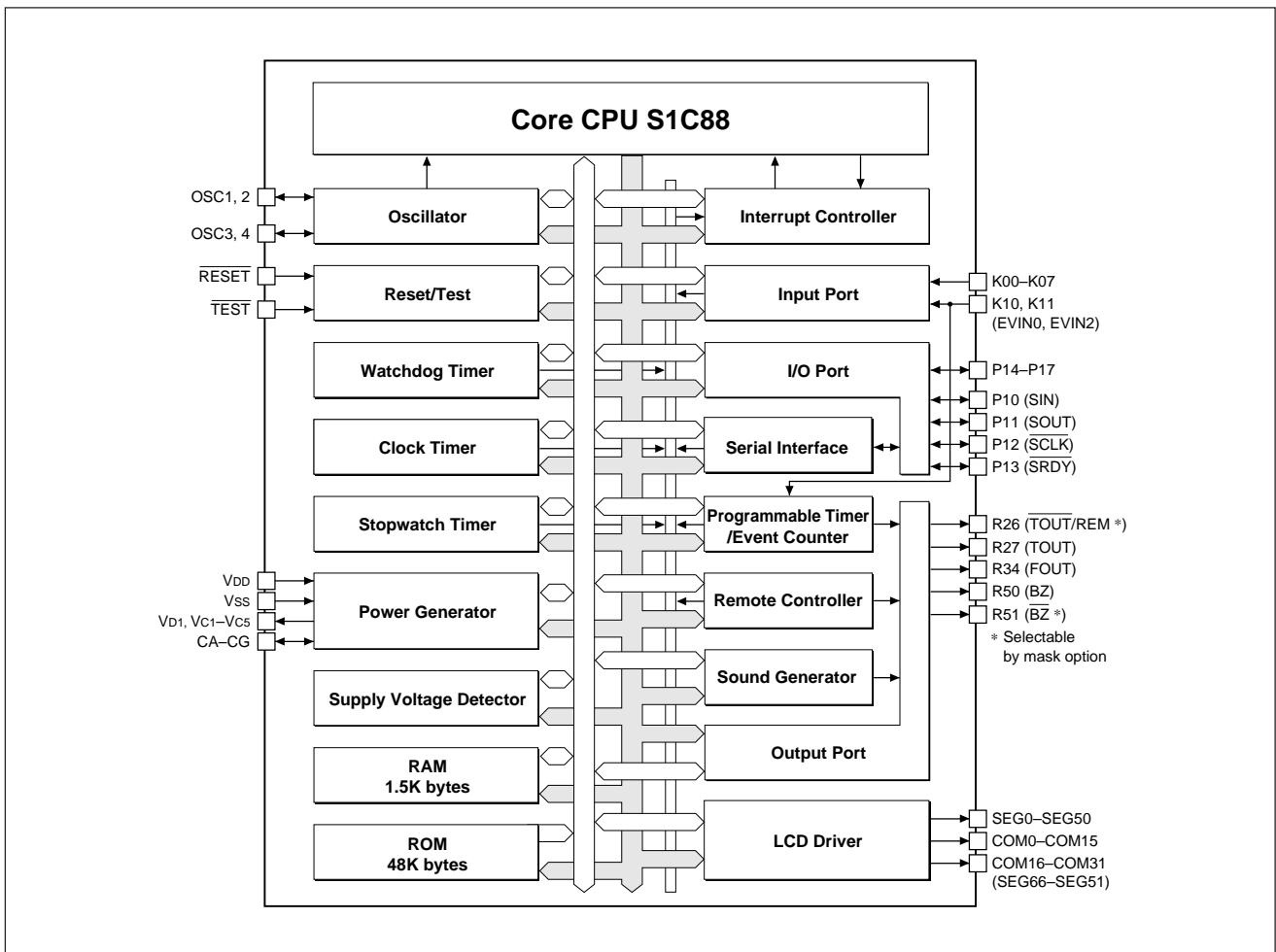
S1C88848

- Sound generator Envelope function, equipped with volume control
 - Watchdog timer Built-in
 - Supply voltage detection (SVD) circuit 16 value programmable (1.8V to 4.35V) (*2)
 - Interrupt

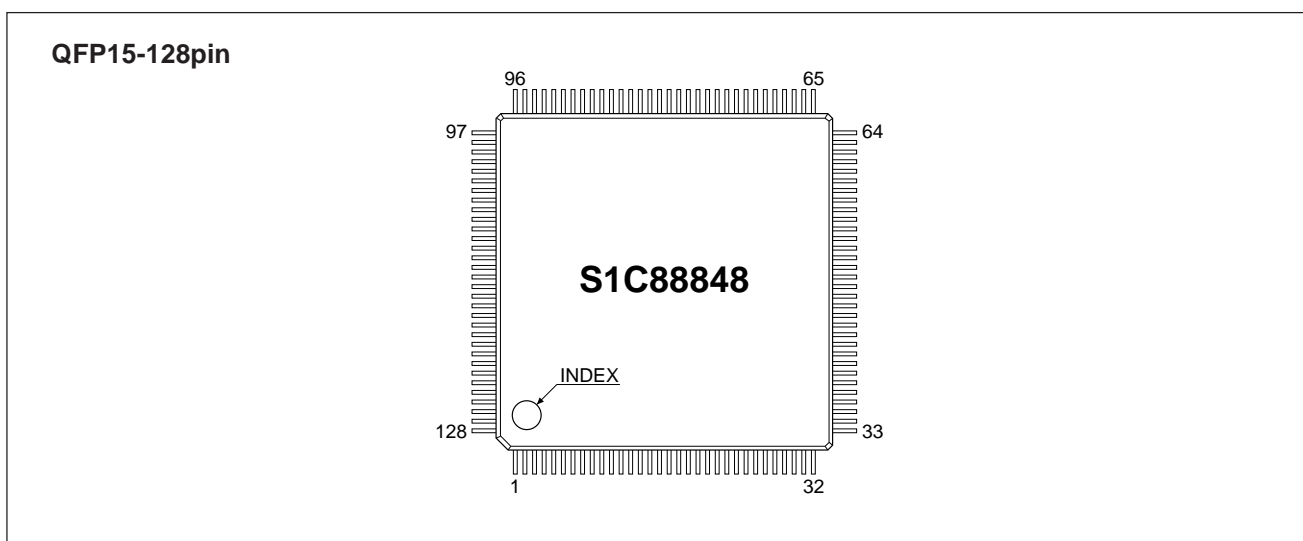
External interrupt: Input port interrupt	2 systems (3 types)
Internal interrupt: Clock timer interrupt	1 system (4 types)
Stopwatch timer interrupt	1 system (3 types)
Programmable timer interrupt	2 systems (4 types)
Serial interface interrupt	1 system (3 types)
Remote-control output interrupt	1 system (1 type)
 - Supply voltage 1.8V to 5.5V (*3)
 - Current consumption (Typ.)

SLEEP mode:	1 μ A
HALT mode (32kHz crystal oscillation):	1.7 μ A
HALT mode (8.2MHz ceramic oscillation):	100 μ A
Run (32kHz crystal oscillation):	4 μ A
Run (8.2MHz ceramic oscillation):	700 μ A
 - Supply form QFP15-128pin or chip
- *1 Mask option *2 Software selection
*3 A supply voltage of less than 2.4 V affects the LCD contrast.

■ BLOCK DIAGRAM



■ PIN LAYOUT DIAGRAM



■ PIN DESCRIPTION

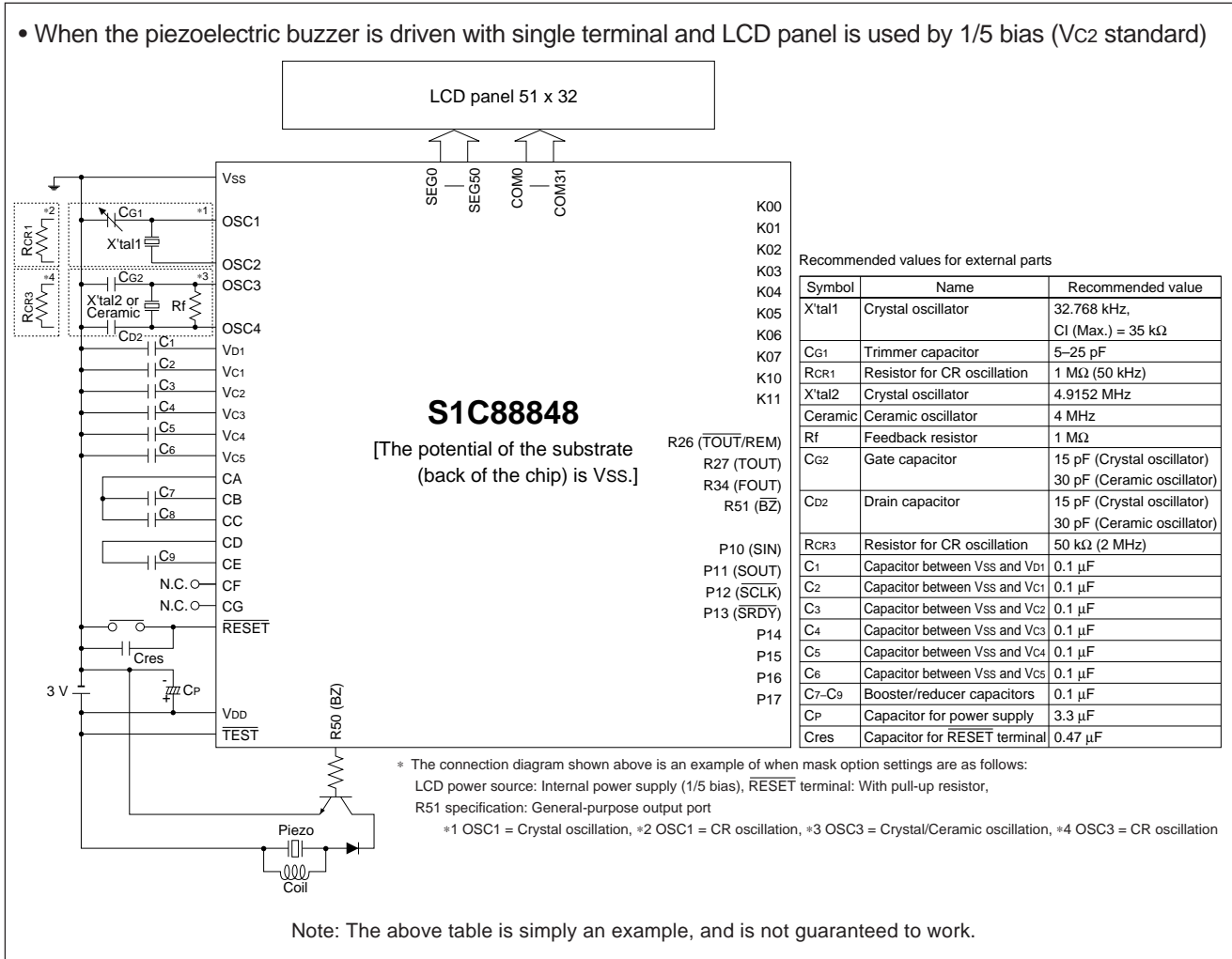
Pin name	Pin No.	In/out	Function
V _{DD}	71	–	Power supply (+) terminal
V _{SS}	72	–	Power supply (GND) terminal
V _{D1}	70	–	Internal operating voltage output terminal
V _{C1} –V _{C5}	67–63	O	LCD drive voltage output terminals
CA–CG	62–58, 95, 96	–	LCD voltage boost/reduce-capacitor connection terminals
OSC1	73	I	OSC1 oscillation input terminal (select crystal or CR oscillation by mask option)
OSC2	74	O	OSC1 oscillation output terminal
OSC3	68	I	OSC3 oscillation input terminal (select crystal, ceramic or CR oscillation by mask option)
OSC4	69	O	OSC3 oscillation output terminal
K00–K07	86–79	I	Input port terminals (K00–K07)
K10/EVIN0	78	I	Input port terminal (K10) or event counter external clock input terminal (EVIN0)
K11/EVIN2	77	I	Input port terminal (K11) or event counter external clock input terminal (EVIN2)
R26/TOUT/REM	97	O	Output port terminal (R26), programmable timer underflow signal inverted output terminal (TOUT) or remote-control carrier output terminal (REM) (selectable by mask option)
R27/TOUT	98	O	Output port terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R34/FOUT	99	O	Output port terminal (R34) or clock output terminal (FOUT)
R50/BZ	100	O	Output port terminal (R50) or buzzer output terminal (BZ)
R51/BZ	101	O	Output port terminal (R51) or buzzer inverted output terminal (BZ) (selectable by mask option)
P10/SIN	94	I/O	I/O port terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	93	I/O	I/O port terminal (P11) or serial I/F data output terminal (SOUT)
P12/SCLK	92	I/O	I/O port terminal (P12) or serial I/F clock I/O terminal (SCLK)
P13/SRDY	91	I/O	I/O port terminal (P13) or serial I/F ready signal output terminal (SRDY)
P14–P17	90–87	I/O	I/O port terminals (P14–P17)
COM0–COM15	102–117	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	56–41	O	LCD common output terminals or LCD segment output terminals COM16–COM31 (when 1/32 duty is selected) SEG66–SEG51 (when 1/16 or 1/8 duty is selected) COM16, SEG65–SEG51 (when 1/17 duty is selected)
SEG0–SEG39	118–128, 1–29	O	LCD segment output terminals
SEG40–SEG50	30–40	O	LCD segment output terminals or DC output terminals (selectable by mask option)
RESET	76	I	Initial reset input terminal
TEST *1	75	I	Test input terminal

*1 TEST is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.

S1C88848

■ BASIC EXTERNAL CONNECTION DIAGRAM

- When the piezoelectric buzzer is driven with single terminal and LCD panel is used by 1/5 bias (Vc2 standard)



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