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S1R72005
Application Note

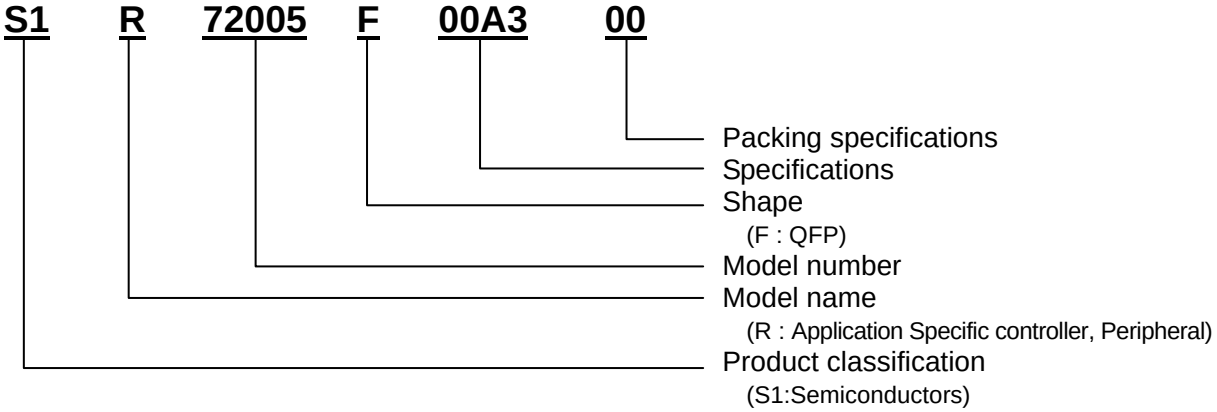
SEIKO EPSON CORPORATION

Rev.1.3

NOTICE

Product number format

- DEVICES



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1 DESCRIPTION

The S1R72005 is an On-The-Go (OTG) device controller LSI supporting USB2.0-compliant, full-speed (12 Mbps) mode. In addition to both host and peripheral functions, it incorporates OTG functions on one chip, enabling an OTG dual-role device operation.

The S1R72005 Application Note summarizes and provides register information for S1R72005.

2 REGISTERS

2.1 Register Map

0x00 to 0x2F

The shaded fields are read/write-enabled regardless of clock supply conditions.

Addr.	Register Name		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	(16bitAccess)	(8bitAccess)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	MainIntStat	MainIntStat_0	DetFreezeDMA	PCIntStat	HCIntStat	MainIntStat_1	DMACmp	PortErr	Cross44V	RcvEP0Setup
0x01		MainIntStat_1	DetReset	DetResume	DetNonJ	DetSuspend	DetRmtWkup	DetSRP	ChangeConnStat	ChangeID
0x02	HCIntStat	HCIntStat							FmNumberOver	SOF
0x03		PIPEIntStat				PIPEdIntStat	PIPEcIntStat	PIPEbIntStat	PIPEaIntStat	PIPE0IntStat
0x04	PCIntStat	PCIntStat								RcvSOF
0x05		EPIntStat	INTranCmp		EPeIntStat	EPdIntStat	EPcIntStat	EPbIntStat	EPaIntStat	EP0IntStat
0x06	(Reserved)	(Reserved)								
0x07		(Reserved)								
0x08	MainIntEnb	MainIntEnb_0	EnDetFreezeDMA	EnPCIntStat	EnHCIntStat	EnMainIntStat_1	EnDMACmp	EnPortErr	EnCross44V	EnRcvEP0Setup
0x09		MainIntEnb_1	EnDetReset	EnDetResume	EnDetNonJ	EnDetSuspend	EnDetRmtWkup	EnDetSRP	EnChangeConnStat	EnChangeID
0x0A	HCIntEnb	HCIntEnb							EnFmNumberOver	EnSOF
0x0B		PIPEIntEnb				EnPIPEdIntStat	EnPIPEcIntStat	EnPIPEbIntStat	EnPIPEaIntStat	EnPIPE0IntStat
0x0C	PCIntEnb	PCIntEnb								EnRcvSOF
0x0D		EPIntEnb	EnINTranCmp		EnEPeIntStat	EnEPdIntStat	EnEPcIntStat	EnEPbIntStat	EnEPaIntStat	EnEP0IntStat
0x0E	(Reserved)	(Reserved)								
0x0F		(Reserved)								

0x10	PIPE0IntStat	PIPE0IntStat	PIPE0TranCmp	CTLTranCmp		PIPE0InShortRcv	PIPE0InOverSize	PIPE0TranErr	PIPE0Stalled	PIPE0NoResp
0x11		(Reserved)								
0x12	PIPEabIntStat	PIPEaIntStat	PIPEaTranCmp			PIPEaInShortRcv	PIPEaInOverSize	PIPEaTranErr	PIPEaStalled	PIPEaNoResp
0x13		PIPEbIntStat	PIPEbTranCmp			PIPEbInShortRcv	PIPEbInOverSize	PIPEbTranErr	PIPEbStalled	PIPEbNoResp
0x14	PIPEcdIntStat	PIPEcIntStat	PIPEcTranCmp			PIPEcInShortRcv	PIPEcInOverSize	PIPEcTranErr	PIPEcStalled	PIPEcNoResp
0x15		PIPEdIntStat	PIPEdTranCmp			PIPEdInShortRcv	PIPEdInOverSize	PIPEdTranErr	PIPEdStalled	PIPEdNoResp
0x16	(Reserved)	(Reserved)								
0x17		(Reserved)								
0x18	PIPE0IntEnb	PIPE0IntEnb	EnPIPE0TranCmp	EnCTLTranCmp		EnPIPE0InShortRcv	EnPIPE0InOverSize	EnPIPE0TranErr	EnPIPE0Stalled	EnPIPE0NoResp
0x19		(Reserved)								
0x1A	PIPEabIntEnb	PIPEaIntEnb	EnPIPEaTranCmp			EnPIPEaInShortRcv	EnPIPEaInOverSize	EnPIPEaTranErr	EnPIPEaStalled	EnPIPEaNoResp
0x1B		PIPEbIntEnb	EnPIPEbTranCmp			EnPIPEbInShortRcv	EnPIPEbInOverSize	EnPIPEbTranErr	EnPIPEbStalled	EnPIPEbNoResp
0x1C	PIPEcdIntEnb	PIPEcIntEnb	EnPIPEcTranCmp			EnPIPEcInShortRcv	EnPIPEcInOverSize	EnPIPEcTranErr	EnPIPEcStalled	EnPIPEcNoResp
0x1D		PIPEdIntEnb	EnPIPEdTranCmp			EnPIPEdInShortRcv	EnPIPEdInOverSize	EnPIPEdTranErr	EnPIPEdStalled	EnPIPEdNoResp
0x1E	(Reserved)	(Reserved)								
0x1F		(Reserved)								

0x20	EP0IntStat	EP0IntStat			EP0INTranACK	EP0OUTTranACK	EP0INTranNAK	EP0OUTTranNAK	EP0INTranErr	EP0OUTTranErr
0x21		(Reserved)								
0x22	EPabIntStat	EPaIntStat		EPaOUTShortACK	EPaINTranACK	EPaOUTTranACK	EPaINTranNAK	EPaOUTTranNAK	EPaINTranErr	EPaOUTTranErr
0x23		EPbIntStat		EPbOUTShortACK	EPbINTranACK	EPbOUTTranACK	EPbINTranNAK	EPbOUTTranNAK	EPbINTranErr	EPbOUTTranErr
0x24	EPcdIntStat	EPcIntStat		EPcOUTShortACK	EPcINTranACK	EPcOUTTranACK	EPcINTranNAK	EPcOUTTranNAK	EPcINTranErr	EPcOUTTranErr
0x25		EPdIntStat		EPdOUTShortACK	EPdINTranACK	EPdOUTTranACK	EPdINTranNAK	EPdOUTTranNAK	EPdINTranErr	EPdOUTTranErr
0x26	EPeIntStat	EPeIntStat		EPeOUTShortACK	EPeINTranACK	EPeOUTTranACK	EPeINTranNAK	EPeOUTTranNAK	EPeINTranErr	EPeOUTTranErr
0x27		(Reserved)								
0x28	EP0IntEnb	EP0IntEnb			EnEP0INTranACK	EnEP0OUTTranACK	EnEP0INTranNAK	EnEP0OUTTranNAK	EnEP0INTranErr	EnEP0OUTTranErr
0x29		(Reserved)								
0x2A	EPabIntEnb	EPaIntEnb		EnEPaOUTShortACK	EnEPaINTranACK	EnEPaOUTTranACK	EnEPaINTranNAK	EnEPaOUTTranNAK	EnEPaINTranErr	EnEPaOUTTranErr
0x2B		EPbIntEnb		EnEPbOUTShortACK	EnEPbINTranACK	EnEPbOUTTranACK	EnEPbINTranNAK	EnEPbOUTTranNAK	EnEPbINTranErr	EnEPbOUTTranErr
0x2C	EPcdIntEnb	EPcIntEnb		EnEPcOUTShortACK	EnEPcINTranACK	EnEPcOUTTranACK	EnEPcINTranNAK	EnEPcOUTTranNAK	EnEPcINTranErr	EnEPcOUTTranErr
0x2D		EPdIntEnb		EnEPdOUTShortACK	EnEPdINTranACK	EnEPdOUTTranACK	EnEPdINTranNAK	EnEPdOUTTranNAK	EnEPdINTranErr	EnEPdOUTTranErr
0x2E	EPeIntEnb	EPeIntEnb		EnEPeOUTShortACK	EnEPeINTranACK	EnEPeOUTTranACK	EnEPeINTranNAK	EnEPeOUTTranNAK	EnEPeINTranErr	EnEPeOUTTranErr
0x2F		(Reserved)								

0x30 to 0x5F

Addr.	Register Name		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	(16bitAccess)	(8bitAccess)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x30	MacroConfig	MacroConfig				COMPPwrDown				ExtResMode
0x31		RevNumber	RevNumber[7:0]							
0x32	CommonControl	CommonControl				ResetXcvr	ResetPC	ResetHC	ResetOTGC	ResetALL
0x33		HCPCCommon						OpMode[2:0]		
0x34	OTGCCommon	OTGCMonitor	LSConnect	ID	LineState[1:0]				Comp20V	Comp44V
0x35		OTGCControl	AllowRmtWkup			BusPwrSel	OTGStateCmd[3:0]			
0x36	HCCommon	(Reserved)								
0x37		HCControl				EnNoFmBulkMode			HCStateCmd[1:0]	
0x38	HCFmNumber	HCFmNumber_H						HCFmNumber[10:8]		
0x39		HCFmNumber_L	HCFmNumber[7:0]							
0x3A	PCCommon	PCControl								SendWakeup
0x3B		PCUSBAddress		USBAddress[6:0]						
0x3C	PCFmNumber	PCFmNumber_H	FnInValid					PCFmNumber[10:8]		
0x3D		PCFmNumber_L	PCFmNumber[7:0]							
0x3E	PipeEPCommon	PipeEPCommon								SetBuffer
0x3F		EPCommon						AutoEnShort	ALLForceNAK	EPrForceSTALL

0x40	DMAConfig	DMAConfig_0	DINLatency[4:0]				DOUTLatency[4:0]			
0x41		DMAConfig_1	ActiveDMA	DMAClkPhase	DMATranMode[1:0]		DREQLevel	DMAEndian	StrobeMode	DMABus8x16
0x42	DMAControl	DMAControl_0			BurstFIFORemain				BurstLength[1:0]	
0x43		DMAControl_1	DMAAbort							DMAGo
0x44	DMACount_H	(Reserved)								
0x45		DMACount_H	DMACount[23:16]							
0x46	DMACount_L	DMACount_M	DMACount[15:8]							
0x47		DMACount_L	DMACount[7:0]							
0x48	CPUConfig	CPUConfig_0		WaitPortDisable	WaitMode	IntMode		CPUEndian		CPUBus8x16
0x49		CPUConfig_1		WaitPortDisable	WaitMode	IntMode		CPUEndian		CPUBus8x16
0x4A	ClkControl	ClkMonitor					CPUClkActive	PLLClkActive	EnPLL	EnOSC
0x4B		ClkControl	OSCWakeUpTime[1:0]		PLLWakeUpTime[1:0]		HCSleep	PCSleep	MainSleep	XcvrSleep
0x4C	ClkCommand	(Reserved)								
0x4D		ClkCommand	ClkCommand[7:0]							
0x4E	(Reserved)	(Reserved)								
0x4F		(Reserved)								

0x50	PIPE0Setup_0	PIPE0Setup_0	PIPE0Setup_0[7:0]
0x51		PIPE0Setup_1	PIPE0Setup_1[7:0]
0x52	PIPE0Setup_2	PIPE0Setup_2	PIPE0Setup_2[7:0]
0x53		PIPE0Setup_3	PIPE0Setup_3[7:0]
0x54	PIPE0Setup_4	PIPE0Setup_4	PIPE0Setup_4[7:0]
0x55		PIPE0Setup_5	PIPE0Setup_5[7:0]
0x56	PIPE0Setup_6	PIPE0Setup_6	PIPE0Setup_6[7:0]
0x57		PIPE0Setup_7	PIPE0Setup_7[7:0]
0x58	EP0Setup_0	EP0Setup_0	EP0Setup_0[7:0]
0x59		EP0Setup_1	EP0Setup_1[7:0]
0x5A	EP0Setup_2	EP0Setup_2	EP0Setup_2[7:0]
0x5B		EP0Setup_3	EP0Setup_3[7:0]
0x5C	EP0Setup_4	EP0Setup_4	EP0Setup_4[7:0]
0x5D		EP0Setup_5	EP0Setup_5[7:0]
0x5E	EP0Setup_6	EP0Setup_6	EP0Setup_6[7:0]
0x5F		EP0Setup_7	EP0Setup_7[7:0]

0x60 to 0x8F

Addr.	Register Name		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	(16bitAccess)	(8bitAccess)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x60	0Config	0Config_0	JoinDMA	FIFOClr						
0x61		0Config_1	DirPID[1:0]				EPNumber[3:0]			
0x62	0MaxPktSize	0MaxPktSize_H		BufferPage[4:0]						
0x63		0MaxPktSize_L	MaxPktSize[6:0]							
0x64	PIPE0Control_0	PIPE0CTLAutoMode						DataStageDir	NoDataStage	EnCTLAuto
0x65		PIPE0TranConfig		Continuity[2:0]				FuncAddr[2:0]		
0x66	PIPE0Control_1	PIPE0Control				Toggle				TranGo
0x67		PIPE0TotalSize_H	TotalSize[23:16]							
0x68	PIPE0Control_2	PIPE0TotalSize_M	TotalSize[15:8]							
0x69		PIPE0TotalSize_L	TotalSize[7:0]							
0x6A	EP0Control	EP0Control_0		AutoForceNAK	InEnShortPkt		InForceNAK	InForceSTALL	OutForceNAK	OutForceSTALL
0x6B		EP0Control_1	InToggleStat		InToggleSet	InToggleClr	OutToggleStat		OutToggleSet	OutToggleClr
0x6C	0FIFOforCPU	0FIFOforCPU_H	FIFOforCPU[15:8]							
0x6D		0FIFOforCPU_L	FIFOforCPU[7:0]							
0x6E	0FIFOControl	0FIFOControl_0	FIFOEmpty	FIFOFull	EnFIFOwr	EnFIFOrd	EnFIFOByteAccess	FIFODataRemain[10:8]		
0x6F		0FIFOControl_1	FIFODataRemain[7:0]							

0x70	aConfig	aConfig_0	JoinDMA	FIFOClr	ToggleMode	AutoZeroLen				
0x71		aConfig_1	DirPID[1:0]		TranType[1:0]		EPNumber[3:0]			
0x72	aMaxPktSize	aMaxPktSize_H		BufferPage[4:0]					MaxPktSize[9:8]	
0x73		aMaxPktSize_L	MaxPktSize[7:0]							
0x74	PIPEaControl_0	PIPEaInterval	Interval[7:0]							
0x75		PIPEaTranConfig		Continuity[2:0]				FuncAddr[2:0]		
0x76	PIPEaControl_1	PIPEaControl				Toggle				TranGo
0x77		PIPEaTotalSize_H	TotalSize[23:16]							
0x78	PIPEaControl_2	PIPEaTotalSize_M	TotalSize[15:8]							
0x79		PIPEaTotalSize_L	TotalSize[7:0]							
0x7A	EPaControl	EPaControl_0	EnEndPoint	AutoForceNAK	EnShortPkt	AutoForceNAKShort			ForceNAK	ForceSTALL
0x7B		EPaControl_1					ToggleStat		ToggleSet	ToggleClr
0x7C	aFIFOforCPU	aFIFOforCPU_H	FIFOforCPU[15:8]							
0x7D		aFIFOforCPU_L	FIFOforCPU[7:0]							
0x7E	aFIFOControl	aFIFOControl_0	FIFOEmpty	FIFOFull	EnFIFOwr	EnFIFOrd	EnFIFOByteAccess	FIFODataRemain[10:8]		
0x7F		aFIFOControl_1	FIFODataRemain[7:0]							

0x80	bConfig	bConfig_0	JoinDMA	FIFOClr	ToggleMode	AutoZeroLen				
0x81		bConfig_1	DirPID[1:0]		TranType[1:0]		EPNumber[3:0]			
0x82	bMaxPktSize	bMaxPktSize_H		BufferPage[4:0]					MaxPktSize[9:8]	
0x83		bMaxPktSize_L	MaxPktSize[7:0]							
0x84	PIPEbControl_0	PIPEbInterval	Interval[7:0]							
0x85		PIPEbTranConfig		Continuity[2:0]				FuncAddr[2:0]		
0x86	PIPEbControl_1	PIPEbControl				Toggle				TranGo
0x87		PIPEbTotalSize_H	TotalSize[23:16]							
0x88	PIPEbControl_2	PIPEbTotalSize_M	TotalSize[15:8]							
0x89		PIPEbTotalSize_L	TotalSize[7:0]							
0x8A	EPbControl	EPbControl_0	EnEndPoint	AutoForceNAK	EnShortPkt	AutoForceNAKShort			ForceNAK	ForceSTALL
0x8B		EPbControl_1					ToggleStat		ToggleSet	ToggleClr
0x8C	bFIFOforCPU	bFIFOforCPU_H	FIFOforCPU[15:8]							
0x8D		bFIFOforCPU_L	FIFOforCPU[7:0]							
0x8E	bFIFOControl	bFIFOControl_0	FIFOEmpty	FIFOFull	EnFIFOwr	EnFIFOrd	EnFIFOByteAccess	FIFODataRemain[10:8]		
0x8F		bFIFOControl_1	FIFODataRemain[7:0]							

0x90 to 0xBF

Addr.	Register Name		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	(16bitAccess)	(8bitAccess)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x90	cConfig	cConfig_0	JoinDMA	FIFOClr	ToggleMode	AutoZeroLen				
0x91		cConfig_1	DirPID[1:0]		TranType[1:0]		EPNumber[3:0]			
0x92	cMaxPktSize	cMaxPktSize_H		BufferPage[4:0]					MaxPktSize[9:8]	
0x93		cMaxPktSize_L	MaxPktSize[7:0]							
0x94	PIPEcControl_0	PIPEcInterval	Interval[7:0]							
0x95		PIPEcTranConfig		Continuity[2:0]				FuncAddr[2:0]		
0x96	PIPEcControl_1	PIPEcControl				Toggle				TranGo
0x97		PIPEcTotalSize_H	TotalSize[23:16]							
0x98	PIPEcControl_2	PIPEcTotalSize_M	TotalSize[15:8]							
0x99		PIPEcTotalSize_L	TotalSize[7:0]							
0x9A	EPcControl	EPcControl_0	EnEndPoint	AutoForceNAK	EnShortPkt	AutoForceNAKShort			ForceNAK	ForceSTALL
0x9B		EPcControl_1					ToggleStat		ToggleSet	ToggleClr
0x9C	cFIFOforCPU	cFIFOforCPU_H	FIFOforCPU[15:8]							
0x9D		cFIFOforCPU_L	FIFOforCPU[7:0]							
0x9E	cFIFOControl	cFIFOControl_0	FIFOEmpty	FIFOFull	EnFIFOwr	EnFIFOrd	EnFIFOByteAccess	FIFODataRemain[10:8]		
0x9F		cFIFOControl_1	FIFODataRemain[7:0]							

0xA0	dConfig	dConfig_0	JoinDMA	FIFOClr	ToggleMode	AutoZeroLen				
0xA1		dConfig_1	DirPID[1:0]		TranType[1:0]		EPNumber[3:0]			
0xA2	dMaxPktSize	dMaxPktSize_H		BufferPage[4:0]					MaxPktSize[9:8]	
0xA3		dMaxPktSize_L	MaxPktSize[7:0]							
0xA4	PIPEdControl_0	PIPEdInterval	Interval[7:0]							
0xA5		PIPEdTranConfig		Continuity[2:0]				FuncAddr[2:0]		
0xA6	PIPEdControl_1	PIPEdControl				Toggle				TranGo
0xA7		PIPEdTotalSize_H	TotalSize[23:16]							
0xA8	PIPEdControl_2	PIPEdTotalSize_M	TotalSize[15:8]							
0xA9		PIPEdTotalSize_L	TotalSize[7:0]							
0xAA	EPdControl	EPdControl_0	EnEndPoint	AutoForceNAK	EnShortPkt	AutoForceNAKShort			ForceNAK	ForceSTALL
0xAB		EPdControl_1					ToggleStat		ToggleSet	ToggleClr
0xAC	dFIFOforCPU	dFIFOforCPU_H	FIFOforCPU[15:8]							
0xAD		dFIFOforCPU_L	FIFOforCPU[7:0]							
0xAE	dFIFOControl	dFIFOControl_0	FIFOEmpty	FIFOFull	EnFIFOwr	EnFIFOrd	EnFIFOByteAccess	FIFODataRemain[10:8]		
0xAF		dFIFOControl_1	FIFODataRemain[7:0]							

0xB0	eConfig	eConfig_0	JoinDMA	FIFOClr	ToggleMode	AutoZeroLen				
0xB1		eConfig_1	DirPID[1:0]		TranType[1:0]		EPNumber[3:0]			
0xB2	eMaxPktSize	eMaxPktSize_H		BufferPage[4:0]					MaxPktSize[9:8]	
0xB3		eMaxPktSize_L	MaxPktSize[7:0]							
0xB4	PIPEeControl_0	PIPEeInterval	Interval[7:0]							
0xB5		PIPEeTranConfig		Continuity[2:0]				FuncAddr[2:0]		
0xB6	PIPEeControl_1	PIPEeControl				Toggle				TranGo
0xB7		PIPEeTotalSize_H	TotalSize[23:16]							
0xB8	PIPEeControl_2	PIPEeTotalSize_M	TotalSize[15:8]							
0xB9		PIPEeTotalSize_L	TotalSize[7:0]							
0xBA	EPeControl	EPeControl_0	EnEndPoint	AutoForceNAK	EnShortPkt	AutoForceNAKShort			ForceNAK	ForceSTALL
0xBB		EPeControl_1					ToggleStat		ToggleSet	ToggleClr
0xBC	eFIFOforCPU	eFIFOforCPU_H	FIFOforCPU[15:8]							
0xBD		eFIFOforCPU_L	FIFOforCPU[7:0]							
0xBE	eFIFOControl	eFIFOControl_0	FIFOEmpty	FIFOFull	EnFIFOwr	EnFIFOrd	EnFIFOByteAccess	FIFODataRemain[10:8]		
0xBF		eFIFOControl_1	FIFODataRemain[7:0]							

0xC0 to 0xEF

Addr.	Register Name		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	(16bitAccess)	(8bitAccess)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0xC0	(Reserved)	(Reserved)								
0xC1		(Reserved)								
0xC2	(Reserved)	(Reserved)								
0xC3		(Reserved)								
0xC4	(Reserved)	(Reserved)								
0xC5		(Reserved)								
0xC6	(Reserved)	(Reserved)								
0xC7		(Reserved)								
0xC8	(Reserved)	(Reserved)								
0xC9		(Reserved)								
0xCA	(Reserved)	(Reserved)								
0xCB		(Reserved)								
0xCC	(Reserved)	(Reserved)								
0xCD		(Reserved)								
0xCE	(Reserved)	(Reserved)								
0xCF		(Reserved)								

0xD0	(Reserved)	(Reserved)								
0xD1		(Reserved)								
0xD2	(Reserved)	(Reserved)								
0xD3		(Reserved)								
0xD4	(Reserved)	(Reserved)								
0xD5		(Reserved)								
0xD6	(Reserved)	(Reserved)								
0xD7		(Reserved)								
0xD8	(Reserved)	(Reserved)								
0xD9		(Reserved)								
0xDA	(Reserved)	(Reserved)								
0xDB		(Reserved)								
0xDC	(Reserved)	(Reserved)								
0xDD		(Reserved)								
0xDE	(Reserved)	(Reserved)								
0xDF		(Reserved)								

0xE0	E_OTGStateCmd	(Reserved)								
0xE1		E_OTGStateCmd	E_OTGStateCmd [7:0]							
0xE2	(Reserved)	(Reserved)								
0xE3		(Reserved)								
0xE4	(Reserved)	(Reserved)								
0xE5		(Reserved)								
0xE6	(Reserved)	(Reserved)								
0xE7		(Reserved)								
0xE8	(Reserved)	(Reserved)								
0xE9		(Reserved)								
0xEA	(Reserved)	(Reserved)								
0xEB		(Reserved)								
0xEC	(Reserved)	(Reserved)								
0xED		(Reserved)								
0xEE	(Reserved)	(Reserved)								
0xEF		(Reserved)								

0xF0 to 0xFF

Addr.	Register Name		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	(16bitAccess)	(8bitAccess)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0xF0	(Reserved)	(Reserved)								
0xF1		(Reserved)								
0xF2	(Reserved)	(Reserved)								
0xF3		(Reserved)								
0xF4	(Reserved)	(Reserved)								
0xF5		(Reserved)								
0xF6	(Reserved)	(Reserved)								
0xF7		(Reserved)								
0xF8	(Reserved)	(Reserved)								
0xF9		(Reserved)								
0xFA	(Reserved)	(Reserved)								
0xFB		(Reserved)								
0xFC	(Reserved)	(Reserved)								
0xFD		(Reserved)								
0xFE	(Reserved)	(Reserved)								
0xFF		(Reserved)								

2.2 Detailed Description of Each Register

2.2.1 Interrupt Main Block

2.2.1.1 0x00 Main Interrupt Status0 (MainIntStat_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x00	MainIntStat_0	7: DetFreezeDMA	R(W)	0: None	1: DetFreezeDMA Occurred	00h
		6: PCIntStat	R	0: None	1: Peripheral Interrupt Occurred	
		5: HCIntStat	R	0: None	1: Host Interrupt Occurred	
		4: MainIntStat_1	R	0: None	1: Main Interrupt 1 Occurred	
		3: DMACmp	R(W)	0: None	1: DMA Transfer Complete	
		2: PortErr	R(W)	0: None	1: Port Error Occurred	
		1: Cross44V	R(W)	0: None	1: Vbus Crossed 4.4V	
		0: RcvEP0Setup	R(W)	0: None	1: Receive EP 0 Setup Transaction	

Displays an S1R72005 interrupt. You can identify an interrupt cause by referring to this register when an interrupt is issued. This register has bits both indirectly and directly indicating an interrupt cause.

A bit indirectly indicating a cause allows determination of the relevant interrupt status register to track the bit directly indicating the cause. Clearing a bit directly indicating the fundamental cause automatically clears the bit indirectly indicating this register's interrupt cause.

For a bit directly indicating an interrupt cause, you can clear the cause by setting the relevant bit to "1." If an interrupt is enabled by the MainIntEnb_0 register, the xINT pin is asserted when an interrupt cause is set to "1," issuing an interrupt to the CPU. The xINT pin is negated if all relevant interrupt causes are cleared.

Bit7 DetFreezeDMA

Directly indicates an interrupt cause.

This bit is set to "1" when DMA word access (16-bit access) is used, the FIFODataRemain of the channel using the DMA is set to "1," and the DMACount at that time is greater than "1" during USB reception (IN transaction during host operation or OUT transaction when peripherals are operating).

DMA transfer is halted when this bit is set to "1." However, the DMAControl register's DMAGo bit is not changed to "0."

This interrupt continues to be asserted while FIFODataRemain = 1 and DMACount > 1.

Since reading of odd-bytes is disabled when the DMACount is greater than "1" during DMA word access, if this interrupt is asserted, the data for the remaining one byte must be read from the FIFOforCPU register while the FIFOControl register's EnFIFOByteAccess bit in the relevant channel is set to "1."

This interrupt is issued during both host and peripheral operations.

This interrupt is issued, for example, when the last packet is received in an odd byte, although the DMACount remains adequate after the DMACount register has been set to an excessive size.

Bit6 PCIntStat

Indirectly indicates an interrupt cause.

This bit is set to "1" when the PCIntStat or EPIntStat register has an interrupt cause and the relevant cause is enabled. This interrupt is issued only when peripherals are operating.

Bit5 HCIntStat

Indirectly indicates an interrupt cause.

This bit is set to "1" when the HCIntStat or PIPEIntStat register has an interrupt cause and the relevant cause is enabled. This interrupt is issued only during host operations.

Bit4 MainIntStat_1

Indirectly indicates an interrupt cause.

This bit is set to "1" when the MainIntStat_1 register has an interrupt cause and the relevant cause is enabled. This bit is used for 8-bit register access.

Bit3 DMACmp

Directly indicates an interrupt cause.

This bit is set to "1" when DMA transfers triggered by the DMAControl_1 register's DMAGo bit are completed up to the size specified by the DMACount_H to L registers. This cause is also set when the DMAControl_1 register's DMAGo bit is changed from "1" to "0" before DMA transfer is completed.

Bit2 PortErr

Set to "1" if a port error (the USB bus does not enter into an idle state, even though a transaction is completed at the frame end: bubble) is detected during host operations. At the same time, the PIPExControl register's TranGo bit is cleared in all channels and the transaction is halted. To restart the transaction, clear this PortErr bit and set the relevant channel's TranGo bit accordingly. This interrupt is issued only during host operations.

Bit1 Cross44V

Directly indicates an interrupt cause.

This bit is set to "1" if the V_{BUS} voltage crosses a threshold of 4.4 V. This bit is enabled regardless of clock input conditions.

Bit0 RcvEP0Setup

Directly indicates an interrupt cause.

This bit is set to "1" when the setup stage is completed at endpoint 0 and the received data is stored in the EP0Setup_0 to EP0Setup_7 registers.When this bit is set to "1," the EP0Control_0 register's InForceSTALL and OutForceSTALL bits are automatically set to "0," and the InForceNAK and OutForceNAK bits to "1."

While the RcvEP0Setup bit is set to "1," do not change the EP0Control_0 register's InForceNAK, OutForceNAK, InForceSTALL and OutForceSTALL bits.

This interrupt is issued only when peripherals are operating.

2.2.1.2 0x01 Main Interrupt Status1 (MainIntStat_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x01	MainIntStat_1	7: DetReset	R(W)	0: None	1: Reset Detected	00h
		6: DetResume	R(W)	0: None	1: Resume Detected	
		5: DetNonJ	R(W)	0: None	1: NonJ Interrupt Occurred	
		4: DetSuspend	R(W)	0: None	1: Susupend Detected	
		3: DetRmtWkup	R(W)	0: None	1: RemoteWakeup Detected	
		2: DetSRP	R(W)	0: None	1: SRP Detected	
		1: ChangeConnStat	R(W)	0: None	1: Connection Status Changed	
		0: ChangeID	R(W)	0: None	1: ChangeID Interrupt Occurred	

As with the MainIntStat_0 register, this also displays an S1R72005 interrupt. You can identify an interrupt cause by referring to this register when an interrupt is issued. This register only has bits directly indicating an interrupt cause. You can clear an interrupt cause by setting the relevant bit to "1." If an interrupt is enabled by the MainIntEnb_1 register, the xINT pin is asserted when an interrupt cause is set to "1," issuing an interrupt to the CPU. The xINT pin is negated if all relevant interrupt causes are cleared.

Bit7 DetReset

Set to "1" if the USB reset state (SE0) is detected when peripherals are operating.

Reset state detection is performed only when peripherals are operating.

Bit6 DetResume

Set to "1" if the USB resume state (K state) is detected when peripherals are operating.

Resume state detection is performed only when peripherals are operating.

Bit5 DetNonJ

Set to "1" if a state other than J is detected on the USB bus in suspend state when peripherals are operating.

If this interrupt is issued, assess the detected signal type based on the SE0 and K states in the OTGCMonitor register's LineState bit.

This bit is enabled regardless of clock input conditions. Non-J state detection is performed only in suspend state when peripherals are operating.

Bit4 DetSuspend

Set to "1" if the USB suspend state (J state for 3 ms) is detected when peripherals are operating.

Suspend state detection is performed only when peripherals are operating.

Bit3 DetRmtWkup

Set to "1" if the remote wakeup state (K state) is detected on the USB bus when the OTGCCommon register's AllowRmtWkup bit is set to "1" during host operations. Remote wakeup state detection is performed only during host operations and when the remote wakeup is enabled.

Bit2 DetSRP

Set to "1" if an SRP signal (data line pulsing: J state for 5 to 10 ms) is detected on the USB bus while device A is in idle state. SRP signal detection is performed only while device A is in idle state.

Bit1 ChangeConnStat

Set to "1" if pullup resistance connection (J state for 2.5μs) or disconnection (SE0 for 2.5μs) is detected for the connection target.

Bit0 ChangeID

Set to "1" if mini A plug's insertion or removal is detected at the OTG receptacle.

This bit is enabled regardless of clock input conditions.

2.2.1.3 0x02 Host Controller Interrupt Status (HCIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x02	HCIntStat	7:				00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1: FmNumberOver	R(W)	0: None	1: Frame Number Over	
		0: SOF	R(W)	0: None	1: SOF Send Complete	

Displays an interrupt applicable to the entire host controller. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1 FmNumberOver

Set to "1" if the frame number counter overflows (the HCFmNumber_H register's MSb [bit 2] is changed from "1" to "0"). An insufficient count digit in the HCFmNumber_H or L register, if any, can be complemented by counting this interrupt.

Bit0 SOF

Set to "1" when the host controller sends an SOF token.

2.2.1.4 0x03 PipeInterrupt Status (PIPEIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x03	PIPEIntStat	7:				00h
		6:				
		5:				
		4: PIPEdIntStat	R	0: None	1: Piped Interrupt Occurred	
		3: PIPEcIntStat	R	0: None	1: Pipec Interrupt Occurred	
		2: PIPEbIntStat	R	0: None	1: Pipeb Interrupt Occurred	
		1: PIPEaIntstat	R	0: None	1: Pipea Interrupt Occurred	
		0: PIPE0IntStat	R	0: None	1: Pipe0 Interrupt Occurred	

Indirectly indicates an interrupt applicable to host controller's pipe control (USB transfer control).

If all bits of the relevant fundamental interrupt cause register (PIPEaIntStat to PIPEeIntStat registers) are cleared, this register's relevant bit is also cleared.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 PIPEdIntStat

Set to "1" when the PIPEdIntStat register has an interrupt cause and the PIPEdIntEnb register's relevant bit is enabled.

Bit3 PIPEcIntStat

Set to "1" when the PIPEcIntStat register has an interrupt cause and the PIPEcIntEnb register's relevant bit is enabled.

Bit2 PIPEbIntStat

Set to "1" when the PIPEbIntStat register has an interrupt cause and the PIPEbIntEnb register's relevant bit is enabled.

Bit1 PIPEaIntStat

Set to "1" when the PIPEaIntStat register has an interrupt cause and the PIPEaIntEnb register's relevant bit is enabled.

Bit0 PIPE0IntStat

Set to "1" when the PIPE0IntStat register has an interrupt cause and the PIPE0IntEnb register's relevant bit is enabled.

2.2.1.5 0x04 Peripheral Controller Interrupt Status (PCIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x04	PCIntStat	7:				00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0: RcvSOF	R(W)	0: None	1: Receive SOF Token	

Displays an interrupt applicable to the entire peripheral controller. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 RcvSOF

Set to "1" when an SOF token is received.

2.2.1.6 0x05 EndpointInterrupt Status (EPIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x05	EPIntStat	7: INTranCmp	R/(W)	0: None	1: IN Transaction Completed	00h
		6:				
		5: EPeIntStat	R	0: None	1: EP e Interrupt Occurred	
		4: EPdIntStat	R	0: None	1: EP d Interrupt Occurred	
		3: EPcIntStat	R	0: None	1: EP c Interrupt Occurred	
		2: EPbIntStat	R	0: None	1: EP b Interrupt Occurred	
		1: EPaIntStat	R	0: None	1: EP a Interrupt Occurred	
		0: EP0IntStat	R	0: None	1: EP 0 Interrupt Occurred	

Directly or indirectly indicates an interrupt cause for each endpoint.

An indirect reference bit is cleared if all interrupt causes (fundamental interrupt causes) for the relevant endpoint are cleared.

Bit7 INTranCmp

Set to "1" if an ACK is received (USB transmission of all data to be transferred is completed) after DMA transfer of the specified byte count has been completed and all data in the FIFO has been transferred for an IN transaction at an endpoint where the Config_0 register's JoinDMA bit is set to "1" in each channel.

Bit6 Reserved

Bit5 EPeIntStat

Set to "1" when the EPeIntStat register has an interrupt cause and the EPeIntEnb register's relevant bit is enabled.

Bit4 EPdIntStat

Set to "1" when the EPdIntStat register has an interrupt cause and the EPdIntEnb register's relevant bit is enabled.

Bit3 EPcIntStat

Set to "1" when the EPcIntStat register has an interrupt cause and the EPcIntEnb register's relevant bit is enabled.

Bit2 EPbIntStat

Set to "1" when the EPbIntStat register has an interrupt cause and the EPbIntEnb register's relevant bit is enabled.

Bit1 EPaIntStat

Set to "1" when the EPaIntStat register has an interrupt cause and the EPaIntEnb register's relevant bit is enabled.

Bit0 EP0IntStat

Set to "1" when the EP0IntStat register has an interrupt cause and the EP0IntEnb register's relevant bit is enabled.

2.2.1.7 0x06 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x06	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.1.8 0x07 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x07	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.1.9 0x08 Main Interrupt Enable0 (MainIntEnb_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x08	MainIntEnb_0	7: EnDetFreezeDMA	R/W	0: Disable	1: Enable	00h
		6: EnPCIntStat	R/W	0: Disable	1: Enable	
		5: EnHCIntStat	R/W	0: Disable	1: Enable	
		4: EnMainIntStat_1	R/W	0: Disable	1: Enable	
		3: EnDMACmp	R/W	0: Disable	1: Enable	
		2: EnPortErr	R/W	0: Disable	1: Enable	
		1: EnCross44V	R/W	0: Disable	1: Enable	
		0: EnRcvEP0Setup	R/W	0: Disable	1: Enable	

Enables/disables the assertion of an interrupt signal to the CPU in the MainIntStat_0 register.

Set the relevant bit to “1” to enable an interruption of the CPU.

The EnCross44V bit is enabled regardless of clock input conditions.

2.2.1.10 0x09 Main Interrupt Enable1 (MainIntEnb_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x09	MainIntEnb_1	7: EnDetReset	R/W	0: Disable	1: Enable	00h
		6: EnDetResume	R/W	0: Disable	1: Enable	
		5: EnDetNonJ	R/W	0: Disable	1: Enable	
		4: EnDetSuspend	R/W	0: Disable	1: Enable	
		3: EnDetRmtWkup	R/W	0: Disable	1: Enable	
		2: EnDetSRP	R/W	0: Disable	1: Enable	
		1: EnChangeConnStat	R/W	0: Disable	1: Enable	
		0: EnChangeID	R/W	0: Disable	1: Enable	

Enables/disables a MainIntStat_1 register interrupt cause.

Set the relevant bit to “1” to enable an interruption of the CPU.

The DetNonJ and ChangeID bits are enabled regardless of clock input conditions.

2.2.1.11 0x0A Host Controller Interrupt Enable (HCIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x0A	HCIntEnb	7:				00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1: EnFmNumberOver	R/W	0: Disable	1: Enable	
		0: EnSOF	R/W	0: Disable	1: Enable	

Enables/disables an HCIntStat register interrupt cause.

Set the relevant bit to "1" to allow transmission of an HCIntStat register interrupt cause to the MainIntStat register's HCIntStat bit.

2.2.1.12 0x0B PipeInterrupt Enable (PIPEIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x0B	PIPEIntEnb	7:				00h
		6:				
		5:				
		4: EnPIPEdIntStat	R/W	0: Disable	1: Enable	
		3: EnPIPEcIntStat	R/W	0: Disable	1: Enable	
		2: EnPIPEbIntStat	R/W	0: Disable	1: Enable	
		1: EnPIPEaIntstat	R/W	0: Disable	1: Enable	
		0: EnPIPE0IntStat	R/W	0: Disable	1: Enable	

Enables/disables a PIPEIntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PIPEIntStat register interrupt cause to the MainIntStat register’s HC_IntStat bit.

2.2.1.13 0x0C Peripheral Controller Interrupt Enable (PCIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x0C	PCIntEnb	7:				00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0: RcvSOF	R/W	0: Disable	1: Enable	

Enables/disables a PCIntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PCIntStat register interrupt cause to the MainIntStat register’s PCIntStat bit.

2.2.1.14 0x0D EndpointInterrupt Enable (EPIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x0D	EPIntEnb	7: INTranCmp	R/W	0: Disable	1: Enable	00h
		6:				
		5: EPeIntStat	R/W	0: Disable	1: Enable	
		4: EPdIntStat	R/W	0: Disable	1: Enable	
		3: EPcIntStat	R/W	0: Disable	1: Enable	
		2: EPbIntStat	R/W	0: Disable	1: Enable	
		1: EPaIntStat	R/W	0: Disable	1: Enable	
		0: EP0IntStat	R/W	0: Disable	1: Enable	

Enables/disables an EPIntStat register interrupt cause.

In indirect reference cause bits, set the relevant bit to “1” to transmit an EPIntStat register interrupt cause to the MainIntStat register’s PC_IntStat bit.

2.2.1.15 0x0E (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x0E	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.1.16 0x0F (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x0F	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.2 Pipe Interrupt Block

2.2.2.1 0x10 Pipe0 Interrupt Status (PIPE0IntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x10	PIPE0IntStat	7: PIPE0TranCmp	R(W)	0: None	1: Transaction Complete	00h
		6: CTLTranCmp	R(W)	0: None	1: Control Transaction Complete	
		5:				
		4: PIPE0InShortRcv	R(W)	0: None	1: Receive ShortPacket	
		3: PIPE0InOverSize	R(W)	0: None	1: Receive Oversize Packet	
		2: PIPE0TranErr	R(W)	0: None	1: Transfer Error Occured	
		1: PIPE0Stalled	R(W)	0: None	1: Stall Occured	
		0: PIPE0NoResp	R(W)	0: None	1: Device NoResponce	

Displays a PIPE0 interrupt cause. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

These interrupts occur only during host operations.

Bit7 PIPE0TranCmp

Set to "1" when transfer of the data size specified by the PIPE0TotalSize_H to L registers is completed.

For an OUT transaction, "completed" means that the last packet in the total size (transmittable size) has been transferred from the FIFO onto the USB and an ACK has been received from a device. For an IN transaction, it means that the last packet in the total size (receivable size) has been received in the FIFO without errors.

This bit is not changed to "1" if an unexpected short packet is received without errors. In this case, a PIPE0InShortRcv interrupt is issued.

If "0" is written to the PiPE0Control register's TranGo bit to stop operation during transaction execution, this bit is set to "1" after the transaction being executed when the bit has been cleared is successfully completed.

This cause is not set if a STALL is received or in cases of completion with errors.

Bit6 CTLTranCmp

Set to "1" if all control transfer stages are successfully completed after the transaction has been started with the PIPE0CTLAutoMode register's EnCTLAuto bit set to "1."In this case, no PIPE0TranCmp interrupt is issued.

If an error is detected or a STALL is received during a transaction, an interrupt cause corresponding to each of the following cases, rather than this cause, is set to that time, no matter what the transaction stage is. However, if an unexpected short packet is received at the data stage, no PIPE0InShortRcv interrupt cause is set, but the transaction shifts to the status stage.

Bit5 Reserved

Bit4 PIPE0InShortRcv

Set to "1" if an unexpected short packet is received without errors before the receivable size specified by the PIPE0TotalSize_H to L registers is reached for an IN transaction when the PIPE0CTLAutoMode register's EnCTLAuto bit is set to "0."

In this case, no PIPE0TranCmp interrupt is issued, although the PIPE0Control register's TranGo bit is cleared to halt the transaction. In addition, this interrupt does not occur when the PIPE0CTLAutoMode register's EnCTLAuto is enabled.

Bit3 PIPE0InOverSize

Set to “1” if packets larger than the size specified by the PIPE0MaxPktSize register are received in one IN transaction. Although data reception and transaction are halted at this point, data received before the maximum packet size has been reached remains in the FIFO.

Bit2 PIPE0TranErr

Set to “1” if a CRC error, bit stuff error, PID error (damaged PID code data), or protocol error (detection of an unexpected or undefined PID, toggle sequence error, etc.) is detected three times in succession, in total, for an IN transaction. In this case, the TranGo in this channel is cleared to halt the transaction (no ACK handshake is sent after data reception).This bit is not set when a NAK is received or the above transmission error is not repeated three or more times.

Bit1 PIPE0Stalled

Set to “1” if a STALL is returned from a device during transaction execution. When a STALL is received, this channel’s TranGo bit is cleared to halt the transaction.

Bit0 PIPE0NoResp

Set to “1” if a device reply wait timeout (no device reply) is detected three times in succession. At this point, this channel’s TranGo bit is cleared to halt the transaction.

2.2.2.2 0x11 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x11	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.2.3 0x12 PipeA Interrupt Status (PIPEaIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x12	PIPEaIntStat	7: PIPEaTranCmp	R(W)	0: None	1: Transaction Complete	00h
		6:				
		5:				
		4: PIPEaInShortRcv	R(W)	0: None	1: Receive ShortPacket	
		3: PIPEaInOverSize	R(W)	0: None	1: Receive Oversize Packet	
		2: PIPEaTranErr	R(W)	0: None	1: Transfer Error Occured	
		1: PIPEaStalled	R(W)	0: None	1: Stall Occured	
		0: PIPEaNoResp	R(W)	0: None	1: Device NoResponce	

Displays a PIPEa interrupt cause. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

These interrupts occur only during host operations.

Bit7 PIPEaTranCmp

Set to "1" when transfer of the data size specified by the PIPEaTotalSize_H to L registers is completed.

For an OUT transaction, "completed" means that the last packet in the total size (transmittable size) has been transferred from the FIFO onto the USB and an ACK has been received from a device. For an IN transaction, it means that the last packet in the total size (receivable size) has been received in the FIFO without errors.

This bit is not changed to "1" if an unexpected short packet is received without errors. In this case, a PIPEaInShortRcv interrupt is issued.

If "0" is written to the PIPEaControl register's TranGo bit to stop operation during transaction execution, this bit is set to "1."

This cause is not set if a STALL is received or in cases of completion with errors.

Bit6 Reserved

Bit5 Reserved

Bit4 PIPEaInShortRcv

Set to "1" if an unexpected short packet is received without errors before the receivable size specified by the PIPEaTotalSize_H to L registers is reached for an IN transaction. In this case, no PIPEaTranCmp interrupt is issued, although the PiPEaControl register's TranGo bit is cleared to halt the transaction.

Bit3 PIPEaInOverSize

Set to "1" if packets larger than the size specified by the PIPEaMaxPktSize register are received in one IN transaction. Although data reception and transaction are halted at this point, data received before the maximum packet size has been reached remains in the FIFO.

Bit2 PIPEaTranErr

Set to "1" if a CRC error, bit stuff error, PID error (damaged PID code data), or protocol error (detection of an unexpected or undefined PID, toggle sequence error, etc.) is detected three times in succession, in total, for an IN transaction. In this case, the TranGo in this channel is cleared to halt the transaction (no ACK handshake is sent after data reception). This bit is not set when a NAK is received or the above transmission error is not repeated three or more times.

Bit1 PIPEaStalled

Set to "1" if a STALL is returned from a device during transaction execution. When a STALL is received, this channel's TranGo bit is cleared to halt the transaction.

Bit0 PIPEaNoResp

Set to "1" if a device reply wait timeout (no device reply) is detected three times in succession. At this point, this channel's TranGo bit is cleared to halt the transaction.

2.2.2.4 0x13 PipeB Interrupt Status (PIPEbIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x13	PIPEbIntStat	7: PIPEbTranCmp	R(W)	0: None	1: Transaction Complete	00h
		6:				
		5:				
		4: PIPEbInShortRcv	R(W)	0: None	1: Receive ShortPacket	
		3: PIPEbInOverSize	R(W)	0: None	1: Receive Oversize Packet	
		2: PIPEbTranErr	R(W)	0: None	1: Transfer Error Occured	
		1: PIPEbStalled	R(W)	0: None	1: Stall Occured	
		0: PIPEbNoResp	R(W)	0: None	1: Device NoResponce	

Displays a PIPEb interrupt cause. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

These interrupts occur only during host operations.

Bit7 PIPEbTranCmp

Set to "1" when transfer of the data size specified by the PIPEbTotalSize_H to L registers is completed.

For an OUT transaction, "completed" means that the last packet in the total size (transmittable size) has been transferred from the FIFO onto the USB and an ACK has been received from a device. For an IN transaction, it means that the last packet in the total size (receivable size) has been received in the FIFO without errors.

This bit is not changed to "1" if an unexpected short packet is received without errors. In this case, a PIPEbInShortRcv interrupt is issued.

If "0" is written to the PIPEaControl register's TranGo bit to stop operation during transaction execution, this bit is set to "1."

This cause is not set if a STALL is received or in cases of completion with errors.

Bit6 Reserved

Bit5 Reserved

Bit4 PIPEbInShortRcv

Set to "1" if an unexpected short packet is received without errors before the receivable size specified by the PIPEbTotalSize_H to L registers is reached for an IN transaction. In this case, no PIPEbTranCmp interrupt is issued, although the PiPEaControl register's TranGo bit is cleared to halt the transaction.

Bit3 PIPEbInOverSize

Set to "1" if packets larger than the size specified by the PIPEbMaxPktSize register are received in one IN transaction. Although data reception and transaction are halted at this point, data received before the maximum packet size has been reached remains in the FIFO.

Bit2 PIPEbTranErr

Set to “1” if a CRC error, bit stuff error, PID error (damaged PID code data), or protocol error (detection of an unexpected or undefined PID, toggle sequence error, etc.) is detected three times in succession, in total, for an IN transaction. In this case, the TranGo in this channel is cleared to halt the transaction (no ACK handshake is sent after data reception). This bit is not set when a NAK is received or the above transmission error is not repeated three or more times.

Bit1 PIPEbStalled

Set to “1” if a STALL is returned from a device during transaction execution. When a STALL is received, this channel’s TranGo bit is cleared to halt the transaction.

Bit0 PIPEbNoResp

Set to “1” if a device reply wait timeout (no device reply) is detected three times in succession. At this point, this channel’s TranGo bit is cleared to halt the transaction.

2.2.2.5 0x14 PipeC Interrupt Status (PIPEcIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x14	PIPEcIntStat	7: PIPEcTranCmp	R(W)	0: None	1: Transaction Complete	00h
		6:				
		5:				
		4: PIPEcInShortRcv	R(W)	0: None	1: Receive ShortPacket	
		3: PIPEcInOverSize	R(W)	0: None	1: Receive Oversize Packet	
		2: PIPEcTranErr	R(W)	0: None	1: Transfer Error Occured	
		1: PIPEcStalled	R(W)	0: None	1: Stall Occured	
		0: PIPEcNoResp	R(W)	0: None	1: Device NoResponce	

Displays a PIPEc interrupt cause. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

These interrupts occur only during host operations.

Bit7 PIPEcTranCmp

Set to "1" when transfer of the data size specified by the PIPEcTotalSize_H to L registers is completed.

For an OUT transaction, "completed" means that the last packet in the total size (transmittable size) has been transferred from the FIFO onto the USB and an ACK has been received from a device. For an IN transaction, it means that the last packet in the total size (receivable size) has been received in the FIFO without errors.

This bit is not changed to "1" if an unexpected short packet is received without errors. In this case, a PIPEcInShortRcv interrupt is issued.

If "0" is written to the PiPEcControl register's TranGo bit to stop operation during transaction execution, this bit is set to "1."

This cause is not set if a STALL is received or in cases of completion with errors.

Bit6 Reserved

Bit5 Reserved

Bit4 PIPEcInShortRcv

Set to "1" if an unexpected short packet is received without errors before the receivable size specified by the PIPEcTotalSize_H to L registers is reached for an IN transaction. In this case, no PIPEcTranCmp interrupt is issued, although the PiPEaControl register's TranGo bit is cleared to halt the transaction.

Bit3 PIPEcInOverSize

Set to "1" if packets larger than the size specified by the PIPEcMaxPktSize register are received in one IN transaction. Although data reception and transaction are halted at this point, data received before the maximum packet size has been reached remains in the FIFO.

Bit2 PIPEcTranErr

Set to “1” if a CRC error, bit stuff error, PID error (damaged PID code data), or protocol error (detection of an unexpected or undefined PID, toggle sequence error, etc.) is detected three times in succession, in total, for an IN transaction. In this case, the TranGo in this channel is cleared to halt the transaction (no ACK handshake is sent after data reception).This bit is not set when a NAK is received or the above transmission error is not repeated three or more times.

Bit1 PIPEcStalled

Set to “1” if a STALL is returned from a device during transaction execution. When a STALL is received, this channel’s TranGo bit is cleared to halt the transaction.

Bit0 PIPEcNoResp

Set to “1” if a device reply wait timeout (no device reply) is detected three times in succession. At this point, this channel’s TranGo bit is cleared to halt the transaction.

2.2.2.6 0x15 PipeD Interrupt Status (PIPEdIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x15	PIPEdIntStat	7: PIPEdTranCmp	R(W)	0: None	1: Transaction Complete	00h
		6:				
		5:				
		4: PIPEdInShortRcv	R(W)	0: None	1: Receive ShortPacket	
		3: PIPEdInOverSize	R(W)	0: None	1: Receive Oversize Packet	
		2: PIPEdTranErr	R(W)	0: None	1: Transfer Error Occured	
		1: PIPEdStalled	R(W)	0: None	1: Stall Occured	
		0: PIPEdNoResp	R(W)	0: None	1: Device NoResponce	

Displays a PIPEd interrupt cause. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

These interrupts occur only during host operations.

Bit7 PIPEdTranCmp

Set to "1" when transfer of the data size specified by the PIPEdTotalSize_H to L registers is completed.

For an OUT transaction, "completed" means that the last packet in the total size (transmittable size) has been transferred from the FIFO onto the USB and an ACK has been received from a device. For an IN transaction, it means that the last packet in the total size (receivable size) has been received in the FIFO without errors.

This bit is not changed to "1" if an unexpected short packet is received without errors. In this case, a PIPEdInShortRcv interrupt is issued.

If "0" is written to the PiPEdControl register's TranGo bit to stop operation during transaction execution, this bit is set to "1."

This cause is not set if a STALL is received or in cases of completion with errors.

Bit6 Reserved

Bit5 Reserved

Bit4 PIPEdInShortRcv

Set to "1" if an unexpected short packet is received without errors before the receivable size specified by the PIPEdTotalSize_H to L registers is reached for an IN transaction. In this case, no PIPEdTranCmp interrupt is issued, although the PiPEaControl register's TranGo bit is cleared to halt the transaction.

Bit3 PIPEdInOverSize

Set to "1" if packets larger than the size specified by the PIPEdMaxPktSize register are received in one IN transaction. Although data reception and transaction are halted at this point, data received before the maximum packet size has been reached remains in the FIFO.

Bit2 PIPEdTranErr

Set to “1” if a CRC error, bit stuff error, PID error (damaged PID code data), or protocol error (detection of an unexpected or undefined PID, toggle sequence error, etc.) is detected three times in succession, in total, for an IN transaction. In this case, the TranGo in this channel is cleared to halt the transaction (no ACK handshake is sent after data reception). This bit is not set when a NAK is received or the above transmission error is not repeated three or more times.

Bit1 PIPEdStalled

Set to “1” if a STALL is returned from a device during transaction execution. When a STALL is received, this channel’s TranGo bit is cleared to halt the transaction.

Bit0 PIPEdNoResp

Set to “1” if a device reply wait timeout (no device reply) is detected three times in succession. At this point, this channel’s TranGo bit is cleared to halt the transaction.

2.2.2.7 0x16 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x16	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.2.8 0x17 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x17	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.2.9 0x18 Pipe0 Interrupt Enable (PIPE0IntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x18	PIPE0IntEnb	7: EnPIPE0TranCmp	R/W	0: Disable	1: Enable	00h
		6: EnCTLTranCmp	R/W	0: Disable	1: Enable	
		5:				
		4: EnPIPE0InShortRcv	R/W	0: Disable	1: Enable	
		3: EnPIPE0InOverSize	R/W	0: Disable	1: Enable	
		2: EnPIPE0TranErr	R/W	0: Disable	1: Enable	
		1: EnPIPE0Stalled	R/W	0: Disable	1: Enable	
		0: EnPIPE0NoResp	R/W	0: Disable	1: Enable	

Enables/disables a PIPE0IntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PIPE0IntStat register interrupt cause to the PIPEIntStat register’s PIPE0IntStat bit.

2.2.2.10 0x19 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x19	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.2.11 0x1A PipeA Interrupt Enable (PIPEaIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x1A	PIPEaIntEnb	7: EnPIPEaTranCmp	R/W	0: Disable	1: Enable	00h
		6:				
		5:				
		4: EnPIPEaInShortRcv	R/W	0: Disable	1: Enable	
		3: EnPIPEaInOverSize	R/W	0: Disable	1: Enable	
		2: EnPIPEaTranErr	R/W	0: Disable	1: Enable	
		1: EnPIPEaStalled	R/W	0: Disable	1: Enable	
		0: EnPIPEaNoResp	R/W	0: Disable	1: Enable	

Enables/disables a PIPEaIntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PIPEaIntStat register interrupt cause to the PIPEIntStat register’s PIPEaIntStat bit.

2.2.2.12 0x1B PipeB Interrupt Enable (PIPEbIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x1B	PIPEbIntEnb	7: EnPIPEbTranCmp	R/W	0: Disable	1: Enable	00h
		6:				
		5:				
		4: EnPIPEbInShortRcv	R/W	0: Disable	1: Enable	
		3: EnPIPEbInOverSize	R/W	0: Disable	1: Enable	
		2: EnPIPEbTranErr	R/W	0: Disable	1: Enable	
		1: EnPIPEbStalled	R/W	0: Disable	1: Enable	
		0: EnPIPEbNoResp	R/W	0: Disable	1: Enable	

Enables/disables a PIPEbIntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PIPEbIntStat register interrupt cause to the PIPEIntStat register’s PIPEbIntStat bit.

2.2.2.13 0x1C PipeC Interrupt Enable (PIPEcIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x1C	PIPEcIntEnb	7: EnPIPEcTranCmp	R/W	0: Disable	1: Enable	00h
		6:				
		5:				
		4: EnPIPEcInShortRcv	R/W	0: Disable	1: Enable	
		3: EnPIPEcInOverSize	R/W	0: Disable	1: Enable	
		2: EnPIPEcTranErr	R/W	0: Disable	1: Enable	
		1: EnPIPEcStalled	R/W	0: Disable	1: Enable	
		0: EnPIPEcNoResp	R/W	0: Disable	1: Enable	

Enables/disables a PIPEcIntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PIPEcIntStat register interrupt cause to the PIPEIntStat register’s PIPEcIntStat bit.

2.2.2.14 0x1D PipeD Interrupt Enable (PIPEdIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x1D	PIPEdIntEnb	7: EnPIPEdTranCmp	R/W	0: Disable	1: Enable	00h
		6:				
		5:				
		4: EnPIPEdInShortRcv	R/W	0: Disable	1: Enable	
		3: EnPIPEdInOverSize	R/W	0: Disable	1: Enable	
		2: EnPIPEdTranErr	R/W	0: Disable	1: Enable	
		1: EnPIPEdStalled	R/W	0: Disable	1: Enable	
		0: EnPIPEdNoResp	R/W	0: Disable	1: Enable	

Enables/disables a PIPEdIntStat register interrupt cause.

Set the relevant bit to “1” to transmit a PIPEdIntStat register interrupt cause to the PIPEIntStat register’s PIPEdIntStat bit.

2.2.2.15 0x1E (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x1E	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.2.16 0x1F (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x1F	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.3 Endpoint Interrupt Block

2.2.3.1 0x20 Endpoint0 Interrupt Status (EP0IntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x20	EP0IntStat	7:				00h
		6:				
		5: EP0INTranAck	R(W)	0: None	1: IN Transaction ACK	
		4: EP0OUTTranACK	R(W)	0: None	1: OUT Transaction ACK	
		3: EP0INTranNAK	R(W)	0: None	1: IN Transaction NAK	
		2: EP0OUTTranNAK	R(W)	0: None	1: OUT Transaction NAK	
		1: EP0INTranErr	R(W)	0: None	1: IN Transaction Error	
		0: EP0OUTTranErr	R(W)	0: None	1: OUT Transaction Error	

Displays the interrupt status at endpoint 0. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

These interrupts occur only when peripherals are operating.

Bit7 Reserved

Bit6 Reserved

Bit5 EP0INTranAck

Set to "1" when an ACK is received by an IN transaction.

Bit4 EP0OUTTranACK

Set to "1" when an ACK is returned by an OUT transaction.

Bit3 EP0INTranNAK

Set to "1" when a NAK is returned by an IN transaction.

Bit2 EP0OUTTranNAK

Set to "1" when a NAK is returned to an OUT transaction.

Bit1 EP0INTranErr

Set to "1" when a STALL is returned, a packet error is detected or a handshake timeout occurs during an IN transaction.

Bit0 EP0OUTTranErr

Set to "1" when a STALL is returned or a packet error is detected during an OUT transaction.

2.2.3.2 0x21 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x21	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.3.3 0x22 EndpointA Interrupt Status (EPaIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x22	EPaIntStat	7:				00h
		6: EPaOUTShortACK	R(W)	0: None	1: OUT Short Packet ACK	
		5: EPaINTranAck	R(W)	0: None	1: IN Transaction ACK	
		4: EPaOUTTranACK	R(W)	0: None	1: OUT Transaction ACK	
		3: EPaINTranNAK	R(W)	0: None	1: IN Transaction NAK	
		2: EPaOUTTranNAK	R(W)	0: None	1: OUT Transaction NAK	
		1: EPaINTranErr	R(W)	0: None	1: IN Transaction Error	
		0: EPaOUTTranErr	R(W)	0: None	1: OUT Transaction Error	

Displays the interrupt status at endpointA. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 EPaOUTShortACK

Set to "1" when a short packet is received and an ACK is returned by an OUT transaction.

Bit5 EPaINTranAck

Set to "1" when an ACK is received by an IN transaction.

Bit4 EPaOUTTranACK

Set to "1" when an ACK is returned by an OUT transaction.

Bit3 EPaINTranNAK

Set to "1" when a NAK is returned by an IN transaction.

Bit2 EPaOUTTranNAK

Set to "1" when a NAK is returned to an OUT transaction.

Bit1 EPaINTranErr

Set to "1" when a STALL is returned, a packet error is detected or a handshake timeout occurs during an IN transaction.

Bit0 EPaOUTTranErr

Set to "1" when a STALL is returned or a packet error is detected during an OUT transaction.

2.2.3.4 0x23 EndpointB Interrupt Status (EPbIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x23	EPbIntStat	7:				00h
		6: EPbOUTShortACK	R(W)	0: None	1: OUT Short Packet ACK	
		5: EPbINTranAck	R(W)	0: None	1: IN Transaction ACK	
		4: EPbOUTTranACK	R(W)	0: None	1: OUT Transaction ACK	
		3: EPbINTranNAK	R(W)	0: None	1: IN Transaction NAK	
		2: EPbOUTTranNAK	R(W)	0: None	1: OUT Transaction NAK	
		1: EPbINTranErr	R(W)	0: None	1: IN Transaction Error	
		0: EPbOUTTranErr	R(W)	0: None	1: OUT Transaction Error	

Displays the interrupt status at endpointB. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 EPbOUTShortACK

Set to "1" when a short packet is received and an ACK is returned by an OUT transaction.

Bit5 EPbINTranAck

Set to "1" when an ACK is received by an IN transaction.

Bit4 EPbOUTTranACK

Set to "1" when an ACK is returned by an OUT transaction.

Bit3 EPbINTranNAK

Set to "1" when a NAK is returned by an IN transaction.

Bit2 EPbOUTTranNAK

Set to "1" when a NAK is returned to an OUT transaction.

Bit1 EPbINTranErr

Set to "1" when a STALL is returned, a packet error is detected or a handshake timeout occurs during an IN transaction.

Bit0 EPbOUTTranErr

Set to "1" when a STALL is returned or a packet error is detected during an OUT transaction.

2.2.3.5 0x24 EndpointC Interrupt Status (EPcIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x24	EPcIntStat	7:				00h
		6: EPcOUTShortACK	R(W)	0: None	1: OUT Short Packet ACK	
		5: EPcINTranAck	R(W)	0: None	1: IN Transaction ACK	
		4: EPcOUTTranACK	R(W)	0: None	1: OUT Transaction ACK	
		3: EPcINTranNAK	R(W)	0: None	1: IN Transaction NAK	
		2: EPcOUTTranNAK	R(W)	0: None	1: OUT Transaction NAK	
		1: EPcINTranErr	R(W)	0: None	1: IN Transaction Error	
		0: EPcOUTTranErr	R(W)	0: None	1: OUT Transaction Error	

Displays the interrupt status at endpointC. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 EPcOUTShortACK

Set to "1" when a short packet is received and an ACK is returned by an OUT transaction.

Bit5 EPcINTranAck

Set to "1" when an ACK is received by an IN transaction.

Bit4 EPcOUTTranACK

Set to "1" when an ACK is returned by an OUT transaction.

Bit3 EPcINTranNAK

Set to "1" when a NAK is returned by an IN transaction.

Bit2 EPcOUTTranNAK

Set to "1" when a NAK is returned to an OUT transaction.

Bit1 EPcINTranErr

Set to "1" when a STALL is returned, a packet error is detected or a handshake timeout occurs during an IN transaction.

Bit0 EPcOUTTranErr

Set to "1" when a STALL is returned or a packet error is detected during an OUT transaction.

2.2.3.6 0x25 EndpointD Interrupt Status (EPdIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x25	EPdIntStat	7:				00h
		6: EPdOUTShortACK	R(W)	0: None	1: OUT Short Packet ACK	
		5: EPdINTranAck	R(W)	0: None	1: IN Transaction ACK	
		4: EPdOUTTranACK	R(W)	0: None	1: OUT Transaction ACK	
		3: EPdINTranNAK	R(W)	0: None	1: IN Transaction NAK	
		2: EPdOUTTranNAK	R(W)	0: None	1: OUT Transaction NAK	
		1: EPdINTranErr	R(W)	0: None	1: IN Transaction Error	
		0: EPdOUTTranErr	R(W)	0: None	1: OUT Transaction Error	

Displays the interrupt status at endpointD. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 EPdOUTShortACK

Set to "1" when a short packet is received and an ACK is returned by an OUT transaction.

Bit5 EPdINTranAck

Set to "1" when an ACK is received by an IN transaction.

Bit4 EPdOUTTranACK

Set to "1" when an ACK is returned by an OUT transaction.

Bit3 EPdINTranNAK

Set to "1" when a NAK is returned by an IN transaction.

Bit2 EPdOUTTranNAK

Set to "1" when a NAK is returned to an OUT transaction.

Bit1 EPdINTranErr

Set to "1" when a STALL is returned, a packet error is detected or a handshake timeout occurs during an IN transaction.

Bit0 EPdOUTTranErr

Set to "1" when a STALL is returned or a packet error is detected during an OUT transaction.

2.2.3.7 0x26 EndpointE Interrupt Status (EPeIntStat)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x26	EPeIntStat	7:				00h
		6: EPeOUTShortACK	R(W)	0: None	1: OUT Short Packet ACK	
		5: EPeINTranAck	R(W)	0: None	1: IN Transaction ACK	
		4: EPeOUTTranACK	R(W)	0: None	1: OUT Transaction ACK	
		3: EPeINTranNAK	R(W)	0: None	1: IN Transaction NAK	
		2: EPeOUTTranNAK	R(W)	0: None	1: OUT Transaction NAK	
		1: EPeINTranErr	R(W)	0: None	1: IN Transaction Error	
		0: EPeOUTTranErr	R(W)	0: None	1: OUT Transaction Error	

Displays the interrupt status at endpointE. This register has bits directly indicating an interrupt cause.

When this register is set to "1," you can clear an interrupt cause by writing "1" to the relevant bit.

Bit7 Reserved

Bit6 EPeOUTShortACK

Set to "1" when a short packet is received and an ACK is returned by an OUT transaction.

Bit5 EPeINTranAck

Set to "1" when an ACK is received by an IN transaction.

Bit4 EPeOUTTranACK

Set to "1" when an ACK is returned by an OUT transaction.

Bit3 EPeINTranNAK

Set to "1" when a NAK is returned by an IN transaction.

Bit2 EPeOUTTranNAK

Set to "1" when a NAK is returned to an OUT transaction.

Bit1 EPeINTranErr

Set to "1" when a STALL is returned, a packet error is detected or a handshake timeout occurs during an IN transaction.

Bit0 EPeOUTTranErr

Set to "1" when a STALL is returned or a packet error is detected during an OUT transaction.

2.2.3.8 0x27 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x27	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.3.9 0x28 Endpoint0 Interrupt Enable (EP0IntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x28	EP0IntEnb	7:				00h
		6:				
		5: EnEP0INTranAck	R/W	0: Disable	1: Enable	
		4: EnEP0OUTTranACK	R/W	0: Disable	1: Enable	
		3: EnEP0INTranNAK	R/W	0: Disable	1: Enable	
		2: EnEP0OUTTranNAK	R/W	0: Disable	1: Enable	
		1: EnEP0INTranErr	R/W	0: Disable	1: Enable	
		0: EnEP0OUTTranErr	R/W	0: Disable	1: Enable	

Enables/disables an EP0IntStat register interrupt cause.

Set the relevant bit to “1” to transmit an EP0IntStat register interrupt cause to the EPIntStat register’s EP0IntStat bit.

2.2.3.10 0x29 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x29	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.3.11 0x2A EndpointA Interrupt Enable (EPaIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x2A	EPaIntEnb	7:				00h
		6: EnEPaOUTShortACK	R/W	0: Disable	1: Enable	
		5: EnEPaINTranAck	R/W	0: Disable	1: Enable	
		4: EnEPaOUTTranACK	R/W	0: Disable	1: Enable	
		3: EnEPaINTranNAK	R/W	0: Disable	1: Enable	
		2: EnEPaOUTTranNAK	R/W	0: Disable	1: Enable	
		1: EnEPaINTranErr	R/W	0: Disable	1: Enable	
		0: EnEPaOUTTranErr	R/W	0: Disable	1: Enable	

Enables/disables an EPaIntStat register interrupt cause.

Set the relevant bit to “1” to transmit an EPaIntStat register interrupt cause to the EPIntStat register’s EPaIntStat bit.

2.2.3.12 0x2B EndpointB Interrupt Enable (EPbIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x2B	EPbIntEnb	7:				00h
		6: EnEPbOUTShortACK	R/W	0: Disable	1: Enable	
		5: EnEPbINTranAck	R/W	0: Disable	1: Enable	
		4: EnEPbOUTTranACK	R/W	0: Disable	1: Enable	
		3: EnEPbINTranNAK	R/W	0: Disable	1: Enable	
		2: EnEPbOUTTranNAK	R/W	0: Disable	1: Enable	
		1: EnEPbINTranErr	R/W	0: Disable	1: Enable	
		0: EnEPbOUTTranErr	R/W	0: Disable	1: Enable	

Enables/disables an EPbIntStat register interrupt cause.

Set the relevant bit to “1” to transmit an EPbIntStat register interrupt cause to the EPIntStat register’s EPbIntStat bit.

2.2.3.13 0x2C EndpointC Interrupt Enable (EPcIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x2C	EPcIntEnb	7:				00h
		6: EnEPcOUTShortACK	R/W	0: Disable	1: Enable	
		5: EnEPcINTranAck	R/W	0: Disable	1: Enable	
		4: EnEPcOUTTranACK	R/W	0: Disable	1: Enable	
		3: EnEPcINTranNAK	R/W	0: Disable	1: Enable	
		2: EnEPcOUTTranNAK	R/W	0: Disable	1: Enable	
		1: EnEPcINTranErr	R/W	0: Disable	1: Enable	
		0: EnEPcOUTTranErr	R/W	0: Disable	1: Enable	

Enables/disables an EPcIntStat register interrupt cause.

Set the relevant bit to “1” to transmit an EPcIntStat register interrupt cause to the EPIntStat register’s EPcIntStat bit.

2.2.3.14 0x2D EndpointD Interrupt Enable (EPdIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x2D	EPdIntEnb	7:				00h
		6: EnEPdOUTShortACK	R/W	0: Disable	1: Enable	
		5: EnEPdINTranAck	R/W	0: Disable	1: Enable	
		4: EnEPdOUTTranACK	R/W	0: Disable	1: Enable	
		3: EnEPdINTranNAK	R/W	0: Disable	1: Enable	
		2: EnEPdOUTTranNAK	R/W	0: Disable	1: Enable	
		1: EnEPdINTranErr	R/W	0: Disable	1: Enable	
		0: EnEPdOUTTranErr	R/W	0: Disable	1: Enable	

Enables/disables an EPdIntStat register interrupt cause.

Set the relevant bit to “1” to transmit an EPdIntStat register interrupt cause to the EPIntStat register’s EPdIntStat bit.

2.2.3.15 0x2E EndpointE Interrupt Enable (EPeIntEnb)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x2E	EPeIntEnb	7:				00h
		6: EnEPeOUTShortACK	R/W	0: Disable	1: Enable	
		5: EnEPeINTranAck	R/W	0: Disable	1: Enable	
		4: EnEPeOUTTranACK	R/W	0: Disable	1: Enable	
		3: EnEPeINTranNAK	R/W	0: Disable	1: Enable	
		2: EnEPeOUTTranNAK	R/W	0: Disable	1: Enable	
		1: EnEPeINTranErr	R/W	0: Disable	1: Enable	
		0: EnEPeOUTTranErr	R/W	0: Disable	1: Enable	

Enables/disables an EPeIntStat register interrupt cause.

Set the relevant bit to “1” to transmit an EPeIntStat register interrupt cause to the EPIntStat register’s EPeIntStat bit.

2.2.3.16 0x2F (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x2F	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.4 Common Block

2.2.4.1 0x30 Macro Configuration (MacroConfig)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x30	MacroConfig	7:				00h
		6:				
		5:				
		4: COMPPwrDown	R/W	0:Normal	1: Internal 2.0V-comparator and 4.4V-comparator is powerdown	
		3:				
		2:				
		1:				
		0: ExtResMode	R/W	0: Use internal pull-up/pull down resistance	1: Use external pull-up/pull-down resistance	

Configures internal circuits.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 COMPPwrDown

This bit powers down the internal VBUS-2.0 V and VBUS-4.4 V comparators.

To minimize power consumption when the chip is inactive, set this register to 1.

0 – Operate normally

1 – Power down the VBUS-2.0 V and VBUS-4.4 V comparators

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 ExtResMode

Specifies whether to use the internal pullup/pulldown resistance.

0 - Uses the internal VBUS comparator.

1 - Uses an external pullup/pulldown resistance.

2.2.4.2 0x31 Revision Number (RevNumber)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x31	RevNumber	7: RevNumber[7]	R	RevisionNumber[7:0]	02h
		6: RevNumber[6]			
		5: RevNumber[5]			
		4: RevNumber[4]			
		3: RevNumber[3]			
		2: RevNumber[2]			
		1: RevNumber[1]			
		0: RevNumber[0]			

Bit7-0 RevNumber

Indicates the S1R72005's revision number.

These bits are enabled regardless of clock input conditions.

2.2.4.3 0x32 Common Control (CommonControl)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x32	CommonControl	7:				00h
		6:				
		5:				
		4: ResetXcvr	R/W	0: Normal	1: Transceiver Reset	
		3: ResetPC	R/W	0: Normal	1: PC Reset	
		2: ResetHC	R/W	0: Normal	1: HC Reset	
		1: ResetOTGC	R/W	0: Normal	1: OTGC Reset	
		0: ResetALL	R/W	0: Normal	1: ALL Reset	

Controls functions involving the entire S1R72005.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 ResetXcvr

You can reset the S1R72005 transceiver by setting this bit to "1." Clear this bit to "0" to exit reset.

0 - No operation (reset completed)

1 - Reset

Bit3 ResetPC

Resets the S1R72005 peripheral controller. Setting this bit to "1" initializes the following registers:

- HCPC_Common register
- PC_Control register
- PC_USBAddress register
- PC_FmNumber_H to L registers
- PipeEP_Common register
- EP_Common register
- EP0Setup_0 to 7 registers
- PC_IntStat register's RcvSOF field
- PC_IntEnb register's EnRcvSOF field

This bit is automatically cleared after initialization (for the F/W, it is not necessary to check that the bit is cleared due to reset completion).

0 - No operation (reset completed)

1 - Reset

Bit2 ResetHC

Resets the S1R72005 host controller. Setting this bit to “1” initializes the following registers:

- HC_IntStat.FmNumberOver
- HC_IntStat.SOF
- HC_IntEnb.FmNumberOver
- HC_IntEnb.SOF
- CommonControl.OpMode bit
- HCCommon register
- HCFmNumber register
- PIPE0Setup_0 to PIPE0Setup_7 registers

This bit is automatically cleared after initialization (for the F/W, it is not necessary to check that the bit is cleared due to reset completion).

0 - No operation (reset completed)

1 - Reset

Bit1 ResetOTGC

Resets the S1R72005 OTG controller. Setting this bit to “1” initializes the following registers:

- HCIntStat.FmNumberOver bit
- HCIntStat.SOF bit
- OTGCCommon register
- HCCommon.HCStateCmd bit
- HCFmNumber register

This bit is automatically cleared after initialization (for the F/W, it is not necessary to check that the bit is cleared due to reset completion).

0 - No operation (reset completed)

1 - Reset

Bit0 ResetALL

Resets the entire S1R72005.Setting this bit to “1” initializes the S1R72005 registers.

However, a read-only register or bit is not cleared by a reset.

This bit is automatically cleared after initialization (for the F/W, it is not necessary to check that the bit is cleared due to reset completion).

0 - No operation (reset completed)

1 - Reset

2.2.4.4 0x33 Host Controller & Peripheral Controller Common Control (HCPCCommon)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x33	HCPCCommon	7:				01h
		6:				
		5:				
		4:				
		3:				
		2: OpMode[2]	R	Operation Mode[2:0]		
		1: OpMode[1]	R			
		0: OpMode[0]	R			

This register controls functions common to both host and peripheral controllers.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2-0 OpMode [2:0]

Indicates the transceiver macro's operating mode.

In general, the firmware does not write a value to this bit.

000b - Normal operation

001b - Non-driving

010b - Disables bit stuffing and NRZI encoding (during peripheral operations)

011b - (Reserved)

100b - HostReset (when the host is operating)

101b - HostResume (when the host is operating)

110b - (Reserved)

111b - (Reserved)

2.2.4.5 0x34 OTG Controller Monitor (OTGCMonitor)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x34	OTGCMonitor	7: LSConnect	R	0: LS Device Not Connected	1: LS Device Connected	40h
		6: ID	R	0: Mini-A Inserted	1: Mini-A Not Inserted	
		5: LineState[1]	R	Line State[1:0]		
		4: LineState[0]	R			
		3:				
		2:				
		1: Comp20V	R	0: 2.0V or Under	1: Over 2.0V	
		0: Comp44V	R	0: Under 4.4V	1: 4.4V or Over	

Displays USB- and OTG-related USB port and VBUS states.

Bit7 LSConnect

Indicates whether a LOW-speed device is connected.

0 - No LOW-speed device is connected.

1 - A LOW-speed device is connected.

Bit6 ID

Indicates whether a mini A plug is inserted into the OTG receptacle (ID pin input condition). This bit is enabled regardless of clock input conditions.

0 - A mini A plug is inserted.

1 - No mini A plug is inserted.

Bit5-4 LineState [1:0]

Displays the signal status on the USB data line (the value received by the DP/DM's single-end receiver). These bits are enabled regardless of clock input conditions.

00b - SE0

01b - J

10b - K

11b - SE1

Bit3 Reserved

Bit2 Reserved

Bit1 Comp20V

Displays the output results of the VBUS 2.0V comparator. This bit is enabled regardless of clock input conditions.

0 - 2.0V or lower (≤ 2.0V)

1 - Higher than 2.0V (2.0V<)

Bit0 Comp44V

Displays the output results of the VBUS 4.4V comparator. This bit is enabled regardless of clock input conditions.

0 - Lower than 4.4V (< 4.4V)

1 - 4.4V or higher (4.4V≤)

2.2.4.6 0x35 OTG Controller Control (OTGCControl)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x35	OTGCControl	7: AllowRmtWkup	R/W	0: Do Not Allow Remote Wakeup	1: Allow Remote Wakeup	08h
		6:				
		5:				
		4: BusPwrSel	R/W	0: Limit 8mA	1: No Limit 8mA	
		3: OTGStateCmd[3]	R/W	OTG State Command[3:0]		
		2: OTGStateCmd[2]	R/W			
		1: OTGStateCmd[1]	R/W			
		0: OTGStateCmd[0]	R/W			

Controls the OTG controller.

Bit7 AllowRmtWkup

Setting determines whether the remote wakeup detection function is enabled or disabled during host operations.

0 - Disables remote wakeup detection function.

1 – Enables the remote wakeup detection function.

Bit6 Reserved

Bit5 Reserved

Bit4 BusPwrSel

Sets the VBUS output.

0 - Allows up to 8mA. (≤ 8mA)

1 - Allows over 8mA. (>8mA)

Bit3-0 OTGStateCmd [3:0]

Specifies the OTG controller operations. As the OTG state shifts, controller circuits, detection functions, etc. required in the state are automatically activated by writing an appropriate value to this bit.

0000b - "a_idle"

0001b - "a_wait_vrise"

0010b - "a_wait_bcon"

0011b - "a_host"

0100b - "a_suspend"

0101b - "a_peripheral"

0110b - "a_vbus_err"

0111b - "a_wait_vfall"

1000b - "b_idle"

1001b - "b_srp_init_d" *1 (data line pulsing)

1010b - "b_srp_init_v" (V_{BUS} pulsing)

1011b - "b_peripheral"

1100b - "b_wait_acon"

1101b - "b_host"

1110b - "b_srp_init_v5" *2 (5V-V_{BUS} pulsing)

1111b - No operation

*1 When the HV_{DD} supply voltage is 3.25V or less, use the E_OTGStateCmd register (0xE1) for SRP Data-line Pulsing. For discussions of usage, etc., see Paragraph 2.2.1.3.

*2 When using "b_srp_init_v5" during V_{BUS} pulsing, note that the V_{BUS} potential will increase up to 5.0V. In this state, the setting of this register's BusPwrSel bit is disabled.

2.2.4.7 0x36 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x36	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.4.8 0x37 Host Controller Control (HCControl)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x37	HCControl	7:				00h
		6:				
		5:				
		4: EnNoFmBulkMode	R/W	0: NoFrameBulkMode Disable	1: NoFrameBulkMode Enable	
		3:				
		2:				
		1: HCStateCmd[1]	R/W	HC State Command[1:0]		
		0: HCStateCmd[0]	R/W			

Controls functions involving the entire host controller.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 EnNoFmBulkMode

Enables/disables the bulk transfer mode without frame control.

Set this bit to "1" for bulk transfers without frame control or SOF issuance. This assigns bulk transactions for the entire USB bandwidth.

This mode is enabled during bulk or control transfer. No SOF token is issued if the TranGo bit is set to "1" for any channel. However, if the HCControl register's HCStateCmd bit is set to "11b" and the TranGo bits on all channels remain "0" for 3 ms or longer, an SOF token is issued to prevent a device from shifting to suspend state.

If isochronous or interrupt transfer is performed while this mode is being set, this bit is cleared, and the bulk transfer mode without frame control is automatically reset.

0 - Transfer in normal mode (normal USB transfer)

1 - Transfer in no frame bulk mode (bulk transfer without frame control)

(Note)

When the TranGo bit is set to "1" for any channel in this mode, no SOF is issued, even if transmission of an OUT or IN token is disabled due to a busy host FIFO, etc (no transaction state). Note that the connection target (peripheral) may shift to the suspend state if such conditions persist for 3 ms or longer.

Bit3 Reserved

Bit2 Reserved

Bit1-0 HCStateCmd [1:0]

Specifies how to send HC controller state signals. As the USB state shifts, signals required in the state can be sent or the required line state can be achieved by writing an appropriate value to this bit.

00b - The suspend state (J state) is attained on the USB signal line. ; "Suspend"

01b - Reset signals (SE0) are issued for the USB signal line. ; "Reset"

10b - The resume state (K state) is attained on the USB signal line. ; "Resume"

11b - SOF tokens are issued (USB transfer). ; "Operational"

When this field is set to "00b" (Suspend) and the remote wake-up is detected, this field automatically changes to "10b" (Resume).

2.2.4.9 0x38 Host Controller Frame Number HIGH (HCFmNumber_H)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x38	HCFmNumber_H	7:				00h
		6:				
		5:				
		4:				
		3:				
		2: HCFmNumber[10]	R	HCFrameNumber[10:8]		
		1: HCFmNumber[9]	R			
		0: HCFmNumber[8]	R			

Displays MSB 3 bits of the frame number counted by the host controller during host operations.

To obtain a frame number during 8-bit access, you must access this and HCFmNumber_L registers in pairs. Access this register first.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2-0 HCFmNumber_H [2:0]

MSB 3 bits of the frame number counted by the host controller are set.

2.2.4.10 0x39 Host Controller Frame Number LOW (HCFmNumber_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x39	HCFmNumber_L	7: HCFmNumber[7]	R	HCFrameNumber[7:0]	00h
		6: HCFmNumber[6]	R		
		5: HCFmNumber[5]	R		
		4: HCFmNumber[4]	R		
		3: HCFmNumber[3]	R		
		2: HCFmNumber[2]	R		
		1: HCFmNumber[1]	R		
		0: HCFmNumber[0]	R		

Displays LSB 8 bits of the frame number counted by the host controller during host operations.

To obtain a frame number during 8-bit access, you must access this and HCFmNumber_H registers in pairs. Access this register first.

Bit7-0 HCFmNumber_L [7:0]

LSB 8 bits of the frame number counted by the host controller are set.

2.2.4.11 0x3A Peripheral Controller Control (PCControl)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x3A	PCControl	7:				00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0: SendWakeup	R/W	0: Normal	1: Send RemoteWakeup Signal	

Controls functions involving the peripheral controller.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 SendWakeup

Set this bit to "1" to output a remote wakeup signal to the USB port (K state).

0 - Sends no remote wakeup signal.

1 - Sends remote wakeup signals.

Clear this bit to "0" to stop sending 1 ms or longer (15 ms Max.) after starting sending remote wakeup signals. Note that the system must have been restored from the suspend state (clocks are supplied to the peripheral controller) when you set this bit to "1."

2.2.4.12 0x3B Peripheral Controller USB Address (PCUSBAddress)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x3B	PCUSBAddress	7:			00h
		6: USBAddress[6]	R/W	USBAddress[6:0]	
		5: USBAddress[5]	R/W		
		4: USBAddress[4]	R/W		
		3: USBAddress[3]	R/W		
		2: USBAddress[2]	R/W		
		1: USBAddress[1]	R/W		
		0: USBAddress[0]	R/W		

Sets a USB address during peripheral controller operations.

Bit7 Reserved

Bit6-0 USBAddress [6:0]

Sets a USB address.

Set the address specified by the host after completion of the status stage of a SetAddress request.

0 to 127 - USB address

2.2.4.13 0x3C Peripheral Controller Frame Number HIGH (PCFmNumber_H)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x3C	PCFmNumber_H	7: FnInvalid	R	0: Frame Number Valid	1: Frame Number Invalid	80h
		6:				
		5:				
		4:				
		3:				
		2: PCFmNumber[10]	R	PCFmNumber[10:8]		
		1: PCFmNumber[9]	R			
		0: PCFmNumber[8]	R			

Accepts MSB 3 bits of the FrameNumber field of the SOF packet received during peripheral operations.

To obtain a frame number during 8-bit access, you must access this and PCFmNumber_L registers in pairs. Access this register first.

Bit7 FnInvalid

Set to "1" when an error occurs in the received SOF packet.

0 - Indicates that an SOF packet was received successfully.

1 - Indicates that an error occurred when an SOF packet was received.

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2-0 PCFmNumber_H [2:0]

MSB 3 bits of the FrameNumber field of the received SOF packet are set.

Note: To acquire the frame number at the time of a 16-bit access, read PCFmNumber (0x3C) twice. The value read the second time becomes the frame number.

2.2.4.14 0x3D Peripheral Controller Frame Number LOW (PCFmNumber_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x3D	PCFmNumber_L	7: PCFmNumber[7]	R	PCFmNumber[7:0]	00h
		6: PCFmNumber[6]	R		
		5: PCFmNumber[5]	R		
		4: PCFmNumber[4]	R		
		3: PCFmNumber[3]	R		
		2: PCFmNumber[2]	R		
		1: PCFmNumber[1]	R		
		0: PCFmNumber[0]	R		

Displays LSB 8 bits of the FrameNumber field of the SOF packet received during peripheral operations.

To obtain a frame number during 8-bit access, you must access this and PCFmNumber_H registers in pairs. Access this register first.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit7-0 PCFmNumber_L [7:0]

LSB 8 bits of the FrameNumber field of the received SOF packet are set.

Note: To acquire the frame number at the time of a 16-bit access, read PCFmNumber (0x3C) twice. The value read the second time becomes the frame number.

2.2.4.15 0x3E Pipe & EndpointCommon (PipeEPCommon)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x3E	PipeEPCommon	7:				00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0: SetBuffer	R/W	0: Normal	1: Starting Buffer Allocation	

This register controls functions common to both pipes and endpoints.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 SetBuffer

Setting this bit to "1" starts FIFO allocation to secure buffer areas for all pipes or endpoints where the buffer page counts and the maximum packet sizes have been set. This bit is automatically cleared to "0" after the buffer areas are secured.

0 - No operation

1 - Secures buffer areas.

Set this bit to secure buffer areas after setting the Config_0 register's BufferPage bit and the MaxPktSize_H/L registers of each pipe or endpoint. When this bit is set to "1," the read/write position pointers in all buffer areas are set at the beginning of the areas (identical state to when the Config register's FIFOClr bit in each channel is set to "1").

Note that transactions in/at all pipes or endpoints must be halted to set this bit to "1." In addition, be sure to start transactions when this bit is set to "0."

(Reference)

It takes about 125ns (48MHz, 6 clocks) to clear this bit to "0" when the bit is set to "1."

2.2.4.16 0x3F EndpointCommon (EPCommon)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x3F	EPCommon	7:				00h
		6:				
		5:				
		4:				
		3:				
		2: AutoEnShort	R/W	0: Disable AutEn Short	1: Enable AutoEn Short	
		1: AllForceNAK	W	0: Normal	1: ALL Force NAK	
		0: AllForceSTALL	W	0: Normal	1: EPr Force STALL	

Configures and displays functions involving all endpoints.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 AutoEnShort

Sets the operating mode of short packet transfers during IN transactions at an endpoint where the a to eConfig_0 register's JoinDMA bit is set to "1."

0 - If the data size after DMA transfer is smaller than the MaxPacketSize, no data is transferred from the FIFO until the EnShortPkt bit is set to "1."

1 - If the data size after DMA transfer is smaller than the MaxPacketSize, the Control_1 register's EnShortPkt bit at the relevant endpoint (EPa to e) is automatically set to "1" to transmit the remaining data. The EnShortPkt bit is cleared to "0" after the remaining data is sent.

The data count to be sent beforehand does not need to be checked and set.

Even for odd data counts, the EnShortPkt bit is set to "1" through automatic evaluation by the H/W.

Bit1 AllForceNAK

Set this bit to "1" to set the EP0Control_0 register's InForceNAK and OutForceNAK bits, as well as the Control_1 register's ForceNAK bit at all endpoints (EPa to e), to "1."

Bit0 AllForceSTALL

Set this bit to "1" to set the Control_1 register's ForceSTALL bit at all endpoints (EPa to e) to "1."

2.2.5 DMA/CPU/Clock Block

2.2.5.1 0x40 DMA Configuration0 (DMAConfig_0)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x40	DMAConfig_0	7: DINLatency[3]	R/W	DINLatency[3:0]	00h
		6: DINLatency[2]	R/W		
		5: DINLatency[1]	R/W		
		4: DINLatency[0]	R/W		
		3: DOUTLatency[3]	R/W	DOUTLatency[3:0]	
		2: DOUTLatency[2]	R/W		
		1: DOUTLatency[1]	R/W		
		0: DOUTLatency[0]	R/W		

Configures data capture/output timings by the DMA.

Bit7-4 DINLatency

Specifies the timing of data capture from external memory to the S1R72005 by the DMA (DMA IN: external memory → S1R72005).

The setting depends on the type of external memory to be connected.

<External memory = SDRAM>

Sets CAS latency.

0 to 15 - CAS latency

Following the falling edge of an xRD (xCAS) signal, data is captured into the S1R72005 at the rising edge of a DMASTRB after the duration set in this bit elapses.

<Others>

Sets the latency from an xDACK.

0 to 15 - Latency from an xDACK

Following the falling edge of an xDACK signal, data is captured into the S1R72005 at the rising edge of a DMASTRB after the duration set in this bit elapses.

Bit3-0 DOUTLatency

Specifies the timing of data output from the S1R72005 to an external memory by the DMA (DMA OUT: S1R72005 → external memory).

The setting depends on the type of external memory to be connected.

<External memory = SDRAM>

Sets the CAS latency.

0 to 15 - CAS latency

Following the falling edge of an xRD (xCAS) signal, data is output so that an SDRAM can capture it at the rising edge of a DMASTRB after the duration set in this bit elapses.

<Others>

Sets the latency from an xDACK.

0 to 15 - Latency from an xDACK

Following the falling edge of an xDACK signal, data is output so that an external memory can capture it at the rising edge of a DMASTRB after the duration set in this bit elapses.

2.2.5.2 0x41 DMA Configuration1 (DMAConfig_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x41	DMAConfig_1	7: ActiveDMA	R/W	0: Non-Active DMA	1: Active DMA	00h
		6: DMAClkPhase	R/W	0: Phase is not reversed	1: Phase is reversed	
		5: DMATranMode[1]	R/W	DMATranMode[1:0]		
		4: DMATranMode[0]	R/W			
		3: DREQLevel	R/W	0: Active Low	1: Active High	
		2: DMAEndian	R/W	0: DMA Big Endian	1: DMA Little Endian	
		1: StrobeMode	R/W	0: Not use xRD/xWR	1: Use xRD/xWR	
		0: DMABus8x16	R/W	0: DMA Bus 16bit Mode	1: DMA Bus 8bit Mode	

Configures functions involving DMA operations and bus.

Bit7 ActiveDMA

Although the DMA will be in pin input mode after a reset, the DMA can be re-enabled by setting this bit to "1."

0 - Disables the DMA.

1 - Enables the DMA.

Bit6 DMAClkPhase

Specifies how to invert the DMASTRB signal phase.

0 - Does not invert the DMASTRB phase.

This setting causes data to be handled at the rising edge of a DMASTRB.

1 - Inverses the DMASTRB phase.

This setting causes data to be handled at the falling edge of a DMASTRB.

Bit5-4 DMATranMode

Specifies the xDACK transfer mode.

This bit is enabled only if this register's StrobeMode bit is set to "0."

00b - (Disabled)

01b - An xDACK is used as a strobe for burst transfers.

With this setting, a number of xDACKs equal to the burst count is output from the S1R72005 to one xDREQ assert.

10b - Data is handled with xDACK + DMASTRB + xRD (xCAS).

This setting is compatible with SDRAM.

11b - Operation in general mode, where data is handled with xDACK + DMASTRB.

Bit3 DREQLevel

Determines the HDMARQ signal's operating level.

0 - Negative logic

1 - Positive logic

Bit2 DMAEndian

Sets big or little endian for the DMA used in 16-bit mode.

0 - MSB 8 bits of data are transferred to the USB first (big endian).

1 - LSB 8 bits of data are transferred to the USB first (little endian).

Bit1 StrobeMode

Specifies whether to use xRD/xWR signals during DMA transfer.

0 - DMA transfer without using xRD/xWR signals.

1 - DMA transfer using xRD/xWR signals.

When this bit is set to "1":

Data is captured at the rising edge of an xRD signal if the DMA transfer direction is "DMA IN" (external memory → S1R72005).

Or data is output so that external memory can capture data at the rising edge of an xWR signal if the DMA transfer direction is "DMA OUT" (S1R72005 → external memory).

Bit0 DMABus8x16

Set this bit to "1" to use the DMA bus in 8-bit mode.

0 - Uses the DMA bus in 16-bit mode.

1 - Uses the DMA bus in 8-bit mode.

2.2.5.3 0x42 DMA Control0 (DMAControl_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x42	DMAControl_0	7:				00h
		6: BurstFIFORemain	R	0: Does not remain	1: Remains	
		5:				
		4:				
		3:				
		2:				
		1: BurstLength[1]	R/W	BurstLength[1:0]		
		0: BurstLength[0]	R/W			

Controls DMA transfer.

Bit7 Reserved

Bit6 BurstFIFORemain

Indicates whether data remains in the local FIFO of the DMA block during DMA burst transfer.

0 - No data remains in the local FIFO.

1 - Data remains in the local FIFO.

Reference

During DMA OUT (S1R72005 → external memory) burst transfer:

If DMA transfer is completed before the count specified by the DMACountH to L registers becomes 0 (for example, if one transfer block is evaluated based on reception of a short packet during USB IN transfer for host operations or USB OUT transfer for peripheral operations) and if the last data is shorter (odd size) than the burst length specified by this register's BurstLength bit, the last odd-sized data transmitted remains stored in the DMA's local FIFO.

In this case, by writing the appropriate size of the data to stuff the burst length to the S1R72005's FIFO using the FIFOforCPU register in the relevant channel, the data in the DMA's local FIFO can be sent together with dummy data to an external memory to capture the last odd data.

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1-0 BurstLength

Sets the DMA burst length.

00b - 1 word
01b - 2 words
10b - 4 words
11b - 8 words

2.2.5.4 0x43 DMA Control1 (DMAControl_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x43	DMAControl_1	7: DMAAbort	W	0: Normal	1: DMA Transfer Abort	00h
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0: DMAGo	R/W	0: DMA Transfer Stop	1: DMA Transfer Start	

Controls DMA transfer.

Bit7 DMAAbort

Set this bit to "1" to abort DMA transfers triggered by the DMAControl_1 register's DMAGo bit.

0 - No operation

1 - Aborts DMA transfer.

In general, follow the recommended procedure given below to abort DMA transfers:

(1) Clear the DMAGo.

(2) Set the DMACount to "0."

(3) Clear the DMACmp interrupt.

(If the DMA is halted by clearing the DMAGo, the DMACmp will not perform an evaluation to determine whether the DMA has been halted.)

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 DMAGo

Set this bit to “1” to start DMA transfers.

DMA transfers can be halted by clearing this bit to “0” during DMA transfer. After DMA transfer is completed up to the byte count set in the DMACount_H to L registers, the MainIntStat register’s DMACmp bit is set to “1,” and this bit automatically reverts to “0.”The MainIntStat register’s DMACmp bit is also set to “1” when DMA transfer is halted using this bit.

0 - Stops DMA transfer.

1 - Starts DMA transfer.

Note 1: The following operations are required for DMA transfers:

1. Set the Config register’s JoinDMA bit at the relevant endpoint to “1.”
2. Set the byte count to be transferred in the DMACount register.
3. Set the DMAConfig register’s ActiveDMA bit to “1.”
4. Set the DMAGo to “1” to start DMA transfer.

(The order can change between 1 and 3 only.)

Note 2: Follow the recommended procedure below to abort DMA transfers:

1. Clear the DMAGo.
2. Set the DMACount to “0.”
3. Clear the DMACmp interrupt.

If the DMA is halted by clearing the DMAGo, the DMACmp will not perform an evaluation to determine whether the DMA has been halted.

To resume transfer after an abort, clear the FIFO and reset the DMACount.

Transfer cannot resume from the abort point.

2.2.5.5 0x44 (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x44	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.5.6 0x45 DMA Count HIGH (DMACount_H)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x45	DMACount_H	7: DMACount[23]	R/W	DMACount[23:16]	00h
		6: DMACount[22]	R/W		
		5: DMACount[21]	R/W		
		4: DMACount[20]	R/W		
		3: DMACount[19]	R/W		
		2: DMACount[18]	R/W		
		1: DMACount[17]	R/W		
		0: DMACount[16]	R/W		

2.2.5.7 0x46 DMA Count Middle (DMACount_M)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x46	DMACount_M	7: DMACount[15]	R/W	DMACount[15:8]	00h
		6: DMACount[14]	R/W		
		5: DMACount[13]	R/W		
		4: DMACount[12]	R/W		
		3: DMACount[11]	R/W		
		2: DMACount[10]	R/W		
		1: DMACount[9]	R/W		
		0: DMACount[8]	R/W		

2.2.5.8 0x47 DMA Count LOW (DMACount_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x47	DMACount_L	7: DMACount[7]	R/W	DMACount[7:0]	00h
		6: DMACount[6]	R/W		
		5: DMACount[5]	R/W		
		4: DMACount[4]	R/W		
		3: DMACount[3]	R/W		
		2: DMACount[2]	R/W		
		1: DMACount[1]	R/W		
		0: DMACount[0]	R/W		

DMACount_H

DMACount_M

DMACount_L

For the DMA transfer byte counts (16,777,215 bytes max., about 16.7 Mbytes), set bits 23 to 16 in the DMACount_H register, bits 15 to 8 in the DMACount_M register, and bits 7 to 0 in the DMACount_L register, respectively.

If transfer is started by the DMAControl_1 register's DMAGo bit, you can check the remaining count by reading this register.

The values in bits 7 to 0 (DMACount_L register) are fixed after reading bits 15 to 8 (DMACount_M register). However, counting continues inside the IC even after the readings are fixed.

Accordingly, access the DMACount_M, (DMACount_H) and DMACount_L registers in this order to read the remaining count during 8-bit register access. During 16-bit access, read LSB bits (bits 15 to 0) first, followed by the MSB bits (bits 23 to 16).

The MSB register need not be read if the count to be transferred does not reach it.

2.2.5.9 0x48 CPU Configuration0 (CPUConfig_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x48	CPUConfig_0	7:				00h
		6: WaitPortDisable	R/W	0: WAIT port enabled	1: WAIT port disabled	
		5: WaitMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		4: IntMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		3:				
		2: CPUEndian	R/W	0: CPU Big Endian	1: CPU Little Endian	
		1:				
		0: CPUBus8x16	R/W	0: CPU Bus 16bit Mode	1: CPU Bus 8bit Mode	

Configures functions involving the CPU interface.

Bit7 Reserved

Bit6 WaitPortDisable

Setting this bit to 1 disables the xWAIT pin function (i.e., port is accessed in fixed cycles).

If the LSI is used with this bit set to 1, insert the appropriate cycles in the CPU bus cycle to meet the AC timing requirements stipulated in the S1R72005#00A300 hardware specifications.

0 – Output xWAIT

1 – Do not output xWAIT

Bit5 WaitMode

Sets the xWAIT pin output mode.

0 - Sets the xWAIT output to “0/Hi-Z.”

1 - Sets the xWAIT output to “0/1.”

Bit4 IntMode

Sets the xINT pin output mode.

0 - Sets the xINT output to “0/Hi-Z.”

1 - Sets the xINT output to “0/1.”

Bit3 Reserved

Bit2 CPUEndian

Sets big or little endian for the CPU bus used in 16-bit mode.

The setting of this bit is linked to that of the CPUConfig_1 register’s CPUEndian bit. The CPU endian can be set using either of these register bits.

This bit is enabled regardless of clock input conditions.

0 - Supports big endian CPU access.

1 - Supports little endian CPU access.

Bit1 Reserved

Bit0 CPUBus8x16

Set this bit to “1” to use the CPU bus in 8-bit mode.

With this bit set to “1,” LSB 8 bits of the FIFOforCPU register in/at each pipe or endpoint are enabled, and MSB 8 bits are disabled.

The setting of this bit is linked to that of the CPUConfig_1 register’s CPUBus8x16 bit.The width of the CPU bus can be set using either of these register bits.

0 - Uses the CPU bus in 16-bit mode.

1 - Uses the CPU bus in 8-bit mode.

2.2.5.10 0x49 CPU Configuration1 (CPUConfig_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x49	CPUConfig_1	7:				00h
		6: WaitPortDisable	R/W	0: WAIT port enabled	1: WAIT port disabled	
		5: WaitMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		4: IntMode	R/W	0: Hi-Z - 0 Mode	1: 1 - 0 Mode	
		3:				
		2: CPUEndian	R/W	0: CPU Big Endian	1: CPU Little Endian	
		1:				
		0: CPUBus8x16	R/W	0: CPU Bus 16bit Mode	1: CPU Bus 8bit Mode	

Configures functions involving the CPU interface.

Bit7 Reserved

Bit6 WaitPortDisable

Setting this bit to 1 disables the xWAIT pin function (i.e., port is accessed in fixed cycles).

If the LSI is used with this bit set to 1, insert the appropriate cycles in the CPU bus cycle to meet the AC timing requirements stipulated in the S1R72005#00A300 hardware specifications.

0 – Output xWAIT

1 – Do not output xWAIT

Bit5 WaitMode

This bit sets xWAIT pin output mode.

0 – xWAIT output in 0/Hi-Z mode

1 – xWAIT output in 0/1 mode

Bit4 IntMode

This bit sets xINT pin output mode.

0 – xINT output in 0/Hi-Z mode

1 – xINT output in 0/1 mode

Bit3 Reserved

Bit2 CPUEndian

Sets big or little endian for the CPU bus used in 16-bit mode.

The setting of this bit is linked to that of the CPUConfig_0 register's CPUEndian bit. The CPU endian can be set using either of these register bits.

This bit is enabled regardless of clock input conditions.

0 - Supports big endian CPU access.

1 - Supports little endian CPU access.

Bit1 Reserved

Bit0 CPUBus8x16

Set this bit to “1” to use the CPU bus in 8-bit mode.

With this bit set to “1,” LSB 8 bits of the FIFOforCPU register in/at each pipe or endpoint are enabled, and MSB 8 bits are disabled.

The setting of this bit is linked to that of the CPUConfig_0 register’s CPUBus8x16 bit. The width of the CPU bus can be set using either of these register bits.

0 - Uses the CPU bus in 16-bit mode.

1 - Uses the CPU bus in 8-bit mode.

2.2.5.11 0x4A Clock Monitor (ClkMonitor)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x4A	ClkMonitor	7:				0Fh
		6:				
		5:				
		4:				
		3: CPUClkActive	R	0: CPU Clock Non-Active	1: CPU Clock Active	
		2: PLLClkActive	R	0: PLL Clock Non-Active	1: PLL Clock Active	
		1: EnPLL	R	0: PLL Disable	1: PLL Enable	
		0: EnOSC	R	0: OSC Disable	1: OSC Enable	

Monitors clock control of S1R72005 internal circuits.

This register can be referenced regardless of clock input conditions.

All clocks are enabled after resets (clocks stabilize during resets).

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 CPUClkActive

Indicates whether clocks are supplied to the CPU Interface and OTG controller (OTGC).

0 - CPU Interface and OTGC clocks are disabled (deactivated).

1 - CPU Interface and OTGC clocks are enabled (activated).

This bit is set to “1” after resetting. If the CPU Interface and OTGC are set to wakeup mode by the ClkCommand register, this bit is also set to “1” after the elapsing of the interval set in the ClkControl register’s OSCWakeupTime and PLLWakeupTime fields to enable clocks.

Bit2 PLLClkActive

Indicates whether clocks output by the PLL are enabled.

0 - PLL clocks are disabled (deactivated).

1 - PLL clocks are enabled (activated).

This bit is set to “1” after resetting. If the PLL is set to wakeup mode by the ClkCommand register, this bit is also set to “1” after the elapsing of the interval set in the ClkControl register’s OSCWakeupTime and PLLWakeupTime fields to enable PLL clocks.

Bit1 EnPLL

Indicates whether the PLL circuit is enabled.

0 - The PLL circuit is disabled.

1 - The PLL circuit is enabled.

This bit is set to “1” after resetting. If the PLL is set in sleep/wakeup mode using the ClkCommand register, this bit changes accordingly.

Bit0 EnOSC

Indicates whether the oscillator is enabled.

0 - The oscillator is disabled.

1 - The oscillator is enabled.

This bit is set to “1” after resetting. If the oscillator is set in sleep/wakeup mode using the ClkCommand register, this bit changes accordingly.

2.2.5.12 0x4B Clock Control (ClkControl)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x4B	ClkControl	7: OSCWakeupTime[1]	R/W	OSCWakeupTime[1:0]		00h
		6: OSCWakeupTime[0]	R/W			
		5: PLLWakeupTime[1]	R/W	PLLWakeupTime[1:0]		
		4: PLLWakeupTime[0]	R/W			
		3: HCSleep	R/W	0: HC Wake	1: HC Sleep	
		2: PCSleep	R/W	0: PC Wake	1: PC Sleep	
		1: MainSleep	R/W	0: Main Wake	1: Main Sleep	
		0: XcvrSleep	R/W	0: Transceiver Wake	1: Transceiver Sleep	

Controls functions involving S1R72005 internal circuit clocks.

- PLL and oscillator timers can be set independently.
- The wakeup timer does not function in the mode in which 48 MHz is directly input from an external source (but clock output to each block can be halted).

Bit7-6 OSCWakeupTime [1:0]

Sets the wait time until oscillator pulses stabilize.

00b - 2.5ms

01b - 5ms

10b - 10ms

11b - Reserved

This timer is active if the oscillator is explicitly set to sleep mode by the CPU (firmware), then resumed from that state. If the oscillator is started by a chip reset, the timer set using this bit will not activate immediately after the reset, since clocks stabilize within the reset period.

Bit5-4 PLLWakeupTime [1:0]

Sets the wait time until PLL output pulses stabilize.

00b - 0.15ms

01b - 0.3ms

10b - 0.6ms

11b - 1.2ms

This timer activates if the PLL is explicitly set to sleep mode by the CPU (firmware), then resumed from that state. If PLL operation is started by a chip reset, the timer set using this bit does not function immediately after the reset, since clocks stabilize within the reset period.

Bit3 HCSleep

Controls clock supply to the HC block.

Set this bit to “1” to stop clock supply to the HC block, setting it to sleep state.

0 - Supplies clocks to the HC block.

1 - Stops clock supply to the HC block.

Bit2 PCSleep

Controls clock supply to the PC block.

Set this bit to “1” to stop clock supply to the PC block, setting it to sleep state.

0 - Supplies clocks to the PC block.

1 - Stops clock supply to the PC block.

Bit1 MainSleep

Controls clock supply to the FIFO core, pipes/endpoints, control register block, and DMA handler.

Set this bit to “1” to stop clock supply to these blocks, setting them to sleep state.

0 - Supplies clocks to the FIFO core, pipes/endpoints, control register block, and DMA handler.

1 - Stops clock supply to the FIFO core, pipes/endpoints, control register block, and DMA handler.

Bit0 XcvrSleep

Controls clock supply to the transceiver.

Set this bit to “1” to stop clock supply to the transceiver, setting it to sleep state.

0 - Supplies clocks to the transceiver.

1 - Stops clock supply to the transceiver.

2.2.5.13 0x4C (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x4C	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.5.14 0x4D Clock Command (ClkCommand)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x4D	ClkCommand	7: ClkCommand[7]	W	ClkCommand[7:0]	00h
		6: ClkCommand[6]	W		
		5: ClkCommand[5]	W		
		4: ClkCommand[4]	W		
		3: ClkCommand[3]	W		
		2: ClkCommand[2]	W		
		1: ClkCommand[1]	W		
		0: ClkCommand[0]	W		

Controls functions involving S1R72005 internal circuit clocks.

The setting of this register is enabled regardless of clock input conditions.

Bit7-0 ClkCommand [7:0]

Controls the oscillator and PLL as well as clock supply to the CPU Interface, OTGC, and HC/PC Common blocks.

55h - Sets the oscillator to wakeup mode.

AAh - Sets the oscillator to sleep mode.

3Ch - Sets the PLL to wakeup mode.

C3h - Sets the PLL to sleep mode.

69h - Sets the CPU Interface, OTGC, and HC/PC Common blocks to wakeup mode.

96h - Sets the CPU Interface, OTGC, and HC/PC Common blocks to sleep mode.

Only the PLL can be halted when the oscillator is operating. Accordingly, the resume time consists of the PLL wakeup time only.

2.2.5.15 0x4E (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x4E	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.5.16 0x4F (Reserved)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x4F	(Reserved)	7:				unfixed
		6:				
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

2.2.6 Control Transfer Command Register Block

2.2.6.1 0x50 to 0x57 Pipe0 Setup Command0 to 7 (PIPE0Setup_0 to PIPE0Setup_7)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x50 to 0x57	PIPE0Setup_0 to PIPE0Setup_7	7: PIPE0Setup_n[7]	R/W	PIPE0Setup_n [7 to 0]	00h
		6: PIPE0Setup_n[6]	R/W		
		5: PIPE0Setup_n[5]	R/W		
		4: PIPE0Setup_n[4]	R/W		
		3: PIPE0Setup_n[3]	R/W		
		2: PIPE0Setup_n[2]	R/W		
		1: PIPE0Setup_n[1]	R/W		
		0: PIPE0Setup_n[0]	R/W		

A device request (8 bytes) is set in this register to conduct control transfer in auto mode (set the PIPE0CTLAutoMode register's EnAutoMode bit to "1"). The set device request is sent to a device as a data packet at the setup stage after a transaction begins.

Regardless of the S1R72005 endian setting, the PIPE0Setup_0 to PIPE0Setup_7 data are issued for the USB, starting with the PIPE0Setup_0 data.

This register setting is not required for manual control transfer (normal mode).

PIPE0Setup_0

Sets the bmRequestType.

PIPE0Setup_1

Sets the bRequest.

PIPE0Setup_2

Sets LSB 8 bits of the wValue.

PIPE0Setup_3

Sets MSB 8 bits of the wValue.

PIPE0Setup_4

Sets LSB 8 bits of the wIndex.

PIPE0Setup_5

Sets MSB 8 bits of the wIndex.

PIPE0Setup_6

Sets LSB 8 bits of the wLength.

PIPE0Setup_7

Sets MSB 8 bits of the wLength.

2.2.6.2 0x58 to 0x5F Endpoint0 Setup0 to 7 (EP0Setup_0 to EP0Setup_7)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x58 to 0x5F	EP0Setup_0 to EP0Setup_7	7: EP0Setup_n[7]	R	EP0Setup_n [7 to 0]	00h
		6: EP0Setup_n[6]	R		
		5: EP0Setup_n[5]	R		
		4: EP0Setup_n[4]	R		
		3: EP0Setup_n[3]	R		
		2: EP0Setup_n[2]	R		
		1: EP0Setup_n[1]	R		
		0: EP0Setup_n[0]	R		

Stores the device request data received at the setup stage at endpoint0.

Regardless of the S1R72005 endian setting, data is stored in the order received, sequentially from EP0Setup_0 to EP0Setup_7.

EP0Setup_0

Sets the bmRequestType.

EP0Setup_1

Sets the bRequest.

EP0Setup_2

Sets LSB 8 bits of the wValue.

EP0Setup_3

Sets MSB 8 bits of the wValue.

EP0Setup_4

Sets LSB 8 bits of the wIndex.

EP0Setup_5

Sets MSB 8 bits of the wIndex.

EP0Setup_6

Sets LSB 8 bits of the wLength.

EP0Setup_7

Sets MSB 8 bits of the wLength.

2.2.7 Channel0 Control Register Block

2.2.7.1 0x60 Channel0 Configuration0 (0Config_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x60	0Config_0	7: JoinDMA	R/W	0: Not Joint to DMA	1: Joint to DMA	00h
		6: FIFOClr	W	0: Normal	1: FIFO Clear	
		5:				
		4:				
		3:				
		2:				
		1:				
		0:				

Sets the basic configuration of channel0 during host operations or endpoint0 during peripheral operations.

Bit7 JoinDMA

Connects this channel or endpoint to the DMA.

The DMA is connected to the channel or endpoint at which this bit is set to "1" most recently.

0 - Does not connect this channel or endpoint to the DMA.

1 - Connect this channel or endpoint to the DMA.

Bit6 FIFOClr

Set this bit to "1" to return the FIFO read/write pointer of this channel or endpoint to the beginning.

After the FIFO is cleared, this bit is automatically cleared to "0."

0 - No operation (clear completed)

1 - Returns the FIFO read/write pointer of this channel or endpoint to the beginning.

While a transaction is suspended during host operations, be sure to clear the FIFO using this bit if you want to start a new transfer to this channel, rather than resuming the halted transfer.

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 Reserved

2.2.7.2 0x61 Channel0 Configuration1 (0Config_1)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x61	0Config_1	7: DirPID[1]	R/W	DirPID[1:0]	00h
		6: DirPID[0]	R/W		
		5:			
		4:			
		3: EPNumber[3]	R/W	EPNumber[3:0]	
		2: EPNumber[2]	R/W		
		1: EPNumber[1]	R/W		
		0: EPNumber[0]	R/W		

Sets the basic configuration of channel 0 during host operations or endpoint 0 during peripheral operations.

Bit7-6 DirPID [1:0]

During host operations

Sets the type of tokens (OUT, IN or SETUP) issued by channel0. The setting of this bit is disabled if the PIPE0CTLAutoMode register's EnCTLAuto bit is set to "1."

00b - Issues OUT tokens.

01b - Issues SETUP tokens.

10b - Issues IN tokens.

11b - (Reserved)

During peripheral operation

Sets the transfer direction at endpoint 0.

00b - OUT direction

01b - (Reserved)

10b - IN direction

11b - (Reserved)

During peripheral operations:

For control transfer, assess the device request received at the setup stage and set this bit for each subsequent stage.

If a token in a different direction from this bit's setting is received, the peripheral controller does not return a handshake (no reply).

Bit5 Reserved

Bit4 Reserved

Bit3-0 EPNumber [3:0]

Sets the endpoint number used for transfer in channel 0 during host operations or the endpoint number (0) to be controlled by this register block during peripheral operations.

0d to 15d - Any endpoint number

Note: Only number 0 can be set during peripheral operations.

2.2.7.3 0x62 Channel0 Max Packet Size HIGH (0MaxPktSize_H)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x62	0MaxPktSize_H	7:				00h
		6: BufferPage[4]	R/W	BufferPage[4:0]		
		5: BufferPage[3]	R/W			
		4: BufferPage[2]	R/W			
		3: BufferPage[1]	R/W			
		2: BufferPage[0]	R/W			
		1:				
		0:				

Sets the buffer area page count of channel 0 during host operations or endpoint 0 during peripheral operations.

Bit7 Reserved

Bit6-2 BufferPage [4:0]

Specifies the FIFO area's buffer page count of this channel or endpoint.

0 - Disabled

1 to 31 - Any buffer page count

The size set by the 0MaxPktSize register represents one buffer page. Accordingly, 0MaxPktSize × BufferPage (this bit) is secured as the buffer area size. The total size of the FIFO area is 2.5 Kbytes. Consider the buffer size secured by other channels or endpoints when setting this bit.

Note: Do not set this field except during SetBuffer execution.

Bit1 Reserved

Bit0 Reserved

2.2.7.4 0x63 Channel0 Max Packet Size LOW (0MaxPktSize_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x63	0MaxPktSize_L	7:			00h
		6: MaxPktSize[6]	R/W	MaxPacketSize [6:0]	
		5: MaxPktSize[5]	R/W		
		4: MaxPktSize[4]	R/W		
		3: MaxPktSize[3]	R/W		
		2: MaxPktSize[2]	R/W		
		1: MaxPktSize[1]	R/W		
		0: MaxPktSize[0]	R/W		

Sets the maximum packet size of channel 0 during host operations or endpoint 0 during peripheral operations.

Bit7 Reserved

Bit6-0 MaxPktSize [6:0]

Sets the maximum byte count for the packet size that the relevant endpoint can send or receive.

Select from 8, 16, 32, and 64 bytes.

0 - (Disabled)

8 to 64 - Byte count for maximum packet size

Note: Do not set this field except during SetBuffer execution.

2.2.7.5 0x64 Pipe0 Control Transfer Auto Mode (PIPE0CTLAutoMode)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x64	PIPE0CTLAutoMode	7:				00h
		6:				
		5:				
		4:				
		3:				
		2: DataStageDir	R/W	0: OUT	1: IN	
		1: NoDataStage	R/W	0: DataStatge Exist	1: DataStage Not Exist	
		0: EnCTLAuto	R/W	0: Auto Stage Sequence Disable	1: Auto Stage Sequence Enable	

Sets functions involving the auto stage sequence for control transfer during host operations.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 DataStageDir

Specifies the transaction direction of the data stage. This bit is enabled only if this register's EnCTLAuto bit is set to "1" and the NoDataStage bit at "0."

0 - OUT transaction

1 - IN transaction

Bit1 NoDataStage

Specifies whether or not the data stage exists. This bit is enabled only if this register's EnCTLAuto bit is set to "1."

0 - The data stage exists.

1 - No data stage exists.

Bit0 EnCTLAuto

Set this bit to “1” to automatically sequence control transfer stages.

0 - No stage sequence

1 - Automatic stage sequence

If a transaction starts by setting this bit to “1” and the PIPE0Control register’s TranGo bit accordingly, the setup, (data), and status stages are automatically sequenced.

At the setup stage, a SETUP token is automatically issued to send the request set in the PIPE0Setup_0 to PIPE0Setup_7 registers.

If the data stage follows, a transaction is automatically executed in the specified direction and with the specified size.

Finally, at the status stage, an appropriate PID token is automatically issued based on the existence and direction of the data stage to send and receive a zero-length packet.

The PIPE0IntStat register’s CTLTranCmp bit is set after the above transaction and stage sequence are completed. If a packet error is detected or a STALL is returned by a device during the sequence, the PIPE0IntStat register’s relevant bit is set to halt the transaction.

2.2.7.6 0x65 Pipe0 Transfer Configuration (PIPE0TranConfig)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x65	PIPE0TranConfig	7:			00h
		6: Continuity[2]	R/W	Continuity[2:0]	
		5: Continuity[1]	R/W		
		4: Continuity[0]	R/W		
		3:			
		2: FuncAddr[2]	R/W	FunctionAddress[2:0]	
		1: FuncAddr[1]	R/W		
		0: FuncAddr[0]	R/W		

Sets basic transfer functions involving channel0 during host operations.

Bit7 Reserved

Bit6-4 Continuity [2:0]

Specifies the continuous execution count (priority) of transactions on this channel for host controller scheduling.

This bit cannot be set to "0".

For host controller scheduling, continuous execution continues to be counted across frames. Although the count includes retransmission due to packet errors, retransmission following an NAK does not depend on the setting of this bit.

0 - Continuous transaction execution count = 8 (Max.)

1 to 7 - Continuous transaction execution count

Bit3 Reserved

Bit2-0 FuncAddr [2:0]

Sets the USB address of the function, including the endpoint controlled by this channel.

0 to 7 - Function address

2.2.7.7 0x66 Pipe0 Control (PIPE0Control)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x66	PIPE0Control	7:				00h
		6:				
		5:				
		4: Toggle	R/W	0: Toggle 0	1: Toggle 1	
		3:				
		2:				
		1:				
		0: TranGo	R/W	0: Standby	1: Transaction Start	

Controls functions involving channel 0 during host operations.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Toggle

Sets the default value for the toggle sequence bit when a transaction starts. This bit also indicates the toggle sequence bit state after a transaction is executed and completed.

0 - Toggle 0

1 - Toggle 1

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 TranGo

Set this bit to “1” to start a transaction on channel 0. The transaction started can be halted by clearing this bit to “0.” This bit also indicates whether a transaction is underway on channel 0.

0 - Stops a transaction.

1 - Starts a transaction (or a transaction is underway).

If this bit is set to “1” when the PIPE0CTLAutoMode register’s EnCTLAuto bit is set to “1,” a transaction and the stage sequence begin.

After completion of the transfer up to the byte count set in the PIPE0TotalSize_H to L registers, the PIPE0IntStat register’s PIPE0TranCmp bit is set to “1,” and this bit automatically reverts to “0.” This bit is also reset to “0” if the PIPE0IntStat register’s InShortRcv, InOverSize, TranErr, Stalled or NoResp bit, or the HCIntStat register’s PortErr bit is set.

If clearing this bit halts a transaction, the PIPE0IntStat register’s relevant bit is set when the current transaction is completed.

The data in the FIFO, the (remaining) total size, and settings for the channel remain unchanged even after a transaction is halted. Reset this bit to “1” to resume a transaction from the point halted.

To start a new transaction, clear the FIFO and reset channel information.

2.2.7.8 0x67 Pipe0 Total Size HIGH (PIPE0TotalSize_H)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x67	PIPE0TotalSize_H	7: TotalSize[23]	R/W	TotalSize[23:16]	00h
		6: TotalSize[22]	R/W		
		5: TotalSize[21]	R/W		
		4: TotalSize[20]	R/W		
		3: TotalSize[19]	R/W		
		2: TotalSize[18]	R/W		
		1: TotalSize[17]	R/W		
		0: TotalSize[16]	R/W		

2.2.7.9 0x68 Pipe0 Total Size Middle (PIPE0TotalSize_M)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x68	PIPE0TotalSize_M	7: TotalSize[15]	R/W	TotalSize[15:8]	00h
		6: TotalSize[14]	R/W		
		5: TotalSize[13]	R/W		
		4: TotalSize[12]	R/W		
		3: TotalSize[11]	R/W		
		2: TotalSize[10]	R/W		
		1: TotalSize[9]	R/W		
		0: TotalSize[8]	R/W		

2.2.7.10 0x69 Pipe0 Total Size LOW (PIPE0TotalSize_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x69	PIPE0TotalSize_L	7: TotalSize[7]	R/W	TotalSize[7:0]	00h
		6: TotalSize[6]	R/W		
		5: TotalSize[5]	R/W		
		4: TotalSize[4]	R/W		
		3: TotalSize[3]	R/W		
		2: TotalSize[2]	R/W		
		1: TotalSize[1]	R/W		
		0: TotalSize[0]	R/W		

PIPE0TotaSize_H

PIPE0TotalSize_M

PIPE0TotalSize_L

For the total byte count for the transfer data on channel0 (16,777,214 bytes Max.: about 16.4 Mbytes), set bits 23 to 16 in the PIPE0TotalSize_H register, bits 15 to 8 in the PIPE0TotalSize_M register, and bits 7 to 0 in the PIPE0TotalSize_L register.

Set the size of the data packet to be transferred (or received) at the data stage in this bit if the PIPE0CTLAutoMode register's EnCTLAuto and NoDataStage bits are set to "1" and "0," respectively.

If a transaction starts by the PIPE0Control register's TranGo bit, you can check the remaining count by reading this register.

The values for bits 7 to 0 (PIPE0TotalSize_L register) are fixed after reading bits 15 to 8 (PIPE0TotalSize_M register). However, counting continues inside the IC, even after the readings are fixed.

Accordingly, access the PIPE0TotalSize_M, (PIPE0TotalSize_H) and PIPE0TotalSize_L registers in this sequence to read the remaining count during 8-bit register access. During 16-bit access, first read the LSB bits (bits 15 to 0), then the MSB bits (bits 23 to 16).

The MSB register need not be read if the count to be transferred does not reach it the value set therein.

A zero-length packet is sent after an OUT transaction is executed with the TotalSize set to "0." If an OUT or IN transaction is executed with the TotalSize set to "0xFFFFFF," the total size is not limited and is not counted. In this case, neither the PIPE0IntStat register TranCmp nor CTLTranCmp bit is set.

2.2.7.11 0x6A Endpoint0 Control0 (EP0Control_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x6A	EP0Control_0	7:				00h
		6: AutoForceNAK	R/W	0: Normal	1: Auto Force NAK	
		5: InEnShortPkt	R/W	0: Normal	1: Send Short Packet	
		4:				
		3: InForceNAK	R/W	0: Normal	1: In Force NAK	
		2: InForceSTALL	R/W	0: Normal	1: In Force STALL	
		1: OutForceNAK	R/W	0: Normal	1: Out Force NAK	
		0: OutForceSTALL	R/W	0: Normal	1: Out Force STALL	

Configures operations at endpoint 0 during peripheral operations.

Bit7 Reserved

Bit6 AutoForceNAK

*The function of this bit has problem.

please see the chapter 3.2 of this document.

Automatically sets the EP0Control_0 register InForceNAK or OutForceNAK bit to "1" when a transaction is successfully completed at endpoint 0.

0 - Does not automatically set the InForceNAK or OutForceNAK bit.

1 - Automatically sets the InForceNAK or OutForceNAK bit.

This bit is used to halt each transaction, apart from other transactions.

Bit5 InEnShortPkt

Set this bit to "1" to enable the current data in the FIFO to be sent as short packets, even if the data count in the FIFO does not reach the maximum packet size for an IN transaction at endpoint 0. After transmission of a short packet is completed, this bit is automatically cleared to "0." A zero-length packet is sent if this bit is set to "1" when there is no data in the FIFO.

0 - No operation

1 - Sends the current data in the FIFO.

Bit4 Reserved

Bit3 InForceNAK

Set this bit to "1" to return an NAK to an IN transaction, regardless of the data count in the FIFO.

In addition, this bit is automatically set to "1" if the MainIntStat_0 register's RcvEP0Setup bit is set to "1" when the setup stage is completed. Do not clear this bit to "0" when the MainIntStat_0 register's RcvEP0Setup bit is set to "1."

If the transfer direction of the data stage is "IN," the data stage can be executed by setting the 0Config_1 register's DirPID bit to the IN direction and clearing this bit to "0."

If the transfer direction of the data stage is "OUT," the status stage can be executed by

clearing this bit to “0” when the stage is ready to be executed.

If this bit is set during a transaction, the setting will apply only for the next transaction and thereafter.

0 - No operation

1 - Returns an NAK to an IN transaction.

Bit2 InForceSTALL

Set this bit to "1" to return a STALL to an IN transaction. This bit setting precedes that of the InForceNAK bit. In addition, this bit is set to "0" if the MainIntStat_0 register's RcvEP0Setup bit is set to "1" when the setup stage is completed. Do not set this bit to "1" when the MainIntStat_0 register's RcvEP0Setup bit is set to "1."

If this bit is set during a transaction, the setting will apply only for the next transaction and thereafter.

0 - No operation

1 - Returns a STALL to an IN transaction.

Bit1 OutForceNAK

Set this bit to "1" to return an NAK to an OUT transaction, regardless of the data count in the FIFO.

In addition, this bit is automatically set to "1" if the MainIntStat_0 register's RcvEP0Setup bit is set to "1" when the setup stage is completed. Do not clear this bit to "0" when the MainIntStat_0 register's RcvEP0Setup bit is set to "1."

If the transfer direction of the data stage is "OUT," the data stage can be executed by setting the 0Config_1 register's DirPID bit to the OUT direction and clearing this bit to "0."

If the transfer direction of the data stage is "IN," the status stage can be executed by clearing this bit to "0" when the stage is ready to be executed.

If this bit is set during a transaction, the setting will apply only for the next transaction and thereafter.

0 - No operation

1 - Returns an NAK to an OUT transaction.

Bit0 OutForceSTALL

Set this bit to "1" to return a STALL to an OUT transaction. This bit setting precedes that of the OutForceNAK bit.

In addition, this bit is set to "0" if the MainIntStat_0 register's RcvEP0Setup bit is set to "1" when the setup stage is completed. Do not set this bit to "1" when the MainIntStat_0 register's RcvEP0Setup bit is set to "1."

If this bit is set during a transaction, the setting will apply only for the next transaction and thereafter.

0 - No operation

1 - Returns a STALL to an OUT transaction.

2.2.7.12 0x6B Endpoint0 Control1 (EP0Control_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x6B	EP0Control_1	7: InToggleStat	R	0: In Transaction Toggle 0	1: In Transaction Toggle 1	00h
		6:				
		5: InToggleSet	W	0: Normal	1: In Transaction Toggle Set	
		4: InToggleClr	W	0: Normal	1: InTransaction Toggle Clear	
		3: OutToggleStat	R	0: Out Transaction Toggle 0	1: Out Transaction Toggle 1	
		2:				
		1: OutToggleSet	W	0: Normal	1: Out Transaction Toggle Set	
		0: OutToggleClr	W	0: Normal	1: Out Transaction Toggle Clear	

Configures operations at endpoint 0 during peripheral operations.

Bit7 InToggleStat

Indicates the toggle sequence bit state during an IN transaction.

0 - Toggle 0 (IN transaction)

1 - Toggle 1 (IN transaction)

Bit6 Reserved

Bit5 InToggleSet

Set this bit to "1" to set the toggle sequence bit of an IN transaction to "1."

0 - No operation

1 - Toggle 1 (IN transaction)

Bit4 InToggleClr

Set this bit to "1" to set the toggle sequence bit of an IN transaction to "0."

0 - No operation

1 - Toggle 0 (IN transaction)

Bit3 OutToggleStat

Indicates the toggle sequence bit state during an OUT transaction.

0 - Toggle 0 (OUT transaction)

1 - Toggle 1 (OUT transaction)

Bit2 Reserved

Bit1 OutToggleSet

Set this bit to "1" to set the toggle sequence bit of an OUT transaction to "1."

0 - No operation

1 - Toggle 1 (OUT transaction)

Bit0 OutToggleClr

Set this bit to “1” to set the toggle sequence bit of an OUT transaction to “0.”

0 - No operation

1 - Toggle 0 (OUT transaction)

2.2.7.13 0x6C Channel0 FIFO for CPU HIGH (0FIFOforCPU_H)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x6C	0FIFOforCPU_H	7: FIFOforCPU[15]	R/W	FIFOforCPU[15:8]	unfixed
		6: FIFOforCPU[14]	R/W		
		5: FIFOforCPU[13]	R/W		
		4: FIFOforCPU[12]	R/W		
		3: FIFOforCPU[11]	R/W		
		2: FIFOforCPU[10]	R/W		
		1: FIFOforCPU[9]	R/W		
		0: FIFOforCPU[8]	R/W		

Bit7-0 FIFOforCPU [15:8]

This register is used for PIO access to the FIFO on channel 0 or at endpoint 0. If the CPUConfig_0 register's CPUBus8x16 bit is set to "0," this register displays MSB 8 bits of 16-bit data.

When the aFIFOControl_0 register's FIFOwr bit is set to "1," you can write data to the FIFO by writing the value to this register.

When the aFIFOControl_0 register's FIFOrd bit is set to "1," you can read data from the FIFO by reading the value from this register.

When this register is accessed, the internal reference pointer inside the FIFO proceeds automatically.

Do not access this register when aFIFOControl_0 register's FIFOByteAccess bit is set to "1" or the CPUConfig_0 register's CPUBus8x16 bit is set to "1."

2.2.7.14 0x6D Channel0 FIFO for CPU LOW (0FIFOforCPU_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x6D	0FIFOforCPU_L	7: FIFOforCPU[7]	R/W	FIFOforCPU[7:0]	unfixed
		6: FIFOforCPU[6]	R/W		
		5: FIFOforCPU[5]	R/W		
		4: FIFOforCPU[4]	R/W		
		3: FIFOforCPU[3]	R/W		
		2: FIFOforCPU[2]	R/W		
		1: FIFOforCPU[1]	R/W		
		0: FIFOforCPU[0]	R/W		

Bit7-0 FIFOforCPU [7:0]

This register is used for PIO access to the FIFO on channel 0 or at endpoint 0. If the CPUConfig_0 register's CPUBus8x16 bit is set to "0," this register shows LSB 8 bits of 16-bit data.

When the aFIFOControl_0 register's FIFOwr bit is set to "1," you can write data to the FIFO by writing a value to this register.

When the aFIFOControl_0 register's FIFOrd bit is set to "1," you can read data from the FIFO by reading the value from this register.

When this register is accessed, the reference pointer inside the FIFO proceeds automatically.

PIO access is enabled only for setting or referencing this register if the aFIFOControl_0 register's FIFOByteAccess bit or the CPUConfig_0 register's CPUBus8x16 bit is set to "1."

2.2.7.15 0x6E Channel0 FIFO Control0 (0FIFOControl_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x6E	0FIFOControl_0	7: FIFOEmpty	R	0: FIFO Not Empty	1: FIFO Empty	80h
		6: FIFOFull	R	0: FIFO Not Full	1: FIFO Full	
		5: EnFIFOwr	R/W	0: Disable CPU FIFO Write	1: Enable CPU FIFO Write	
		4: EnFIFOrd	R/W	0: Disable CPU FIFO Read	1: Enable CPU FIFO Read	
		3: EnFIFOByteAccess	R/W	0: Normal	1: Byte Access Enable	
		2: FIFODataRemain[10]	R	FIFODataRemain[10:8]		
		1: FIFODataRemain[9]	R			
		0: FIFODataRemain[8]	R			

Displays and controls the FIFO area state on channel 0 or at endpoint 0.

Bit7 FIFOEmpty

A value of "1" for this bit means that the FIFO area on channel 0 or at endpoint 0 is empty. A value of "1" is set when all pages specified by the MaxPktSize_H register's BufferPage bit are empty. This bit assumes a value of "0" if non-empty pages exist.

0 - The FIFO area is not empty.

1 - The FIFO area is empty.

Bit6 FIFOFull

A value of "1" for this bit means that the FIFO area on channel 0 or at endpoint 0 is full. A value of "1" is set when all pages specified by the MaxPktSize_H register's BufferPage bit are full.

This bit assumes a value of "0" if non-full pages exist.

0 - The FIFO area is not full.

1 - The FIFO area is full.

Bit5 EnFIFOwr

Set this bit to "1" to enable data writing to the FIFO through the PIO.

0 - Disables data writing to the FIFO through the PIO.

1 - Enables data writing to the FIFO through the PIO.

Bit4 EnFIFOrd

Set this bit to "1" to enable data reading from the FIFO through the PIO.

0 - Disables data reading from the FIFO through the PIO.

1 - Enables data reading from the FIFO through the PIO.

Bit3 EnFIFOByteAccess

Set this bit to "1" if register access is in 16 bit units and PIO access to the FIFO is in byte units. If this bit is set to "1," access to MSB 8 bits (0FIFOforCPU_H register) of the PIO register is disabled and there will be only access to LSB 8 bits (0FIFOforCPU_L register).

0 - PIO access in word units

1 - PIO access in byte units

Reference

For big endian:

Data is accessed as follows when the FIFOforCPU register is accessed with this bit set to "1":

Write: If the system memory data is 0x1234, 0x34 is written to the FIFO.

Read: If data in the FIFO is 0x1234, it is read as 0x1212.

Bit2-0 FIFODataRemain [10:8]

Indicates MSB 3 bits (bits 10 to 8) of the remaining data byte count in the FIFO on channel 0 or at endpoint 0. The remaining data count shows a value for the entire FIFO on the channel or at the endpoint in question.

The values for bits 7 to 0 (0FIFOControl_1 register's FIFODataRemain[7] to [0] bits) are fixed after this register (bits 10 to 8) is read. However, counting continues inside the IC even after the readings are fixed.

Accordingly, access the 0FIFOControl_0 (FIFODataRemain[10] to [8]) and 0FIFOControl_1 (FIFODataRemain[7] to [0]) registers in this sequence to read the remaining data count during 8-bit register access. This register need not be read.

2.2.7.16 0x6F Channel0 FIFO Control1 (0FIFOControl_1)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x6F	0FIFOControl_1	7: FIFODataRemain[7]	R	FIFODataRemain[7:0]	00h
		6: FIFODataRemain[6]	R		
		5: FIFODataRemain[5]	R		
		4: FIFODataRemain[4]	R		
		3: FIFODataRemain[3]	R		
		2: FIFODataRemain[2]	R		
		1: FIFODataRemain[1]	R		
		0: FIFODataRemain[0]	R		

Displays and controls the FIFO area state on channel 0 or at endpoint 0.

Bit7-0 FIFODataRemain [7:0]

Indicates LSB 8 bits (bits 7 to 0) of the remaining data byte count in the FIFO on channel 0 or at endpoint 0. The remaining data count shows a value for the entire FIFO on the channel or at the endpoint in question.

The values in this register (bits 7 to 0) are fixed after bits 10 to 8 (0FIFOControl_0 register's FIFODataRemain[10] to [8] bits) are read. However, counting continues inside the IC even after the readings are fixed.

Accordingly, access the 0FIFOControl_0 (FIFODataRemain[10] to [8]) and 0FIFOControl_1 (FIFODataRemain[7] to [0]) registers in this sequence to read the remaining data count during 8-bit register access. However, the 0FIFOControl_0 register's FIFODataRemain[10] to [8] need not be read.

2.2.8 ChannelA Control Block

2.2.8.1 0x70 ChannelA Configuration0 (aConfig_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x70	aConfig_0	7: JoinDMA	R/W	0: Not Joint to DMA	1: Joint to DMA	00h
		6: FIFOClr	W	0: Normal	1: FIFO Clear	
		5: ToggleMode	R/W	0: When normal completed toggle	1: Always toggle	
		4: AutoZeroLen	R/W	0: Disable AutoZeroLen Mode	1: Enable AutoZeroLen Mode	
		3:				
		2:				
		1:				
		0:				

Sets the basic configuration of channel A during host operations or endpoint A during peripheral operations.

Bit7 JoinDMA

Connects this channel or endpoint to the DMA.

The DMA is connected to the channel or endpoint where this bit is most recently set to "1."

0 - Does not connect this channel or endpoint to the DMA.

1 - Connect this channel or endpoint to the DMA.

Bit6 FIFOClr

Set this bit to "1" to return the FIFO read/write pointer of this channel or endpoint to the beginning.

After the FIFOClr is completed, this bit is automatically cleared to "0."

0 - No operation (clear completed)

1 - Returns the FIFO read/write pointer of this channel or endpoint to the beginning.

While a transaction is suspended during host operations, be sure to clear the FIFO using this bit if you want to start a new transfer to this channel, rather than resuming the halted transfer.

Bit5 ToggleMode

Sets the toggle bit's operating mode. This bit setting is enabled only when the aConfig_1 register's TranType bit is set to "10b" (interrupt transfer).

0 - Only toggles a successful transaction.

1 - Toggles all transactions.

Bit4 AutoZeroLen

During host operations

Specifies whether to automatically supply a zero-length packet at the end of transfer after the data size specified by the PIPEaTotalSizeH to L registers has been completely transferred when the maximum packet size is reached. This bit is enabled only for OUT transfers.

During peripheral operations

If the aConfig_0 register's JoinDMA bit is set to "1" during an IN transaction, the EnShortPkt bit is automatically set to "1" after all data has been transferred (settings identical to those for the EPIntStat register's INTranCmp bit).With this setting, a zero-length packet can be sent automatically to the same token types.

The EnShortPkt bit automatically set to "1" is cleared to "0" after one token is received. All of the data (zero-length packet in this case) is then transmitted.

0 - Does not automatically supply a zero-length packet.

1 - Automatically supplies a zero-length packet.

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 Reserved

2.2.8.2 0x71 ChannelA Configuration1 (aConfig_1)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x71	aConfig_1	7: DirPID[1]	R/W	DirPID[1:0]	00h
		6: DirPID[0]	R/W		
		5: TranType[1]	R/W	TranType[1:0]	
		4: TranType[0]	R/W		
		3: EPNumber[3]	R/W	EPNumber[3:0]	
		2: EPNumber[2]	R/W		
		1: EPNumber[1]	R/W		
		0: EPNumber[0]	R/W		

Sets the basic configuration of channelA during host operations or endpointA during peripheral operations.

Bit7-6 DirPID [1:0]

During host operations

Sets the token types (OUT, IN or SETUP) issued by this channel.

00b - Issues OUT tokens.

01b - Issues SETUP tokens.

10b - Issues IN tokens.

11b - (Reserved)

During peripheral operations

Sets the transfer direction at this endpoint.

00b - OUT direction

01b - (Reserved)

10b - IN direction

11b - (Reserved)

Bit5-4 TranType [1:0]

Sets the transfer type for this channel during host operations or the transfer type corresponding to this endpoint during peripheral operations.

00b - Control transfer

01b - Isochronous transfer

10b - Bulk transfer

11b - Interrupt transfer

Bit3-0 EPNumber [3:0]

Sets the endpoint number used for transfer on this channel during host operations or the endpoint number to be controlled by this register block during peripheral operations.

0 to 15 - Any endpoint number

2.2.8.3 0x72 ChannelA Max Packet Size HIGH (aMaxPktSize_H)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x72	aMaxPktSize_H	7:			00h
		6: BufferPage[4]	R/W	BufferPage[4:0]	
		5: BufferPage[3]	R/W		
		4: BufferPage[2]	R/W		
		3: BufferPage[1]	R/W		
		2: BufferPage[0]	R/W		
		1: MaxPktSize[9]	R/W	Max packet size[9:8]	
		0: MaxPktSize[8]	R/W		

Sets the maximum packet size for channelA during host operations or endpointA during peripheral operations. This register also sets the buffer area page count for each operation.

Bit7 Reserved

Bit6-2 BufferPage [4:0]

Specifies the FIFO area's buffer page count for this channel or endpoint.

0 - Disabled

1 to 31 - Any buffer page count

The size set by the aMaxPktSize register represents one buffer page. Accordingly, aMaxPktSize × BufferPage (this bit) is secured as the buffer area size. The total size of the FIFO area is 2.5 Kbytes. Consider the buffer size secured by other channels or endpoints when setting this bit.

Note: Do not set this field except during SetBuffer execution.

Bit1-0 MaxPktSize [9:8]

Sets the higher 2 bits of the maximum byte count (10 bits) for the packet size that the endpoint in question can send or receive.

"00b" is set in these bits for bulk (control) or interrupt transfers, since the maximum packet size is 64 bytes.

For isochronous transfers, set the higher 2 bits in the range from 2 to 1,022 bytes.

0 - Disabled

2 to 1022 - Maximum packet size byte count

2.2.8.4 0x73 ChannelA Max Packet Size LOW (aMaxPktSize_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x73	aMaxPktSize_L	7: MaxPktSize[7]	R/W	MaxPacketSize [7:0]	00h
		6: MaxPktSize[6]	R/W		
		5: MaxPktSize[5]	R/W		
		4: MaxPktSize[4]	R/W		
		3: MaxPktSize[3]	R/W		
		2: MaxPktSize[2]	R/W		
		1: MaxPktSize[1]	R/W		
		0: MaxPktSize[0]	R/W		

Sets the maximum packet size for channelA during host operations or endpointA during peripheral operations.

Bit7-0 MaxPktSize [7:0]

Sets LSB 8 bits of the maximum byte count (10 bits) for the packet size the endpoint in question can send or receive.

Select from 8, 16, 32, and 64 bytes for bulk (control) transfers.

For interrupt transfers, set a size in the range from 2 to 64 bytes.

For isochronous transfers, set LSB 8 bits in the range from 2 to 1,022 bytes.

Note that the maximum packet size must be an even number of bytes (2 byte units).

0	Disabled
8, 16, 32, 64	Bulk/control transfer
2 to 64	Interrupt transfer
2 to 1022	Isochronous transfer

Note: Set this field only during SetBuffer execution.

2.2.8.5 0x74 PipeA Interval Time (PIPEaInterval)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x74	PIPEaInterval	7: Interval[7]	R/W	Interval[7:0]	00h
		6: Interval[6]	R/W		
		5: Interval[5]	R/W		
		4: Interval[4]	R/W		
		3: Interval[3]	R/W		
		2: Interval[2]	R/W		
		1: Interval[1]	R/W		
		0: Interval[0]	R/W		

Sets the token issue interval (cycle) on channelA during host operations.

Bit7-0 Interval [7:0]

Specifies the token issue interval (cycle) for interrupt transfers in ms order (frame units). This bit setting is enabled only when the aConfig register's TranType bit is set to "10b" (interrupt transfer). This bit cannot be set to "0d".

This bit also determines transaction retransmission intervals.

0 - Disabled

1 to 255 - Token issue cycle (ms [frame])

2.2.8.6 0x75 PipeA Transfer Configuration (PIPEaTranConfig)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x75	PIPEaTranConfig	7:			00h
		6: Continuity[2]	R/W	Continuity[2:0]	
		5: Continuity[1]	R/W		
		4: Continuity[0]	R/W		
		3:			
		2: FuncAddr[2]	R/W	FunctionAddress[2:0]	
		1: FuncAddr[1]	R/W		
		0: FuncAddr[0]	R/W		

Sets basic transfer functions involving channelA during host operations.

Bit7 Reserved

Bit6-4 Continuity [2:0]

Specifies the continuous execution count of transactions (continuous issue count of tokens) in this channel for host controller scheduling.

This bit setting is enabled only when the aConfig register's TranType bit is set to "00b" (bulk transfer) or "01b" (control transfer). This bit cannot be set to "0d".

For host controller scheduling, continuous execution continues to be counted across frames. Although the count includes retransmission due to packet errors, retransmission following an NAK does not depend on the setting of this bit.

0 - Continuous transaction execution count = 8 (Max.)

1 to 7 - Continuous transaction execution count

Bit3 Reserved

Bit2-0 FuncAddr [2:0]

Sets the USB address of the function, including the endpoint controlled by this channel.

0 to 7 - Function address

2.2.8.7 0x76 PipeA Control (PIPEaControl)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x76	PIPEaControl	7:				00h
		6:				
		5:				
		4: Toggle	R/W	0: Toggle 0	1: Toggle 1	
		3:				
		2:				
		1:				
		0: TranGo	R/W	0: Standby	1: Transaction Start	

Controls functions involving channelA during host operations.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Toggle

Sets the default value for the toggle sequence bit when a transaction starts. This bit also indicates the toggle sequence bit state after a transaction is executed and completed.

0 - Toggle 0

1 - Toggle 1

Bit3 Reserved

Bit2 Reserved

Bit1 Reserved

Bit0 TranGo

Set this bit to “1” to start a transaction on this channel. The started transaction can be halted by clearing this bit to “0.” This bit also indicates whether a transaction is underway on this channel.

0 - Stops a transaction.

1 - Starts a transaction (or a transaction is underway).

After completion of the transfer up to the byte count set in the PIPEaTotalSize_H to L registers, the PIPEaIntStat register’s PIPEaTranCmp bit is set to “1,” and this bit automatically reverts to “0.” This bit is also reset to “0” if the PIPEaIntStat register’s InShortRcv, InOverSize, TranErr, Stalled, or NoResp bit is set. It is not reset to “0” if a transaction is halted due to factors that cause the HCIntStat register’s PortErr bit to be set.

If clearing this bit halts a transaction, the relevant PIPEaIntStat register bit is set when the current transaction is completed.

The data in the FIFO, the (remaining) total size, and settings for the channel remain unchanged even after a transaction is halted. Reset this bit to “1” to resume a transaction from the point halted.

To start a new transaction, clear the FIFO and reset channel information.

2.2.8.8 0x77 PipeA Total Size HIGH (PIPEaTotalSize_H)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x77	PIPEaTotalSize_H	7: TotalSize[23]	R/W	TotalSize[23:16]	00h
		6: TotalSize[22]	R/W		
		5: TotalSize[21]	R/W		
		4: TotalSize[20]	R/W		
		3: TotalSize[19]	R/W		
		2: TotalSize[18]	R/W		
		1: TotalSize[17]	R/W		
		0: TotalSize[16]	R/W		

2.2.8.9 0x78 PipeA Total Size Middle (PIPEaTotalSize_M)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x78	PIPEaTotalSize_M	7: TotalSize[15]	R/W	TotalSize[15:8]	00h
		6: TotalSize[14]	R/W		
		5: TotalSize[13]	R/W		
		4: TotalSize[12]	R/W		
		3: TotalSize[11]	R/W		
		2: TotalSize[10]	R/W		
		1: TotalSize[9]	R/W		
		0: TotalSize[8]	R/W		

2.2.8.10 0x79 PipeA Total Size LOW (PIPEaTotalSize_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x79	PIPEaTotalSize_L	7: TotalSize[7]	R/W	TotalSize[7:0]	00h
		6: TotalSize[6]	R/W		
		5: TotalSize[5]	R/W		
		4: TotalSize[4]	R/W		
		3: TotalSize[3]	R/W		
		2: TotalSize[2]	R/W		
		1: TotalSize[1]	R/W		
		0: TotalSize[0]	R/W		

PIPEaTotal_H

PIPEaTotal_M

PIPEaTotal_L

For the total byte count for the transfer data on channelA (16,777,214 bytes Max.: about 16.4 Mbytes), set bits 23 to 16 in the PIPEaTotalSize_H register, bits 15 to 8 in the PIPEaTotalSize_M register and bits 7 to 0 in the PIPEaTotalSize_L register.

If the PIPEaControl register's TranGo bit starts a transaction, you can check the remaining count by reading this register.

The values for bits 7 to 0 (PIPEaTotalSize_L register) are fixed after reading bits 15 to 8 (PIPEaTotalSize_M register). However, counting continues inside the IC even after the readings are fixed.

Accordingly, access the PIPEaTotalSize_M, (PIPEaTotalSize_H), and PIPEaTotalSize_L registers in this sequence to read the remaining count during 8-bit register access. During 16-bit access, first read the LSB bits (bits 15 to 0), then the MSB bits (bits 23 to 16).

The MSB register need not be read if the count to be transferred does not reach it.

A zero-length packet is sent after an OUT transaction is executed with the TotalSize set to "0." If an OUT or IN transaction is executed with the TotalSize set to "0xFFFFFF," the total size is not limited and is not counted. In this case, the PIPEaIntStat register's TranCmp bit is not set.

2.2.8.11 0x7A EndpointA Control0 (EPaControl_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x7A	EPaControl_0	7: EnEndPoint	R/W	0: Enable EndPoint	1: Disable EndPoint	00h
		6: AutoForceNAK	R/W	0: Normal	1: Auto Force NAK	
		5: EnShortPkt	R/W	0: Normal	1: Send Short Packet	
		4: AutoForceNAKShort		0: Normal	1: Auto Force NAK Short	
		3:				
		2:				
		1: ForceNAK	R/W	0: Normal	1: Force NAK	
		0: ForceSTALL	R/W	0: Normal	1: Force STALL	

Configures operations at endpointA during peripheral operations.

Bit7 EnEndPoint

Set this bit to "1" to enable this endpoint.

When this bit is set to "0," access to this endpoint is neglected.

Set the bit based on the SetConfiguration request from the host.

0 - Disables this endpoint.

1 - Enables this endpoint.

Bit6 AutoForceNAK

Automatically sets the EPaControl_0 register's ForceNAK bit to "1" when a transaction is successfully completed at this endpoint.

0 - Does not set the ForceNAK bit automatically.

1 - Automatically sets the ForceNAK bit.

This bit is used to halt each transaction, apart from other transactions.

Bit5 EnShortPkt

Set this bit to "1" to enable transmission of the current data in the FIFO as short packets, even if the data count in the FIFO does not reach the maximum packet size for an IN transaction at this endpoint. After an entire short packet is sent, this bit is automatically cleared to "0." A zero-length packet is sent if this bit is set to "1" when there is no data in the FIFO.

This bit is enabled only if the aConfig_1 register's DirPID bit is set to "01b" (IN direction).

0 - No operation

1 - Sends the current data in the FIFO.

Bit4 AutoForceNAKShort

When this bit is set to "1," the ForceNAK bit is automatically set to "1" if the packet received by this endpoint is a short packet when an OUT transaction is successfully completed.

If the AutoForceNAK bit is set to "1," AutoForceNAKShort bit is preceded by the AutoForceNAK bit.

0 - Does not automatically set the ForceNAK bit to "1."

1 - Automatically sets the ForceNAK bit to "1."

Bit3 Reserved

Bit2 Reserved

Bit1 ForceNAK

Set this bit to "1" to return an NAK in response to a transaction, regardless of the data count in the FIFO.

If this bit is set during a transaction, the setting will apply only for the next transaction and thereafter.

0 - No operation

1 - Forcibly returns an NAK.

Bit0 ForceSTALL

Set this bit to "1" to return a STALL in response to a transaction at this endpoint. This bit setting precedes that of the ForceNAK bit.

If this bit is set during a transaction, the setting will apply only for the next transaction and thereafter.

0 - No operation

1 - Forcibly returns a STALL.

2.2.8.12 0x7B EndpointA Control1 (EPaControl_1)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x7B	EPaControl_1	7:				00h
		6:				
		5:				
		4:				
		3: ToggleStat	R	0: Transaction Toggle 0	1: Transaction Toggle 1	
		2:				
		1: ToggleSet	W	0: Normal	1: Transaction Toggle Set	
		0: ToggleClr	W	0: Normal	1: Transaction Toggle Clear	

Configures operations at endpointA during peripheral operations.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 ToggleStat

Indicates the toggle sequence bit state.

0 - Toggle 0

1 - Toggle 1

Bit2 Reserved

Bit1 ToggleSet

Set this bit to “1” to set the toggle sequence bit to “1.”

0 - No operation

1 - Toggle 1

Bit0 ToggleClr

Set this bit to “1” to set the toggle sequence bit to “0.”

0 - No operation

1 - Toggle 0

2.2.8.13 0x7C ChannelA FIFO for CPU HIGH (aFIFOforCPU_H)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x7C	aFIFOforCPU_H	7: FIFOforCPU[15]	R/W	FIFOforCPU[15:8]	unfixed
		6: FIFOforCPU[14]	R/W		
		5: FIFOforCPU[13]	R/W		
		4: FIFOforCPU[12]	R/W		
		3: FIFOforCPU[11]	R/W		
		2: FIFOforCPU[10]	R/W		
		1: FIFOforCPU[9]	R/W		
		0: FIFOforCPU[8]	R/W		

Bit7-0 FIFOforCPU [15:8]

This register is used for PIO access to the FIFO in this channel or at this endpoint. If the CPUConfig_0 register's CPUBus8x16 bit is set to "0," this register shows MSB 8 bits of 16-bit data.

When the aFIFOControl_0 register's FIFOwr bit is set to "1," you can write data to the FIFO by writing a value to this register.

When the aFIFOControl_0 register's FIFOrd bit is set to "1," you can read data from the FIFO by reading the value from this register.

When this register is accessed, the reference pointer inside the FIFO proceeds automatically.

Do not access this register when aFIFOControl_0 register's FIFOByteAccess bit is set to "1" or the CPUConfig_0 register's CPUBus8x16 bit is set to "1."

2.2.8.14 0x7D ChannelA FIFO for CPU LOW (aFIFOforCPU_L)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x7D	aFIFOforCPU_L	7: FIFOforCPU[7]	R/W	FIFOforCPU[7:0]	unfixed
		6: FIFOforCPU[6]	R/W		
		5: FIFOforCPU[5]	R/W		
		4: FIFOforCPU[4]	R/W		
		3: FIFOforCPU[3]	R/W		
		2: FIFOforCPU[2]	R/W		
		1: FIFOforCPU[1]	R/W		
		0: FIFOforCPU[0]	R/W		

Bit7-0 FIFOforCPU [7:0]

This register is used for PIO access to the FIFO in this channel or at this endpoint. If the CPUConfig_0 register's CPUBus8x16 bit is set to "0," this register shows LSB 8 bits of 16-bit data.

When the aFIFOControl_0 register's FIFOwr bit is set to "1," you can write data to the FIFO by writing a value to this register.

When the aFIFOControl_0 register's FIFOrd bit is set to "1," you can read data from the FIFO by reading the value from this register.

When this register is accessed, the reference pointer inside the FIFO proceeds automatically.

PIO access is enabled only for setting or referencing this register if the aFIFOControl_0 register's FIFOByteAccess bit or the CPUConfig_0 register's CPUBus8x16 bit is set to "1."

2.2.8.15 0x7E ChannelA FIFO Control0 (aFIFOControl_0)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0x7E	aFIFOControl_0	7: FIFOEmpty	R	0: FIFO Not Empty	1: FIFO Empty	80h
		6: FIFOFull	R	0: FIFO Not Full	1: FIFO Full	
		5: EnFIFOwr	R/W	0: Disable CPU FIFO Write	1: Enable CPU FIFO Write	
		4: EnFIFOrd	R/W	0: Disable CPU FIFO Read	1: Enable CPU FIFO Read	
		3: EnFIFOByteAccess	R/W	0: Normal	1: Byte Access Enable	
		2: FIFODataRemain[10]	R	FIFODataRemain[10:8]		
		1: FIFODataRemain[9]	R			
		0: FIFODataRemain[8]	R			

Displays and controls the FIFO area state on channelA or at endpointA.

Bit7 FIFOEmpty

A value of "1" for this bit means that the FIFO area on this channel or at this endpoint is empty. A value of "1" is set when all pages specified by the MaxPktSize_H register's BufferPage bit are empty. This bit assumes a value of "0" if non-empty pages exist.

Make sure that this bit is set to "0" when reading data from the FIFO through the PIO.

0 - The FIFO area is not empty.

1 - The FIFO area is empty.

Bit6 FIFOFull

A value of "1" for this bit indicates that the FIFO area on this channel or at this endpoint is full.

"1" is set when all pages specified by the MaxPktSize_H register's BufferPage bit are full. This bit assumes a value of "0" if non-full pages exist.

Make sure this bit is set to "0" when writing data to the FIFO through the PIO.

0 - The FIFO area is not full.

1 - The FIFO area is full.

Bit5 EnFIFOwr

Set this bit to "1" to enable data writing to the FIFO through the PIO.

0 - Disables data writing to the FIFO through the PIO.

1 - Enables data writing to the FIFO through the PIO.

Bit4 EnFIFOrd

Set this bit to "1" to enable data reading from the FIFO through the PIO.

0 - Disables data reading from the FIFO through the PIO.

1 - Enables data reading from the FIFO through the PIO.

Bit3 EnFIFOByteAccess

Set this bit to “1” if register access is in 16 bit units and PIO access to the FIFO is in byte units. If this bit is set to “1,” access to MSB 8 bits (aFIFOforCPU_H register) of the PIO register is disabled, and only access to LSB 8 bits (aFIFOforCPU_L register) is possible.

0 - PIO access in word units

1 - PIO access in byte units

Reference

For big endian:

Data is accessed as follows when the FIFOforCPU register is accessed with this bit set to “1”:

Write: If the system memory data is 0x1234, 0x34 is written to the FIFO.

Read: If the data value in the FIFO is 0x1234, it is read as 0x1212.

Bit2-0 FIFODataRemain [10:8]

Indicates MSB 3 bits (bits 10 to 8) of the remaining data byte count in the FIFO on channelA or at endpointA. The remaining data count indicates a value for the entire FIFO on the channel or at the endpoint in question.

The values for bits 7 to 0 (aFIFOControl_1 register’s FIFODataRemain[7] to [0] bits) are fixed after reading this register (bits 10 to 8). However, counting continues inside the IC, even after the readings are fixed.

Accordingly, access the aFIFOControl_0 (FIFODataRemain[10] to [8]) and aFIFOControl_1 (FIFODataRemain[7] to [0]) registers in this sequence to read the remaining data count during 8-bit register access. This register need not be read.

2.2.8.16 0x7F ChannelA FIFO Control1 (aFIFOControl_1)

Address	Register Name	Bit Symbol	R/W	Description	Reset
0x7F	aFIFOControl_1	7: FIFODataRemain[7]	R	FIFODataRemain[7:0]	00h
		6: FIFODataRemain[6]	R		
		5: FIFODataRemain[5]	R		
		4: FIFODataRemain[4]	R		
		3: FIFODataRemain[3]	R		
		2: FIFODataRemain[2]	R		
		1: FIFODataRemain[1]	R		
		0: FIFODataRemain[0]	R		

Displays and controls the FIFO area state on channelA or at endpointA.

Bit7-0 FIFODataRemain [7:0]

Indicates LSB 8 bits (bits 7 to 0) of the remaining data byte count in the FIFO on channelA or at endpointA. The remaining data count shows a value for the entire FIFO on the channel or at the endpoint in question.

The values in this register (bits 7 to 0) are fixed after reading bits 10 to 8 (aFIFOControl_0 register's FIFODataRemain[10] to [8] bits). However, counting continues inside the IC even after the readings are fixed.

Accordingly, access the aFIFOControl_0 (FIFODataRemain[10] to [8]) and aFIFOControl_1 (FIFODataRemain[7] to [0]) registers in this sequence to read the remaining data count during 8-bit register access. The aFIFOControl_0 register's FIFODataRemain[10] to [8] need not be read.

2.2.9 ChannelB Register Block

The register contents of the channelB register block (0x80 to 0x8F) are the same as those of the channelA register block (0x70 to 0x7F). For more information, refer to the discussion of channelA.

When making a reference, change the register names as follows:

aConfig_0/1	→ bConfig_0/1
aMaxPktSize_H/L	→ bMaxPktSize_H/L
PIPEaInterval	→ PIPEbInterval
PIPEaTranConfig	→ PIPEbTranConfig
PIPEaControl	→ PIPEbControl
PIPEaTotalSizeH/M/L	→ PIPEbTotalSizeH/M/L
EPaControl_0/1	→ EPbControl_0/1
aFIFOforCPU_H/L	→ bFIFOforCPU_H/L
aFIFOControl_0/1	→ bFIFOControl_0/1

Apply the same rule to other registers (i.e., in addition to those above) whose names include characters indicating a channel (interrupt-related registers, etc.).

2.2.10 ChannelC Register Block

The register contents of the channelC register block (0x90 to 0x9F) are the same as those of the channelA register block (0x70 to 0x7F). For more information, refer to the discussion of channelA.

When making a reference, change the register names as follows:

aConfig_0/1	→ cConfig_0/1
aMaxPktSize_H/L	→ cMaxPktSize_H/L
PIPEaInterval	→ PIPEcInterval
PIPEaTranConfig	→ PIPEcTranConfig
PIPEaControl	→ PIPEcControl
PIPEaTotalSizeH/M/L	→ PIPEcTotalSizeH/M/L
EPaControl_0/1	→ EPcControl_0/1
aFIFOforCPU_H/L	→ cFIFOforCPU_H/L
aFIFOControl_0/1	→ cFIFOControl_0/1

Apply the same rule to other registers (i.e., in addition to those above) whose names include characters indicating a channel (interrupt-related registers, etc.).

2.2.11 ChannelD Register Block

The register contents of the channelD register block (0xA0 to 0xAF) are the same as those of the channelA register block (0x70 to 0x7F). For more information, refer to the discussion of channelA.

When making a reference, change the register names as follows:

aConfig_0/1	→ dConfig_0/1
aMaxPktSize_H/L	→ dMaxPktSize_H/L
PIPEaInterval	→ PIPEdInterval
PIPEaTranConfig	→ PIPEdTranConfig
PIPEaControl	→ PIPEdControl
PIPEaTotalSizeH/M/L	→ PIPEdTotalSizeH/M/L
EPaControl_0/1	→ EPdControl_0/1
aFIFOforCPU_H/L	→ dFIFOforCPU_H/L
aFIFOControl_0/1	→ dFIFOControl_0/1

Apply the same rule to other registers (i.e., in addition to those above) whose names include characters indicating a channel (interrupt-related registers, etc.).

2.2.12 ChannelE Register Block

The contents of registers in the channel E register block (0xB0 to 0xBF) are identical to those in the channel A register block (0x70 to 0x7F). For more information on the channel E registers, refer to the description of channel A registers. In that case, please confirm that each register name is read as shown below.

(1) eConfig (0xB0, 0xB1)	= 0x003F
(2) eMaxPktSize (0xB2, 0xB3)	= 0x0010
(3) PIPEeControl_0 (0xB4, 0xB5)	= 0x0107
(4) PIPEeControl_1 (0xB6, 0xB7)	= 0x00FF
(5) PIPEeControl_2 (0xB8, 0xB9)	= 0xFFFF
(6) eFIFOControl (0xBE, 0xBF)	= 0x0000
(7) PipeEPCommon (0x3E, 0x3F)	= 0x0100
(8) PIPEeControl_1 (0xB6, 0xB7)	= 0x01FF

In addition, register names including letters representing a channel (e.g., interrupt related registers) should be read in the same way as above.

Dummy pipe (PIPEe) settings during host operations required for the S1R72005#00A100 do not need to be set in the S1R72005#00A300.

2.2.13 0xE1 Extra OTG State Command (E_OTGStateCmd)

Address	Register Name	Bit Symbol	R/W	Description		Reset
0xE1	E_OTGStateCmd	7:E_OTGStateCmd[7]	R/W			08h
		6:E_OTGStateCmd[6]	R/W			
		5:E_OTGStateCmd[5]	R/W			
		4:E_OTGStateCmd[4]	R/W			
		3:E_OTGStateCmd[3]	R/W			
		2:E_OTGStateCmd[2]	R/W			
		1:E_OTGStateCmd[1]	R/W			
		0:E_OTGStateCmd[0]	R/W			

The E_OTGStateCmd register is used to control OTG state transitions.

Writing 0x84 to this register pulls up the DP line.

Writing 0x00 to this register validates the setting of OTGStateCmd (0x35).

Do not set the other values. (Setting prohibited.)

When the HVDD power voltage exceeds 3.25V, SRP Data-line Pulsing is executed using this register or OTGStateCmd register (0x35).

When the HVDD power voltage is 3.25V or less, you must use this register to execute SRP Data-line Pulsing.

[Use example of SRP Data-line Pulsing]

(1) Confirm that 2ms (Tb_se0_srp) or more elapsed after b_idle was set as the VBUS voltage was below 2.0V.

(2) Set 0x84 into the E_OTGStateCmd register.
The voltage of the DP line is then set high.

(3) Wait for the duration of Tb_DATA_PLS (5 to 10 ms).

(4) Set 0x00 in the E_OTGStateCmd register.

This makes the setting of OTGStateCmd(0x35 bits 3 to 0) valid. The setting is automatically determined by the b_idle state. The voltage of the DP line is then set low.

2.2.14 0xC0 to 0xFF Register Blocks

The 0xC0 to 0xCF, 0xD0 to 0xDF, 0xE0 to 0xEF, and 0xF0 to 0xFF blocks are reserved. IC operations involving access to these blocks is not guaranteed. The reset value is “unfixed.”

3 KNOWN PROBLEMS AND CORRECTIVE RESPONSE

Notes on Using the EPSON S1R72005OTG Controller

The following problems have been encountered with the S1R72005 controller.

This chapter describes various ways to prevent the occurrence of such problems.

Consider the following when using the application software and driver software.

3.1 Known Problems When the S1R72005 Operates as a USB Host

A problem encountered with the earlier S1R72005B00A100 and S1R72005F00A100 models wherein the host issues an unintended token has been resolved in the S1R72005B00A300 and S1R72005F00A300.

No corrective measures are required in software.

3.2 Known Problems When the S1R72005 Operates as USB Device

3.2.1 Steps that May Cause Problems When the S1R72005 Operates as a USB Host

Problem of S1R72005 when the S1R72005 operates as USB device.

The phenomena described in Section 3.1 may arise if conditions (1) to (3) below are met at the same time.

(1). The EP0Control_0(0x6A) AutoForceNAK's value is "1", and the EP0Control_0.OutForceNAK bit or EP0Control_0.InForceNAK is "0".

so the Endpoint 0 can accept the transaction request from the host.

(2). Some Endpoints except Endpoint 0 are executing some transaction.

(3). One Endpoint except Endpoint 0 has finished some transaction before the transaction initiation for the Endpoint 0.

If these conditions (1) to (3) are met at the same time, the Endpoint0's InForceNAK or OutForceNAK bit is set to one by hardware problem.

If the Endpoint 0 does not have this hardware problem , The Endpoint 0 can accept token from host and can execute transaction one time, but the EP0 always returns the NAK handshake to the host because of this hardware problem.

When Endpoint0's AutoForceNAK bit is "1", The transaction behavior of EP0 and Other Endpoints is shown by the following table.

transaction of endpoints except EP0	EP0 IN and OutForceNAK status	result
OUT tolken – DATA – ACK	OutForceNAK is set	problem
OUT tolken – DATA(ShortPacket) – ACK	OutForceNAK is set	problem
OUT tolken – DATA(with CRC error)	OutForceNAK is not set	normal
OUT tolken – DATA(ToggleMiss) – ACK	OutForceNAK is not set	normal
OUT tolken – DATA – NAK	OutForceNAK is not set	normal
IN tolken – DATA – ACK	InForceNAK is set	problem
IN tolken – DATA(ShortPacket) – ACK	InForceNAK is set	problem
IN tolken – NAK	InForceNAK is not set	normal
IN tolken – DATA – ACK(with error)	InForceNAK is not set	normal

3.2.2 Basic Response (Recommended)

You should not use EP0 AutoForceNAK function.

In stead of using EP0's AutoForceNAK, We suggest the following method.

When the 0MaxPktSize_H.BufferPage register's value was set up as one, you can get the EP0InTranAck or EP0OutTranAck interrupt event as result of each transaction completion.

If you use those interrupts, you can get to know the completion timing of each EP0 transaction.

So, it is not necessary to use the AutoForceNAK function of Endpoint 0.

At the time, As the need arises, you can set the InForceNAK and OutForceNAK bit of EP0Control register.

If you want to use the AutoForceNAK of EP0, you should carefully avoid the conflict of transaction between EP0 and other endpoints.

By the way, Other endpoints except EP0 do not have this problem.

So, you can use the AutoForceNAK function except the EP0.

4 REVISION HISTORY

Revised on	Revision	Application	Type of Revision	Correction Contents
04/1/9	1.20	Chapter 3 in general	Addition	Addition of Section 3, “Known Problems and Action”
		0x32	Correction	Correction of register initialized by ResetHC
		0x32	Correction	Correction of register initialized by ResetOTGC
		0x37	Addition	Addition to discussion of HCStateCmd register
		0x3C, 0x3D	Addition	Addition of notes on reading PCFmNumber
		0x42	Correction	Correction of position error involving BurstFIFORemain bit in DMAControl register
04/2/27	1.21	Chapter 4 in general	Change	Change “Revision” to “Application” in the table Change Revision page to Revision register address or Revision chapter
		0x3C, 3D	Correction	Correction of notes on how to read PCFmNumber (Misprint of address)
07/10/10	1.30	4.REVISION HISTORY	Deletion	Deletion of history before 04/01/01. (important information is not included in deletion.)
		0x30	Addition	Addition of COMPPwrDown bit to register.
		0x48, 0x49	Addition	Addition of WaitPortDisable bit to register.
		Chapter 2.2.12	Deletion	Deletion of description about Dummy Pipe.
		Chapter 3.1	Deletion	Deletion of description about Host function problem.
		Chapter 3.2	Addition	Addition of description about Device function problem.
		0x6A	Addition	Addition of attention about AutoFofoceNAK problem.

(Types of Revision)

Correction: Correction of inaccuracies or errors

Change: Revisions in the content (or specifications) of an account or description

Addition: Addition of new content

Deletion: Deletion of content

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