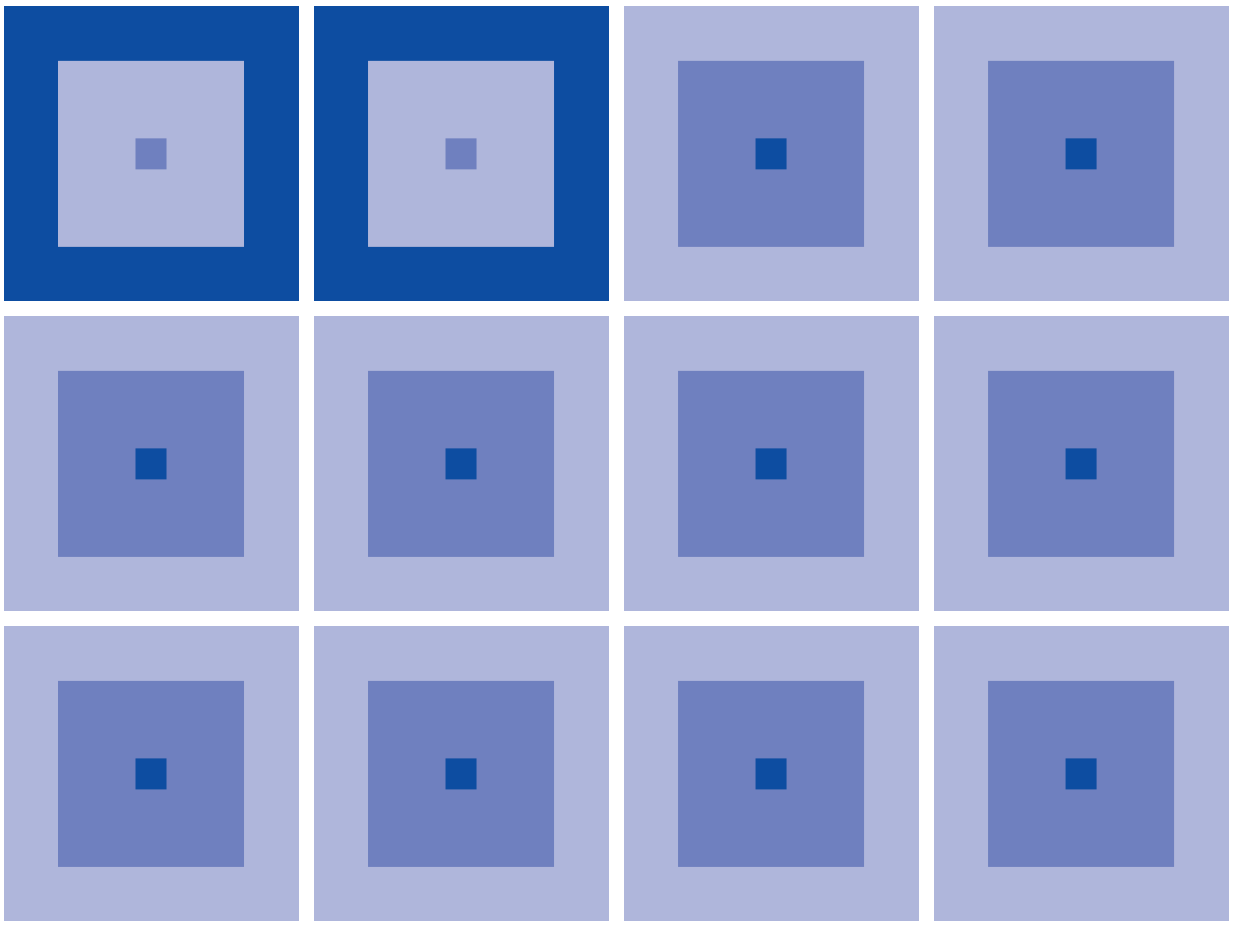
EPSON

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

S1C88848

Technical Manual

S1C88848 Technical Hardware



SEIKO EPSON CORPORATION

Configuration of product number

Devices

S1 C 88104 F 0A01 00

Packing specifications
- 00 : Besides tape & reel
- 0A : TCP BL 2 directions
- 0B : Tape & reel BACK
- 0C : TCP BR 2 directions
- 0D : TCP BT 2 directions
- 0E : TCP BD 2 directions
- 0F : Tape & reel FRONT
- 0G : TCP BT 4 directions
- 0H : TCP BD 4 directions
- 0J : TCP SL 2 directions
- 0K : TCP SR 2 directions
- 0L : Tape & reel LEFT
- 0M : TCP ST 2 directions
- 0N : TCP SD 2 directions
- 0P : TCP ST 4 directions
- 0Q : TCP SD 4 directions
- 0R : Tape & reel RIGHT
- 99 : Specs not fixed

Specification

Package
[D: die form; F: QFP]

Model number

Model name
[C: microcomputer, digital products]

Product classification
[S1: semiconductor]

Development tools

S5U1 C 88348 D1 1 00

Packing specifications
[00: standard packing]

Version
[1: Version 1]

Tool type
- Hx : ICE
- Ex : EVA board
- Px : Peripheral board
- Wx : Flash ROM writer for the microcomputer
- Xx : ROM writer peripheral board
- Cx : C compiler package
- Ax : Assembler package
- Dx : Utility tool by the model
- Qx : Soft simulator

Corresponding model number
[88348: for S1C88348]

Tool classification
[C: microcomputer use]

Product classification
[S5U1: development tool for semiconductor products]

Contents

1 INTRODUCTION

The S1C88848 microcomputer features the S1C88 (Model 3) CMOS 8-bit core CPU along with ROM, RAM, a remote-control carrier output, a dot-matrix LCD controller / driver that allows driving of up to 1,632 pixels, three different timers and a serial interface with optional asynchronization or clock synchronization.

The S1C88848 is fully operable over a wide range of voltages, and can perform stable operations even at low voltage (1.8 V Min.). Like all the devices in the S1C Family, this microcomputer has low current consumption (1.7 µA at standby mode)*4.
The S1C88848 also contains the SVD circuit for detecting drop of battery voltage, and is most suitable for remote controllers for home electric appliances.

1.1 Features

Table 1.1.1 lists the features of the S1C88848.

Table 1.1.1 Main features

Core CPU	S1C88 (MODEL3) CMOS 8-bit core CPU
Main (OSC3) oscillation circuit	Crystal oscillation/ceramic oscillation/CR oscillation*1 8.2 MHz (Max.) (start clock source)
Sub (OSC1) oscillation circuit	Crystal oscillation/CR oscillation*1 32.768 kHz (Typ.)
Instruction set	608 types (usable for multiplication and division instructions)
Min. instruction execution time	0.244 µsec/8.2 MHz (2-clock instructions)
Internal ROM capacity	48K bytes
Internal RAM capacity	1.5K bytes/RAM, 402 bytes/display memory
Input port	10 bits (2 bits can be configured for event counter external clock inputs) Internal pull-up resistors are available*1
Output port	5 bits (can be configured for buzzer*2, TOUT*2, FOUT*2 and infrared remote-control carrier*1 outputs) SEG40–SEG50 are usable as DC output ports*1
I/O port	8 bits (4 bits can be configured for serial interface inputs/outputs*2) Internal pull-up resistors are available*1
LCD driver	Dot matrix type (compatible with 5 × 8 or 5 × 5 fonts*2) 51 segments × 32 common*1, *2 66 segments × 17 common*1 67 segments × 16 common*1, *2 67 segments × 8 common*1 Built-in LCD power supply circuit (booster type, 5 or 4 potentials)
Remote controller	Infrared remote-control carrier output or DC output
Serial interface	1 ch. (optional clock synchronous system or asynchronous system)
Timer	Programmable timer: 16-bit × 2 ch. or 8-bit × 4 ch.*2, with event counter function Clock timer: 8-bit × 1 ch. Stopwatch timer: 8-bit × 1 ch.
Sound generator	Envelope function, equipped with volume control
Watchdog timer	Built-in
Supply voltage detection (SVD)	16 different voltage levels detectable (1.8–4.35 V)*2
Interrupt	External interrupt: Input interrupt 2 systems (3 types) Internal interrupt: Clock timer interrupt 1 system (4 types) Stopwatch timer interrupt 1 system (3 types) Programmable timer interrupt 2 systems (4 types) Serial interface interrupt 1 system (3 types) Remote-control output interrupt 1 system (1 type)
Supply voltage	1.8–5.5 V*3
Current consumption*4	SLEEP status: 1 µA (Typ.) HALT status (32 kHz crystal oscillation): 1.7 µA (Typ.) HALT status (8 MHz ceramic oscillation): 100 µA (Typ.) Run status (32 kHz crystal oscillation): 4 µA (Typ.) Run status (8 MHz ceramic oscillation): 700 µA (Typ.)
Supply form	QFP15-128pin or chip

*1 Mask option *2 Software selection *3 A supply voltage of less than 2.4 V affects the LCD contrast.

*4 After an initial reset, both OSC1 and OSC3 go ON and the CPU starts operating with the OSC3 clock. Furthermore, the remote controller operates with the OSC3 clock regardless of whether the REM output option is selected or not. When the remote controller is not used, it should be turned OFF in the initial routine that will be executed after an initial reset to reduce current consumption.

1.2 Block Diagram

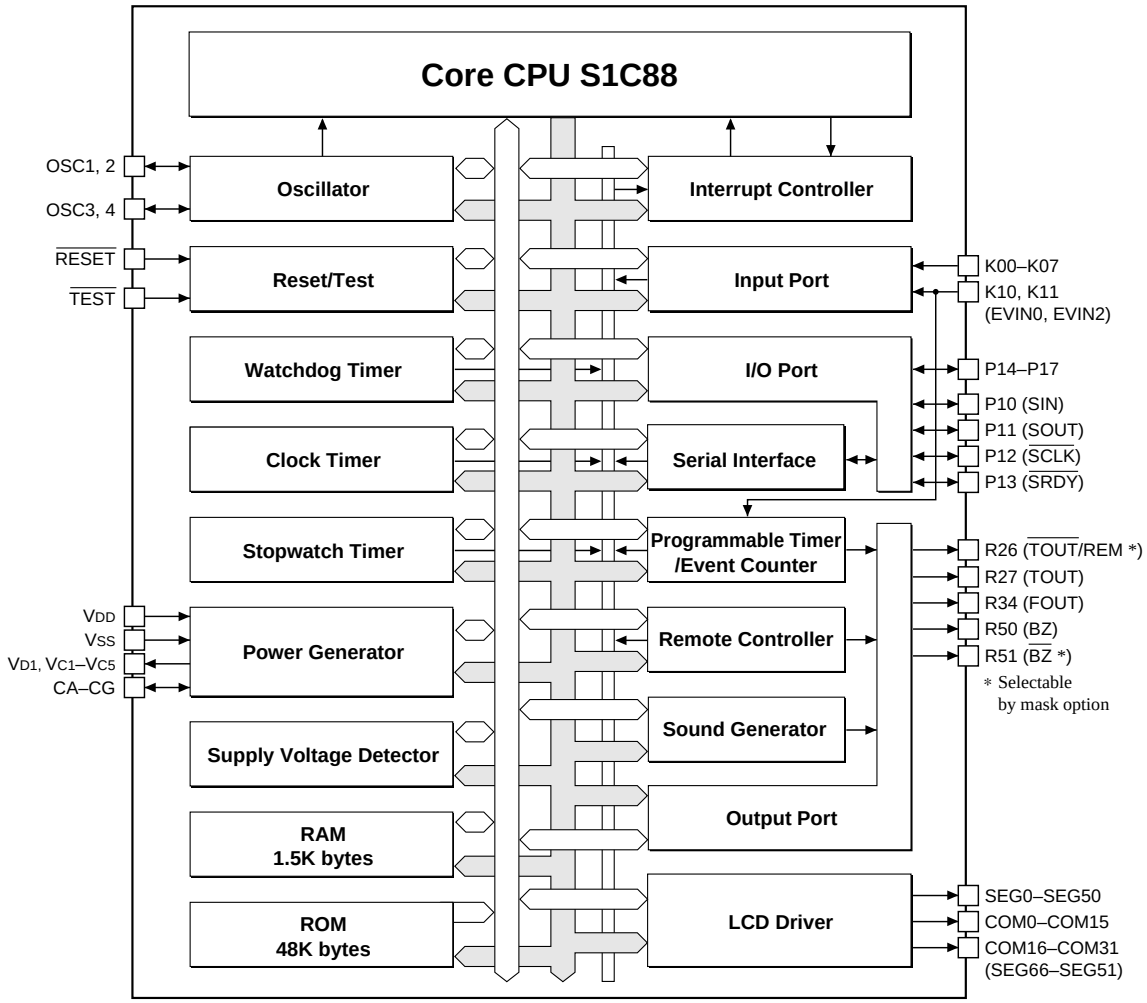
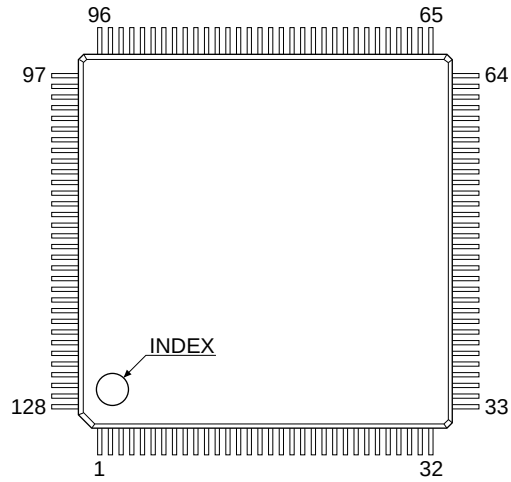


Fig. 1.2.1 Block diagram

1.3 Pins

1.3.1 Pin layout diagram

QFP15-128pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG11	33	SEG43	65	V_{C3}	97	R26/$\overline{TOUT}$/REM
2	SEG12	34	SEG44	66	V_{C2}	98	R27/TOUT
3	SEG13	35	SEG45	67	V_{C1}	99	R34/FOUT
4	SEG14	36	SEG46	68	OSC3	100	R50/BZ
5	SEG15	37	SEG47	69	OSC4	101	R51/$\overline{BZ}$
6	SEG16	38	SEG48	70	V_{D1}	102	COM0
7	SEG17	39	SEG49	71	V_{DD}	103	COM1
8	SEG18	40	SEG50	72	V_{SS}	104	COM2
9	SEG19	41	COM31/SEG51	73	OSC1	105	COM3
10	SEG20	42	COM30/SEG52	74	OSC2	106	COM4
11	SEG21	43	COM29/SEG53	75	$\overline{TEST}$	107	COM5
12	SEG22	44	COM28/SEG54	76	$\overline{RESET}$	108	COM6
13	SEG23	45	COM27/SEG55	77	K11/EVIN2	109	COM7
14	SEG24	46	COM26/SEG56	78	K10/EVIN0	110	COM8
15	SEG25	47	COM25/SEG57	79	K07	111	COM9
16	SEG26	48	COM24/SEG58	80	K06	112	COM10
17	SEG27	49	COM23/SEG59	81	K05	113	COM11
18	SEG28	50	COM22/SEG60	82	K04	114	COM12
19	SEG29	51	COM21/SEG61	83	K03	115	COM13
20	SEG30	52	COM20/SEG62	84	K02	116	COM14
21	SEG31	53	COM19/SEG63	85	K01	117	COM15
22	SEG32	54	COM18/SEG64	86	K00	118	SEG0
23	SEG33	55	COM17/SEG65	87	P17	119	SEG1
24	SEG34	56	COM16/SEG66	88	P16	120	SEG2
25	SEG35	57	N.C.	89	P15	121	SEG3
26	SEG36	58	CE *1	90	P14	122	SEG4
27	SEG37	59	CD *1	91	P13/$\overline{SRDY}$	123	SEG5
28	SEG38	60	CC	92	P12/$\overline{SCLK}$	124	SEG6
29	SEG39	61	CB	93	P11/SOUT	125	SEG7
30	SEG40	62	CA	94	P10/SIN	126	SEG8
31	SEG41	63	V_{C5}	95	CF *2	127	SEG9
32	SEG42	64	V_{C4}	96	CG *2	128	SEG10

N.C.: No Connection

∗1: N.C. when the LCD is driven with V_{C1} standard (1/4 bias) configuration.

∗2: N.C. when the LCD is driven with V_{C2} standard (1/5 bias) configuration.

Fig. 1.3.1.1 Pin layout

1.3.2 Pin description

Table 1.3.2.1 Pin description

Pin name	Pin No.	In/out	Function
V_{DD}	71	–	Power supply (+) terminal
V_{SS}	72	–	Power supply (GND) terminal
V_{D1}	70	–	Internal operating voltage output terminal
V_{C1}–V_{C5}	67–63	O	LCD drive voltage output terminal
CA–CG	62–58, 95, 96	–	LCD voltage boost/reduce-capacitor connection terminals
OSC1	73	I	OSC1 oscillation input terminal (select crystal or CR oscillation by mask option)
OSC2	74	O	OSC1 oscillation output terminal
OSC3	68	I	OSC3 oscillation input terminal (select crystal, ceramic or CR oscillation by mask option)
OSC4	69	O	OSC3 oscillation output terminal
K00–K07	86–79	I	Input port terminals (K00–K07)
K10/EVIN0	78	I	Input port terminal (K10) or event counter external clock input terminal (EVIN0)
K11/EVIN2	77	I	Input port terminal (K11) or event counter external clock input terminal (EVIN2)
R26/$\overline{\text{TOUT}}$/REM	97	O	Output port terminal (R26), programmable timer underflow signal inverted output terminal ($\overline{\text{TOUT}}$) or remote-control carrier output terminal (REM) (selectable by mask option)
R27/TOUT	98	O	Output port terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R34/FOUT	99	O	Output port terminal (R34) or clock output terminal (FOUT)
R50/BZ	100	O	Output port terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BZ}}$	101	O	Output port terminal (R51) or buzzer inverted output terminal ($\overline{\text{BZ}}$) (selectable by mask option)
P10/SIN	94	I/O	I/O port terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	93	I/O	I/O port terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	92	I/O	I/O port terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	91	I/O	I/O port terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14–P17	90–87	I/O	I/O port terminals (P14–P17)
COM0–COM15	102–117	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	56–41	O	LCD common output terminals or LCD segment output terminals COM16–COM31 (when 1/32 duty is selected) SEG66–SEG51 (when 1/16 or 1/8 duty is selected) COM16, SEG65–SEG51 (when 1/17 duty is selected)
SEG0–SEG39	118–128, 1–29	O	LCD segment output terminals
SEG40–SEG50	30–40	O	LCD segment output terminals or DC output terminals (selectable by mask option)
$\overline{\text{RESET}}$	76	I	Initial reset input terminal
$\overline{\text{TEST}}$ *1	75	I	Test input terminal

*1 $\overline{\text{TEST}}$ is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.

1.4 Mask Option

Mask options shown below are provided for the S1C88848. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog, that has been prepared as the development software tool of the S1C88848, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the winfog. Refer to the "S5U1C88000C Manual II" for details on the winfog.

S1C88848 optional specifications

(1) $\overline{\text{RESET}}$ terminal pull-up resistor

This mask option can select whether the pull-up resistor for the $\overline{\text{RESET}}$ terminal is used or not.

(2) External reset by simultaneous LOW input to the input port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 4.1.2, "Simultaneous LOW level input at input port terminals K00–K03", for details.

(3) OSC1 oscillation circuit

The specification of the OSC1 oscillation circuit can be selected from "Crystal oscillation" and "CR oscillation". Refer to Section 5.3.3, "OSC1 oscillation circuit", for details.

(4) OSC3 oscillation circuit

The specification of the OSC3 oscillation circuit can be selected from among three types: "Crystal oscillation", "Ceramic oscillation" and "CR oscillation". Refer to Section 5.3.4, "OSC3 oscillation circuit", for details.

(5) Input port pull-up resistor

This mask option can select whether the pull-up resistor for the input port terminal is used or not. It is possible to select for each bit of the input ports. Refer to Section 5.4, "Input Ports (K ports)", for details.

(6) R26, R51 output port specifications

The R26 port can be configured as a general-purpose output port, $\overline{\text{TOUT}}$ output port (TOUT inverted output) or REM (remoto-control carrier) output port.
The R51 port can be configured as a general-purpose output port or $\overline{\text{BZ}}$ output port (BZ inverted output). Refer to Section 5.5, "Output Ports (R ports)", for details.

(7) I/O port pull-up resistor

This mask option can select whether the pull-up resistor for the I/O port terminal (it works during input mode) is used or not. It is possible to select for each bit of the I/O ports. Refer to Section 5.6, "I/O Ports (P ports)", for details.

Since P10 to P13 are shared with the serial interface I/O terminals, the selected P10 and P12 terminal configuration is applied to the serial input (SIN) terminal and serial clock input terminal ($\overline{\text{SCLK}}$ in clock synchronous mode) when the serial interface is used. Refer to Section 5.7, "Serial Interface", for details.

(8) LCD drive duty

The drive duty for the built-in LCD driver can be selected from software switchable (between 1/32 and 1/16), fixed at 1/17 and fixed at 1/8. Refer to Section 5.11, "LCD Controller", for details.

(9) LCD power supply

Either the internal power supply or an external power supply can be selected as the LCD system power source. Furthermore, when using the internal power supply, the LCD drive voltage can be set for a 4.5 V panel or a 5.5 V panel and the drive bias to 1/5 or 1/4. Refer to Section 5.11, "LCD Controller", for details.

(10) SEG40–SEG50 port specifications

The SEG40 to SEG50 ports can be configured as LCD segment output ports or general-purpose output ports. Refer to Section 5.11, "LCD Controller", for details of the LCD segment output, and Section 5.5, "Output Ports (R ports)", for details of the DC output.

Option list

The following options can be set for the S1C88848. Multiple specifications are available in each option item as indicated in the Option List. Select the specifications that meet the target system and check the appropriate box.

The option selection is done interactively on the screen during winfog execution, using this option list as reference.

S5U1C88000P option list

A OSC1 SYSTEM CLOCK

☐ 1. Internal Clock
☐ 2. User Clock

B OSC3 SYSTEM CLOCK

☐ 1. Internal Clock
☐ 2. User Clock

S1C88848 mask option list (1/2)

1 OSC1 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. CR

2 OSC3 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. Ceramic
☐ 3. CR

3 MULTIPLE KEY ENTRY RESET

• Combination ... ☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

4 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K04	☐ 1. With Resistor	☐ 2. Gate Direct
• K05	☐ 1. With Resistor	☐ 2. Gate Direct
• K06	☐ 1. With Resistor	☐ 2. Gate Direct
• K07	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• $\overline{\text{RESET}}$	☐ 1. With Resistor	☐ 2. Gate Direct

5 I/O PORT PULL UP RESISTOR

• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct
• P14	☐ 1. With Resistor	☐ 2. Gate Direct
• P15	☐ 1. With Resistor	☐ 2. Gate Direct
• P16	☐ 1. With Resistor	☐ 2. Gate Direct
• P17	☐ 1. With Resistor	☐ 2. Gate Direct

S1C88848 mask option list (2/2)

6 LCD DRIVE DUTY

☐ 1. 1/32 & 1/16 Duty
☐ 2. 1/17 Duty
☐ 3. 1/8 Duty

7 LCD POWER SUPPLY

☐ 1. Internal TYPE A (V_{C2} Standard, 1/5 Bias, 4.5 V)
☐ 2. External
☐ 3. Internal TYPE B (V_{C2} Standard, 1/5 Bias, 5.5 V)
☐ 4. Internal TYPE D (V_{C1} Standard, 1/4 Bias, 4.5 V)

8 R51 OUTPUT PORT SPECIFICATION

☐ 1. With $\overline{BZ}$ (Use)
☐ 2. Without $\overline{BZ}$ (Not Use)

9 R26 OUTPUT PORT SPECIFICATION *1

☐ 1. REM Output
☐ 2. $\overline{TOUT}$ Output
☐ 3. DC Output

10 SEG40–SEG50 PORT SPECIFICATIONS

• SEG40	☐ 1. SEG Output	☐ 2. DC Output
• SEG41	☐ 1. SEG Output	☐ 2. DC Output
• SEG42	☐ 1. SEG Output	☐ 2. DC Output
• SEG43	☐ 1. SEG Output	☐ 2. DC Output
• SEG44	☐ 1. SEG Output	☐ 2. DC Output
• SEG45	☐ 1. SEG Output	☐ 2. DC Output
• SEG46	☐ 1. SEG Output	☐ 2. DC Output
• SEG47	☐ 1. SEG Output	☐ 2. DC Output
• SEG48	☐ 1. SEG Output	☐ 2. DC Output
• SEG49	☐ 1. SEG Output	☐ 2. DC Output
• SEG50	☐ 1. SEG Output	☐ 2. DC Output

*1 After an initial reset, the remote controller operates with the OSC3 clock regardless of whether the REM output option is selected or not. When the remote controller is not used, it should be turned OFF in the initial routine that will be executed after an initial reset to reduce current consumption.

2 POWER SUPPLY

In this section, we will explain the operating voltage and the configuration of the internal power supply circuit of the S1C88848.

2.1 Operating Voltage

The S1C88848 operating power voltage is as follows:

V_{DD} = 1.8 V to 5.5 V

Note, however, a supply voltage of less than 2.4 V affects the LCD contrast. (See Note below.)

2.2 Internal Power Supply Circuit

The S1C88848 incorporates the power supply circuit shown in Figure 2.2.1. When voltage within the range described above is supplied to V_{DD} (+) and V_{SS} (GND), all the voltages needed for the internal circuit are generated internally in the IC.

Roughly speaking, the power supply circuit is divided into two sections.

The internal logic voltage regulator generates the operating voltage <V_{D1}> for driving the internal logic circuits and the OSC3 and OSC1 oscillation circuits.

The LCD system power supply circuit generates the LCD drive voltages <V_{C1}> to <V_{C5}>. In 1/5 bias mode, V_{C1} is generated by halving V_{C2} output from the LCD system voltage regulator and V_{C3} to V_{C5} are generated by boosting V_{C2}. These five voltages can be supplied from outside the IC by mask option.

Furthermore, 1/4 bias drive can be selected by mask option. In this case, the V_{C2} voltage level becomes equal to the V_{C3} voltage level. When 1/4 bias is selected, V_{C2} to V_{C5} are generated by boosting V_{C1}.
See Chapter 7, "ELECTRICAL CHARACTERISTICS" for the voltage values.
In the S1C88848, the LCD drive voltage is supplied to the built-in LCD driver which drives the LCD panel connected to the SEG and COM terminals.

Notes:
- *Do not use the V_{C1}–V_{C5} outputs for driving external circuits.*
- *When the supply voltage is 2.4 V or less ($V_{DD} \leq 2.4$), the V_{C2} voltage generated is almost the same as V_{DD}. Since the V_{C2} voltage affects the LCD contrast, V_{DD} must be higher than 2.4 V to obtain stable display quality.*
  In the 1/4 bias configuration, V_{C1} does not exceed 1.4 V because V_{C2}–V_{C5} voltages are generated by boosting the V_{C1} voltage. Thus the supply voltage within the range of 1.8–5.5 V does not affects the LCD contrast in the 1/4 bias configuration.

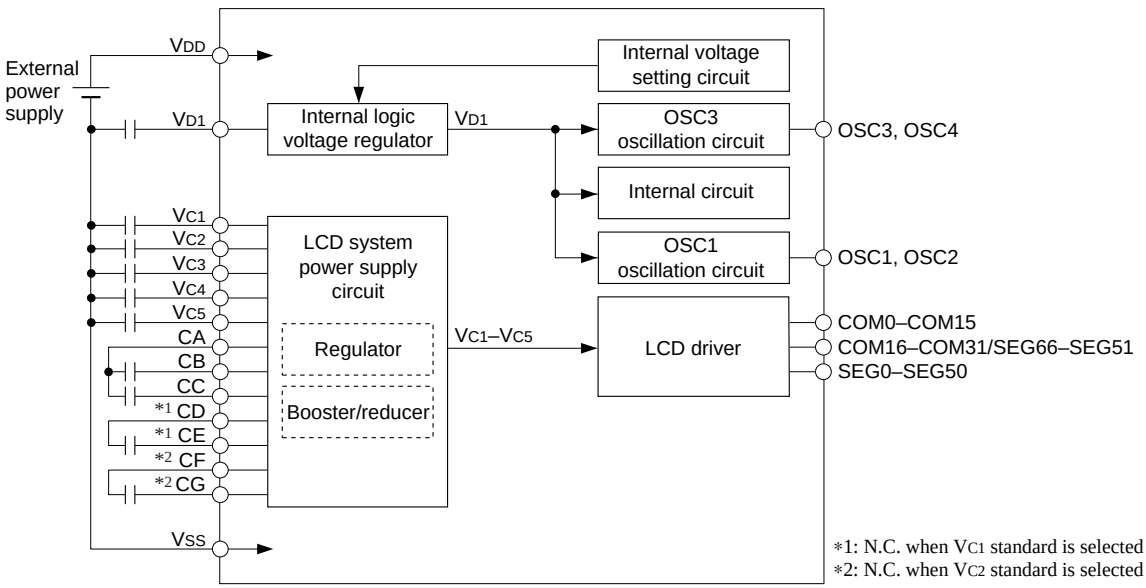


Fig. 2.2.1 Configuration of power supply circuit

3 CPU AND MEMORY CONFIGURATION

In this section, we will explain the CPU and memory configuration.

3.1 CPU

The S1C88848 utilize the S1C88 8-bit core CPU whose resistor configuration, command set, etc. are virtually identical to other units in the family of processors incorporating the S1C88.

See the "S1C88 Core CPU Manual" for the S1C88.

The S1C88848 supports Model 3/minimum mode of the S1C88 CPU which allows accessing of the internal memory mapped within the physical space from 000000H to 00FFFFH.

3.2 Internal Memory

The S1C88848 is equipped with internal ROM and RAM as shown in Figure 3.2.1.

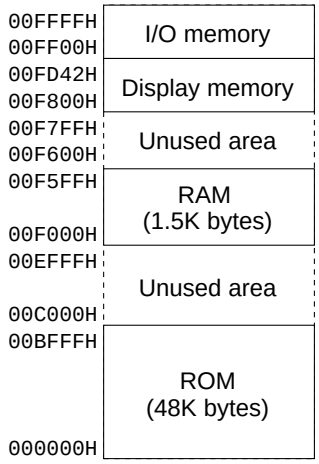


Fig. 3.2.1 Internal memory map

3.2.1 ROM

The internal ROM capacity is shown below.

Capacity: 48K bytes
Address: 000000H to 00BFFFH

3.2.2 RAM

The internal RAM capacity is shown below.

Capacity: 1.5K bytes
Address: 00F000H to 00F5FFH

3.2.3 I/O memory

A memory mapped I/O method is employed in the S1C88848 for interfacing with internal peripheral circuit. Peripheral circuit control bits and data register are arranged in data memory space. Control and data exchange are conducted via normal memory access. The I/O memory is arranged from address 00FF00H to address 00FFFFH. See Section 5.1, "I/O Memory Map", for details of the I/O memory.

3.2.4 Display memory

The S1C88848 is equipped with an internal display memory which stores a display data for LCD driver.
The display memory is arranged from address 00F800H to address 00FD42H (including the unused area). See Section 5.11, "LCD Controller", for details of the display memory.

3.3 Exception Processing Vectors

Address 000000H to address 000029H in the program area of the S1C88848 is assigned as exception processing vectors. Furthermore, from address 00002CH to address 0000FFH, software interrupt vectors are assignable to any two bytes which begin with an even address.
Table 3.3.1 lists the vector addresses and the exception processing factors to which they correspond.

Table 3.3.1 Vector addresses and exception processing factors

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	Programmable timer 1 interrupt	
000008H	Programmable timer 0 interrupt	
00000AH	K10, K11 input interrupt	
00000CH	K04–K07 input interrupt	
00000EH	K00–K03 input interrupt	
000010H	Serial I/F error interrupt	
000012H	Serial I/F receiving complete interrupt	
000014H	Serial I/F transmitting complete interrupt	
000016H	Stopwatch timer 100 Hz interrupt	
000018H	Stopwatch timer 10 Hz interrupt	
00001AH	Stopwatch timer 1 Hz interrupt	
00001CH	Clock timer 32 Hz interrupt	
00001EH	Clock timer 8 Hz interrupt	
000020H	Clock timer 2 Hz interrupt	
000022H	Clock timer 1 Hz interrupt	
000024H	Remote-control carrier output interrupt	
000026H	Programmable timer 3 interrupt	↓
000028H	Programmable timer 2 interrupt	Low
00002AH	System reserved (cannot be used)	No priority rating
00002CH : 0000FEH	Software interrupt	

For each vector address and the address after it, the start address of the exception processing routine is written into the subordinate and super ordinate sequence. When an exception processing factor is generated, the exception processing routine is executed starting from the recorded address.

When multiple exception processing factors are generated at the same time, execution starts with the highest priority item.
The priority sequence shown in Table 3.3.1 assumes that the interrupt priority levels are all the same. The interrupt priority levels can be set by software in each system. (See Section 5.15 "Interrupt and Standby Status".)

Note: For exception processing other than reset, SC (system condition flag) and PC (program counter) are evacuated to the stack and branches to the exception processing routines. Consequently, when returning to the main routine from exception processing routines, please use the RETE instruction.

See the "S1C88 Core CPU Manual" for information on CPU operations when an exception processing factor is generated.

3.4 CC (Customized Condition Flag)

The S1C88848 does not use the customized condition flag (CC) in the core CPU. Accordingly, it cannot be used as a branching condition for the conditional branching instruction (JRS, CARS).

4 INITIAL RESET

Initial reset in the S1C88848 is required in order to initialize circuits. This chapter describes initial reset factors and the initial settings for internal registers.

4.1 Initial Reset Factors

There are two initial reset factors for the S1C88848 as shown below.

(1) $\overline{\text{RESET}}$ terminal
(2) Simultaneous LOW level input at input port terminals K00–K03.

Figure 4.1.1 shows the configuration of the initial reset circuit.

The CPU and peripheral circuits are initialized by means of initial reset factors. When the factor is canceled, the CPU commences reset exception processing. (See "S1C88 Core CPU Manual".)

When this occurs, reset exception processing vectors, Bank 0, 000000H–000001H from program memory are read out and the program (initialization routine) which begins at the readout address is executed.

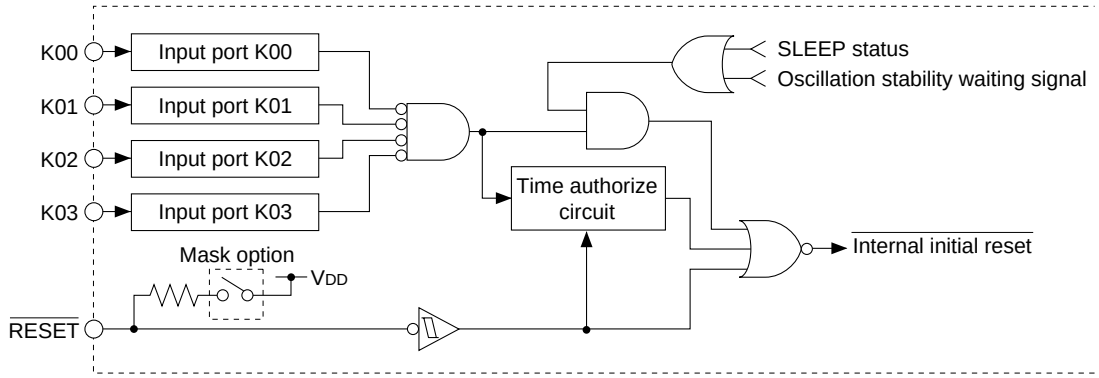


Fig. 4.1.1 Configuration of initial reset circuit

4.1.1 $\overline{\text{RESET}}$ terminal

Initial reset can be done by executed externally inputting a LOW level to the $\overline{\text{RESET}}$ terminal.
Be sure to maintain the $\overline{\text{RESET}}$ terminal at LOW level for the regulation time after the power on to assure the initial reset.
In addition, be sure to use the $\overline{\text{RESET}}$ terminal for the first initial reset after the power is turned on.
The $\overline{\text{RESET}}$ terminal is equipped with a pull-up resistor. You can select whether or not to use by mask option.

4.1.2 Simultaneous LOW level input at input port terminals K00–K03

Another way of executing initial reset externally is to input a LOW level simultaneously to the input ports (K00–K03) selected by mask option.
Since there is a built-in time authorize circuit, be sure to maintain the designated input port terminal at LOW level for two seconds (when the oscillation frequency fOSC1 = 32.768 kHz) or more to perform the initial reset by means of this function.
However, the time authorize circuit is bypassed during the SLEEP (standby) status and oscillation stabilization waiting period, and initial reset is executed immediately after the simultaneous LOW level input to the designated input ports.
The combination of input ports (K00–K03) that can be selected by mask option are as follows:
(1) Not use
(2) K00 & K01
(3) K00 & K01 & K02
(4) K00 & K01 & K02 & K03

For instance, if mask option (4) "K00 & K01 & K02 & K03" is selected, initial reset will take place when the input level at input ports K00–K03 is simultaneously LOW.
When using this function, make sure that the designated input ports do not simultaneously switch to LOW level while the system is in normal operation.

4.1.3 Initial reset sequence

After cancellation of the LOW level input to the $\overline{\text{RESET}}$ terminal, when the power is turned on, the start-up of the CPU is held back until the oscillation stabilization waiting time (128 / fOSC1 sec.) has elapsed. Figure 4.1.3.1 shows the operating sequence following initial reset release.

Also, when using the initial reset by simultaneous LOW level input into the input port, you should be careful of the following points.

(1) During SLEEP status, since the time authorization circuit is bypassed, an initial reset is triggered immediately after a LOW level simultaneous input value. In this case, the CPU starts after waiting the oscillation stabilization time, following cancellation of the LOW level simultaneous input.

(2) Other than during SLEEP status, an initial reset will be triggered 1–2 seconds after a LOW level simultaneous input. In this case, since a reset differential pulse (256 / fOSC1 sec.) is generated within the S1C88848, the CPU will start even if the LOW level simultaneous input status is not canceled.

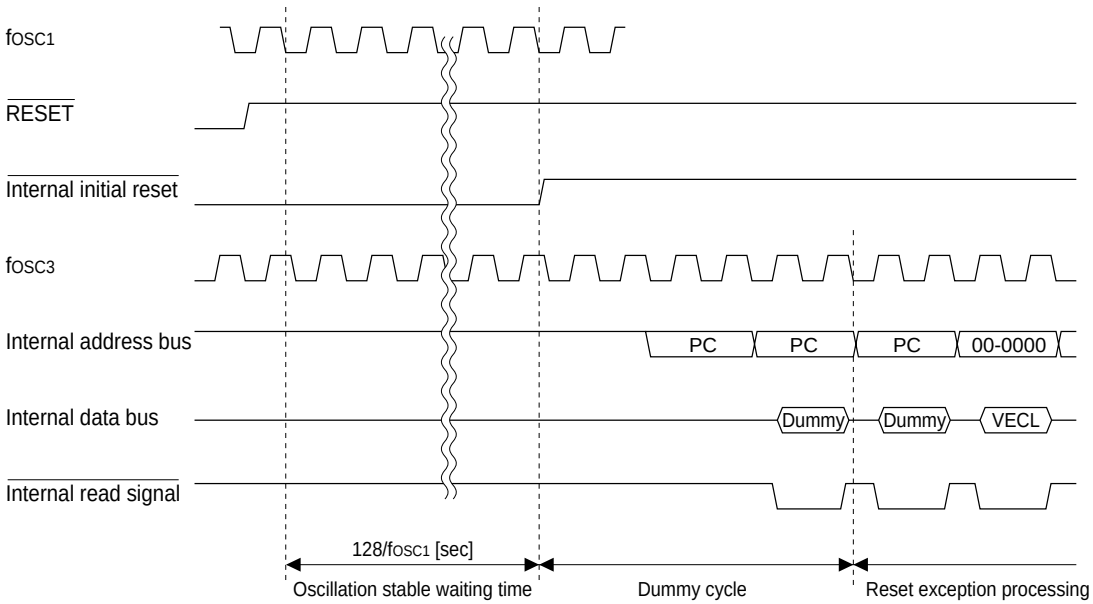


Fig. 4.1.3.1 Initial reset sequence

4.2 Initial Settings After Initial Reset

The CPU internal registers are initialized as follows during initial reset.

Table 4.2.1 Initial settings

Register name	Code	Bit length	Setting value
Data register A	A	8	Undefined
Data register B	B	8	Undefined
Index (data) register L	L	8	Undefined
Index (data) register H	H	8	Undefined
Index register IX	IX	16	Undefined
Index register IY	IY	16	Undefined
Program counter	PC	16	Undefined*
Stack pointer	SP	16	Undefined
Base register	BR	8	Undefined
Zero flag	Z	1	0
Carry flag	C	1	0
Overflow flag	V	1	0
Negative flag	N	1	0
Decimal flag	D	1	0
Unpack flag	U	1	0
Interrupt flag 0	I0	1	1
Interrupt flag 1	I1	1	1
New code bank register	NB	8	01H
Code bank register	CB	8	Undefined*
Expand page register	EP	8	00H
Expand page register for IX	XP	8	00H
Expand page register for IY	YP	8	00H

* Reset exception processing loads the preset values stored in 0 bank, 000000H–000001H into the PC. At the same time, 01H of the NB initial value is loaded into CB.

Initialize the registers which are not initialized at initial reset using software.

Since the internal RAM and display memory are not initialized at initial reset, be sure to initialize using software.

The respectively stipulated initializations are done for internal peripheral circuits. If necessary, the initialization should be done using software.
For initial value at initial reset, see the sections on the I/O memory map and peripheral circuit descriptions in the following chapter of this Manual.

5 PERIPHERAL CIRCUITS AND THEIR OPERATION

The peripheral circuits of the S1C88848 is interfaced with the CPU by means of the memory mapped I/O method. For this reason, just as with other memory access operations, peripheral circuits can be controlled by manipulating I/O memory. Below is a description of the operation and control method for each individual peripheral circuit.

5.1 I/O Memory Map

Table 5.1.1(a) I/O Memory map (00FF00H–00FF10H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00	D7	BSMD1	General-purpose register	1	0	0	R/W	Reserved register (Note)
	D6	BSMD0	General-purpose register			0	R/W	
	D5	CEMD1	General-purpose register			1	R/W	
	D4	CEMD0	General-purpose register			1	R/W	
	D3	CE3	General-purpose register			0	R/W	
	D2	CE2	General-purpose register			0	R/W	
	D1	CE1	General-purpose register			0	R/W	
	D0	CE0	General-purpose register			0	R/W	
00FF01	D7	SPP7	General-purpose register	1	0	0	R/W	Reserved register (Note)
	D6	SPP6	General-purpose register			0	R/W	
	D5	SPP5	General-purpose register			0	R/W	
	D4	SPP4	General-purpose register			0	R/W	
	D3	SPP3	General-purpose register			0	R/W	
	D2	SPP2	General-purpose register			0	R/W	
	D1	SPP1	General-purpose register			0	R/W	
	D0	SPP0	General-purpose register			0	R/W	
00FF02	D7	EBR	General-purpose register	1	0	0	R/W	Reserved register
	D6	WT2	General-purpose register			0	R/W	
	D5	WT1	General-purpose register			0	R/W	
	D4	WT0	General-purpose register			0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	1	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	1	R/W	
	D1	VD1C1	General-purpose register	1	0	0	R/W	Reserved register
	D0	VD1C0	General-purpose register			0	R/W	
00FF10	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	LCCLK	General-purpose register	1	0	0	R/W	Reserved register
	D3	LCFRM	General-purpose register			0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	General-purpose register	1	0	0	R/W	Reserved register

*1 When 1/8 or 1/17 duty has been selected by mask option, setting of this register becomes invalid.

Note) When debugging using the S1C88 Family debugging tools ICE (S5U1C88000H5) and Peripheral Circuit Board (S5U1C88000P), all the interrupts including $\overline{\text{NMI}}$ are disabled until values are written to addresses "00FF00H" and "00FF01H".

Table 5.1.1(b) I/O Memory map (00FF11H–00FF21H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF11	D7	–	–	–	–	–		"0" when being read
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	
00FF12	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	SVDDT	SVD data	Low	Normal	0	R	
	D4	SVDON	SVD circuit On/Off control	On	Off	0	R/W	
	D3	SVDS3	SVD criteria voltage setting SVDS3 SVDS2 SVDS1 SVDS0 Voltage 1 1 1 1 4.35 V 1 1 1 0 4.17 V 1 1 0 1 4.00 V 1 1 0 0 3.83 V 1 0 1 1 3.67 V 1 0 1 0 3.50 V 1 0 0 1 3.33 V 1 0 0 0 3.17 V 0 1 1 1 3.00 V 0 1 1 0 2.83 V 0 1 0 1 2.67 V 0 1 0 0 2.50 V 0 0 1 1 2.33 V 0 0 1 0 2.17 V 0 0 0 1 2.00 V 0 0 0 0 1.83 V			0	R/W	
	D2	SVDS2				0	R/W	
	D1	SVDS1				0	R/W	
	D0	SVDS0				0	R/W	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF21	D7	PREM1	REM carrier interrupt priority register	PREM1 PREM0 PPT3 PPT2 PPT1 PPT0 PK11 PK10 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PREM0				0	R/W	
	D5	PPT3	Programmable timer 2–3 interrupt priority register			0	R/W	
	D4	PPT2				0	R/W	
	D3	PPT1	Programmable timer 0–1 interrupt priority register			0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10–K11 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	

Table 5.1.1(c) I/O Memory map (00FF22H–00FF27H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10–K11 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10–K11 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag			0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	
00FF26	D7	EPT3	Programmable timer 3 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT2	Programmable timer 2 interrupt enable register			0	R/W	
	D5	EREM	REM carrier interrupt enable register			0	R/W	
	D4	REMC	REM carrier generation On/Off	On	Off	1	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF27	D7	FPT3	Programmable timer 3 interrupt factor flag	(R) Generated	(R) Not generated	0	R/W	
	D6	FPT2	Programmable timer 2 interrupt factor flag			0	R/W	
	D5	FREM	REM carrier interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D4	REMSO	Forced REM output On/Off	On	Off	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

Table 5.1.1(d) I/O Memory map (00FF28H–00FF30H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF28	D7	–	–	–	–	–		"0" when being read
	D6	RT1	REM τ cycle (division ratio) setting RT1 RT0 Division ratio 1 1 1/32 1 0 1/20 0 1 1/16 0 0 1/12			0	R/W	
	D5	RT0				0	R/W	
	D4	RCDIV	REM carrier cycle setting	fOSC3/96	fOSC3/64	0	R/W	
	D3	RCDUTY3	REM carrier duty setting RCDUTYx Duty 3 2 1 0 (RCDIV = 0) (RCDIV = 1) 1 0 1 1 – 12/24 1 0 1 0 – 11/24 1 0 0 1 – 10/24 1 0 0 0 – 9/24 0 1 1 1 – 8/24 0 1 1 0 – 7/24 0 1 0 1 – 6/24 0 1 0 0 – 5/24 0 0 1 1 4/8 4/24 0 0 1 0 3/8 3/24 0 0 0 1 2/8 2/24 0 0 0 0 1/8 1/24			0	R/W	∗2
	D2	RCDUTY2				0	R/W	
	D1	RCDUTY1				0	R/W	
	D0	RCDUTY0				0	R/W	
00FF29	D7	RIC3	REM interrupt counter setting			–	W	∗1
	D6	RIC2	(0–0EH: 0–14τ clock)			–	W	Constantly "0" when
	D5	RIC1	The counter operates one-time only by writing			–	W	being read
	D4	RIC0	and is reset to 0FH after counting.			–	W	
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		Constantly "0" when
	D1	–	–	–	–	–		being read
	D0	–	–	–	–	–		
00FF2A	D7	ROUT1	REM output duration setting (0–3: 0–3τ)			0	R/W	∗1
	D6	ROUT0	Operates one-time only by writing.			0	R/W	
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		Constantly "0" when
	D2	–	–	–	–	–		being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF30	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	MODE160	8/16-bit mode selection (timer 0/1)	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	fOSC3	fOSC1	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	fOSC3	fOSC1	0	R/W	

∗1 Effective only for hardware timer method. Writing is not allowed in software timer method.

∗2 When RCDIV = "1", the REM signal is not output if RCDUTYx is "1100" or more.
When RCDIV = "0", settings RCDUTYx to "0100" or more are same as RCDUTYx = "0011".

Table 5.1.1(e) I/O Memory map (00FF31H–00FF35H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF31	D7	EVCNT0	Timer 0 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL0	Timer 0 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 0 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL0	Timer 0 pulse polarity selection: Down count timing in event counter mode	Rising edge of K10 input	Falling edge of K10 input	0	R/W	
			Timer 0 pulse polarity selection: In pulse width measurement mode	High level measurement for K10 input	Low level measurement for K10 input			
	D4	PSC01	Timer 0 prescaler dividing ratio selection			0	R/W	
	D3	PSC00	PSC01 = 1, PSC00 = 1: Source clock / 64			0	R/W	
			PSC01 = 1, PSC00 = 0: Source clock / 16					
			PSC01 = 0, PSC00 = 1: Source clock / 4					
			PSC01 = 0, PSC00 = 0: Source clock / 1					
	D2	CONT0	Timer 0 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET0	Timer 0 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN0	Timer 0 Run/Stop control	Run	Stop	0	R/W	
00FF32	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC11	Timer 1 prescaler dividing ratio selection			0	R/W	
	D3	PSC10	PSC11 = 1, PSC10 = 1: Source clock / 64			0	R/W	
			PSC11 = 1, PSC10 = 0: Source clock / 16					
			PSC11 = 0, PSC10 = 1: Source clock / 4					
			PSC11 = 0, PSC10 = 0: Source clock / 1					
	D2	CONT1	Timer 1 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET1	Timer 1 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN1	Timer 1 Run/Stop control	Run	Stop	0	R/W	
00FF33	D7	RLD07	Timer 0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD06	Timer 0 reload data D6			1	R/W	
	D5	RLD05	Timer 0 reload data D5			1	R/W	
	D4	RLD04	Timer 0 reload data D4			1	R/W	
	D3	RLD03	Timer 0 reload data D3			1	R/W	
	D2	RLD02	Timer 0 reload data D2			1	R/W	
	D1	RLD01	Timer 0 reload data D1			1	R/W	
	D0	RLD00	Timer 0 reload data D0 (LSB)			1	R/W	
00FF34	D7	RLD17	Timer 1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD16	Timer 1 reload data D6			1	R/W	
	D5	RLD15	Timer 1 reload data D5			1	R/W	
	D4	RLD14	Timer 1 reload data D4			1	R/W	
	D3	RLD13	Timer 1 reload data D3			1	R/W	
	D2	RLD12	Timer 1 reload data D2			1	R/W	
	D1	RLD11	Timer 1 reload data D1			1	R/W	
	D0	RLD10	Timer 1 reload data D0 (LSB)			1	R/W	
00FF35	D7	PTD07	Timer 0 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD06	Timer 0 counter data D6			1	R	
	D5	PTD05	Timer 0 counter data D5			1	R	
	D4	PTD04	Timer 0 counter data D4			1	R	
	D3	PTD03	Timer 0 counter data D3			1	R	
	D2	PTD02	Timer 0 counter data D2			1	R	
	D1	PTD01	Timer 0 counter data D1			1	R	
	D0	PTD00	Timer 0 counter data D0 (LSB)			1	R	

Table 5.1.1(f) I/O Memory map (00FF36H–00FF3BH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF36	D7	PTD17	Timer 1 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD16	Timer 1 counter data D6			1	R	
	D5	PTD15	Timer 1 counter data D5			1	R	
	D4	PTD14	Timer 1 counter data D4			1	R	
	D3	PTD13	Timer 1 counter data D3			1	R	
	D2	PTD12	Timer 1 counter data D2			1	R	
	D1	PTD11	Timer 1 counter data D1			1	R	
	D0	PTD10	Timer 1 counter data D0 (LSB)			1	R	
00FF38	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE162	8/16-bit mode selection (timer 2/3)	16-bit x 1	8-bit x 2	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	CKSEL3	Prescaler 3 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL2	Prescaler 2 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF39	D7	EVCNT2	Timer 2 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL2	Timer 2 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 2 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL2	Timer 2 pulse polarity selection: Down count timing in event counter mode	Rising edge of K11 input	Falling edge of K11 input	0	R/W	
			Timer 2 pulse polarity selection: In pulse width measurement mode	High level measurement for K11 input	Low level measurement for K11 input			
	D4	PSC21	Timer 2 prescaler dividing ratio selection			0	R/W	
	D3	PSC20	PSC21 = 1, PSC20 = 1: Source clock / 64 PSC21 = 1, PSC20 = 0: Source clock / 16 PSC21 = 0, PSC20 = 1: Source clock / 4 PSC21 = 0, PSC20 = 0: Source clock / 1			0	R/W	
	D2	CONT2	Timer 2 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET2	Timer 2 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN2	Timer 2 Run/Stop control	Run	Stop	0	R/W	
00FF3A	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC31	Timer 3 prescaler dividing ratio selection			0	R/W	
	D3	PSC30	PSC31 = 1, PSC30 = 1: Source clock / 64 PSC31 = 1, PSC30 = 0: Source clock / 16 PSC31 = 0, PSC30 = 1: Source clock / 4 PSC31 = 0, PSC30 = 0: Source clock / 1			0	R/W	
	D2	CONT3	Timer 3 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET3	Timer 3 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN3	Timer 3 Run/Stop control	Run	Stop	0	R/W	
00FF3B	D7	RLD27	Timer 2 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD26	Timer 2 reload data D6			1	R/W	
	D5	RLD25	Timer 2 reload data D5			1	R/W	
	D4	RLD24	Timer 2 reload data D4			1	R/W	
	D3	RLD23	Timer 2 reload data D3			1	R/W	
	D2	RLD22	Timer 2 reload data D2			1	R/W	
	D1	RLD21	Timer 2 reload data D1			1	R/W	
	D0	RLD20	Timer 2 reload data D0 (LSB)			1	R/W	

Table 5.1.1(g) I/O Memory map (00FF3CH–00FF41H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF3C	D7	RLD37	Timer 3 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD36	Timer 3 reload data D6			1	R/W	
	D5	RLD35	Timer 3 reload data D5			1	R/W	
	D4	RLD34	Timer 3 reload data D4			1	R/W	
	D3	RLD33	Timer 3 reload data D3			1	R/W	
	D2	RLD32	Timer 3 reload data D2			1	R/W	
	D1	RLD31	Timer 3 reload data D1			1	R/W	
	D0	RLD30	Timer 3 reload data D0 (LSB)			1	R/W	
00FF3D	D7	PTD27	Timer 2 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD26	Timer 2 counter data D6			1	R	
	D5	PTD25	Timer 2 counter data D5			1	R	
	D4	PTD24	Timer 2 counter data D4			1	R	
	D3	PTD23	Timer 2 counter data D3			1	R	
	D2	PTD22	Timer 2 counter data D2			1	R	
	D1	PTD21	Timer 2 counter data D1			1	R	
	D0	PTD20	Timer 2 counter data D0 (LSB)			1	R	
00FF3E	D7	PTD37	Timer 3 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD36	Timer 3 counter data D6			1	R	
	D5	PTD35	Timer 3 counter data D5			1	R	
	D4	PTD34	Timer 3 counter data D4			1	R	
	D3	PTD33	Timer 3 counter data D3			1	R	
	D2	PTD32	Timer 3 counter data D2			1	R	
	D1	PTD31	Timer 3 counter data D1			1	R	
	D0	PTD30	Timer 3 counter data D0 (LSB)			1	R	
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 0 0 0 f_{OSC1} / 1 0 0 1 f_{OSC1} / 2 0 1 0 f_{OSC1} / 4 0 1 1 f_{OSC1} / 8 1 0 0 f_{OSC3} / 1 1 0 1 f_{OSC3} / 2 1 1 0 f_{OSC3} / 4 1 1 1 f_{OSC3} / 8			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when being read
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz			0	R	
	D5	TMD5	Clock timer data 4 Hz			0	R	
	D4	TMD4	Clock timer data 8 Hz			0	R	
	D3	TMD3	Clock timer data 16 Hz			0	R	
	D2	TMD2	Clock timer data 32 Hz			0	R	
	D1	TMD1	Clock timer data 64 Hz			0	R	
	D0	TMD0	Clock timer data 128 Hz			0	R	

Table 5.1.1(h) I/O Memory map (00FF42H–00FF45H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data			–	R	
	D6	SWD6				–	R	
	D5	SWD5	BCD (1/10 sec)			–	R	
	D4	SWD4				–	R	
	D3	SWD3	Stopwatch timer data			–	R	
	D2	SWD2				–	R	
	D1	SWD1	BCD (1/100 sec)			–	R	
	D0	SWD0				–	R	
00FF44	D7	–	–	–	–	–		Constantly "0" when being read
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*1
	D0	BZON	Buzzer output control	On	Off	0	R/W	
00FF45	D7	–	–	–	–	–		"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection			0	R/W	
	D5	DUTY1				0	R/W	
	D4	DUTY0				0	R/W	
	D3	–	–	–	–	–		"0" when being read
	D2	BZFQ2	Buzzer frequency selection			0	R/W	
	D1	BZFQ1				0	R/W	
	D0	BZFQ0				0	R/W	

DUTY2–0 / Buzzer frequency (Hz)

2	1	0	4096.0 / 2048.0	3276.8 / 1638.4	2730.7 / 1365.3	2340.6 / 1170.3
0	0	0	8/16	8/20	12/24	12/28
0	0	1	7/16	7/20	11/24	11/28
0	1	0	6/16	6/20	10/24	10/28
0	1	1	5/16	5/20	9/24	9/28
1	0	0	4/16	4/20	8/24	8/28
1	0	1	3/16	3/20	7/24	7/28
1	1	0	2/16	2/20	6/24	6/28
1	1	1	1/16	1/20	5/24	5/28

BZFQ2	BZFQ1	BZFQ0	Frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

*1 Reset to "0" during one-shot output.

Table 5.1.1(i) I/O Memory map (00FF48H–00FF51H)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR	Parity enable register		With parity	Non parity	0	R/W	Only for
	D5	PMD	Parity mode selection		Odd	Even	0	R/W	asynchronous mode
	D4	SCS1	Clock source selection SCS1 SCS0 Clock source 1 1 Programmable timer				0	R/W	In the clock synchronous slave mode, external clock is
	D3	SCS0	1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16				0	R/W	selected.
	D2	SMD1	Serial I/F mode selection SMD1 SMD0 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD0	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF	Serial I/F enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER	Framing error flag	R	Error	No error	0	R/W	Only for
				W	Reset (0)	No operation			asynchronous mode
	D5	PER	Parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER	Overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG	Receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN	Receive enable		Enable	Disable	0	R/W	
	D1	TXTRG	Transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN	Transmit enable		Enable	Disable	0	R/W	
00FF4A	D7	TRXD7	Transmit/Receive data D7 (MSB)		High	Low	X	R/W	
	D6	TRXD6	Transmit/Receive data D6				X	R/W	
	D5	TRXD5	Transmit/Receive data D5				X	R/W	
	D4	TRXD4	Transmit/Receive data D4				X	R/W	
	D3	TRXD3	Transmit/Receive data D3				X	R/W	
	D2	TRXD2	Transmit/Receive data D2				X	R/W	
	D1	TRXD1	Transmit/Receive data D1				X	R/W	
	D0	TRXD0	Transmit/Receive data D0 (LSB)				X	R/W	
00FF50	D7	SIK07	K07 interrupt selection register		Interrupt enable	Interrupt disable	0	R/W	
	D6	SIK06	K06 interrupt selection register				0	R/W	
	D5	SIK05	K05 interrupt selection register				0	R/W	
	D4	SIK04	K04 interrupt selection register				0	R/W	
	D3	SIK03	K03 interrupt selection register				0	R/W	
	D2	SIK02	K02 interrupt selection register				0	R/W	
	D1	SIK01	K01 interrupt selection register				0	R/W	
	D0	SIK00	K00 interrupt selection register				0	R/W	
00FF51	D7	–	–		–	–	–		Constantly "0" when being read
	D6	–	–		–	–	–		
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		
	D2	–	–		–	–	–		
	D1	SIK11	K11 interrupt selection register		Interrupt enable	Interrupt disable	0	R/W	
	D0	SIK10	K10 interrupt selection register				0	R/W	

Table 5.1.1(j) I/O Memory map (00FF52H–00FF63H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF52	D7	KCP07	K07 input comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register			1	R/W	
	D3	KCP03	K03 input comparison register			1	R/W	
	D2	KCP02	K02 input comparison register			1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FF53	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KCP11	K11 input comparison register	Falling edge	Rising edge	1	R/W	
	D0	KCP10	K10 input comparison register			1	R/W	
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data			–	R	
	D5	K05D	K05 input port data			–	R	
	D4	K04D	K04 input port data			–	R	
	D3	K03D	K03 input port data			–	R	
	D2	K02D	K02 input port data			–	R	
	D1	K01D	K01 input port data			–	R	
	D0	K00D	K00 input port data			–	R	
00FF55	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	_		
	D4	–	–	–	–	_		
	D3	–	–	–	–	_		
	D2	–	–	–	–	_		
	D1	K11D	K11 input port data	High level input	Low level input	–	R	
	D0	K10D	K10 input port data			–	R	
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register			0	R/W	
	D5	IOC15	P15 I/O control register			0	R/W	
	D4	IOC14	P14 I/O control register			0	R/W	
	D3	IOC13	P13 I/O control register			0	R/W	
	D2	IOC12	P12 I/O control register			0	R/W	
	D1	IOC11	P11 I/O control register			0	R/W	
	D0	IOC10	P10 I/O control register			0	R/W	
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data			1	R/W	
	D5	P15D	P15 I/O port data			1	R/W	
	D4	P14D	P14 I/O port data			1	R/W	
	D3	P13D	P13 I/O port data			1	R/W	
	D2	P12D	P12 I/O port data			1	R/W	
	D1	P11D	P11 I/O port data			1	R/W	
	D0	P10D	P10 I/O port data			1	R/W	

Table 5.1.1(k) I/O Memory map (00FF70H–00FF78H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF70	D7	HZR51	R51 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR50	R50 high impedance control			0	R/W	
	D5	HZR4H	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR4L	General-purpose register			0	R/W	
	D3	HZR1H	General-purpose register			0	R/W	
	D2	HZR1L	General-purpose register			0	R/W	
	D1	HZR0H	General-purpose register			0	R/W	
	D0	HZR0L	General-purpose register			0	R/W	
00FF71	D7	HZR27	R27 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR26	R26 high impedance control			0	R/W	
	D5	HZR25	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR24	General-purpose register			0	R/W	
	D3	HZR23	GP register/SEG47 high impedance control	1/Hi-Z	0/Output	0	R/W	*1
	D2	HZR22	GP register/SEG48 high impedance control			0	R/W	
	D1	HZR21	GP register/SEG49 high impedance control			0	R/W	
	D0	HZR20	GP register/SEG50 high impedance control			0	R/W	
00FF72	D7	HZR37	GP register/SEG40 high impedance control	1/Hi-Z	0/Output	0	R/W	*1
	D6	HZR36	GP register/SEG41 high impedance control			0	R/W	
	D5	HZR35	GP register/SEG42 high impedance control			0	R/W	
	D4	HZR34	R34 high impedance control	Hi-Z	Output	0	R/W	
	D3	HZR33	GP register/SEG43 high impedance control	1/Hi-Z	0/Output	0	R/W	*1
	D2	HZR32	GP register/SEG44 high impedance control			0	R/W	
	D1	HZR31	GP register/SEG45 high impedance control			0	R/W	
	D0	HZR30	GP register/SEG46 high impedance control			0	R/W	
00FF75	D7	R27D	R27 output port data	High	Low	1	R/W	
	D6	R26D	R26 output port data			1 *2	R/W	
	D5	R25D	General-purpose register	1	0	1	R/W	Reserved register
	D4	R24D	General-purpose register			1	R/W	
	D3	R23D	GP register/SEG47 output port data	1/High	0/Low	1	R/W	*1
	D2	R22D	GP register/SEG48 output port data			1	R/W	
	D1	R21D	GP register/SEG49 output port data			1	R/W	
	D0	R20D	GP register/SEG50 output port data			1	R/W	
00FF76	D7	R37D	GP register/SEG40 output port data	1/High	0/Low	1	R/W	*1
	D6	R36D	GP register/SEG41 output port data			1	R/W	
	D5	R35D	GP register/SEG42 output port data			1	R/W	
	D4	R34D	R34 output port data	High	Low	1	R/W	
	D3	R33D	GP register/SEG43 output port data	1/High	0/Low	1	R/W	*1
	D2	R32D	GP register/SEG44 output port data			1	R/W	
	D1	R31D	GP register/SEG45 output port data			1	R/W	
	D0	R30D	GP register/SEG46 output port data			1	R/W	
00FF78	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	R51D	R51 output port data	High	Low	1	R/W	
	D0	R50D	R50 output port data			0	R/W	

*1 The SEGxx high-impedance control and SEGxx output port data bits are effective only when the SEGxx terminal is configured for DC output. The bit corresponding to the SEG terminal that is configured for LCD segment output can be used as a general-purpose register. The SEG terminals to be used for DC output can be selected from among SEG40–SEG50 by mask option.

*2 "0" when $\overline{\text{TOUT}}$ output or REM output is selected by mask option.

5.2 Watchdog Timer

5.2.1 Configuration of watchdog timer

The S1C88848 is equipped with a watchdog timer driven by OSC1 as source oscillation. The watchdog timer must be reset periodically in software, and if reset of more than 3–4 seconds (when fOSC1 = 32.768 kHz) does not take place, a non-maskable interrupt signal is generated and output to the CPU.

Figure 5.2.1.1 is a block diagram of the watchdog timer.

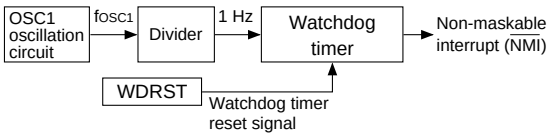


Fig. 5.2.1.1 Block diagram of watchdog timer

By running watchdog timer reset during the main routine of the program, it is possible to detect program runaway as if watchdog timer processing had not been applied. Normally, this routine is integrated at points that are regularly being processed.

The watchdog timer continues to operate during HALT and when a HALT state is continuous for longer than 3–4 seconds, the CPU shifts to exception processing.
During SLEEP, the watchdog timer is stopped.

5.2.2 Interrupt function

In cases where the watchdog timer is not periodically reset in software, the watchdog timer outputs an interrupt signal to the CPU's $\overline{\text{NMI}}$ (level 4) input. Unmaskable and taking priority over other interrupts, this interrupt triggers the generation of exception processing. See the "S1C88 Core CPU Manual" for more details on $\overline{\text{NMI}}$ exception processing.
This exception processing vector is set at 000004H.

5.2.3 Control of watchdog timer

Table 5.2.3.1 shows the control bits for the watchdog timer.

WDRST: 00FF40H•D2

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" to WDRST, the watchdog timer is reset, after which it is immediately restarted.
Writing "0" will mean no operation.
Since WDRST is for writing only, it is constantly set to "0" during readout.

5.2.4 Programming notes

(1) The watchdog timer must reset within 3-second cycles by software.

(2) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when fOSC1 is 32.768 kHz).

Table 5.2.3.1 Watchdog timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1	FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when being read
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

5.3 Oscillation Circuits

5.3.1 Configuration of oscillation circuits

The S1C88848 is twin clock system with two internal oscillation circuits (OSC1 and OSC3).
The OSC3 oscillation circuit generates the main clock when the CPU and some peripheral circuits (output port, serial interface, programmable timer and remote controller) are in high speed operation.
The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) sub-clock.
Figure 5.3.1.1 shows the configuration of the oscillation circuit.

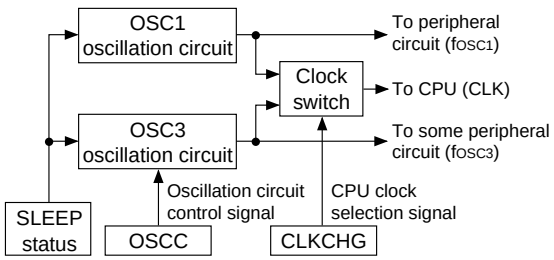


Fig. 5.3.1.1 Configuration of oscillation circuits

At initial reset, OSC3 oscillation circuit is selected for the CPU operating clock. Switching the system clock between OSC1 and OSC3 and turning the OSC3 oscillation circuit ON and OFF are controlled by software. OSC3 circuit is utilized when high speed operation of the CPU and some peripheral circuits become necessary. Otherwise, OSC1 should be used to generate the operating clock and OSC3 circuit placed in a stopped state in order to reduce current consumption.

5.3.2 Mask option

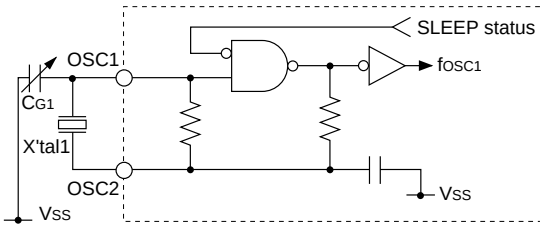
OSC1 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ CR oscillation circuit

OSC3 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ Ceramic oscillation circuit
- ☐ CR oscillation circuit

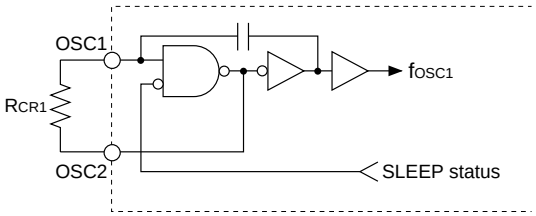
In terms of the oscillation circuit types for OSC1, either crystal oscillation or CR oscillation can be selected by mask option.
In terms of oscillation circuit types for OSC3, either crystal oscillation, ceramic oscillation or CR oscillation can be selected bymask option, in the same way as OSC1.

5.3.3 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) system clock which is utilized during low speed operation (low power mode) of the CPU and peripheral circuits. Furthermore, even when OSC3 is utilized as the system clock, OSC1 continues to generate the source clock for the clock timer and stopwatch timer.
This oscillation circuit stops when the SLP instruction is executed.
In terms of the oscillation circuit types, either crystal oscillation or CR oscillation can be selected by mask option.
Figure 5.3.3.1 shows the configuration of the OSC1 oscillation circuit.



(1) Crystal oscillation circuit



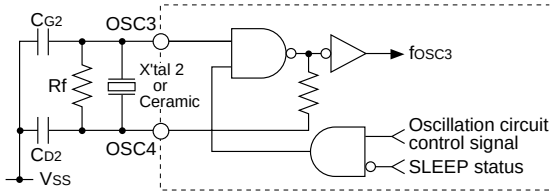
(2) CR oscillation circuit

Fig. 5.3.3.1 OSC1 oscillation circuit

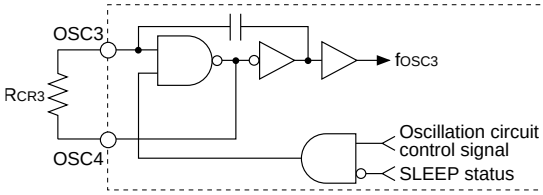
When crystal oscillation is selected, a crystal oscillation circuit can be easily formed by connecting a crystal oscillator X'tal1 (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals along with a trimmer capacitor C_{G1} (5–25 pF) between the OSC1 terminal and V_{SS}.
When CR oscillation is selected, connect a resistor (R_{CR1}) between the OSC1 and OSC2 terminals.

5.3.4 OSC3 oscillation circuit

The OSC3 oscillation circuit generates the system clock when the CPU and some peripheral circuits (output port, serial interface, programmable timer and remote controller) are in high speed operation. This oscillation circuit stops when the SLP instruction is executed, or the OSCC register is set to "0". In terms of oscillation circuit types, any one of crystal oscillation, ceramic oscillation or CR oscillation can be selected by mask option. Figure 5.3.4.1 shows the configuration of the OSC3 oscillation circuit.



(1) Crystal/Ceramic oscillation circuit



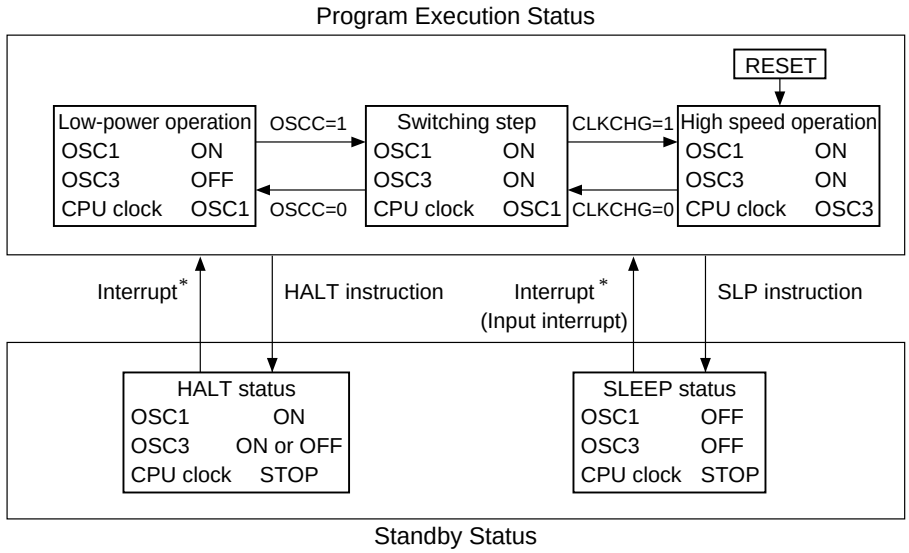
(2) CR oscillation circuit

Fig. 5.3.4.1 OSC3 oscillation circuit

When crystal or ceramic oscillation circuit is selected, the crystal or ceramic oscillation circuit are formed by connecting either a crystal oscillator (X'tal2) or a combination of ceramic oscillator (Ceramic) and feedback resistor (Rf) between OSC3 and OSC4 terminals and connecting two capacitors (C_{G2}, C_{D2}) between the OSC3 terminal and V_{SS}, and between the OSC4 terminal and V_{SS}, respectively. When CR oscillation is selected, the CR oscillation circuit is formed merely by connecting a resistor (R_{CR3}) between OSC3 and OSC4 terminals.

5.3.5 Switching the CPU clock

You can use either OSC1 or OSC3 as the system clock for the CPU and you can switch over by means of software.
You can save power by turning the OSC3 oscillation circuit off while the CPU is operating in OSC1. When you must operate on OSC3, you can change to high speed operation by turning the OSC3 oscillation circuit ON and switching over the system clock. In this case, since several 100 µsec to several 10 msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON, you should switch over the clock after stabilization time has elapsed. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
When switching over from the OSC3 to the OSC1, turn the OSC3 oscillation circuit OFF immediately following the clock changeover.
Figure 5.3.5.1 indicates the status transition diagram for clock changeover.



* The return destination from the standby status becomes the program execution status prior to shifting to the standby status

Fig. 5.3.5.1 Status transition diagram for clock changeover

5.3.6 Control of oscillation circuit

Table 5.3.6.1 shows the control bits for the oscillation circuits.

Table 5.3.6.1 Oscillation circuit control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF02	D7	EBR	General-purpose register	1	0	0	R/W	Reserved register
	D6	WT2	General-purpose register			0	R/W	
	D5	WT1	General-purpose register			0	R/W	
	D4	WT0	General-purpose register			0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	1	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	1	R/W	
	D1	VD1C1	General-purpose register	1	0	0	R/W	Reserved register
	D0	VD1C0	General-purpose register			0	R/W	

OSCC: 00FF02H•D2

Controls the ON and OFF settings of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When the CPU and some peripheral circuits (output port, serial interface, programmable timer and remote controller) are to be operated at high speed, OSCC is to be set to "1". At all other times, it should be set to "0" in order to reduce current consumption.
At initial reset, OSCC is set to "1" (OSC3 oscillation ON).

CLKCHG: 00FF02H•D3

Selects the operating clock for the CPU.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

When the operating clock for the CPU is switched to OSC3, CLKCHG should be set to "1" and when the clock is switched to OSC1, CLKCHG should be set to "0".
At initial reset, CLKCHG is set to "1" (OSC3 clock).

5.3.7 Programming notes

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.

- CPU operating clock
  OSC1
- OSC3 oscillation circuit
  OFF (When the OSC3 clock is not necessary for some peripheral circuits.)

(2) Since several 100 µsec to several 10 msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes ON. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)

(3) When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation OFF with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

5.4 Input Ports (K ports)

5.4.1 Configuration of input ports

The S1C88848 is equipped with 10 input port bits (K00–K07, K10 and K11) which are usable as general purpose input port terminals with interrupt function.

K10 and K11 terminals double as the external clock (EVIN0 and EVIN2) input terminals of the programmable timer (event counter) with input port functions sharing the input signals. (See "5.10 Programmable Timer")

Each input port is equipped with a pull-up resistor. The mask option can be used to select either "With resistor" or "Gate direct" for each input port. Figure 5.4.1.1 shows the structure of the input port.

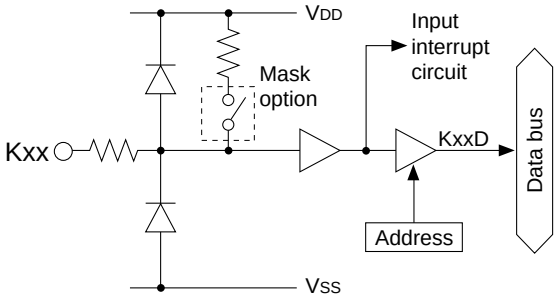


Fig. 5.4.1.1 Structure of input port

Each input port terminal is directly connected via a three-state buffer to the data bus. Furthermore, the input signal state at the instant of input port readout is read in that form as data.

5.4.2 Mask option

Input port pull-up resistors		
K00	☐ With resistor	☐ Gate direct
K01	☐ With resistor	☐ Gate direct
K02	☐ With resistor	☐ Gate direct
K03	☐ With resistor	☐ Gate direct
K04	☐ With resistor	☐ Gate direct
K05	☐ With resistor	☐ Gate direct
K06	☐ With resistor	☐ Gate direct
K07	☐ With resistor	☐ Gate direct
K10	☐ With resistor	☐ Gate direct
K11	☐ With resistor	☐ Gate direct

Input ports K00–K07, K10 and K11 are all equipped with pull-up resistors. The mask option can be used to select 'With resistor' or 'Gate direct' for each port (bit).

The 'With resistor' option is rendered suitable for purposes such as push switch or key matrix input. When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

When 'Gate direct' is selected, the pull-up resistor is detached and the port is rendered suitable for purposes such as slide switch input and interfacing with other LSIs.
In this case, take care that a floating state does not occur in input.

For unused input ports, select the default setting of "With resistor".

5.4.3 Interrupt function and input comparison register

Input port K00–K07, K10 and K11 are all equipped with an interrupt function. These input ports are divided into three groupings: K00–K03 (K0L), K04–K07 (K0H) and K10–K11 (K1). Furthermore, the interrupt generation condition for each series of terminals can be set by software.
When the interrupt generation condition set for each series of terminals is met, the interrupt factor flag FK0L, FK0H or FK1 corresponding to the applicable series is set at "1" and an interrupt is generated.

Interrupt can be prohibited by setting the interrupt enable registers EK0L, EK0H and EK1 for the corresponding interrupt factor flags.
Furthermore, the priority level for input interrupt can be set at the desired level (0–3) using the interrupt priority registers PK00–PK01 and PK10–PK11 corresponding to each of two groups K0x (K00–K07) and K1x (K10–K11).
For details on the interrupt control registers for the above and on operations subsequent to interrupt generation, see "5.15 Interrupt and Standby Status".

The exception processing vectors for each interrupt factor are set as follows:

K10–K11 input interrupt: 00000AH
K04–K07 input interrupt: 00000CH
K00–K03 input interrupt: 00000EH

Figure 5.4.3.1 shows the configuration of the input interrupt circuit.

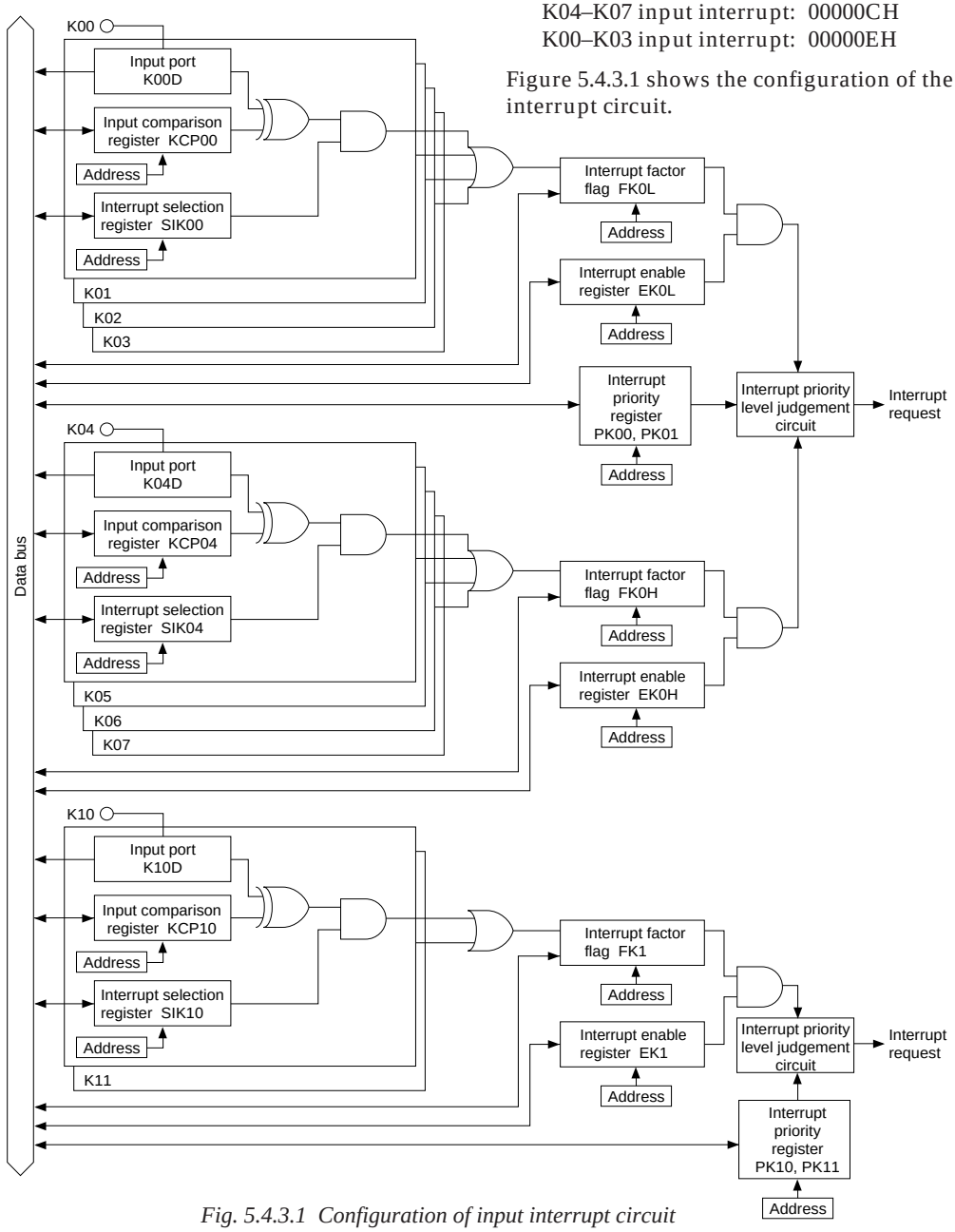


Fig. 5.4.3.1 Configuration of input interrupt circuit

The interrupt selection registers SIK00–SIK03, SIK04–SIK07 and SIK10–SIK11 and input comparison registers KCP00–KCP03, KCP04–KCP07 and KCP10–KCP11 for each port are used to set the interrupt generation condition described above.

Input port interrupt can be permitted or prohibited by the setting of the interrupt selection register SIK. In contrast to the interrupt enable register EK which masks the interrupt factor for each series of terminals, the interrupt selection register SIK is masks the bit units.

The input comparison register KCP selects whether the interrupt for each input port will be generated on the rising edge or the falling edge of input.

When the data content of the input terminals in which interrupt has been permitted by the interrupt selection register SIK and the data content of the input comparison register KCP change from a conformity state to a non-conformity state, the interrupt factor flag FK should be set to "1" and an interrupt is generated.

Figure 5.4.3.2 shows an example of interrupt generation in the series of terminals K0L (K00–K03).

Because interrupt has been prohibited for K00 by the interrupt selection register SIK00, with the settings as shown in (2), an interrupt will not be generated.
Since K03 is "0" in the next settings (3) in the figure, the non-conformity between the input terminal data K01–K03 where interrupt is permitted and the data from the input comparison registers KCP01–KCP03 generates an interrupt.
In line with the explanation above, since the change in the contents of input data and input comparison registers KCP from a conformity state to a non-conformity state introduces an interrupt generation condition, switching from one non-conformity state to another, as is the case in (4) in the figure, will not generate an interrupt. Consequently, in order to be able to generate a second interrupt, either the input terminal must be returned to a state where its content is once again in conformity with that of the input comparison register KCP, or the input comparison register KCP must be reset.
Input terminals for which interrupt is prohibited will not influence an interrupt generation condition.

Interrupt is generated in exactly the same way in the other two series of terminals K0H (K04–K07) and K1 (K10–K11).

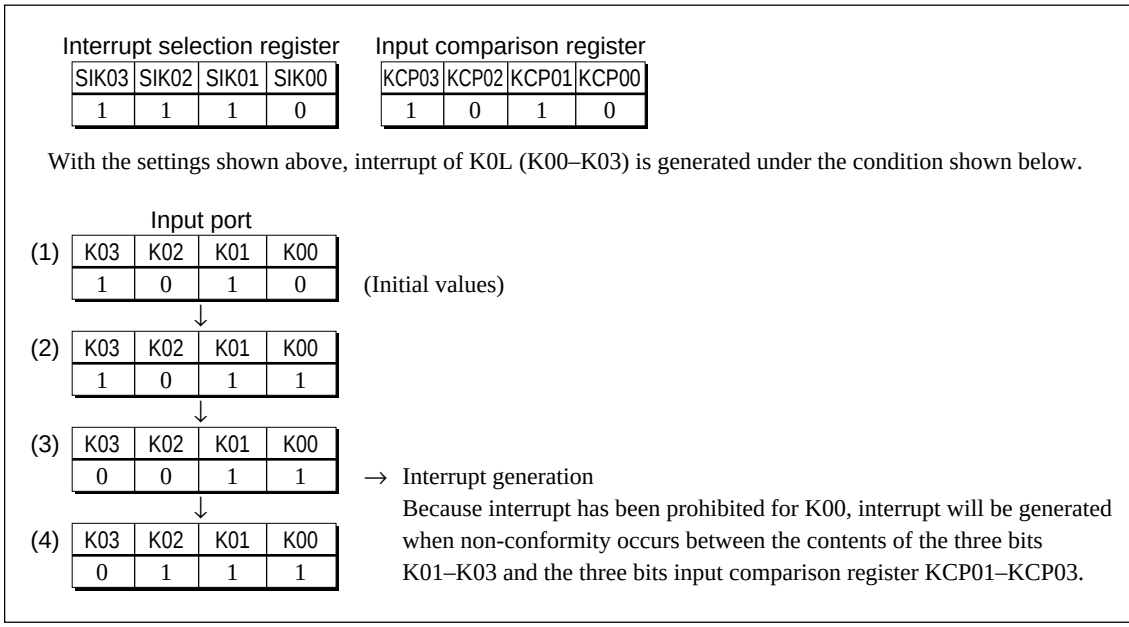


Fig. 5.4.3.2 Interrupt generation example in K0L (K00–K03)

5.4.4 Control of input ports

Table 5.4.4.1 shows the input port control bits.

Table 5.4.4.1(a) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF50	D7	SIK07	K07 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D6	SIK06	K06 interrupt selection register			0	R/W	
	D5	SIK05	K05 interrupt selection register			0	R/W	
	D4	SIK04	K04 interrupt selection register			0	R/W	
	D3	SIK03	K03 interrupt selection register			0	R/W	
	D2	SIK02	K02 interrupt selection register			0	R/W	
	D1	SIK01	K01 interrupt selection register			0	R/W	
	D0	SIK00	K00 interrupt selection register			0	R/W	
00FF51	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SIK11	K11 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D0	SIK10	K10 interrupt selection register			0	R/W	
00FF52	D7	KCP07	K07 input comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register			1	R/W	
	D3	KCP03	K03 input comparison register			1	R/W	
	D2	KCP02	K02 input comparison register			1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FF53	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KCP11	K11 input comparison register	Falling edge	Rising edge	1	R/W	
	D0	KCP10	K10 input comparison register			1	R/W	
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data			–	R	
	D5	K05D	K05 input port data			–	R	
	D4	K04D	K04 input port data			–	R	
	D3	K03D	K03 input port data			–	R	
	D2	K02D	K02 input port data			–	R	
	D1	K01D	K01 input port data			–	R	
	D0	K00D	K00 input port data			–	R	
00FF55	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	_		
	D4	–	–	–	–	_		
	D3	–	–	–	–	_		
	D2	–	–	–	–	_		
	D1	K11D	K11 input port data	High level input	Low level input	–	R	
	D0	K10D	K10 input port data			–	R	

Table 5.4.4.1(b) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 = 1 1	Level 3	0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register	PSIF1 PSIF0 = 1 0	Level 2	0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register	PSW1 PSW0 = 0 1	Level 1	0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register	PTM1 PTM0 = 0 0	Level 0	0	R/W	
	D0	PTM0				0	R/W	
00FF21	D7	PREM1	REM carrier interrupt priority register	PREM1 PREM0 = 1 1	Level 3	0	R/W	
	D6	PREM0				0	R/W	
	D5	PPT3	Programmable timer 2–3 interrupt priority register	PPT3 PPT2 = 1 0	Level 2	0	R/W	
	D4	PPT2				0	R/W	
	D3	PPT1	Programmable timer 0–1 interrupt priority register	PPT1 PPT0 = 0 1	Level 1	0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10–K11 interrupt priority register	PK11 PK10 = 0 0	Level 0	0	R/W	
	D0	PK10				0	R/W	
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10–K11 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R)	(R)	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag	Interrupt	No interrupt	0	R/W	
	D5	FK1	K10–K11 interrupt factor flag	factor is	factor is	0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag	generated	generated	0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag	(W)	(W)	0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag	Reset	No operation	0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

K00D–K07D: 00FF54H
K10D, K11D: 00FF55H•D0, D1

Input data of input port terminal Kxx can be read out.

When "1" is read: HIGH level
When "0" is read: LOW level
Writing: Invalid

The terminal voltage of each of the input port K00–K07, K10 and K11 can be directly read out as either a "1" for HIGH (V_{DD}) level or a "0" for LOW (V_{SS}) level.
This bit is exclusively for readout and are not usable for write operations.

SIK00–SIK07: 00FF50H
SIK10, SIK11: 00FF51H•D0, D1

Sets the interrupt generation condition (interrupt permission / prohibition) for input port terminals K00–K07, K10 and K11.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

SIKxx is the interrupt selection register which correspond to the input port Kxx. A "1" setting permits interrupt in that input port and a "0" prohibits it. Changes of state in an input terminal in which interrupt is prohibited, will not influence interrupt generation.
At initial reset, this register is set to "0" (interrupt prohibited).

KCP00–KCP07: 00FF52H
KCP10, KCP10: 00FF53H•D0, D1

Sets the interrupt generation condition (interrupt generation timing) for input port terminals K00–K07, K10 and K11.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

KCPxx is the input comparison register which correspond to the input port Kxx. Interrupt in those ports which have been set to "1" is generated on the falling edge of the input and in those set to "0" on the rising edge.
At initial reset, this register is set to "1" (falling edge).

PK00, PK01: 00FF20H•D6, D7
PK10, PK11: 00FF21H•D0, D1

Sets the input interrupt priority level. The two bits PK00 and PK01 are the interrupt priority registers corresponding to the interrupts for K00–K07 (K0L and K0H). Corresponding to K10–K11 (K1), the two bits PK10 and PK11 perform the same function.
Table 5.4.4.2 shows the interrupt priority level which can be set by this register.

Table 5.4.4.2 Interrupt priority level settings

PK11 PK01	PK10 PK00	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EK0L, EK0H, EK1: 00FF23H•D3, D4, D5

How interrupt generation to the CPU is permitted or prohibited.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

The interrupt enable register EK0L corresponds to K00–K03, EK0H to K04–K07, and EK1 to K10–K11. Interrupt is permitted in those series of terminals set to "1" and prohibited in those set to "0".
At initial reset, this register is set to "0" (interrupt prohibited).

FK0L, FK0H, FK1: 00FF25H•D3, D4, D5

Indicates the generation state for an input interrupt.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Reset factor flag
When "0" is written: Invalid

The interrupt factor flag FK0L corresponds to K00–K03, FK0H to K04–K07, and FK1 to K10–K11. They are set to "1" by the occurrence of an interrupt generation condition.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is all reset to "0".

5.4.5 Programming note

When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

5.5 Output Ports (R ports)

5.5.1 Configuration of output ports

The S1C88848 is equipped with 5 bits of output ports (R26, R27, R34, R50 and R51).
Furthermore, the terminals within SEG40–SEG50 that are not used for driving an LCD can be configured as DC output ports by mask option.

Figure 5.5.1.1 shows the basic structure (excluding special output circuits) of the output ports.
The output specification of each port is fixed at complementary output.

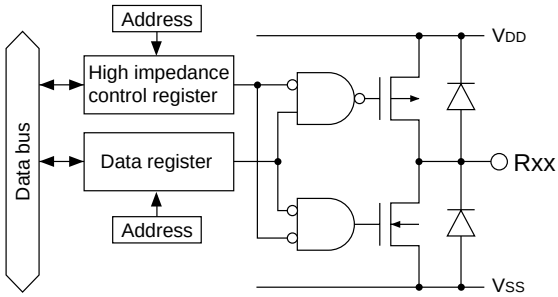


Fig. 5.5.1.1 Structure of output ports

Each output port can be set into high impedance state by software.

Besides normal DC output, the output ports have special output functions. The R27, R34 and R50 functions can be selected by software and the R26 and R51 functions can be selected by mask option.

5.5.2 Mask option

R26 and R51 output port specifications
R26 ..... ☐ DC output
☐ $\overline{\text{TOUT}}$ output
☐ REM output
R51 ..... ☐ DC output
☐ $\overline{\text{BZ}}$ output

SEG40–SEG50 output port specifications

SEG40	☐ DC output	☐ SEG output
SEG41	☐ DC output	☐ SEG output
SEG42	☐ DC output	☐ SEG output
SEG43	☐ DC output	☐ SEG output
SEG44	☐ DC output	☐ SEG output
SEG45	☐ DC output	☐ SEG output
SEG46	☐ DC output	☐ SEG output
SEG47	☐ DC output	☐ SEG output
SEG48	☐ DC output	☐ SEG output
SEG49	☐ DC output	☐ SEG output
SEG50	☐ DC output	☐ SEG output

The mask option allows selection of special outputs for the R26 and R51 output ports as well as the DC output.

The R26 port can be configured as the $\overline{\text{TOUT}}$ output port (TOUT signal inverted output) or REM output (remote-control carrier output). The R51 port can be set as the $\overline{\text{BZ}}$ output port (buzzer signal inverted output).
SEG40 to SEG50 can also be configured as general-purpose DC output ports or LCD segment output ports.

5.5.3 High impedance control

The output port can be high impedance controlled in software.

A high impedance control register is set for each output port terminal as shown below. Either complementary output and high impedance state can be selected with this register.

HZR26: R26 high impedance control register
HZR27: R27 high impedance control register
HZR34: R34 high impedance control register
HZR50: R50 high impedance control register
HZR51: R51 high impedance control register

HZR20: SEG50 high impedance control register *
HZR21: SEG49 high impedance control register *
HZR22: SEG48 high impedance control register *
HZR23: SEG47 high impedance control register *
HZR30: SEG46 high impedance control register *
HZR31: SEG45 high impedance control register *
HZR32: SEG44 high impedance control register *
HZR33: SEG43 high impedance control register *
HZR35: SEG42 high impedance control register *
HZR36: SEG41 high impedance control register *
HZR37: SEG40 high impedance control register *

* These registers function as a high-impedance control register only when the corresponding SEG terminal is configured for general-purpose DC output. When the SEG terminal is configured for LCD segment output, the corresponding register becomes a general-purpose register.

When a high impedance control register HZRxx is set to "1", the corresponding output port terminal becomes high impedance state and when set to "0", it becomes complementary output.

5.5.4 DC output

As Figure 5.5.1.1 shows, when "1" is written to the output port data register, the output terminal switches to HIGH (V_{DD}) level and when "0" is written it switches to LOW (V_{SS}) level. When output is in a high impedance state, the data written to the data register is output from the terminal at the instant when output is switched to complementary.

5.5.5 Special output

Besides normal DC output, each output port can also be assigned special output function by software (R27, R34, R50) or mask option (R26, R51) as shown in Table 5.5.5.1.

Table 5.5.5.1 Special output ports

Output port	Special output
R26	$\overline{TOUT}$ output or REM output (mask option)
R27	TOUT output (software selection)
R34	FOUT output (software selection)
R50	BZ output (software selection)
R51	$\overline{BZ}$ output (mask option)

■ REM output (R26)

A mask option is provided so the R26 output port terminal can be used for outputting a REM signal (remote control carrier signal).
When REM output is selected, the R26 data register is disconnected from the R26 terminal and can be used as a general-purpose register that does not affect the output.
The REM output is controlled using the remote controller registers. Refer to Section 5.13, "Remote Controller" for details.

■ TOUT output (R27), $\overline{TOUT}$ output (R26)

In order for the S1C88848 to provide clock signal to an external device, the R27 output port terminal can be used to output a TOUT signal (clock output by the programmable timer). Furthermore, the R26 output port terminal can be used to output a $\overline{TOUT}$ signal (TOUT inverted signal). The configuration of the output ports R26 and R27 is shown in Figure 5.5.5.1.

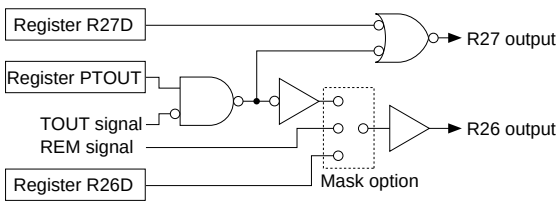


Fig. 5.5.5.1 Configuration of R26 and R27

The output control for the TOUT ($\overline{TOUT}$) signals is done by the register PTOUT. When you set "1" for the PTOUT, the TOUT ($\overline{TOUT}$) signal is output from the R27 (R26) output port terminal. When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D.
The data register R26D does not affect the $\overline{TOUT}$ output.

The TOUT signal is generated from the programmable timer underflow signal by halving the frequency.
With respect to frequency control, see "5.10 Programmable Timer".
Since the TOUT ($\overline{TOUT}$) signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by setting the register, a hazard of a 1/2 cycle or less is generated.
Figure 5.5.5.2 shows the output waveform of the TOUT ($\overline{TOUT}$) signal.

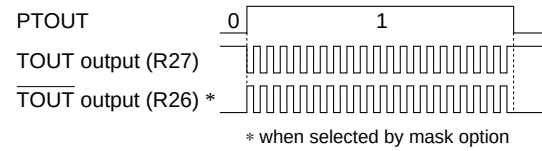


Fig. 5.5.5.2 TOUT ($\overline{TOUT}$) output waveform

■ FOUT output (R34)

In order for the S1C88848 to provide clock signal to an external device, a FOUT signal (divided clock of oscillation clock f_{OSC1} or f_{OSC3}) can be output from the output port terminal R34.
Figure 5.5.5.3 shows the configuration of output port R34.

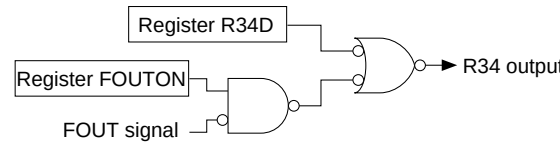


Fig. 5.5.5.3 Configuration of R34

The output control for the FOUT signal is done by the register FOUTON. When you set "1" for the FOUTON, the FOUT signal is output from the output port terminal R34, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R34D.
The frequency of the FOUT signal can be selected in software by setting the registers FOUT0–FOUT2. The frequency is selected any one from among eight settings as shown in Table 5.5.5.2.

Table 5.5.5.2 FOUT frequency setting

FOUT2	FOUT1	FOUT0	FOUT frequency
0	0	0	f_{OSC1} / 1
0	0	1	f_{OSC1} / 2
0	1	0	f_{OSC1} / 4
0	1	1	f_{OSC1} / 8
1	0	0	f_{OSC3} / 1
1	0	1	f_{OSC3} / 2
1	1	0	f_{OSC3} / 4
1	1	1	f_{OSC3} / 8

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

When the FOUT frequency is made "fOSC3 / n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several 100 µsec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to ON state.
Since the FOUT signal is generated asynchronously from the register FOUTON, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.5.5.4 shows the output waveform of the FOUT signal.

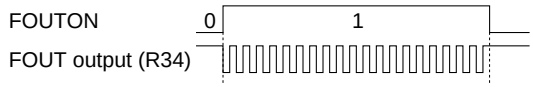


Fig. 5.5.5.4 Output waveform of FOUT signal

■ BZ output (R50), $\overline{BZ}$ output (R51)

In order for the S1C88848 to drive an external buzzer, a BZ signal (sound generator output) can be output from the output port terminal R50. Furthermore, the R51 output port terminal can be used to output a $\overline{BZ}$ signal (BZ inverted signal). The configuration of the output ports R50 and R51 is shown in Figure 5.5.5.5.

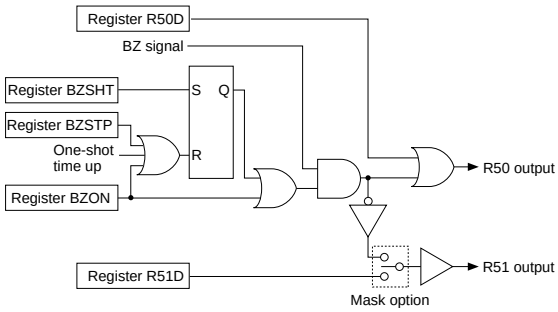


Fig. 5.5.5.5 Configuration of R50 and R51

The output control for the BZ ($\overline{BZ}$) signal is done by the registers BZON, BZSHT and BZSTP. When you set "1" for the BZON or BZSHT, the BZ ($\overline{BZ}$) signal is output from the output port terminal R50 (R51). When "0" is set for the BZON or "1" is set for the BZSTP, the R50 goes LOW (VSS) and the R51 goes HIGH (VDD).

To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
The BZ ($\overline{BZ}$) signal is generated by the sound generator. With respect to control of frequency and envelope, see "5.12 Sound Generator".
Since the BZ ($\overline{BZ}$) signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by setting the registers, a hazard of a 1/2 cycle or less is generated.
Figure 5.5.5.6 shows the output waveform of the BZ ($\overline{BZ}$) signal.

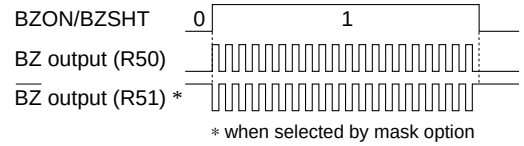


Fig. 5.5.5.6 BZ ($\overline{BZ}$) output waveform

5.5.6 Control of output ports

Table 5.5.6.1 shows the output port control bits.

Table 5.5.6.1(a) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF70	D7	HZR51	R51 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR50	R50 high impedance control			0	R/W	
	D5	HZR4H	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR4L	General-purpose register			0	R/W	
	D3	HZR1H	General-purpose register			0	R/W	
	D2	HZR1L	General-purpose register			0	R/W	
	D1	HZR0H	General-purpose register			0	R/W	
	D0	HZR0L	General-purpose register			0	R/W	
00FF71	D7	HZR27	R27 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR26	R26 high impedance control			0	R/W	
	D5	HZR25	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR24	General-purpose register			0	R/W	
	D3	HZR23	GP register/SEG47 high impedance control	1/Hi-Z	0/Output	0	R/W	*1
	D2	HZR22	GP register/SEG48 high impedance control			0	R/W	
	D1	HZR21	GP register/SEG49 high impedance control			0	R/W	
	D0	HZR20	GP register/SEG50 high impedance control			0	R/W	
00FF72	D7	HZR37	GP register/SEG40 high impedance control	1/Hi-Z	0/Output	0	R/W	*1
	D6	HZR36	GP register/SEG41 high impedance control			0	R/W	
	D5	HZR35	GP register/SEG42 high impedance control			0	R/W	
	D4	HZR34	R34 high impedance control	Hi-Z	Output	0	R/W	
	D3	HZR33	GP register/SEG43 high impedance control	1/Hi-Z	0/Output	0	R/W	*1
	D2	HZR32	GP register/SEG44 high impedance control			0	R/W	
	D1	HZR31	GP register/SEG45 high impedance control			0	R/W	
	D0	HZR30	GP register/SEG46 high impedance control			0	R/W	
00FF75	D7	R27D	R27 output port data	High	Low	1	R/W	
	D6	R26D	R26 output port data			1 *2	R/W	
	D5	R25D	General-purpose register	1	0	1	R/W	Reserved register
	D4	R24D	General-purpose register			1	R/W	
	D3	R23D	GP register/SEG47 output port data	1/High	0/Low	1	R/W	*1
	D2	R22D	GP register/SEG48 output port data			1	R/W	
	D1	R21D	GP register/SEG49 output port data			1	R/W	
	D0	R20D	GP register/SEG50 output port data			1	R/W	
00FF76	D7	R37D	GP register/SEG40 output port data	1/High	0/Low	1	R/W	*1
	D6	R36D	GP register/SEG41 output port data			1	R/W	
	D5	R35D	GP register/SEG42 output port data			1	R/W	
	D4	R34D	R34 output port data	High	Low	1	R/W	
	D3	R33D	GP register/SEG43 output port data	1/High	0/Low	1	R/W	*1
	D2	R32D	GP register/SEG44 output port data			1	R/W	
	D1	R31D	GP register/SEG45 output port data			1	R/W	
	D0	R30D	GP register/SEG46 output port data			1	R/W	
00FF78	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	R51D	R51 output port data	High	Low	1	R/W	
	D0	R50D	R50 output port data			0	R/W	

*1 The SEGxx high-impedance control and SEGxx output port data bits are effective only when the SEGxx terminal is configured for DC output. The bit corresponding to the SEG terminal that is configured for LCD segment output can be used as a general-purpose register. The SEG terminals to be used for DC output can be selected from among SEG40–SEG50 by mask option.

*2 "0" when $\overline{\text{TOUT}}$ output or REM output is selected by mask option.

Table 5.5.6.1(b) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE160	8/16-bit mode selection (timer 0/1)	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	fOSC3	fOSC1	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	fOSC3	fOSC1	0	R/W	
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1	FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when being read
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF44	D7	–	–	–	–	–		Constantly "0" when being read
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*1
	D0	BZON	Buzzer output control	On	Off	0	R/W	

*1 Reset to "0" during one-shot output.

■ High impedance control

HZR26, HZR27: 00FF71H•D6, D7
HZR34: 00FF72H•D4
HZR50, HZR51: 00FF70H•D6, D7

Sets the output terminals to a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

HZRxx is the high impedance control register which correspond to the Rxx output port terminal. When "1" is set to the HZRxx register, the corresponding output port terminal becomes high impedance state and when "0" is set, it becomes complementary output.
This control is effective even if the port is set as a special output port.
At initial reset, this register is set to "0" (complementary).

HZR20–HZR23: 00FF71H•D0–D3
HZR30–HZR33: 00FF72H•D0–D3
HZR35–HZR37: 00FF72H•D5–D7

Sets the SEG40–SEG50 terminals (configured for DC output) to a high impedance state.

When "1" is written: High impedance
When "0" is written: Complementary
Reading: Valid

HZR20–23, HZR30–33 and HZR35–37 are the high impedance control registers that correspond to the SEG50–47, SEG46–43 and SEG42–40 terminals, respectively, and are effective only when the SEG terminal is configured for DC output by mask option. HZRxx for the terminal configured as LCD segment output can be used as a general-purpose register that does not affect the output.
At initial reset, this register is set to "0" (complementary).

■ DC output control

R26D, R27D: 00FF75H•D6, D7
R34D: 00FF76H•D4
R50D, R51D: 00FF78H•D0, D1

Sets the data output from the output port terminal Rxx.

When "1" is written: HIGH level output
When "0" is written: LOW level output
Reading: Valid

RxxD is the data register for the Rxx output port. When "1" is set to the register, the corresponding output port terminal goes HIGH (V_{DD}), and when "0" is set, it goes LOW (V_{SS}).
At initial reset, R50D is set to "0" (LOW level output). The other registers are set to "1" (HIGH level output).
When R26 and / or R51 are set to the special outputs by mask option, R26D and / or R51D can be used as general-purpose registers that do not affect the output status.

R20D–R23D: 00FF75H•D0–D3
R30D–R33D: 00FF76H•D0–D3
R35D–R37D: 00FF76H•D5–D7

Sets data to be output from the SEG40–SEG50 terminals (configured for DC output).

When "1" is written: HIGH level output
When "0" is written: LOW level output
Reading: Valid

R20D–23D, R30D–33D and R35D–37D are the data registers that correspond to the SEG50–47, SEG46–43 and SEG42–40 terminals, respectively, and are effective only when the SEG terminal is configured for DC output by mask option. RxxD for the terminal configured as LCD segment output can be used as a general-purpose register that does not affect the output.
At initial reset, this register is set to "1" (HIGH level output).

■ Special output control

Note: Refer to Section 5.13, "Remote Controller", for the control registers used for REM output.

PTOUT: 00FF30H•D2

Controls the TOUT (programmable timer output clock) signal output.

When "1" is written: TOUT signal output ON
When "0" is written: TOUT signal output OFF
Reading: Valid

PTOUT is the output control register for TOUT signal. When "1" is set to the register, the TOUT ($\overline{TOUT}$) signal is output from the output port terminal R27 (R26). When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D. The data register R26D does not affect the $\overline{TOUT}$ output.
At initial reset, PTOUT is set to "0" (output OFF).
The $\overline{TOUT}$ signal can be output from R26 only when the function is selected by mask option.

FOUTON: 00FF40H•D3

Controls the FOUT (f_{OSC1} / f_{OSC3} dividing clock) signal output.

When "1" is written: FOUT signal output
When "0" is written: HIGH level (DC) output
Reading: Valid

FOUTON is the output control register for FOUT signal. When "1" is set, the FOUT signal is output from the output port terminal R34 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R34D.
At initial reset, FOUTON is set to "0" (HIGH level output).

FOUT0, FOUT1, FOUT2: 00FF40H•D4, D5, D6

FOUT signal frequency is set as shown in Table 5.5.6.2.

Table 5.5.6.2 FOUT frequency settings

FOUT2	FOUT1	FOUT0	FOUT frequency
0	0	0	f_{OSC1} / 1
0	0	1	f_{OSC1} / 2
0	1	0	f_{OSC1} / 4
0	1	1	f_{OSC1} / 8
1	0	0	f_{OSC3} / 1
1	0	1	f_{OSC3} / 2
1	1	0	f_{OSC3} / 4
1	1	1	f_{OSC3} / 8

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

At initial reset, this register is set to "0" (f_{OSC1} / 1).

BZON: 00FF44H•D0

Controls the buzzer (BZ and $\overline{BZ}$) signal output.

When "1" is written: Buzzer signal output ON
When "0" is written: Buzzer signal output OFF
Reading: Valid

BZON is the output control register for buzzer signal. When "1" is set to the register, the BZ ($\overline{BZ}$) signal is output from the output port terminal R50 (R51). When "0" is set, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
At initial reset, BZON is set to "0" (output OFF).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZSHT: 00FF44H•D5

Controls the one-shot buzzer output.

When "1" is written: Trigger
When "0" is written: No operation

When "1" is read: Busy
When "0" is read: Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate. The BZ ($\overline{BZ}$) signal is output from the R50 (R51) terminal. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed.
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") state. The trigger is invalid during ON (BZON = "1") state. When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON, "1" is read from BZSHTand when the output is OFF, "0" is read.
At initial reset, BZSHT is set to "0" (ready).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZSTP: 00FF44H•D6

Forcibly stops the one-shot buzzer output.

When "1" is written: Forcibly stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.5.7 Programming notes

(1) Since the special output signals (TOUT / $\overline{TOUT}$, FOUT, BZ / $\overline{BZ}$) are generated asynchronously from the output control registers (PTOUT, FOUTON, BZON, BZSHT and BZSTP), when the signals is turned ON or OFF by the output control register settings, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the special output signals (TOUT / $\overline{TOUT}$, FOUT, BZ / $\overline{BZ}$) are in the enable status, an unstable clock is output for the special output at the time of return from the SLEEP state. Consequently, when shifting to the SLEEP state, you should set the special output signal to the disable status prior to executing the SLP instruction.

(3) When the FOUT frequency is made "f_{OSC3} / n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several 100 µsec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to ON state.

5.6 I/O Ports (P ports)

5.6.1 Configuration of I/O ports

The S1C88848 is equipped with 8 bits of I/O ports (P10–P17).
Figure 5.6.1.1 shows the structure of an I/O port.

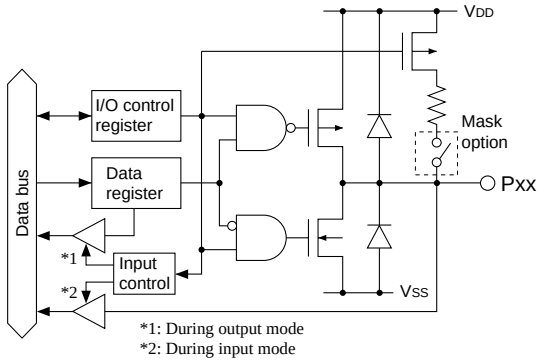


Fig. 5.6.1.1 Structure of I/O port

I/O port can be set for input or output mode in one bit unit. These settings are performed by writing data to the I/O control registers.
I/O port terminals P10–P13 are shared with serial interface input/output terminals. The function of the terminals is switchable in software. With respect to the serial interface, see "5.7 Serial Interface".
The data registers and I/O control registers of the I/O ports set as serial interface outputs are usable as general purpose registers with read/write capabilities which do not affect I/O activities of the terminal.
The same as above, I/O control registers of the I/O ports set as serial interface inputs are usable as general purpose register.

5.6.2 Mask option

I/O port pull-up resistors

P10	☐ With resistor	☐ Gate direct
P11	☐ With resistor	☐ Gate direct
P12	☐ With resistor	☐ Gate direct
P13	☐ With resistor	☐ Gate direct
P14	☐ With resistor	☐ Gate direct
P15	☐ With resistor	☐ Gate direct
P16	☐ With resistor	☐ Gate direct
P17	☐ With resistor	☐ Gate direct

I/O ports P10–P17 are equipped with a pull-up resistor which goes ON in the input mode. Whether this resistor is used or not can be selected for each port (one bit unit).
In cases where the 'With resistor' option is selected, the pull-up resistor goes ON when the port is in input mode.
When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = RIN x (CIN + load capacitance on the board) x 1.6 [sec]

RIN: Pull up resistance Max. value
CIN: Terminal capacitance Max. value

For unused I/O ports, select the default setting of "With resistor".

5.6.3 I/O control registers and I/O mode

I/O ports P10–P17 are set either to input or output modes by writing data to the I/O control registers IOC10–IOC17 which correspond to each bit.
To set an I/O port to input mode, write "0" to the I/O control register.
An I/O port which is set to input mode will shift to a high impedance state and functions as an input port.
Readout in input mode consists simply of a direct readout of the input terminal state: the data being "1" when the input terminal is at HIGH (VDD) level and "0" when it is at LOW (VSS) level.
When the "With resistor" option is selected using the mask option, the resistor is pulled up onto the port terminal in input mode.
Even in input mode, data can be written to the data registers without affecting the terminal state.
To set an I/O port to output mode, write "1" to the I/O control register. An I/O port which is set to output mode functions as an output port.
When port output data is "1", a HIGH (VDD) level is output and when it is "0", a LOW (VSS) level is output. Readout in output mode consists of the contents of the data register.
At initial reset, I/O control registers are set to "0" (I/O ports are set to input mode).

5.6.4 Control of I/O ports

Table 5.6.4.1 shows the I/O port control bits.

Table 5.6.4.1 I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register			0	R/W	
	D5	IOC15	P15 I/O control register			0	R/W	
	D4	IOC14	P14 I/O control register			0	R/W	
	D3	IOC13	P13 I/O control register			0	R/W	
	D2	IOC12	P12 I/O control register			0	R/W	
	D1	IOC11	P11 I/O control register			0	R/W	
	D0	IOC10	P10 I/O control register			0	R/W	
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data			1	R/W	
	D5	P15D	P15 I/O port data			1	R/W	
	D4	P14D	P14 I/O port data			1	R/W	
	D3	P13D	P13 I/O port data			1	R/W	
	D2	P12D	P12 I/O port data			1	R/W	
	D1	P11D	P11 I/O port data			1	R/W	
	D0	P10D	P10 I/O port data			1	R/W	

P10D–P17D: 00FF63H

How I/O port terminal P1x data readout and output data settings are performed.

When writing data:

When "1" is written: HIGH level
When "0" is written: LOW level

When the I/O port is set to output mode, the data written is output as is to the I/O port terminal. In terms of port data, when "1" is written, the port terminal goes to HIGH (V_{DD}) level and when "0" is written to a LOW (V_{SS}) level.
Even when the port is in input mode, data can still be written in.

When reading out data:

When "1" is read: HIGH level ("1")
When "0" is read: LOW level ("0")

When an I/O port is in input mode, the voltage level being input to the port terminal is read out. When terminal voltage is HIGH (V_{DD}), it is read as a "1", and when it is LOW (V_{SS}), it is read as a "0". Furthermore, in output mode, the contents of the data register are read out.
At initial reset, this register is set to "1" (HIGH level).

The data registers of I/O ports set for the output terminal of serial interface can be used as general purpose registers with read/write capabilities which do not affect I/O activities of the terminals.

IOC10–IOC17: 00FF61H

Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOC1x is the I/O control register which correspond to each I/O port in a bit unit.
Writing "1" to the IOC1x register will switch the corresponding I/O port P1x to output mode, and writing "0" will switch it to input mode.
At initial reset, this register is set to "0" (input mode).

The data registers of I/O ports set for the input terminal of serial interface can be used as general purpose registers with read/write capabilities which do not affect I/O activities of the terminals.

5.6.5 Programming note

When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

5.7 Serial Interface

5.7.1 Configuration of serial interface

The S1C88848 incorporates a full duplex serial interface (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software.
Figure 5.7.1.1 shows the configuration of the serial interface.

Serial interface input / output terminals, SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are shared with I / O ports P10–P13. In order to utilize these terminals for the serial interface input / output terminals, proper settings have to be made with registers ESIF, SMD0 and SMD1. (At initial reset, these terminals are set as I / O port terminals.)
The direction of I / O port terminals set for serial interface input / output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I / O control registers for the I / O ports become invalid.

Table 5.7.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P10	SIN
P11	SOUT
P12	$\overline{\text{SCLK}}$
P13	$\overline{\text{SRDY}}$

* The terminals used may vary depending on the transfer mode.

SIN and SOUT are serial data input and output terminals which function identically in clock synchronous system and asynchronous system.
$\overline{\text{SCLK}}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input / output terminal. $\overline{\text{SRDY}}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are superfluous, the I / O port terminals P12 and P13 can be used as I / O ports.
In the same way, when clock synchronous master mode is selected, since $\overline{\text{SRDY}}$ is superfluous, the I / O port terminal P13 can be used as I / O port.

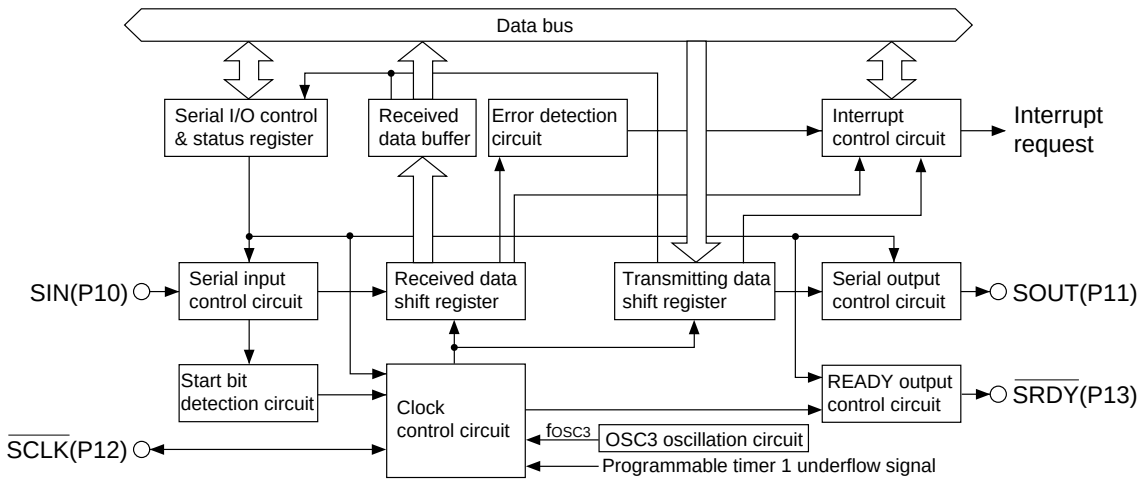


Fig. 5.7.1.1 Configuration of serial interface

5.7.2 Mask option

Since serial interface input / output terminals are shared with the I / O ports, serial interface terminal specifications have necessarily been selected with the mask option for I / O ports.

I/O port pull-up resistors
P10 (SIN) ..... ☐ With resistor ☐ Gate direct
P12 (SCLK) .... ☐ With resistor ☐ Gate direct

Each I / O port terminal is equipped with a pull-up resistor which goes ON in input mode. A selection can be made for each port (one bit unit) as to whether or not the resistor will be used. Specifications (whether the pull-up will be used or not) of P10 (SIN) and P12 (SCLK) which will become input terminals when using the serial interface are decided by settings the options for the I / O port.

When "Gate direct" is selected in the serial I / F mode, be sure that the input terminals do not go into a floating state.

5.7.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMD0 and SMD1 as shown in the table below.

Table 5.7.3.1 Transfer modes

SMD1	SMD0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 5.7.3.2 Terminal settings corresponding to each transfer mode

Mode	SIN	SOUT	SCLK	SRDY
Asynchronous 8-bit	Input	Output	P12	P13
Asynchronous 7-bit	Input	Output	P12	P13
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P13

At initial reset, transfer mode is set to clock synchronous master mode.

■ Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and clock synchronous 8-bit serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the SCLK terminal which enables control of the external (slave side) serial I / O device. Since the SRDY terminal is not utilized in this mode, it can be used as an I / O port.
Figure 5.7.3.1(a) shows the connection example of input / output terminals in the clock synchronous master mode.

■ Clock synchronous slave mode

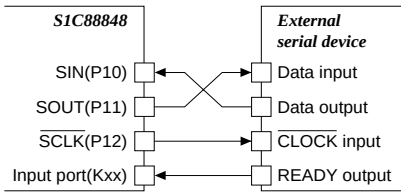
In this mode, a synchronous clock from the external (master side) serial input / output device is utilized and clock synchronous 8-bit serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the SCLK terminal and is utilized by this interface as the synchronous clock.
Furthermore, the SRDY signal indicating the transmit-receive ready status is output from the SRDY terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCS0 and SCS1 used to select the clock source are invalid.
Figure 5.7.3.1(b) shows the connection example of input / output terminals in the clock synchronous slave mode.

■ Asynchronous 7-bit mode

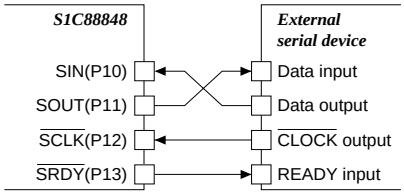
In this mode, asynchronous 7-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd / even / none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the SCLK terminal is not used. Furthermore, since the SRDY terminal is not utilized either, both of these terminals can be used as I / O ports.
Figure 5.7.3.1(c) shows the connection example of input / output terminals in the asynchronous mode.

■ Asynchronous 8-bit mode

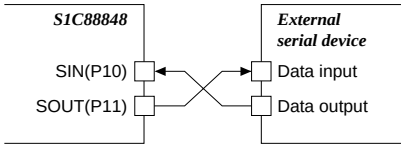
In this mode, asynchronous 8-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd / even / none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the SCLK terminal is not used. Furthermore, since the SRDY terminal is not utilized either, both of these terminals can be used as I / O ports.
Figure 5.7.3.1(c) shows the connection example of input / output terminals in the asynchronous mode.



(a) Clock synchronous master mode



(b) Clock synchronous slave mode



(c) Asynchronous 7-bit/8-bit mode

Fig. 5.7.3.1 Connection examples of serial interface I/O terminals

5.7.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCS0 and SCS1 as shown in table below.

Table 5.7.4.1 Clock source

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

This register setting is invalid in clock synchronous slave mode and the external clock input from the SCLK terminal is used.
When the "programmable timer" is selected, the programmable timer 1 underflow signal is divided by 1/2 and this signal used as the clock source. With respect to the transfer rate setting, see "5.10 Programmable Timer".
At initial reset, the synchronous clock is set to "f_{OSC3} / 16".
Whichever clock is selected, the signal is further divided by 1/16 and then used as the synchronous clock.
Furthermore, external clock input is used as is for SCLK in clock synchronous slave mode.
Table 5.7.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.
When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several 100 µsec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to ON status.

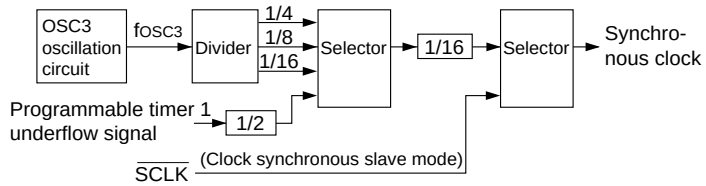


Fig. 5.7.4.1 Division of the synchronous clock

Table 5.7.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	f_{OSC3} = 3.072 MHz		f_{OSC3} = 4.608 MHz		f_{OSC3} = 4.9152 MHz	
	PSC1X	RLD1X	PSC1X	RLD1X	PSC1X	RLD1X
9,600	0 (1/1)	09H	0 (1/1)	0EH	0 (1/1)	0FH
4,800	0 (1/1)	13H	0 (1/1)	1DH	0 (1/1)	1FH
2,400	0 (1/1)	27H	0 (1/1)	3BH	0 (1/1)	3FH
1,200	0 (1/1)	4FH	0 (1/1)	77H	0 (1/1)	7FH
600	0 (1/1)	9FH	0 (1/1)	EFH	0 (1/1)	FFH
300	1 (1/4)	4FH	1 (1/4)	77H	1 (1/4)	7FH
150	1 (1/4)	9FH	1 (1/4)	EFH	1 (1/4)	FFH

5.7.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

■ Shift register and received data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.

Data being transmitted are written to TRXD0–TRXD7 and converted to serial through the shift register and is output from the SOUT terminal.

In the reception section, a received data buffer is installed separate from the shift register.
Data being received are input to the SIN terminal and is converted to parallel through the shift register and written to the received data buffer. Since the received data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

■ Transmit enable register and transmit control bit

For transmitting control, use the transmit enable register TXEN and transmit control bit TXTRG.

The transmit enable register TXEN is used to set the transmitting enable / disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.

The transmit control bit TXTRG is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRG whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.
In addition, TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.

When not transmitting, set TXEN to "0" to disable transmitting status.

■ Receive enable register, receive control bit

For receiving control, use the receive enable register RXEN and receive control bit RXTRG.
Receive enable register RXEN is used to set receiving enable / disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.
With the above setting, receiving begins and serial data input from the SIN terminal goes to the shift register.
The operation of the receive control bit RXTRG is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit RXTRG is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRG to start receiving. (When "1" is written to RXTRG in slave mode, $\overline{\text{SRDY}}$ switches to "0".)
In an asynchronous system, RXTRG is used to prepare for next data receiving. After reading the received data from the received data buffer, write "1" into RXTRG to signify that the received data buffer is empty. If "1" is not written into RXTRG, the overrun error flag OER will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRG.)
In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.

When you do not receive, set RXEN to "0" to disable receiving status.

5.7.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCS0 and SCS1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the $\overline{\text{SCLK}}$ terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the $\overline{\text{SCLK}}$ terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line ($\overline{\text{SCLK}}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

Transfer data is fixed at 8 bits and both transmitting and receiving are conducted with the LSB (bit 0) coming first.

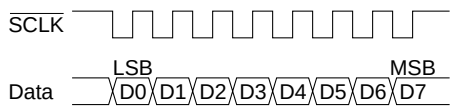


Fig. 5.7.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "5.7.8 Interrupt function".

■ Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input/output ports SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are set as I/O port terminals P10–P13 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.

(3) Setting of transfer mode
Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

Master mode: SMD0 = "0", SMD1 = "0"
Slave mode: SMD0 = "1", SMD1 = "0"

(4) Clock source selection
In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 5.7.4.1.)
This selection is not necessary in the slave mode.

Since all the registers mentioned in (2)–(4) are assigned to the same address, it's possible to set them all with one instruction. The parity enable register EPR is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control
When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See "5.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.3 Oscillation Circuits".)

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN and the receive enable register RXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRG and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUT terminal. When the final bit (MSB) is output, the SOUT terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag FSTRA is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

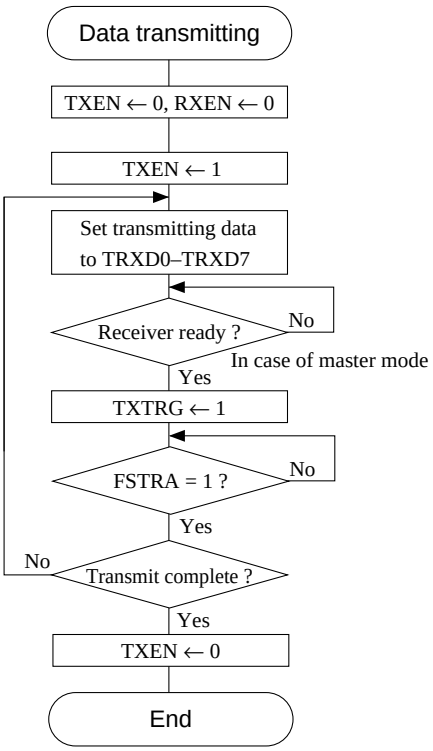


Fig. 5.7.6.2 Transmit procedure in clock synchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN and transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRG and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal. The received data input from the SIN terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the received data buffer and the receiving complete interrupt factor flag FSREC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

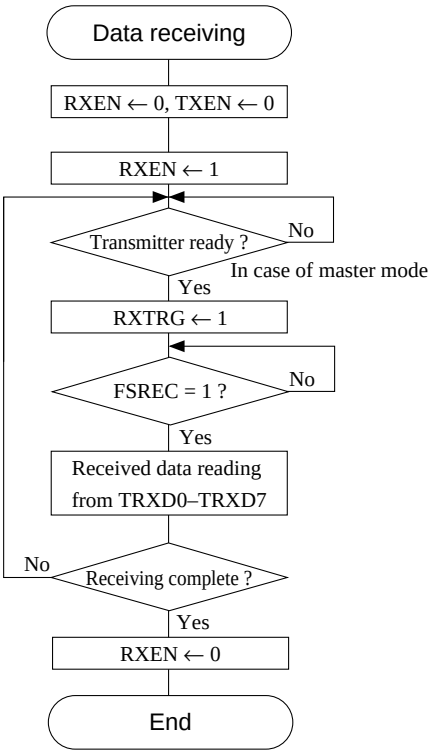


Fig. 5.7.6.3 Receiving procedure in clock synchronous mode

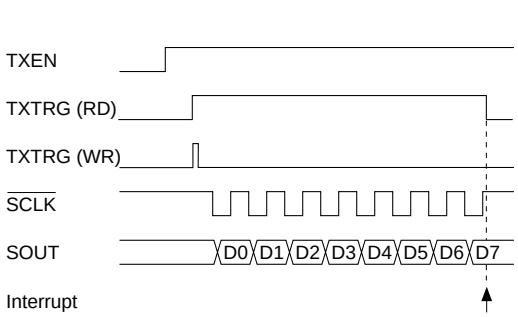
■ Transmit/receive ready ($\overline{\text{SRDY}}$) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an $\overline{\text{SRDY}}$ signal is output to indicate whether or not this serial interface can transmit / receive to the master side (external serial input / output device). This signal is output from the $\overline{\text{SRDY}}$ terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (LOW level) and becomes "1" (HIGH level) when there is a BUSY status, such as during transmit / receive operation.

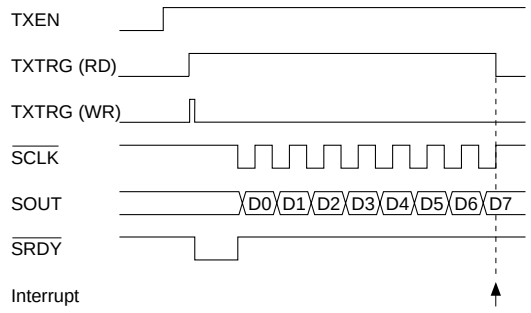
The $\overline{\text{SRDY}}$ signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRG or the receive control bit RXTRG and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge). When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I / O port. At this time, since the $\overline{\text{SRDY}}$ terminal is not set and instead P13 functions as the I / O port, you can apply this port for said control.

■ Timing chart

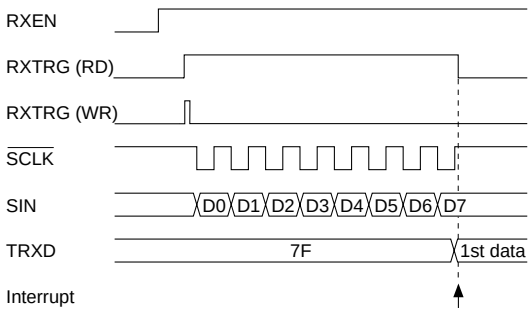
The timing chart for the clock synchronous system transmission is shown in Figure 5.7.6.4.



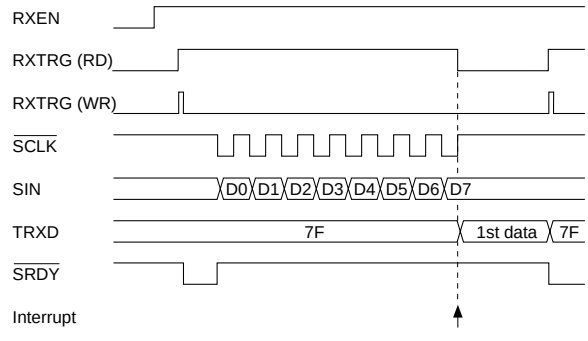
(a) Transmit timing for master mode



(b) Transmit timing for slave mode



(c) Receive timing for master mode



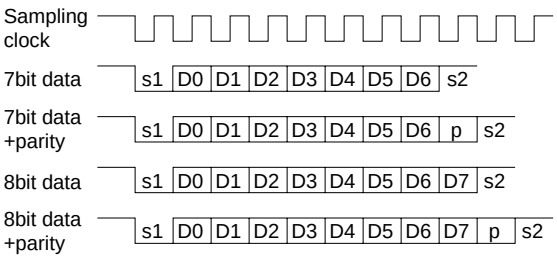
(d) Receive timing for slave mode

Fig. 5.7.6.4 Timing chart (clock synchronous system transmission)

5.7.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start / stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.

For transfer data in the asynchronous 7-bit mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the asynchronous 8-bit mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit and stop bit are respectively fixed at one bit and data is transmitted and received by placing the LSB (bit 0) at the front.



s1 : Start bit (Low level, 1 bit)
s2 : Stop bit (High level, 1 bit)
p : Parity bit

Fig. 5.7.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "5.7.8 Interrupt function" for the serial interface interrupts.

■ Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input / output terminals SIN and SOUT are set as I / O port terminals P10 and P11 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use. $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I / O port terminals P12 and P13.

(3) Setting of transfer mode
Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

7-bit mode: SMD0 = "0", SMD1 = "1"
8-bit mode: SMD0 = "1", SMD1 = "1"

(4) Parity bit selection
When checking and adding parity bits, write "1" into the parity enable register EPR to set to "with parity check". As a result of this setting, in the asynchronous 7-bit mode, it has a 7 bits data + parity bit configuration and in the asynchronous 8-bit mode it has an 8 bits data + parity bit configuration.In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMD.
When "0" is written to the PMD register to select "without parity check" in the asynchronous 7-bit mode, data configuration is set to 7 bits data (no parity) and in the asynchronous 8-bit mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection
Select the clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 5.7.4.1.)
Since all the registers mentioned in (2)–(5) are assigned to the same address, it's possible to set them all with one instruction.

(6) Clock source control
When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See "5.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.3 Oscillation Circuits".)

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7. Also, when 7-bit data is selected, the TRXD7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRG and start transmitting.
This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUT terminal in synchronize to its rising edge. The transmitting data set to the shift register is shifted one bit at a time at each rising edge of the clock thereafter and is output from the SOUT terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output.

The transmitting complete interrupt factor flag FSTRA is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

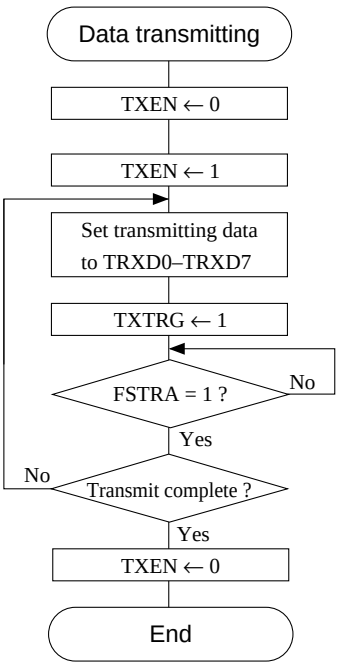


Fig. 5.7.7.2 Transmit procedure in asynchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN to set the receiving disable status and to reset the respective PER, OER, FER flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SIN terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag FSERR is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the received data buffer and the receiving complete interrupt flag FSREC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag FSREC is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the received data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRG to inform that the receive data has been read out. When the following data is received prior to writing "1" to RXTRG, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

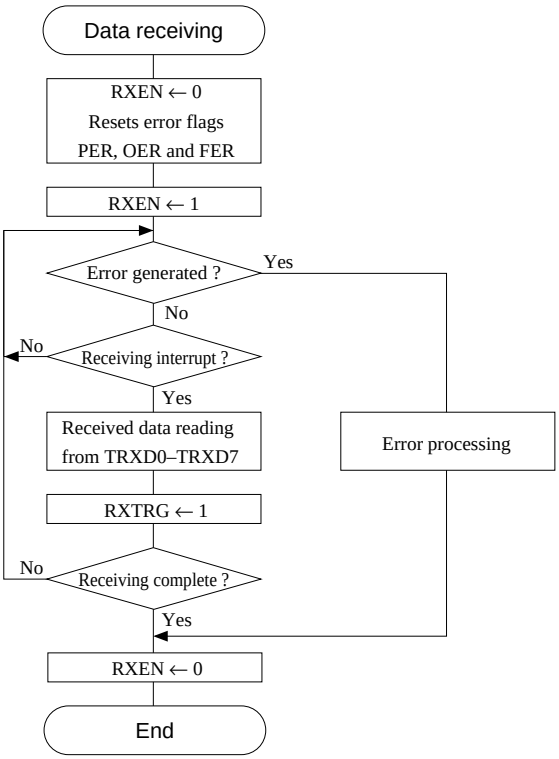


Fig. 5.7.7.3 Receiving procedure in asynchronous mode

■ Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPR register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.

The parity check is performed when data received in the shift register is transferred to the received data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMD register match. When it does not match, it is recognized as an parity error and the parity error flag PER and the error interrupt factor flag FSERR are set to "1".

When interrupt has been enabled, an error interrupt is generated at this point.

The PER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

The received data at this point cannot assured because of the parity error.

(2) Framing error

In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FER and the error interrupt factor flag FSERR are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.

The FER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data for it is loaded into the receive data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receipt, such data cannot be assured.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

When the next data is received before "1" is written to RXTRG, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OER and the error interrupt factor flag FSERR are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OER flag is reset to "0" by writing "1" into it.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

Furthermore, when the timing for writing "1" to RXTRG and the timing for the received data transfer to the received data buffer overlap, it will be recognized as an overrun error.

■ Timing chart

Figure 5.7.7.4 show the asynchronous transfer timing chart.

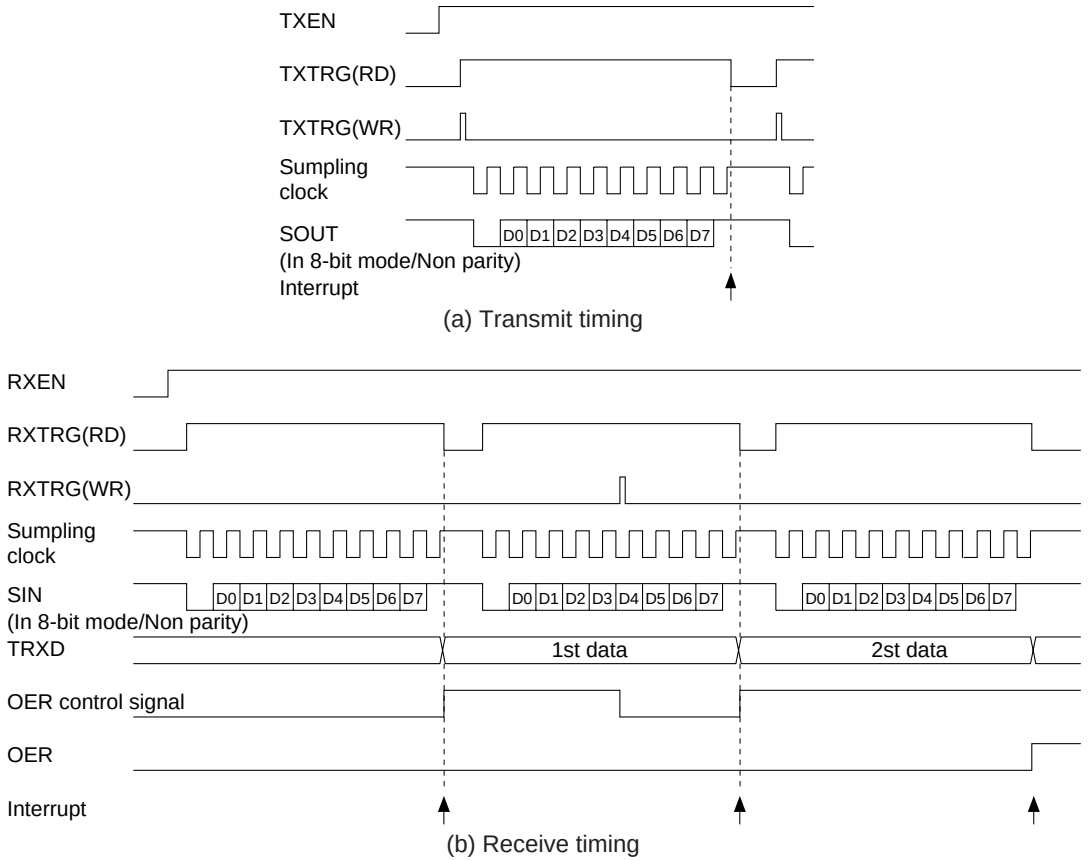


Fig. 5.7.7.4 Timing chart (asynchronous transfer)

5.7.8 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- **Transmitting complete interrupt**
- **Receiving complete interrupt**
- **Error interrupt**

The interrupt factor flag FSxxx and the interrupt enable register ESxxx for the respective interrupt factors are provided and then the interrupt enable/disable can be selected by the software. In addition, a priority level of the serial interface interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSIF0 and PSIF1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.15 Interrupt and Standby Status".
Figure 5.7.8.1 shows the configuration of the serial interface interrupt circuit.

■ Transmitting complete interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag FSTRA to "1". When set in this manner, if the corresponding interrupt enable register ESTRA is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESTRA and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSTRA is set to "1".
The interrupt factor flag FSTRA is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting start (writing "1" to TXTRG) can be controlled by generation of this interrupt factor.
The exception processing vector address for this interrupt factor is set at 000014H.

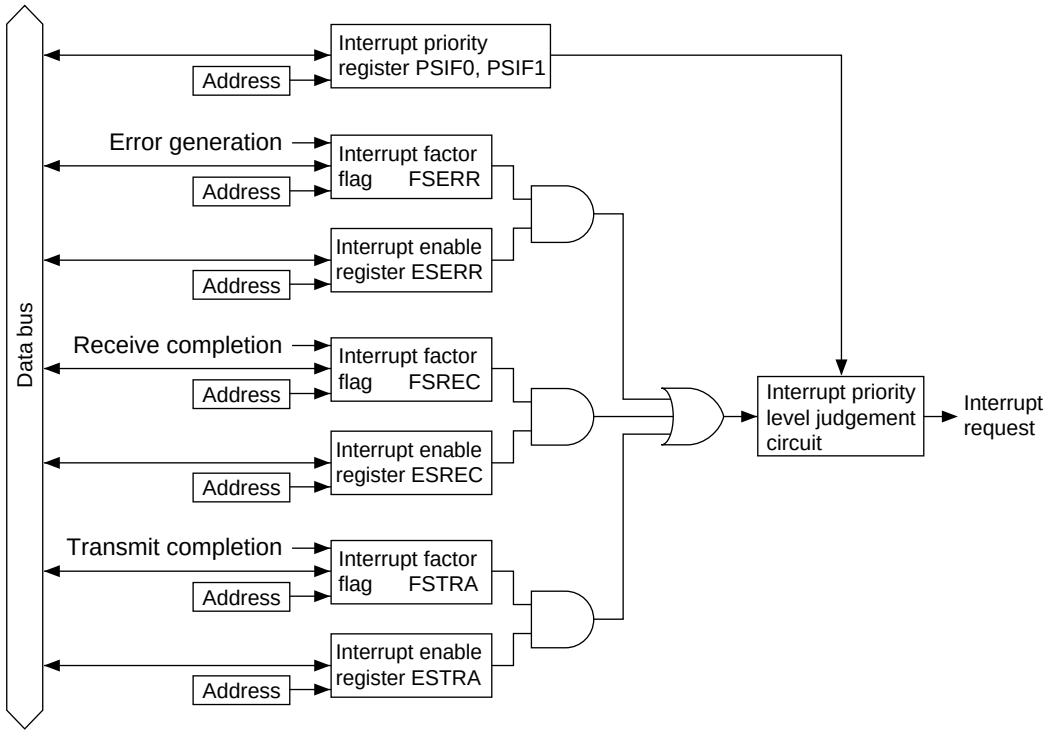


Fig. 5.7.8.1 Configuration of serial interface interrupt circuit

■ Receiving complete interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the received data buffer and it sets the interrupt factor flag FSREC to "1". When set in this manner, if the corresponding interrupt enable register ESREC is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESREC and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSREC is set to "1".
The interrupt factor flag FSREC is reset to "0" by writing "1".

The generation of this interrupt factor permits the received data to be read.

Also, the interrupt factor flag is set to "1" when a parity error or framing error is generated.

The exception processing vector address for this interrupt factor is set at 000012H.

■ Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag FSERR to "1". When set in this manner, if the corresponding interrupt enable register ESERR is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written in the interrupt enable register ESERR and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSERR is set to "1".
The interrupt factor flag FSERR is reset to "0" by writing "1".

Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PER (parity error), OER (overrun error) and FER (framing error).

The exception processing vector address for this interrupt factor is set at 000010H.

5.7.9 Control of serial interface

Table 5.7.9.1 show the serial interface control bits.

Table 5.7.9.1(a) Serial interface control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR	Parity enable register		With parity	Non parity	0	R/W	Only for
	D5	PMD	Parity mode selection		Odd	Even	0	R/W	asynchronous mode
	D4	SCS1	Clock source selection SCS1 SCS0 Clock source 1 1 Programmable timer				0	R/W	In the clock synchronous slave mode, external clock is
	D3	SCS0	1 0 fOSC3 / 4 0 1 fOSC3 / 8 0 0 fOSC3 / 16				0	R/W	selected.
	D2	SMD1	Serial I/F mode selection SMD1 SMD0 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD0	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF	Serial I/F enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER	Framing error flag	R	Error	No error	0	R/W	Only for
				W	Reset (0)	No operation			asynchronous mode
	D5	PER	Parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER	Overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG	Receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN	Receive enable		Enable	Disable	0	R/W	
	D1	TXTRG	Transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN	Transmit enable		Enable	Disable	0	R/W	
00FF4A	D7	TRXD7	Transmit/Receive data D7 (MSB)		High	Low	X	R/W	
	D6	TRXD6	Transmit/Receive data D6				X	R/W	
	D5	TRXD5	Transmit/Receive data D5				X	R/W	
	D4	TRXD4	Transmit/Receive data D4				X	R/W	
	D3	TRXD3	Transmit/Receive data D3				X	R/W	
	D2	TRXD2	Transmit/Receive data D2				X	R/W	
	D1	TRXD1	Transmit/Receive data D1				X	R/W	
	D0	TRXD0	Transmit/Receive data D0 (LSB)				X	R/W	
00FF20	D7	PK01	K00–K07 interrupt priority register		PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00					0	R/W	
	D5	PSIF1	Serial interface interrupt priority register				0	R/W	
	D4	PSIF0					0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register				0	R/W	
	D2	PSW0					0	R/W	
	D1	PTM1	Clock timer interrupt priority register				0	R/W	
	D0	PTM0					0	R/W	

Table 5.7.9.1(b) Serial interface control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10–K11 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10–K11 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

ESIF: 00FF48H•D0

Sets the serial interface terminals (P10–P13).

When "1" is written: Serial input/output terminal
When "0" is written: I/O port terminal
Reading: Valid

The ESIF is the serial interface enable register and P10–P13 terminals become serial input/output terminals (SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) when "1" is written, and they become I/O port terminals when "0" is written.
Also, see Table 5.7.3.2 for the terminal settings according to the transfer modes.
At initial reset, ESIF is set to "0" (I/O port).

SMD0, SMD1: 00FF48H•D1, D2

Set the transfer modes according to Table 5.7.9.2.

Table 5.7.9.2 Transfer mode settings

SMD1	SMD0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

SMD0 and SMD1 can also read out.
At initial reset, this register is set to "0" (clock synchronous master mode).

SCS0, SCS1: 00FF48H•D3, D4

Select the clock source according to Table 5.7.9.3.

Table 5.7.9.3 Clock source selection

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

SCS0 and SCS1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid.
At initial reset, this register is set to "0" (f_{OSC3} / 16).

EPR: 00FF48H•D6

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPR, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPR setting becomes invalid in the clock synchronous mode.
At initial reset, EPR is set to "0" (non parity).

PMD: 00FF48H•D5

Selects odd parity / even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

When "1" is written to PMD, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPR. When "0" has been written to EPR, the parity setting by PMD becomes invalid.
At initial reset, PMD is set to "0" (even parity).

TXEN: 00FF49H•D0

Sets the serial interface to the transmitting enable status.

When "1" is written: Transmitting enable
When "0" is written: Transmitting disable
Reading: Valid

When "1" is written to TXEN, the serial interface shifts to the transmitting enable status and shifts to the transmitting disable status when "0" is written.
Set TXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, TXEN is set to "0" (transmitting disable).

TXTRG: 00FF49H•D1

Functions as the transmitting start trigger and the operation status indicator (transmitting / stop status).

When "1" is read: During transmitting
When "0" is read: During stop

When "1" is written: Transmitting start
When "0" is written: Invalid

Starts the transmitting when "1" is written to TXTRG after writing the transmitting data.
TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRG is set to "0" (during stop).

RXEN: 00FF49H•D2

Sets the serial interface to the receiving enable status.

When "1" is written: Receiving enable
When "0" is written: Receiving disable
Reading: Valid

When "1" is written to RXEN, the serial interface shifts to the receiving enable status and shifts to the receiving disable status when "0" is written.
Set RXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, RXEN is set to "0" (receiving disable).

RXTRG: 00FF49H•D3

Functions as the receiving start trigger or preparation for the following data receiving and the operation status indicator (during receiving / during stop).

When "1" is read: During receiving
When "0" is read: During stop

When "1" is written: Receiving start / following data receiving preparation
When "0" is written: Invalid

RXTRG has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRG in the clock synchronous system, is used as the trigger for the receiving start.
Writes "1" into RXTRG to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{\text{SRDY}}$ becomes "0" at the point where "1" has been written into into the RXTRG.)

RXTRG is used in the asynchronous system for preparation of the following data receiving. Reads the received data located in the received data buffer and writes "1" into RXTRG to inform that the received data buffer has shifted to empty. When "1" has not been written to RXTRG, the overrun error flag OER is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRG, an overrun error occurs.)

In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRG is set to "0" (during stop).

TRXD0–TRXD7: 00FF4AH

During transmitting

Write the transmitting data into the transmit shift register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to starting transmitting.
In the case of continuous transmitting, wait for the transmitting complete interrupt, then write the data.
The TRXD7 becomes invalid for the asynchronous 7-bit mode.
Converted serial data for which the bits set at "1" as HIGH (V_{DD}) level and for which the bits set at "0" as LOW (V_{SS}) level are output from the SOUT terminal.

During receiving

Read the received data.

When "1" is read: HIGH level
When "0" is read: LOW level

The data from the received data buffer can be read out. Since the sift register is provided separately from this buffer, reading can be done during the receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)
Read the data after waiting for the receiving complete interrupt.
When performing parity check in the asynchronous 7-bit mode, "0" is loaded into the 8th bit (TRXD7) that corresponds to the parity bit.
The serial data input from the SIN terminal is level converted, making the HIGH (V_{DD}) level bit "1" and the LOW (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER: 00FF49H•D4

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OER is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when the receiving of data has been completed prior to the writing of "1" to RXTRG in the asynchronous mode.
OER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", OER is set to "0" (no error).

PER: 00FF49H•D5

Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PER is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, if data that does not match the parity is received, a parity error is generated.
PER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", PER is set to "0" (no error).

FER: 00FF49H•D6

Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FER is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving of the asynchronous mode has become "0", a framing error is generated.
FER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", FER is set to "0" (no error).

PSIF0, PSIF1: 00FF20H•D4, D5

Sets the priority level of the serial interface interrupt. The two bits PSIF0 and PSIF1 are the interrupt priority register corresponding to the serial interface interrupt. Table 5.7.9.4 shows the interrupt priority level which can be set by this register.

Table 5.7.9.4 Interrupt priority level settings

PSIF1	PSIF0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESTRA, ESREC, ESERR: 00FF23H•D0, D1, D2

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

ESTRA, ESREC and ESERR are interrupt enable registers that respectively correspond to the interrupt factors for transmitting complete, receiving complete and receiving error. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSTRA, FSREC, FSERR: 00FF25H•D0, D1, D2

Indicates the serial interface interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FSTRA, FSREC and FSERR are interrupt factor flags that respectively correspond to the interrupts for transmitting complete, receiving complete and receiving error and are set to "1" by generation of each factor.
Transmitting complete interrupt factor is generated at the point where the data transmitting of the shift register has been completed.
Receiving complete interrupt factor is generated at the point where the received data has been transferred into the received data buffer.
Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.7.10 Programming notes

(1) Be sure to initialize the serial interface mode in the transmitting / receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation. Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXEN = RXEN = "0".)

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.) Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag FSERR is set to "1" prior to the receiving complete interrupt factor flag FSREC for the time indicated in Table 5.7.10.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag FSREC to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag FSREC is not set to "1" and a receiving complete interrupt is not generated.

Table 5.7.10.1 Time difference between FSERR and FSREC on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several 100 µsec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to ON status.

5.8 Clock Timer

5.8.1 Configuration of clock timer

The S1C88848 has built in a clock timer that uses the OSC1 oscillation circuit as clock source. The clock timer is composed of an 8-bit binary counter that uses the 256 Hz signal dividing f_{OSC1} as its input clock and can read the data of each bit (128–1 Hz) by software.
Normally, this clock timer is used for various timing functions such as clocks.
The configuration of the clock timer is shown in Figure 5.8.1.1.

5.8.2 Interrupt function

The clock timer can generate an interrupt by each of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals.
The configuration of the clock timer interrupt circuit is shown in Figure 5.8.2.1.

Interrupts are generated by respectively setting the corresponding interrupt factor flags FTM32, FTM8, FTM2 and FTM1 at the falling edge of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals to "1". Interrupt can be prohibited by the setting the interrupt enable registers ETM32, ETM8, ETM2 and ETM1 corresponding to each interrupt factor flag.
In addition, a priority level of the clock timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PTM0 and PTM1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.15 Interrupt and Standby Status".

The exception processing vector addresses for each interrupt factor are respectively set as shown below.

32 Hz interrupt:	00001CH
8 Hz interrupt:	00001EH
2 Hz interrupt:	000020H
1 Hz interrupt:	000022H

Figure 5.8.2.2 shows the timing chart for the clock timer.

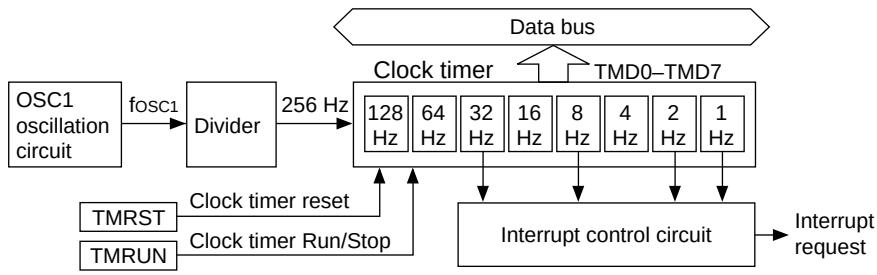


Fig. 5.8.1.1 Configuration of clock timer

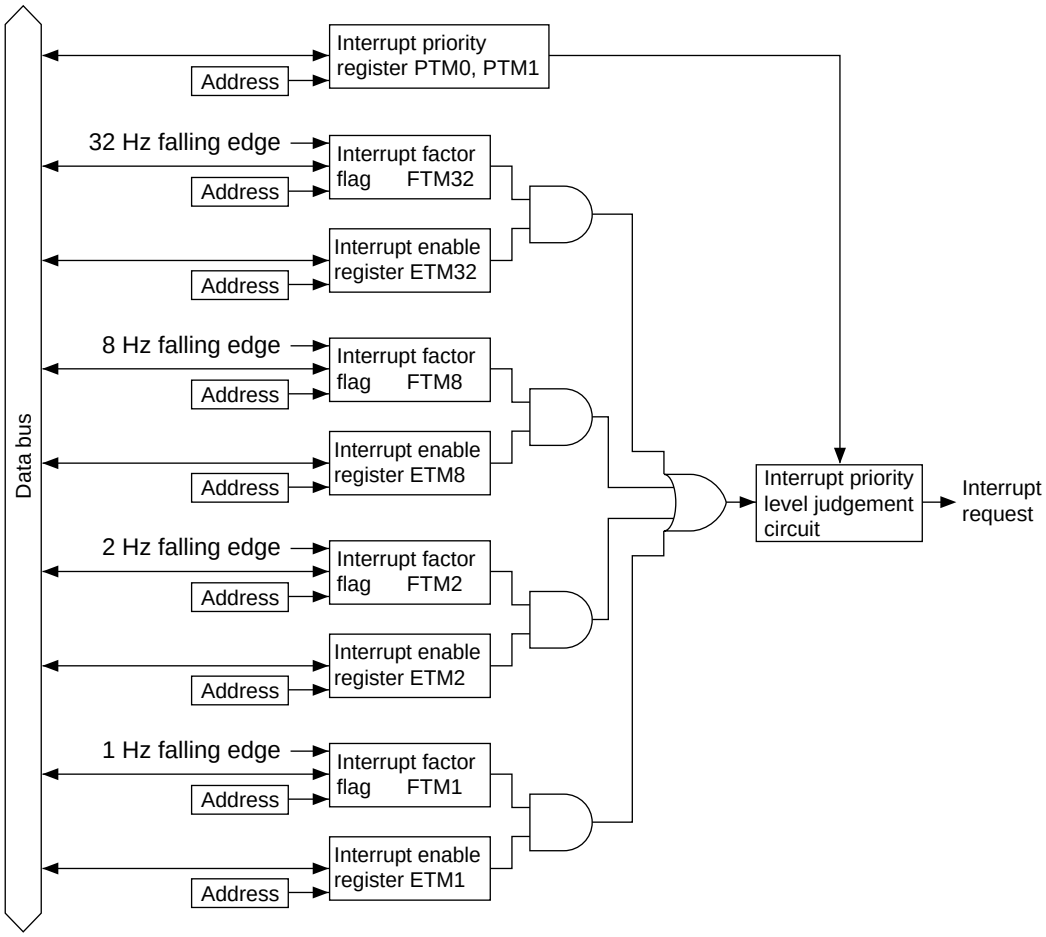


Fig. 5.8.2.1 Configuration of clock timer interrupt circuit

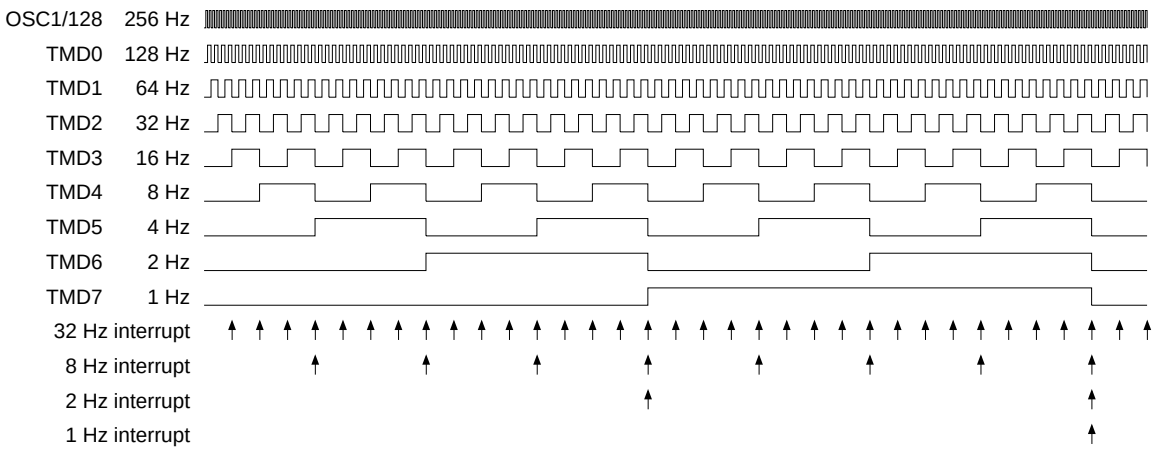


Fig. 5.8.2.2 Timing chart of clock timer

5.8.3 Control of clock timer

Table 5.8.3.1 shows the clock timer control bits.

Table 5.8.3.1 Clock timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz			0	R	
	D5	TMD5	Clock timer data 4 Hz			0	R	
	D4	TMD4	Clock timer data 8 Hz			0	R	
	D3	TMD3	Clock timer data 16 Hz			0	R	
	D2	TMD2	Clock timer data 32 Hz			0	R	
	D1	TMD1	Clock timer data 64 Hz			0	R	
	D0	TMD0	Clock timer data 128 Hz			0	R	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag			0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	

TMD0–TMD7: 00FF41H

The clock timer data can be read out.
Each bit of TMD0–TMD7 and frequency correspondence are as follows:

TMD0:	128Hz	TMD4:	8Hz
TMD1:	64Hz	TMD5:	4Hz
TMD2:	32Hz	TMD6:	2Hz
TMD3:	16Hz	TMD7:	1Hz

Since the TMD0–TMD7 is exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

TMRST: 00FF40H•D1

Resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to the TMRST.
When the clock timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the TMRST.
Since the TMRST is exclusively for writing, it always becomes "0" during reading.

TMRUN: 00FF40H•D0

Controls RUN / STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer starts up-counting by writing "1" to the TMRUN and stops by writing "0".
In the STOP status, the count data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the TMRUN is set to "0" (STOP).

PTM0, PTM1: 00FF20H•D0, D1

Sets the priority level of the clock timer interrupt. The two bits PTM0 and PTM1 are the interrupt priority register corresponding to the clock timer interrupt. Table 5.8.3.2 shows the interrupt priority level which can be set by this register.

Table 5.8.3.2 Interrupt priority level settings

PTM1	PTM0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ETM1, ETM2, ETM8, ETM32: 00FF22H•D0–D3

Enables or disables the generation of an interrupt for the CPU.

When "1" is written:	Interrupt enabled
When "0" is written:	Interrupt disabled
Reading:	Valid

The ETM1, ETM2, ETM8 and ETM32 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 2 Hz, 8 Hz and 32 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FTM1, FTM2, FTM8, FTM32: 00FF24H•D0–D3

Indicates the clock timer interrupt generation status.

When "1" is read:	Interrupt factor present
When "0" is read:	Interrupt factor not present
When "1" is written:	Resets factor flag
When "0" is written:	Invalid

The FTM1, FTM2, FTM8 and FTM32 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 2 Hz, 8 Hz and 32 Hz and are set to "1" at the falling edge of each signal.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.8.4 Programming notes

(1) The clock timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to the TMRUN, the timer shifts to STOP status when the counter is incremented "1". The TMRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.8.4.1 shows the timing chart of the RUN / STOP control.

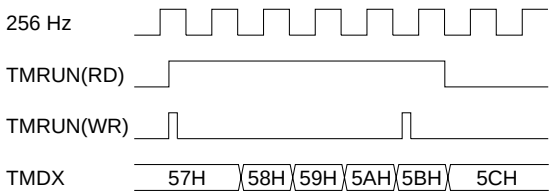


Fig. 5.8.4.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the clock timer is in the RUN status (TMRUN = "1"). The clock timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (TMRUN = "0") prior to executing the SLP instruction.

5.9 Stopwatch Timer

5.9.1 Configuration of stopwatch timer

The S1C88848 has a built-in 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is composed of a 4-bit 2 stage BCD counter (1/100 sec units and 1/10 sec units) that makes the 256 Hz signal that divides the fOSC1 the input clock and it can read the count data by software.
Figure 5.9.1.1 shows the configuration of the stopwatch timer.
The stopwatch timer can be used as a timer different from the clock timer and can easily realize stopwatch and other such functions by software.

5.9.2 Count up pattern

The stopwatch timer is respectively composed of the 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7.

Figure 5.9.2.1 shows the count up pattern of the stopwatch timer.

The feedback dividing circuit generates an approximate 100 Hz signal at 2/256 sec and 3/256 sec intervals from a 256 Hz signal divided from fOSC1.

The 1/100 sec counter (SWD0–SWD3) generates an approximate 10 Hz signal at 25/256 sec and 26/256 sec intervals by counting the approximate 100 Hz signal generated by the feedback dividing circuit in 2/256 sec and 3/256 sec intervals. The count-up is made approximately 1/100 sec counting by the 2/256 sec and 3/256 sec intervals.

The 1/10 sec counter (SWD4–SWD7) generates a 1 Hz signal by counting the approximate 10 Hz signal generated by the 1/100 sec counter at 25/256 sec and 26/256 sec intervals in 4:6 ratios.

The count-up is made approximately 1/10 sec counting by 25/256 sec and 26/256 sec intervals.

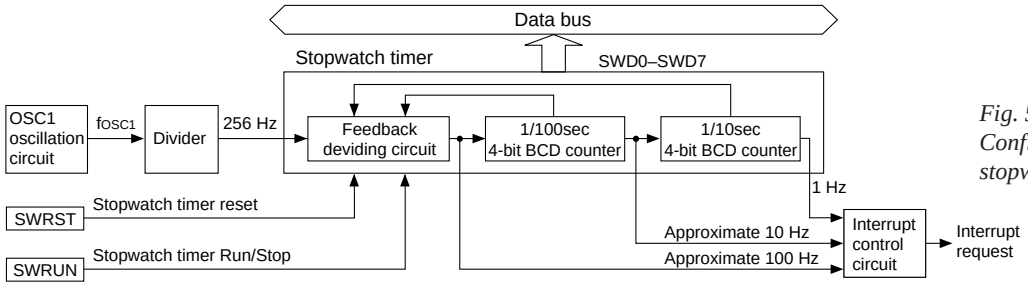


Fig. 5.9.1.1 Configuration of stopwatch timer

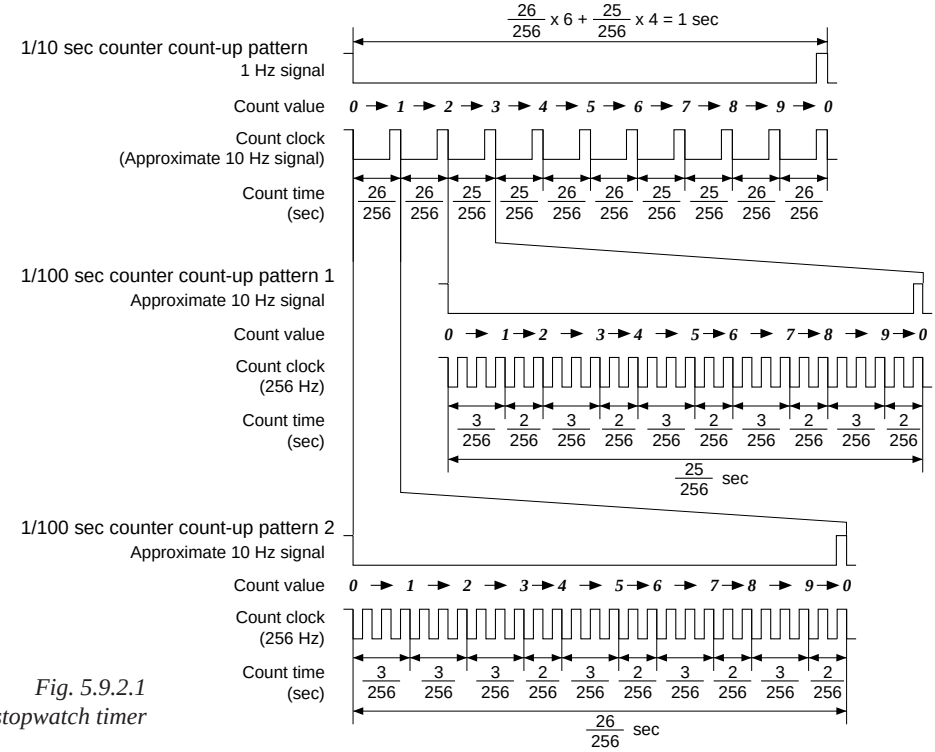


Fig. 5.9.2.1 Count-up pattern of stopwatch timer

5.9.3 Interrupt function

The stopwatch timer can generate an interrupt by each of the 100 Hz (approximately 100 Hz), 10 Hz (approximately 10 Hz) and 1 Hz signals.
Figure 5.9.3.1 shows the configuration of the stopwatch timer interrupt circuit.

The corresponding factor flags FSW100, FSW10 and FSW1 are respectively set to "1" at the falling edge of the 100 Hz, 10 Hz and 1 Hz signal and an interrupt is generated. Interrupt can be prohibited by the setting of the interrupt enable registers ESW100, ESW10 and ESW1 corresponding to each interrupt factor flag.

In addition, a priority level of the stopwatch timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSW0 and PSW1.
For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.15 Interrupt and Standby Status".
The exception processing vector addresses of each interrupt factor are respectively set as shown below.

100 Hz interrupt: 000016H
10 Hz interrupt: 000018H
1 Hz interrupt: 00001AH

Figure 5.9.3.2 shows the timing chart for the stopwatch timer.

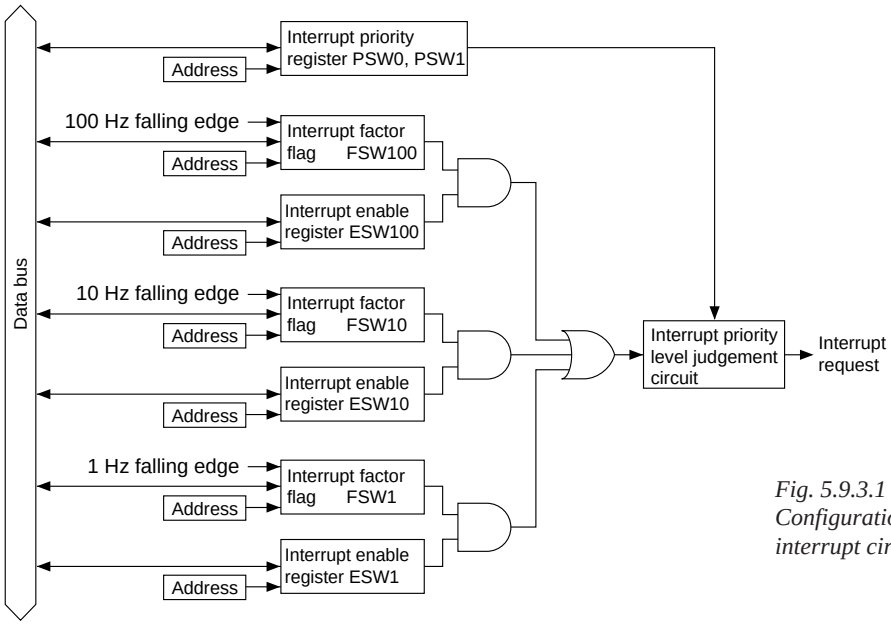


Fig. 5.9.3.1
Configuration of the stopwatch timer interrupt circuit

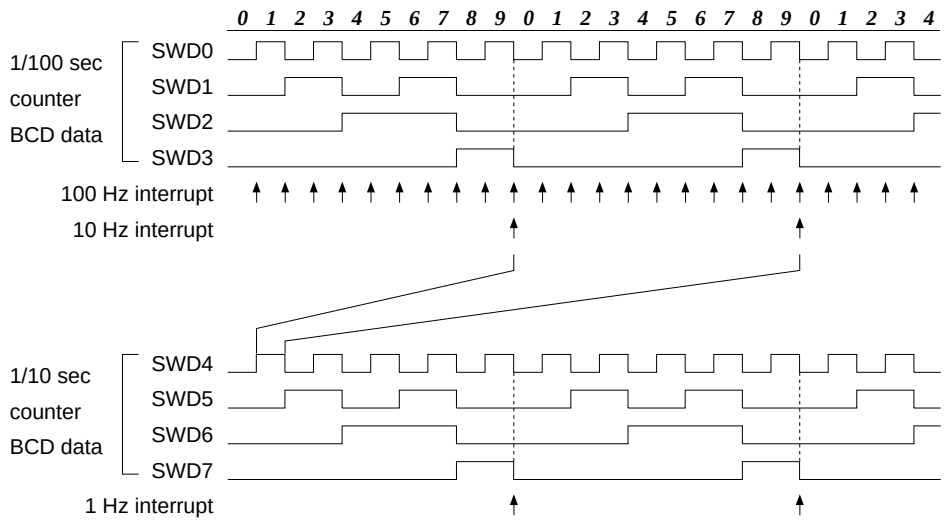


Fig. 5.9.3.2
Stopwatch timer timing chart

5.9.4 Control of stopwatch timer

Table 5.9.4.1 shows the stopwatch timer control bits.

Table 5.9.4.1 Stopwatch timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data			–	R	
	D6	SWD6				–	R	
	D5	SWD5	BCD (1/10 sec)			–	R	
	D4	SWD4				–	R	
	D3	SWD3	Stopwatch timer data			–	R	
	D2	SWD2				–	R	
	D1	SWD1	BCD (1/100 sec)			–	R	
	D0	SWD0				–	R	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 Priority PTM1 PTM0 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag			0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	

SWD0–SWD7: 00FF43H

The stopwatch timer data can be read out.
Higher and lower nibbles and BCD digit correspondence are as follows:

SWD0–SWD3: BCD (1/100sec)
SWD4–SWD7: BCD (1/10sec)

Since SWD0–SWD7 are exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

SWRST: 00FF42H•D1

Resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset by writing "1" to the SWRST. When the stopwatch timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the SWRST.
Since the SWRST is exclusively for writing, it always becomes "0" during reading.

SWRUN: 00FF42H•D0

Controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The stopwatch timer starts up-counting by writing "1" to the SWRUN and stops by writing "0".
In the STOP status, the timer data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the SWRUN is set at "0" (STOP).

PSW0, PSW1: 00FF20H•D2, D3

Sets the priority level of the stopwatch timer interrupt.
The two bits PSW0 and PSW1 are the interrupt priority register corresponding to the stopwatch timer interrupt. Table 5.9.4.2 shows the interrupt priority level which can be set by this register.

Table 5.9.4.2 Interrupt priority level settings

PSW1	PSW0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESW1, ESW10, ESW100: 00FF22H•D4, D5, D6

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

The ESW1, ESW10 and ESW100 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 10 Hz and 100 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSW1, FSW10, FSW100: 00FF24H•D4, D5, D6

Indicates the stopwatch timer interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

The FSW1, FSW10 and FSW100 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 10 Hz and 100 Hz and are set to "1" in synchronization with the falling edge of each signal. When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.9.5 Programming notes

(1) The stopwatch timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the SWRUN register. Consequently, when "0" is written to the SWRUN, the timer shifts to STOP status when the counter is incremented "1". The SWRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.9.5.1 shows the timing chart of the RUN / STOP control.

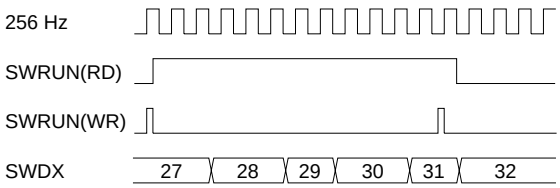


Fig. 5.9.5.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the stopwatch timer is in the RUN status (SWRUN = "1"). The stopwatch timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (SWRUN = "0") prior to executing the SLP instruction.

5.10 Programmable Timer

5.10.1 Configuration of programmable timer

The S1C88848 has four systems of 8-bit programmable timers (timer 0 through timer 3) built-in. Each timer consists of an 8-bit presettable down counter and timers 0 and 1 or timers 2 and 3 can be cascaded. Consequently, each pair of timers can be used as 8-bit × 2 channels or 16-bit × 1 channel of programmable timer. They also have an event counter function and a pulse width measurement function using the K10 or K11 input port terminal.

Figure 5.10.1.1 shows the configuration of the programmable timer.

Programmable setting of the transfer rate is possible, due to the fact that the programmable timer 1 underflow signal can be used as a synchronous clock for the serial interface.
Furthermore, the halved underflow signals (TOUT) of timers 0 and 1 can also be output externally from the R27 output port terminal. The R26 output port terminal can also be used to output the $\overline{\text{TOUT}}$ signal (TOUT inverted signal) by mask option.

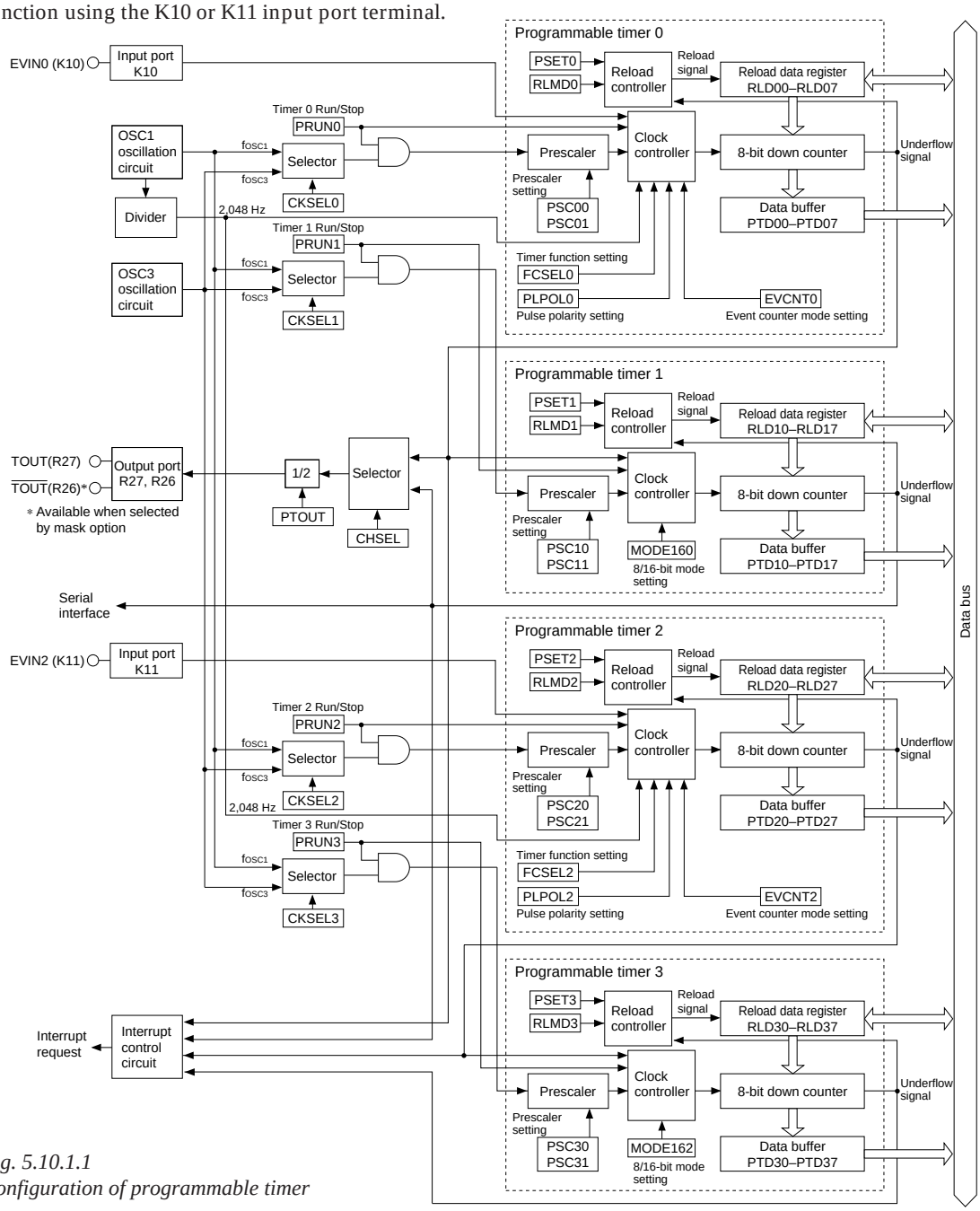


Fig. 5.10.1.1
Configuration of programmable timer

5.10.2 Count operation and setting basic mode

Here we will explain the basic operation and setting of the programmable timer.

■ Setting of initial value and counting down

The timers 0 to 3 have a down counter and reload data register.

The reload data register RLDx0–RLDx7 (register for timer x, x = 0 to 3) is used to set the initial value of the counter.
By writing "1" to the preset control bit PSETx, the down counter loads the initial value set in the reload data register RLDx.
Therefore, down-counting is executed from the stored initial value according to the input clock.
The register PRUNx is provided to control the RUN / STOP for each timer.
After the reload data has been preset into the counter, down-counting is begun by writing "1" to this register. When "0" is written, the clock input is disabled and the count stops.
The control of this RUN / STOP has no affect on the counter data. The counter data is maintained even during the stoppage of the counter and it can start the count, continuing from that data.

The reading of the counter data can be done through the data buffers PTDx0–PTDx7 with optional timing.
When the down-counting has progressed and an underflow is generated, the counter reloads the initial value set in the reload data register RLDx.
This underflow signal controls an interrupt generation, pulse (TOUT signal) output and serial interface clocking, in addition to reloading the counter.

■ Continuous/one-shot mode setting

By writing "1" to the continuous / one-shot mode selection register CONTx, the programmable timer is set to the continuous mode. In the continuous mode, the initial counter value is automatically loaded when an underflow is generated, and counting is continued. This mode is suitable when programmable intervals are necessary (such as an interrupt and a synchronous clock for the serial interface).
On the other hand, when writing "0" to the register CONTx, the programmable timer is set to the one-shot mode. The counter loads an initial value and stops when an underflow is generated. At this time, the RUN / STOP control register PRUNx is automatically reset to "0". After the counter stops, a one-shot count can be performed once again by writing "1" to register PRUNx. This mode is suitable for single time measurement, for example.

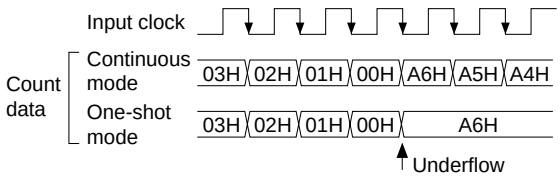


Fig. 5.10.2.2 Continuous mode and one-shot mode

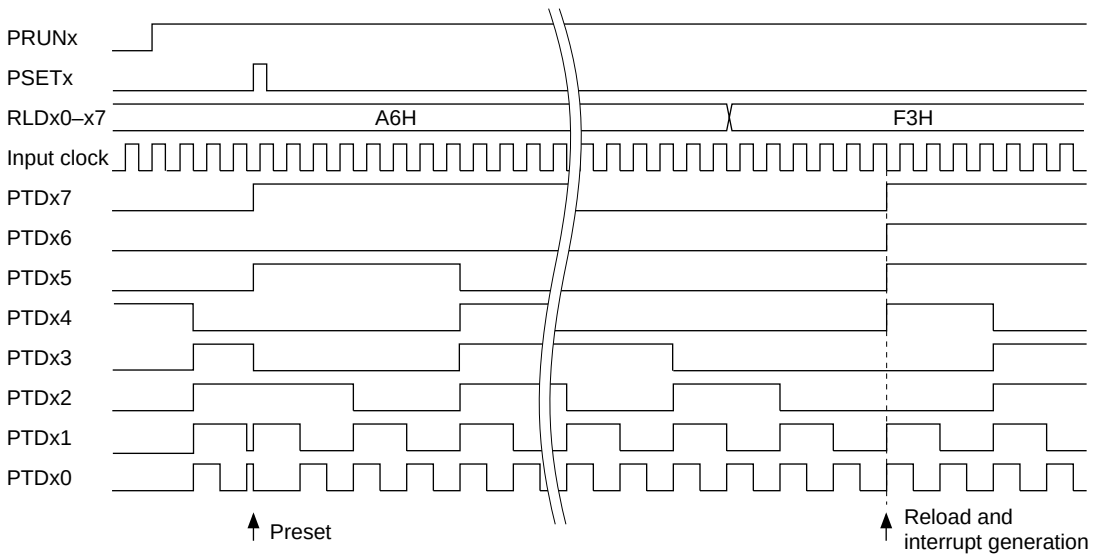


Fig. 5.10.2.1 Basic operation timing of the counter

■ 8/16-bit mode setting

By writing "0" to the 8/16-bit mode selection register MODE160 (MODE162), timer 0 and timer 1 (timer 2 and timer 3) are set as independent timers in 8-bit × 2 channels. In this mode, timer 0 and timer 1 (timer 2 and timer 3) can be controlled individually and each of them operates independently.

On the other hand, when writing "1" to the register MODE160 (MODE162), timer 0 and timer 1 (timer 2 and timer 3) are set as 1 channel 16-bit timer. This is done by setting timer 0 (timer 2) to the lower 8 bits, and timer 1 (timer 3) to the upper 8 bits. The timer is controlled by the timer 0 (timer 2) registers. In this case, the control registers for timer 1 (timer 3) are invalid. (PRUN1 and PRUN3 are fixed at "0".)

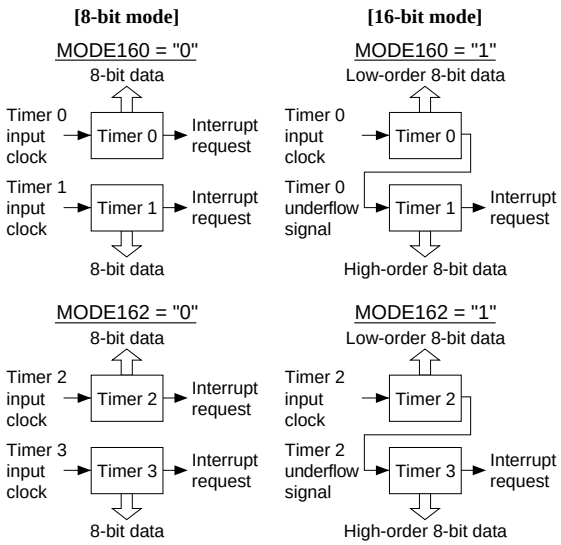


Fig. 5.10.2.3 8/16-bit mode setting and counter configuration

5.10.3 Setting of input clock

A prescaler has been provided for each timer. The prescaler generates the input clock for each timer by dividing the source clock signal from the OSC1 or OSC3 oscillation circuit.

The source clock and the dividing ratio of the prescaler can be selected individually for each timer by software.

The input clocks are configured by the following sequence.

(1) Selection of source clock

Select the source clock (OSC1 or OSC3) for each prescaler. This is done using the source clock selection register CKSELx: when "0" is written, OSC1 is selected and when "1" is written, OSC3 is selected. When the 16-bit mode is selected, the source clock is selected by the register CKSEL0 (timer 0) or CKSEL2 (timer 2), and the settings of the register CKSEL1 (timer 1) or CKSEL3 (timer 3) becomes invalid.

When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer.

From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several 100 µsec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)

At initial reset, OSC3 oscillation circuit is set to ON status.

(2) Selection of prescaler dividing ratio

Select the dividing ratio of each prescaler from among 4 types. This selection is done by the prescaler dividing ratio selection register PSCx0/PSCx1. Setting value and dividing ratio correspondence are shown in Table 5.10.3.1.

Table 5.10.3.1 Selection of prescaler dividing ratio

PSC31 PSC21 PSC11 PSC01	PSC30 PSC20 PSC10 PSC00	Prescaler dividing ratio
1	1	Source clock / 64
1	0	Source clock / 16
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PRUNx, the source clock is input to the prescaler. Therefore, the clock with selected dividing ratio is input to the timer and the timer starts counting down.

When the 16-bit mode has been selected, the dividing ratio for the source clock is selected by register PSC0 (timer 0) or PSC2 (timer 2) and the setting of the register PSC1 (timer 1) or PSC3 (timer 3) becomes invalid.

5.10.4 Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a timer that obtains fixed cycles using the OSC1 or OSC3 oscillation circuit as a clock source.
See "5.10.2 Count operation and basic mode setting" for basic operation and control, and "5.10.3 Setting input clock" for the clock source and setting of the prescaler.

5.10.5 Event counter mode

Timer 0 includes an even counter function that counts by inputting an external clock (EVIN0) to input port K10. Also timer 2 has an event counter function that uses the K11 input port terminal (EVIN2). This function is selected by writing "1" to the timer 0 (timer 2) counter mode selection register EVCNT0 (EVCNT2).
When the event counter mode is selected, timer 0 (timer 2) operates as an event counter and timer 1 (timer 3) operates as a normal timer in 8-bit mode. In the 16-bit mode, timers 0 and 1 (timers 2 and 3) operate as 1 channel 16-bit event counter. In the event counter mode, since the timer 0 (timer 2) is clocked externally, the setting of the registers PSC0 (PSC2) become invalid.
Count down timing can be controlled by either the falling edge or rising edge selected by the timer 0 (timer 2) pulse polarity selection register PLPOL0 (PLPOL2). When "0" is written to the register PLPOL0 (PLPOL2), the falling edge is selected, and when "1" is written, the rising edge is selected. The timing is shown in Figure 5.10.5.1.

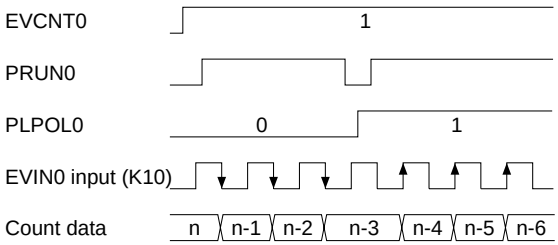


Fig. 5.10.5.1 Timing chart for event counter mode (timer 0)

The event counter also includes a noise rejecter to eliminate noise such as chattering for the external clock (EVIN0, EVIN2). This function is selected by writing "1" to the timer 0 (timer 2) function selection register FCSEL0 (FCSEL2).

For a reliable count when "with noise rejecter" is selected, you must allow 0.98 msec or more pulse width for both LOW and HIGH levels. (The noise rejecter allows clocking counter at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K10 or K11 input port terminal. Consequently, the pulse width that can reliably be rejected is 0.48 msec.)
Figure 5.10.5.2 shows the count down timing with the noise rejecter selected.

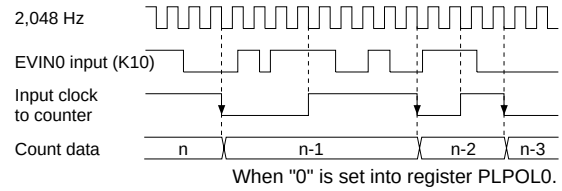


Fig. 5.10.5.2 Count down timing with noise rejecter (timer 0)

The event counter mode is the same as the timer mode except that the clock is external (EVIN0, EVIN2).
See "5.10.2 Count operation and setting basic mode" for the basic operation and control.

5.10.6 Pulse width measurement timer mode

Timer 0 includes a pulse width measurement function that measures the width of the input signal (EVIN0) to the K10 input port terminal. Also timer 2 has a pulse width measurement function that uses the K11 input port terminal (EVIN2). This function is selected by writing "1" to the timer function selection register FCSEL0 (FCSEL2) when in the timer mode (EVCNT0 = "0" in timer 0, EVCNT2 = "0" in timer 2).
When the pulse width measurement mode is selected, timer 0 (timer 2) operates as an pulse width measurement and timer 1 (timer 3) operates as a normal timer in 8-bit mode. In the 16-bit mode, timers 0 and 1 (timers 2 and 3) operate as 1 channel 16-bit pulse width measurement.
The level of the input signal (EVIN0, EVIN2) for measurement can be changed either a LOW or HIGH level by the timer 0 (timer 2) pulse polarity selection register PLPOL0 (PLPOL2). When "0" is written to register PLPOL0 (PLPOL2), a LOW level width is measured and when "1" is written, a HIGH level width is measured. The timing is shown in Figure 5.10.6.1.
The pulse width measurement timer mode is the same as the timer mode except that the input clock is controlled by the level of the signal (EVIN0 or EVIN2) input to the K10 or K11 input port terminal.
See "5.10.2 Count operation and setting basic mode" for the basic operation and control.

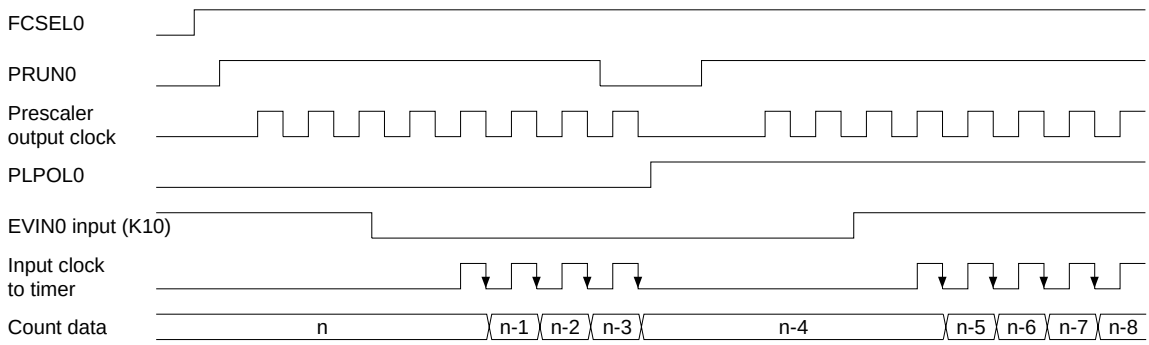


Fig. 5.10.6.1 Timing chart for pulse width measurement timer mode (timer 0)

5.10.7 Interrupt function

The programmable timer can generate an interrupt due to an underflow signal of each timer. Figure 5.10.7.1 shows the configuration of the programmable timer interrupt circuit.
The respectively corresponding interrupt factor flag FPTx is set to "1" and an interrupt is generated by an underflow signal of timer x. Interrupt can also be disabled by setting the interrupt enable register EPTx corresponding to the interrupt factor flag.
In addition, a priority level of the programmable timer interrupt for the CPU can be set at levels 0 to 3 using the interrupt priority registers PPT0 and PPT1 (for timers 0 and 1), and PPT2 and PPT3 (for timers 2 and 3).

For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.15 Interrupt and Standby Status".
The exception processing vector addresses of each interrupt factor are respectively set as shown below.

Programmable timer 0 interrupt: 000008H
Programmable timer 1 interrupt: 000006H
Programmable timer 2 interrupt: 000028H
Programmable timer 3 interrupt: 000026H

When the 16-bit mode is selected, the interrupt factor flag FPT0 (FPT2) is not set to "1" and a timer 0 (timer 2) interrupt cannot be generated. (In the 16-bit mode, the interrupt factor flag FPT1 (FPT3) is set to "1" by an underflow of the 16-bit counter.

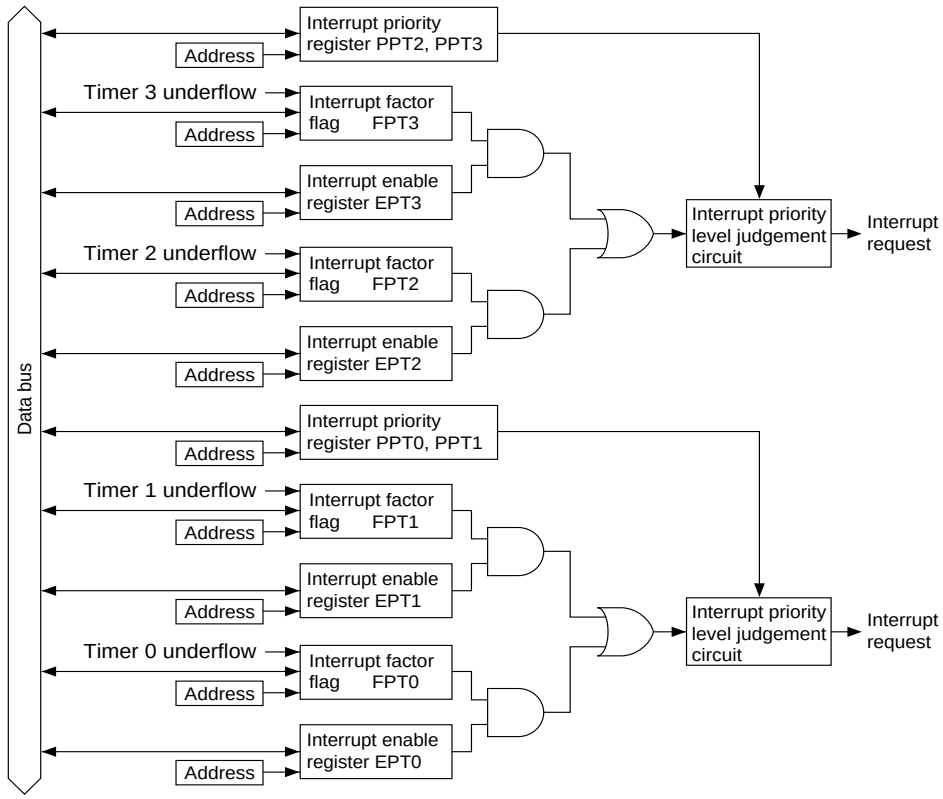


Fig. 5.10.7.1 Configuration of programmable timer interrupt circuit

5.10.8 Setting of TOUT output

The programmable timer can generate the TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated from the above mentioned underflow signal by halving the frequency. The timer underflow which is to be used can be selected by the TOUT output channel selection register CHSEL. When writing "0" to register CHSEL, timer 0 is selected and when "1" is written, timer 1 is selected. However, in the 16-bit mode, it is fixed in timer 1 (underflow of the 16-bit timer) and the setting of register CHSEL becomes invalid.
Figure 5.10.8.1 shows the TOUT signal waveform when channel switching.

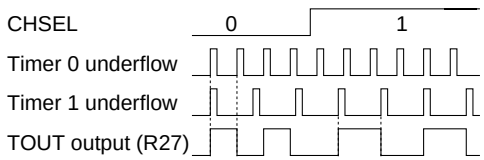


Fig. 5.10.8.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R27 output port terminal, and the programmable clock can be supplied to an external device.
Furthermore, the R26 output port terminal can be used to output the $\overline{\text{TOUT}}$ signal (TOUT inverted signal) by mask option.
The configuration of the output ports R27 and R26 is shown in Figure 5.10.8.2.

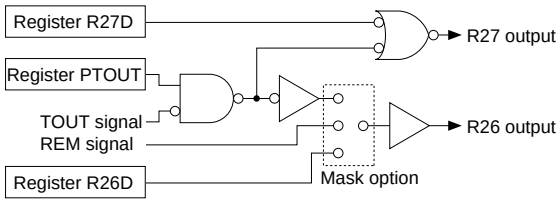


Fig. 5.10.8.2 Configuration of R27 and R26

The output control for the TOUT ($\overline{\text{TOUT}}$) signal is done by the register PTOUT. When you set "1" for the PTOUT, the TOUT ($\overline{\text{TOUT}}$) signal is output from the R27 (R26) output port terminal. When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D. The data register R26D does not affect the $\overline{\text{TOUT}}$ output.

Since the TOUT signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.
Figure 5.10.8.3 shows the output waveform of TOUT signal.

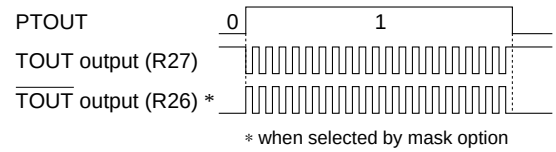


Fig. 5.10.8.3 TOUT output waveform

5.10.9 Transmission rate setting of serial interface

The underflow signal of the timer 1 can be used to clock the serial interface. The transmission rate setting in this case is made in registers PSC1 and RLD1, and is used to set the count mode to the reload count mode (RLMD1 = "1").
Since the underflow signal of the timer 1 is divided by 1/32 in the serial interface, the value set in register RLD1 which corresponds to the transmission rate is shown in the following expression:

$$\mathbf{RLD1 = fosc / (32*bps*4^{PSC1}) - 1}$$

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transmission rate
PSC1: Setting value to the register PSC1 (0–3)

(00H can be set to RLD1)

Table 5.10.9.1 shows an example of the transmission rate setting when the OSC3 oscillation circuit is used as a clock source.

Table 5.10.9.1 Example of transmission rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	f_{OSC3} = 3.072 MHz		f_{OSC3} = 4.608 MHz		f_{OSC3} = 4.9152 MHz	
	PSC1	RLD1	PSC1	RLD1	PSC1	RLD1
9,600	0 (1/1)	09H	0 (1/1)	0EH	0 (1/1)	0FH
4,800	0 (1/1)	13H	0 (1/1)	1DH	0 (1/1)	1FH
2,400	0 (1/1)	27H	0 (1/1)	3BH	0 (1/1)	3FH
1,200	0 (1/1)	4FH	0 (1/1)	77H	0 (1/1)	7FH
600	0 (1/1)	9FH	0 (1/1)	EFH	0 (1/1)	FFH
300	1 (1/4)	4FH	1 (1/4)	77H	1 (1/4)	7FH
150	1 (1/4)	9FH	1 (1/4)	EFH	1 (1/4)	FFH

5.10.10 Control of programmable timer

Table 5.10.10.1 shows the programmable timer control bits.

Table 5.10.10.1(a) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE160	8/16-bit mode selection (timer 0/1)	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF31	D7	EVCNT0	Timer 0 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL0	Timer 0 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 0 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL0	Timer 0 pulse polarity selection: Down count timing in event counter mode	Rising edge of K10 input	Falling edge of K10 input	0	R/W	
			Timer 0 pulse polarity selection: In pulse width measurement mode	High level measurement for K10 input	Low level measurement for K10 input			
	D4	PSC01	Timer 0 prescaler dividing ratio selection			0	R/W	
	D3	PSC00	PSC01 PSC00 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT0	Timer 0 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET0	Timer 0 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN0	Timer 0 Run/Stop control	Run	Stop	0	R/W	
00FF32	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC11	Timer 1 prescaler dividing ratio selection			0	R/W	
	D3	PSC10	PSC11 PSC10 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT1	Timer 1 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET1	Timer 1 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN1	Timer 1 Run/Stop control	Run	Stop	0	R/W	
00FF33	D7	RLD07	Timer 0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD06	Timer 0 reload data D6			1	R/W	
	D5	RLD05	Timer 0 reload data D5			1	R/W	
	D4	RLD04	Timer 0 reload data D4			1	R/W	
	D3	RLD03	Timer 0 reload data D3			1	R/W	
	D2	RLD02	Timer 0 reload data D2			1	R/W	
	D1	RLD01	Timer 0 reload data D1			1	R/W	
	D0	RLD00	Timer 0 reload data D0 (LSB)			1	R/W	

Table 5.10.10.1(b) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF34	D7	RLD17	Timer 1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD16	Timer 1 reload data D6			1	R/W	
	D5	RLD15	Timer 1 reload data D5			1	R/W	
	D4	RLD14	Timer 1 reload data D4			1	R/W	
	D3	RLD13	Timer 1 reload data D3			1	R/W	
	D2	RLD12	Timer 1 reload data D2			1	R/W	
	D1	RLD11	Timer 1 reload data D1			1	R/W	
	D0	RLD10	Timer 1 reload data D0 (LSB)			1	R/W	
00FF35	D7	PTD07	Timer 0 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD06	Timer 0 counter data D6			1	R	
	D5	PTD05	Timer 0 counter data D5			1	R	
	D4	PTD04	Timer 0 counter data D4			1	R	
	D3	PTD03	Timer 0 counter data D3			1	R	
	D2	PTD02	Timer 0 counter data D2			1	R	
	D1	PTD01	Timer 0 counter data D1			1	R	
	D0	PTD00	Timer 0 counter data D0 (LSB)			1	R	
00FF36	D7	PTD17	Timer 1 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD16	Timer 1 counter data D6			1	R	
	D5	PTD15	Timer 1 counter data D5			1	R	
	D4	PTD14	Timer 1 counter data D4			1	R	
	D3	PTD13	Timer 1 counter data D3			1	R	
	D2	PTD12	Timer 1 counter data D2			1	R	
	D1	PTD11	Timer 1 counter data D1			1	R	
	D0	PTD10	Timer 1 counter data D0 (LSB)			1	R	
00FF38	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE162	8/16-bit mode selection (timer 2/3)	16-bit x 1	8-bit x 2	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	CKSEL3	Prescaler 3 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL2	Prescaler 2 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF39	D7	EVCNT2	Timer 2 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL2	Timer 2 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 2 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL2	Timer 2 pulse polarity selection: Down count timing in event counter mode	Rising edge of K11 input	Falling edge of K11 input	0	R/W	
			Timer 2 pulse polarity selection: In pulse width measurement mode	High level measurement for K11 input	Low level measurement for K11 input			
	D4	PSC21	Timer 2 prescaler dividing ratio selection (PSC21 = 1, PSC20 = 1: Source clock / 64)			0	R/W	
	D3	PSC20	Timer 2 prescaler dividing ratio selection (PSC21 = 1, PSC20 = 0: Source clock / 16; PSC21 = 0, PSC20 = 1: Source clock / 4; PSC21 = 0, PSC20 = 0: Source clock / 1)			0	R/W	
	D2	CONT2	Timer 2 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET2	Timer 2 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN2	Timer 2 Run/Stop control	Run	Stop	0	R/W	

Table 5.10.10.1(c) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF3A	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC31	Timer 3 prescaler dividing ratio selection PSC31 PSC30 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D3	PSC30				0	R/W	
	D2	CONT3	Timer 3 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET3	Timer 3 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN3	Timer 3 Run/Stop control	Run	Stop	0	R/W	
00FF3B	D7	RLD27	Timer 2 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD26	Timer 2 reload data D6			1	R/W	
	D5	RLD25	Timer 2 reload data D5			1	R/W	
	D4	RLD24	Timer 2 reload data D4			1	R/W	
	D3	RLD23	Timer 2 reload data D3			1	R/W	
	D2	RLD22	Timer 2 reload data D2			1	R/W	
	D1	RLD21	Timer 2 reload data D1			1	R/W	
	D0	RLD20	Timer 2 reload data D0 (LSB)			1	R/W	
00FF3C	D7	RLD37	Timer 3 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD36	Timer 3 reload data D6			1	R/W	
	D5	RLD35	Timer 3 reload data D5			1	R/W	
	D4	RLD34	Timer 3 reload data D4			1	R/W	
	D3	RLD33	Timer 3 reload data D3			1	R/W	
	D2	RLD32	Timer 3 reload data D2			1	R/W	
	D1	RLD31	Timer 3 reload data D1			1	R/W	
	D0	RLD30	Timer 3 reload data D0 (LSB)			1	R/W	
00FF3D	D7	PTD27	Timer 2 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD26	Timer 2 counter data D6			1	R	
	D5	PTD25	Timer 2 counter data D5			1	R	
	D4	PTD24	Timer 2 counter data D4			1	R	
	D3	PTD23	Timer 2 counter data D3			1	R	
	D2	PTD22	Timer 2 counter data D2			1	R	
	D1	PTD21	Timer 2 counter data D1			1	R	
	D0	PTD20	Timer 2 counter data D0 (LSB)			1	R	
00FF3E	D7	PTD37	Timer 3 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD36	Timer 3 counter data D6			1	R	
	D5	PTD35	Timer 3 counter data D5			1	R	
	D4	PTD34	Timer 3 counter data D4			1	R	
	D3	PTD33	Timer 3 counter data D3			1	R	
	D2	PTD32	Timer 3 counter data D2			1	R	
	D1	PTD31	Timer 3 counter data D1			1	R	
	D0	PTD30	Timer 3 counter data D0 (LSB)			1	R	
00FF21	D7	PREM1	REM carrier interrupt priority register			0	R/W	
	D6	PREM0				0	R/W	
	D5	PPT3	Programmable timer 2–3 interrupt priority register			0	R/W	
	D4	PPT2				0	R/W	
	D3	PPT1	Programmable timer 0–1 interrupt priority register			0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10–K11 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	

PREM1 PREM0 / PPT3 PPT2 / PPT1 PPT0 / PK11 PK10 / Priority level

PREM1 / PPT3 / PPT1 / PK11	PREM0 / PPT2 / PPT0 / PK10	Priority level
1	1	Level 3
1	0	Level 2
0	1	Level 1
0	0	Level 0

Table 5.10.10.1(d) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10–K11 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10–K11 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag			0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	
00FF26	D7	EPT3	Programmable timer 3 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT2	Programmable timer 2 interrupt enable register			0	R/W	
	D5	EREM	REM carrier interrupt enable register			0	R/W	
	D4	REMC	REM carrier generation On/Off	On	Off	1	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF27	D7	FPT3	Programmable timer 3 interrupt factor flag	(R) Generated	(R) Not generated	0	R/W	
	D6	FPT2	Programmable timer 2 interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D5	FREM	REM carrier interrupt factor flag			0	R/W	
	D4	REMSO	Forced REM output On/Off	On	Off	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

MODE160: 00FF30H•D4
MODE162: 00FF38H•D4

Selects the 8 / 16-bit mode.

When "1" is written: 16 bits × 1 channel
When "0" is written: 8 bits × 2 channels
Reading: Valid

MODE160 is used to select whether timers 0 and 1 will be used as 2 channel independent 8-bit timers or as a 1 channel combined 16-bit timer. The 8 / 16-bit mode for timers 2 and 3 is selected with MODE162. When "0" is written to MODE16x, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected.
At initial reset, MODE16x is set to "0" (8-bit × 2 channels).

CKSEL0: 00FF30H•D0
CKSEL1: 00FF30H•D1
CKSEL2: 00FF38H•D0
CKSEL3: 00FF38H•D1

Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

CKSELx is used to select the source clock of prescaler x (for timer x) from OSC1 and OSC3. When "0" is written to CKSELx, OSC1 is selected and when "1" is written, OSC3 is selected.
When event counter mode has been selected, the setting of the CKSEL0 or CKSEL2 becomes invalid. In the same way, setting of the CKSEL1 or CKSEL3 becomes invalid when 16-bit mode has been selected.
At initial reset, this register is set to "0" (OSC1 clock).

PSC00, PSC01: 00FF31H•D3, D4
PSC10, PSC11: 00FF32H•D3, D4
PSC20, PSC21: 00FF39H•D3, D4
PSC30, PSC31: 00FF3AH•D3, D4

Select the dividing ratio of the prescaler.
Two-bit PSCx0 and PSCx1 is the prescaler dividing ratio selection registers for timer x. The prescaler dividing ratios that can be set by these registers are shown in Table 5.10.10.2.

Table 5.10.10.2 Selection of prescaler dividing ratio

PSC31 PSC21 PSC11 PSC01	PSC30 PSC20 PSC10 PSC00	Prescaler dividing ratio
1	1	Source clock / 64
1	0	Source clock / 16
0	1	Source clock / 4
0	0	Source clock / 1

When event counter mode has been selected, the setting of the PSC0 or PSC2 becomes invalid. In the same way, the setting of the PSC1 or PSC3 becomes invalid when 16-bit mode has been selected.
At initial reset, this register is set to "0" (input clock / 1).

EVCNT0: 00FF31H•D7
EVCNT2: 00FF39H•D7

Select the counter mode for the timer 0 and timer 2.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

EVCNTx is used to select whether timer x will be used as an event counter or a timer. When "1" is written to EVCNTx, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, EVCNTx is set to "0" (timer mode).

FCSEL0: 00FF31H•D6
FCSEL2: 00FF39H•D6

Select the function for each counter mode of timer 0 and timer 2.

• In timer mode

When "1" is written: Pulse width measurement timer mode
When "0" is written: Normal mode
Reading: Valid

In the timer mode, select whether timer 0 or timer 2 will be used as a pulse width measurement timer or a normal timer. When "1" is written to FCSELx, timer x is set in the pulse width measurement mode and the counting is done according to the signal level input to the K10 (EVIN0) input port terminal for timer 0 or the K11 (EVIN2) input port terminal for timer 2. When "0" is written to FCSELx, the normal mode is selected and the counting is not affected by the input port terminal.

• In event counter mode

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

In the event counter mode, FCSELx is used to select whether the noise rejecter for the K10 (EVIN0) input port terminal for timer 0 or the K11 (EVIN2) input port terminal for timer 2 is enabled or not. When "1" is written to FCSELx, the noise rejecter is selected and counting is done by an external clock with 0.98 msec or more pulse width. The noise rejecter allows clocking counter at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K10 (K11) input port terminal. Consequently, the pulse width that can reliably be rejected is 0.48 msec.

When "0" is written to FCSELx, the noise rejector is not selected and the counting is done directly by an external clock input to the K10 (K11) input port terminal.
At initial reset, FCSELx is set to "0".

PLPOL0: 00FF31H•D5
PLPOL2: 00FF39H•D5

Select the pulse polarity for the K10 and K11 input port terminals.

• In event counter mode

When "1" is written:	Rising edge
When "0" is written:	Falling edge
Reading:	Valid

In the event counter mode, PLPOLx is used to select whether the falling edge of the external clock, which is input to the K10 (EVIN0) input port terminal for timer 0 or the K11 (EVIN2) input port terminal for timer 2, is counted or the rising edge is counted. When "0" is written to PLPOLx, the falling edge is selected and when "1" is written, the rising edge is selected.

• In pulse width measurement mode

When "1" is written:	High level pulse width measurement
When "0" is written:	LOW level pulse width measurement
Reading:	Valid

In the pulse width measurement mode, PLPOLx is used to select whether the LOW level width of the external signal, which is input to the K10 (EVIN0) input port terminal for timer 0 or the K11 (EVIN2) input port terminal for timer 2, is measured or the HIGH level is measured. When "0" is written to PLPOLx, the LOW level width measurement is selected and when "1" is written, the HIGH level width measurement is selected.
In the normal mode (EVCNTx = FCSELx = "0"), the setting of PLPOLx becomes invalid.
At initial reset, PLPOLx is set to "0".

CONT0: 00FF31H•D2
CONT1: 00FF32H•D2
CONT2: 00FF39H•D2
CONT3: 00FF3AH•D2

Selects the continuous / one-shot mode.

When "1" is written:	Continuous mode
When "0" is written:	One-shot mode
Reading:	Valid

CONTx is used to select whether timer x will be used in the continuous mode or in the one-shot mode.

By writing "1" to CONTx, the programmable timer is set to the continuous mode. In the continuous mode, the initial counter value is automatically loaded when an underflow is generated, and counting is continued. On the other hand, when writing "0" to CONTx, the programmable timer is set to the one-shot mode. The counter loads an initial value and stops when an underflow is generated. At this time, PRUNx is automatically reset to "0".
At initial reset, this register is set to "0" (one-shot mode).

RLD00–RLD07: 00FF33H
RLD10–RLD17: 00FF34H
RLD20–RLD27: 00FF3BH
RLD30–RLD37: 00FF3CH

Sets the initial value for the counter.
The reload data set in RLDx is loaded into the counter of timer x and is counted down with that as the initial value.
Reload data is loaded to the counter under two conditions, when "1" is written to PSETx and when the counter underflow automatically loads.
At initial reset, this register is set to "FFH".

PTD00–PTD07: 00FF35H
PTD10–PTD17: 00FF36H
PTD20–PTD27: 00FF3DH
PTD30–PTD37: 00FF3EH

Timer x data is read from PTDx.
These bits act as a buffer to maintain the counter data during readout, and the data can be read as optional timing. However, in the 16-bit mode, to avoid a read error (data error when a borrow from timer 0 (timer 2) to timer 1 (timer 3) is generated in the middle of reading PTD0 and PTD1 (PTD2 and PTD3)), PTD1 (PTD3) latches the timer 1 (timer 3) counter data according to the reading of PTD0 (PTD2).
The latched status of PTD1 (PTD3) is canceled according to the readout of PTD1 (PTD3) or when 0.73–1.22 msec (depends on the readout timing) has elapsed. Therefore, in 16-bit mode, be sure to read the counter data of PTD0 (PTD2) and PTD1 (PTD3) in order.
Since these bits are exclusively for reading, the write operation is invalid.
At initial reset, these bits are set to "FFH".

PSET0: 00FF31H•D1
PSET1: 00FF32H•D1
PSET2: 00FF39H•D1
PSET3: 00FF3AH•D1

Presets the reload data to the counter.

When "1" is written: Preset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PSETx, the reload data in PLDx is preset to the counter of timer x. When the counter of timer x is preset in the RUN status, it restarts immediately after presetting.
In the case of STOP status, the reload data that has been preset is maintained.
No operation results when "0" is written.
When the 16-bit mode is selected, writing "1" to PSET1 or PSET3 is invalid.
This bit is exclusively for writing, it always becomes "0" during reading.

PRUN0: 00FF31H•D0
PRUN1: 00FF32H•D0
PRUN2: 00FF39H•D0
PRUN3: 00FF3AH•D0

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter of timer x starts down-counting by writing "1" to PRUNx and stops by writing "0".
In the STOP status, the counter data is maintained until it is preset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
When the 16-bit mode is selected, PRUN1 or PRUN3 is fixed at "0".
At initial reset and when an underflow is generated in the one-shot mode, this register is set to "0" (STOP).

CHSEL: 00FF30H•D3

Selects a channel for generating the TOUT signal.

When "1" is written: Timer 1 underflow
When "0" is written: Timer 0 underflow
Reading: Valid

Select whether the timer 0 underflow will be used for the TOUT signal or the timer 1 underflow will be used. When "0" is written to CHSEL, timer 0 is selected and when "1" is written, timer 1 is selected.When the 16-bit mode has been selected, it is fixed to timer 1 (underflow of the 16-bit timer), and setting of CHSEL becomes invalid.
At initial reset, CHSEL is set to "0" (timer 0 underflow).

PTOUT: 00FF30H•D2

Controls the TOUT (programmable timer output clock) signal output.

When "1" is written: TOUT signal output ON
When "0" is written: TOUT signal output OFF
Reading: Valid

PTOUT is the output control register for TOUT ($\overline{\text{TOUT}}$) signal. When "1" is set to the register, the TOUT ($\overline{\text{TOUT}}$) signal is output from the output port terminal R27 (R26). When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D. The data register R26D does not affect the $\overline{\text{TOUT}}$ output.
At initial reset, PTOUT is set to "0" (OFF).
The $\overline{\text{TOUT}}$ signal can be output from R26 only when the function is selected by mask option.

PPT0, PPT1: 00FF21H•D2, D3
PPT2, PPT3: 00FF21H•D4, D5

Set the priority level of the programmable timer interrupt.
PPT0–PPT1 and PPT2–PPT3 are the interrupt priority registers that correspond to the timers 0–1 and timers 2–3 interrupts, respectively. Table 5.10.10.3 shows the interrupt priority level which can be set by this register.

Table 5.10.10.3 Interrupt priority level settings

PPT3 PPT1	PPT2 PPT0	Interrupt priority level
1	1	Level 3 ($\overline{\text{IRQ3}}$)
1	0	Level 2 ($\overline{\text{IRQ2}}$)
0	1	Level 1 ($\overline{\text{IRQ1}}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EPT0: 00FF23H•D6
EPT1: 00FF23H•D7
EPT2: 00FF26H•D6
EPT3: 00FF26H•D7

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

EPTx is the interrupt enable register that corresponds to the interrupt factor for timer x. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
When the 16-bit mode is selected, setting of EPT0 or EPT2 becomes invalid.
At initial reset, this register is set to "0" (interrupt disabled).

FPT0: 00FF25H•D6
FPT1: 00FF25H•D7
FPT2: 00FF27H•D6
FPT3: 00FF27H•D7

Indicates the programmable timer interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FPTx is the interrupt factor flag that corresponds to the interrupt for timer x and are set to "1" in synchronization with the underflow of the counter. When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
When the 16-bit mode is selected, the interrupt factor flag FPT0 or FPT2 is not set to "1" and a timer 0 or timer 2 interrupt cannot be generated. (In the 16-bit mode, the interrupt factor flag FPT1 or FPT3 is set to "1" by an underflow of the 16-bit counter.)
At initial reset, this flag is reset to "0".

5.10.11 Programming notes

(1) The programmable timer is actually made to RUN / STOP in synchronization with the falling edge of the input clock after writing to the PRUNx register. Consequently, when "0" is written to the PRUNx, the timer stops when the counter is decremented "1". The PRUNx maintains "1" for reading until the timer actually stops.
Figure 5.10.11.1 shows the timing chart of the RUN / STOP control.

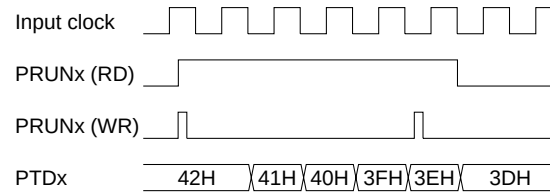


Fig. 5.10.11.1 Timing chart of RUN/STOP control

The event counter mode is excluded from the above note.

(2) The SLP instruction is executed when the programmable timer is in the RUN status (PRUNx = "1"). The programmable timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (PRUNx = "0") prior to executing the SLP instruction.
In the same way, disable the TOUT signal output (PTOUT = "0") to avoid an unstable clock output to the R27 (R26) output port terminal.

(3) Since the TOUT signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register setting, a hazard of a 1 / 2 cycle or less is generated.

(4) When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several 100 µsec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to ON status.

(5) When the 16-bit mode has been selected, be sure to read the counter data in the order of PTD0 and PTD1 (PTD2 and PTD3). Moreover, the time interval between reading PTD0 and PTD1 (PTD2 and PTD3) should be 0.73 msec or less.

(6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

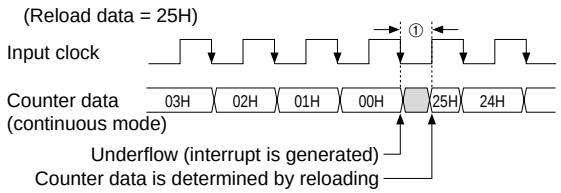


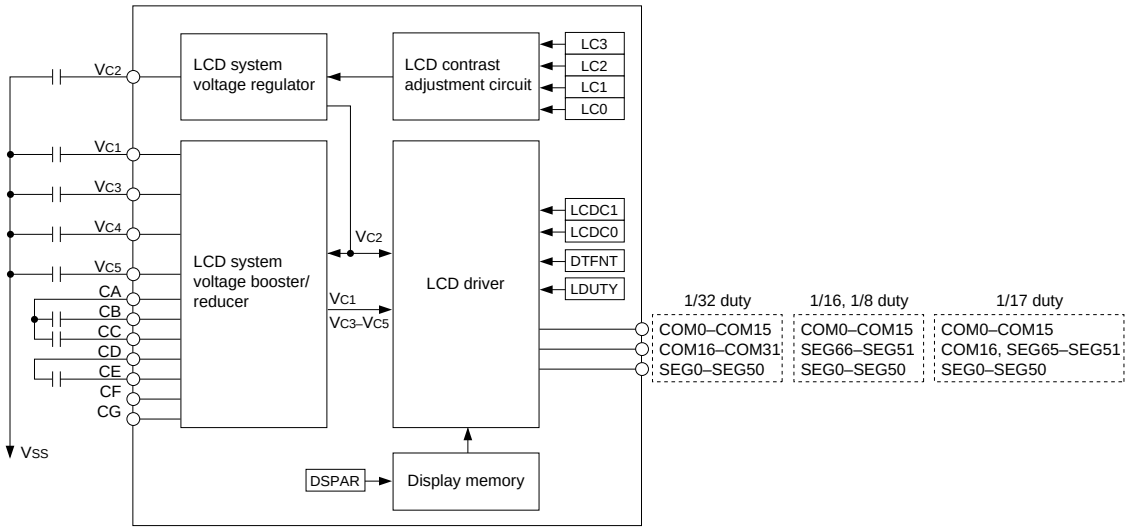
Fig. 5.10.11.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with the OSC3 (high-speed clock).

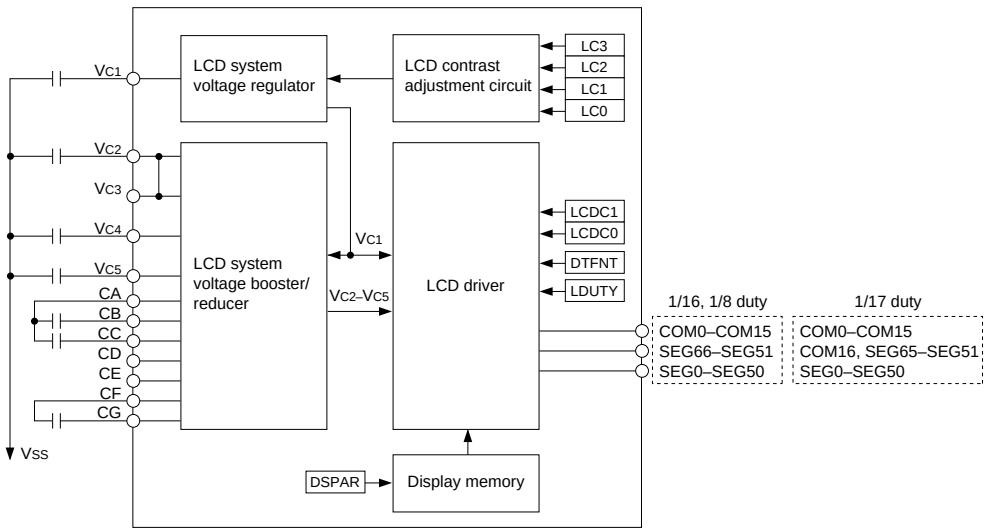
5.11 LCD Controller

5.11.1 Configuration of LCD controller

The S1C88848 has a built-in dot matrix LCD driver that allows driving of an LCD panel with a maximum of 1,632 dots (51 segments × 32 commons). Figure 5.11.1.1 shows the configuration of the LCD controller and the drive power supply.



(a) VC2 standard (1/5 bias mode)



(b) VC1 standard (1/4 bias mode)

Fig. 5.11.1.1 Configuration of LCD controller and drive power supply

5.11.2 Mask option

LCD drive duty
- ☐ 1/32 & 1/16 duty
- ☐ 1/17 duty
- ☐ 1/8 duty

SEG40–SEG50 port specifications

SEG40	☐ DC output	☐ SEG output
SEG41	☐ DC output	☐ SEG output
SEG42	☐ DC output	☐ SEG output
SEG43	☐ DC output	☐ SEG output
SEG44	☐ DC output	☐ SEG output
SEG45	☐ DC output	☐ SEG output
SEG46	☐ DC output	☐ SEG output
SEG47	☐ DC output	☐ SEG output
SEG48	☐ DC output	☐ SEG output
SEG49	☐ DC output	☐ SEG output
SEG50	☐ DC output	☐ SEG output

LCD power supply
- ☐ Internal power supply TYPE A (V_{C2} standard, 1/5 bias, 4.5 V)
- ☐ Internal power supply TYPE B (V_{C2} standard, 1/5 bias, 5.5 V)
- ☐ Internal power supply TYPE D (V_{C1} standard, 1/4 bias, 4.5 V)
- ☐ External power supply

■ LCD drive duty

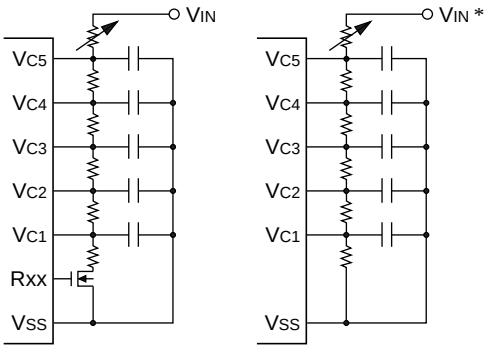
The drive duty for the built-in LCD driver can be selected from software switchable between 1/32 and 1/16, fixed at 1/17 and fixed at 1/8 by mask option.
When "1/32 & 1/16 duty" is selected, the drive duty can be selected by software. When "0" is written to the drive duty selection register LDUTY, 1/32 duty is selected and when "1" is written, 1/16 duty is selected.
When "1/17 duty" or "1/8 duty" is selected, the drive duty is fixed at 1/17 or 1/8, and setting of LDUTY becomes invalid.
When the built-in LCD driver is not used, select the default setting of "1/32 & 1/16 duty".

■ SEG40–SEG50 port specifications

The SEG40 to SEG50 ports can be configured as LCD segment output ports or general-purpose output ports. Refer to Section 5.5, "Output Ports (R ports)", for details of the DC output.

■ LCD power supply

Either the internal power supply (built-in LCD system voltage regulator and voltage booster/reducer) or an external power supply can be selected by mask option to generate the LCD system drive voltages V_{C1}–V_{C5}.
Furthermore, the internal power supply can be selected from among three types, TYPE A, TYPE B and TYPE D, according to the LCD panel characteristics.
The internal power supply is designed for a small scale LCD panel and is not suitable for driving a panel that has large size pixels or for driving a large capacity panel using an external expanded LCD driver. In this case, select external power supply and input the regulated voltage from outside the IC.
Note that the LCD must be driven with 1/5 bias when external power supply is selected.
Figure 5.11.2.1 shows the circuit examples when using an external power supply.



* V_{SS} level or high impedance when LCD is not driven.

Fig. 5.11.2.1 Circuit examples when using an external power supply

5.11.3 LCD driver

The maximum number of dots changes according to the drive duty selection.
When 1/32 duty is selected, the combined common/segment output terminal is switched to the common terminal. An LCD panel with 51 segments × 32 commons (maximum 1,632 dots) can be driven.
When 1/17 duty is selected, COM16 in the combined common/segment output terminals is switched to the common terminal and other terminals are configured as segment terminals. An LCD panel with 66 segments × 17 commons (maximum 1,122 dots) can be driven.
When 1/16 duty is selected, the combined common/segment output terminal is switched to the segment terminal. An LCD panel with 67 segments × 16 commons (maximum 1,072 dots) can be driven.
When 1/8 duty is selected, the combined common/segment output terminal is switched to the segment terminal as when 1/16 duty is selected. An LCD panel with 67 segments × 8 commons (maximum 536 dots) can be driven. Furthermore, when 1/8 duty is selected, terminals COM8–COM15 become invalid, in that they always output an OFF signal.
Table 5.11.3.1 shows the correspondence between the drive duty and the maximum number of displaying dots.

Figures 5.11.3.1 to 5.11.3.4 show the 1/5 bias drive waveforms.
When driving with 1/4 bias, the V_{C2} voltage level is the same as V_{C3}.

Table 5.11.3.1 Correspondence between drive duty and maximum number of displaying dots

Mask option	LDUTY	Duty	Common terminal	Segment terminal	Maximum number of display dots
1/32 & 1/16 duty	0	1/32	COM0–COM31	SEG0–SEG50	1,632 dots
	1	1/16	COM0–COM15	SEG0–SEG66	1,072 dots
1/17 duty	×	1/17	COM0–COM16	SEG0–SEG65	1,122 dots
1/8 duty	×	1/8	COM0–COM7	SEG0–SEG66	536 dots

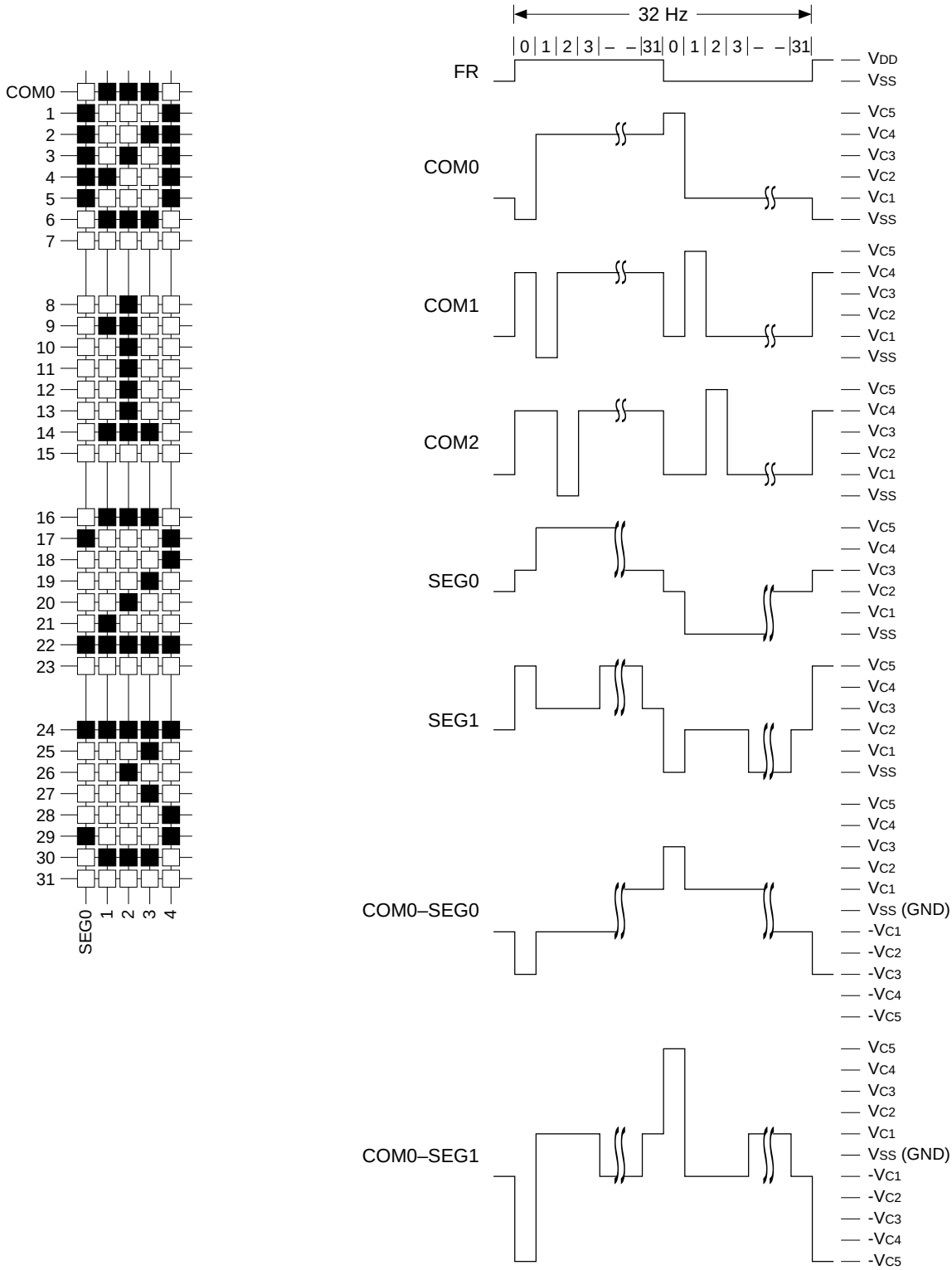


Fig. 5.11.3.1 Drive waveform for 1/32 duty

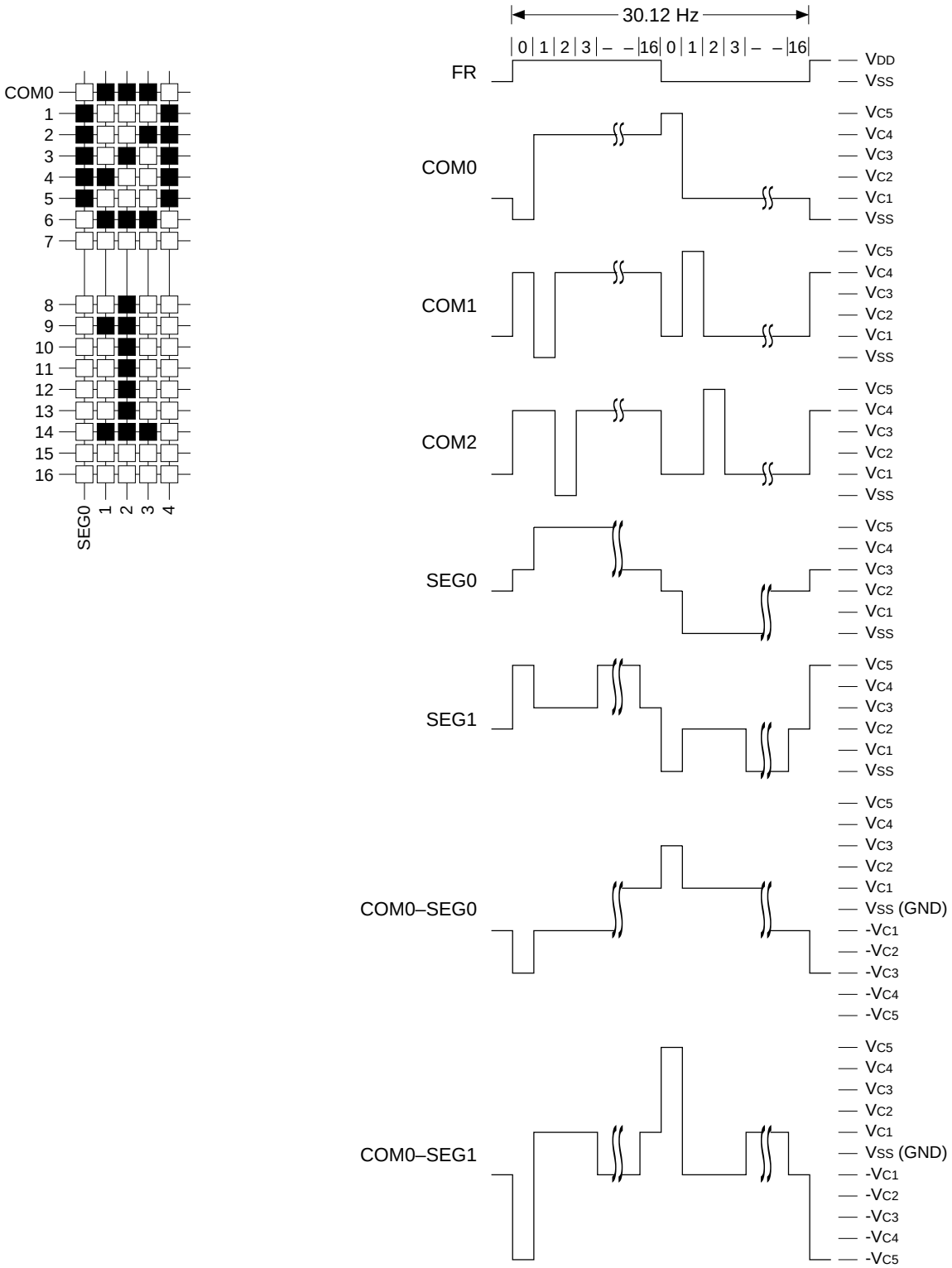


Fig. 5.11.3.2 Drive waveform for 1/17 duty

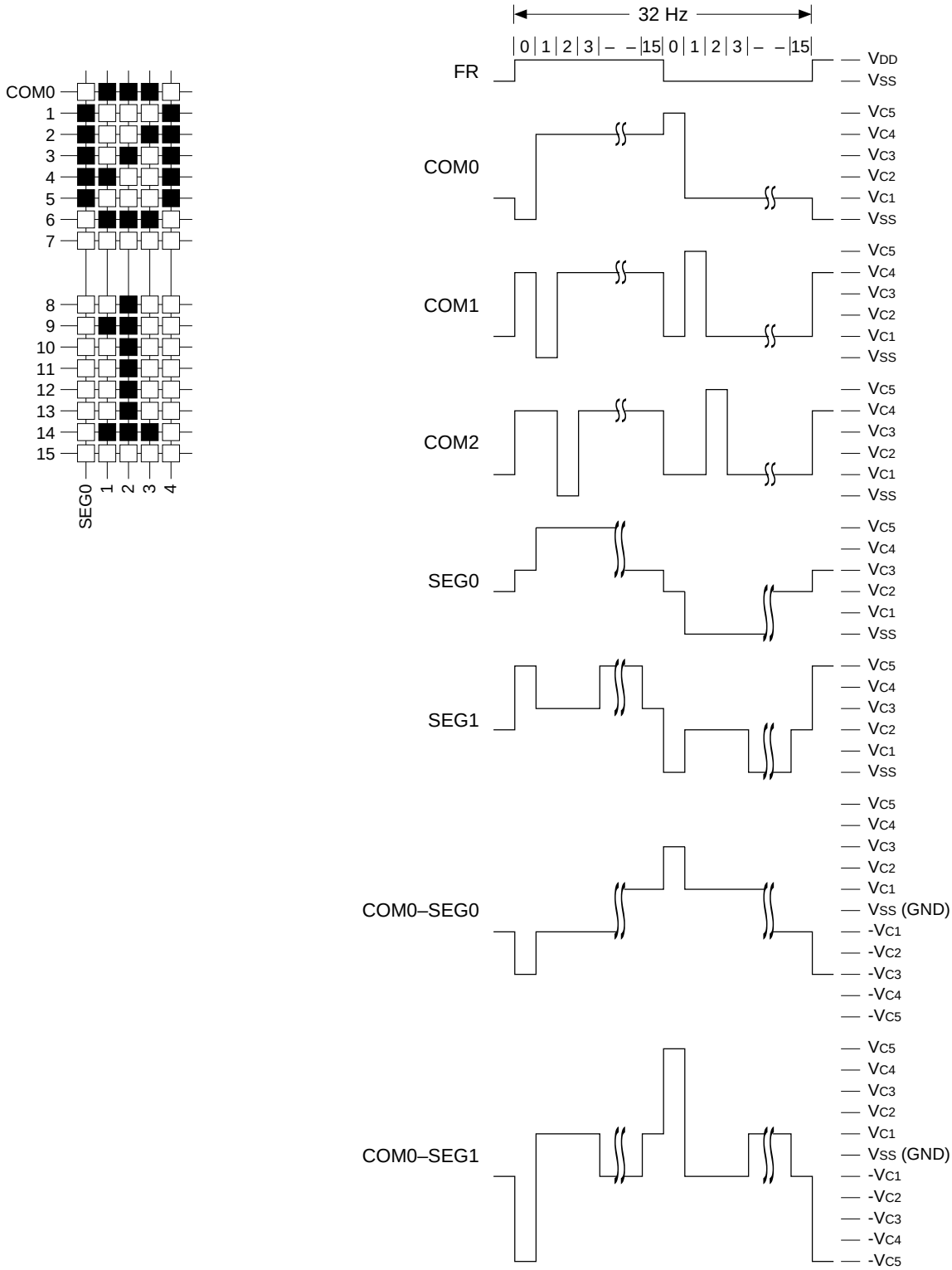


Fig. 5.11.3.3 Drive waveform for 1/16 duty

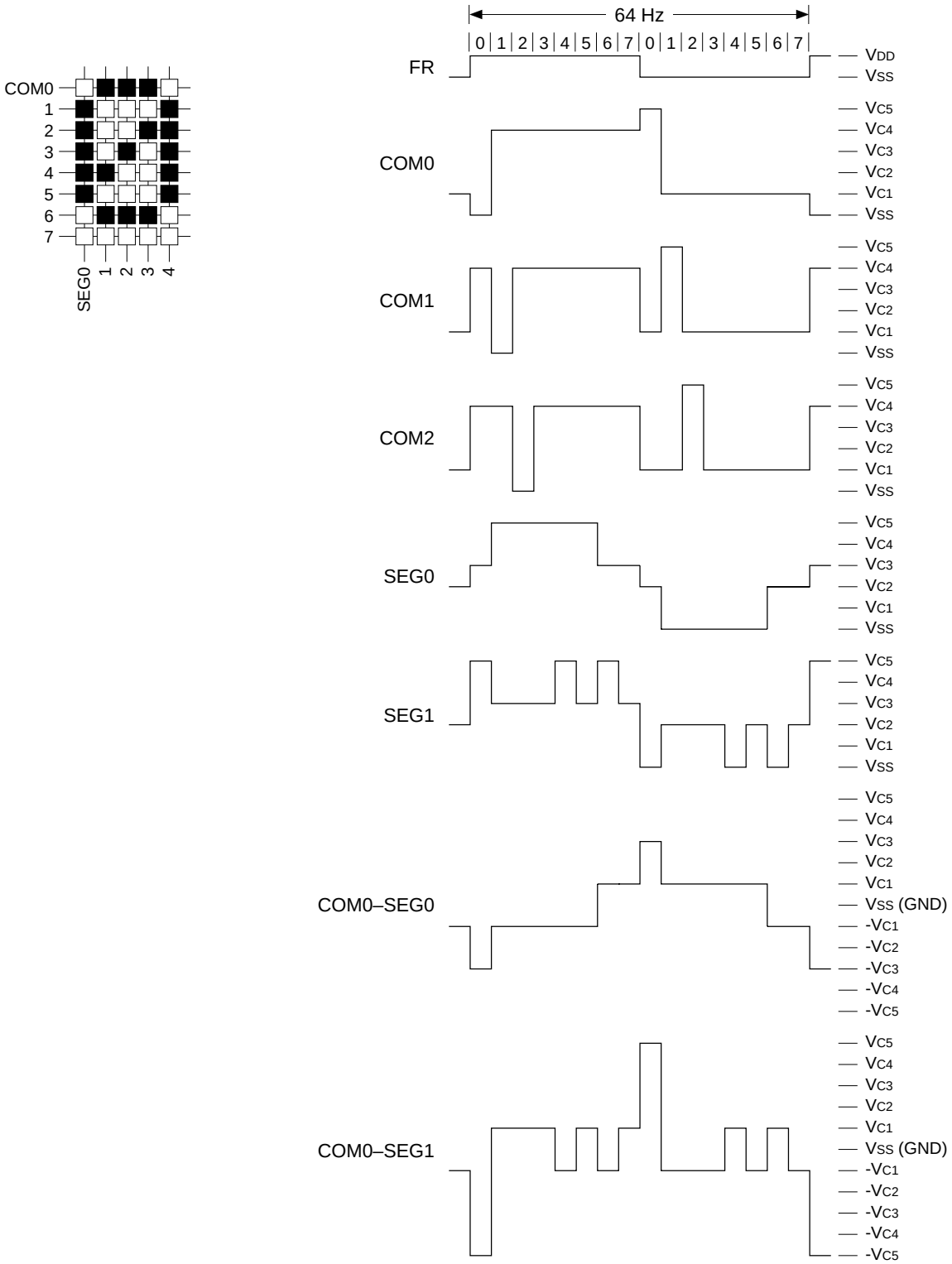


Fig. 5.11.3.4 Drive waveform for 1/8 duty

5.11.4 Display control

The display status of the built-in LCD driver and the contrast adjustment can be controlled with the built-in LCD controller. The LCD display status can be selected by display control registers LCDC0 and LCDC1. Setting the value and display status are shown in Table 5.11.4.1.

Table 5.11.4.1 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

All the dots in the LCD display can be turned on or off directly by the drive waveform output from the LCD driver, and data in the display memory is not changed. Also, since the common terminal at this time is set to static drive when all the dots are on and is set to dynamic drive when they are off, this function can be used as follows:

(1) Since all dots on is binary output (V_{C5} and V_{SS}) with static drive, the common / segment terminal can be used as a monitor terminal for the OSC1 oscillation frequency adjustment. However, COM16 cannot be set in static drive when 1 / 17 duty is selected.

(2) Since all dots off is dynamic drive, you can brink the entire LCD display without changing display memory data.

Selecting LCD drive OFF turns the LCD drive power circuit OFF and all the V_{C1}–V_{C5} terminals go to V_{SS} level. However, if external power supply has been selected by the mask option, the V_{C1}–V_{C5} shift to floating status when drive is turned OFF. Furthermore, when the SLP instruction is executed, registers LCDC0 and LCDC1 are automatically reset to "0" (set to drive off) by hardware.

The LCD contrast can be adjusted in 16 stages. This adjustment is done by the contrast adjustment register LC0–LC3, and the setting values correspond to the contrast as shown in Table 5.11.4.2. However, if external power supply has been selected by the mask option, the contrast adjustment register LC0–LC3 is ineffective and contrast adjustment cannot be done. When LCx is set to a value from A to F in TYPE B, the same contrast results without changing the set value.

Table 5.11.4.2 LCD contrast adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
:	:	:	:	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

Note: Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

5.11.5 Display memory

The S1C88848 has a built-in 402-byte display memory. The display memory is allocated to address F800H–FD42H (including unavailable areas) and the correspondence between the memory bits and common / segment terminal is changed according to the selection status of the following items.

(1) Drive duty (1/32, 1/17, 1/16 or 1/8 duty)
(2) Dot font (5 × 8 or 5 × 5 dots)

When 1 / 17, 1 / 16 or 1 / 8 duty is selected for drive duty, two-screen memory can be secured, and the two screens can be switched by the display memory area selection register DSPAR. When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.
Furthermore, memory allocation for 5 × 8 dots and 5 × 5 dots can be selected in order to easily display 5 × 5-dot font characters on the LCD panel.
This selection can be done by the dot font selection register DTFNT: when "0" is written to DTFNT, 5 × 8 dots is selected and when "1" is written, 5 × 5 dots is selected.
The correspondence between the display memory bits set according to the drive duty and font size, and the common / segment terminals are shown in Figures 5.11.5.1–5.11.5.8.
When "1" is written to the display memory bit corresponding to the dot on the LCD panel, the dot goes ON and when "0" is written, it goes OFF. Since display memory is designed to permit reading / writing, it can be controlled in bit units by logical operation instructions and other means (read, modify and write instructions).
The display memory bits that have not been assigned can be used as general purpose RAM with read / write capabilities. Even when external memory has expanded into the display memory area, this area is not released to external memory. Access to this area is always via display memory.

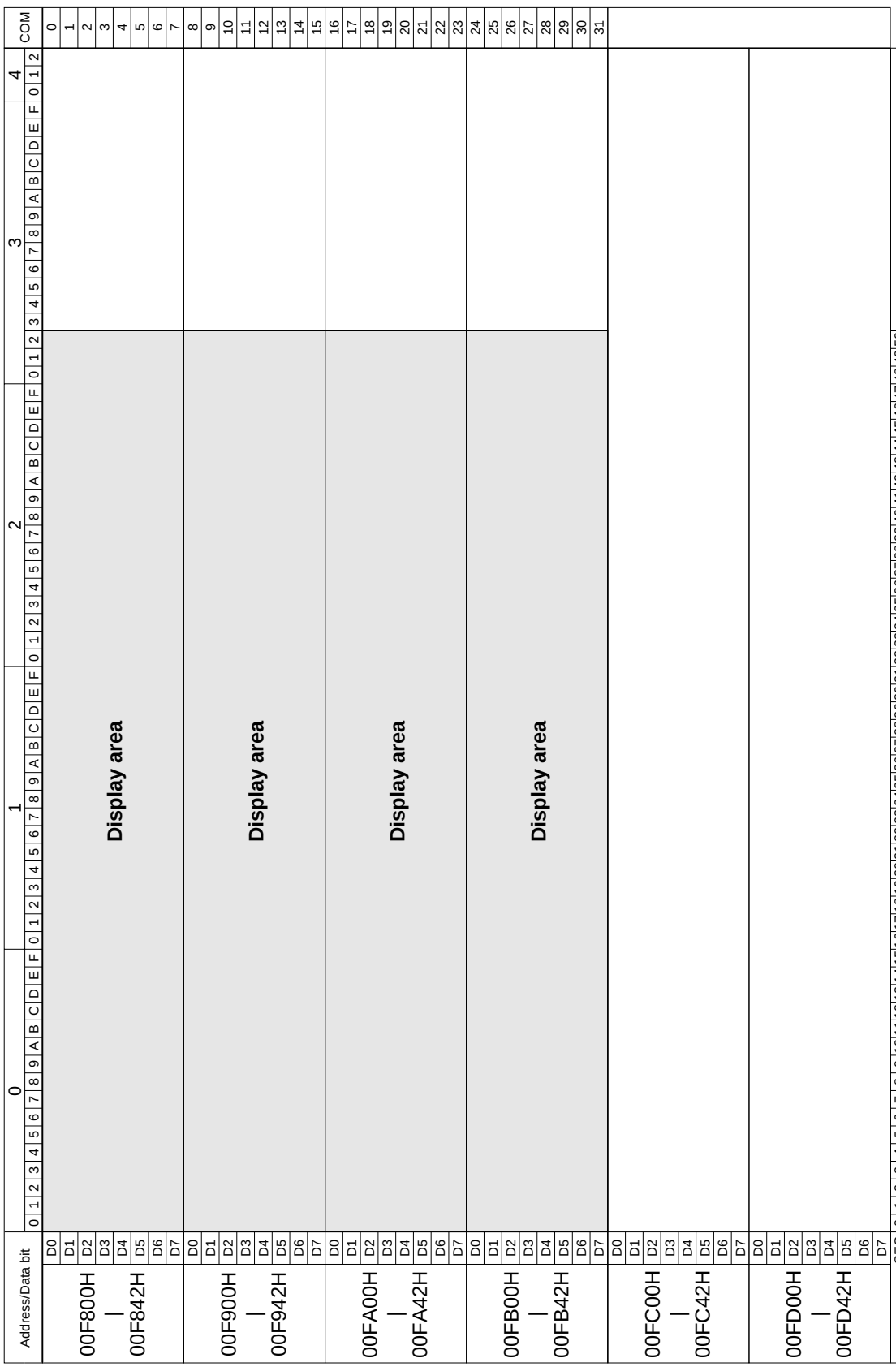


Fig. 5.11.5.1 1/32 duty and 5 × 8 dots display memory map

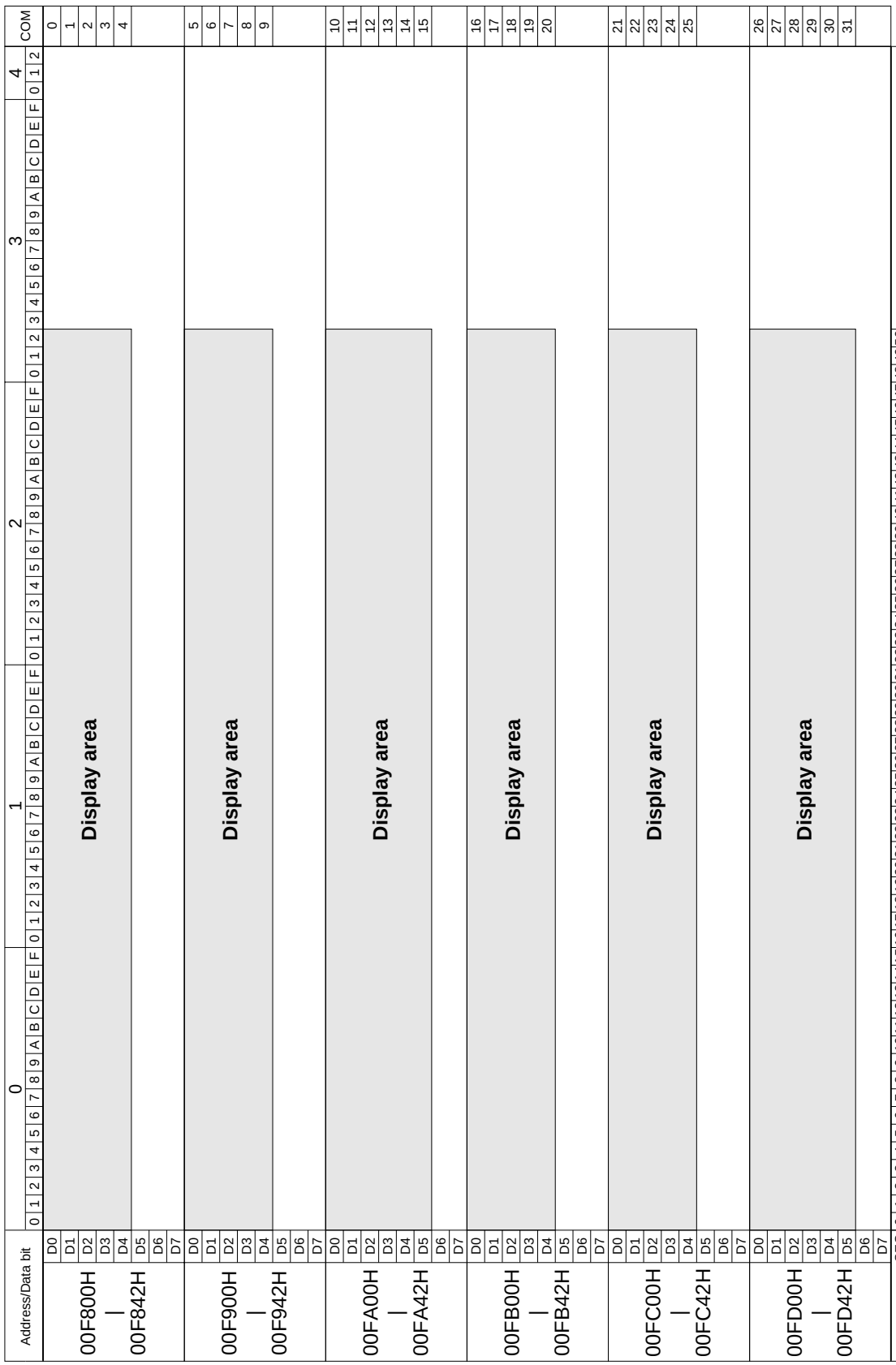


Fig. 5.11.5.2 1/32 duty and 5 ×5 dots display memory map

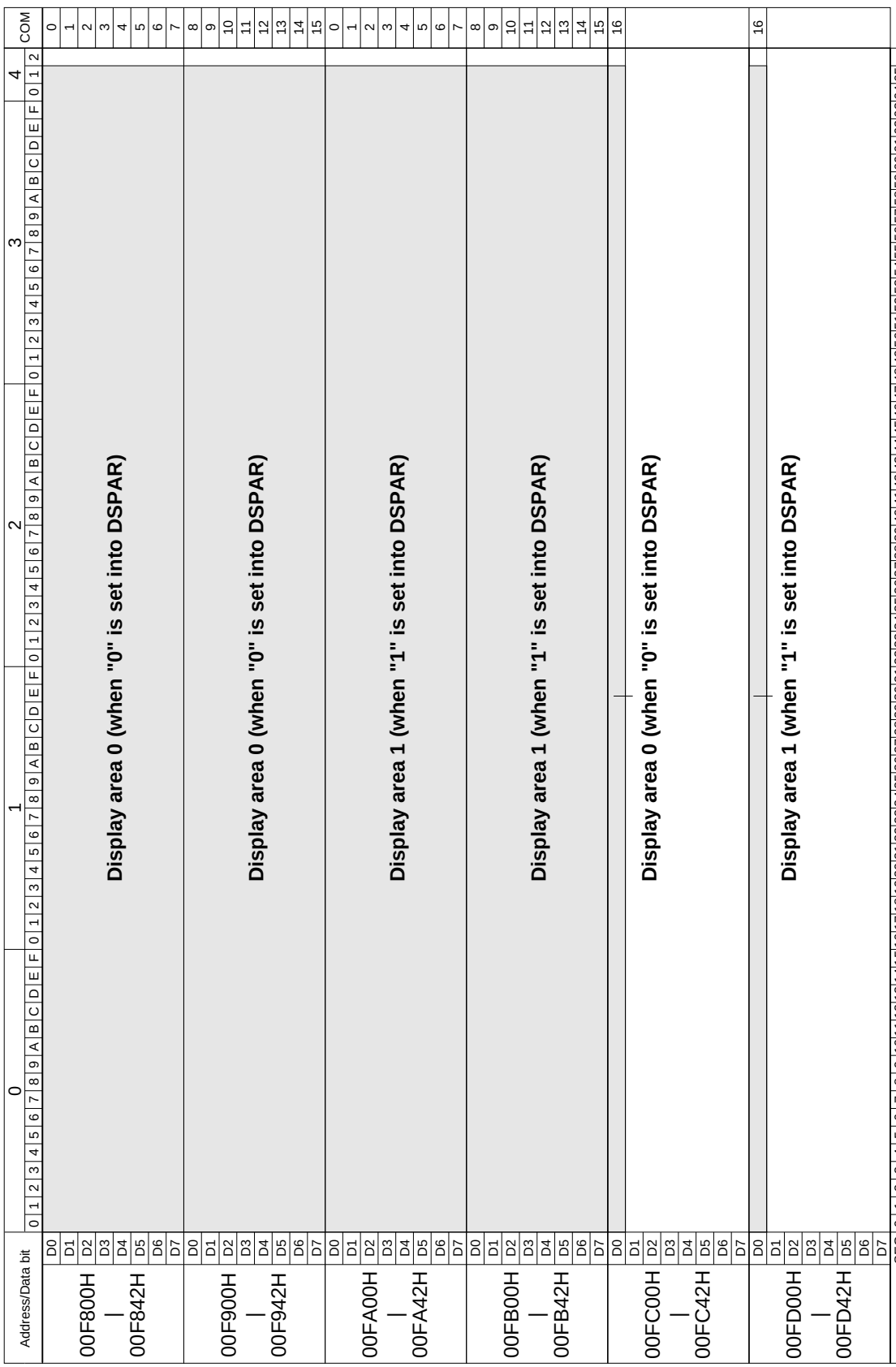


Fig. 5.11.5.3 1/17 duty and 5 × 8 dots display memory map

Address/Data bit		0								1								2								3								4		COM
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	
00F800H — 00F842H	D0	Display area 0 (when "0" is set into DSPAR)																																		0
	D1																																			1
	D2																																			2
	D3																																			3
	D4																																			4
	D5																																			
	D6																																			
	D7																																			
00F900H — 00F942H	D0	Display area 0 (when "0" is set into DSPAR)																																		5
	D1																																			6
	D2																																			7
	D3																																			8
	D4																																			9
	D5																																			
	D6																																			
	D7																																			
00FA00H — 00FA42H	D0	Display area 0 (when "0" is set into DSPAR)																																		10
	D1																																			11
	D2																																			12
	D3																																			13
	D4																																			14
	D5																																			15
	D6																																			16
	D7																																			
00FB00H — 00FB42H	D0	Display area 1 (when "1" is set into DSPAR)																																		0
	D1																																			1
	D2																																			2
	D3																																			3
	D4																																			4
	D5																																			
	D6																																			
	D7																																			
00FC00H — 00FC42H	D0	Display area 1 (when "1" is set into DSPAR)																																		5
	D1																																			6
	D2																																			7
	D3																																			8
	D4																																			9
	D5																																			
	D6																																			
	D7																																			
00FD00H — 00FD42H	D0	Display area 1 (when "1" is set into DSPAR)																																		10
	D1																																			11
	D2																																			12
	D3																																			13
	D4																																			14
	D5																																			15
	D6																																			16
	D7																																			
	SEG	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	

Fig. 5.11.5.4 1/17 duty and 5 ×5 dots display memory map

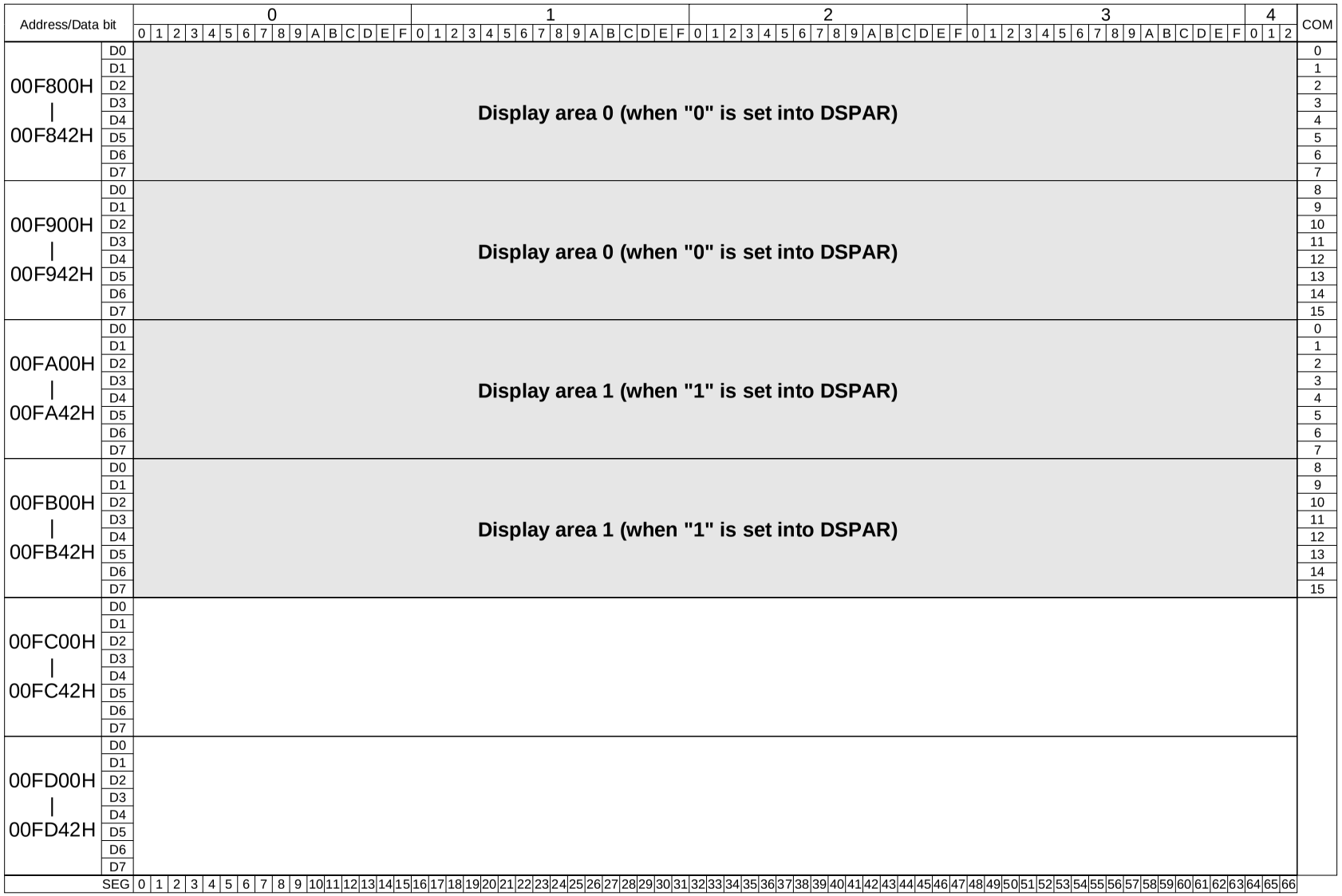


Fig. 5.11.5.5 1/16 duty and 5 × 8 dots display memory map

Fig. 5.11.5.6 1/16 duty and 5 × 5 dots display memory map

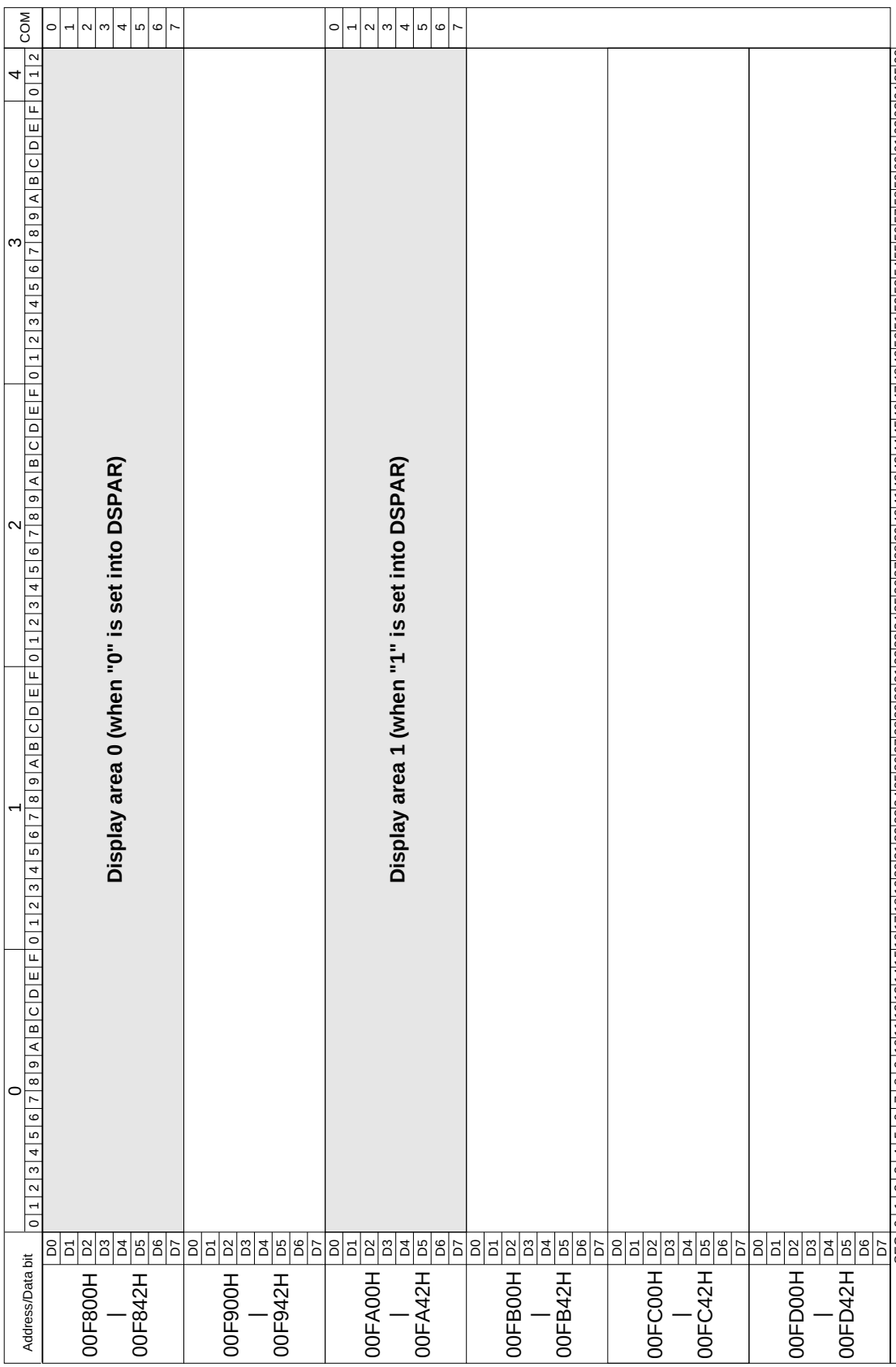


Fig. 5.11.5.7 1/8 duty and 5 × 8 dots display memory map

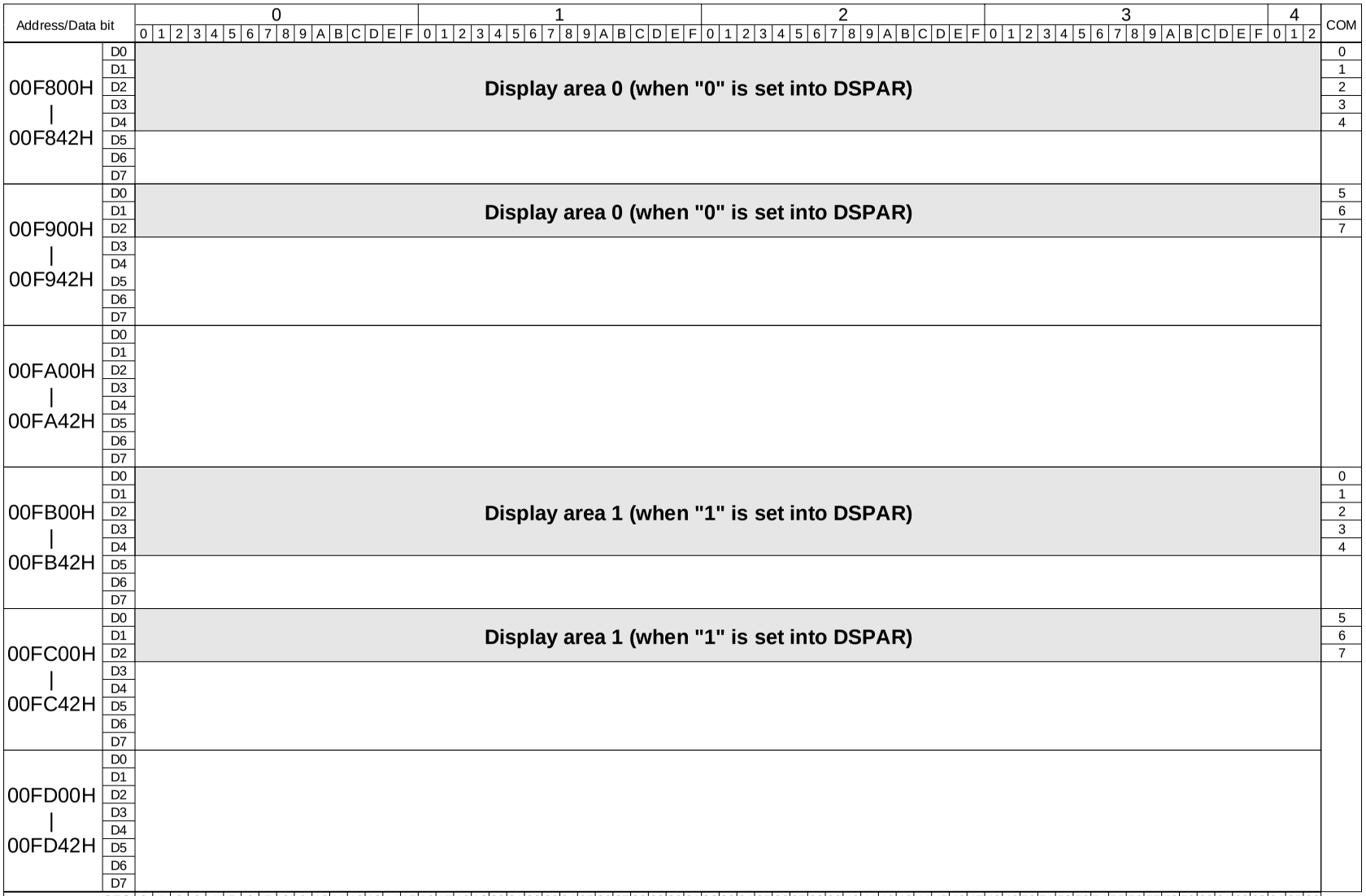


Fig. 5.11.5.8 1/8 duty and 5 × 5 dots display memory map

5.11.6 Control of LCD controller

Table 5.11.6.1 shows the LCD controller control bits.

Table 5.11.6.1 LCD controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF10	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	LCCLK	General-purpose register	1	0	0	R/W	Reserved register
	D3	LCFRM	General-purpose register			0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	General-purpose register	1	0	0	R/W	Reserved register
00FF11	D7	–	–	–	–	–		"0" when being read
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	

*1 When 1/8 or 1/17 duty has been selected by mask option, setting of this register becomes invalid.

LDUTY: 00FF10H•D1

Selects the drive duty.

When "1" is written: 1/16 duty
When "0" is written: 1/32 duty
Reading: Valid

When "1/32 & 1/16 duty" is selected by mask option, select whether the drive duty will be 1/32 or 1/16.
When "0" is written to LDUTY, 1/32 duty is selected and the combined common/segment output terminal is switched to the common terminal.
When "1" is written to LDUTY, 1/16 duty is selected and the combined common/segment output terminal is switched to the segment terminal.
When "1/17 duty" or "1/8 duty" is selected by mask option, the setting of LDUTY becomes invalid.
The correspondence between the display memory bits set according to the drive duty, and the common/segment terminals are shown in Figures 5.11.5.1–5.11.5.8.
At initial reset, LDUTY is set to "0" (1/32 duty).

DTFNT: 00FF10H•D2

Selects the dot font.

When "1" is written: 5×5 dots
When "0" is written: 5×8 dots
Reading: Valid

Select 5×8 dots or 5×5 dots type for the display memory area.
When "0" is written to DTFNT, 5×8 dots is selected and when "1" is written, 5×5 dots is selected.
The correspondence between the display memory bits set according to the dot font, and the common/segment terminals are shown in Figures 5.11.5.1–5.11.5.8.
At initial reset, DTFNT is set to "0" (5×8 dots).

DSPAR: 00FF11H•D6

Selects the display area.

When "1" is written: Display area 1
When "0" is written: Display area 0
Reading: Valid

Selects which display area is secured for two screens in the display memory, will be displayed when 1/17, 1/16 or 1/8 duty is selected.
When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.

When 1/32 duty is selected, since the display area is only for one screen, the setting of DSPAR becomes invalid.
The correspondence between the display memory bits set according to the display area, and the common/segment terminals are shown in Figures 5.11.5.1–5.11.5.8.
At initial reset, DSPAR is set to "0" (display area 0).

LCDC0, LCDC1: 00FF11H•D4, D5

Controls the LCD display.

Table 5.11.6.2 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

The four settings mentioned above can be made without changing the display memory data.
At initial reset and in the SLEEP status, this register is set to "0" (drive off).

LC0–LC3: 00FF11H•D0–D3

Adjusts the LCD contrast.

Table 5.11.6.3 LCD contract adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

The contrast can be adjusted in 16 stages as mentioned above. This adjustment changes the drive voltage on terminals V_{C1}–V_{C5}.
At initial reset, this register is set to "0".

Notes:
- *If external power supply has been selected by the mask option, the contrast adjustment register LC0–LC3 is ineffective.*
- *Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.*

5.11.7 Programming note

When the SLP instruction is executed, display control registers LCDC0 and LCDC1 are automatically reset to "0" by hardware.

5.12 Sound Generator

5.12.1 Configuration of sound generator

The S1C88848 has a built-in sound generator for generating the buzzer (BZ and $\overline{BZ}$) signal.
The BZ signal generated from the sound generator can be output from the R50 output port terminal. Furthermore, the R51 terminal can be set as the $\overline{BZ}$ signal (BZ inverted signal) output by mask option.
Aside permitting the respective setting of the buzzer signal frequency and sound level (duty adjustment) to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 5.12.1.1 shows the configuration of the sound generator.

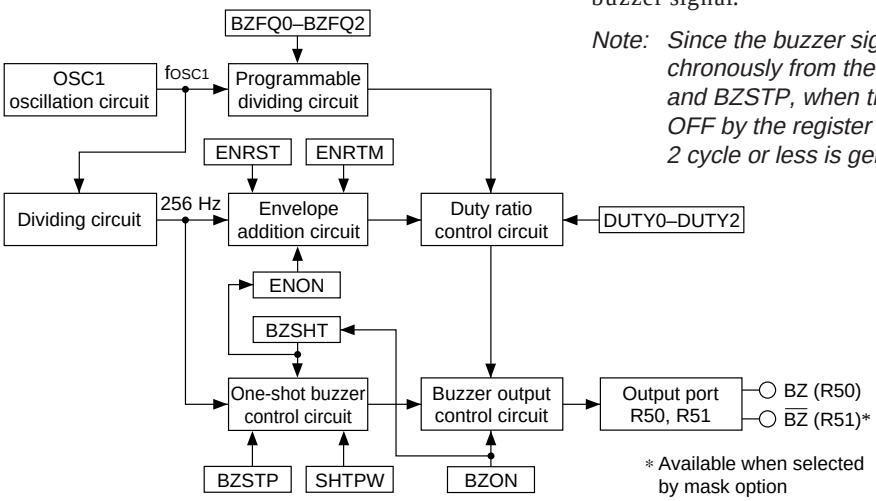


Fig. 5.12.1.1 Configuration of sound generator

5.12.2 Control of buzzer output

The BZ signal can be output from the R50 output port terminal. Furthermore, the R51 output port terminal can be used to output the $\overline{BZ}$ signal (BZ inverted signal) by mask option.
The configuration of the output ports R50 and R51 is shown in Figure 5.12.2.1.

The output control for the buzzer signal generated by the sound generator is done by the buzzer output control register BZON, one-shot buzzer trigger bit BZSHT and one-shot buzzer forced stop bit BZSTP. When "1" is set to BZON or BZSTP, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the buzzer signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
Figure 5.12.2.2 shows the output waveform of the buzzer signal.

Note: Since the buzzer signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.

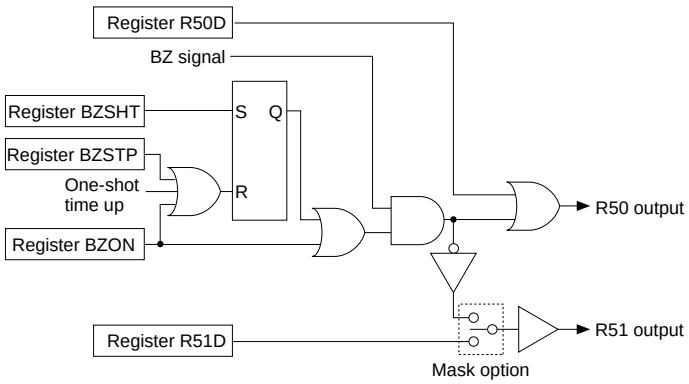


Fig. 5.12.2.1 Configuration of R50 and R51

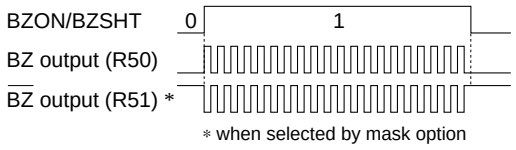


Fig. 5.12.2.2 Buzzer output waveform

5.12.3 Setting of buzzer frequency and sound level

The buzzer signal is divided signal using the OSC1 oscillation circuit (32.768 kHz) as the clock source and 8 frequencies can be selected. This selection is done by the buzzer frequency selection register BZFQ0–BZFQ2. The setting value and buzzer frequency correspondence is shown in Table 5.12.3.1.

By selecting the duty ratio of the buzzer signal from among 8 types, the buzzer sound level can be adjusted. This selection is made in the duty ratio selection register DUTY0–DUTY2. The setting value and duty ratio correspondence is shown in Table 5.12.3.2.

Table 5.12.3.1 Buzzer signal frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Table 5.12.3.2 Duty ratio settings

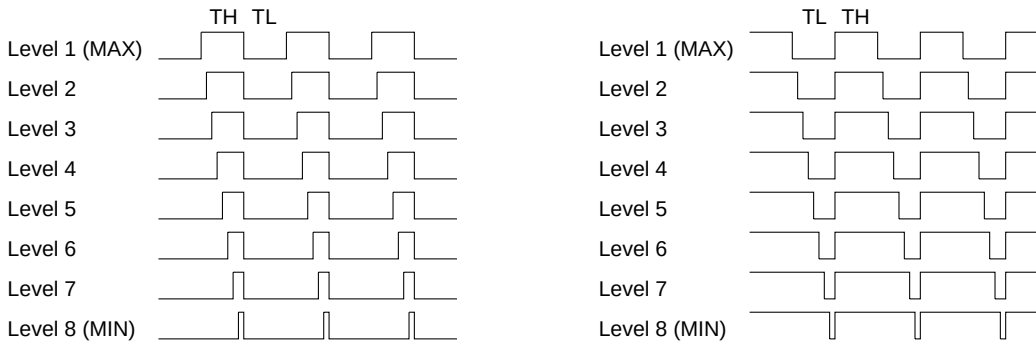
Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

Duty ratio refers to the ratio of pulse width to the pulse cycle; given that HIGH level output time is TH, and low level output time is TL the BZ signal duty ratio becomes TH / (TH+TL) and the $\overline{BZ}$ signal duty ratio becomes TL / (TH+TL).
When DUTY0–DUTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum.

Conversely, when DUTY0–DUTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.

Note that the duty ratio setting differ depending on frequency. See Table 5.12.3.2.

Note: When using the digital envelope, the DUTY0–DUTY2 setting becomes invalid.



(a) BZ signal *(b) $\overline{BZ}$ signal*

Fig. 5.12.3.1 Duty ratio of buzzer signal waveform

5.12.4 Digital envelope

A digital envelope with duty control can be added to the buzzer signal.
The envelope can be realized by staged changing of the same duty ratio as detailed in Table 5.12.3.2 in the preceding section from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" to the envelope control register ENON. When "0" is written, the duty ratio is set at the level selected in DUTY0–DUTY2.

By writing "1" to ENON to turn the buzzer output ON (writing "1" to BZON), the buzzer signal with a level 1 duty ratio is output, and then the duty ratio can be attenuated in stages to level 8. The attenuated envelope can be returned to level 1 by writing "1" to the envelope reset bit ENRST. When attenuated to level 8, the duty level remains at level 8 until the buzzer output is turned OFF (writing "0" to BZON) or writing "1" to ENRST.
The stage changing time for the envelope level can be selected either 125 msec or 62.5 msec by the envelope attenuation time selection register ENRTM.
Figure 5.12.4.1 shows the timing chart of the digital envelope.

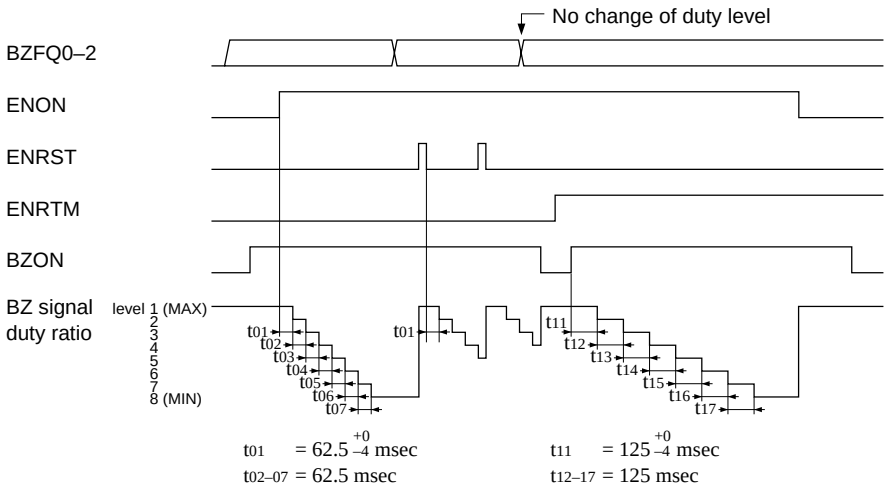


Fig. 5.12.4.1 Timing chart of digital envelope

5.12.5 One-shot output

The sound generator has a built-in one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by the one-shot buzzer duration selection register SHTPW for buzzer signal output time.
The output control of the one-shot buzzer is done by writing "1" to the one-shot buzzer trigger BZSHT, then the buzzer signal is output in synchronization with the internal 256 Hz signal from the output port terminal. Thereafter, when the set time has elapsed, the buzzer signal in synchronization with the 256 Hz signal automatically goes OFF in the same manner.
The BZSHT can be read to determine status. When BZSHT is "1", it indicates a BUSY status (during one-shot output) and when BZSHT is "0", it indicates a READY status (during stop).
When you want to turn the buzzer signal OFF prior to the elapse of the set time, the buzzer signal can be immediately stopped (goes OFF in asynchonization with 256 Hz signal) by writing "1" to the one-shot forced stop bit BZSTP.

Since the one-shot output has a short duration, an envelope cannot be added. (When "1" is written to BZSHT, ENON is automatically reset to "0".) Consequently, only the frequency and sound level can be set for one-shot output.

The control for the one-shot output is invalid during normal buzzer output.

Figure 5.12.5.1 shows the timing chart of the one-shot output.

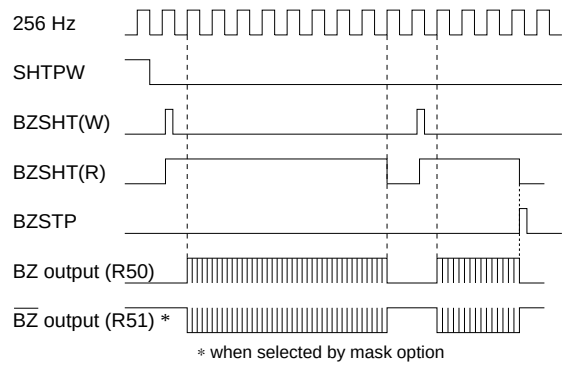


Fig. 5.12.5.1 Timing chart of one-shot output

5.12.6 Control of sound generator

Table 5.12.6.1 shows the sound generator control bits.

Table 5.12.6.1 Sound generator control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF44	D7	–	–		–	–	–		Constantly "0" when
	D6	BZSTP	One-shot buzzer forcibly stop		Forcibly stop	No operation	–	W	being read
	D5	BZSHT	One-shot buzzer trigger/status	R	Busy	Ready	0	R/W	
				W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection		125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time		1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset		Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control		On	Off	0	R/W	*1
	D0	BZON	Buzzer output control		On	Off	0	R/W	
00FF45	D7	–	–		–	–	–		"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection				0	R/W	
	D5	DUTY1					0	R/W	
	D4	DUTY0					0	R/W	
	D3	–	–		–	–	–		"0" when being read
	D2	BZFQ2	Buzzer frequency selection				0	R/W	
	D1	BZFQ1					0	R/W	
	D0	BZFQ0					0	R/W	

DUTY2–0 / Buzzer frequency (Hz)

2	1	0	4096.0 / 2048.0	3276.8 / 1638.4	2730.7 / 1365.3	2340.6 / 1170.3
0	0	0	8/16	8/20	12/24	12/28
0	0	1	7/16	7/20	11/24	11/28
0	1	0	6/16	6/20	10/24	10/28
0	1	1	5/16	5/20	9/24	9/28
1	0	0	4/16	4/20	8/24	8/28
1	0	1	3/16	3/20	7/24	7/28
1	1	0	2/16	2/20	6/24	6/28
1	1	1	1/16	1/20	5/24	5/28

BZFQ2 / BZFQ1 / BZFQ0 / Frequency (Hz)

BZFQ2	BZFQ1	BZFQ0	Frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

*1 Reset to "0" during one-shot output.

BZON: 00FF44H•D0

Controls the buzzer (BZ and $\overline{BZ}$) signal output.

When "1" is written: Buzzer signal output ON
When "0" is written: Buzzer signal output OFF
Reading: Valid

BZON is the output control register for buzzer signal. When "1" is set to the register, the BZ ($\overline{BZ}$) signal is output from the output port terminal R50 (R51). When "0" is set, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
At initial reset, BZON is set to "0" (output OFF).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZFQ0–BZFQ2: 00FF45H•D0–D2

Selects the buzzer signal frequency.

Table 5.12.6.2 Buzzer frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer frequency can be selected from among the above 8 types that have divided the OSC1 clock. At initial reset, this register is set at "0" (4096.0 Hz).

DUTY0–DUTY2: 00FF45H•D4–D6

Selects the duty ratio of the buzzer signal.

Table 5.12.6.3 Duty ratio settings

Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

The buzzer sound level can be adjusted by selecting the duty ratio from among the above 8 types. However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.
At initial reset, this register is set to "0" (level 1).

ENRST: 00FF44H•D2

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

The envelope is reset by writing "1" to ENRST and the duty ratio returns to level 1 (maximum). Writing "0" to ENRST and writing "1" when an envelope has not been added become invalid. Since ENRST is exclusively for writing, it always becomes "0" during reading.

ENON: 00FF44H•D1

Controls the addition of an envelope to the buzzer signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to ENON, an envelope can be added to buzzer signal output. When "0" is written, an envelope is not added and the buzzer signal is fixed at the duty ratio selected in DUTY0–DUTY2.
At initial reset and when "1" is written to BZSHT, ENON is set to "0" (OFF).

ENRTM: 00FF44H•D3

Selects the envelope attenuation time that is added to the buzzer signal.

When "1" is written: 1.0 sec
(125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec
(62.5 msec × 7 = 437.5 msec)
Reading: Valid

The attenuation time of the digital envelope is determined by the time for changing the duty ratio. The duty ratio is changed in 125 msec (8 Hz) units when "1" is written to ENRTM and in 62.5 msec (16 Hz) units, when "0" is written.
This setting becomes invalid when an envelope has been set to OFF (ENON = "0").
At initial reset, ENRTM is set to "0" (0.5 sec).

SHTPW: 00FF44H•D4

Selects the output duration width of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

The one-shot buzzer output duration width is set to 125 msec when "1" is written to SHTPW and 62.5 msec, when "0" is written.
At initial reset, SHTPW is set to "0" (31.25 msec).

BZSHT: 00FF44H•D5

Controls the one-shot buzzer output.

When "1" is written: Trigger
When "0" is written: No operation

When "1" is read: Busy
When "0" is read: Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate. The BZ ($\overline{BZ}$) signal is output from the R50 (R51) terminal. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed.
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") state. The trigger is invalid during ON (BZON = "1") state.
When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON, "1" is read from BZSHTand when the output is OFF, "0" is read.
At initial reset, BZSHT is set to "0" (ready).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZSTP: 00FF44H•D6

Forcibly stops the one-shot buzzer output.

When "1" is written: Forcibly stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.12.7 Programming notes

(1) Since the buzzer signal is generated asynchronously from the register BZON, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the buzzer signal output is in the enable status (BZON = "1" or BZSHT = "1"), unstable clock is output from the output terminal at the time of return from the SLEEP status. Consequently, when shifting to the SLEEP status, you should set the buzzer signal output to the disable status (BZON = BZSHT = "0") prior to executing the SLP instruction.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status.

5.13 Remote Controller (REM)

5.13.1 Configuration of remote controller

The S1C88848 has a remote controller (REM circuit) built-in. It can easily adapt to various remote controllers by connecting an infrared remote LED and a transistor as shown in Figure 5.13.1.1.

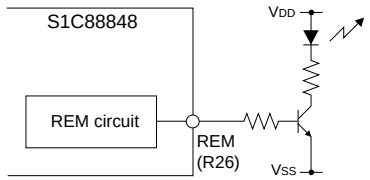


Fig. 5.13.1.1 Remote LED control circuit

Figure 5.13.1.2 shows the configuration of the REM circuit.

The generally used infrared remote controllers employ a method that generates transmission waveforms in pulse modulation as shown in Figure 5.13.1.3 and transmits the signal.
First the transmission code is modulated in a pulse phase modulation (PPM) method to generate the modulation signal, and the carrier that has constant frequency is amplitude-modulated (AM) using the modulation signal. As a result, transmission waveforms are generated. Transmission is done by driving the infrared LED using the transmission waveform.

In this remote controller, the carrier generated from the carrier generation circuit is controlled to turn the output ON and OFF and the transmission waveform is generated. This transmission waveform can be output from the REM (R26) terminal. At initial reset and while remote output stops, the REM (R26) terminal goes low level (VSS). The carrier frequency and duty ratio can be selected by the software from among 4 types. (details are explained later) This remote controller supports the following two modes for controlling the modulation signal (carrier ON / OFF).

- Soft-timer mode (Software timer control mode)
- Hard-timer mode (Hardware timer control mode)

In the soft-timer mode, the carrier ON / OFF timing and the time are controlled by the software. The optional ON / OFF time can be set within the range that is controlled by the software. In the hard-timer mode, the carrier ON / OFF timing and the output time are controlled by the REMOUT time generator based on the reference cycle (τ) that is generated by the τ (reference cycle) generation circuit dividing the carrier. For the reference cycle (τ), the carrier dividing ratio can be selected by the software from 4 types. The REMOUT (REM output) time can be selected by the software from 4 types, 0 to 3 times as long as the reference cycle (τ). The ON / OFF time is limited to some extent in comparison with the soft-timer mode, but the software's share is decreased because the interrupt can be used. Features of the soft-timer mode and hard-timer mode are shown in Table 5.13.1.1.

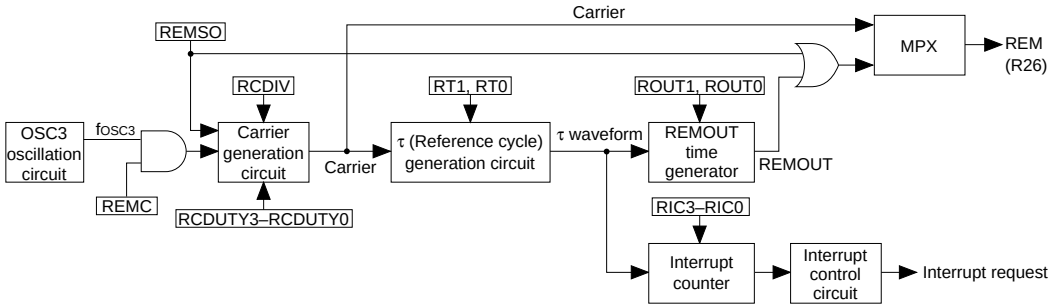


Fig. 5.13.1.2 Configuration of REM circuit

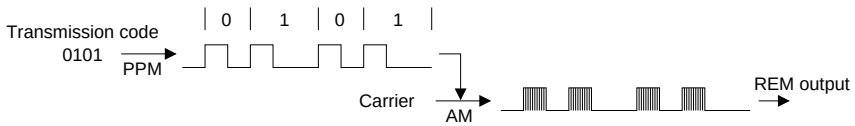


Fig. 5.13.1.3 Remote transmission method

Table 5.13.1.1 Features of soft-timer mode and hard-timer mode

Item	Soft-timer mode	Hard-timer mode
Processing of other routines during REM output	Difficult	Possible
Reference cycle (τ) sway during REM transmission	Source oscillation sway and errors caused by instruction cycles	Source oscillation sway only
Setting of REM output width	Variable to any width	Fixed to several widths
Relation between REM reference cycle and modulation frequency cycle	Variable	Fixed to several cycles
Carrier waveform	Duty slightly disturbed before and after ON time	Stabilized at setting

5.13.2 Mask option

R26 output port specification
R26 ..... ☐ DC output
☐ $\overline{\text{TOUT}}$ output
☐ REM output

The R26 output port can be configured for REM output, $\overline{\text{TOUT}}$ output ($\overline{\text{TOUT}}$ inverted output) or general-purpose DC output by mask option.
Selecting REM output allows remote control carrier output by the control described in Sections 5.13.3 through 5.13.5. Refer to Section 5.5, "Output Ports (R ports)", for how to control DC output and $\overline{\text{TOUT}}$ output.

5.13.3 Carrier

The carrier is generated by the carrier generation circuit using the OSC3 clock as the source clock. The carrier cycle and duty ratio selections and the carrier generation circuit ON / OFF control can be done by software.
The control for the carrier is same procedure for both the soft-timer mode and the hard-timer mode. Perform the carrier settings before starting the transmission in each mode.
The carrier cycle can be selected as a division ratio of the OSC3 clock using the REM carrier cycle setting register RCDIV. When "0" is written to RCDIV, f_{OSC3} / 64 is selected and when "1" is written, f_{OSC3} / 96 is selected.
The carrier duty ratio is set as shown in Table 5.13.3.1 using the REM carrier duty setting register RCDUTY0–RCDUTY3. The selectable values and range depend on the RCDIV value. When RCDIV = "1", the remote controller does not output the REM signal if RCDUTY is "1100" or more. When RCDIV = "0", setting RCDUTY to "0100" or more selects the same duty ratio as RCDUTY = "0011".
Carrier settings can be done even when the OSC3 oscillation circuit is in OFF status. Furthermore, when these are set once, the set contents are maintained until an initial reset is performed.

Note: The setting of RCDIV and the RCDUTY should be done when the REM circuit is OFF (REMC = "0") before starting remote transmission. If changing the contents when the REM circuit is ON, it may cause a malfunction.

Table 5.13.3.1 Carrier duty ratio

RCDUTY				Carrier duty ratio	
3	2	1	0	RCDIV = "0" (f_{OSC3}/64)	RCDIV = "1" (f_{OSC3}/96)
1	0	1	1	–	12/24
1	0	1	0	–	11/24
1	0	0	1	–	10/24
1	0	0	0	–	9/24
0	1	1	1	–	8/24
0	1	1	0	–	7/24
0	1	0	1	–	6/24
0	1	0	0	–	5/24
0	0	1	1	4/8	4/24
0	0	1	0	3/8	3/24
0	0	0	1	2/8	2/24
0	0	0	0	1/8	1/24

The carrier generation circuit is turned ON and OFF by the REM carrier ON / OFF register REMC. By writing "1" to REMC, the carrier generation circuit goes ON and generates the carrier. When REMC is set to "0" by writing, the carrier generation circuit goes OFF and the carrier generation stops.
The OSC3 clock is divided to generate the carrier. Therefore, the OSC3 oscillation circuit must be ON before starting remote output. Remote output should be done when the OSC3 oscillation has stabilized. Make sure that the OSC3 oscillation has stabilized before starting a remote controller. After turning the OSC3 oscillation circuit ON until the oscillation stabilizes, an interval of several 100 µsec to several 10 msec is required. Therefore, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting a remote control output. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to ON status.
Figure 5.13.3.1 shows the carrier waveform.

Note: Except when outputting the remote control waveform, REMC should be fixed at "0" to prevent outputting unnecessary waveforms and to reduce current consumption. However at initial reset, the REMC register is set to "1" for initializing the carrier generation circuit. The register must not be set to "0" until after initialization (within 32 machine cycles).

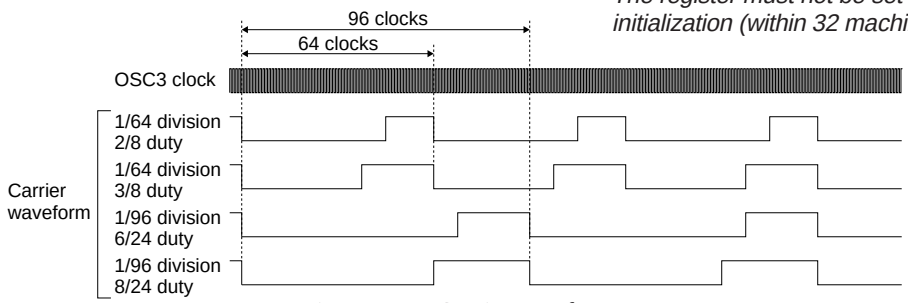


Fig. 5.13.3.1 Carrier waveform

5.13.4 Soft-timer mode

In the soft-timer mode, software controls the ON / OFF time and timing of the carrier output. This mode does not use the τ (reference cycle) generation circuit, REMOUT time generator and interrupt control circuit that are used in the hard-timer mode, and operates with the configuration as shown in Figure 5.13.4.1.

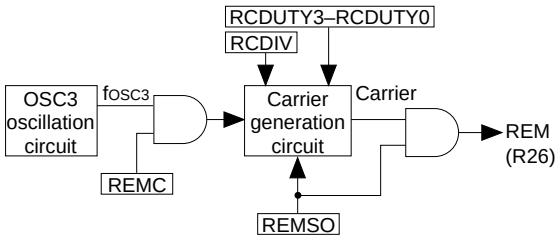


Fig. 5.13.4.1 REM circuit configuration in soft-timer mode

The ON / OFF control of the carrier output is done using the REM forced output ON / OFF register REMSO. By writing "1" to REMSO, the carrier is output to the REM (R26) terminal and when "0" is written, the REM (R26) terminal goes low level (VSS). However, the carrier must be generated by writing "1" to REMC before writing "1" to REMSO. Figure 5.13.4.2 shows the timing chart in the soft-timer mode.

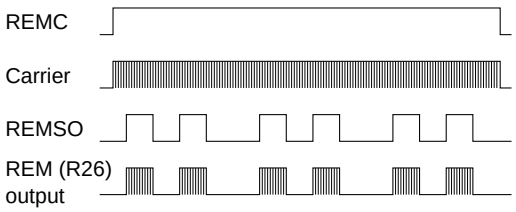


Fig. 5.13.4.2 Timing chart (soft-timer mode)

The remote output using REMSO is started in synchronization with the carrier generation circuit by the hardware.

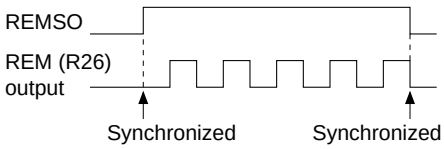


Fig. 5.13.4.3 Carrier output control using REMSO

Note: Be sure to control the carrier output using REMSO. Do not control the carrier output using REMC by setting the REMSO register to "1".

5.13.5 Hard-timer mode and REM interrupt

In the soft-timer mode, the CPU is occupied for the remote output processing so that it has no flexibility for execution of other routines. To alleviate this problem, the S1C88848 supports the hard-timer mode explained below.
In the hard-timer mode, the carrier ON / OFF, that is controlled using the REM forced output ON / OFF register REMSO in the soft-timer mode, is done in the hardware by using the τ (reference cycle) generation circuit and the REMOUT time generator. τ (reference cycle) is generated from the carrier by dividing, and is used for reference of the carrier ON / OFF time in the hard-timer mode. The dividing ratio of τ (reference cycle) is selected from 4 types by the software. The carrier ON / OFF time can be set for each transmission data bit by the software using τ (reference cycle) as reference. Furthermore, the interrupt function is provided so that the setting can be done without synchronizing with the timing of the carrier output.
The interrupt timing can also be set by the software using τ (reference cycle) as the reference same as the ON / OFF time.
The circuit in the hard-timer mode is configured as shown in Figure 5.13.1.2, and all the REM circuit is used. However, REMSO that is used to control the carrier output in the soft-timer mode should be fixed at "0". If "1" is written to REMSO, REM output are forcibly done regardless of the control of the hard-timer mode.

■ τ (reference cycle)

τ (reference cycle) is used as reference for the carrier output ON time and interrupt timing specified by the software, and is generated by the τ (reference cycle) generation circuit by dividing carrier. This dividing ratio can be selected using the REM τ cycle setting registers RT1 and RT0 from 4 types as shown in Table 5.13.5.1.

Table 5.13.5.1 τ (reference cycle) setting

RT1	RT0	τ dividing ratio
1	1	fcarrier / 32
1	0	fcarrier / 20
0	1	fcarrier / 16
0	0	fcarrier / 12

* fcarrier indicates carrier frequency. It is selected with the REM carrier cycle setting register RCDIV.

The actual time of τ (reference cycle) can be found using the following expression according to the OSC3 oscillation frequency, carrier cycle selection and the above selection.

τ (reference cycle) [sec] = 1 / (f_{OSC3} × DIV1 × DIV2)

f_{OSC3}: OSC3 oscillation frequency
DIV1: Content of carrier cycle (dividing ratio) set with RCDIV (1/64 or 1/96)
DIV2: Content of τ dividing ratio set with RT1 and RT0 (1/12, 1/16, 1/20 or 1/32)

Table 5.13.5.2 shows the examples of τ (reference cycle) when f_{OSC3} is 3.64 MHz.

Table 5.13.5.2 τ (reference cycle) examples

Register settings			τ (reference cycle)
RCDIV	RT1	RT0	f_{OSC3} = 3.64 MHz
1	1	1	0.844 msec (1184.9 Hz)
1	1	0	0.527 msec (1895.8 Hz)
1	0	1	0.422 msec (2369.8 Hz)
1	0	0	0.316 msec (3159.7 Hz)
0	1	1	0.563 msec (1777.3 Hz)
0	1	0	0.352 msec (2843.8 Hz)
0	0	1	0.281 msec (3554.7 Hz)
0	0	0	0.211 msec (4739.6 Hz)

The carrier output ON time can be set to 4 types (0τ to 3τ) based on the τ (reference cycle) set, so set the τ (reference cycle) after due consideration.

Figure 5.13.5.1 shows the τ waveform when fcarrier /12 has been selected.
τ waveform is kept on outputting from the τ (reference cycle) generation circuit according to the set dividing ratio while REMC is "1".

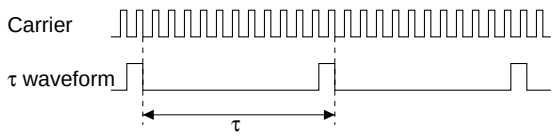


Fig. 5.13.5.1 τ waveform (when fcarrier /12 is selected)

It is possible to set τ (reference cycle) even if the OSC3 oscillation circuit is in OFF status. Furthermore, when it is set once, the set contents are maintained until an initial reset is performed.

When REMC is set to "0", the REM circuit stops synchronously with τ. This timing is shown in Figure 5.13.5.2.

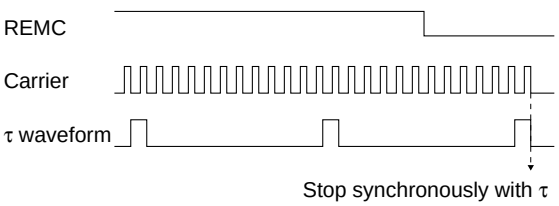


Fig. 5.13.5.2 REM circuit stop timing

Maximum of 384 machine cycles* are required until the REM circuit stops after REMC is set to "0". Even if the CPU clock is changed from OSC3 to OSC1 after REMC is set to "0", OSC3 must not be turned OFF before the REM circuit stops.

* This time depends on the value of the set τ cycle. If a shorter τ cycle is set, the maximum time required for the REM circuit to stop after REMC is set to "0" is shortened.

If the REM circuit is restarted from OFF state with REMC = "0", the timing of the τ waveform rises one carrier before the set division ratio.

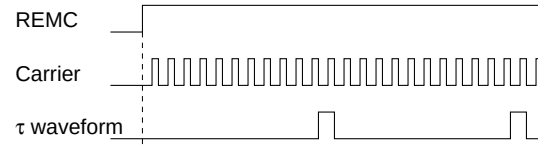


Fig. 5.13.5.3 τ generation circuit restart timing

Note: The setting of the RT register should be done when the REM circuit is OFF (REMC = "0") before starting remote transmission. Changing the contents when the REM circuit is ON may cause a malfunction.

■ Setting of carrier output width

In the soft-timer mode, the carrier output width (carrier output ON time) is controlled by writing to REMSO, but in the hard-timer mode, it can be specified with values 0 to 3, which mean the number of τ cycles described above, in each transmission data bit. Since the carrier output ON/OFF is controlled by the hardware in synchronizing with τ waveform, it is unnecessary to watch the ON time and to specify the OFF timing by the software. The carrier output width can be selected by writing data to the REM output ON time setting register ROUT1 and ROUT0 from among 4 types as shown in Table 5.13.5.3.

Table 5.13.5.3 Setting of carrier output width

ROUT1	ROUT0	Carrier output width
1	1	3τ
1	0	2τ
0	1	1τ
0	0	0τ

The carrier is output in synchronizing with the rising edge of the τ waveform after writing data to ROUT. Data written to ROUT is maintained while the REM circuit is ON until the next data is written.

The carrier output starts using the write signal for this register and the carrier output will be ON from the rising edge of the τ waveform immediately after that until the period set in the register has passed. In other words, the register data is valid only one time after writing. Consequently, data must be written every time even when outputting the same data successively.
ROUT is set to "0H" at initial reset and when REMC is set to "0". Consequently, after turning the REM circuit ON ("1" is written to REMC), REM output becomes low level (V_{SS}) until a value other than "0H" is written to ROUT.
Figure 5.13.5.4 shows the timing of data writing to the ROUT register and the carrier output.

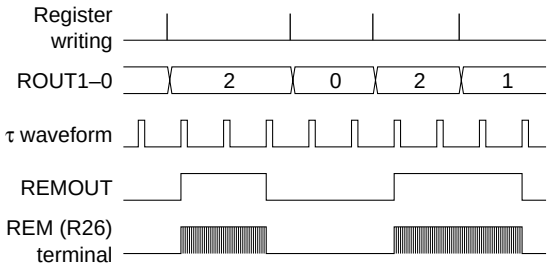


Fig. 5.13.5.4 Carrier output timing

Note: The values set in ROUT is taken into the REMOUT time generator synchronously with the rise of a τ waveform. For this reason, avoid writing data into the ROUT register during one carrier cycle immediately before and after the rise of the τ waveform.

■ Remote controller (REM) interrupt

The carrier output ON time for one transmission data bit is controlled by writing data to the above mentioned REM output ON time setting register ROUT. The OFF time is from when the output is turned OFF to when the next carrier output starts by writing to the same register. Since the carrier output is turned ON at the rising edge of the τ waveform after writing data, the next data must be written during the last τ cycle in the carrier OFF period of the current transmission data. To decide its timing, an interrupt is used in the hard-timer mode.
By using the interrupt, the CPU is released from the processing such as a timing watch, and can execute other processing.

The timing to generate interrupt can be set by the software using τ cycle as reference the same as the carrier output width. The interrupt timing can be selected by writing data to the REM interrupt generation counter setting register RIC3–RIC0. The time until an interrupt request occurs (t_{RI}) is given by:

$$t_{RI} = t_{RIC} + (1 \pm 1 \text{ instruction cycle})$$

Where t_{RIC} is the time set by RIC. The relation between RIC and t_{RIC} is:

$$t_{RIC} = (RIC3 \times 2^3 + RIC2 \times 2^2 + RIC1 \times 2 + RIC0) \times \tau$$

As with the REMOUT time generator, the REM interrupt counter starts counting synchronously with the rising edge of the τ waveform. The interrupt control circuit generates a REM interrupt synchronously with the τ pulse when the count is completed.

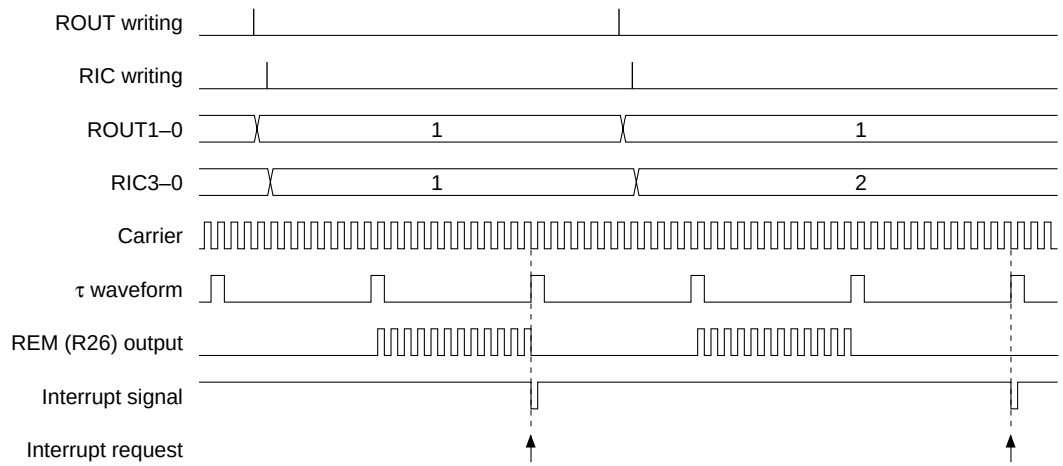


Fig. 5.13.5.5 REM interrupt timing

The τ waveform is counted at every rising edge. When the count becomes the number set in RIC, the interrupt factor flag FREM is set to "1" and an interrupt occurs in synchronization with that riging edge.
Set the next carrier output width and the interrupt timing using this interrupt.
The REM interrupt can be disabled through the interrupt enable register EREM. However, regardless of the setting of EREM, FREM is set to "1" when the counting of the interrupt τ cycles are completed.
FREM is reset to "0" by writing "1".
In addition, a priority level of the REM interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PREM0 and PREM1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.15 Interrupt and Standby Status".
The exception processing vector addresses for the REM interrupt factor is set to 000024H.
Figure 5.13.5.6 shows the configuration of the REM interrupt circuit.

Data written to RIC is maintained while the REM circuit is ON until the next data is written. However, the counting of τ waveform starts using the write signal for RIC the same as ROUT, so this register data is valid only one time after writing. Consequently, data must be written every time even when generating the next interrupt in the same cycle count.
The RIC register is undefined at initial reset. However, the counting of τ cycles is not performed until RIC is written after that.

Notes:
- *Once data has been written in RIC, avoid writing other data into the register before a REM interrupt occurs (which would otherwise cause an invalid interrupt).*
- *The values allowed for RIC are 0 to 0EH.*

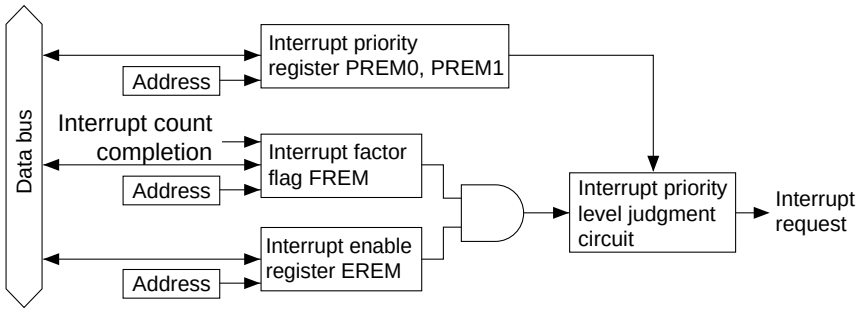


Fig. 5.13.5.6 Configuration of the REM interrupt circuit

5.13.6 Control of remote controller

Table 5.13.6.1 shows the remote controller control bits.

Table 5.13.6.1(a) Remote controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF28	D7	–	–	–	–	–		"0" when being read
	D6	RT1	REM τ cycle (division ratio) setting RT1 RT0 Division ratio 1 1 1/32 1 0 1/20 0 1 1/16 0 0 1/12			0	R/W	
	D5	RT0				0	R/W	
	D4	RCDIV	REM carrier cycle setting	fosc3/96	fosc3/64	0	R/W	
	D3	RCDUTY3	REM carrier duty setting RCDUTYx (3 2 1 0) Duty (RCDIV = 0) Duty (RCDIV = 1) 1 0 1 1 – 12/24 1 0 1 0 – 11/24 1 0 0 1 – 10/24 1 0 0 0 – 9/24 0 1 1 1 – 8/24 0 1 1 0 – 7/24 0 1 0 1 – 6/24 0 1 0 0 – 5/24 0 0 1 1 4/8 4/24 0 0 1 0 3/8 3/24 0 0 0 1 2/8 2/24 0 0 0 0 1/8 1/24			0	R/W	∗2
	D2	RCDUTY2				0	R/W	
	D1	RCDUTY1				0	R/W	
	D0	RCDUTY0				0	R/W	
00FF29	D7	RIC3	REM interrupt counter setting			–	W	∗1
	D6	RIC2	(0–0EH: 0–14τ clock)			–	W	Constantly "0" when
	D5	RIC1	The counter operates one-time only by writing			–	W	being read
	D4	RIC0	and is reset to 0FH after counting.			–	W	
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		Constantly "0" when
	D1	–	–	–	–	–		being read
	D0	–	–	–	–	–		
00FF2A	D7	ROUT1	REM output duration setting (0–3: 0–3τ)			0	R/W	∗1
	D6	ROUT0	Operates one-time only by writing.			0	R/W	
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		Constantly "0" when
	D2	–	–	–	–	–		being read
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF21	D7	PREM1	REM carrier interrupt priority register	PREM1 PREM0 PPT3 PPT2 PPT1 PPT0 PK11 PK10 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PREM0				0	R/W	
	D5	PPT3	Programmable timer 2–3 interrupt			0	R/W	
	D4	PPT2	priority register			0	R/W	
	D3	PPT1	Programmable timer 0–1 interrupt			0	R/W	
	D2	PPT0	priority register			0	R/W	
	D1	PK11	K10–K11 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	

∗1 Effective only for hardware timer method. Writing is not allowed in software timer method.

∗2 When RCDIV = "1", the REM signal is not output if RCDUTYx is "1100" or more.
When RCDIV = "0", settings RCDUTYx to "0100" or more are same as RCDUTYx = "0011".

Table 5.13.6.1(b) Remote controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF26	D7	EPT3	Programmable timer 3 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT2	Programmable timer 2 interrupt enable register			0	R/W	
	D5	EREM	REM carrier interrupt enable register			0	R/W	
	D4	REMC	REM carrier generation On/Off	On	Off	1	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF27	D7	FPT3	Programmable timer 3 interrupt factor flag	(R) Generated	(R) Not generated	0	R/W	
	D6	FPT2	Programmable timer 2 interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D5	FREM	REM carrier interrupt factor flag			0	R/W	
	D4	REMSO	Forced REM output On/Off	On	Off	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

REMC: 00FF26H•D4

Turns the carrier generation on and off.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to REMC, the carrier generation circuit turns ON.
Writing "0" turns the carrier generation circuit OFF.
At initial reset, REMC is set to "1" (ON).

REMSO: 00FF27H•D4

Controls the carrier output in the soft-timer mode.

When "1" is written: Carrier output ON
When "0" is written: Carrier output OFF
Reading: Valid

By writing "1" to REMSO when REMC has been set to "1", carrier is output from the REM (R26) terminal. When "0" is written, the REM (R26) terminal goes to low level (V_{SS}).
At initial reset, REMSO is set to "0" (carrier output OFF).

Note: The REMSO register is for the exclusive use of the soft-timer mode. When controlling with the hard-timer mode, REMSO should be fixed at "0".

RCDIV: 00FF28H•D4

Selects the carrier cycle.

When "1" is written: f_{OSC3} / 96
When "0" is written: f_{OSC3} / 64
Reading: Valid

When "1" is written to RCDIV, the carrier frequency is set to f_{OSC3} / 96. When "0" is written, it is set to f_{OSC3} / 64.
This setting must be done when the remote controller is in OFF status (REMC = "0").
At initial reset, RCDIV is set to "0" (f_{OSC3} / 64).

RCDUTY0–RCDUTY3: 00FF28H•D0–D3

Selects the duty ratio of the carrier.
Duty ratio set by RCDUTY0–RCDUTY3 varies according to the carrier cycle set by RCDIV as shown in the table below. When RCDIV = "1", the REM signal is not output if RCDUTY is "1100" or more. When RCDIV = "0", settings RCDUTY to "0100" or more are same as RCDUTY = "0011".

Table 5.13.6.2 Selection of carrier duty ratio

RCDUTY				Carrier duty ratio	
3	2	1	0	RCDIV = "0" (f_{OSC3}/64)	RCDIV = "1" (f_{OSC3}/96)
1	0	1	1	–	12/24
1	0	1	0	–	11/24
1	0	0	1	–	10/24
1	0	0	0	–	9/24
0	1	1	1	–	8/24
0	1	1	0	–	7/24
0	1	0	1	–	6/24
0	1	0	0	–	5/24
0	0	1	1	4/8	4/24
0	0	1	0	3/8	3/24
0	0	0	1	2/8	2/24
0	0	0	0	1/8	1/24

This setting must be done when the remote controller is in OFF status (REMC = "0").
At initial reset, RCDUTY is set to "0H".

RT0, RT1: 00FF28H•D5, D6

Selects the τ (reference cycle).
When controlling in the hard-timer mode, select the τ (reference cycle) that is used as a reference for the timing generation.

Table 5.13.6.3 τ (reference cycle) setting

RT1	RT0	τ dividing ratio
1	1	fcarrier / 32
1	0	fcarrier / 20
0	1	fcarrier / 16
0	0	fcarrier / 12

* fcarrier indicates the carrier frequency selected with RCDIV.

This setting must be done when the remote controller is in OFF status (REMC = "0").
At initial reset, RT is set to "0" (fcarrier / 12).

ROUT0, ROUT1: 00FF2AH•D6, D7

When controlling in the hard-timer mode, select the carrier output width.

Table 5.13.6.4 Setting of carrier output width

ROUT1	ROUT0	Carrier output width
1	1	3τ
1	0	2τ
0	1	1τ
0	0	0τ

By writing data to this register, the carrier for set τ cycles is output from the REM (R26) terminal in synchronization with the rising edge of the τ waveform immediately after that.
The setting (writing) of carrier output width must be done at every bit of the transmission data.
At initial reset and when REMC is set to "0", ROUT is set to "0" (0τ).

Note: The ROUT register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

RIC0–RIC3: 00FF29H•D4–D7

The τ cycle count for generating a REM interrupt is set to this register.
By writing data to this register when the REM circuit has been ON (REMC = "1"), the counting of τ waveform is started by synchronizing with the rising edge of the τ waveform immediately after that. When the count becomes the number set in this register, an interrupt occurs. Set the next transmission data and interrupt timing using this interrupt.
Do not set "0FH" in this register.
The setting (writing) of interrupt τ cycle must be done at every bit of the transmission data.
RIC is exclusively for writing, it always becomes "0" during reading.
At initial reset, RIC is undefined.

Note: The RIC register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

PREM0, PREM1: 00FF21H•D6, D7

Sets the REM interrupt priority level. The two bits PREM0 and PREM1 are the interrupt priority registers corresponding to the REM interrupt. Table 5.13.6.5 shows the interrupt priority level which can be set by this register.

Table 5.13.6.5 Interrupt priority level settings

PREM1	PREM0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, PREM is set to "0" (level 0).

EREM: 00FF26H•D5

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

EREM is the interrupt enable register that corresponds to the REM interrupt factor. The REM interrupt is enabled when this register is set to "1" and is disabled when this register is set to "0".
At initial reset, EREM is set to "0" (interrupt disabled).

FREM: 00FF27H•D5

Indicates the REM interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FREM is the interrupt factor flag that corresponds to the REM interrupt and is set to "1" when the interrupt τ cycle set with the RIC register has passed (counting of the τ waveform has completed).

When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, FREM is reset to "0".

5.13.7 Programming notes

(1) The following programming steps are needed to initialize the REM circuit (τ clock, REM interrupt circuit):

- Write data at addresses 00FF28H and 00FF29H in that order within 80 machine clocks (equivalent to ten 4-cycle instructions) after release from initial reset.
- With REMC = "0", the REM circuit must not be stopped within cycle of 1τ after data has been written at address 00FF29H.
- To initialize the REM interrupt circuit, write "1" to the REM interrupt factor flag FREM to clear it at least an interval of 2τ after data has been written at address 00FF29H.

(2) After initial reset, REMC is set to "1" to initialize the carrier generation circuit. REMC can only be reset to "0" after initialization (at least 32 machine cycles later).

(3) The REM circuit does not stop immediately after REMC is reset to "0". It stops synchronously with the interval τ, during which OSC3 must be held ON.

(4) With the REM circuit in operation, do not write data at addresses 00FF29H and 00FF2AH (REM interrupt generation counter and REM output ON time setting register) during an interval of one carrier before and after the rise of τ.

(5) With the REM circuit in operation, do not write data at addresses 00FF28H (τ cycle setting register).

(6) During the operation under hard-timer mode, the REMSO register must be fixed at "0".

(7) If the RIC register is set again before a REM interrupt occurs with the RIC register set, an invalid interrupt may occur.

(8) The values that can be set in the REM interrupt generation counter are from 0 to EH. Remember, writing FH into RIC may cause an error.

(9) Soft-timer mode cannot coexist with hard-timer mode.
To use them in combination, stop the REM circuit before selecting either.

5.14 Supply Voltage Detection (SVD) Circuit

5.14.1 Configuration of SVD circuit

The S1C88848 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON / OFF and the SVD criteria voltage setting can be done with software.
Figure 5.14.1.1 shows the configuration of the SVD circuit.

5.14.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 16 types shown in Table 5.14.2.1 by the SVDS3–SVDS0 registers.

Table 5.14.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	4.35
1	1	1	0	4.17
1	1	0	1	4.00
1	1	0	0	3.83
1	0	1	1	3.67
1	0	1	0	3.50
1	0	0	1	3.33
1	0	0	0	3.17
0	1	1	1	3.00
0	1	1	0	2.83
0	1	0	1	2.67
0	1	0	0	2.50
0	0	1	1	2.33
0	0	1	0	2.17
0	0	0	1	2.00
0	0	0	0	1.83

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.
To obtain a stable detection result, the SVD circuit must be ON for at least 100 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

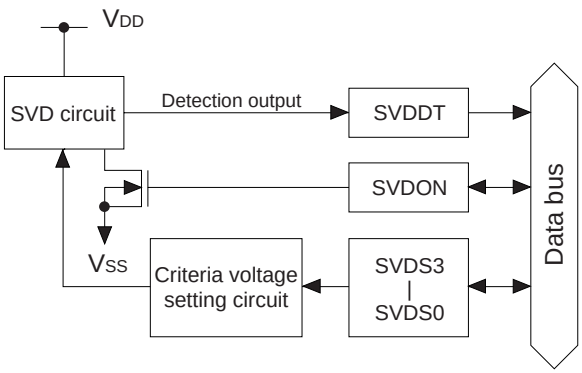


Fig. 5.14.1.1 Configuration of SVD circuit

5.14.3 Control of SVD circuit

Table 5.14.3.1 shows the SVD circuit control bits.

Table 5.14.3.1 Control bits of SVD circuit

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF12	D7	–	–	–	–	–		Constantly "0" when
	D6	–	–	–	–	–		being read
	D5	SVDDT	SVD data	Low	Normal	0	R	
	D4	SVDON	SVD circuit On/Off control	On	Off	0	R/W	
	D3	SVDS3	SVD criteria voltage setting					
	D2	SVDS2						
	D1	SVDS1						
	D0	SVDS0						

SVDS3	SVDS2	SVDS1	SVDS0	Voltage	SR	R/W
1	1	1	1	4.35 V	0	R/W
1	1	1	0	4.17 V		
1	1	0	1	4.00 V		
1	1	0	0	3.83 V		
1	0	1	1	3.67 V	0	R/W
1	0	1	0	3.50 V		
1	0	0	1	3.33 V		
1	0	0	0	3.17 V		
0	1	1	1	3.00 V	0	R/W
0	1	1	0	2.83 V		
0	1	0	1	2.67 V		
0	1	0	0	2.50 V		
0	0	1	1	2.33 V		
0	0	1	0	2.17 V	0	R/W
0	0	0	1	2.00 V		
0	0	0	0	1.83 V		

SVDS3–SVDS0: 00FF12H•D3–D0

Criteria voltage for SVD is set as shown in Table 5.14.2.1.
At initial reset, this register is set to "0".

SVDON: 00FF12H•D4

Controls the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a supply voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least 100 µsec.
At initial reset, this register is set to "0".

SVDDT: 00FF12H•D5

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

5.14.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least 100 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

5.15 Interrupt and Standby Status

■ Types of interrupts

Eight systems and 18 types of interrupts have been provided for the S1C88848.

External interrupt
- K00–K07 input interrupt (2 types)
- K10–K11 input interrupt (1 type)

Internal interrupt
- Clock timer interrupt (4 types)
- Stopwatch timer interrupt (3 types)
- Programmable timer 0–1 interrupt (2 types)
- Programmable timer 2–3 interrupt (2 types)
- Serial interface interrupt (3 types)
- Remote controller interrupt (1 type)

An interrupt factor flag that indicates the generation of an interrupt factor and an interrupt enable register that sets enable / disable for interrupt requests have been provided for each interrupt and interrupt generation can be optionally set for each factor.
In addition, an interrupt priority register has been provided for each system of interrupts and the priority of interrupt processing can be set to 3 levels in each system.
Figure 5.15.1 shows the configuration of the interrupt circuit.

Refer to the explanations of the respective peripheral circuits for details on each interrupt.

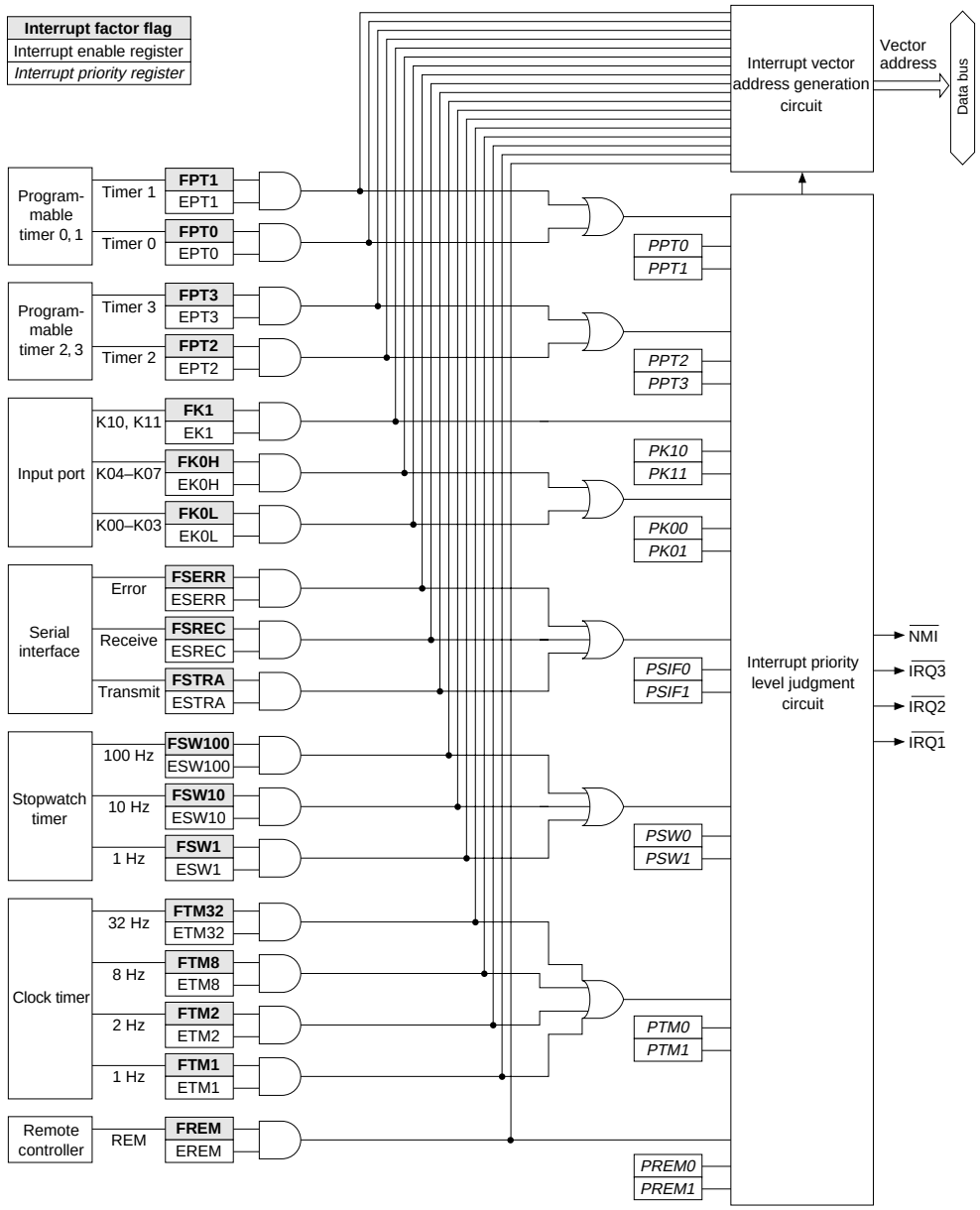


Fig. 5.15.1 Configuration of interrupt circuit

■ HALT status

By executing the program's HALT instruction, the S1C88848 shifts to the HALT status.
Since CPU operation stops in the HALT status, power consumption can be reduced with only peripheral circuit operation.
Cancellation of the HALT status is done by initial reset or an optional interrupt request, and the CPU restarts program execution from an exception processing routine.
See the "S1C88 Core CPU Manual" for the HALT status and reactivation sequence.

■ SLEEP status

By executing the program's SLP instruction, the S1C88848 shifts to the SLEEP status.
Since the operation of the CPU and peripheral circuits stop completely in the SLEEP status, power consumption can be reduced even more than in the HALT status.
Cancellation of the SLEEP status is done by initial reset or an input interrupt from the input port. The CPU reactivates after waiting 128 / fOSC1 seconds of oscillation stabilization time. At this time, the CPU restarts program execution from an exception processing routine (input interrupt routine).

Note: Since oscillation is unstable for a short time after reactivation from the SLEEP status, the wait time is not always 3.9 msec even when using the 32.768 kHz crystal oscillator for the OSC1 oscillation circuit.

5.15.1 Interrupt generation conditions

The interrupt factor flags that indicate the generation of their respective interrupt factors are provided for the previously indicated 8 systems and 18 types of interrupts and they will be set to "1" by the generation of a factor.

In addition, interrupt enable registers with a 1 to 1 correspondence to each of the interrupt factor flags are provided. An interrupt is enabled when "1" is written and interrupt is disabled when "0" is written.

The CPU manages the enable / disable of interrupt requests at the interrupt priority level. An interrupt priority register that sets the priority level is provided for each of the interrupts of the 8 systems and the CPU accepts only interrupts above the level that has been indicated with the interrupt flags (I0 and I1).
Consequently, the following three conditions are necessary for the CPU to accept the interrupt.

(1) The interrupt factor flag has been set to "1" by generation of an interrupt factor.
(2) The interrupt enable register corresponding to the above has been set to "1".
(3) The interrupt priority register corresponding to the above has been set to a priority level higher than the interrupt flag (I0 and I1) setting.

The CPU initially samples the interrupt for the first op-code fetch cycle of each instruction. Thereupon, the CPU shifts to the exception processing when the above mentioned conditions have been established.
See the "S1C88 Core CPU Manual" for the exception processing sequence.

5.15.2 Interrupt factor flag

Table 5.15.2.1 shows the correspondence between the factors generating an interrupt and the interrupt factor flags.
The corresponding interrupt factor flags are set to "1" by generation of the respective interrupt factors.
The corresponding interrupt factor can be confirmed by reading the flags through software.

Table 5.15.2.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 underflow	FPT1	(00FF25 D7)
Programmable timer 0 underflow	FPT0	(00FF25 D6)
Programmable timer 3 underflow	FPT3	(00FF27 D7)
Programmable timer 2 underflow	FPT2	(00FF27 D6)
Non matching of the K10–K11 inputs and the input comparison registers KCP10–KCP11	FK1	(00FF25 D5)
Non matching of the K04–K07 inputs and the input comparison registers KCP04–KCP07	FK0H	(00FF25 D4)
Non matching of the K00–K03 inputs and the input comparison registers KCP00–KCP03	FK0L	(00FF25 D3)
Serial interface receiving error (in asynchronous mode)	FSERR	(00FF25 D2)
Serial interface receiving completion	FSREC	(00FF25 D1)
Serial interface transmitting completion	FSTRA	(00FF25 D0)
Falling edge of the stopwatch timer 100 Hz signal	FSW100	(00FF24 D6)
Falling edge of the stopwatch timer 10 Hz signal	FSW10	(00FF24 D5)
Falling edge of the stopwatch timer 1 Hz signal	FSW1	(00FF24 D4)
Rising edge of the clock timer 32 Hz signal	FTM32	(00FF24 D3)
Rising edge of the clock timer 8 Hz signal	FTM8	(00FF24 D2)
Rising edge of the clock timer 2 Hz signal	FTM2	(00FF24 D1)
Rising edge of the clock timer 1 Hz signal	FTM1	(00FF24 D0)
Remote controller output control	FREM	(00FF27 D5)

Interrupt factor flag that has been set to "1" is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are reset to "0".

Note: When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

5.15.3 Interrupt enable register

The interrupt enable register has a 1 to 1 correspondence with each interrupt factor flag and enable / disable of interrupt requests can be set.

When "1" is written to the interrupt enable register, an interrupt request is enabled, and is disabled when "0" is written. This register also permits reading, thus making it possible to confirm that a status has been set.
At initial reset, the interrupt enable registers are set to "0" and shifts to the interrupt disable status.
Table 5.15.3.1 shows the correspondence between the interrupt enable registers and the interrupt factor flags.

5.15.4 Interrupt priority register and interrupt priority level

The interrupt priority registers shown in Table 5.15.4.1 are set to each system of interrupts and the interrupt priority levels for the CPU can be set to the optional priority level (0–3). As a result, it is possible to have multiple interrupts that match the system's interrupt processing priority levels.

The interrupt priority level between each system can optionally be set to three levels by the interrupt priority register. However, when more than one system is set to the same priority level, they are processed according to the default priority level.

Table 5.15.4.2 Setting of interrupt priority level

P*1	P*0	Interrupt priority level	
1	1	Level 3	($\overline{\text{IRQ3}}$)
1	0	Level 2	($\overline{\text{IRQ2}}$)
0	1	Level 1	($\overline{\text{IRQ1}}$)
0	0	Level 0	(non)

Table 5.15.3.1 Interrupt enable registers and interrupt factor flags

Interrupt	Interrupt factor flag		Interrupt enable register	
Programmable timer 1	FPT1	(00FF25 D7)	EPT1	(00FF23 D7)
Programmable timer 0	FPT0	(00FF25 D6)	EPT0	(00FF23 D6)
Programmable timer 3	FPT3	(00FF27 D7)	EPT3	(00FF26 D7)
Programmable timer 2	FPT2	(00FF27 D6)	EPT2	(00FF26 D6)
K10–K11 input	FK1	(00FF25 D5)	EK1	(00FF23 D5)
K04–K07 input	FK0H	(00FF25 D4)	EK0H	(00FF23 D4)
K00–K03 input	FK0L	(00FF25 D3)	EK0L	(00FF23 D3)
Serial interface receiving error	FSERR	(00FF25 D2)	ESERR	(00FF23 D2)
Serial interface receiving completion	FSREC	(00FF25 D1)	ESREC	(00FF23 D1)
Serial interface transmitting completion	FSTRA	(00FF25 D0)	ESTRA	(00FF23 D0)
Stopwatch timer 100 Hz	FSW100	(00FF24 D6)	ESW100	(00FF22 D6)
Stopwatch timer 10 Hz	FSW10	(00FF24 D5)	ESW10	(00FF22 D5)
Stopwatch timer 1 Hz	FSW1	(00FF24 D4)	ESW1	(00FF22 D4)
Clock timer 32 Hz	FTM32	(00FF24 D3)	ETM32	(00FF22 D3)
Clock timer 8 Hz	FTM8	(00FF24 D2)	ETM8	(00FF22 D2)
Clock timer 2 Hz	FTM2	(00FF24 D1)	ETM2	(00FF22 D1)
Clock timer 1 Hz	FTM1	(00FF24 D0)	ETM1	(00FF22 D0)
Remote controller	FREM	(00FF27 D5)	EREM	(00FF26 D5)

Table 5.15.4.1 Interrupt priority register

Interrupt	Interrupt priority register	
Programmable timer 0–1 interrupt	PPT0, PPT1	(00FF21 D2, D3)
Programmable timer 2–3 interrupt	PPT2, PPT3	(00FF21 D4, D5)
K10–K11 input interrupt	PK10, PK11	(00FF21 D0, D1)
K00–K07 input interrupt	PK00, PK01	(00FF20 D6, D7)
Serial interface interrupt	PSIF0, PSIF1	(00FF20 D4, D5)
Stopwatch timer interrupt	PSW0, PSW1	(00FF20 D2, D3)
Clock timer interrupt	PTM0, PTM1	(00FF20 D0, D1)
Remote controller interrupt	PREM0, PREM1	(00FF21 D6, D7)

At initial reset, the interrupt priority registers are all set to "0" and each interrupt is set to level 0. Furthermore, the priority levels in each system have been previously decided and they cannot be changed.
The CPU can mask each interrupt by setting the interrupt flags (I0 and I1). The relation between the interrupt priority level of each system and interrupt flags is shown in Table 5.15.4.3, and the CPU accepts only interrupts above the level indicated by the interrupt flags.
The $\overline{NMI}$ (watchdog timer) that has level 4 priority, is always accepted regardless of the setting of the interrupt flags.

Table 5.15.4.3 Interrupt mask setting of CPU

I1	I0	Acceptable interrupt
1	1	Level 4 ($\overline{NMI}$)
1	0	Level 4, Level 3 ($\overline{IRQ3}$)
0	1	Level 4, Level 3, Level 2 ($\overline{IRQ2}$)
0	0	Level 4, Level 3, Level 2, Level 1 ($\overline{IRQ1}$)

After an interrupt has been accepted, the interrupt flags are written to the level of that interrupt. However, interrupt flags after an $\overline{NMI}$ has been accepted are written to level 3 (I0 = I1 = "1").

Table 5.15.4.4 Interrupt flags after acceptance of interrupt

Accepted interrupt priority level		I1	I0
Level 4	($\overline{NMI}$)	1	1
Level 3	($\overline{IRQ3}$)	1	1
Level 2	($\overline{IRQ2}$)	1	0
Level 1	($\overline{IRQ1}$)	0	1

The set interrupt flags are reset to their original value on return from the interrupt processing routine. Consequently, multiple interrupts up to 3 levels can be controlled by the initial settings of the interrupt priority registers alone. Additional multiplexing can be realized by rewriting the interrupt flags and interrupt enable register in the interrupt processing routine.

Note: Beware. If the interrupt flags have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

5.15.5 Exception processing vectors

When the CPU accepts an interrupt request, it starts exception processing following completion of the instruction being executed. In exception processing, the following operations branch the program.

(1) In the minimum mode, the program counter (PC) and system condition flag (SC) are moved to stack and in the maximum mode, the code bank register (CB), PC and SC are moved.

(2) The branch destination address is read from the exception processing vector corresponding to each exception processing (interrupt) factor and is placed in the PC.

An exception vector is 2 bytes of data in which the top address of each exception (interrupt) processing routine has been stored and the vector addresses correspond to the exception processing factors as shown in Table 5.15.5.1.

Table 5.15.5.1 Vector address and exception processing correspondence

Vector address	Exception processing factor	Priority
000000H	Reset	High ↑
000002H	Zero division	
000004H	Watchdog timer ($\overline{NMI}$)	
000006H	Programmable timer 1 interrupt	
000008H	Programmable timer 0 interrupt	
00000AH	K10, K11 input interrupt	
00000CH	K04–K07 input interrupt	
00000EH	K00–K03 input interrupt	
000010H	Serial I/F error interrupt	
000012H	Serial I/F receiving complete interrupt	
000014H	Serial I/F transmitting complete interrupt	
000016H	Stopwatch timer 100 Hz interrupt	
000018H	Stopwatch timer 10 Hz interrupt	
00001AH	Stopwatch timer 1 Hz interrupt	
00001CH	Clock timer 32 Hz interrupt	
00001EH	Clock timer 8 Hz interrupt	
000020H	Clock timer 2 Hz interrupt	
000022H	Clock timer 1 Hz interrupt	
000024H	Remote-control carrier output interrupt	
000026H	Programmable timer 3 interrupt	↓
000028H	Programmable timer 2 interrupt	Low
00002AH	System reserved (cannot be used)	No priority rating
00002CH : 0000FEH	Software interrupt	

Note: An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the top portion of an exception processing routine must be described within the common area (000000H–007FFFH).

5.15.6 Control of interrupt

Table 5.15.6.1 shows the interrupt control bits.

Table 5.15.6.1(a) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF21	D7	PREM1	REM carrier interrupt priority register	PREM1 PREM0 PPT3 PPT2 PPT1 PPT0 PK11 PK10 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D6	PREM0				0	R/W	
	D5	PPT3	Programmable timer 2–3 interrupt priority register			0	R/W	
	D4	PPT2				0	R/W	
	D3	PPT1	Programmable timer 0–1 interrupt priority register			0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10–K11 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10–K11 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated / (W) Reset	(R) No interrupt factor is generated / (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag			0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated / (W) Reset	(R) No interrupt factor is generated / (W) No operation	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10–K11 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag			0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

Table 5.15.6.1(b) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF26	D7	EPT3	Programmable timer 3 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT2	Programmable timer 2 interrupt enable register			0	R/W	
	D5	EREM	REM carrier interrupt enable register			0	R/W	
	D4	REMC	REM carrier generation On/Off	On	Off	1	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF27	D7	FPT3	Programmable timer 3 interrupt factor flag	(R) Generated	(R) Not generated	0	R/W	
	D6	FPT2	Programmable timer 2 interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D5	FREM	REM carrier interrupt factor flag			0	R/W	
	D4	REMSO	Forced REM output On/Off	On	Off	0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

Refer to the explanations on the respective peripheral circuits for the setting content and control method for each bit.

5.15.7 Programming notes

(1) When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

(2) Beware. If the interrupt flags (I0 and I1) have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the front portion of an exception processing routine must be described within the common area (000000H–007FFFH).

(4) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

5.16 Notes for Low Current Consumption

The S1C88848 can turn circuits, which consume a large amount of power, ON or OFF by control registers.
You can reduce power consumption by creating a program that operates the minimum necessary circuits using these control registers.

Next, which circuit systems' operation can be controlled and their control registers (instructions) are explained. You should refer to these when programming.

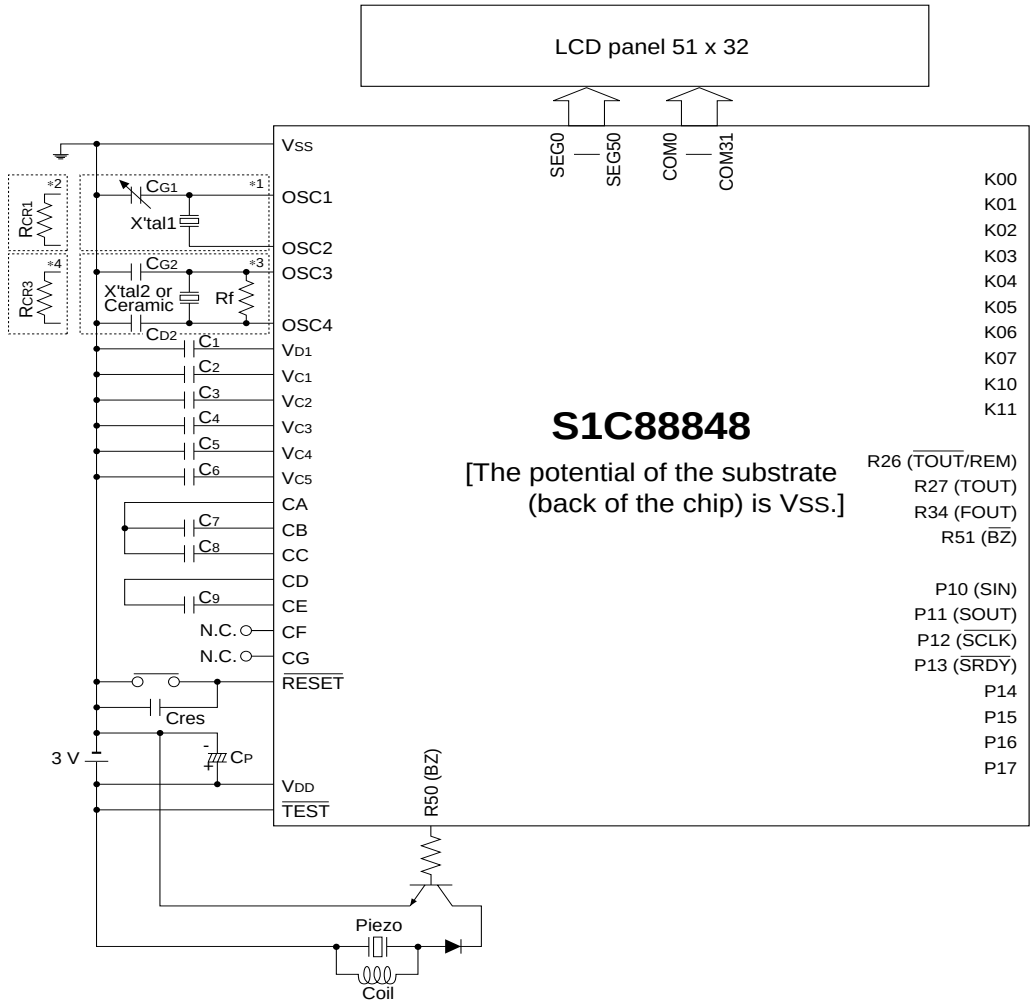
See Chapter 7, "ELECTRICAL CHARACTERISTICS" for the current consumption.

Table 5.16.1 Circuit systems and control registers

Circuit type	Control register (Instruction)	Status at time of initial resetting
CPU	HALT and SLP instructions	Operation status
Oscillation circuit	CLKCHG, OSCC	OSC3 clock (CLKCHG = "1") OSC3 oscillation ON (OSCC = "1")
LCD controller	LCDC0, LCDC1	Drive OFF (LCDC0 = LCDC1 = "0")
SVD circuit	SVDON	OFF status (SVDON = "0")
Remote controller	REMC	ON status (REMC = "1")

6 BASIC EXTERNAL WIRING DIAGRAM

● **When the piezoelectric buzzer is driven single terminal and LCD panel is used by 1/5 bias (V_{C2} standard)**



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.)=35 kΩ
C_{G1}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for CR oscillation	1 MΩ (50 kHz)
X'tal2	Crystal oscillator	4.9152 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
C_{D2}	Drain capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
R_{CR3}	Resistor for CR oscillation	50 kΩ (2 MHz)

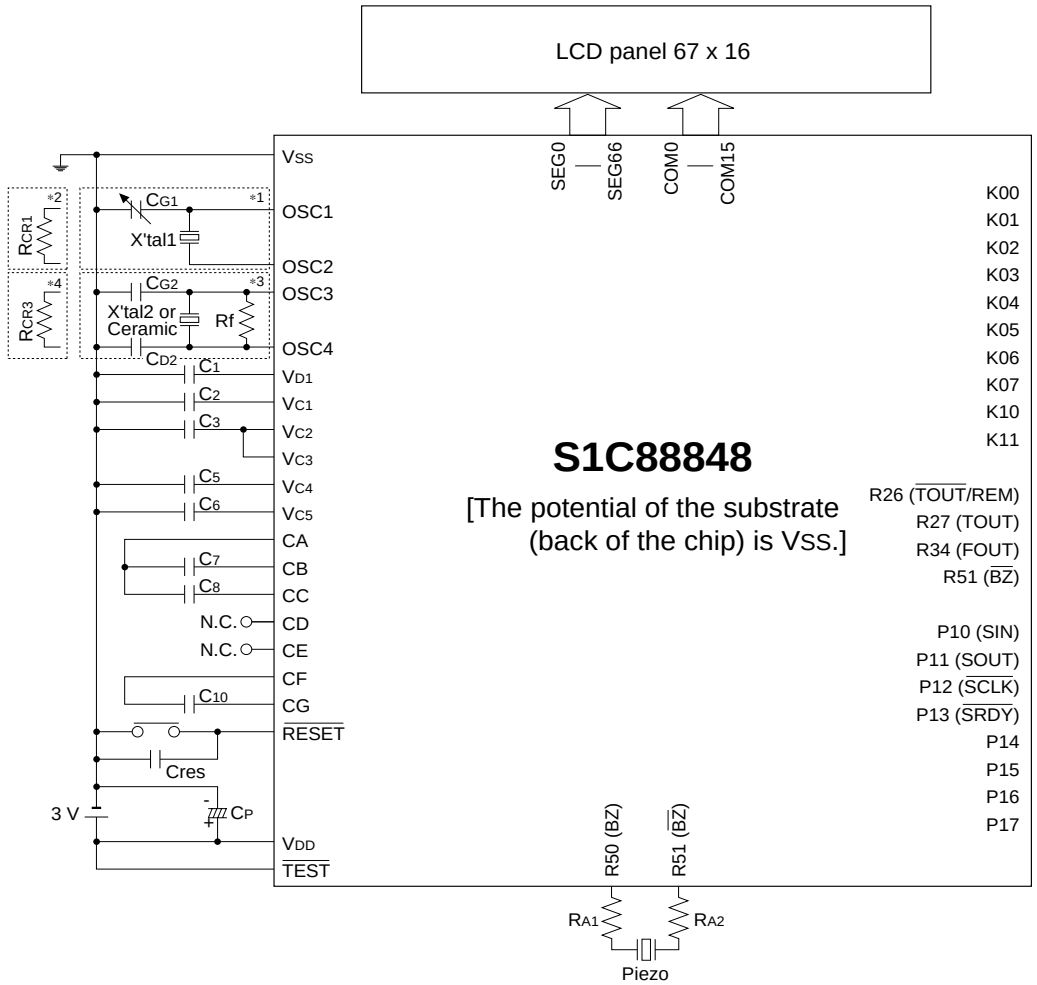
Symbol	Name	Recommended value
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_9	Booster/reducer capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

* The connection diagram shown above is an example of when mask option settings are as follows:
LCD power source: Internal power supply (1/5 bias), $\overline{RESET}$ terminal: With pull-up resistor,
R51 specification: General-purpose output port

∗1 OSC1 = Crystal oscillation, ∗2 OSC1 = CR oscillation, ∗3 OSC3 = Crystal/Ceramic oscillation, ∗4 OSC3 = CR oscillation

Note: The above table is simply an example. Refer to Chapter 7, "ELECTRICAL CHARACTERISTICS", for detailed characteristics.

● **When the piezoelectric buzzer is driven directl and LCD panel is used by 1/4 bias (V_{C1} standard)**



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.)=35 kΩ
C_{G1}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for CR oscillation	1 MΩ (50 kHz)
X'tal2	Crystal oscillator	4.9152 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
C_{D2}	Drain capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
R_{CR3}	Resistor for CR oscillation	50 kΩ (2 MHz)

Symbol	Name	Recommended value
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7	Booster/reducer capacitor	0.1 µF
C_8	Booster/reducer capacitor	0.1 µF
C_{10}	Booster/reducer capacitor	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF
R_{A1}, R_{A2}	Protection resistance	100 Ω

∗ The connection diagram shown above is an example of when mask option settings are as follows: LCD power source: Internal power supply (1/4 bias), $\overline{RESET}$ terminal: With pull-up resistor, R51 specification: $\overline{BZ}$ output port

∗1 OSC1 = Crystal oscillation, ∗2 OSC1 = CR oscillation, ∗3 OSC3 = Crystal / Ceramic oscillation, ∗4 OSC3 = CR oscillation

Note: The above table is simply an example. Refer to Chapter 7, "ELECTRICAL CHARACTERISTICS", for detailed characteristics.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +6.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +6.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	1
Operating temperature	Topr		-20 to +70	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	

Note) 1 In case of plastic package.

7.2 Recommended Operating Conditions

(V_{SS} = 0 V, Ta = -20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	V_{DD}		1.8		5.5	V	
Operating frequency	f_{OSC1}	V_{DD} = 1.8 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		8.2	MHz	
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			6.0	V	
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	1
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	1
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	1, 2
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	1
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	1
Capacitor between CA and CB	C_7			0.1		µF	1
Capacitor between CA and CC	C_8			0.1		µF	1
Capacitor between CD and CE	C_9			0.1		µF	1, 2
Capacitor between CF and CG	C_{10}			0.1		µF	1, 3

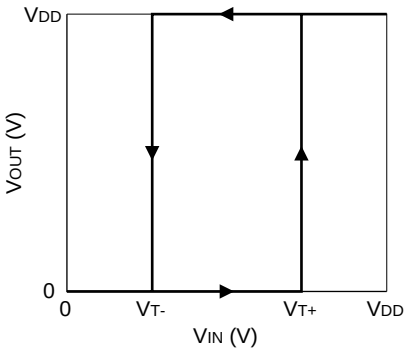
Note) 1 When LCD drive power is not used, the capacitor is not necessary.
In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.
2 When LCD drive power is used by 1/4 bias, the C_4 and C_9 capacitors are not necessary.
3 When LCD drive power is used by 1/5 bias, the C_{10} capacitor is not necessary.

7.3 DC Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Pxx		0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Pxx		0		0.2V_{DD}	V	
High level input voltage (2)	V_{IH2}	Kxx		0.4V_{DD}		0.9V_{DD}	V	
Low level input voltage (2)	V_{IL2}	Kxx		0.1V_{DD}		0.4V_{DD}	V	
High level schmitt input voltage	V_{T+}	$\overline{RESET}$		0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$		0.1V_{DD}		0.5V_{DD}	V	
High level output current (1)	I_{OH}	Pxx, Rxx, V_{OH} = 0.9V_{DD}				-0.5	mA	
Low level output current (1)	I_{OL}	Pxx, Rxx, V_{OL} = 0.1V_{DD}		0.5			mA	
High level output current (2)	I_{SEGOH}	SEG40–SEG50, V_{OH} = 0.9V_{DD}				-0.5	mA	1
Low level output current (2)	I_{SEGOL}	SEG40–SEG50, V_{OL} = 0.1V_{DD}		0.5			mA	1
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$		-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx		-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$	V_{DD} = 5.5 V	200	350	500	kΩ	2
			V_{DD} = 3.0 V	100	270	400	kΩ	2
			V_{DD} = 1.8 V	100	230	400	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN} = 0V, f = 1 MHz, Ta = 25°C			7	15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1 V				-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1 V		5			µA	

Note) 1 SEG40–SEG50 are configured for DC output by mask option.
2 When pull-up resistor is added by mask option.



7.4 Analog Circuit Characteristics

■ LCD drive circuit

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number, display pattern). Therefore, these should be evaluated by connecting to the actual panel to be used. See "7.8 Characteristics Curves" for the load characteristics.

• TYPE A

Unless otherwise specified: $V_{DD} = V_{C2}$ (LCX = FH) + 0.1 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_{10} = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C2}	When 1 MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)		0.38V_{C5}	0.405V_{C5}	0.43V_{C5}	V	
	V_{C5} TYPE A	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H	Typ×0.94	3.89	Typ×1.06	V	1
			LCX = 1H		3.96		V	
			LCX = 2H		4.04		V	
			LCX = 3H		4.11		V	
			LCX = 4H		4.18		V	
			LCX = 5H		4.26		V	
			LCX = 6H		4.34		V	
			LCX = 7H		4.42		V	
			LCX = 8H		4.50		V	
			LCX = 9H		4.58		V	
			LCX = AH		4.66		V	
			LCX = BH		4.74		V	
			LCX = CH		4.82		V	
			LCX = DH		4.90		V	
			LCX = EH		4.99		V	
			LCX = FH		5.08		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

• TYPE B

Unless otherwise specified: $V_{DD} = V_{C2}$ (LCX = FH) + 0.1 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_{10} = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C2}	When 1 MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)		0.38V_{C5}	0.405V_{C5}	0.43V_{C5}	V	
	V_{C5} TYPE B	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H	Typ×0.94	4.73	Typ×1.06	V	1
			LCX = 1H		4.83		V	
			LCX = 2H		4.92		V	
			LCX = 3H		5.02		V	
			LCX = 4H		5.11		V	
			LCX = 5H		5.21		V	
			LCX = 6H		5.30		V	
			LCX = 7H		5.40		V	
			LCX = 8H		5.50		V	
			LCX = 9H		5.60		V	
			LCX = AH		5.70		V	
			LCX = BH		5.70		V	
			LCX = CH		5.70		V	
			LCX = DH		5.70		V	
			LCX = EH		5.70		V	
			LCX = FH		5.70		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

• TYPE D

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_3, C_5–C_8, C_{10} = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	When 1 MΩ load resistor is connected between V_{SS} and V_{C1} (no panel load)		0.247V_{C5}	0.263V_{C5}	0.279V_{C5}	V	
	V_{C5} TYPE D	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H	Typ×0.94	3.80	Typ×1.06	V	1
			LCX = 1H		3.88		V	
			LCX = 2H		3.96		V	
			LCX = 3H		4.03		V	
			LCX = 4H		4.15		V	
			LCX = 5H		4.22		V	
			LCX = 6H		4.30		V	
			LCX = 7H		4.38		V	
			LCX = 8H		4.45		V	
			LCX = 9H		4.53		V	
			LCX = AH		4.65		V	
			LCX = BH		4.72		V	
			LCX = CH		4.80		V	
			LCX = DH		4.88		V	
			LCX = EH		4.95		V	
			LCX = FH		5.07		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

■ SVD circuit

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 0	Typ×0.92	1.83	Typ×1.08	V	
		Level 1		2.00		V	
		Level 2		2.17		V	
		Level 3		2.33		V	
		Level 4		2.50		V	
		Level 5		2.67		V	
		Level 6		2.83		V	
		Level 7		3.00		V	
		Level 8		3.17		V	
		Level 9		3.33		V	
		Level 10		3.50		V	
		Level 11		3.67		V	
		Level 12		3.83		V	
		Level 13		4.00		V	
		Level 14		4.17		V	
		Level 15		4.35		V	

7.5 Power Current Consumption

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, OSC1 = 32.768 kHz crystal oscillation, C_G = 25 pF, OSC3 = crystal/ceramic oscillation, C_1–C_{10} = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current	I_{DD1}	In SLEEP status *1		1.0	3.0	µA	
	I_{DD2}	In HALT status *2		1.7	4.0	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		4.0	7.0	µA	
	I_{DD4}	CPU is in operating (8 MHz) *4		0.7	0.9	mA	
LCD drive circuit current	I_{LCD1}	TYPE B. 1/16 duty, V_{DD} = 3.0 V		10.0	13.0	µA	1
	I_{LCD2}	TYPE D. 1/16 duty, V_{DD} = 3.0 V		7.0	10.0	µA	1
SVD circuit current	I_{SVDN}	V_{DD} = 3.0 V		5.0	10.0	µA	
OSC1 CR oscillation current	I_{CR1}	R_{CR1} = 1 MΩ (50 kHz)		5.0	20.0	µA	2

*1 OSC1: Stop, OSC3 = Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status

*2 OSC1: Oscillating, OSC3 = Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status

*3 OSC1: Oscillating, OSC3 = Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status

*4 OSC1: Oscillating, OSC3 = Oscillating, CPU, ROM, RAM: Operating in 8 MHz, Clock timer: Operating, Others: Stop status

See "7.8 Characteristics Curves" for current consumption with an operating frequency other than 8 MHz.

Note) 1 The LCD drive circuit current varies according to the display patterns.

2 When OSC1 CR oscillation circuit is selected by the mask option.

7.6 AC Characteristics

■ Operating range

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency	f_{OSC1}	V_{DD} = 1.8 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		8.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	25	61	67	µs	
		2-cycle instruction	50	122	133	µs	
		3-cycle instruction	75	183	200	µs	
		4-cycle instruction	100	244	267	µs	
		5-cycle instruction	125	305	333	µs	
		6-cycle instruction	150	366	400	µs	
Instruction execution time (during operation with OSC3 clock)	tcy	1-cycle instruction	0.2		66.7	µs	
		2-cycle instruction	0.5		133.3	µs	
		3-cycle instruction	0.7		200.0	µs	
		4-cycle instruction	1.0		266.7	µs	
		5-cycle instruction	1.2		333.3	µs	
		6-cycle instruction	1.5		400.0	µs	

■ Serial interface

• Clock synchronous master mode

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	ns	
Receiving data input set-up time	tsms	250			ns	
Receiving data input hold time	tsmh	100			ns	

• Clock synchronous slave mode

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	ns	
Receiving data input set-up time	tsss	100			ns	
Receiving data input hold time	tssh	100			ns	

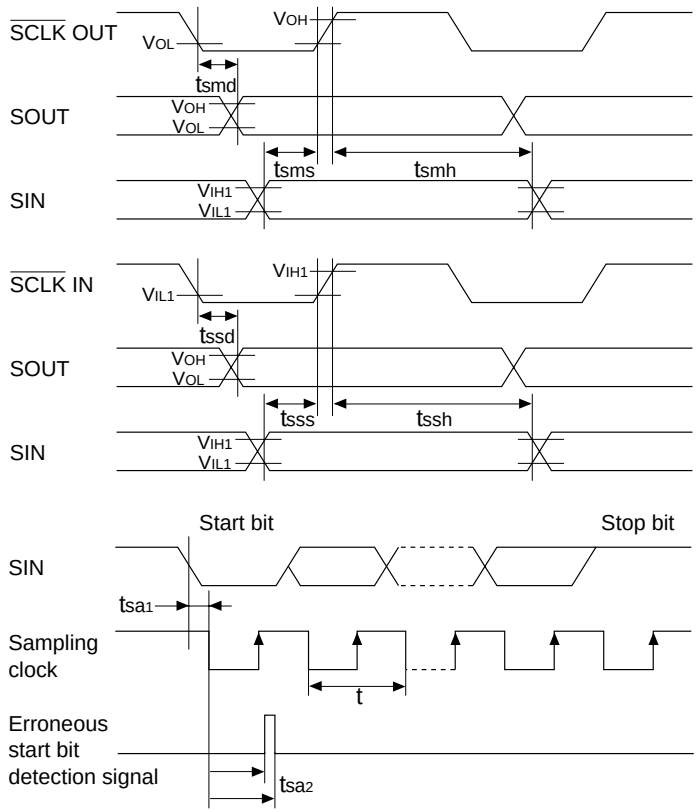
• Asynchronous system

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	s	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	s	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

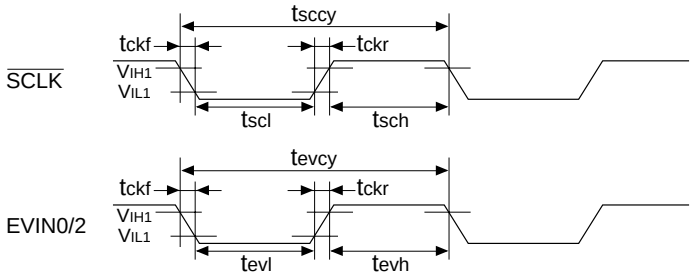


■ Input clock

• $\overline{\text{SCLK}}$, EVIN0/2 input clock

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

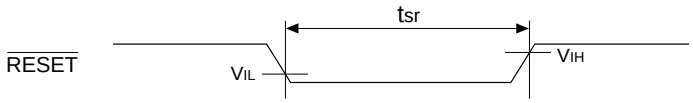
Item		Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	tsccy	2			µs	
	"H" pulse width	tsch	1			µs	
	"L" pulse width	tscl	1			µs	
EVIN0/2 input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			s	
	"H" pulse width	tevh	32 / f_{OSC1}			s	
	"L" pulse width	tevl	32 / f_{OSC1}			s	
EVIN0/2 input clock time (Without noise rejector)	Cycle time	tevcy	2			µs	
	"H" pulse width	tevh	1			µs	
	"L" pulse width	tevl	1			µs	
Input clock rising time		tckr			25	ns	
Input clock falling time		tckf			25	ns	



• $\overline{\text{RESET}}$ input clock

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C, V_{IH} = 0.5V_{DD}, V_{IL} = 0.1V_{DD}

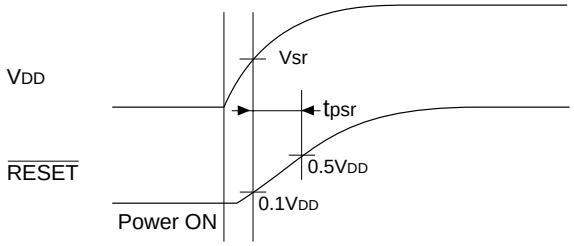
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µs	

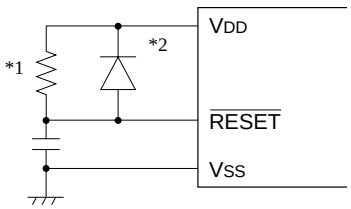


■ Power ON reset

Condition: VSS = 0 V, Ta = -20 to 70°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	1.8			V	
$\overline{\text{RESET}}$ input time	tpsr	10			ms	





*1 When the built-in pull up resistor is not used.

*2 Because the potential of the $\overline{\text{RESET}}$ terminal not reached VDD level or higher.

7.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

■ OSC1 (Crystal)

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, Crystal oscillator = Q12C2*, C_{G1} = 25 pF (external), C_{D1} = Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	s	
External gate capacitance	C_{G1}	Including board capacitance	5		25	pF	1
Built-in drain capacitance	C_{D1}	In case of the chip		12		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-15		15	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 5 to 25 pF	15			ppm	

* Q12C2 Made by Seiko Epson corporation

Note) 1 When crystal oscillation is selected by mask option.

■ OSC1 (CR)

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

■ OSC3 (Crystal)

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, Crystal oscillator = Q21CA301xxx*, R_F = 1 MΩ, C_{G2} = C_{D2} = 15 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta			15	50	ms	1

* Q21CA301xxx Made by Seiko Epson corporation

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

■ OSC3 (Ceramic)

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, Ceramic oscillator = CSA4.00MG / CSA8.00MTZ*, R_F = 1 MΩ, C_{G2} = C_{D2} = 30 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				1	ms	

* CSA4.00MG / CSA8.00MTZ Made by Murata Mfg. corporation

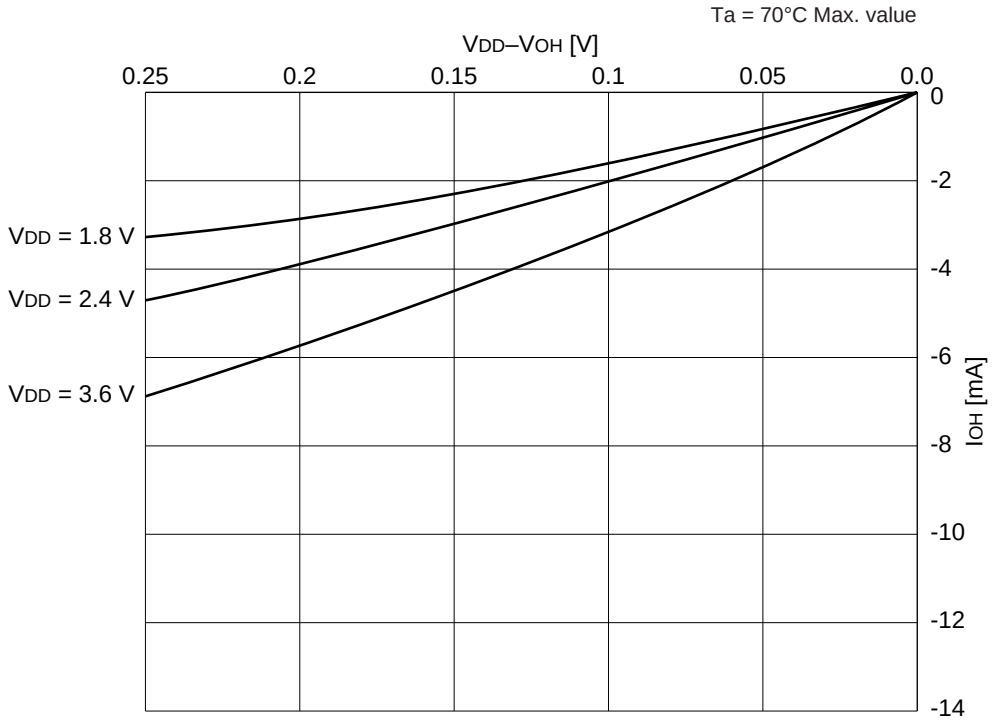
■ OSC3 (CR)

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -20 to 70°C

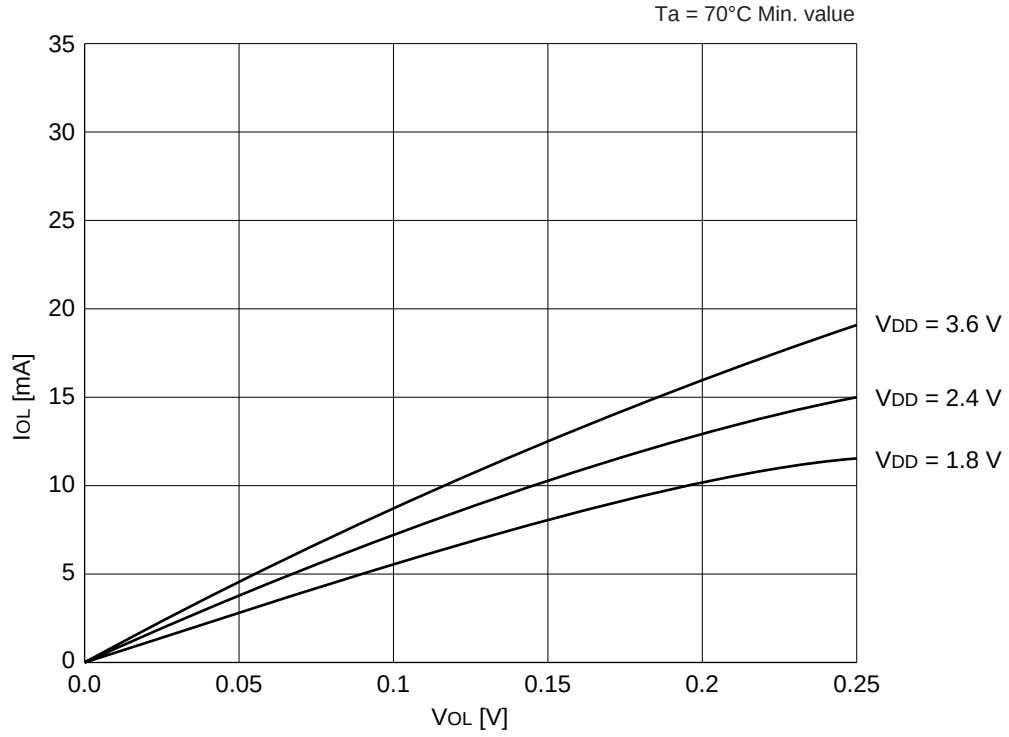
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

7.8 Characteristics Curves (reference value)

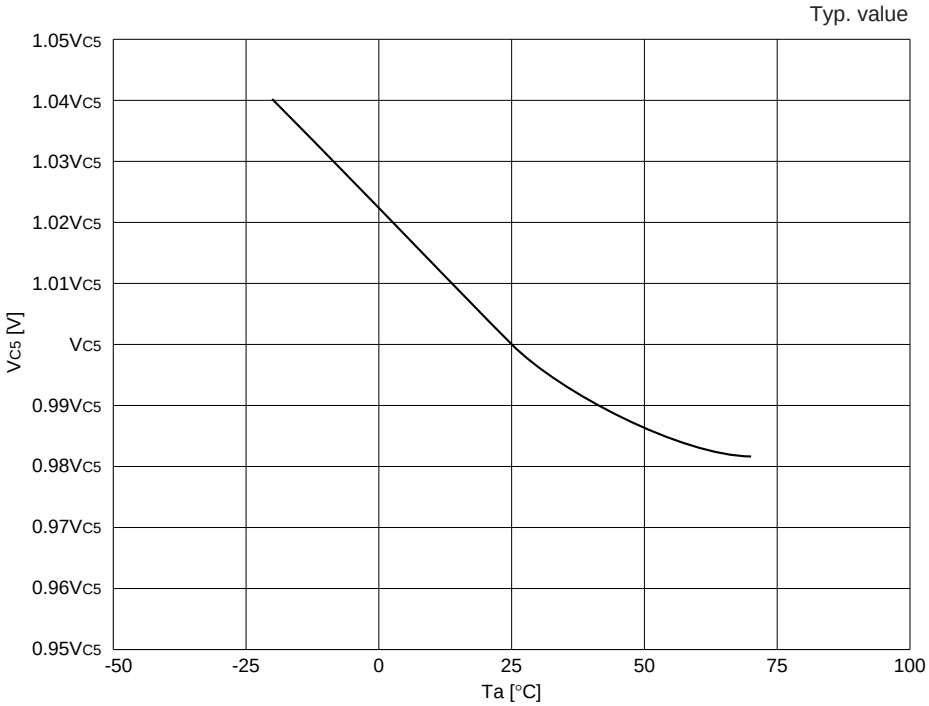
■ High level output current-voltage characteristic



■ Low level output current-voltage characteristic

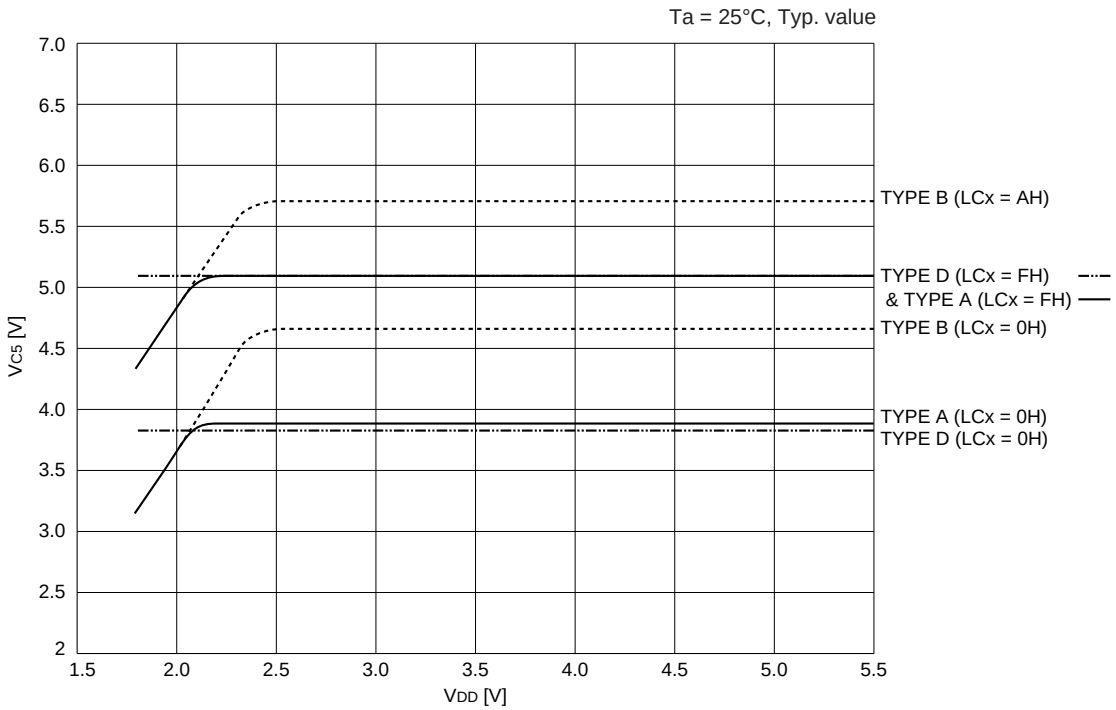


■ LCD drive voltage-ambient temperature characteristic

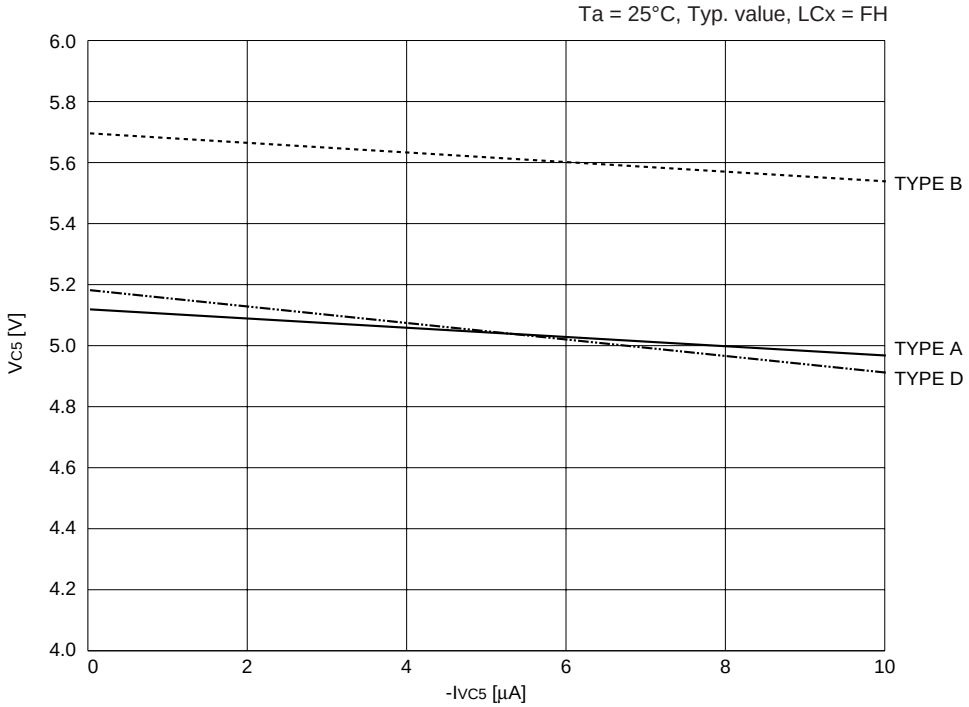


■ LCD drive voltage-supply voltage characteristic

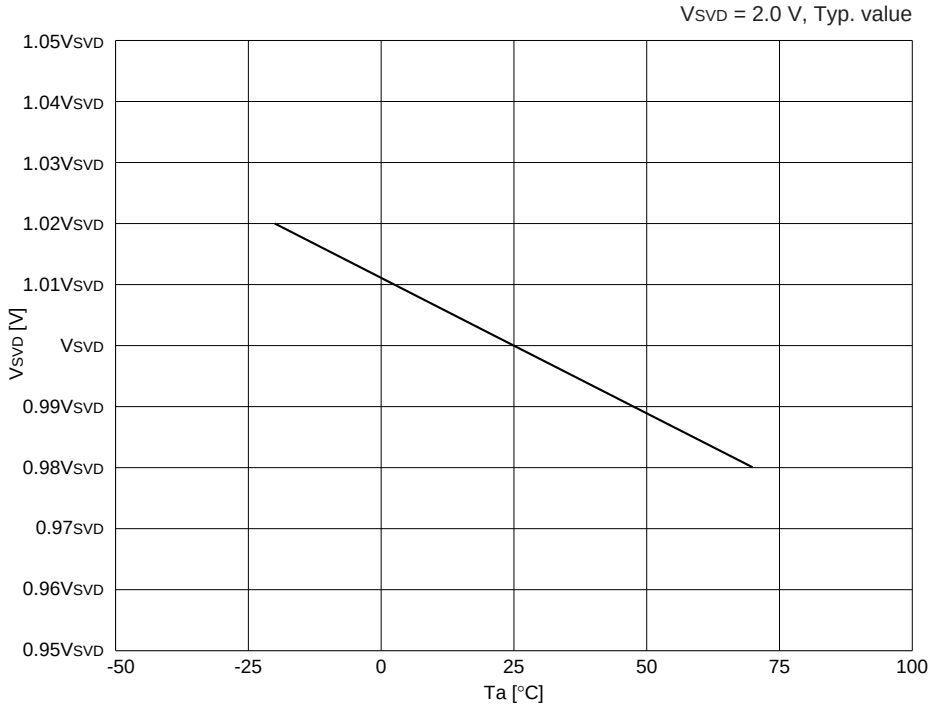
When 1 MΩ load resistor is connected between VSS and VC5 (no panel load)



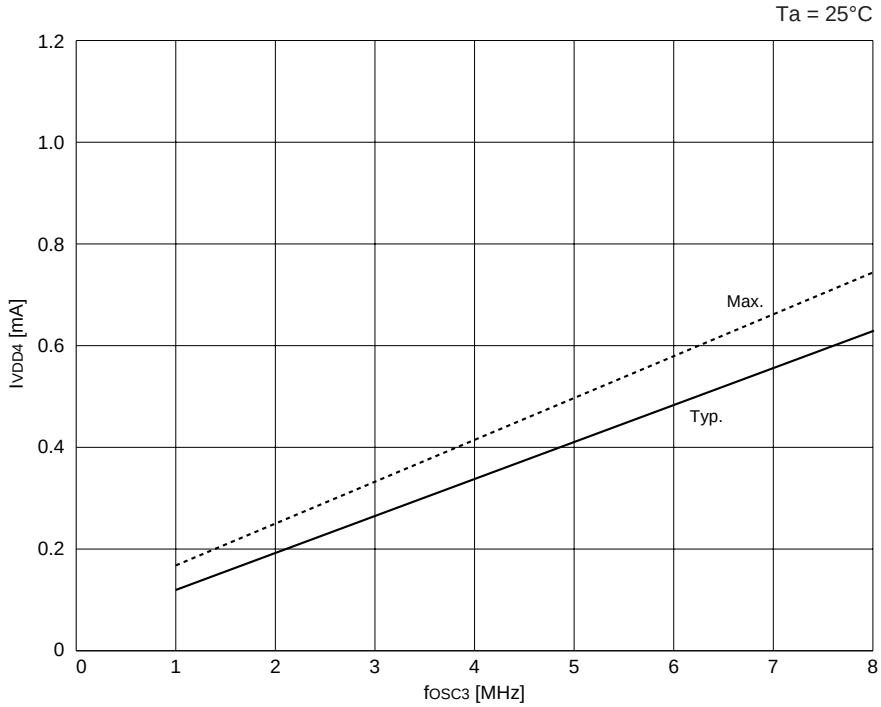
■ LCD drive voltage-load characteristic



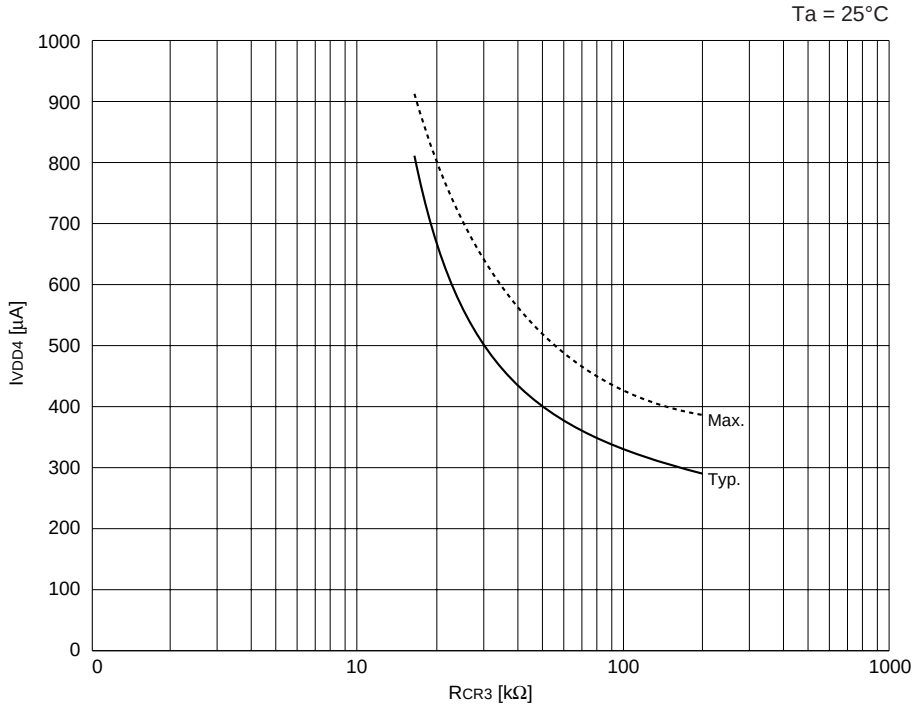
■ SVD voltage-ambient temperature characteristic



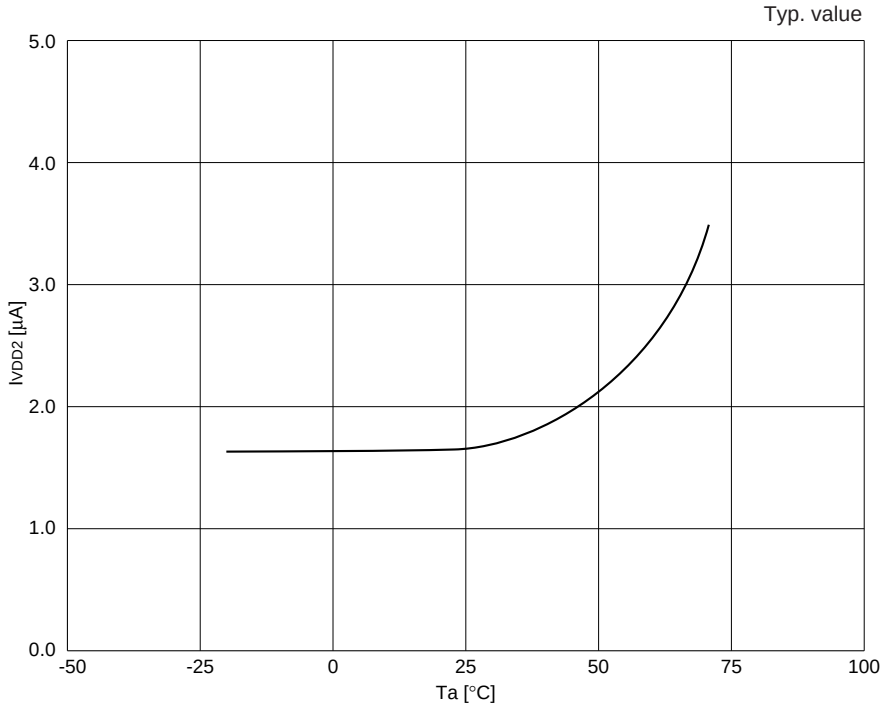
■ Power current (CPU is in operating) <OSC3 crystal/ceramic oscillation>



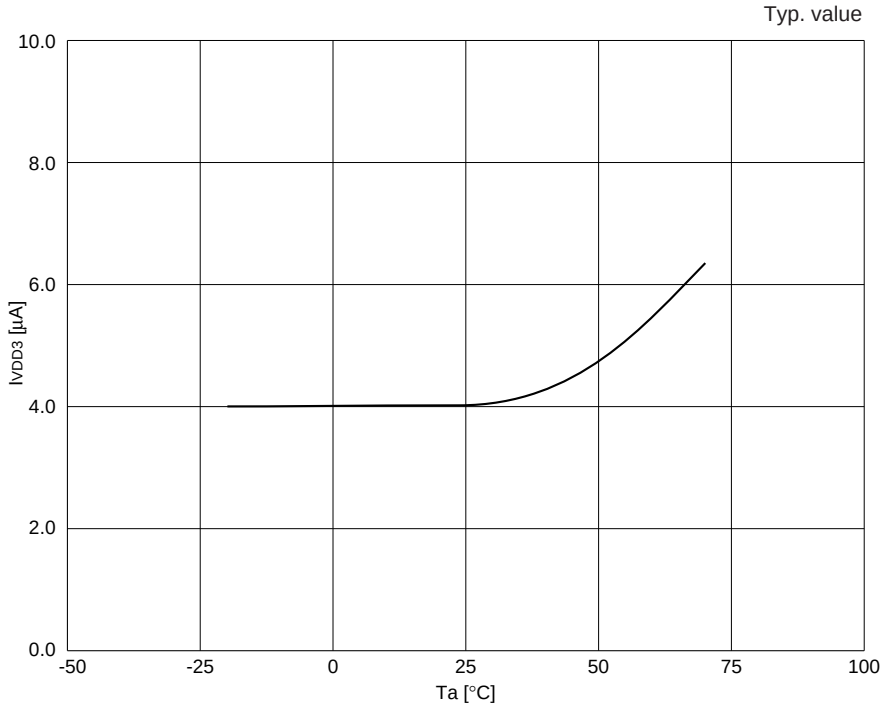
■ Power current (CPU is in operating) <OSC3 CR oscillation>



■ Power current-ambient temperature characteristic (In HALT status)



■ Power current-ambient temperature characteristic (CPU is under 32.768 kHz operation)

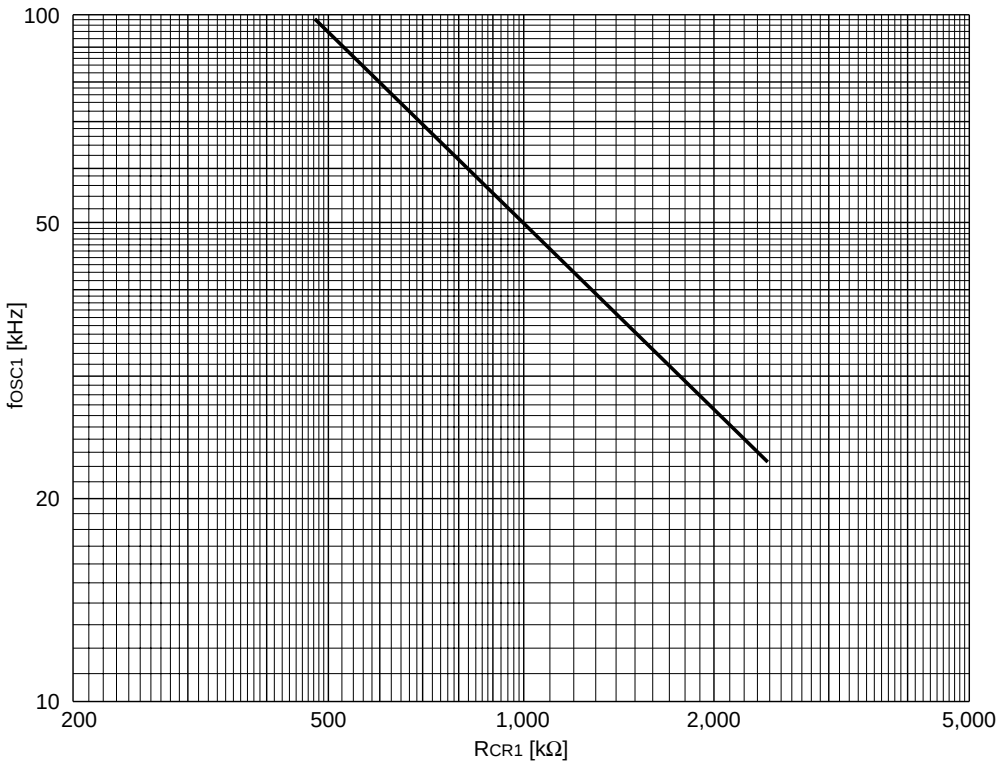


■ CR oscillation frequency characteristic

Note: Oscillation frequency changes depending on the conditions (components used, board pattern, etc.). In particular, the OSC3 oscillation frequency changes extensively depending on the product form (chip, plastic package or ceramic package) and board capacitance. Therefore, use the following charts for reference only and select the resistance value after evaluating the actual product. (The resistance value should be set to $R_{CR3} \geq 15$ kΩ.)

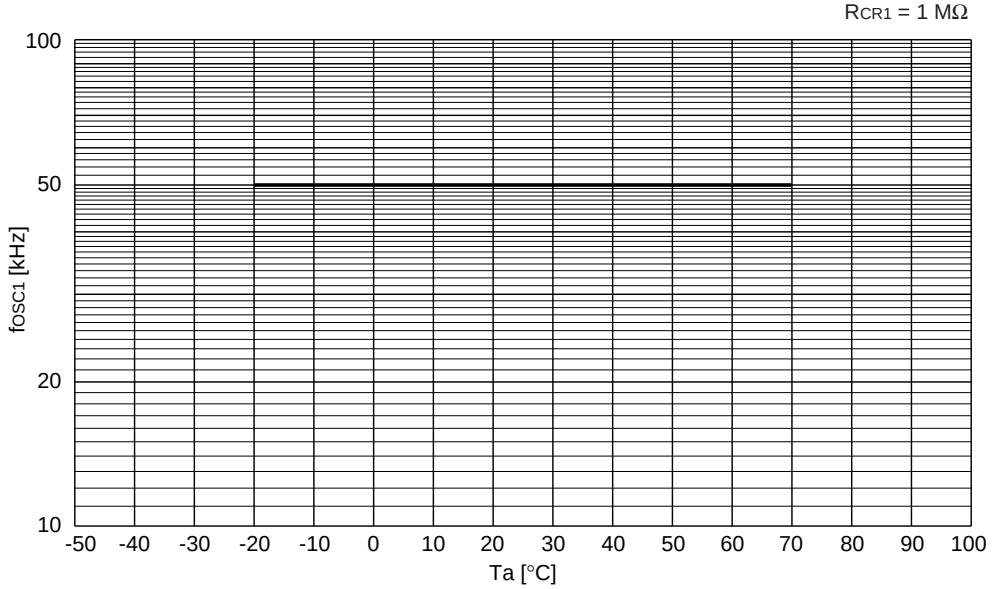
• Oscillation frequency resistor characteristic (OSC1)

Ta = 25°C, Typ. value



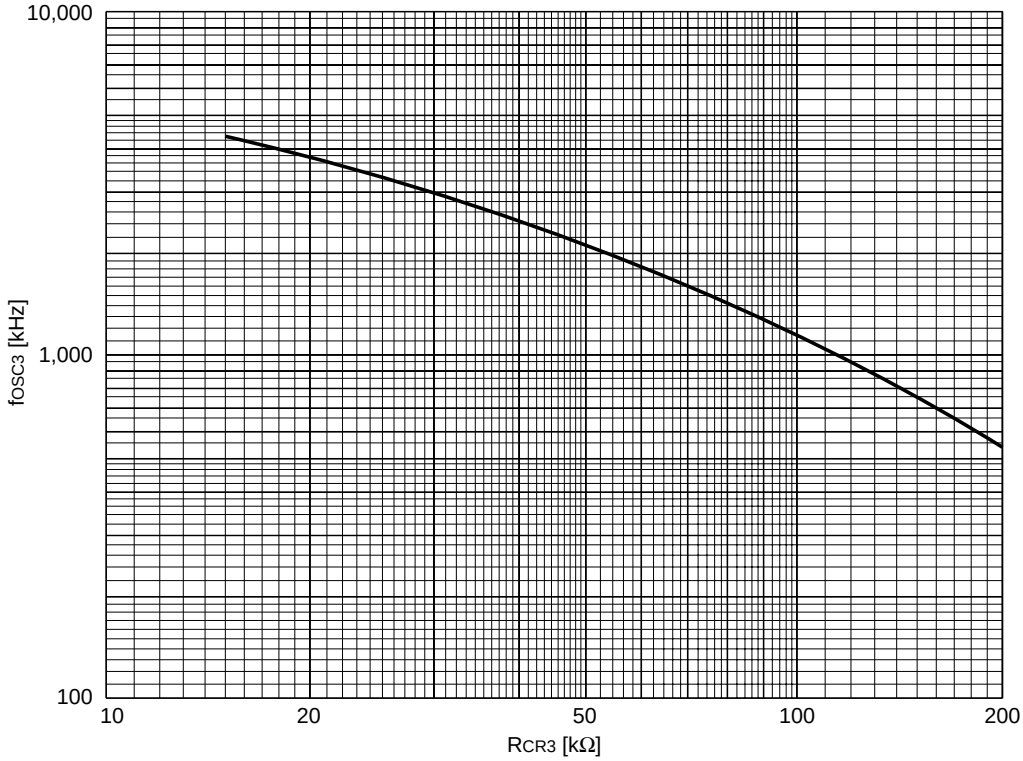
• Oscillation frequency temperature characteristic (OSC1)

R_{CR1} = 1 MΩ



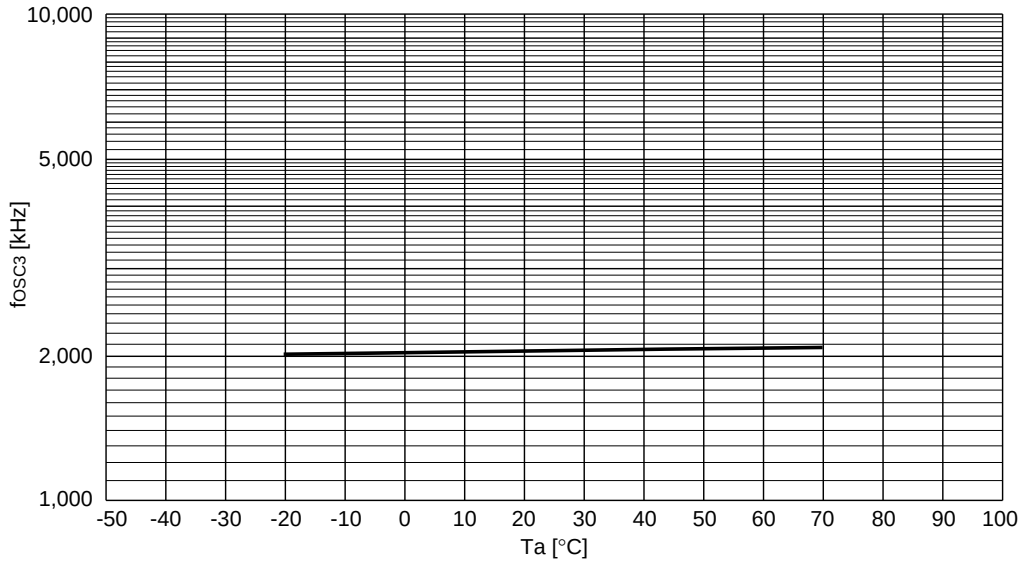
- **Oscillation frequency resistor characteristic (OSC3)**

Ta = 25°C, Typ. value



- **Oscillation frequency temperature characteristic (OSC3)**

RCR3 = 50 kΩ

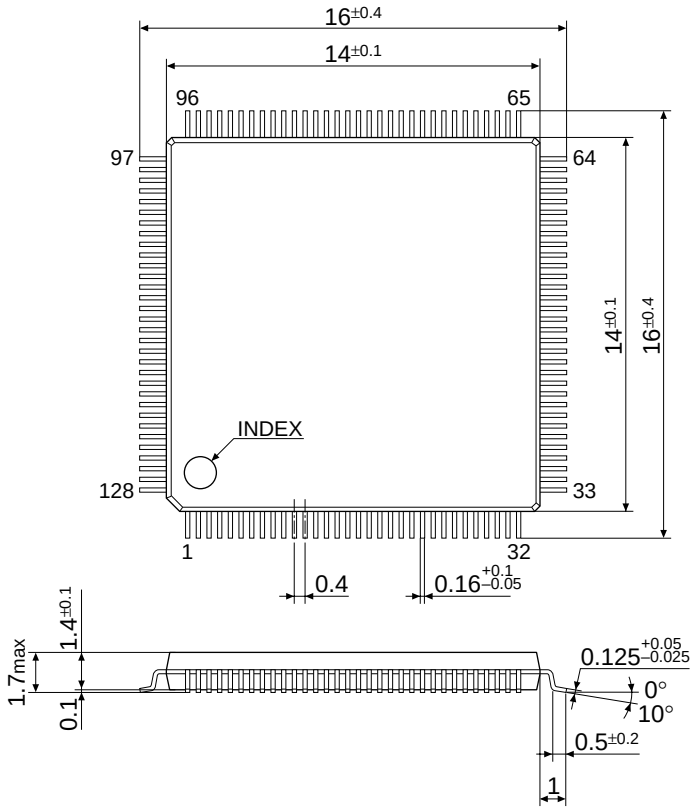


8 PACKAGE

8.1 Plastic Package

QFP15-128pin

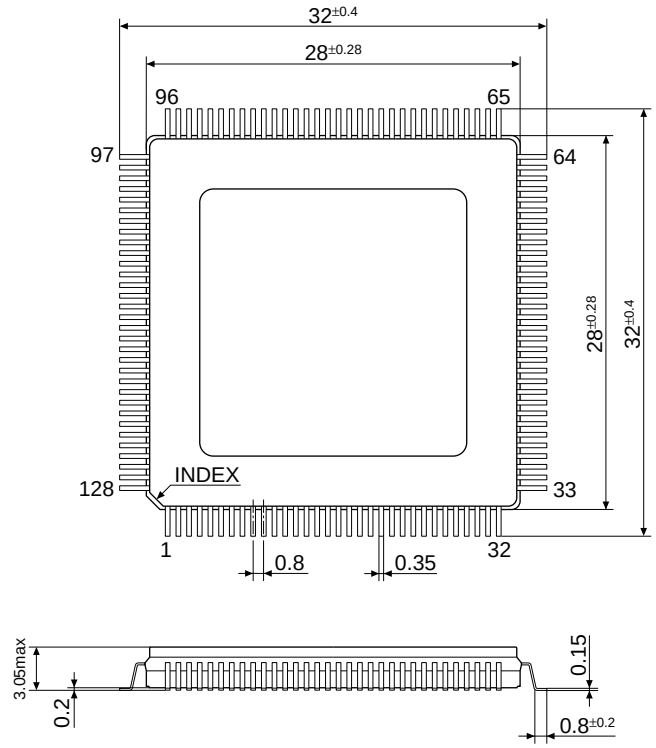
(Unit: mm)



8.2 Ceramic Package

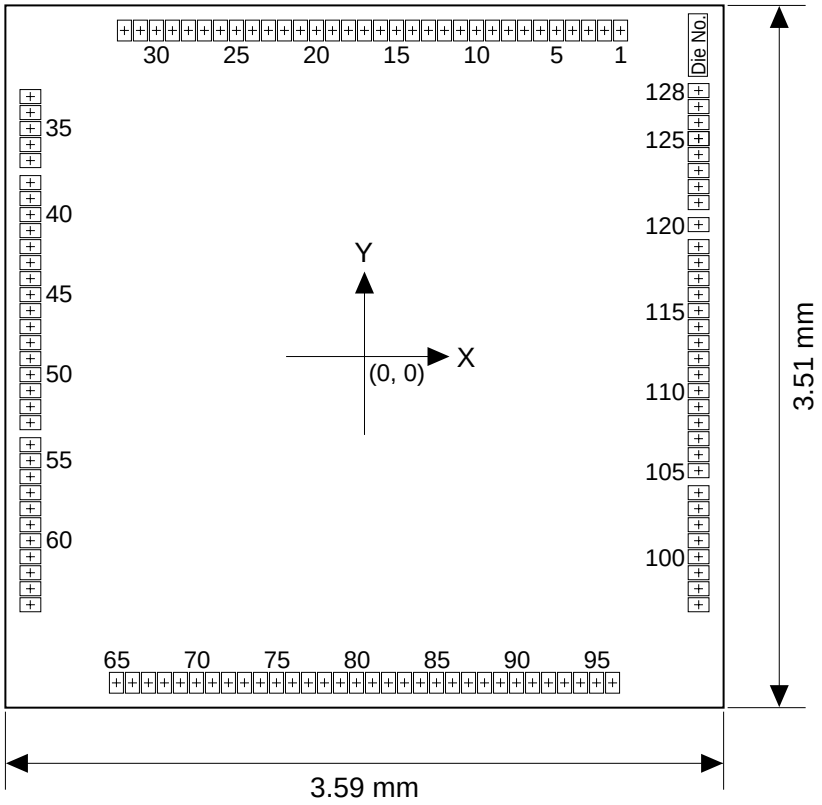
QFP8-128pin

(Unit: mm)



9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 70 × 104 µm

9.2 Pad Coordinates

Table 9.2.1 Pad coordinates (Unit: mm)

Pad		Dimensions		Pad		Dimensions		Pad		Dimensions	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	V_{C3}	1.28	1.63	44	COM6	-1.67	0.39	87	SEG33	0.52	-1.63
2	V_{C2}	1.20	1.63	45	COM7	-1.67	0.31	88	SEG34	0.60	-1.63
3	V_{C1}	1.12	1.63	46	COM8	-1.67	0.23	89	SEG35	0.68	-1.63
4	OSC3	1.04	1.63	47	COM9	-1.67	0.15	90	SEG36	0.76	-1.63
5	OSC4	0.96	1.63	48	COM10	-1.67	0.07	91	SEG37	0.84	-1.63
6	V_{D1}	0.88	1.63	49	COM11	-1.67	-0.01	92	SEG38	0.92	-1.63
7	V_{DD}	0.80	1.63	50	COM12	-1.67	-0.09	93	SEG39	1.00	-1.63
8	V_{SS}	0.72	1.63	51	COM13	-1.67	-0.17	94	SEG40	1.08	-1.63
9	OSC1	0.64	1.63	52	COM14	-1.67	-0.25	95	SEG41	1.16	-1.63
10	OSC2	0.56	1.63	53	COM15	-1.67	-0.33	96	SEG42	1.24	-1.63
11	$\overline{\text{TEST}}$	0.48	1.63	54	SEG0	-1.67	-0.44	97	SEG43	1.67	-1.24
12	$\overline{\text{RESET}}$	0.40	1.63	55	SEG1	-1.67	-0.52	98	SEG44	1.67	-1.16
13	K11/EVIN2	0.32	1.63	56	SEG2	-1.67	-0.60	99	SEG45	1.67	-1.08
14	K10/EVIN0	0.24	1.63	57	SEG3	-1.67	-0.68	100	SEG46	1.67	-1.00
15	K07	0.16	1.63	58	SEG4	-1.67	-0.76	101	SEG47	1.67	-0.92
16	K06	0.08	1.63	59	SEG5	-1.67	-0.84	102	SEG48	1.67	-0.84
17	K05	0.00	1.63	60	SEG6	-1.67	-0.92	103	SEG49	1.67	-0.76
18	K04	-0.08	1.63	61	SEG7	-1.67	-1.00	104	SEG50	1.67	-0.68
19	K03	-0.16	1.63	62	SEG8	-1.67	-1.08	105	COM31/SEG51	1.67	-0.57
20	K02	-0.24	1.63	63	SEG9	-1.67	-1.16	106	COM30/SEG52	1.67	-0.49
21	K01	-0.32	1.63	64	SEG10	-1.67	-1.24	107	COM29/SEG53	1.67	-0.41
22	K00	-0.40	1.63	65	SEG11	-1.24	-1.63	108	COM28/SEG54	1.67	-0.33
23	P17	-0.48	1.63	66	SEG12	-1.16	-1.63	109	COM27/SEG55	1.67	-0.25
24	P16	-0.56	1.63	67	SEG13	-1.08	-1.63	110	COM26/SEG56	1.67	-0.17
25	P15	-0.64	1.63	68	SEG14	-1.00	-1.63	111	COM25/SEG57	1.67	-0.09
26	P14	-0.72	1.63	69	SEG15	-0.92	-1.63	112	COM24/SEG58	1.67	-0.01
27	P13/$\overline{\text{SRDY}}$	-0.80	1.63	70	SEG16	-0.84	-1.63	113	COM23/SEG59	1.67	0.07
28	P12/$\overline{\text{SCLK}}$	-0.88	1.63	71	SEG17	-0.76	-1.63	114	COM22/SEG60	1.67	0.15
29	P11/SOUT	-0.96	1.63	72	SEG18	-0.68	-1.63	115	COM21/SEG61	1.67	0.23
30	P10/SIN	-1.04	1.63	73	SEG19	-0.60	-1.63	116	COM20/SEG62	1.67	0.31
31	CF	-1.12	1.63	74	SEG20	-0.52	-1.63	117	COM19/SEG63	1.67	0.39
32	CG	-1.20	1.63	75	SEG21	-0.44	-1.63	118	COM18/SEG64	1.67	0.47
33	R26/$\overline{\text{TOUT}}$/REM	-1.67	1.30	76	SEG22	-0.36	-1.63	119	COM17/SEG65	1.67	0.55
34	R27/TOUT	-1.67	1.22	77	SEG23	-0.28	-1.63	120	COM16/SEG66	1.67	0.66
35	R34/FOUT	-1.67	1.14	78	SEG24	-0.20	-1.63	121	N.C.	1.67	0.77
36	R50/BZ	-1.67	1.06	79	SEG25	-0.12	-1.63	122	CE	1.67	0.85
37	R51/$\overline{\text{BZ}}$	-1.67	0.98	80	SEG26	-0.04	-1.63	123	CD	1.67	0.93
38	COM0	-1.67	0.87	81	SEG27	0.04	-1.63	124	CC	1.67	1.01
39	COM1	-1.67	0.79	82	SEG28	0.12	-1.63	125	CB	1.67	1.09
40	COM2	-1.67	0.71	83	SEG29	0.20	-1.63	126	CA	1.67	1.17
41	COM3	-1.67	0.63	84	SEG30	0.28	-1.63	127	V_{C5}	1.67	1.25
42	COM4	-1.67	0.55	85	SEG31	0.36	-1.63	128	V_{C4}	1.67	1.33
43	COM5	-1.67	0.47	86	SEG32	0.44	-1.63	–	–	–	–

10 PRECAUTIONS ON MOUNTING

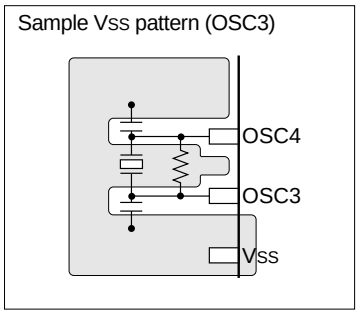
<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3, OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3, OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



  (3) When supplying an external clock to the OSC1 (OSC3) terminal, the clock source should be connected to the OSC1 (OSC3) terminal in the shortest line.
  Furthermore, do not connect anything else to the OSC2 (OSC4) terminal.

- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 (OSC3) and VDD, please keep enough distance between OSC1 (OSC3) and VDD or other signals on the board pattern.

<Reset Circuit>

- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor is added to the $\overline{\text{RESET}}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.

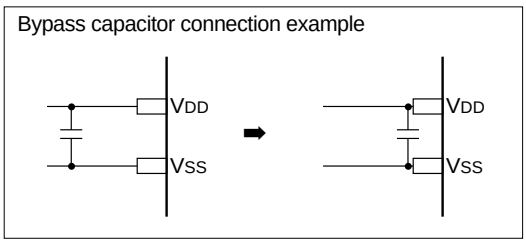
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminals with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



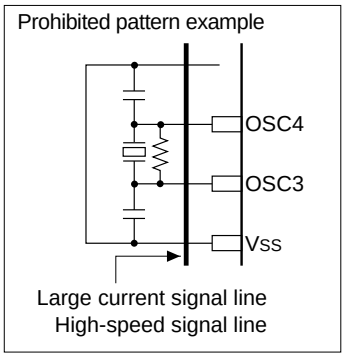
  (3) Components which are connected to the VD1, VC1–VC5 and CA–CG terminals, such as capacitors, should be connected in the shortest line.
  In particular, the VC1–VC5 voltages affect the display quality.

- Do not connect anything to the VC1–VC5 and CA–CG terminals when the LCD driver is not used.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.

- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

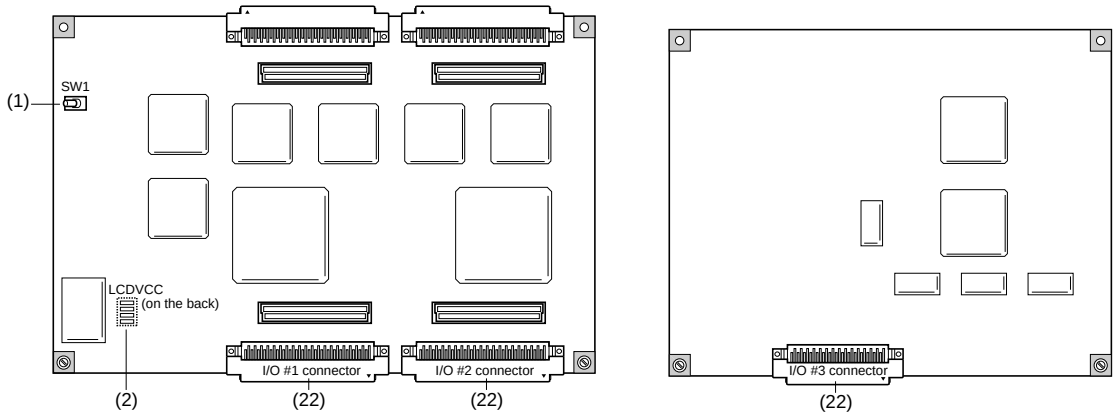
  (3) As well as the face of the IC, shield the back and side too.

APPENDIX A S5U1C88000P1&S5U1C88816P2 MANUAL (Peripheral Circuit Board for S1C88848)

This manual describes how to use the Peripheral Circuit Board for S1C88848 (S5U1C88000P1&S5U1C88816P2). This circuit board is used to provide emulation functions when it is installed in the ICE (S5U1C88000H5), a debugging tool for the 8-bit Single Chip Microcomputer S1C88 Family.
The explanation assumes that the S1C88848 circuit data has been downloaded into the S1C88 Family Peripheral Circuit Board (S5U1C88000P1).
Refer to the "S5U1C88000P Manual" for how to download circuit data into the S1C88 Family Peripheral Circuit Board (S5U1C88000P1) and common specifications of the board. For details on ICE functions and how to operate the debugger, refer to the separately prepared manuals.

A.1 Names and Functions of Each Part

The following explains the names and functions of each part of the S5U1C88000P1&S5U1C88816P2.



Main board (S5U1C88000P1) *Add-on board (S5U1C88816P2)*

Fig. A.1.1 Board layout

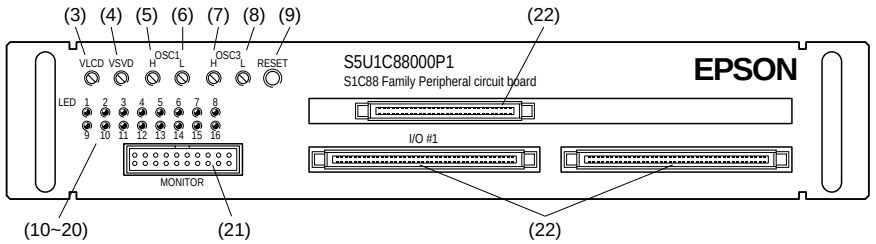


Fig. A.1.2 Panel layout (S5U1C88000P1)

(1) SW1
When downloading circuit data, set this switch to the "3" position. Otherwise, set to position "1".

(2) LCDVCC (on the back of the S5U1C88000P1 board)
The internal power voltage (V_{C5}) for the LCD driver can be varied using the DIP switch as shown in Table A.1.1. Be aware that the V_{C5} voltage level on this board is different from that of the actual IC.

(3) VLCD control
Unused.

(4) VSVD control
This control is used for varying the power supply voltage to confirm the supply voltage detection (SVD) function. (Refer to Section A.2.2, "Differences from Actual IC".)

Table A.1.1 Setting LCDVCC

LCDVCC				Setting
1	2	3	4	
ON	OFF	OFF	ON	V_{C5} = 6 V
OFF	ON	OFF	OFF	V_{C5} = 5.75 V
OFF	OFF	ON	OFF	V_{C5} = 5.5 V
OFF	OFF	OFF	ON	V_{C5} = 5 V
Other combinations				Not allowed

* The voltage value assumes that the LCD contrast adjustment register LC0–LC3 is 0FH. There is a need to allow for a maximum ±6% of error due to the characteristics of the parts used on this board.

(5) OSC1 H control
This control is used for coarse adjustment of the OSC1 CR oscillation frequency.

(6) OSC1 L control
This control is used for fine adjustment of the OSC1 CR oscillation frequency.

(7) OSC3 H control
This control is used for coarse adjustment of the OSC3 CR oscillation frequency.

(8) OSC3 L control
This control is used for fine adjustment of the OSC3 CR oscillation frequency.

(9) RESET switch
This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(10) LEDs 1 to 3 (Reserved)
Unused.

(11) LED 4 (CLKCHG)
Indicates the CPU operating clock.
Lit: OSC3 (CLKCHG register = "1")
Not lit: OSC1 (CLKCHG register = "0")

(12) LED 5 (OSCC)
Indicates the OSC3 oscillation status.
Lit: OSC3 oscillation is on (OSCC register = "1")
Not lit: OSC3 oscillation is off (OSCC register = "0")

(13) LED 6 (SVDON)
Indicates the SVD circuit status.
Lit: SVD circuit is on (SVDON register = "1")
Not lit: SVD circuit is off (SVDON register = "0")

(14) LED 7 (LCDC)
Indicates the LCD circuit status.
Lit: LCD circuit is on (LCDC register = Not "00")
Not lit: LCD circuit is off (LCDC register = "00")

(15) LED 8 (Reserved)
Unused.

(16) LED 9 (HALT/SLEEP)
Indicates the CPU status.
Lit: HALT or SLEEP
Not lit: RUN

(17) LED 10 (OSC1 operating clock)
The OSC1 operating clock is connected to this LED. The corresponding monitor pin (pin 10) can be used to check the OSC1 clock frequency.

(18) LED 11 (OSC3 operating clock)
The OSC3 operating clock is connected to this LED. The corresponding monitor pin (pin 11) can be used to check the OSC3 clock frequency.

(19) LEDs 12 to 15 (Reserved)
Unused.

(20) LED 16 (FPGA configuration)
If the FPGA on the S5U1C88000P1 includes circuit data, this LED lights when the power is turned on. If this LED does not light at power-up, a circuit data must be written to the FPGA before debugging can be started (turn the power on again after writing data).

(21) LED signal monitor connector
This connector provides the signals that drive the LEDs shown above for monitoring. The signals listed below are output from the connector pins. The signal level is high when the LED is lit and is low when the LED is not lit.

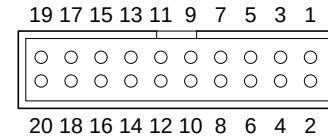


Fig. A.1.3 LED signal monitor connector

Pin 4: LED 4 (CPU operating clock)
Pin 5: LED 5 (OSC3 oscillation status)
Pin 6: LED 6 (SVD circuit status)
Pin 7: LED 7 (LCD circuit status)
Pin 9: LED 9 (HALT/SLEEP, RUN status)
Pin 10: OSC1 operating clock
Pin 11: OSC3 operating clock

Pin 18: OSC1 CR oscillation frequency monitor pin
Pin 19: OSC3 CR oscillation frequency monitor pin

Pins 1 to 3, 8, 12 to 17 and 20 are not used.
The OSC3 CR oscillation clock is connected to pins 18 and 19. (The CR oscillation circuit on this board always operates even if crystal oscillation is selected by mask option and regardless of the OSCC register status.) These pins can be used to monitor CR oscillation when adjusting the oscillation frequency.

(22) I/O #1, I/O #2, I/O #3 connectors
These are the connectors for connecting the I/O and LCD. The I/O cables (80-pin/40-pin × 2 flat type, 60-pin/30-pin × 2 flat type) are used to connect to the target system.

A.2 Precautions

Take the following precautions when using the S5U1C88000P1&S5U1C88816P2.

A.2.1 Precaution for operation

(1) Turn the power of all equipment off before connecting or disconnecting cables.

(2) Make sure that the input ports (K00–K03) are not all set to low when turning the power on until the mask option data is loaded, as the key-entry reset function may activated.

(3) The mask option data must be loaded before debugging can be started.

A.2.2 Differences from actual IC

Caution is called for due to the following function and property related differences with the actual IC. If these precautions are overlooked, it may not operate on the actual IC, even if it operates on the ICE in which the S5U1C88000P1&S5U1C88816P2 has been installed.

(1) I/O differences

Interface power voltage

This board and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter or similar circuit on the target system side to accommodate the required interface voltage.

Drive capability of each output port

The drive capability of each output port on this board is higher than that of the actual IC. When designing the application system and software, refer to Chapter 7, "ELECTRICAL CHARACTERISTICS" to confirm the drive capability of each output port.

Input port characteristics

The AC characteristic of the input terminal is different from that of the actual IC and it affects the input interrupt function. Therefore, evaluate the operation in the actual IC if the rise/fall time of the input signal is long.

Protective diode of each port

All I/O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between this board and the target system are set to +3.3 V. Therefore, this board and the target system cannot be interfaced with a voltage exceeding V_{DD} even if the output ports are configured with open-drain output.

Pull-up resistance value

The pull-up resistance values on this board are set to 300 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "ELECTRICAL CHARACTERISTICS".

Note that when using pull-up resistors to pull the input terminals high, the input terminals may require a certain period to reach a valid high level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since rise delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by this board differs significantly from that of the actual IC. Inspecting the LEDs on the S5U1C88000P1 front panel may help keep track of approximate current consumption. The following factors / components greatly affect device current consumption:

Those which can be verified by LEDs and monitor pins

a) Run and Halt execution ratio
(verified by LEDs and monitor pins on the ICE)
b) CPU operating clock change control
(LED 4: monitor pin 4)
c) OSC3 oscillation on / off control
(LED 5: monitor pin 5)
d) SVD circuit on / off control
(LED 6: monitor pin 6)
e) LCD power supply control
(LED 7: monitor pin 7)
f) SLEEP and Halt execution ratio
(LED 9: monitor pin 9)
g) OSC1 operating clock
(LED 10: monitor pin 10)
h) OSC3 operating clock
(LED 11: monitor pin 11)

Those that can only be counteracted by system or software

i) Current consumed by the internal pull-up resistors
j) Input ports in a floating state

The S1C88848 does not support a heavy load protection function. Therefore, current consumption of the S1C88848 does not change if LED8 is lit to indicate that the IC is in heavy load protection mode.

(3) Functional precautions

LCD circuit

- Pay attention to the output drive capability and output voltage of the LCD terminals (SEG, COM), since they are different from those of the actual IC. The system and the software should be designed in order to adjust the LCD contrast. The S5U1C88000P1 board allows switching of the LCD drive voltage with its switch on the back side. (Refer to Section A.1, "Names and Functions of Each Part")
- When the LCDC0 and LCDC1 registers are both set to "0" (LCD power control circuit is off), the SEG and COM terminal outputs of the actual IC are fixed at V_{SS} level. Note, however, that the COM outputs are fixed at V_{C4} level and the SEG outputs are fixed at V_{C3} (= V_{C2}) level in this board.

SVD circuit

- The SVD function is realized by artificially varying the power supply voltage using the VSVD control on the front panel of the S5U1C88000P1.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. The delay time on this board differs from that of the actual IC. Refer to Chapter 7, "ELECTRICAL CHARACTERISTICS" when setting the appropriate wait time for the actual IC.

Oscillation circuit

- The OSC1 crystal oscillation frequency is fixed at 32.768 kHz.
- The OSC1 CR oscillation frequency can be adjusted in the range of approx. 20 kHz to 500 kHz using the control on the S5U1C88000P1 front panel. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "ELECTRICAL CHARACTERISTICS" to select the appropriate operating frequency.
- The OSC3 crystal oscillation frequency is fixed at 4.9152 MHz.
- The OSC3 CR oscillation frequency can be adjusted in the range of approx. 100 kHz to 8 MHz using the control on the S5U1C88000P1 front panel. Note that the actual IC does not operate with all of these frequencies; refer to Chapter 7, "ELECTRICAL CHARACTERISTICS" to select the appropriate operating frequency.
- The S5U1C88000P1&S5U1C88816P2 does not include the OSC3 ceramic oscillation circuit. When ceramic oscillation circuit is selected by mask option, the S5U1C88816P2 uses the on-board crystal oscillation circuit.

- When using an external clock, adjust the external clock (amplitude: 3.3 V ±5%, duty: 50% ±10%) and input to the OSC1 or OSC3 terminal with VSS as GND.
- This board can operate normally even when the CPU clock is switched to OSC3 (CLKCHG = "1") immediately after the OSC3 oscillation control circuit is turned on (OSCC = "1") without a wait time inserted. In the actual IC, an oscillation stability wait time is required before switching the CPU clock after the OSC3 oscillation is turned on. Refer to Chapter 7, "ELECTRICAL CHARACTERISTICS" when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with this board, may not function properly with the actual IC.
- This board contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, this board can operate with the OSC3 circuit.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on this board differs from that of theactual IC.

Access to undefined address space

If any undefined space in the S1C88848's internal ROM/RAM or I/O is accessed for data read or write operations, the read/written value is indeterminate. Additionally, it is important to remain aware that the indeterminate state differs between this board and the actual IC.

Reset circuit

Keep in mind that the operation sequence from when the ICE with this board installed is powered on until the time at which the program starts running differs from the sequence of the actual IC. This is because this board becomes capable of operating as a debugging system after the user program and optional data are downloaded.

Internal power supply circuit

The LCD drive voltage on this board is different from that on the actual IC.

(4) Notes on model support

Parameter file

The ROM, RAM and I/O spaces in the ICE with this board installed are configured when the debugger on the personal computer starts up using the parameter file (88848.par) provided for each model.
The parameter file allows the user to modify its contents according to the ROM and RAM spaces actually used. However, do not configure areas other than below.

ROM area: 0000H to BFFFH
RAM area: F000H to F5FFH
Stack area: F000H to F5FFH

(5) S5U1C88816P2 (add-on board)

This board provides only the 1/17 duty LCD drive function (COM16 output) for the S1C88848. When 1/17 duty mode is not used, this board is not required.

A.3 Connecting to the Target System

This section explains how to connect the S5U1C88000P1&S5U1C88816P2 to the target system.

Note: Turn the power of all equipment off before connecting or disconnecting cables.

Use the I/O cables (80-pin/40-pin × 2 flat type, 60-pin/30-pin × 2 flat type) to connect between the I/O #1 to I/O #3 connectors of the front panel and the target system.
Connect the 80-pin and 60-pin cable connectors to the I/O #1 to I/O #3 connectors, and the 40-pin × 2 and 30-pin × 2 connectors to the target system. Be careful as power (V_{DD}) is supplied to I/O #1 and I/O #2 connectors. When 1/17 duty mode is not used, the S5U1C88816P2 board and the I/O #3 cable are not required.

The following shows the clock frequencies generated from the on-board crystal oscillation circuits:
OSC1 crystal oscillation circuit: 32.768 kHz
OSC3 crystal oscillation circuit: 4.9152 MHz

When CR oscillation is selected, the oscillation frequency can be adjusted using the controls on the front panel (OSC1H and OSC1L for adjusting OSC1, OSC3H and OSC3L for adjusting OSC3). Use a frequency counter or other equipment to be connected to the OSC1 CR oscillation frequency monitor pin (pin 18) on the monitor connector or OSC3 CR oscillation frequency monitor pin (pin 19) for monitoring the frequency during adjustment. Be sure of the frequency when using this monitor pin because the CR oscillation frequency is initially undefined.

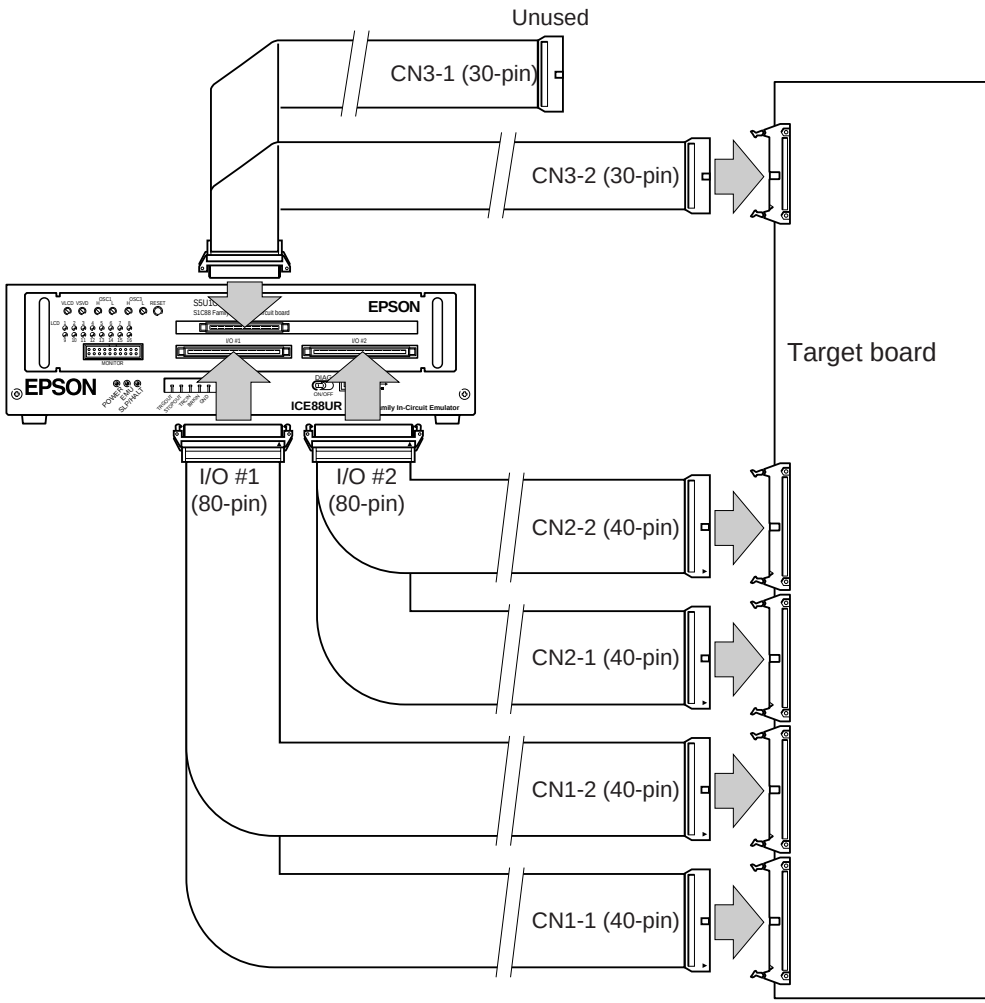


Fig. A.3.1 Connecting to the target system

I/O connector pin assignment

Table A.3.1 I/O #1 connector

40-pin CN1-1		40-pin CN1-2	
No.	Pin name	No.	Pin name
1	V_{DD} (3.3 V)	1	N.C.
2	V_{DD} (3.3 V)	2	N.C.
3	V_{SS}	3	N.C.
4	V_{SS}	4	N.C.
5	K00	5	N.C.
6	K01	6	N.C.
7	K02	7	SEG50DC*1
8	K03	8	SEG49DC*1
9	K04	9	SEG48DC*1
10	K05	10	SEG47DC*1
11	K06	11	N.C.
12	K07	12	N.C.
13	K10/EVIN2	13	R26/$\overline{TOUT}$/REM
14	K11/EVIN0	14	R27/TOUT
15	N.C.	15	SEG46DC*1
16	N.C.	16	SEG45DC*1
17	N.C.	17	SEG44DC*1
18	N.C.	18	SEG43DC*1
19	N.C.	19	R34/FOUT
20	N.C.	20	SEG42DC*1
21	N.C.	21	SEG41DC*1
22	N.C.	22	SEG40DC*1
23	P10/SIN	23	R50/BZ
24	P11/SOUT	24	R51/$\overline{BZ}$
25	P12/$\overline{SCLK}$	25	COM0
26	P13/$\overline{SRDY}$	26	COM1
27	P14	27	COM2
28	P15	28	COM3
29	P16	29	COM4
30	P17	30	COM5
31	N.C.	31	COM6
32	N.C.	32	COM7
33	N.C.	33	COM8
34	N.C.	34	COM9
35	N.C.	35	COM10
36	N.C.	36	COM11
37	N.C.	37	COM12
38	N.C.	38	COM13
39	N.C.	39	COM14
40	N.C.	40	COM15

Table A.3.2 I/O #2 connector

40-pin CN2-1		40-pin CN2-2	
No.	Pin name	No.	Pin name
1	V_{DD} (3.3 V)	1	SEG27
2	V_{DD} (3.3 V)	2	SEG28
3	V_{SS}	3	SEG29
4	V_{SS}	4	SEG30
5	$\overline{RESET}$	5	SEG31
6	N.C.	6	SEG32
7	OSC1EX	7	SEG33
8	OSC3EX	8	SEG34
9	V_{C1}	9	SEG35
10	V_{C2}	10	SEG36
11	V_{C3}	11	SEG37
12	V_{C4}	12	SEG38
13	V_{C5}	13	SEG39
14	SEG0	14	SEG40
15	SEG1	15	SEG41
16	SEG2	16	SEG42
17	SEG3	17	SEG43
18	SEG4	18	SEG44
19	SEG5	19	SEG45
20	SEG6	20	SEG46
21	SEG7	21	SEG47
22	SEG8	22	SEG48
23	SEG9	23	SEG49
24	SEG10	24	SEG50
25	SEG11	25	SEG51/COM31
26	SEG12	26	SEG52/COM30
27	SEG13	27	SEG53/COM29
28	SEG14	28	SEG54/COM28
29	SEG15	29	SEG55/COM27
30	SEG16	30	SEG56/COM26
31	SEG17	31	SEG57/COM25
32	SEG18	32	SEG58/COM24
33	SEG19	33	SEG59/COM23
34	SEG20	34	SEG60/COM22
35	SEG21	35	SEG61/COM21
36	SEG22	36	SEG62/COM20
37	SEG23	37	SEG63/COM19
38	SEG24	38	SEG64/COM18
39	SEG25	39	SEG65/COM17
40	SEG26	40	SEG66/COM16

∗1 The SEG40 to SEG50 pins on this board cannot be configured as DC output ports even if DC output is selected by mask option. When DC output is selected, use the SEG40DC to SEG50DC pins provided as a substitute for them.
The SEG40DC to SEG50DC pins go Hi-Z status when the SEG40 to SEG50 pins are configured as LCD segment output ports by mask option.

Table A.3.3 I/O #3 connector

30-pin CN3-1		30-pin CN3-2	
No.	Pin name	No.	Pin name
1	N.C.	1	N.C.
2	N.C.	2	N.C.
3	N.C.	3	N.C.
4	N.C.	4	N.C.
5	N.C.	5	N.C.
6	N.C.	6	N.C.
7	N.C.	7	COM16*2
8	N.C.	8	N.C.
9	N.C.	9	N.C.
10	N.C.	10	N.C.
11	N.C.	11	N.C.
12	N.C.	12	N.C.
13	N.C.	13	N.C.
14	N.C.	14	N.C.
15	N.C.	15	N.C.
16	N.C.	16	N.C.
17	N.C.	17	N.C.
18	N.C.	18	N.C.
19	N.C.	19	N.C.
20	N.C.	20	N.C.
21	N.C.	21	N.C.
22	N.C.	22	N.C.
23	N.C.	23	N.C.
24	N.C.	24	N.C.
25	N.C.	25	N.C.
26	N.C.	26	N.C.
27	N.C.	27	N.C.
28	N.C.	28	N.C.
29	N.C.	29	N.C.
30	N.C.	30	N.C.

*2 Pin 7 in this connector outputs the COM16 signal only when 1/17 duty mode is used. When 1/17 duty mode is not used, this add-on board is not required.

APPENDIX B DIFFERENCES FROM S1C8F360

The S1C8F360 microcomputer with Flash built-in can be used as a development tool for the S1C88848. The table below summarizes the functional differences between the S1C8F360 and the S1C88848.

Function	S1C8F360	S1C88848
SVD	• A/D conversion type • 00FF12H is different from the S1C88848	• Comparator type
LCD power supply	• TYPE B V_{C5} (max.) = 6.38 V (LCx = FH) • V_{C1} standard (1/4 bias) is not supported	• TYPE B V_{C5} (max.) = 5.7 V (LCx = AH) • Supports V_{C1} standard (1/4 bias)
Initial reset sequence	• After an initial reset, only the OSC1 oscillation circuit starts operating and the OSC1 clock is used as the CPU clock.	• After an initial reset, both the OSC1 and OSC3 oscillation circuit start operating and the OSC3 clock is used as the CPU clock.
Memory size	• ROM: 60K • RAM: 2K	• ROM: 48K • RAM: 1.5K
External memory access	• Supported	• Not supported
LCD drive duty	• 1/17 is not supported	• Supports 1/17 duty
Package	• QFP21-176pin ($24 \times 24mm^2$) Pin layout is compatible with the S1C88848.	• QFP15-128pin ($14 \times 14mm^2$) Pin layout is compatible with the S1C8F360.
Infrared remote-control carrier output	• Not supported	• Supported
Programmable timer	• 8-bit × 2 ch. or 16-bit × 1 ch.	• 8-bit × 4 ch. or 16-bit × 2 ch.
DC output option for segment pins	• Not available	• Up to 11 bits are available
Output port	• R00 to R51 (34 bits)	• R26, R27, R34, R50, R51 (5 bits)
I/O port	• P00 to P07, P10 to P17 (16 bits)	• P10 to P17 (8 bits)
Analog comparator	• Available	• Not available
Successive approximation type A/D	• Available	• Not available
DC characteristics	• See the S1C8F360 Technical Manual. • Input port (Kxx) high-level input voltage (V_{IH}) and low-level input voltage (V_{IL}) are different from the S1C88848.	• See Chapter 7, "Electrical Characteristics". • Kxx incorporates Schmitt circuit
I/O memory map	• See the S1C8F360 Technical Manual.	• See Section 5.1, "I/O Memory Map".
V_{OSC} pin	• Provided. A capacitor is required.	• Not provided
Load resistance between V_{SS} and V_{C1}	• Required	• Not required
CR oscillation characteristic	• See the S1C8F360 Technical Manual.	• See Chapter 7, "Electrical Characteristics".
OSC3 oscillation characteristic (crystal)	• Crystal oscillation start time: max. 20 ms	• Crystal oscillation start time: max. 50 ms
SVD reset	• Provided	• Not provided
Remote-control (REM) status after an initial reset	• Not provided	• After an initial reset, the remote controller operates with the OSC3 clock regardless of whether the REM output option is selected or not. When the remote controller is not used, it should be turned OFF in the initial routine that will be executed after an initial reset to reduce current consumption.

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S1C88848
Technical Manual

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Document code: 404830600
Issue January, 2004
Printed in Japan ⓁA