EPSON

S1C88649

8-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Character Generator ROM (192K bytes)
- Dot-matrix LCD Driver (80 × 16)

■ DESCRIPTION

The S1C88649 is an 8-bit microcomputer for portable equipment with an LCD display that has a built-in LCD controller/driver and a character generator (kanji) ROM. This microcomputer features low-voltage (1.8V) and high-speed (4.2MHz) operations as well as low-current consumption (2.5µA during standby). The LCD controller/driver contains an LCD drive power supply circuit and can drive an maximum of 80 × 16-dot LCD panel in low-power consumption. Furthermore, the S1C88649 has a built-in 11 × 12-dot kanji font ROM that contains JIS level-1 and level-2 kanji sets and other characters, this makes it possible to display kanji characters without any external kanji font ROM. This 8-bit CPU has up to 16MB accessible address space allowing easy implementation of a large data processing application. The S1C88649 is suitable for display modules, portable CD/MD and solid audio players, cordless phones, digital TV remote control units and other applications that required an exclusive LCD driver in conventional systems.

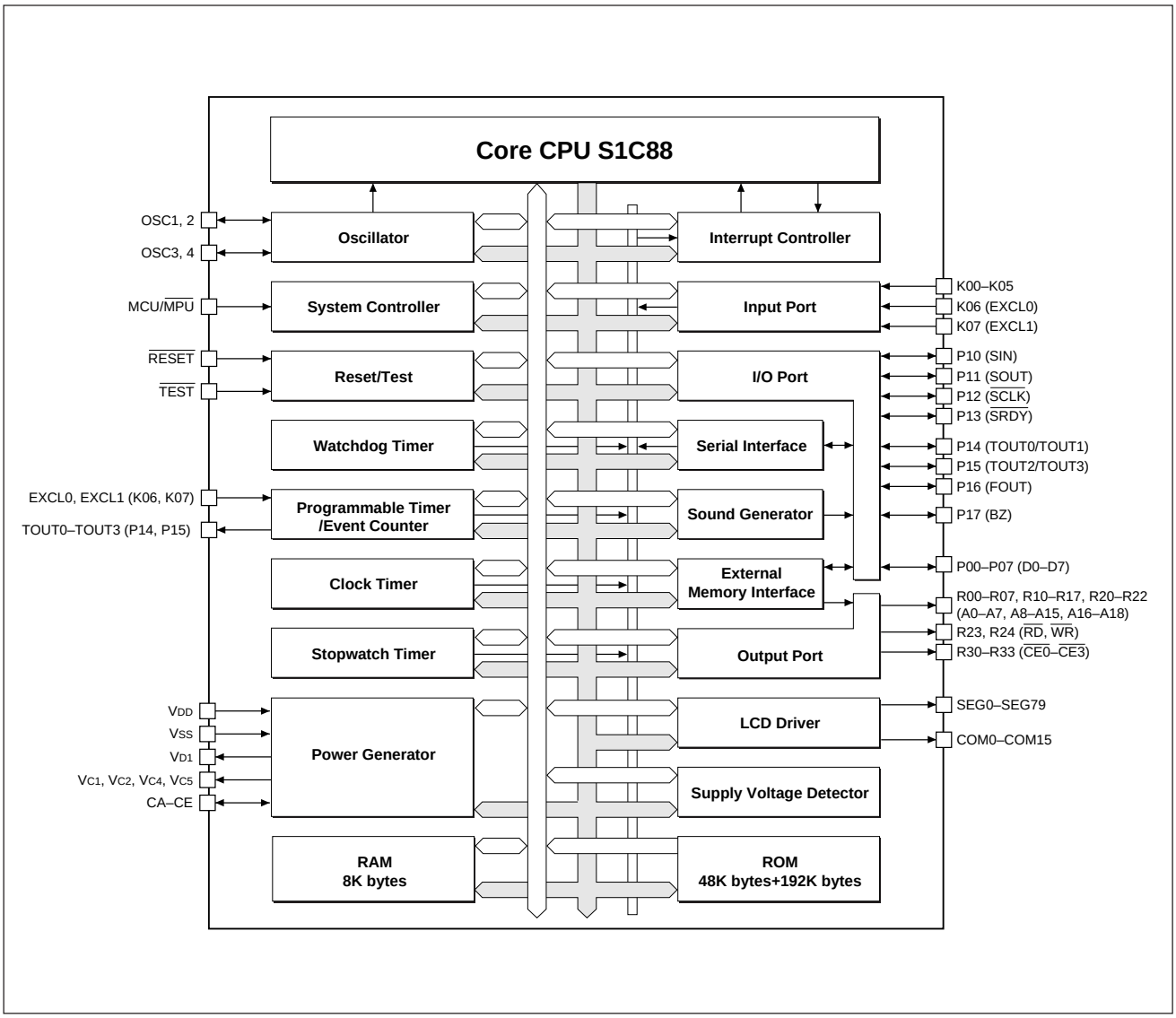
■ FEATURES

- Core CPU ..... S1C88 (MODEL3) CMOS 8-bit core CPU
- Main (OSC3) oscillation circuit ..... Crystal oscillation circuit/ceramic oscillation circuit 4.2MHz (Max.)
  or CR oscillation circuit 2.0MHz (Max.) (∗1)
- Sub (OSC1) oscillation circuit ..... Crystal oscillation circuit/CR oscillation circuit 32.768kHz (Typ.) (∗1)
- Instruction set ..... 608 types (usable for multiplication and division instructions)
- Min. instruction execution time 0.476µsec/4.2MHz (2-clock)
- Internal ROM capacity ..... Program ROM: 48K bytes
  Kanji font ROM: 192K bytes (can be used for a program/data ROM)
- Internal RAM capacity ..... RAM: 8K bytes
  Display memory: 480 bytes
- Bus line ..... Address bus: 19 bits (also usable as a general output port when not used as a bus)
  Data bus: 8 bits (also usable as a general I/O port when not used as a bus)
  $\overline{CE}$ signal: 4 bits
  $\overline{WR}$ signal: 1 bit
  $\overline{RD}$ signal: 1 bit
  (also usable as a general output port when not used as a bus)
- Input port ..... 8 bits (2 bits can be set for event counter external clock input)
- Output port ..... 0–3 bits (when the external bus is used)
  25 bits (when the external bus is not used)
- I/O port ..... 8 bits (when the external bus is used)
  16 bits (when the external bus is not used)
  (shard with serial interface, buzzer, FOUT and TOUT terminals)
- Serial interface ..... 1 ch. (optional clock synchronous system or asynchronous system)
- Timer ..... Programmable timer: 16 bits × 2 ch. or 8 bits × 4 ch.
  Clock timer: 1 ch.
  Stopwatch timer: 1 ch.
- LCD driver ..... Dot matrix type (supports 5 × 8 or 5 × 5 dot fonts and 11 × 12 kanji font)
  80 segments × 16 or 8 commons (∗2) (1/4 bias)
  Built-in LCD power supply circuit (booster type, 4 potentials)

- Sound generator ..... Envelope function, equipped with volume control
- Watchdog timer ..... Built-in
- Supply voltage detection (SVD) circuit ... 13 value programmable (1.8V to 2.7V)
- Interrupt ..... External interrupt: Input port interrupt 1 system (8 types)
  Internal interrupt: Timer interrupt 3 systems (15 types)
  Serial interface interrupt 1 system (3 types)
- Supply voltage ..... 1.8V to 3.6V
- Current consumption (Typ.) ..... SLEEP mode: 1µA
  HALT mode (32kHz Crystal oscillation): 2.5µA
  HALT mode (32kHz CR oscillation): 10µA
  Run (32kHz Crystal oscillation): 7µA
  Run (32kHz CR oscillation): 15µA
  Run (4MHz ceramic oscillation): 670µA
  Run (2MHz CR oscillation): 500µA
- Package ..... Chip

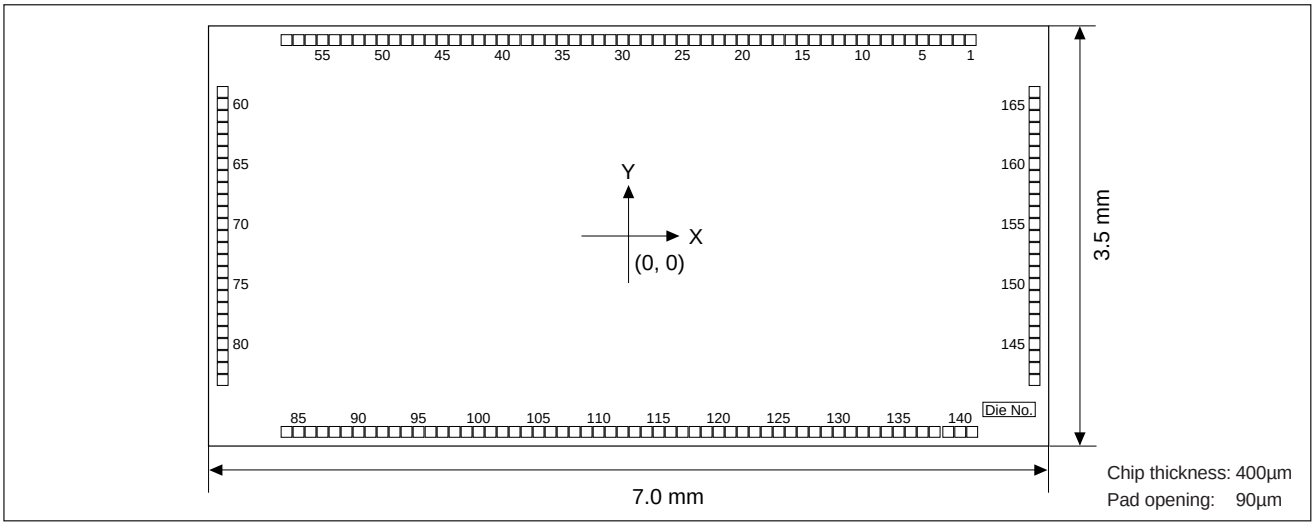
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PAD LAYOUT

● Diagram of Pad Layout



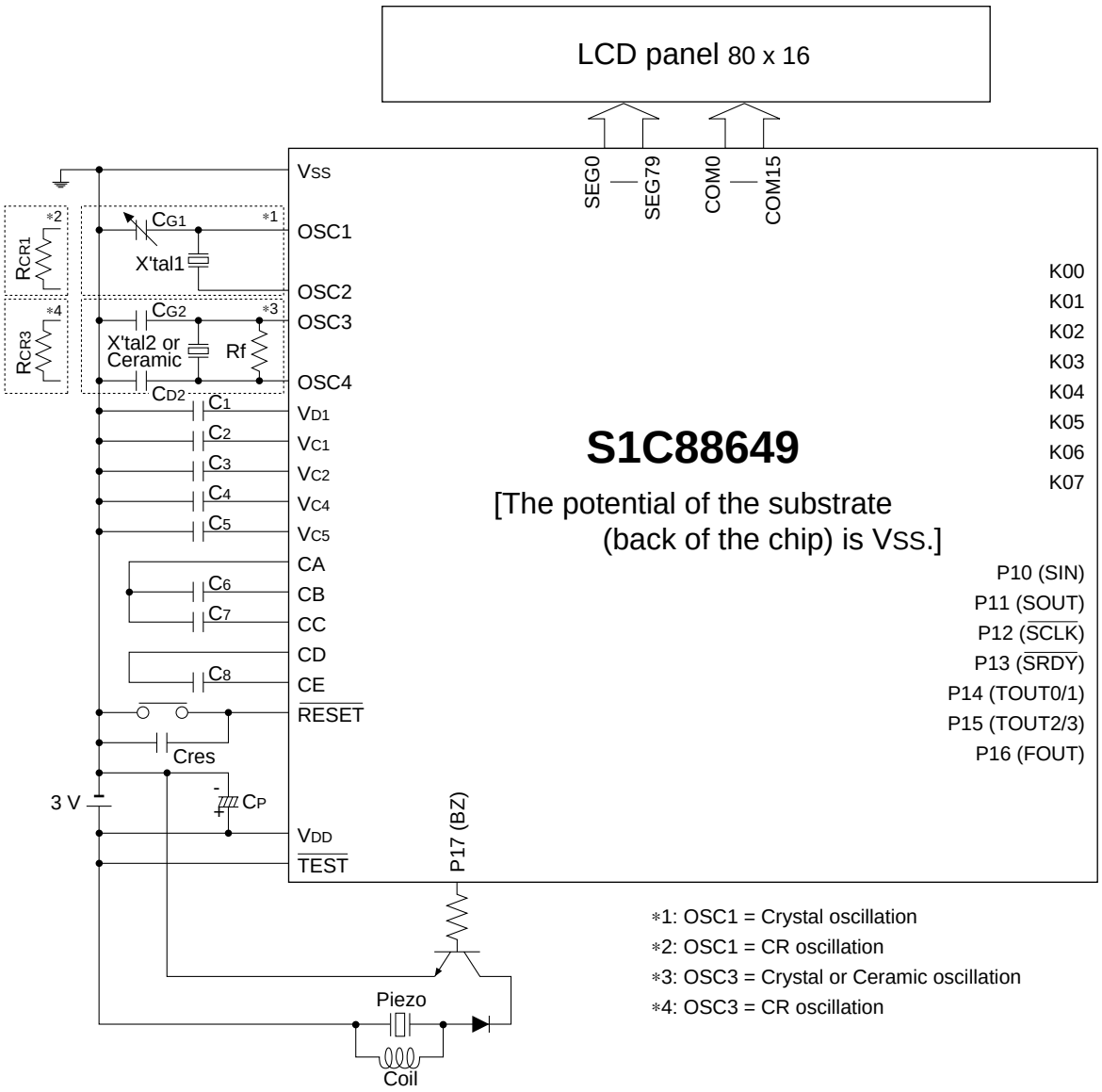
● Pad Coordinates

Pad		Coordinate		Pad		Coordinate		Pad		Coordinate		Pad		Coordinate	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	V_{DD}	2.850	1.632	43	R13/A11	-1.350	1.632	85	SEG26	-2.750	-1.632	127	SEG68	1.450	-1.632
2	V_{SS}	2.750	1.632	44	R14/A12	-1.450	1.632	86	SEG27	-2.650	-1.632	128	SEG69	1.550	-1.632
3	OSC1	2.650	1.632	45	R15/A13	-1.550	1.632	87	SEG28	-2.550	-1.632	129	SEG70	1.650	-1.632
4	OSC2	2.550	1.632	46	R16/A14	-1.650	1.632	88	SEG29	-2.450	-1.632	130	SEG71	1.750	-1.632
5	$\overline{RESET}$	2.450	1.632	47	R17/A15	-1.750	1.632	89	SEG30	-2.350	-1.632	131	SEG72	1.850	-1.632
6	$\overline{TEST}$	2.350	1.632	48	R20/A16	-1.850	1.632	90	SEG31	-2.250	-1.632	132	SEG73	1.950	-1.632
7	MCU/$\overline{MPU}$	2.250	1.632	49	R21/A17	-1.950	1.632	91	SEG32	-2.150	-1.632	133	SEG74	2.050	-1.632
8	K07/EXCL1	2.150	1.632	50	R22/A18	-2.050	1.632	92	SEG33	-2.050	-1.632	134	SEG75	2.150	-1.632
9	K06/EXCL0	2.050	1.632	51	R23/$\overline{RD}$	-2.150	1.632	93	SEG34	-1.950	-1.632	135	SEG76	2.250	-1.632
10	K05	1.950	1.632	52	R24/$\overline{WR}$	-2.250	1.632	94	SEG35	-1.850	-1.632	136	SEG77	2.350	-1.632
11	K04	1.850	1.632	53	R30/$\overline{CE0}$	-2.350	1.632	95	SEG36	-1.750	-1.632	137	SEG78	2.450	-1.632
12	K03	1.750	1.632	54	R31/$\overline{CE1}$	-2.450	1.632	96	SEG37	-1.650	-1.632	138	SEG79	2.550	-1.632
13	K02	1.650	1.632	55	R32/$\overline{CE2}$	-2.550	1.632	97	SEG38	-1.550	-1.632	139	COM15	2.663	-1.632
14	K01	1.550	1.632	56	R33/$\overline{CE3}$	-2.650	1.632	98	SEG39	-1.450	-1.632	140	COM14	2.763	-1.632
15	K00	1.450	1.632	57	V_{DD}	-2.750	1.632	99	SEG40	-1.350	-1.632	141	COM13	2.863	-1.632
16	P17/BZ	1.350	1.632	58	V_{SS}	-2.850	1.632	100	SEG41	-1.250	-1.632	142	COM12	3.382	-1.200
17	P16/FOUT	1.250	1.632	59	SEG0	-3.382	1.200	101	SEG42	-1.150	-1.632	143	COM11	3.382	-1.100
18	P15/TOUT2/TOUT3	1.150	1.632	60	SEG1	-3.382	1.100	102	SEG43	-1.050	-1.632	144	COM10	3.382	-1.000
19	P14/TOUT0/TOUT1	1.050	1.632	61	SEG2	-3.382	1.000	103	SEG44	-0.950	-1.632	145	COM9	3.382	-0.900
20	P13/$\overline{SRDY}$	0.950	1.632	62	SEG3	-3.382	0.900	104	SEG45	-0.850	-1.632	146	COM8	3.382	-0.800
21	P12/$\overline{SCLK}$	0.850	1.632	63	SEG4	-3.382	0.800	105	SEG46	-0.750	-1.632	147	COM7	3.382	-0.700
22	P11/SOUT	0.750	1.632	64	SEG5	-3.382	0.700	106	SEG47	-0.650	-1.632	148	COM6	3.382	-0.600
23	P10/SIN	0.650	1.632	65	SEG6	-3.382	0.600	107	SEG48	-0.550	-1.632	149	COM5	3.382	-0.500
24	P07/D7	0.550	1.632	66	SEG7	-3.382	0.500	108	SEG49	-0.450	-1.632	150	COM4	3.382	-0.400
25	P06/D6	0.450	1.632	67	SEG8	-3.382	0.400	109	SEG50	-0.350	-1.632	151	COM3	3.382	-0.300
26	P05/D5	0.350	1.632	68	SEG9	-3.382	0.300	110	SEG51	-0.250	-1.632	152	COM2	3.382	-0.200
27	P04/D4	0.250	1.632	69	SEG10	-3.382	0.200	111	SEG52	-0.150	-1.632	153	COM1	3.382	-0.100
28	P03/D3	0.150	1.632	70	SEG11	-3.382	0.100	112	SEG53	-0.050	-1.632	154	COM0	3.382	0.000
29	P02/D2	0.050	1.632	71	SEG12	-3.382	0.000	113	SEG54	0.050	-1.632	155	CE	3.382	0.100
30	P01/D1	-0.050	1.632	72	SEG13	-3.382	-0.100	114	SEG55	0.150	-1.632	156	CD	3.382	0.200
31	P00/D0	-0.150	1.632	73	SEG14	-3.382	-0.200	115	SEG56	0.250	-1.632	157	CC	3.382	0.300
32	R00/A0	-0.250	1.632	74	SEG15	-3.382	-0.300	116	SEG57	0.350	-1.632	158	CB	3.382	0.400
33	R01/A1	-0.350	1.632	75	SEG16	-3.382	-0.400	117	SEG58	0.450	-1.632	159	CA	3.382	0.500
34	R02/A2	-0.450	1.632	76	SEG17	-3.382	-0.500	118	SEG59	0.550	-1.632	160	V_{C5}	3.382	0.600
35	R03/A3	-0.550	1.632	77	SEG18	-3.382	-0.600	119	SEG60	0.650	-1.632	161	V_{C4}	3.382	0.700
36	R04/A4	-0.650	1.632	78	SEG19	-3.382	-0.700	120	SEG61	0.750	-1.632	162	V_{C2}	3.382	0.800
37	R05/A5	-0.750	1.632	79	SEG20	-3.382	-0.800	121	SEG62	0.850	-1.632	163	V_{C1}	3.382	0.900
38	R06/A6	-0.850	1.632	80	SEG21	-3.382	-0.900	122	SEG63	0.950	-1.632	164	OSC3	3.382	1.000
39	R07/A7	-0.950	1.632	81	SEG22	-3.382	-1.000	123	SEG64	1.050	-1.632	165	OSC4	3.382	1.100
40	R10/A8	-1.050	1.632	82	SEG23	-3.382	-1.100	124	SEG65	1.150	-1.632	166	V_{D1}	3.382	1.200
41	R11/A9	-1.150	1.632	83	SEG24	-3.382	-1.200	125	SEG66	1.250	-1.632	–	–	–	–
42	R12/A10	-1.250	1.632	84	SEG25	-2.850	-1.632	126	SEG67	1.350	-1.632	–	–	–	–

■ PIN DESCRIPTION

Pin name	Pad No.	In/Out	Function
V_{DD}	1, 57	–	Power supply (+) terminal
V_{SS}	2, 58	–	Power supply (GND) terminal
V_{D1}	166	–	Internal logic system and oscillation system voltage regulator output terminals
V_{C1}, V_{C2}, V_{C4}, V_{C5}	163–160	–	LCD drive voltage output terminals
CA–CE	159–155	–	Booster capacitor connection terminals for LCD
OSC1	3	I	OSC1 oscillation input terminal (select crystal/CR oscillation by mask option)
OSC2	4	O	OSC1 oscillation output terminal
OSC3	164	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation by mask option)
OSC4	165	O	OSC3 oscillation output terminal
MCU/$\overline{\text{MPU}}$	7	I	Terminal for setting MCU or MPU modes
K00–K05	15–10	I	Input terminals (K00–K05)
K06/EXCL0	9	I	Input terminal (K06) or programmable timer external clock input terminal (EXCL0)
K07/EXCL1	8	I	Input terminal (K07) or programmable timer external clock input terminal (EXCL1)
R00–R07/A0–A7	32–39	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	40–47	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R22/A16–A18	48–50	O	Output terminals (R20–R22) or address bus (A16–A18)
R23/$\overline{\text{RD}}$	51	O	Output terminal (R23) or read signal output terminal ($\overline{\text{RD}}$)
R24/$\overline{\text{WR}}$	52	O	Output terminal (R24) or write signal output terminal ($\overline{\text{WR}}$)
R30–R33/$\overline{\text{CE0}}$–$\overline{\text{CE3}}$	53–56	O	Output terminals (R30–R33) or chip enable signal output terminals ($\overline{\text{CE0}}$–$\overline{\text{CE3}}$)
P00–P07/D0–D7	31–24	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	23	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	22	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	21	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	20	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14/TOUT0/TOUT1	19	I/O	I/O terminal (P14) or programmable timer underflow signal output terminal (TOUT0/TOUT1)
P15/TOUT2/TOUT3	18	I/O	I/O terminal (P15) or programmable timer underflow signal output terminal (TOUT2/TOUT3)
P16/FOUT	17	I/O	I/O terminal (P16) or clock output terminal (FOUT)
P17/BZ	16	I/O	I/O terminal (P17) or buzzer signal output terminal (BZ)
COM0–COM15	154–139	O	LCD common output terminals
SEG0–SEG79	59–138	O	LCD segment output terminals
$\overline{\text{RESET}}$	5	I	Initial reset input terminal
$\overline{\text{TEST}}$	6	I	Test input terminal

■ BASIC EXTERNAL CONNECTION DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ
C_{G1}	Trimmer capacitor	0–25 pF
R_{CR1}	Resistor for CR oscillation	1.5 MΩ
X'tal2	Crystal oscillator	4 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
C_{D2}	Drain capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)

Symbol	Name	Recommended value
R_{CR3}	Resistor for CR oscillation	40 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_6–C_8	Booster capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

Note: The above table is simply an example, and is not guaranteed to work.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +4.7	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +6.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	
Operating temperature	Topr		-20 to +70	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10 sec (lead section)	–	

● Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	V_{DD}		1.8		3.6	V	
Operating frequency	f_{OSC1}		30	32.768	200	kHz	
	f_{OSC3}	CR oscillation	0.03		2.0	MHz	
		Crystal/ceramic oscillation	0.03		4.2	MHz	
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	1
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	1
Capacitor between V_{C4} and V_{SS}	C_4			0.1		µF	1
Capacitor between V_{C5} and V_{SS}	C_5			0.1		µF	1
Capacitor between CA and CB	C_6			0.1		µF	1
Capacitor between CA and CC	C_7			0.1		µF	1
Capacitor between CD and CE	C_8			0.1		µF	1

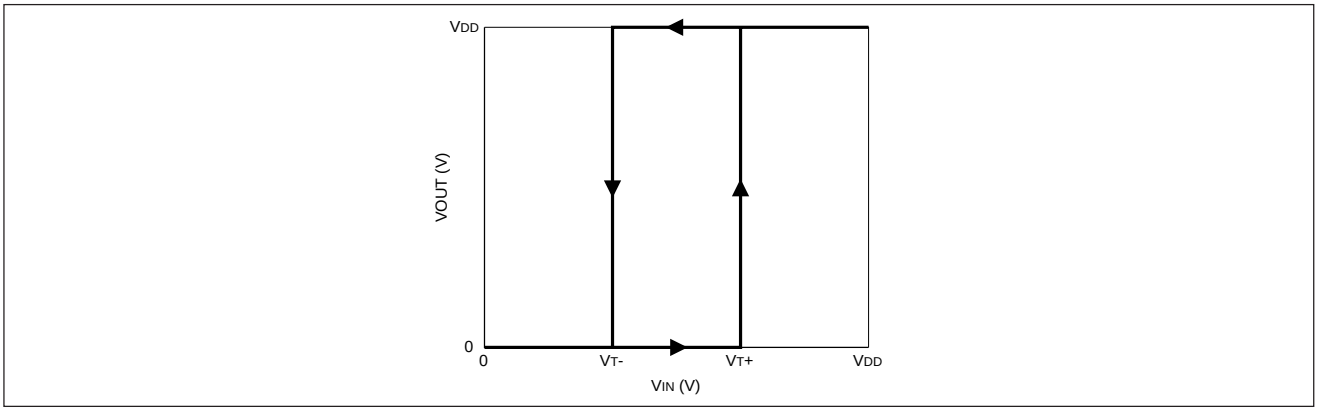
Note) 1 When LCD drive power is not used, the capacitor is not necessary.
In this case, leave the V_{C1} to V_{C5} and CA to CE terminals open.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage	V_{IH}	Kxx, Pxx	0.8V_{DD}		V_{DD}	V	
Low level input voltage	V_{IL}	Kxx, Pxx	0		0.2V_{DD}	V	
High level schmitt input voltage (1)	V_{T1+}	$\overline{RESET}$, MCU/$\overline{MPU}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage (1)	V_{T1-}	$\overline{RESET}$, MCU/$\overline{MPU}$	0.1V_{DD}		0.5V_{DD}	V	
High level schmitt input voltage (2)	V_{T2+}	Kxx	0.4V_{DD}		0.9V_{DD}	V	1
Low level schmitt input voltage (2)	V_{T2-}	Kxx	0.1V_{DD}		0.4V_{DD}	V	1
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9 V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1 V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	100		500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN} = 0V, f = 1MHz, Ta = 25°C			15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1V	5			µA	

Note) 1 When CMOS Schmitt level is selected by mask option.
2 When addition of pull-up resistor is selected by mask option.



● LCD Drive Circuit

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, C_1–C_8=0.1µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	∗1		0.24V_{C5}		0.28V_{C5}	V	
	V_{C2}	∗2		0.48V_{C5}		0.52V_{C5}	V	
	V_{C4}	∗3		0.74V_{C5}		0.78V_{C5}	V	
	V_{C5}	∗4	LCX = 0H		3.64		V	
			LCX = 1H		3.71		V	
			LCX = 2H		3.79		V	
			LCX = 3H		3.86		V	
			LCX = 4H		3.93		V	
			LCX = 5H		4.00		V	
			LCX = 6H		4.07		V	
			LCX = 7H	Typ×0.94	4.15	Typ×1.06	V	
			LCX = 8H		4.22		V	
			LCX = 9H		4.30		V	
			LCX = AH		4.37		V	
			LCX = BH		4.45		V	
			LCX = CH		4.52		V	
			LCX = DH		4.60		V	
			LCX = EH		4.68		V	
			LCX = FH		4.76		V	

∗1 Connects 1 MΩ load resistor between V_{SS} and V_{C1}.
∗2 Connects 1 MΩ load resistor between V_{SS} and V_{C2}.
∗3 Connects 1 MΩ load resistor between V_{SS} and V_{C4}.
∗4 Connects 1 MΩ load resistor between V_{SS} and V_{C5}.

● SVD Circuit

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	SVDS0–3 = "0"		–		V	
		SVDS0–3 = "1"		–		V	
		SVDS0–3 = "2"		–		V	
		SVDS0–3 = "3"		1.8		V	
		SVDS0–3 = "4"		1.85		V	
		SVDS0–3 = "5"		1.9		V	
		SVDS0–3 = "6"		1.95		V	
		SVDS0–3 = "7"		2.0		V	
		SVDS0–3 = "8"		2.05		V	
		SVDS0–3 = "9"	Typ×0.91	2.1	Typ×1.09	V	
		SVDS0–3 = "10"		2.2		V	
		SVDS0–3 = "11"		2.3		V	
		SVDS0–3 = "12"		2.4		V	
		SVDS0–3 = "13"		2.5		V	
		SVDS0–3 = "14"		2.6		V	
		SVDS0–3 = "15"		2.7		V	
SVD circuit response time	t_{SVD}				500	µs	

● Power Current Consumption

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, C_1–C_8=0.1µF, No panel load)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SLEEP mode current consumption	I_{SLP}	OSC1 = OFF, OSC3 = OFF		1	2.5	µA	
HALT mode current consumption	I_{HALT1}	OSC1 = 32kHz Crystal oscillation, OSC3 = OFF		2.5	5	µA	
	I_{HALT2}	OSC1 = 32kHz CR oscillation, OSC3 = OFF		10	20	µA	
	I_{HALT3}	OSC1 = 32kHz Crystal oscillation, OSC3 = 4MHz Ceramic oscillation		130	300	µA	
	I_{HALT4}	OSC1 = 32kHz CR oscillation, OSC3 = 2MHz CR oscillation		220	450	µA	
Runtime current consumption	I_{EXE1}	OSC1 = 32kHz Crystal oscillation, OSC3 = OFF		7	15	µA	
	I_{EXE2}	OSC1 = 32kHz CR oscillation, OSC3 = OFF		15	30	µA	
	I_{EXE3}	OSC1 = 32kHz Crystal oscillation, OSC3 = 4MHz Ceramic oscillation		670	1500	µA	
	I_{EXE4}	OSC1 = 32kHz CR oscillation, OSC3 = 2MHz CR oscillation		500	1000	µA	
Runtime current consumption (Heavy Load Protection Mode)	I_{HVL1}	OSC1 = 32kHz Crystal oscillation, OSC3 = OFF, HLMOD = H		15	30	µA	
	I_{HVL2}	OSC1 = 32kHz CR oscillation, OSC3 = OFF, HLMOD = H		40	80	µA	
LCD drive circuit current	I_{LCDN}	LCDCx = All on, LCx = 8H, f_{OSC1} = 32.768kHz		2	5	µA	1
LCD drive circuit current (Heavy Load Protection Mode)	I_{LCDH}	LCDCx = All on, LCx = 8H, f_{OSC1} = 32.768kHz, HLMOD = H		12	25	µA	2
SVD circuit current	I_{SVD}	SVDON = ON		5	10	µA	3

Note) 1 This value is added to the runtime current consumption when the LCD drive circuit is active.
2 This value is added to the runtime current consumption (in heavy load protection mode) when the LCD drive circuit is active.
3 This value is added to the runtime current consumption (normal mode or heavy load protection mode) when the SVD circuit is active.

● AC Characteristics

Operating range

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency	f_{OSC1}	V_{DD} = 1.8 to 3.6V	30	32.768	200	kHz	
	f_{OSC3}		0.03		4.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	10	61	67	µs	
		2-cycle instruction	20	122	133	µs	
		3-cycle instruction	30	183	200	µs	
		4-cycle instruction	40	244	267	µs	
		5-cycle instruction	50	305	333	µs	
		6-cycle instruction	60	366	400	µs	
Instruction execution time (during operation with OSC3 clock)	tcy	1-cycle instruction	0.5		66.7	µs	
		2-cycle instruction	1.0		133.3	µs	
		3-cycle instruction	1.4		200.0	µs	
		4-cycle instruction	1.9		266.7	µs	
		5-cycle instruction	2.4		333.3	µs	
		6-cycle instruction	2.9		400.0	µs	

External memory access

1. Read cycle

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{IH2}=1.6V, V_{IL2}=0.6V, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, C_L=100pF(load capacitance))

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	tc+tl-100+n•tc/2			ns	1
Address hold time in read cycle	trah	th-80			ns	
Read signal pulse width	trp	tc-50+n•tc/2			ns	1
Data input set-up time in read cycle	trds	300			ns	
Data input hold time in read cycle	trdh	0			ns	

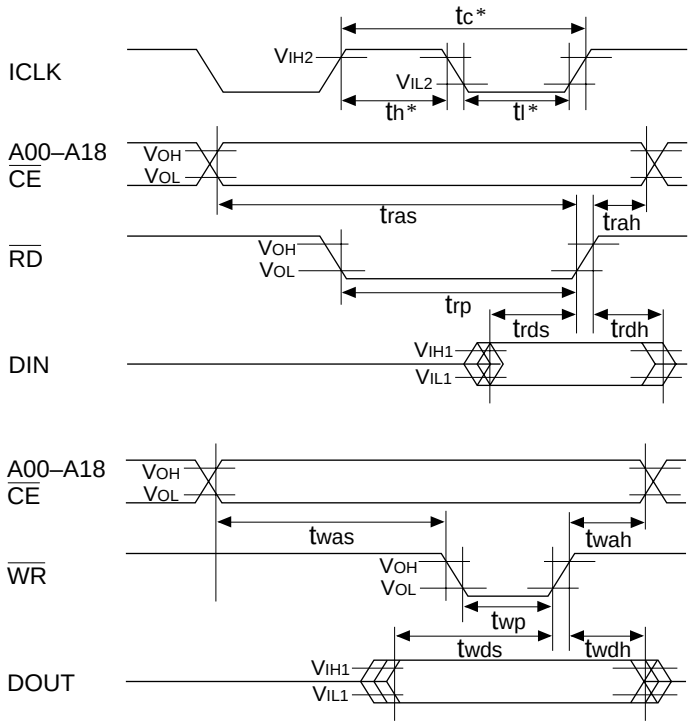
Note) 1 Substitute the number of states for wait insertion in n.

2. Write cycle

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{IH2}=1.6V, V_{IL2}=0.6V, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, C_L=100pF(load capacitance))

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	tc-180			ns	
Address hold time in write cycle	twah	th-80			ns	
Write signal pulse width	twp	tl-40+n•tc/2			ns	1
Data output set-up time in write cycle	twds	tc-180+n•tc/2			ns	1
Data output hold time in write cycle	twdh	th-80		th+80	ns	

Note) 1 Substitute the number of states for wait insertion in n.



* In the case of crystal oscillation and ceramic oscillation: th = 0.5tc ± 0.05tc, tl = tc - th (1/tc: oscillation frequency)
* In the case of CR oscillation: th = 0.5tc ± 0.10tc, tl = tc - th (1/tc: oscillation frequency)

Serial interface

1. Clock synchronous master mode

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			200	ns	
Receiving data input set-up time	tsms	500			ns	
Receiving data input hold time	tsmh	200			ns	

2. Clock synchronous slave mode

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			500	ns	
Receiving data input set-up time	tsss	200			ns	
Receiving data input hold time	tssh	200			ns	

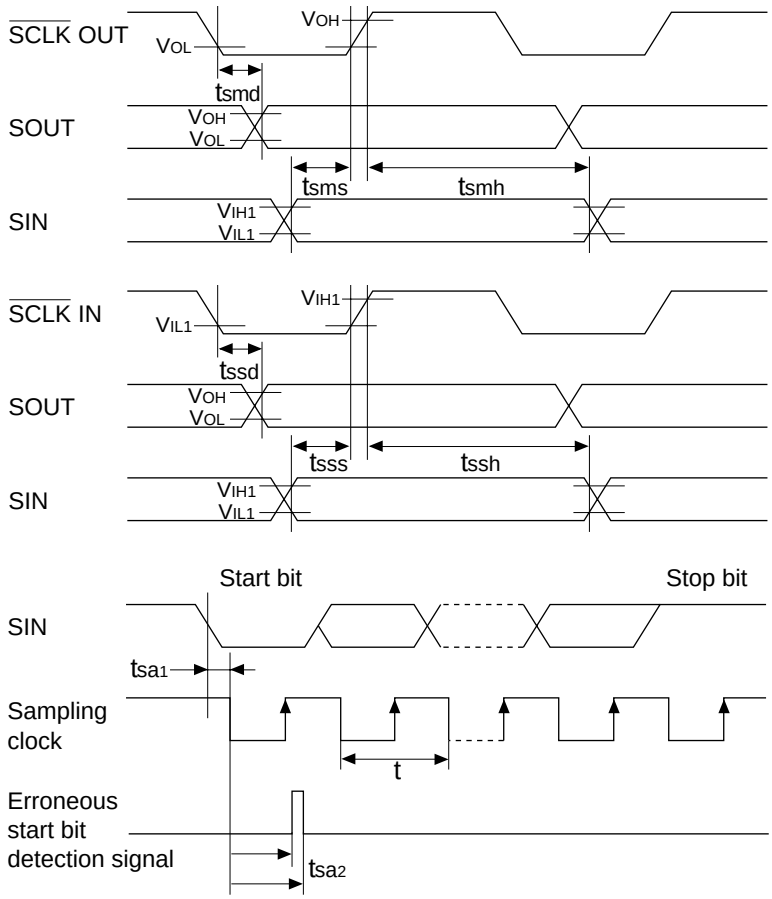
3. Asynchronous system

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	s	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	s	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

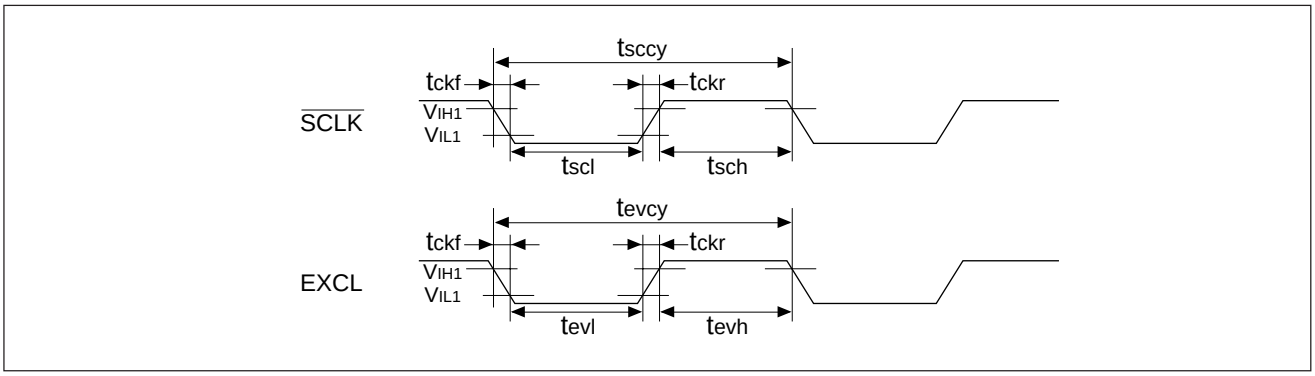


Input clock

1. $\overline{SCLK}$, EXCL input clock

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD})

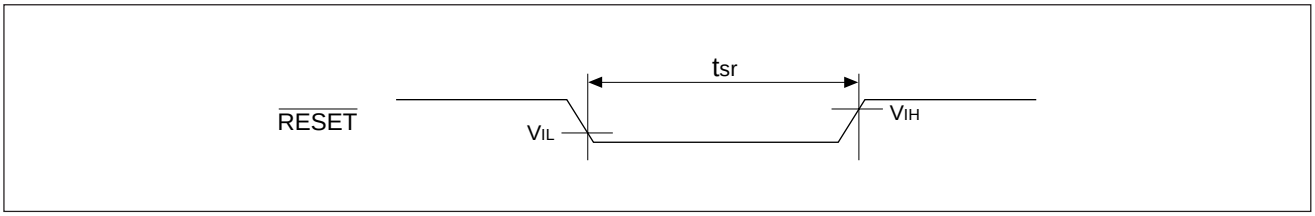
Item		Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	t_{sccy}	4			µs	
	"H" pulse width	t_{sch}	2			µs	
	"L" pulse width	t_{scl}	2			µs	
EXCL input clock time	Cycle time	t_{evcy}	4			µs	
	"H" pulse width	t_{evh}	2			µs	
	"L" pulse width	t_{evl}	2			µs	
Input clock rising time		t_{ckr}			25	ns	
Input clock falling time		t_{ckf}			25	ns	



2. $\overline{\text{RESET}}$ input clock

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, V_{IH}=0.5V_{DD}, V_{IL}=0.1V_{DD})

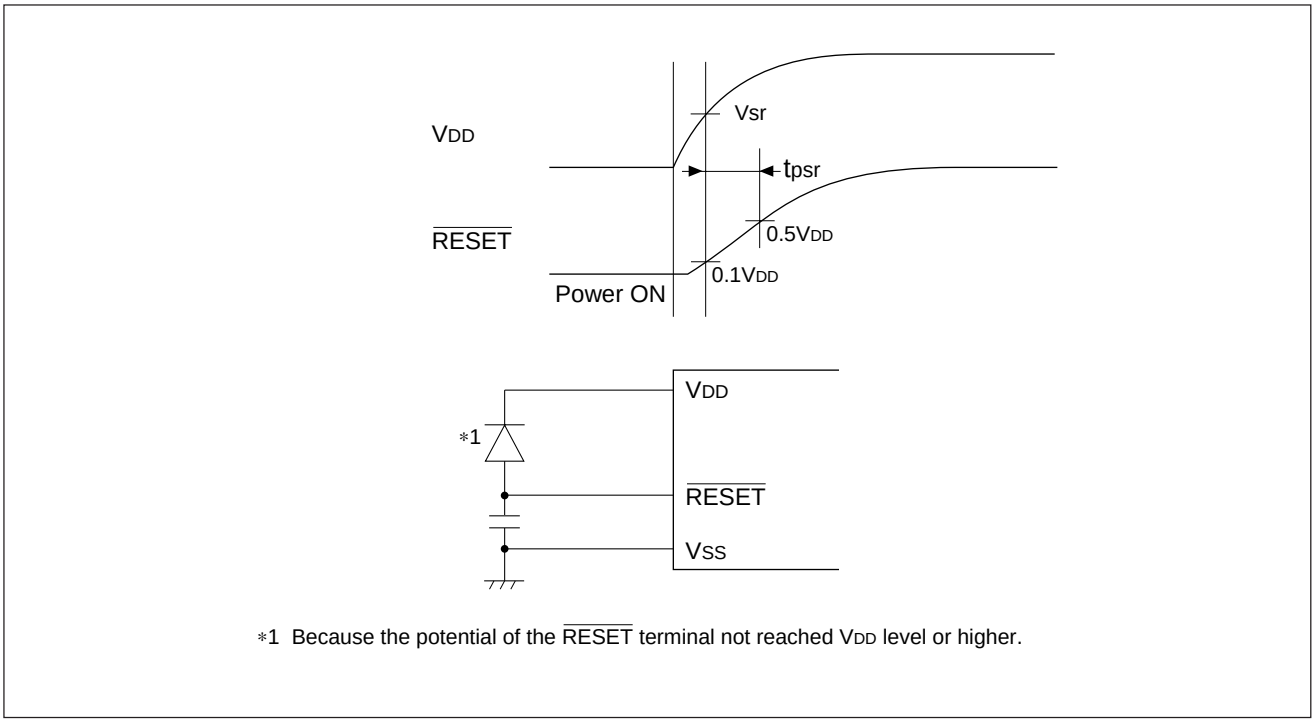
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µs	



Power ON reset

(Condition: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	2.4			V	
$\overline{\text{RESET}}$ input time	tpsr	10			ms	



*1 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

● Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or crystal oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

OSC1 (Crystal)

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, Crystal oscillator=Q12C2*, C_{G1}=25pF, C_{D1}=Built-in)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	s	
External gate capacitance	C_{G1}	Including board capacitance	5		25	pF	
Built-in drain capacitance	C_{D1}	In case of the chip		10		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 5 to 25pF	25			ppm	

* Q12C2 Made by Seiko Epson corporation

OSC1 (CR)

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

OSC3 (Crystal)

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, Crystal oscillator=Q21CA301xxx*, R_F=1MΩ, C_{G2}=C_{D2}=15pF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				10	ms	1

* Q21CA301xxx Made by Seiko Epson corporation

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

OSC3 (Ceramic)

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C, Ceramic oscillator=KBR-4.0MSB*, R_F=1MΩ, C_{G2}=C_{D2}=30pF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				1	ms	1

* KBR-4.0MSB Made by Kyocera

Note) 1 The ceramic oscillation start time changes by the ceramic oscillator to be used, C_{G2} and C_{D2}.

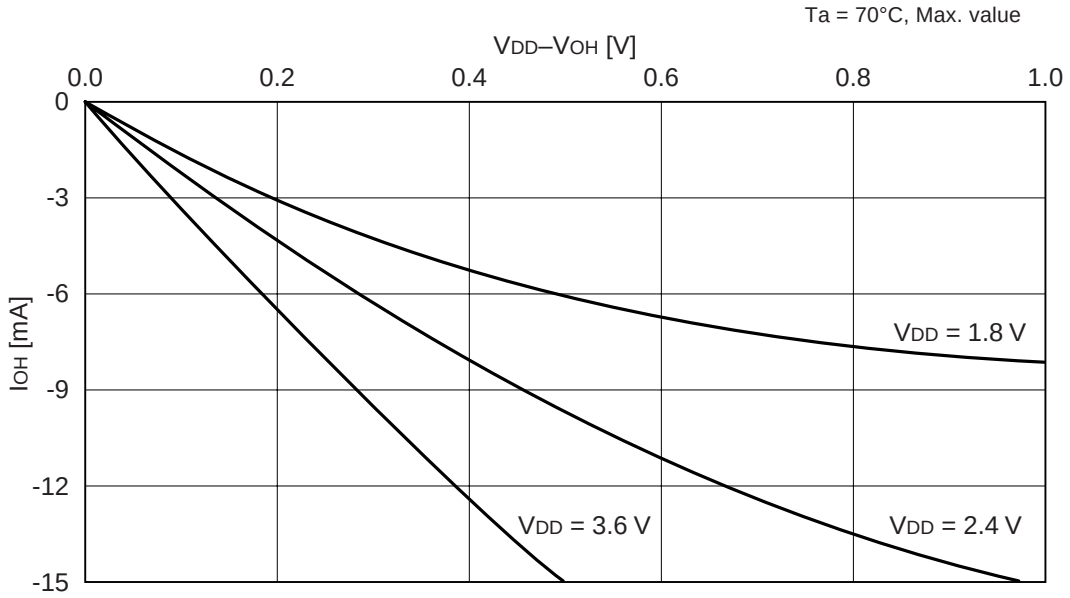
OSC3 (CR)

(Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=25°C)

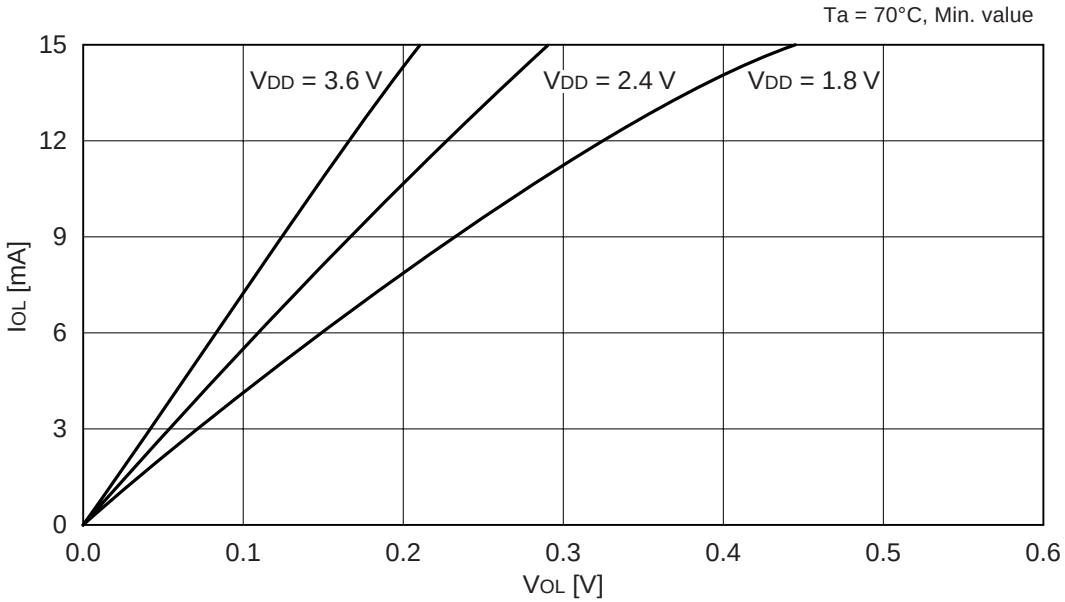
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				100	µs	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

● Characteristics Curves (reference value)

• High level output current-voltage characteristic

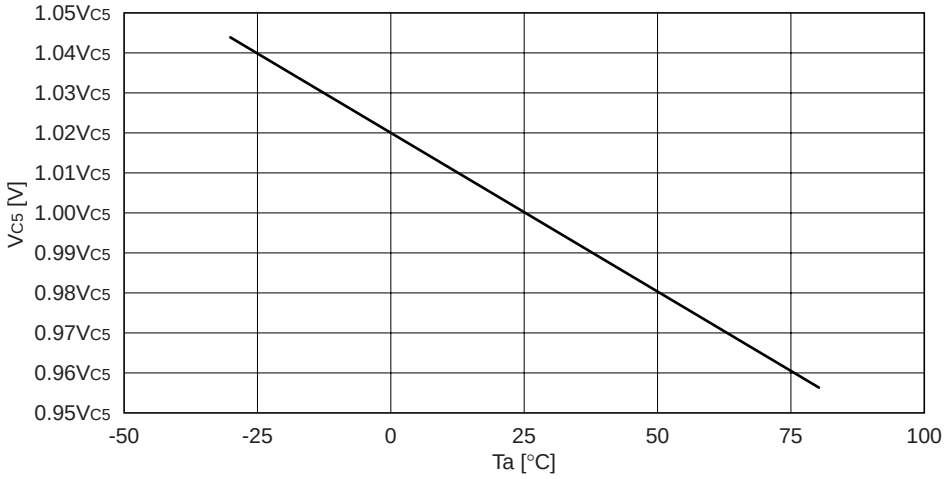


• Low level output current-voltage characteristic



• **LCD drive voltage-ambient temperature characteristic**

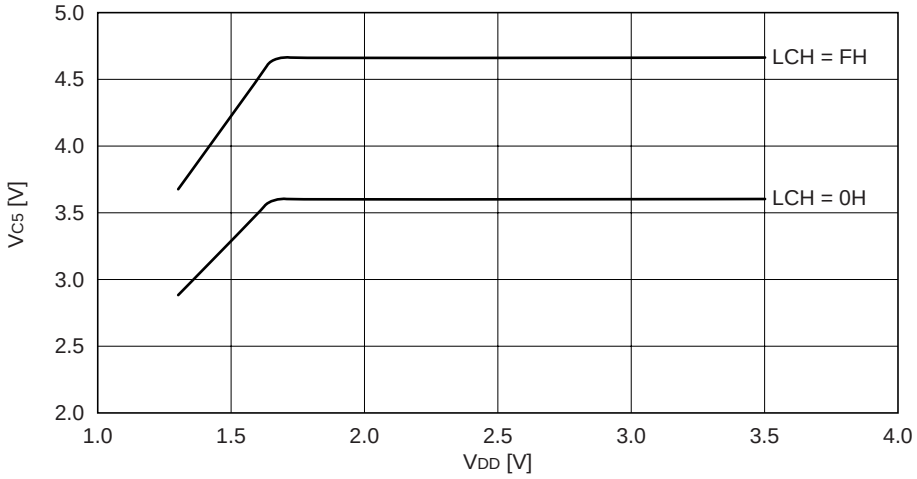
Typ. value



• **LCD drive voltage-supply voltage characteristic**

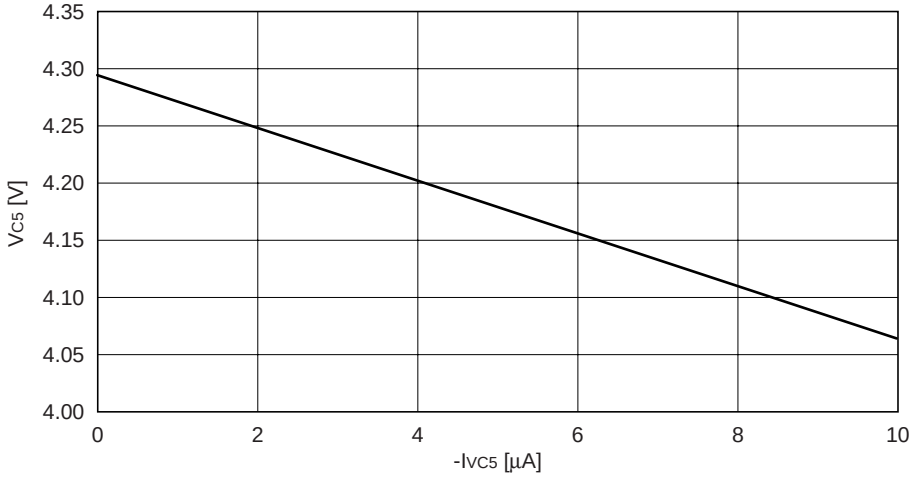
Connects 1MΩ load resistor between VSS and VC5. (no panel load)

Ta = 25°C, Typ. value

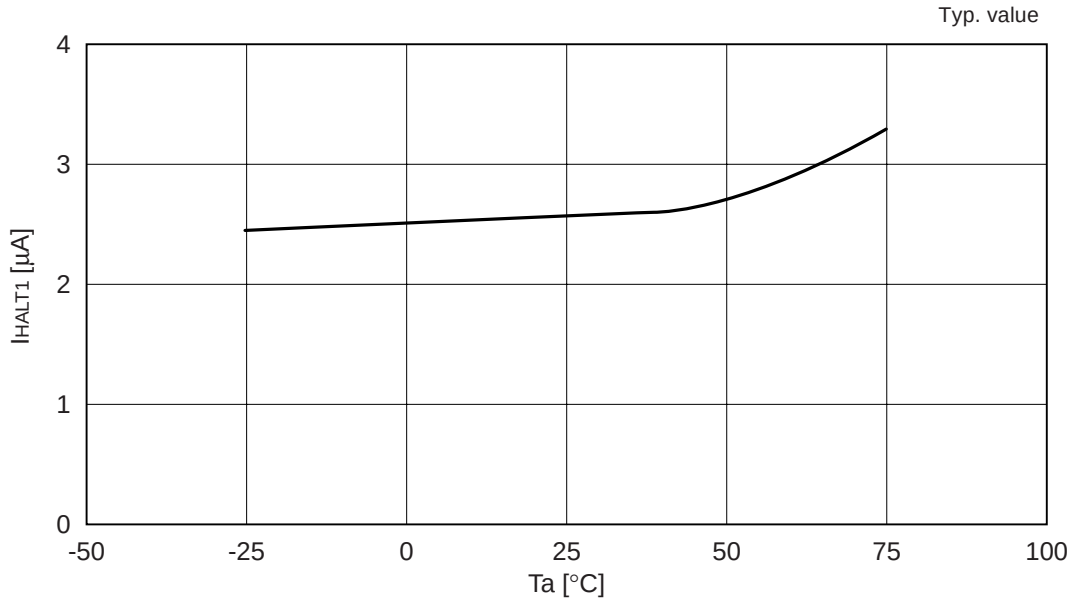


• **LCD drive voltage-load characteristic**

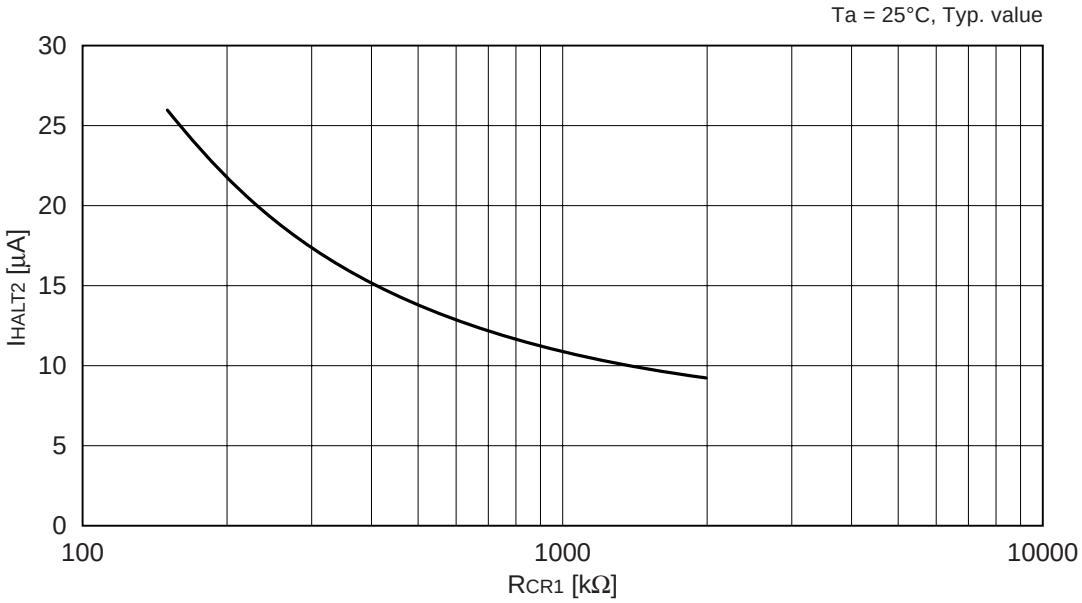
Ta = 25°C, Typ. value, LCx = 8H



• In HALT status current consumption temperature characteristic
(During operation with OSC1) <Crystal oscillation, f_{OSC1} = 32.768kHz>

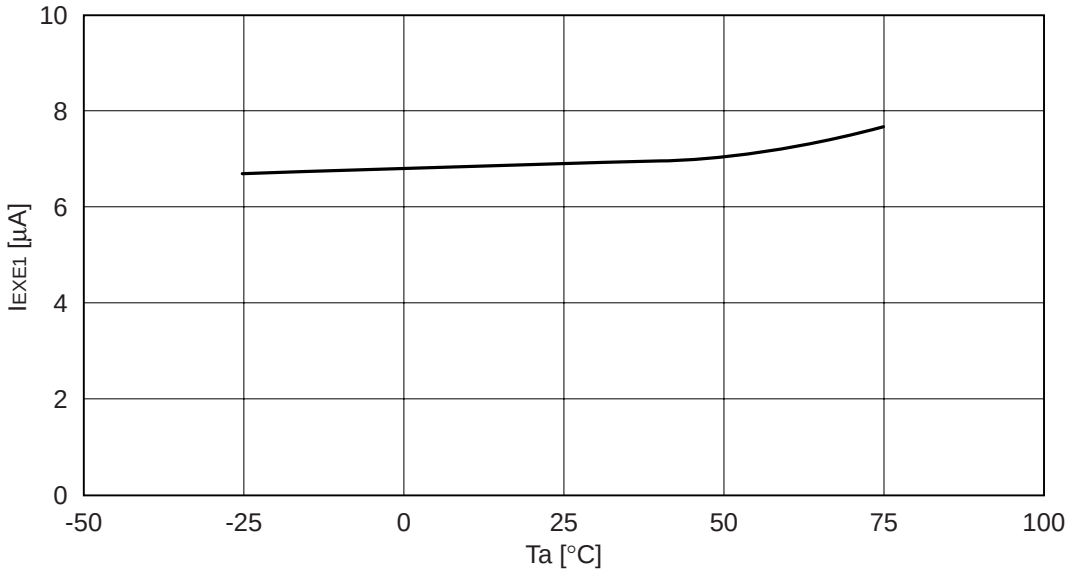


• In HALT status current consumption resistor characteristic
(During operation with OSC1) <CR oscillation>



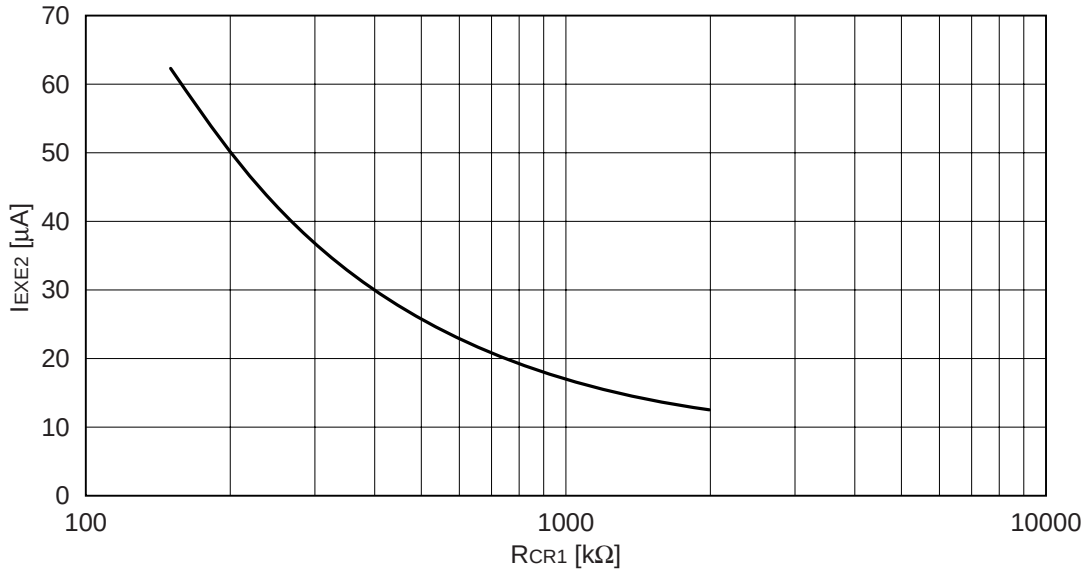
• **In executed status current consumption temperature characteristic (During operation with OSC1) <Crystal oscillation, f_{OSC1} = 32.768kHz>**

Typ. value

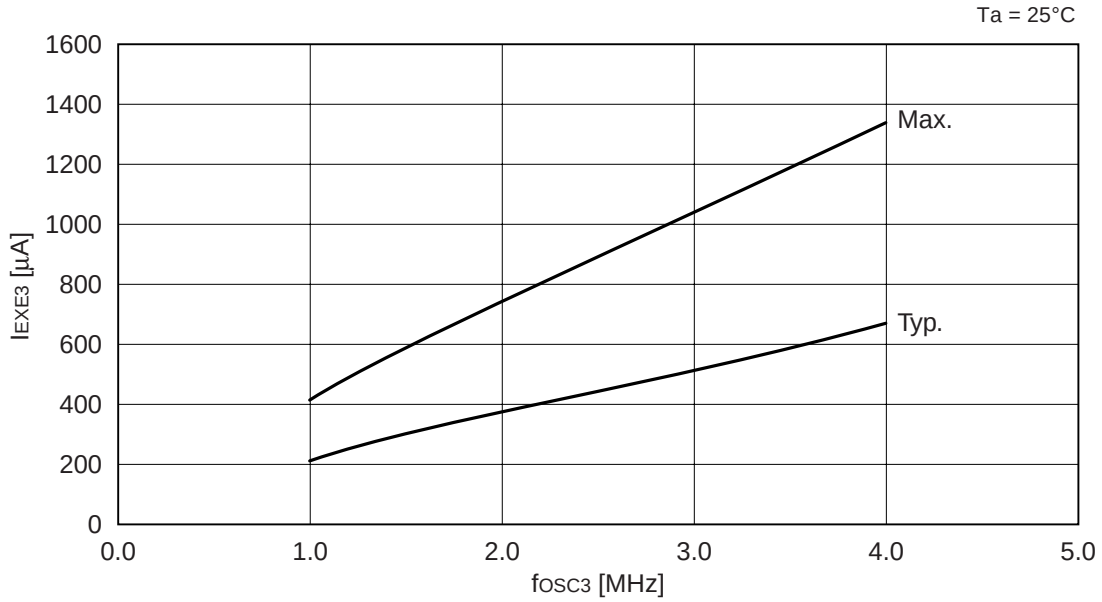


• **In executed status current consumption resistor characteristic (During operation with OSC1) <CR oscillation>**

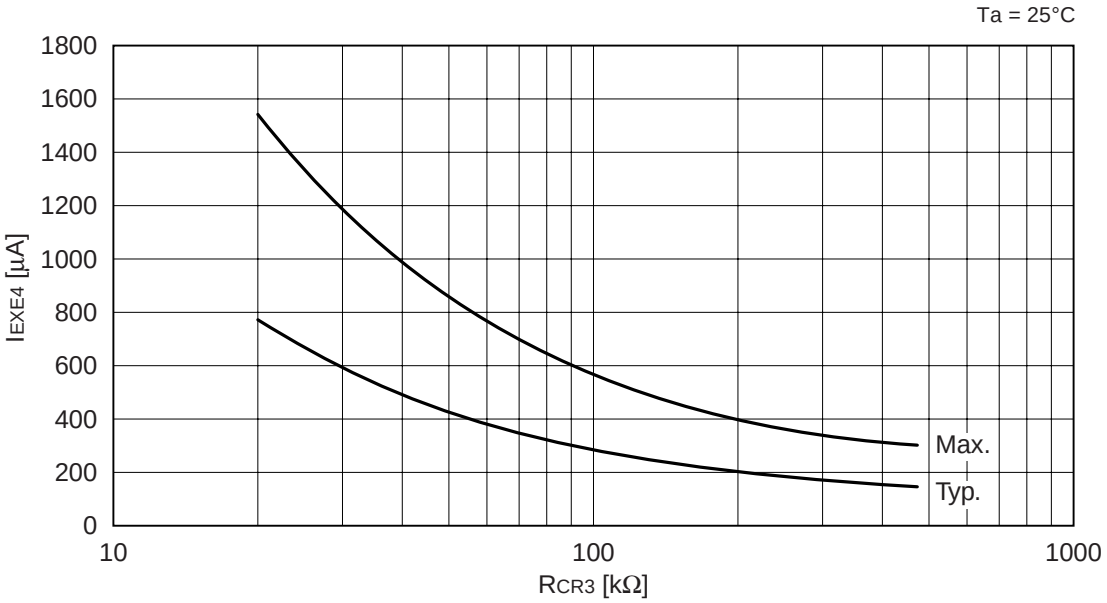
Ta = 25°C, Typ. value



• In executed status current consumption frequency characteristic
(During operation with OSC3) <Crystal oscillation/Ceramic oscillation>

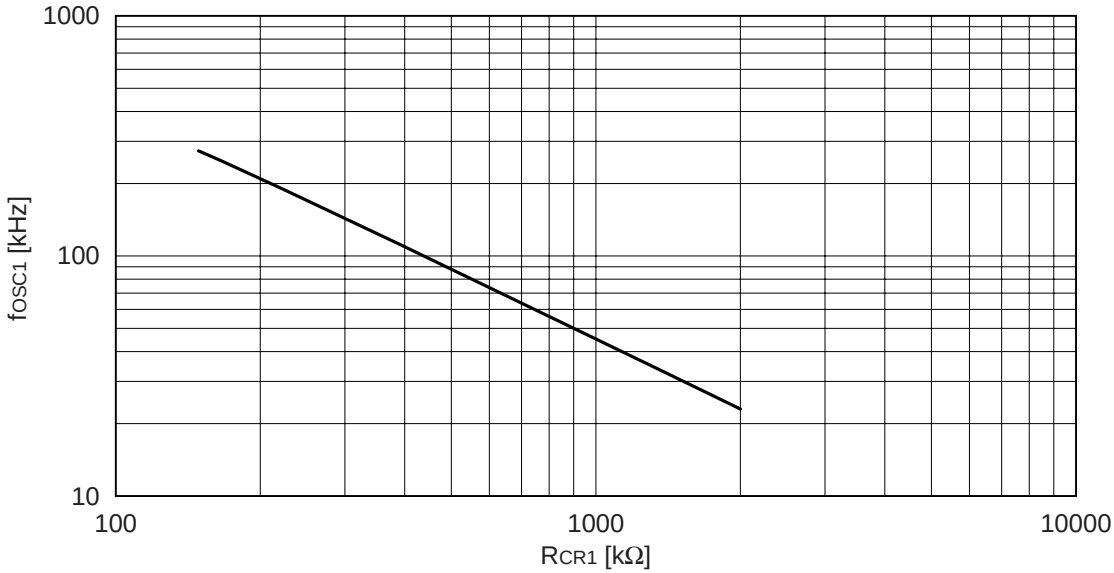


• In executed status current consumption resistor characteristic
(During operation with OSC3) <CR oscillation>



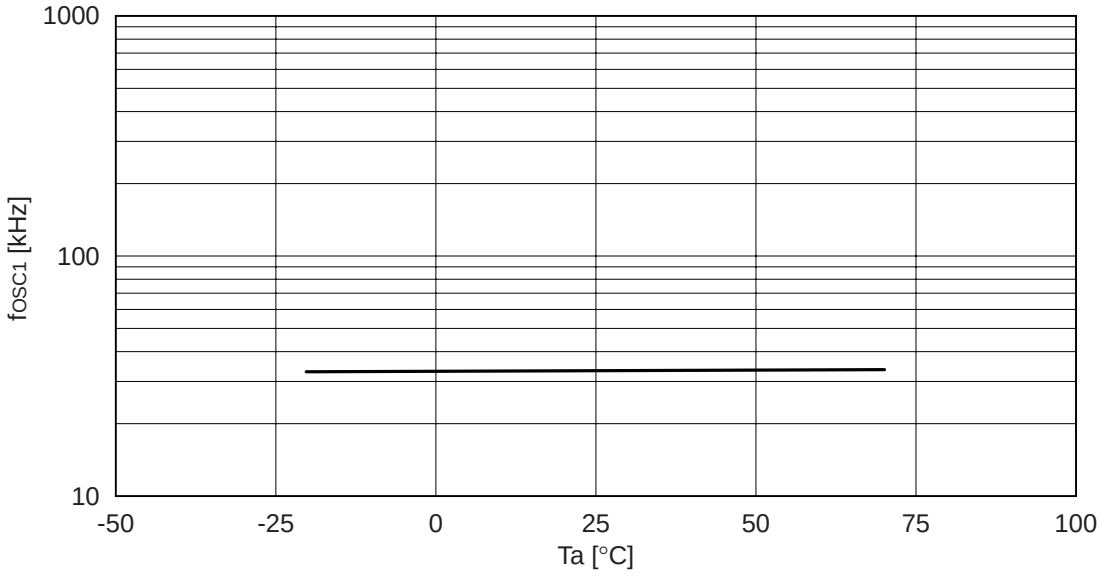
• **Oscillation frequency resistor characteristic (OSC1)**

Ta = 25°C, Typ. value



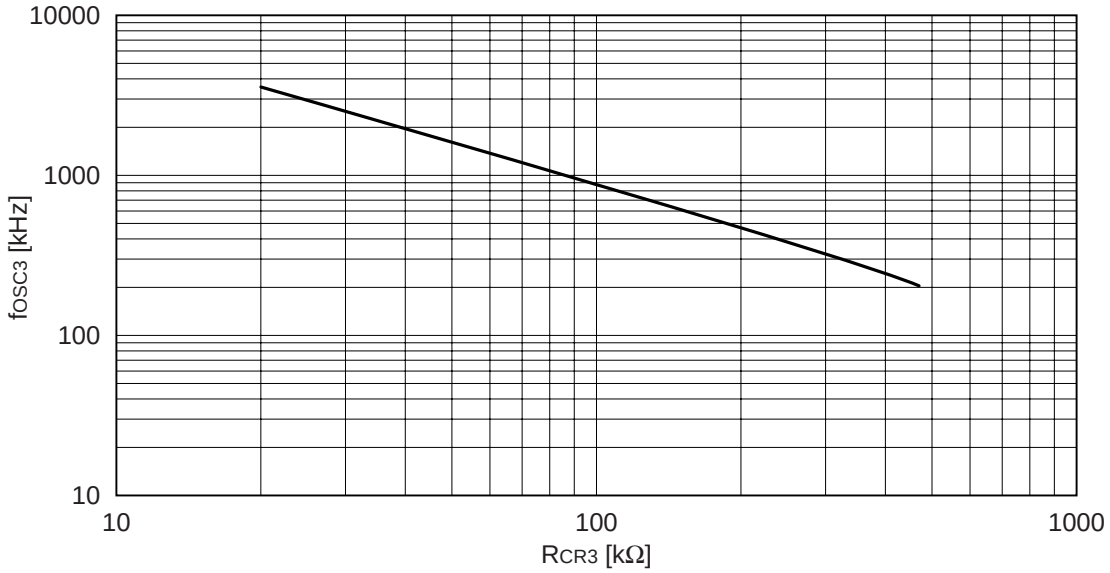
• **Oscillation frequency temperature characteristic (OSC1)**

Typ. value, R_{CR1} = 1500kΩ



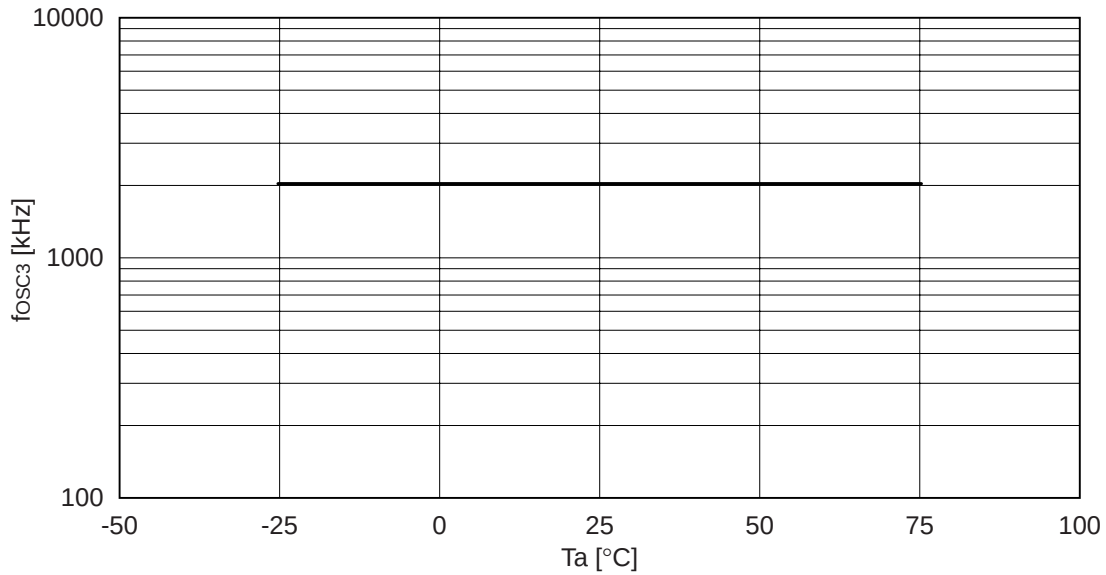
• Oscillation frequency resistor characteristic (OSC3)

Ta = 25°C, Typ. value



• Oscillation frequency temperature characteristic (OSC3)

Typ. value, R_{CR3} = 40kΩ



S1C88649

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5117

■ EPSON Electronic Devices Website
http://www.epsondevice.com

Document code: 404783000
Issue October, 2003
Printed in Japan Ⓛ