EPSON
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S1S60000
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.8

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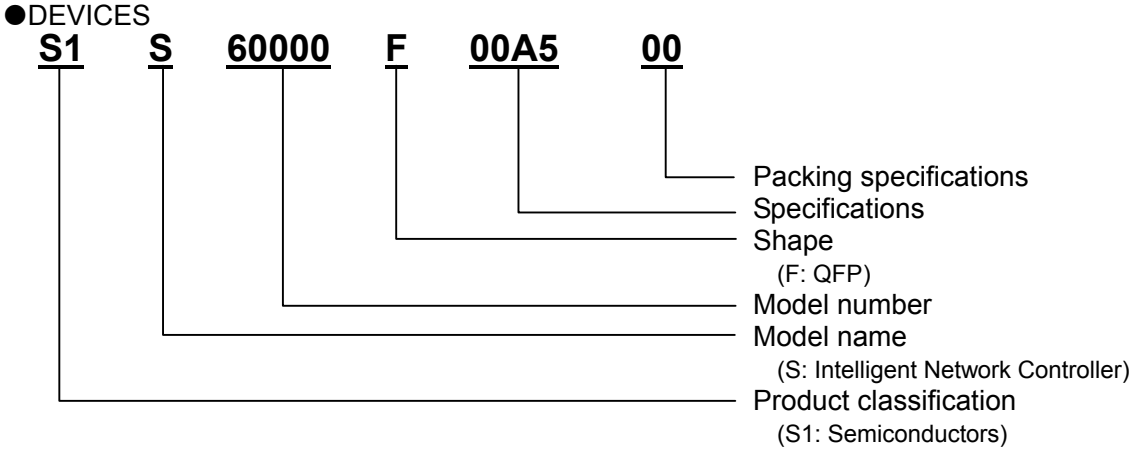

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1. DESCRIPTION

S1S60000 is an intelligent network controller equipped with the built-in protocol processing function. Simplified commands and data from the host CPU enables S1S60000 to establish TCP/IP communication thanks to its capability of internally processing protocols for TCP/IP connection including ARP, ICMP, IP, TCP and UDP. MII (Media Independent Interface) is employed for interfacing the physical layer. Just adding PHY chip designed for MII allows you to realize 10BASE-T/100BASE-TX equipment operable on networks. S1S60000 is best suited for making your 8/16 bits class CPU-featured equipment connectable to network without using a HIGH performance OS or protocol stacks provided by software vendors.
Also, it enables to connect your equipment directly to various types of host CPUs without using additional logic circuits.
There is no trouble in using it on equipment not provided with a general-purpose bus or external bus such as PCI and ISA.

1.1 Features

- Internally processes protocols for up to L4 layer of OSI model.
- Realizes network connection with simple command operations.
- Eliminates license costs thanks to the unique protocol stack.
- General purpose I/O pins and I^2C busses allow controlling hardware simply from network without using a host CPU.
- Realizes the function to convert RS232 into Ethernet and in reverse independently.
- Allows adding or changing the protocols used through rewriting of the Flash ROM.

1.2 Key Specifications

• Protocol supported	ARP, ICMP, IP, TCP, UDP, HTTP[1], DHCP, TFTP[2] and SNMP.
• Interface with physical layer	Media Independent Interface (Complied with Clause 22 of IEEE802.3) 10BASE-T/Full Duplex, 10BASE-T/Half Duplex and 100BASE-TX/Half Duplex (100BASE-TX/Full Duplex is not supported)
• Effective transfer rate	Approximately 5.5Mbps maximum (on UDP transfer)
• Host interface	8/16 bits parallel
• Directly connectable type	Includes SH-3/4, EPSON S1C33, MC68000, MC68030, Philips PR31500/PR31700, Toshiba TX3912, NEC VR4121, PC Card (PCMCIA) and ISA.
• Endian	Switching between little and big is possible.
• Host command system	EPSON Standard Code for Network
• General purpose I/O	16 maximum (Directly controllable from the network. 8 out of 16 are shared with the serial interface.)
• EEPROM Interface	3-wire and 16-bit Interface compatible with 93C46 (partially usable by user).
• I^2C bus	Master function (Multi-master and 10bit slave supported. Fast/Normal mode.) and slave function contained.
• Core CPU	EPSON S1C33240 50MHz
• Built-in Flash ROM	128KB (1KB×128 blocks)
• Power supply	+3.3V, 120mA(Max.)
• Package	QFP15-100pin

S1S60000 series (EPSON Network Controller for Embedded System) is the general name for the network ICs equipped with the built-in protocol stack. S1S60000 is the first product of S1S60000 series.

[1] Can be used only for hardware control.
[2] Can be used only for Flash ROM update from the network.

1.3 Block Diagram

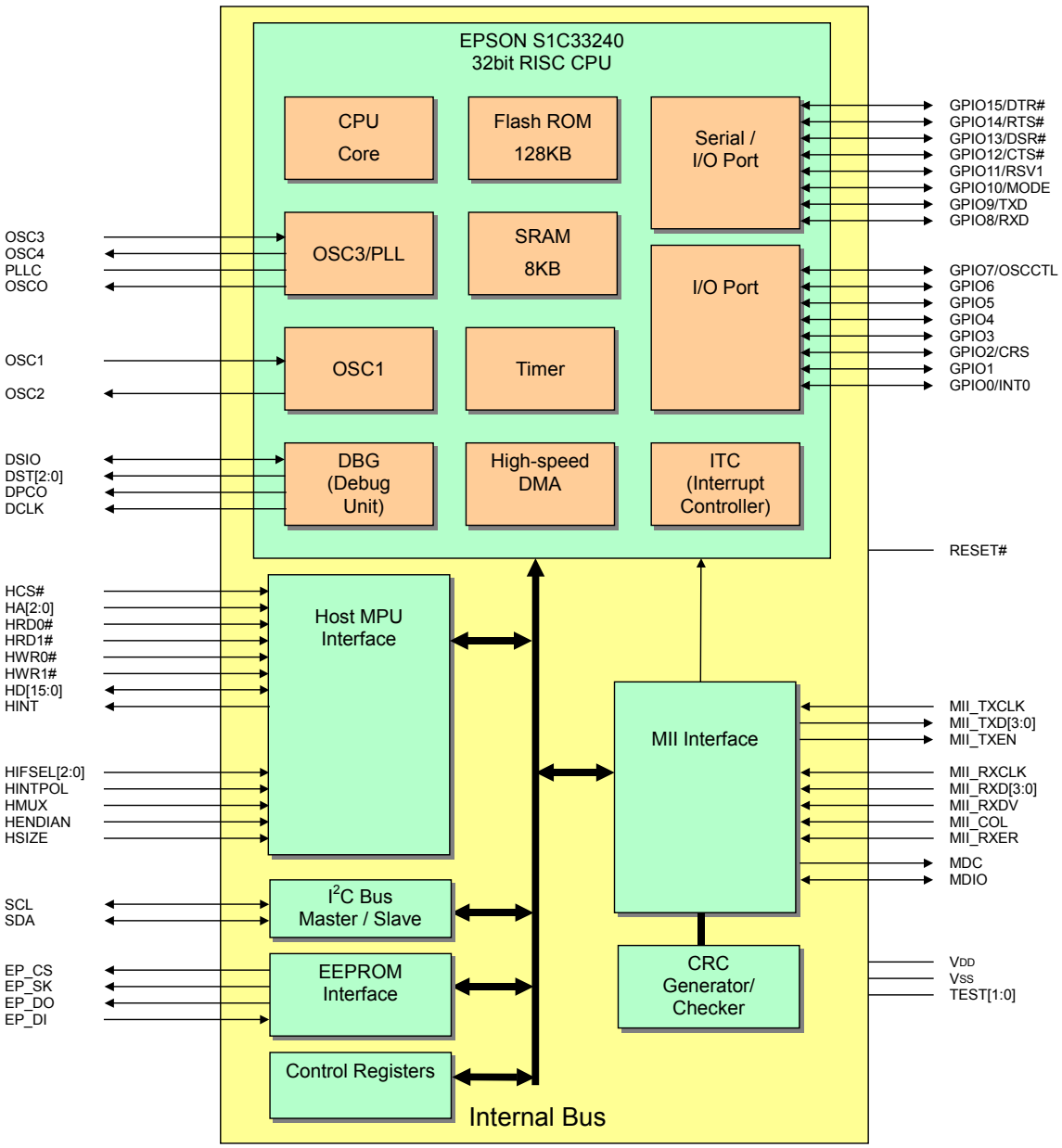
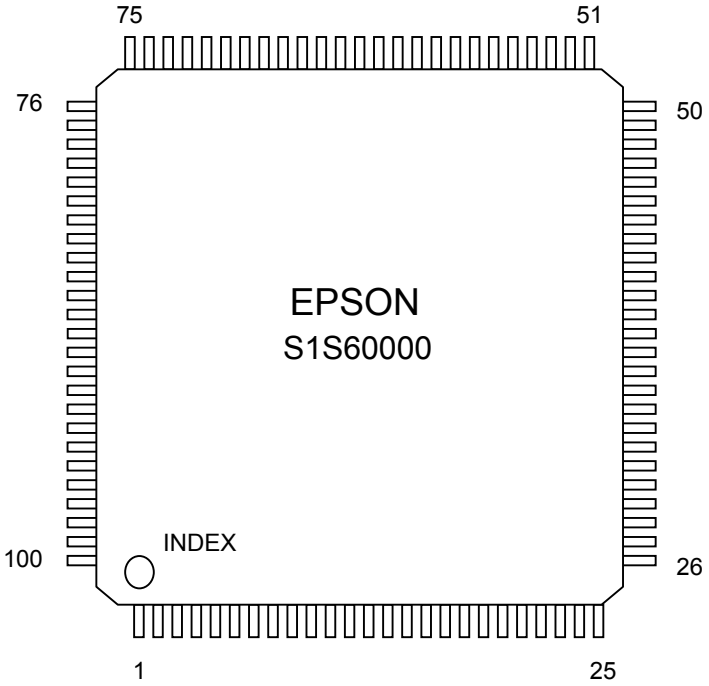


Fig.1.1 S1S60000 Block Diagram

1.4 Pin Description

1.4.1 Pin Layout

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	GPIO15/DTR#	26	MII_COL	51	HA2	76	Reserve
2	GPIO14/RTS#	27	MII_TXD3	52	VSS	77	Reserve
3	GPIO13/DSR#	28	MII_TXD2	53	HD0	78	HIFSEL0
4	GPIO12/CTS#	29	MII_TXD1	54	HD1	79	VDD
5	GPIO11/RSV1	30	MII_TXD0	55	HD2	80	PLLC
6	GPIO10/MODE	31	MII_TXEN	56	HD3	81	TEST0
7	GPIO9/TXD	32	VDD	57	HD4	82	HIFSEL1
8	GPIO8/RXD	33	MII_TXCLK	58	HD5	83	HIFSEL2
9	VSS	34	MII_RXER	59	HD6	84	HMUX
10	GPIO7/OSCCTL	35	MII_RXCLK	60	HD7	85	HINTPOL
11	GPIO6	36	MII_RXDV	61	VDD	86	TEST1
12	GPIO5	37	MII_RXD0	62	HD8	87	OSC4
13	GPIO4	38	MII_RXD1	63	HD9	88	VSS
14	GPIO3	39	MII_RXD2	64	HD10	89	OSC3
15	GPIO2/CRS	40	MII_RXD3	65	HD11	90	VDD
16	GPIO1	41	MDC	66	HD12	91	RESET#
17	GPIO0/INT0	42	MDIO	67	HD13	92	HENDIAN
18	VDD	43	OSC2	68	HD14	93	HSIZE
19	EP_CS	44	VDD	69	HD15	94	OSCO
20	EP_SK	45	VSS	70	VSS	95	DSIO
21	EP_DI	46	OSC1	71	HRD0#	96	DST0
22	EP_DO	47	VDD	72	HRD1#	97	DST1
23	SCL	48	HCS#	73	HWR0#	98	DST2
24	SDA	49	HA0	74	HWR1#	99	DPCO
25	VSS	50	HA1	75	HINT	100	DCLK

Fig.1.2 Pin Layout

1.4.2 Pin Functions

Following describes pins used on S1S60000. Symbol "#" added to a signal name indicates it a negative logic. Notations such as "[15:0]" indicate that the subject signal comprises two or more signal lines. For details of respective pins, refer to Appendix B List of Pin Characteristics.

1.4.2.1 Pin in Power Supply System

Table 1.1 List of Pins used in Power Supply System

Pin name	Pin No.	I/O	Function
VDD	18,32,44,47,61,79,90	—	Built-in logic power supply (+) Power pins. Be sure to supply +3.3V to every pin.
VSS	9,25,45,52,70,88	—	Power supply (-) GND Grounding pins. Be sure to ground every pin.

1.4.2.2 Host Interface Signals

It is the interface used to connect the host CPU. Every input pin including I/O contains a pull-up resister enabling 5V input of HCS#, HA [2:0], HD [15:0], HRD0#, HRD1#, HWR0# and HWR1#. The output is 3.3V CMOS 3-state output.

Table 1.2 List of Host Interface Signals

Pin name	Pin No.	I/O	Function
HCS#	48	I	Host Chip Select: It is the host interface access control signal. Access to the host interface is enabled as long as this signal remains LOW. This pin has a built-in pull-up resister enabling to accept 5V input.
HA[2:0]	51,50,49	I	Host Address: It is the host interface port select signal. It selects the port to be accessed while HCS# = LOW. Following shows the selectable ports. LLx: Command port (write)/Status port (read) LHx: Data port (read/write) Hxx: Flag port (read/write) These pins contain the pull-up resister enabling to accept 5V input. ※ HA0 is used for switching between the upper and lower bytes when the 8-bit interface is selected. Always keep the status LOW when the 16-bit interface is used.
HD[15:0]	69 to 62, 60 to 53	I/O	Host Data: Data signal line of the host interface. When the 8-bit interface is selected, HDATA [7:0] alone is enabled and HDATA [15:8] is not driven. These pins contain the pull-up resister enabling to accept 5V input. Output is 3.3V CMOS output.
HRD0#	71	I	Host Read/Host Write: R/W control signal of the host interface. Function changes depending on the HIFSEL[2:0] bit status in the HIFCR register. For the detail, refer to "4. Host Interface". These pins contain the pull-up resister enabling to accept 5V input.
HRD1#	72	I	
HWR0#	73	I	
HWR1#	74	I	
HINT	75	Tri	Host Interrupt: Interrupt line from S1S60000 to the host interface. Causes of interrupts are identifiable from contents of the flag port. Polarity of the interrupt is changeable by changing state of HINTPOL line at the reset. Since this signal is 3.3V/3-state output, be sure to externally connect a pull-up resister when HINTPOL=L and a pull down resister when HINTPOL=H.
HIFSEL[2:0]	83,82,78	I	Host Interface Select: It is the host interface type select signal. These pins contain the pull-up resister. For the detail, refer to "4. Host Interface".

Pin name	Pin No.	I/O	Function
HMUX	84	I	Host Bus Multiplex It sets whether the address bus and the data bus of the host interface are multiplexed in time-sharing. In case of multiplex, a latched HD[2:0] is used instead of HA[2:0]. The control line to be used for latching varies with the CPU type selected with HIFSEL. L:Multiplex bus, H:Separate bus This pin was not used in our specifications before Rev.1.3 and is set as a separate bus type when nothing is connected to. Connect this pin to GND only when a multiplex bus is used. State of this pin is acquired to the HIFCR register at reset. This pin contains the pull-up resistor.
HINTPOL	85	I	Host Interrupt Polarity Select: It is the polarity select pin for HINT when it is active. L:LOW active, H:HIGH active State of this pin is acquired to HIFCR at reset. This pin contains the pull-up resister.
HENDIAN	92	I	Host Interface Endian Select: It is the endian type select pin. Appropriately selecting the type for a CPU to be used allows switching the upper and lower data on the command or status port and on the data port. L:Little Endian, H:Big Endian State of this pin is acquired to the HIFCR register at reset. This pin contains the pull-up resistor.
HSIZE	93	I	Host Bus Size Select: It is the interface size select pin. It is used to specify the data bus size when accessing the port. L:16bit, H:8bit State of this pin is acquired to HIFCR at reset. This pin contains the pull-up resister.

1.4.2.3 MII Interface Signals

Table 1.3 List of MII Interface Signals

Pin name	Pin No.	I/O	Function
MII_RXCLK	35	I	MII Receive Clock: Receiving clock entered from PHY chip. It is the reference clock of MII_RXD [3:0], MII_RXDV. Its frequency is 2.5MHz for 10BASE-T and 25MHz for 100BASE-TX.
MII_RXD[3:0]	40 to 37	I	MII Receive Data: Receive data entered from PHY chip.
MII_RXDV	36	I	MII Receive Data Valid: Input signal from PHY chip. If it is HIGH at the positive going edge of MII_RXCLK, MII_RXD [3:0] is valid.
MII_TXCLK	33	I	MII Transmit Clock: Transmit clock entered from PHY chip. It is the reference clock of MII_TXD [3:0], MII_TXEN. Its frequency is 2.5MHz for 10BASE-T and 25MHz for 100BASE-TX.
MII_TXD[3:0]	27 to 30	O	MII Transmit Data: Transmit data output to PHY chip.
MII_TXEN	31	O	MII Transmit Enable: Output signal to PHY chip. If it is HIGH at the positive going edge of MII_TXCLK, MII_TXD[3:0] is valid.
MII_RXER	34	I	MII Receive Error: Input signal from PHY chip. This signal indicates that receive data contained an error. It is valid on 100BASE-TX alone and ignored on 10BASE-T.
MII_COL	26	I	MII Collision Detect: It indicates that collision of signals occurred during Half Duplex communication.
MDC	41	O	MII Management Interface Clock: It is the clock used to set up function of PHY chip as well as control it and read its status. This signal is output from S1S60000. MDIO pin sends or receives data in synchronization with this signal.

Pin name	Pin No.	I/O	Function
MDIO	42	I/O	MII Management Interface Data I/O This data is used to set up function of PHY chip as well as control it and read its status. Data for the function setup and control of PHY chip is sent from this pin to PHY chip in synchronization with MDC. When reading status of PHY chip, data from PHY chip is read from this pin in synchronization with MDC. This pin must be connected to a pull-up resister externally.
GPIO2/CRS	15	I	MII Carrier Sense When the alternate function of GPIO2 is selected, this pin functions as CRS input pin to enter state of the carrier in Half Duplex communication. It is not used when Half Duplex communication is not employed.

1.4.2.4 External Device Control Signals

Table 1.4 External Device Control Pins

Pin name	Pin No.	I/O	Function
EP_CS	19	O	EEPROM Chip Select: It is the EEPROM chip select pin.
EP_SK	20	O	EEPROM Serial Clock: It is the EEPROM clock pin.
EP_DI	21	I	EEPROM Data In: It is the EEPROM data input pin.
EP_DO	22	O	EEPROM Data Out: It is the EEPROM data output pin.
SCL	23	OD/I	I^2C Serial Clock: I^2C bus serial clock pin. When the master is selected, it is input signal and it becomes output signal when the slave is selected. Since output of this pin is open drain, a pull-up resister must be provided externally. Select an optimum pull-up resister value taking into consideration of load on the bus as well as noises.
SDA	24	OD/I	I^2C Serial Data: I^2C bus data input/output pin. It is a bi-directional signal used to input or output data and ACK. Since output of this pin is open drain, a pull-up resister must be provided externally. Select an optimum pull-up resister value taking into consideration of load on the bus as well as noises.

1.4.2.5 General Purpose Input and Output Pins

Table 1.5 List of General Purpose Input and Output Pins

Pin name	Pin No.	I/O	Function
GPIO0/INT0	17	I/O	General Purpose I/O [7:0]: They are general purpose input/output pins. They accept 5V input. GPIO0 is used as an interrupt pin and allows sending interrupt notice to a previously specified destination. GPIO2 is used as the CRS input pin in Half Duplex communication. GPIO7 can be used as the OSC control pin in the sleep mode. For the detail, refer to Chapter 5.3. After the hardware is reset, all pins are used for input only.
GPIO1	16	I/O	
GPIO2/CRS	15	I/O	
GPIO3	14	I/O	
GPIO4	13	I/O	
GPIO5	12	I/O	
GPIO6	11	I/O	
GPIO7/OSCCTL	10	I/O	
GPIO8/RXD	8	I/O	General Purpose I/O [15:8]: General-purpose input/output pin for 3.3V CMOS level and Schimitt input. They can be used as start-stop synchronous serial terminals by setting GPLLT register. For details, refer to Chapter 2.3. After the hardware reset, all pins are used for input only.
GPIO9/TXD	7	I/O	
GPIO10/MODE	6	I/O	
GPIO11/RSV1	5	I/O	
GPIO12/CTS#	4	I/O	
GPIO13/DSR#	3	I/O	
GPIO14/RTS#	2	I/O	
GPIO15/DTR#	1	I/O	

1.4.2.6 Clock Generator Pins

Table 1.6 List of Clock Generator Pins

Pin name	Pin No.	I/O	Function
OSC1	46	I	OSC1 clock pin When using the sleep mode in the power management, it is used to connect 32.768kHz crystal. S1S60000 in the sleep mode is operated with this clock. When the sleep mode is not used, connect OSC1 to VSS and open OSC2.
OSC2	43	O	
OSC3	89	I	OSC3 clock pin (for oscillation of crystal/ceramics or for input of external clock) Operating clock oscillation pin for S1S60000. A crystal transducer of 10 to 25MHz is connected. When entering an external clock, input a clock of 10 to 25MHz to OSC3 and make OSC4 open. ※ It is advised to use a clock of 25MHz normally. When any other frequency is used, communication with 100BASE-TX and the power save mode may become unavailable.
OSC4	87	O	
OSCO	94	O	OSC output pin It is used to generate buffered output of OSC3 input. Frequency of output from this pin is the same as that OSC3 input. Supplying clock to PHY chip from this pin helps reducing number of oscillators for PHY. Note: When supplying clock from this pin, be sure to use a crystal oscillator that can meet the frequency accuracy required by PHY chip. Normally, 50ppm maximum accuracy is required.
PLLC	80	—	PLL capacitor connecting pin It is the capacitor connecting pin for doubling OSC3 frequency with the internal PLL. Be sure to connect R and C shown in Fig.1.3. Unless they are connected, this IC does not operate normally.

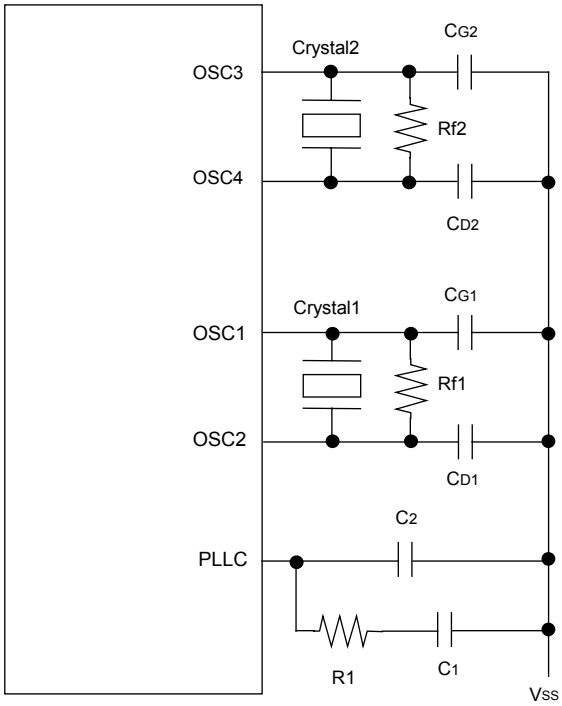


Fig.1.3 Clock Generator Connection Diagram

Crystal1	Crystal transducer	32.768kHz Ci (Max.) =34kΩ
C_{G1}	Gate capacitance	10pF
C_{D1}	Drain capacitance	10pF
Rf1	Feedback resistance	10MΩ
Crystal2	Crystal transducer	25MHz
C_{G2}	Gate capacitance	10pF
C_{D2}	Drain capacitance	10pF
Rf2	Feedback resistance	1MΩ
R1	Resister	4.7kΩ
C_1	Capacitor	100pF
C_2	Capacitor	5pF

1.4.2.7 Other Pins

Table 1.7 Other Pins

Pin name	Pin No.	I/O	Function
DSIO	95	I/O	These pins are used for communication with the debug tool ICD33. ICD33 is mainly use for rewriting flash memory on S1S60000. It should not be connected to any equipment other than above. If these pins are used in an environment full of noise, IC could go into debug state due to the level fluctuation of the DSIO pin and this results into stopping the normal operation. In that case, attach the resister lower than 10kΩ to the outside and pull up to VDD.
DST[2:0]	98,97,96	O	
DPCO	99	O	
DCLK	100	O	
RESET#	91	I	Hardware Reset Input: S1S60000 is reset as the LOW level is input. This pin contains the pull-up resister.
TEST1,TEST0	86,81	I	Test Input: Testing pins for this IC. They are made open when operated normally. They contain the pull-down resistor.
Reserve	77,76	—	These pins are reserved for future expansion. Normally, do not connect.

2. HARDWARE SPECIFICATIONS

2.1 Core CPU

Seiko Epson original 32 bits microcomputer S1C33240 or equivalent is employed for the core CPU. ADC, however, is not built in it.
CPU operating clock, always working identically with the internal bus, is initially set to twice the OSC3. Setting PSEN bit (11 bit) of GENCR register reduces it to 1/4 clock comparing when it operates normally. This arrangement helps reducing operating current.
The inside is processed according to Little Endian.

2.1.1 ROM and Boot Address

S1S60000 contains a 128Kbytes Flash ROM. After the reset, it is started from 0×0C00000, namely area 10 Flash ROM area. Of these 128Kbytes, 127Kbytes are for the system firmware area, while the remaining 1Kbyte is for the user area. The user area ranges from 0×C1FC00 to 0×C1FFFF.
Rewriting in the system firmware is done from the debug serial pin and network by using a special tool and program. To rewrite in the user area, the debug serial pin or host interface can be used. Also, to rewrite in the user area, the debug serial pin or the host interface is used and the host interface command is executed, and it is not necessary to designate an absolute address. However, this area can be used only as a data area. This area cannot store a program for execution.

2.1.2 RAM

S1S60000 contains an 8Kbytes RAM. Device size of this built-in RAM is 32 bits enabling to read/write data of a byte, half-word or word in a single cycle. Since this RAM is exclusively used by S1S60000, user can't operate it.

2.2 Peripheral Circuits

Among the peripheral blocks of the built-in core CPU S1C33240, S1S60000 uses the following built-in peripheral circuits. For details of respective peripheral circuits, refer to "S1C33 Family ASIC Macro Manual".

- C33 core block
  CPU 32-bit RISC type CPU S1C33000
  BCU Bus control unit
  ITC Interrupt controller
  CLG Clock generator
  DBG Functional block for debugging featured with ICD33 (In-Circuit Debugger for S1C33 Family)

- C33 peripheral circuits block
  Pre-scaler Used to set the clock for peripheral circuits programmable
  16 bits programmable timer
  Serial interface
  Input/output port
  Elapsed timer
  C33DMA block
  HSDMA (HIGH-speed DMA) 4-channel

The I/O memory map contained S1S60000 is essentially the same as that of S1C33240. For the detail, refer to "S1C33240 Technical Manual".

2.3 Serial Interface

GPIO[15:8] become the serial interface pins on both of following two conditions.

- GPALT register bit [15:8] = FFh
- GENCR register bit [10:8] (SERCONF) = “000” or “010” or “011”

Under the above condition, the operation mode changes depending on the status of the SERCONF pin and the GPIO10 pin (MODE pins) settings.
Table 2.1 shows relations between settings and operation modes.

Table 2.1 Setting of Serial Interface O.eration Modes

GPALT[15:8]	SERCONF[2:0]	MODE	Mode	Communication conditions
FFh	000	—	Hardware control mode	Fixed (*1)
	010	HIGH	Hardware control mode	Fixed (*1)
		LOW	Serial emulation mode (Active Open)	Variable (*2)
	011	HIGH	Hardware control mode	Fixed (*1)
		LOW	Serial emulation mode (Passive Open)	Variable (*2)
	Other than above	—	Reserved. Do not set any other value.	—
00h	—	—	Used as GPIO[15:8]	—
Other than above	—	—	Disabled. Does not operate in either mode.	—

*1: Start-Stop synchronous serial, 9600 baud, 8-bit data, 1 stop-bit, no parity, no flow control.
*2: Set in the SERMODE register

Note: After selecting each mode, do no access the serial interface for 100ms.

2.3.1 Hardware Control Mode

When the “hardware control mode” mentioned in Table 2.1 is set, the serial interface operates with the hardware control mode. Use of this mode allows confirming and changing each hardware status (EEPROM, I^2C, GPIO) from the serial interface. Use this mode to change the status of the EEPROM when the host CPU is not connected, or when you need to confirm the status of GPIO from the serial interface.
When the hardware control mode is set, the communication conditions are fixed as follows.

Start-Stop synchronous serial, 9600 baud, 8-bit data, 1 stop bit, no parity, no flow control

For details on this mode, refer to Chapter 5.1.4.

2.3.2 Serial Emulation Mode

When the "serial emulation mode" mentioned in Table 2.1 is set, the serial interface operates in the serial emulation mode. In this mode, serial interface transmit and receive data are transmitted and received between destinations connected to the network (S232 is converted to Ethernet and vice versa). This mode is an especially effective way for a device with a conventional RS232 interface to exchange data with another device on the Ethernet. A TCP/IP connection is used. By enabling RTC/CTS control, flow control is also possible. The communication conditions are set up by the SERMODE register.

[Establishing connection]

When GPIO [15:8] is set to the serial emulation mode, the S1S60000 performs processing equivalent to when a System Open command and TCP Open command are transmitted from the host interface. The contents of the SOPAR register are used as parameters by the System Open command. With TCP Open, if SERCONF (bit[10:8] = 010 and Active Open, 011 then Passive Open processing is performed.

In Active Open (when the client is operating), a connection request is issued to establish connection for the IP address (set by the DADR0H, DADR0L register) of the address preset in the EEPROM and the port (set by the PORT register). When the connection is later terminated by the destination, reconnection is performed automatically.

In Passive Open (when the server is operating) the server opens the self-preset communication port (set by the PORT register) and waits for the connection (listen status). Connection is established when it is requested from outside.

[Transmission from Serial Interface to Network]

Serial data received from the serial interface is output to the network when no data is received during the transfer time of about 100 data after the last data was received or when 1 packet (536 bytes) of data was received.

[Transmission from Network to Serial Interface]

Data received from the network is transmitted to the serial interface after an error check is executed and header information is removed inside S1S60000.

Functions of each pin are as shown in Table 2.2.

Table 2.2 Pin Functions when Start-Stop Synchronous Serial is selected

Pin	Pin	Name	In/Out	Function
GPIO15	1	DTR#	O	Data Terminal Ready Indicates that data receiving is enabled. It is a LOW active signal. Enters the LOW status after initialization in the serial emulation mode. Normally HIGH status in the hardware control mode.
GPIO14	2	RTS#	O	Request to Send Indicates that data transmission is enabled. It is a LOW active signal. Enters the LOW status when receiving is possible in the serial emulation mode. Hardware control mode is normally LOW status.
GPIO13	3	DSR#	I	Data Set Ready Input of the state that transmission from outside is enabled. Currently not used.
GPIO12	4	CTS#	I	Clear to Send Input of the state that receive from outside is enabled. It is a LOW active signal. When this pin goes HIGH, transmission is temporarily suspended, and when it returns to LOW, transmission is resumed. Since this operation is controlled according to the interrupt-based software control, the time from the transmission stop to the resumption after signal change is uncertain. So, the external device is requested to start the control when the buffer capacity is sufficient to some extent
GPIO11	5	—	—	—
GPIO10	6	MODE	I	Mode Select Used to switch over normal/hardware control modes. Be sure to set this pin to LOW in the normal mode.
GPIO9	7	TXD	O	Transmit Data Serial transmit data
GPIO8	8	RXD	I	Receive Sata Serial transmit data

TXD and RXD are start-stop synchronous serial pins to be transmitted/received by use of the serial interface Ch.0 function of the built-in S1C33240. For details, refer to the serial interface specifications in the technical manual for the S1C33240. Other control lines are controlled by the software. CTS# signals are processed by internal interruptions.

2.4 Power Supply

2.4.1 Operating Voltage

S1S60000 operates with the voltage supplid across V_{DD} and V_{SS}. This operating voltage is as shown below.

V_{DD} = 3.3±0.3V(V_{SS} = GND)

Note: S1S60000 has 7 V_{DD} pins and 6 V_{SS} pins. Be sure to connect every pin to the power supply so that any of them may not become open.

2.5 Power on Reset

Be sure to implement initial reset at powering on in order to ensure normal start of S1S60000. Schmitt input is applied RESET#.

Operation of OSC3 oscillation circuit is started by the initial reset (RESET#=LOW) and then CPU is started by OSC3 clock at the positive going edge of the reset signal. OSC3 oscillation circuit takes some time until its oscillation stabilizes(V_{DD}=3V, the time required for stabilized oscillation under normal operation condition: 10ms Max.). Thus, in order to ensure positive start of CPU, be sure to release the initial reset only after this time has been elapsed. Make sure that length of the initial reset pulse is longer than the above oscillation stabilizing time. Fig.2.1 shows the timing chart at the power on reset.

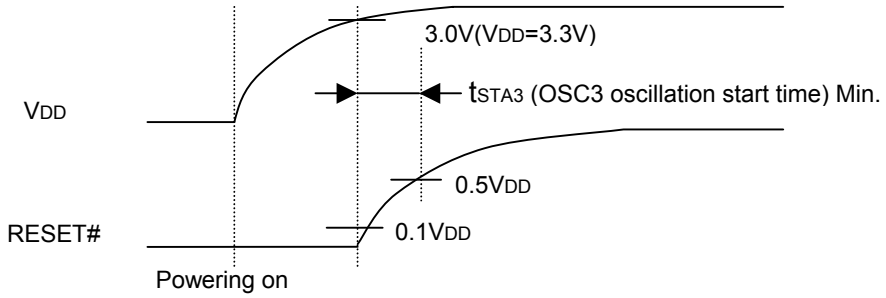


Fig.2.1 Power on Reset Timing

After powering on, maintain RESET# pin below 0.1 • V_{DD} (LOW level) until supply voltage reaches the oscillation start voltage (3.0V) or above. It is also required to maintain RESET# pin below 0.5 • V_{DD} until oscillation of OSC3 oscillation circuit is stabilized.

Note: Oscillation start time of OSC3 oscillation circuit depends on the device substrate pattern used as well as the operating environment. So you must be sure to provide enough time before releasing the reset.

• **Reset pulse**
When S1S60000 is in operation, it is possible to implement the initial reset by inputting LOW level pulse to the RESET# pin.
In this case, however, the pulse width used must be greater than the minimum reset pulse width listed in the "AC Characteristics".
When applying reset pulse while OSC3 oscillation circuit is not in operation, RESET# pin must be maintained at LOW level for a period longer than the oscillation stabilization time. It is the same requirement as that for the power on reset.

• **Check of Resetting Operation**
When S1S60000 hardware started operating after normal resetting, signals EP_SK and EP_CS change for checking connection of the EEPROM. also, when the S1S60000 software started operating, signals MII_MDC and MII_MDIO change for checking connection of the PHY chip. If these signals do not change, check the power supply, the OSC3 clock, state of the RESET# pin and setting of the PLLC pin.
When the initialization with the firmware completes, the BOOT status (000Bh) can be read from the host interface. (But, this does not apply when HIFSEL [2:0] pin is "111" and HIFSEL [2:0] of the HIFCR register is "111." In this setting, it is understood that "the host interface is not connected.")

2.6 OSC3 Clock

Operating clock for S1S60000 is entered to OSC3 pin. For the internal bus and CPU operation, the clock entered from OSC3 is used after it has been doubled. Normally, 25MHz clock is used. The lowest frequency allowed to input is 10MHz.
While the power save mode is turned on, the internal bus clock and CPU operating clock is reduced to 1/4 of the normal operation (1/2 of that input from OSC3).
When operating S1S60000 on 100BASE-TX, be sure to enter 25MHz to OSC3 and operate S1S60000 in the normal mode. Note that it cannot operate in the power saving mode.

3. NETWORK INTERFACE

3.1 MII Interface

S1S60000 employs MII (Media Independent Interface) for connection with the physical layer (PHY chip) enabling it to connect various network PHY chips designed for MII. For the detail of MII, refer to IEEE 802.3 Clause 22 (IEEE 802.3μ). However, your attention is required on the following points.

• CRS (Carrier Sense) signal
This signal is not used in Full Duplex communication. Connect CRS signal to GPIO2 pin only when Half Duplex communication is to take place. Also, when setting PHY forcibly to Half Duplex communication, Half Duplex must be set on GENCR.

• TX_ER signal
This signal is used to propagate the error received with RX_ER. This signal, however, is not used on S1S60000 since it does have a repeating function.

Fig.3.1 and 3.2 show MII transmit waveform and MII receive waveform, respectively.
In transmission, MII_TXEN is set to HIGH level and then level of MII_TXD is changed after MII_TXCLK has reached HIGH level. In Half Duplex communication, interrupt occurs in S1S60000 as MII_COL goes HIGH level thereby forcing MII_TXEN to LOW level and suspending transmission. Then transmission is resumed after a predetermined time.
In receiving, after MII_RXDV has reached HIGH level, MII_RXD is acquired at positive-going edge of MII_RXCLK. If MII_RXER goes HIGH level while communicating with 100BASE-TX, FCS error is set after receiving is complete and the received frames are disposed.

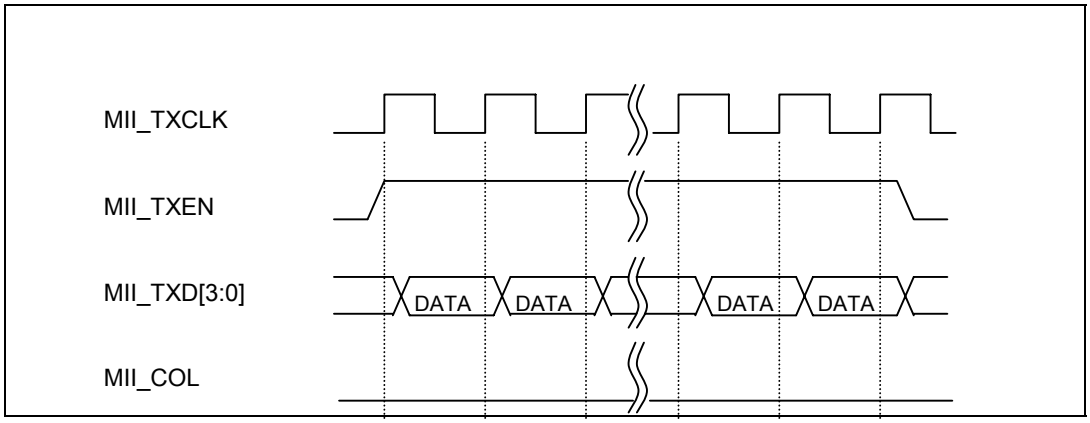


Fig.3.1 MII Transmit Waveform

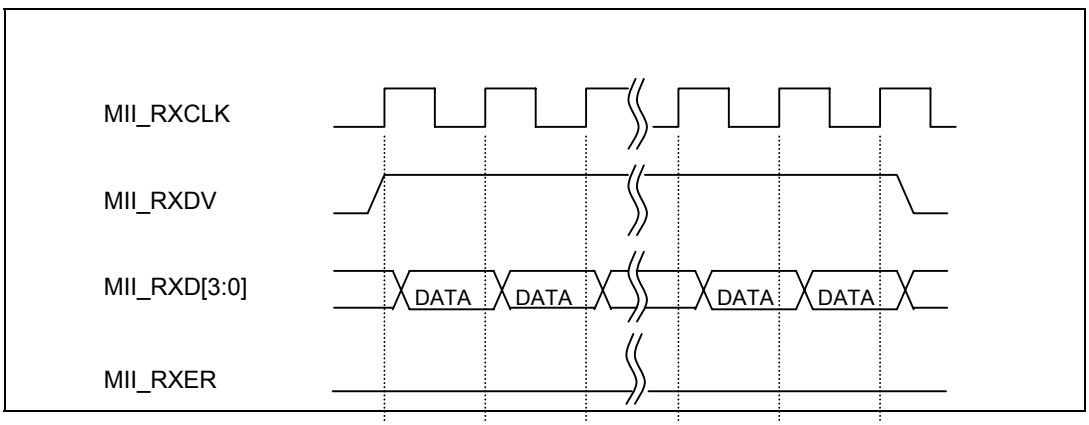


Fig.3.2 MII Receive Waveform

3.2 Management Interface

S1S60000 supports MII management interface. It can write or read registers in PHY through this interface. Fig.3.3 and 3.4 show the waveforms in the read and write operations, respectively.

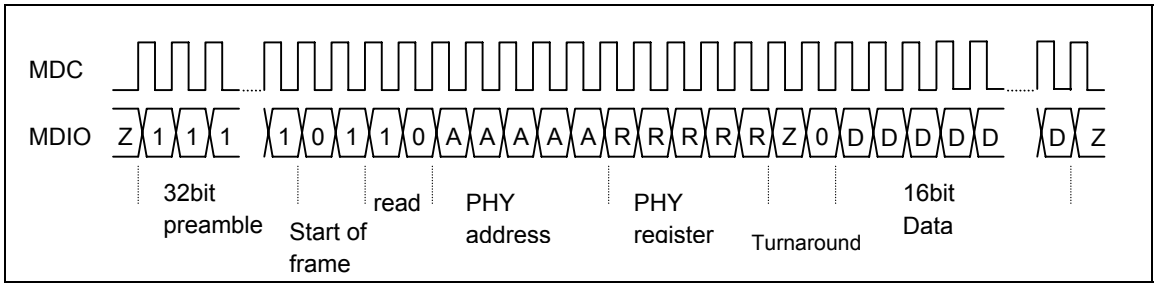


Fig.3.3 MII Management Interface Read Operation

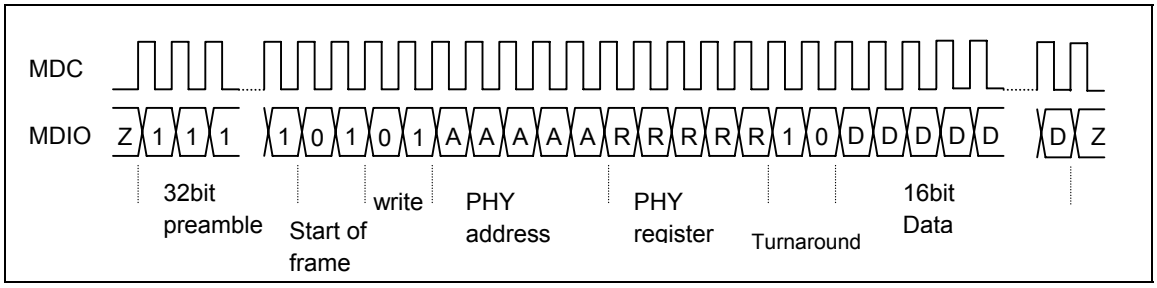


Fig.3.4 MII Management Interface Write Operation

3.3 Connecting PHY Chips

Fig.3.5 shows connection between S1S60000 and PHY chips.
You do not have to connect CRS for Full Duplex communication only. Also, TX_ER signal is not connected.

[Important]
Make necessary setting so that the PHY chip address becomes 0×01 all the time. Operation cannot be guaranteed if set to any other setting.

In the normal operation and the power save mode, OSC pin on S1S60000 outputs the signal being formed after buffering OSC3 input. Thus connecting a 25MHz crystal oscillator to OSC3 input and connecting OSCO to the clock of PHY allows you operate both S1S60000 and PHY with a single crystal oscillator.

Note: Before supplying clock form OSCO to PHY, make sure that it meets the clock accuracy required by PHY. Also make sure that length of the pattern connected is minimized and the clock waveform satisfies requirements of the PHY specification.

If you are using Firmware Version 1, Revision 22 (product number: S1S60000F00A500, IC marking: S1S60000F00A5) or later, it is not necessary to make the ANEGR register settings described below. The setting value will be ignored. When using a product earlier than Revision 22, set ANEGR following the description written below. (Realtek Company's RTL8201L is available only on Firmware Version 1, Revision 22 or later)

After deciding a PHY chip to be used, acquire result of auto negotiation, speed (100BASE/10BASE) established by link and bit information showing the mode (Full Duplex/ Half Duplex) and arrange so that they are reflected to the ANEGR register.

• Acquiring Method of ANEGR Register Value
(1) Seek for a register in which result of auto negotiation can be stored. In general, it is available between 16 and 19 or at 24 or 25.
(2) Set the value obtained by subtracting 16 from the register offset to LSOFF bit.
(3) Set DINV and SINV according to the result storing method.
(4) Set each bit of DUPLEX and SPEED depending on the result store bit position.

Followings are recommended for connection with S1S60000.

Maker name	Model number	ANEGR value
ICS	ICS1893Y-10	10EFh
TDK	78Q2120-64T	20BAh

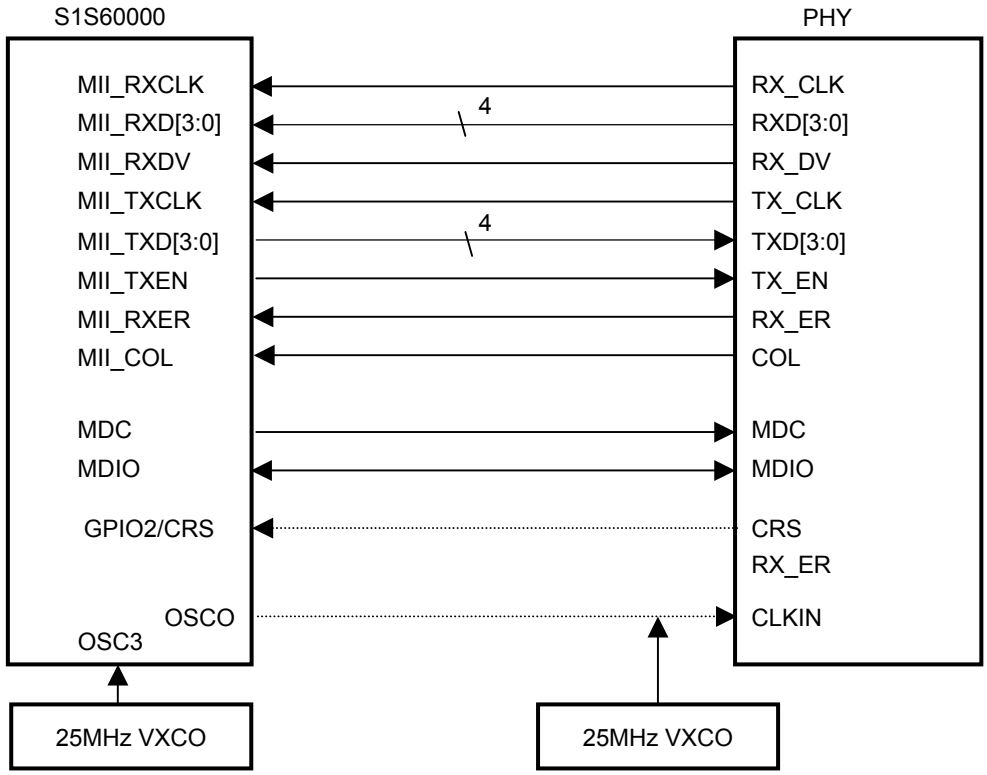


Fig.3.5 Connection between S1S60000 and PHY

3.4 Communication Mode

When using S1S60000, it is normally recommended to select 10BASE-T/Full Duplex mode. S1S60000 does not support 100BASE-TX/Full Duplex communication.
When the automatic negotiation function of the PHY chip is used, the S1S60000 performs auto-negotiation to select the communication mode in the following order: 1) 100Base TX/half-duplex, 2) 10Base T/full-duplex, 3) 10Base T/half-duplex. Communication is performed in the mode of the first link established.
The PHYMODE register can be set to limit the link conditions.

Communication Mode Setup Flow

(1) The auto-negotiation is executed selecting 100BASE-TX/Half Duplex as the target. If it ends successfully, 100BASE-TX/ Half Duplex is employed and the setup process is ended. Otherwise, the negotiation continues to the next step.
(2) The auto-negotiation is started selecting 10BASE-T/Full Duplex as the target. If it ends successfully, 10BASE-T/Full Duplex is employed and the setup process is ended.
Otherwise, the negotiation continues to the next step.
(3) The auto-negotiation is executed selecting 10BASE-T/Half Duplex as the target. If it ends successfully, 10BASE-T/Half Duplex is employed. The setup process is ended. (Even when this is not applicable to auto-negotiation, it is specified that link is made in this state, and it is linked here if the connection is correct.)
(4) If all negotiations ended unsuccessfully, S1S60000 judges that the link has not been established.

4. HOST INTERFACE

The host interface is for connecting S1S60000 to external CPU and is of 8-bit or 16-bit parallel type. The host interface allows connecting six types of CPUs directly depending on its setting.

4.1 Control Signals

Table 4.1 shows the host interface signals. Every input pin including I/O pins contain a pull-up resister enabling then to accept 5V input is acceptable for HCS#, HA [2:0], HD [15:0], HRD0#, HRD1#, HWR0# and HWR1#. Output is 3.3V CMOS or 3-state output. When not using the host interface (when implementing GPIO control independently, for instance), be sure to leave the every host interface signal unconnected.

Table 4.1 Host Interface Signals

Pin name	I/O	Function
HCS#	I	It is the access enable signal. Access available as it goes LOW.
HA[2:0]	I	Port select signal
HD[15:0]	I/O	Input/output data bus
HRD0#	I	A R/W control signal. Its function depends on state of HIFSEL [2:0].
HRD1#	I	A R/W control signal. Its function depends on state of HIFSEL [2:0].
HWR0#	I	A R/W control signal. Its function depends on state of HIFSEL [2:0].
HWR1#	I	A R/W control signal. Its function depends on state of HIFSEL [2:0].
HINT	Tri	It is the interrupt signal. Polarity is settable.
HIFSEL[2:0]	I	Host interface type select signal
HMUX	I	Host interface bus multiplex (enabled at the reset) L:Multiplex bus, H:Separate bus
HINTPOL	I	Host interrupt line polarity select (enabled at the reset) L:LOW active, H:HIGH active
HENDIAN	I	Host interface endian select (enabled at the reset) L:Little Endian, H:Big Endian
HSIZE	I	Host interface size select (enabled at the reset) L:16bit, H:8bit

Tri: 3-state output

When HCS# is LOW, an access port is selected depending on the state of HA [2:0]. Following shows the port assignment.

(1) When 16-bit interface is selected

HA[2:0]	Access port
LLL	Command port (Write) / Status port (Read)
LHL	Data port
HxL	Flag port

Note: The flag port outputs the same contents to the upper and lower 8 bits.

(2) When 8-bit interface is selected

HA[2:0]	Access port
LLL	Lower command port (Write) / Lower status port (Read)
LLH	Upper command port (Write) /Upper status port (Read)
LHL	Lower data port
LHH	Upper data port
Hxx	Flag port

Note: When the 8-bit interface is used, data transfer of one time is completed as access is made to both the upper and lower ports. The order in accessing the upper and lower ports is optional. The flag port does not have the upper or lower port.

4.2 Host Interface Port

4.2.1 Command Port

This port is used to send a command from the host CPU to S1S60000. Since this port is 16-bit wide, two times of access (the upper and lower addresses) are required when the 8-bit interface is used. For detail of the commands, refer to the "S1S60000 Series Host I/F Manual".

4.2.2 Status Port

This port is used to return a status from S1S60000 to the host CPU. Since this port is 16-bit wide, two times of access (the upper and lower addresses) are required when the 8-bit interface is used. For detail, refer to the "S1S60000 Series Host I/F Manual".

4.2.3 Data Port

This port is used to transmit and receive data between the host CPU and S1S60000. Since this port is 16-bit wide, two accesses to the upper address and to the lower address are required when an 8-bit interface is used. Option segments added to a command or status are also transmitted and received through this port. For the detail of options, refer to the "S1S60000 Series Host I/F Manual."
Data are written from the host CPU to the data port only after the WRITE status is returned to the SEND command. At the time, be sure to check the states of HSTREN (bit4) and H2CDV/H2CDC (bit3) of the flag port after each writing before another writing.

4.2.4 Flag Port

This port is used to indicate how a host interface-related command, status or data is processed.
The state of bit [1:0] is the factor that activates the HINT signal, and when any of the bits is 1, the HINT signal goes active (polarity of the signal is changeable). Reading status or data on the host side clears corresponding factors, and when all factors are cleared, the HINT signal turns to inactive. Also, the data processing state inside S1S60000 is checked from the host side according to the state of bit[3:2].
This port is 8-bit wide. Thus, when the 16-bit interface is used or when two times of access (to the upper and lower addresses) are made from the 8-bit interface, the same data is read to the upper and lower bits.

Table 4.2 Flag Port Bit Assignment

bit	Description
7:5	Not used. Value is 0.
4	HSTREN State of data port receiving circuit (R/O) 0: Data port receiving circuit is disabled. 1: Data port receiving circuit is enabled.
3	H2CDV Write data processing state (R/O) 0: Data write available 1: Waiting for data read
2	H2CCV Command processing state (R/O) 0: Command write is available. 1: Waiting processing of command.
1	C2HDV Read data preparation state (R/O) 0: Data to be read is not present. 1: Data to be read is present. (It is cleared as data is read.)
0	C2HSV Status preparation state (R/O) 0: Status to be read is not present. 1: Status to be read is present. (It is cleared as status is read.)

Note: When the host interface is 16 bits wide, the same information is output to bit [15:8] and bit [7:0]. Writing is enabled to bit [7:0] alone.

4.3 Host Interface Type

The host interface type is selected at hardware reset according to the HIFSEL[2:0] pin status as well as the HIFCR data in the EEPROM. Table 4.3 shows assignment of the host interface type.

Table 4.3 Host Interface Type

HIFSEL[2:0]	Type	Example of host CPUs (8/16bit bus)
000	Type 0	Renesas Technology SH-3/4, EPSON S1C33
001	Type 1	MC68000/10
010	Type 2	MC68030/40
011	Type 3	Generic
100	Type 4	Reserved
101	Type 5	MIPS, ISA, NEC VR4121(16bit)
110	Type 6	PCMCIA, Philips PR31500/PR31700, Toshiba TX3912
111	EEPROM	A type is selected in the range of Type0 to Type6 depending on HIFCR data of EEPROM

Type0 This type of interface controls access by use of the independent write signals (byte basis) and a single read signal. Renesas Technology SH-3/4 and EPSON S1C33 belong to this type.

Type1 It controls access by combining the upper/lower byte signal (such as UDS#/LDS#) and the read/write signal. Freescale Semiconductor's MC68000 belongs to this type. In this case, connect the upper byte select signal to HWR0#, the lower byte select signal to HWR1# and the read/write signal to HRD1#. And maintain RD0# unconnected.

Type2 It controls access by combining the data transfer size indicate signal and the read/write signal. MC68030/40 belong to this type. In this case, connect SIZ0 signal to HWR0#, SIZ1 signal to HRD0# and the read/write signal to HRD1#. And maintain HWR1# unconnected.

Type3 It is the general-purpose type. When a given host CPU does not fit into any type, it is used to connect such host CPU by use of an externally generated access signal. In this case, connect the lower byte write signal to HWR0#, the upper byte write signal to HWR1#, the lower byte read signal to HRD0# and the upper byte read signal to HRD1#.

Type4 This type is reserved for future extension. Don't select it.

Type5 It controls access by using the upper/lower byte select signal (composed of two or more signals) plus the independent read signal and the write signals. MIPS and ISA bus belong to this type. In this case, connect the write signal to HWR0#, the upper byte select signal to HWR1# and the read signal to HRD0#. Maintain RD1# unconnected.

Type6 It controls access by use of the independent byte enable signal, independent read enable signal and write signal. PCMCIA interface belongs to this type. In this case, connect the write signal to HWR0#, the read signal to HRD0# and the lower byte enable signal to HRD1#.

EEPROM It selects a type according to HIFCR data of the serial EEPROM. A type is selectable in the range of Type0 to Type6. When EEPROM data is "111" or when EEPROM is not connected, S1S60000 assumes that a host CPU is unconnected.

• Multiplex Bus
Some CPUs use parts or the whole of address lines commonly with data bus in time sharing. Before such CPUs are connected to S1S60000, it is necessary to make HMUX pin LOW and to implement multiplex bus setting. After the setting, a signal that latched HD[2:0] is used as the address instead of HA[2:0]. For the latch signal, use a signal that becomes HIGH during address output period and that turns to LOW while the address is settled, and input it to the following signal lines for each type:
Type0=HRD1#, Type1=HRD0#, Type2=HWR1#, Type5=HRD1#
However, multiplex bus cannot be set for Type 3 (Generic) and Type 6 (PCMCIA).

Fig.4.1 shows the CPU type selection flowchart. Identify type of the target CPU based on its signal line and then check whether an appropriate access is obtainable or not referencing the signal pattern of respective CPUs in Tables 4.5 to 4.10. If the selected pattern does not match the signal pattern, decode the signal externally so that it matches the CPU type of Type 3 Generic or similar pattern.

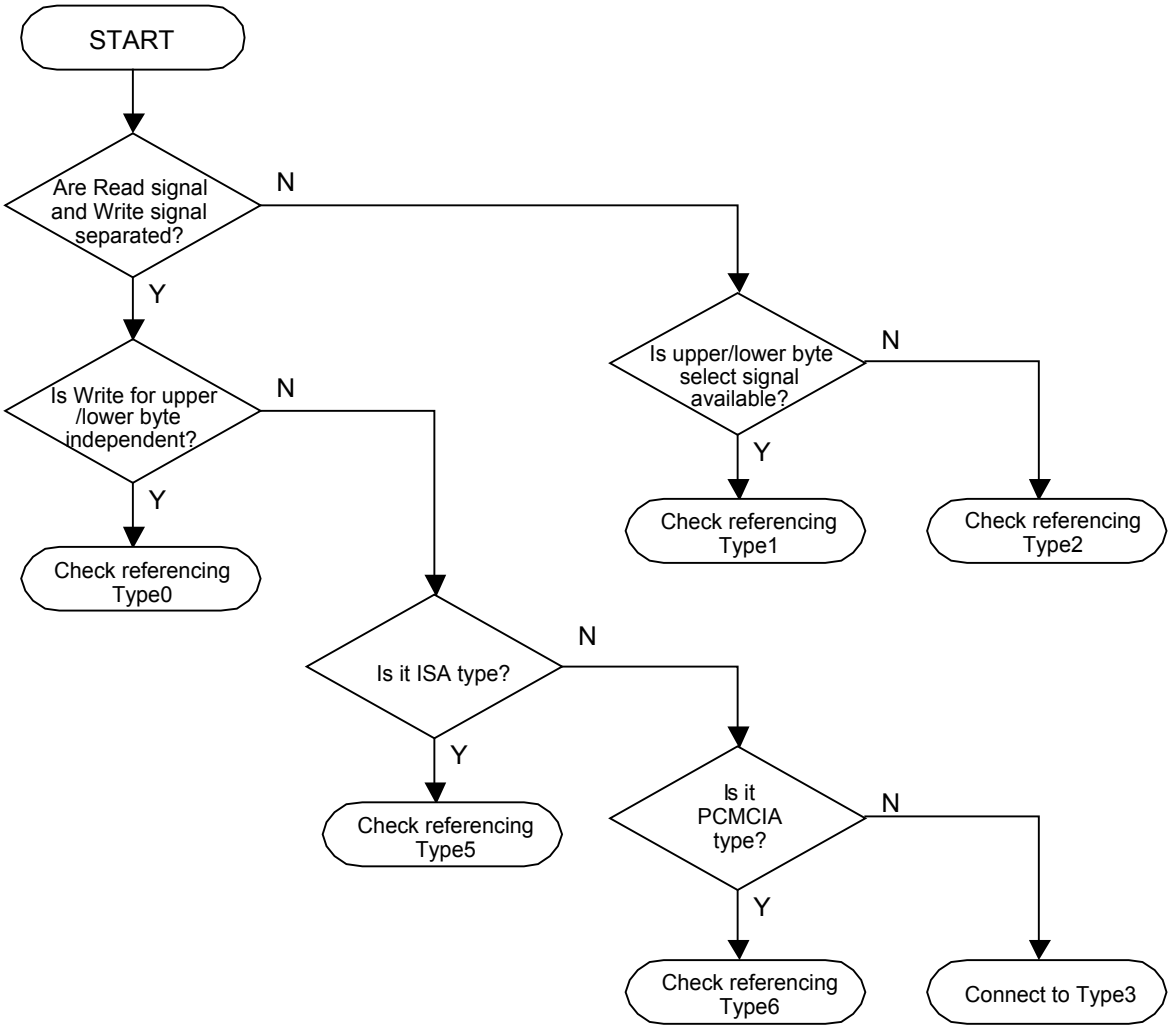


Fig.4.1 Host Interface Type Selection Flowchart

Table 4.4 Signal Connection by CPU Type

Type	Manufacturer	Model	HCS#	HA[2:0]	HD[15:0]	HWR0#	HWR1#	HRD0#	HRD1#	RESET#	Re-mark
Type0	Renesas Technology	SH-3	(*1)	A[2:0]	D[15:0]	WE0#	WE1#	RD#	-/(ASTB)	RESET#	
		SH-4	(*1)	A[2:0]	D[15:0]	WE0#	WE1#	RD#	-/(ASTB)	RESET#	
	EPSON	S1C33	(*1)	A[2:0]	D[15:0]	#WRL	#WRH	#RD	-/(ASTB)	#RESET	
Type1	Freescale Semiconductor	MC68000 MC68010	(*1)	A[2:1], NC	D[15:0]	UDS#	LDS#	-/(ASTB)	R/W#	RESET#	16bit bus only
		MC68008	(*1)	A[2:0]	D[7:0]	—	DS#	-/(ASTB)	R/W#	RESET#	8bit bus only
		MC68HC001	(*1)	A[2:0]	D[15:0]	UDS#	LDS#	-/(ASTB)	R/W#	RESET#	
Type2	Freescale Semiconductor	MC68030	(*1)	A[2:0]	D[31:16]	SIZ0	-/(ASTB)	SIZ1	R/W#	RESET#	
		MC68040	(*1)	A[2:0]	D[31:16]	SIZ0	-/(ASTB)	SIZ1	R/W#	RESET#	
Type3	—	Generic	(*1)	A[2:0]		WR0#	WR1#	RD0#	RD1#	RESET#	
Type5	—	MIPS	(*1)	SA[2:0]	SD[15:0]	MEMW#	SBHE#	MEMR#	-/(ASTB)	inverted RESET	
	IBM	ISA	(*1)	SA[2:0]	SD[15:0]	MEMW#	SBHE#	MEMR#	-/(ASTB)	inverted RESET	
	NEC	VR4121	(*1)	ADD [2:0]	DATA [15:0]	IOW#	SHB#	IOR#	-/(ASTB)	RSTSW#	
Type6	Philips	PR31500 PR31700	GND	A[2:0]	D[23:16], D[31:24]	/CARD IOWR	/CARD xCSL	/CARD IORD	/CARD xCSH	/PON	
	Toshiba	TX3912	GND	A[2:0]	D[23:16], D[31:24]	CARD IOWR*	CARD xCSL*	CARD IORD*	CARD xCSH*	PON*	
	PCMCIA	PC Card	GND	A[2:0]	D[15:0]	-WE	-CE1	-RD	-CE2	inverted RESET	

—: No Connection

-/(ASTB) : NC to connect a CPU of bus separation type. When a CPU of multiplex type is connected, connect an address latch signal to it.

*1: Enter the decoded signal, as needed. Active LOW.

Note: The connections described in this table do not necessarily guarantee the operation. The connection required depends on the operating conditions (including the bus size, bus clock and signal timing). Be sure to reference the signal pattern by type before finalizing your connection.

Table 4.5 Signal Pattern of Type0

				S1S60000 signal line				
R/W	**Endian**	**Bus size**	**Operation**	**HWR0#**	**HWR1#**	**HRD0# (*1)**	**HRD1#**	**HA0**
Write	Little	16bit	Word	L	L	H	H	L
			LOW	L	H	H	H	L
			HIGH	H	L	H	H	H
		8bit	LOW	L	H	H	H	L
			HIGH	L	H	H	H	H
	Big	16bit	Word	L	L	H	H	L
			LOW	L	H	H	H	L
			HIGH	H	L	H	H	H
		8bit	LOW	L	H	H	H	L
			HIGH	L	H	H	H	H
Read	Little	16bit	Word	H	H	L	H	L
			LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
	Big	16bit	Word	H	H	L	H	L
			LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H

*1 HRD1# is constantly kept at HIGH with the internal pull-up resistor. In case of multiplex bus, connect a latch signal here to latch HD[2:0] at the changing point to LOW as the address.

Table 4.6 Signal Pattern of Type1

				S1S60000 signal line				
R/W	**Endian**	**Bus size**	**Operation**	**HWR0#**	**HWR1#**	**HRD0# (*1)**	**HRD1#**	**HA0**
Write	Little	16bit	Word	L	L	H	L	L
			LOW	H	L	H	L	L
			HIGH	L	H	H	L	H
		8bit	LOW	H	L	H	L	L
			HIGH	H	L	H	L	H
	Big	16bit	Word	L	L	H	L	L
			LOW	H	L	H	L	L
			HIGH	L	H	H	L	H
		8bit	LOW	H	L	H	L	L
			HIGH	H	L	H	L	H
Read	Little	16bit	Word	L	L	H	H	L
			LOW	H	L	H	H	L
			HIGH	L	H	H	H	H
		8bit	LOW	H	L	H	H	L
			HIGH	H	L	H	H	H
	Big	16bit	Word	L	L	H	H	L
			LOW	H	L	H	H	L
			HIGH	L	H	H	H	H
		8bit	LOW	H	L	H	H	L
			HIGH	H	L	H	H	H

*1 HRD0# is constantly kept at HIGH with the internal pull-up resistor. In case of multiplex bus, connect a latch signal here to latch HD[2:0] at the changing point to LOW as the address.

Table 4.7 Signal Pattern of Type2

				S1S60000 signal line				
R/W	**Endian**	**Bus size**	**Operation**	**HWR0# (*1)**	**HWR1#**	**HRD0#**	**HRD1#**	**HA0**
Write	Little	16bit	Word	L	H	H	L	L
			LOW	H	H	L	L	L
			HIGH	H	H	L	L	H
		8bit	LOW	H	H	L	L	L
			HIGH	H	H	L	L	H
	Big	16bit	Word	L	H	H	L	L
			LOW	H	H	L	L	L
			HIGH	H	H	L	L	H
		8bit	LOW	H	H	L	L	L
			HIGH	H	H	L	L	H
Read	Little	16bit	Word	L	H	H	H	L
			LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
	Big	16bit	Word	L	H	H	H	L
			LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H

*1 HWR1# is constantly kept at HIGH with the internal pull-up resistor. In case of multiplex bus, connect a latch signal here to latch HD[2:0] at the changing point to LOW as the address.

Table 4.8 Signal Pattern of Type3

				S1S60000 signal line				
R/W	**Endian**	**Bus size**	**Operation**	**HWR0#**	**HWR1#**	**HRD0#**	**HRD1#**	**HA0**
Write	Little	16bit	Word	L	L	H	H	L
			LOW	L	H	H	H	L
			HIGH	H	L	H	H	H
		8bit	LOW	L	H	H	H	L
			HIGH	L	H	H	H	H
	Big	16bit	Word	L	L	H	H	L
			LOW	L	H	H	H	L
			HIGH	H	L	H	H	H
		8bit	LOW	L	H	H	H	L
			HIGH	L	H	H	H	H
Read	Little	16bit	Word	H	H	L	L	L
			LOW	H	H	L	H	L
			HIGH	H	H	H	L	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
	Big	16bit	Word	H	H	L	L	L
			LOW	H	H	L	H	L
			HIGH	H	H	H	L	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H

Table 4.9 Signal Pattern of Type5

				S1S60000 signal line				
R/W	**Endian**	**Bus size**	**Operation**	**HWR0#**	**HWR1#**	**HRD0#**	**HRD1# (*1)**	**HA0**
Write	Little	16bit	Word	L	L	H	H	L
			LOW	L	H	H	H	L
			HIGH	L	L	H	H	H
		8bit	LOW	L	H	H	H	L
			HIGH	L	H	H	H	H
	Big	16bit	Word	L	L	H	H	L
			LOW	L	H	H	H	L
			HIGH	L	L	H	H	H
		8bit	LOW	L	H	H	H	L
			HIGH	L	H	H	H	H
Read	Little	16bit	Word	H	L	L	H	L
			LOW	H	H	L	H	L
			HIGH	H	L	L	H	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H
	Big	16bit	Word	H	L	L	H	L
			LOW	H	H	L	H	L
			HIGH	H	L	L	H	H
		8bit	LOW	H	H	L	H	L
			HIGH	H	H	L	H	H

*1 HRD1# is always HIGH due to the internal pull-up resistor. In case of multiplex bus, latch signal is connected here to latch HD[2:0] at the changing point to LOW and to make it the address.

Table 4.10 Signal Pattern of Type6

				S1S60000 signal line				
R/W	**Endian**	**Bus size**	**Operation**	**HWR0#**	**HWR1#**	**HRD0#**	**HRD1#**	**HA0**
Write	Little	16bit	Word	L	L	H	L	L
			LOW	L	L	H	H	L
			HIGH	L	H	H	L	H
		8bit	LOW	L	L	H	H	L
			HIGH	L	L	H	H	H
	Big	16bit	Word	L	L	H	L	L
			LOW	L	L	H	H	L
			HIGH	L	H	H	L	H
		8bit	LOW	L	L	H	H	L
			HIGH	L	L	H	H	H
Read	Little	16bit	Word	H	L	L	L	L
			LOW	H	L	L	H	L
			HIGH	H	H	L	L	H
		8bit	LOW	H	L	L	H	L
			HIGH	H	L	L	H	H
	Big	16bit	Word	H	L	L	L	L
			LOW	H	L	L	H	L
			HIGH	H	H	L	L	H
		8bit	LOW	H	L	L	H	L
			HIGH	H	L	L	H	H

4.4 Data Swap by Use of Endian

Data is processed in the form of Little Endian inside S1S60000. On the other hand, for matching the connection of Big Endian CPU, S1S60000 swaps data as needed by setting Endian and with the access port and reduces data swapping load on the host CPU side. When an appropriate endian and bus size are selected, you need not be conscious of the swap. The following shows when data is swapped practically:

Following describes examples of actual swap procedures.

- When accessing the command/status port
  Swapping is carried out on the command/status port so that bit orders on the 16-bit register in the host CPU and on the register in S1S60000 become the same. Specifically, the swap is carried out when the big endian and 8-bit bus width are selected.

- When accessing the data port
  When a continued byte string on the memory is transferred, swap on the data port ensures the same byte order on the CPU and S1S60000. Specifically, the swap becomes available when the big endian and 16-bit bus size are selected.

Table 4.11 shows state of the data being written from the host CPU and obtained by S1S60000. Table 4.12 shows state of data being written from S1S60000 and obtained by the host CPU.

Table 4.11 Data Obtained by S1S60000 in Write Operation

R/W	Endian	Bus size	Operation	Command port 1234h write operation	Data port 5678h write operation
Write	Little	16bit	Word	1234	5678
			LOW Byte	xx34	xx78
			HIGH Byte	12xx	56xx
		8bit	LOW Byte	xx34	xx78
			HIGH Byte	xx12	xx56
	Big	16bit	Word	1234	7856(*1)
			LOW Byte	12xx	78xx(*1)
			HIGH Byte	xx34	xx56(*1)
		8bit	LOW Byte	xx12(*1)	xx78
			HIGH Byte	xx34(*1)	xx56

xx: Uncertain
*1: The upper and lower bytes are transposed by the swap operation.

Table 4.12 Data Obtained by Host CPU in Read Operation

R/W	Endian	Bus size	Operation	Status port 1234h read operation	Data port 5678h read operation
Read	Little	16bit	Word	1234	5678
			LOW Byte	zz34	zz78 5678(*2)
			HIGH Byte	12zz	56zz 5678(*2)
		8bit	LOW Byte	zz34	zz78
			HIGH Byte	zz12	zz56
	Big	16bit	Word	1234	7856(*1)
			LOW Byte	12zz	78zz(*1) 7856(*1, *2)
			HIGH Byte	zz34	zz56(*1) 7856(*1, *2)
		8bit	LOW Byte	zz12(*1)	zz78
			HIGH Byte	zz34(*1)	zz56

zz: HIGH impedance, but forced to FFh by the pull-up register.
*1: The upper and lower bytes are transposed by the swap operation.
*2: As for Type0, 16-bit long data is output on the bus, but 8 the host CPU acquires bits alone.

4.5 Access Timing

Writing from the host interface to S1S60000 takes place asynchronously and the state of the signals changes independent of the internal bus clock of S1S60000. Thus, S1S60000 samples state of the host interface signals continuously with the internal bus clock and, after detecting the access state, implements the write operation when it detects the non-access state first. The bus cycle of the host CPU, therefore, must be set to allow at least three times of sampling (2 cycles with the internal bus clock + more than the setup time). Since cycles of the sampling timing can vary according to the internal bus clock, special attention is required when operating S1S60000 at a low internal bus clock.

Table 4.13 Access Time required depending on Operation Mode

OSC3 input	Operation mode	Internal bus clock	Minimum access period (ns)(*1)
25MHz	Normal	50MHz	45
25MHz	Power save	12.5MHz	165
20MHz	Normal	40MHz	55
10MHz	Normal	20MHz	105

*1: The period in which access with the host interface input signal is maintained

Fig.4.2 shows the sampling timing for the write.

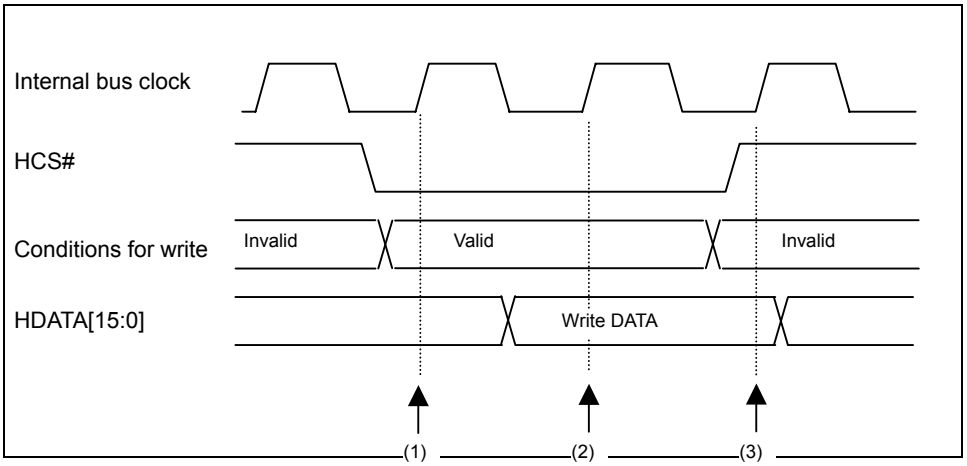


Fig.4.2 Sampling Timing for Write

(1): The timing when the write condition is met for the first time. The data is acquired and held temporarily.
(2): The timing when the write condition is met for the second time. The data is acquired again, used to overwrite (1) data and then held temporarily.
(3): The timing when non-access state is detected for the first time. At the time, no data is acquired. Data acquired by this timing is acquired inside S1S60000.

Operations at respective read timings are essentially the same as the write operation though the data bus drive timing is not identical. Fig.4.3 shows the sampling timing.

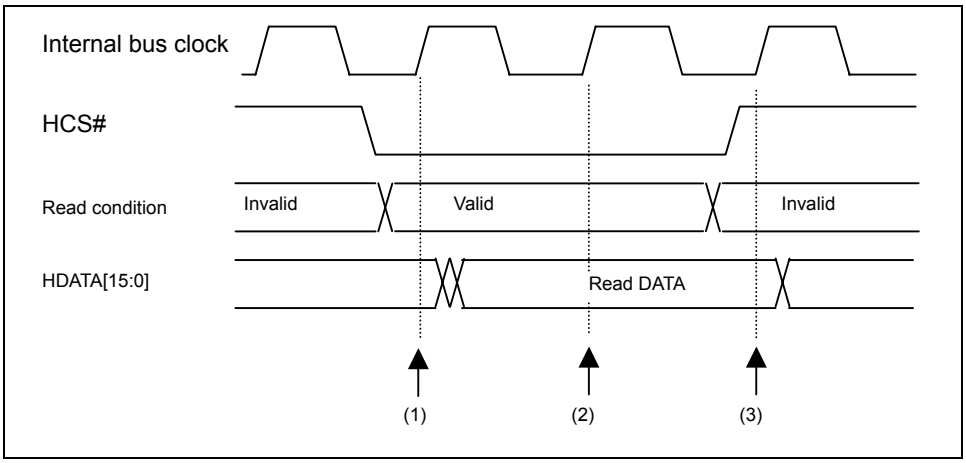


Fig.4.3 Sampling Timing for Read

(1): The timing when the read condition is met for the first time. Driving of the data bus is started.
(2): The timing when the read condition is met for the second time. Driving of the data bus is continued.
(3): The timing when the non-access state is detected for the first time. Driving of the data bus is stopped at this timing.

The access condition is validated only when the write condition or read condition is met and HCS#=LOW. The order, in which above conditions are made valid, is optional. When the setup time requirement was not met because of change of state the signal occurred immediately before the sampling, the sampling condition is regarded invalid. In this case, the valid access must wait for the next sampling.

5. HARDWARE CONTROL

Using GPIO and I^{2}C bus master contained in S1S60000 makes hardware control easier. Following lists controllable hardware.

- Built-in register [to be described in Chapter 5.2]
- GPIO (General-Purpose Input/Output) [to be described in Chapter 5.3]
- I^{2}C slave device [to be described in Chapter 5.4.2]
- EEPROM [to be described in Chapter 5.5]
- Flash ROM: 1Kbyte area available for user

5.1 Control Approach

User can control the built-in hardware of S1S60000 according to the following approaches.

- Control from network
- Control from host interface
- Control form external I^{2}C master
- Control from serial interface

Table 5.1 shows relation between the control approaches and target hardware of control.

Table 5.1 Relation between Control Approaches and Target Hardware

Control approaches	Built-in register	GPIO	I²C Slave	EEPROM	Flash ROM
From network	×	○	○	△	×
From host interface	○	○	○	○	○
From external I²C master	○	○	—	×	×
From serial interface	×	○	○	○	×

○ : Accessible △ : Partially accessible × : Not accessible

5.1.1 Control from Network

Since S1S60000 contains the protocol processing function, it becomes possible to read or control output of GPIO and I^{2}C from network by designating URI. Following shows the URI designation format. All characters are ASCII characters and case insensitive.

Designation format: http://Address:8080/Target[/Destination][?Data]

Address	IP address assigned to S1S60000. Target port number of access is constantly 8080.
Target	Specify one of the followings (target of access) GPIO, I^{2}C, EEPROM ※ In order to prevent inappropriate rewrite, you can prohibit rewrite from network. For the detail, refer to Chapters 5.2.10, 5.2.11 and 5.2.12.
Destination	It depends on the target hardware of read/write such as memory and registers.
Data	It is the data indicating the operation to be conducted on the destination. It depends on the destination. You can specify two or more data by separating them with "&".

To the control request, S1S60000 sends the return value in the following three responses. All return values in the three responses are coded in the same ASCII character string.

In HTTP response header	X-DEVICE-VALUE: Return value
In HEAD element of HTML	<META NAME="DEVICE-VALUE" CONTENT="Return value">
In BODY element of HTML	<DIV CLASS="DEVICE-VALUE">Return value</DIV>

When the hardware control ended unsuccessfully, S1S60000 returns the error using the status line of HTTP response header.

(1) Access to GPIO

When controlling GPIO, code "GPIO" in Target, port number of GPIO in Destination and the data to be output in Data.

Table 5.2 shows the specification format for GPIO access on 1-port basis. Table 5.3 shows the format on 16-port basis. Using the mask, you can operate a specified GPIO alone by setting "1" on the bits corresponding to the target GPIO and setting "0" on all other bits not corresponding to the target.

Table 5.2 GPIO Access Format (1-port basis)

Operation	Designation of port		Designation of output data		Return value
	Digit	Specifiable value	Digit	Specifiable value	Digit
1 port input	2	"00" to "0F" (*1)	—	None	1
1 port output	2	"00" to "0F" (*1)	1	"0","1"	1

*1 : Specify the corresponding GPIO with 2 digits hexadecimal numbers.

Table 5.3 GPIO Access Format (16-port basis)

Operation	Designation of port		Designation of input/output		Designation of mask		Designation of output value		Return value
	Digit	Specifiable value	Digit	Specifiable value	Digit	Specifiable value	Digit	Specifiable value	Digit
16 ports input	2	"0X"	1	"R" (*1)	16	"0","1" (*2)	—	None	16
16 ports output	2	"0X"	1	"W"	16	"0","1" (*2)	16	"0","1"	16

*1 : It can be omitted.

*2 : It can be omitted. Omitting it automatically selects "1111111111111111".

When 16 digits are specified, (when the mask, output value and return value are specified), GPIO15 and GPIO0 are arranged in the upper and the lower, respectively. Table 5.4 shows state of data and return values.

Table 5.4 GPIO Data Designation/Return Value

Return value	Description
"0"	Output is specified and LOW level is being output. When the mask is specified, the port is dropped from the target. If the output value is specified, LOW level is output to the port.
"1"	Output is specified and HIGH level is being output. When the mask is specified, the port is selected as the target of operation. When the output is specified, HIGH level is output to the port.
"L"	Input is specified and LOW level is currently input.
"H"	Input is specified and HIGH level is currently input.
"U"	Not selected as GPIO. It is used as separate function.
"P"	Control from network is prohibited.

[Example 1] When outputting HIGH level to GPIO0 at IP address 192.168.1.1

URI: http://192.168.1.1:8080/GPIO/00?1

Response (HIGH level being output): <DIV NAME="DEVICE-VALUE">1</DIV>

[Example 2] When checking input/output setup and input state of GPIO1 at IP address 192.168.1.1

URI: http://192.168.1.1:8080/GPIO/01

Response (LOW level being input): <DIV NAME="DEVICE-VALUE">L</DIV>

[Example 3] When outputting LOW level to GPIO0 and HIGH level to GPIO4 at IP address 192.168.1.1

URI: http://192.168.1.1:8080/GPIO/0X?W&0000000000010001&0000000000010000

Response: <DIV NAME="DEVICE-VALUE">LLLLPPPPLLL1PLL0</DIV>

[Example 4] When checking input/output setup and input state of GPIO15 from GPIO0 at IP address 192.168.1.1

URI: http://192.168.1.1:8080/GPIO/0X

Response: <DIV NAME="DEVICE-VALUE">LLLLPPPPLLL0PLL0</DIV>

(2) I^2C

When controlling I^2C master function, specify "I^2C" in Target segment and the control data row in Data segment. Destination segment is not provided.

In the control data row, you can specify the value to be output to I^2C bus and the restart timing as well as the timing at which input from I^2C bus is to be received and the byte count used. Control data row is coded as shown below.

Table 5.5 I^2C Control Data Row Coding Method

Element of control data row	Designation method
Slave addressing	Beginning of control data. This addressing must be done after restart. In case of 7-bit addressing, set bit[7:1]=Adr[6:0] and specify R/W bit (1:Read, 0:Write) for bit0. In case of 10-bit addressing, set the first byte's bit[7:3]="11110" and bit[2:1]=Adr[9:8], and then set R/W bit (1:Read,0:Write) for bit0. In the second byte, set bit[7:0]=Adr[7:0].
Value to be output to I^2C bus	2 digits hexadecimal numbers "00" to "FF" for each byte
Restart timing(*1)	"SR"
Input timing from I^2C bus and byte count used (*1)	"LN" and succeeding 2 digits hexadecimal numbers "01" to "08"

*1: It can be coded more than once in the same control data row.

In the control of I^2C master function, the return value takes one of the following values.

Table 5.6 I^2C Control Data Row Coding Method

Return value	Result of control
"ERROR"	Requested control was not completed.
Hexadecimal number x2 (byte count specified with "LN") digits	Completed every requested control and received input from I^2C bus.
"OK"	Completed every requested control.

For writing, the R/W bit is turned to Write and an index is specified at the addressing time and then data is specified. On the other hand, the following procedures are necessary for reading after index specification.

(1) Specify an address. Turn the R/W bit to Write. ← For "writing" an index.
(2) Specify an index.
(3) "SR" ← For selecting a read state while holding the index.
(4) Specify an address. Turn the R/W bit to Read. ← For "reading" data.
(5) Specify the read length with "LN."

When the return value is expressed in hexadecimal numbers and the byte count specified with "LN" is 2 or greater, the byte first received from I^2C bus is arranged in the upper digit and the byte received the next is arranged in the lower digit. Following describes examples of access (following applies to the device where the data that succeeds addressing as an index).

[Example 1] When writing 2 bytes long data (01h, 02h) from Master at IP address 192.168.1.1 to index 0 of 7bit Slave address 02 device.

URI: http://192.168.1.1:8080/I2C?04000102
Response: <DIV NAME="DEVICE-VALUE">OK</DIV>

[Example 2] When reading 3 bytes long data at index 0 of 7bit Slave address 02 device from Master at IP address 192.168.1.1.

URI: http://192.168.1.1:8080/I2C?0400SR05LN03
Response: <DIV NAME="DEVICE-VALUE">000001</DIV>

[Example 3] When reading 3 bytes long data at index 0 of 10bit Slave address 234 device from Master at IP address 192.168.1.1.
URI: http://192.168.1.1:8080/I2C?F43400SRF5LN03
Response: <DIV NAME="DEVICE-VALUE">000001</DIV>

(3) EEPROM
When accessing EEPROM, designate "EEPROM" as the target, offset as the destination and value output to the offset as the data. EEPROM input/output is performed on a word basis (16 bits is counted as 1 word).

Table 5.7 EEPROM Access Format and Return Value

Input/output	Designation of offset		Designation of output data		Return value
	Digit	Specifiable value	Digit	Specifiable value	
Input	2	"00" to "3F"	—	None	"0000" to "FFFF"
Output	2	"11" to "3F"(*1)	4	"0000" to "FFFF"	"OK", "ERROR"

*1 : Rewrite from network is always prohibited in the area from "00" to "10".
And, write to the area prohibited by the user is also disabled when EPMSK register is so set by the user.

[Example 1] When entering data from EEPROM offset 0Dh at IP address 192.168.1.1.
URI: http://192.168.1.1:8080/EEPROM/0D
Response: <DIV NAME="DEVICE-VALUE">0001</DIV>
[Example 2] When outputting data 6401h to EEPROM offset 0Dh at IP address 192.168.1.1.
URI: http://192.168.1.1:8080/EEPROM/0D?6401
Response: <DIV NAME="DEVICE-VALUE">OK</DIV>

5.1.2 Control from Host Interface

When accessing user operable S1S60000 hardware from the host interface, select "SYSTEM" for the terminal point as you specify the command. The internal registers of the S1S60000 and User Flash ROM area are also accessible from the host interface in addition to the hardware accessible from the network. A system can be built by reading the configurations from the User Flash ROM and setting them on the internal registers. For details, refer to "S1S60000 Series Host Interface Manual".

5.1.3 Control from External I²C Master

When controlling the hardware from an external I^2C master, you can access to internal registers by operating S1S60000 as I^2C slave device. For the detail, refer to Chapter 5.4.2.

5.1.4 Control from Serial Interface

Hardware can be controlled by the serial interface only when the GPIO [15:8] is set to be used as a serial interface by the GPALT register, and the GPIO10 pin is HIGH. In this case, the communication data format used is the following ASCII codes. No distinction between upper and lower cases is required.

Designation format:	Target[<space>Destination][?Data]<Return>
Return value format:	Return value<CR><LF>
Target	Specify one of the following (access target), or character string "$VER". GPIO, I^2C or EEPROM
Data	Data indicating the operation to be executed for the destination. It differs depending on the destination. Multiple data are specified by using delimiter "&".
<Return>	Either of CR, CR+LF or LF

The S1S60000 returns a return value in response to a control request. When hardware control fails, it returns an "ERROR" string.

(1) GPIO access

When controlling GPIO, designate "GPIO" as the target, the GPIO port number as the destination and data to be output to the port.

The designation format and data/return value are the same as those of control from the network. Tables 5.3 and 5.4 indicate the designation form when GPIO access is performed on a 16-port basis, and the data/return value states, respectively.

Only a specific GPIO can be operated by setting the bits corresponding to the target GPIO as "1", otherwise "0" in the mask designation. To specify 16 digits (i.e. when mask, output value and return value are designated), the upper order is GPIO15 followed by lower order GPIO0.

[Example 1] Outputting HIGH to GPIO0
Designated data: GPIO<space>/00?1<return>
Return value: 1<CR><LF>

[Example 2] Referring to GPIO1 I/O setting and input status
Designated data: GPIO<space>01<return>
Return value: L<CR><LF>

[Example 3] Outputting LOW to GPIO0 and HIGH to GPIO4
Designated data: GPIO<space>0X?W&0000000000010001&0000000000010000<return>
Return value: LLLLPPPPLLL1PLL0<CR><LF>>

[Example 4] Referring to GPIO15 I/O setting and input status from GPIO0
Designated data: GPIO<space>0X<return>
Return value: LLLLPPPPLLL0PLL0<CR><LF>

(2) I^2C

When controlling I^2C master functions, designate "I^2C" as the target and control data strings as the data. No destination setting is required for the I^2C master.

For control data strings, the value to be output to the I^2C bus, restart timing, timing to receive input from the I^2C bus and its number of bytes can be designated. The control data strings and return values must be written similarly to when controlling from the network as indicated in Tables 5.5 and 5.6.

When the return value is a hexadecimal number and the bytes designated in "LN" are more than 2 bytes, the bytes received by I^2C earlier becomes the upper order and those received later become the lower order of the string. Access examples are indicated as follows (examples when the device used interprets an address designation data as an index).

[Example 1] Writing 2-byte data (01h, 02h) from index 0 of the 7-bit slave address 02 device
Designated data: I2C<space>04000102<return>
Return value: OK<CR><LF>

[Example 2] Reading out 3-byte data from index 0 of the 7-bit slave address 02 device
Designated data: I2C<space>0400SR05LN03<return>
Return value: 000001<CR><LF>

[Example 3] Reading out 3-byte data from index 0 of the 10-bit slave address 234 device
Designated data: I2C<space>F43400SRF5LN03<return>
Return value: 000001<CR><LF>

(3) EEPROM

When accessing EEPROM, designate “EEPROM” as the target, offset as the destination and value output to the offset as the data. EEPROM input/output is performed on a word basis (16 bits is counted as 1 word). The designation format and return values are as follows.

Table 5.8 EEPROM Access Format and Return Values (via Serial)

Input/output	Offset designation		Output data designation		Return values
	Digit	Specifiable value	Digit	Specifiable value	
Input	2	“00” to “3F”	—	None	“0000” to “FFFF”
Output	2	“00” to “3F”	4	“0000” to “FFFF”	“OK”, “ERROR”

Unlike controlling from the network, designation is possible for the entire range.

[Example 1] Inputting data from EEPROM offset 0Dh
Designated data: EEPROM<space>0D<return>
Return value: 0001<CR><LF>

[Example 2] Outputting data 6401h to EEPROM offset 0Dh
Designated data: EEPROM<space>0D?6401<return>
Return value: OK<CR><LF>

(4) Confirming the Firmware Version

If the “$VER” character string is transmitted as the input, an 8-byte ASCII character string representing the currently operating firmware version is returned. The formats of the response strings are described below.

Table 5.9 Configuration of Firmware Version Display Character Text Strings

Data Order	1	2	3	4	5	6	7	8
Contents	Version				Revision No. A		Revision No. B	

Version Numbers (1st - 4th Bytes)

This is the firmware version number. The 1st byte is the HIGH order byte integer, and the 4th byte is the low order byte integer. “0001” means Version 1. The smaller the value displayed, the older the version; the larger the value displayed, the newer the version. The version number will change for large-scale expansion or revision of functions, or after introduction of new specifications that may not be compatible with older specifications.

Revision Number A (5th, 6th Bytes)

This is an uncoded integer. The “00” value indicates the standard firmware, and any setting other than “00” indicates a branch from the standard firmware. The size of the value has no significance. When the value is different, the function may not be compatible because it belongs to another separate branch.

Revision Number B (7th, 8th Bytes)

This is an uncoded integer. Regarding the difference between the version number and the revision number A, a different number is assigned for the revision number every time the firmware is changed. The smaller the value displayed, the older the version; the larger the value displayed, the newer the version.
The standard firmware number (revision number A is “00”) is always an even number.

Example:

For example, if the response character string starts from “00010020” in the leading byte, then this indicates standard S1S60000 firmware version “1”, revision “20”.

∗ This content conforms with the content of Technical Information No. 4 (S1S60000TI-004).

5.2 Built-in Registers

Following lists built-in register that allowing user's setting.

Table 5.10 List of Accessible Built-in Registers

Register name	Offset	Major functions
REVID	0h	Device ID, Revision display (R/O)
MAC0	1h	MAC address
MAC1	2h	MAC address
MAC2	3h	MAC address
GENCR	4h	General-purpose setting register
HIFCR	5h	Specifies host interface
I2CSADR	6h	Specifies I²C slave address
I2CCONF	7h	Specifies I²C clock, specifies noise filter
GPALT	8h	Enables alternate GPIO function
GPCFG	9h	Specifies GPIO I/O
GPDAT	Ah	Specifies GPIO output value
GPMSK	Bh	Specifies operation mask of GPIO from network
EPMSK	Ch	Prohibits EEPROM operation from network
I2CMSK	Dh	Prohibits operation of I²C built-in slave from network
PMWAIT	Eh	Specifies waiting time in power management
PHYMODE	Fh	Specifies operation mode of PHY
ANEGR	10h	Specifies information to be stored among those resulted from the auto-negotiation unique to PHY
IPADRH	11h	IP address
IPADRL	12h	
SNMSKH	13h	Subnet mask
SNMSKL	14h	
DGWH	15h	Default gateway
DGWL	16h	
DADR0H	17h	Destination address 0
DADR0L	18h	
DADR1H	19h	Destination address 1
DADR1L	1Ah	
DADR2H	1Bh	Destination address 2
DADR2L	1Ch	
DADR3H	1Dh	Destination address 3
DADR3L	1Eh	
PORT	1Fh	Port number
DPORT	20h	Destination port number
RSPAR	21h	Serial communication mode setting
TMOUT	22h	Timeout setting
SOPAR	23h	SYSTEM OPEN flag
COMN0	24h	Community name of SNMP Agent
COMN1	25h	
COMN2	26h	
COMN3	27h	

Each register consists of 16 bits. Following describes detail of respective registers (Value in Init. space represents the initial value after reset).

5.2.1 REVID

(Revision ID Register: offset 0h)
Indicates ID and Revision of S1S60000. This is for Read Only.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
REV[7:0]							

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ID[7:0]							

bit	Name	Init.	Description
15:8	REV	01h	(Revision) Indicates revision of the chip. Current value is 01h.
7:0	ID	C3h	(Device ID) Indicates ID of the chip. ID of S1S60000 is C3h.

5.2.2 MAC0,MAC1,MAC2

(Meda Access Controller Address Register: offset 1h, 2h, 3h)
Used to specify MAC address. Size of respective registers is 16 bits. The address is set in the order of network byte in MAC0 lower byte, MAC0 upper byte, MAC1 lower byte up to MAC2 upper byte. Initial values are all 0000h.

Example:
When setting the MAC address 00-00-48-12-34-56, following values are specified to the registers.
MAC0: 0000h, MAC1: 1248h, MAC2: 5634h

Note: When using S1S60000, user is requested to obtain OUI (Organizationally Unique Identifier) from IEEE to set a correct MAC address.

5.2.3 GENCR

(General Configuration Register: offset 4h)

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DISBC	DDSTEN	Reserved	SLPEN	PSEN	SERCONF[2:0]		

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ESKDIV[1:0]		MDCDIV[1:0]		Reserved			

bit	Name	Init.	Description
15	DISBC	0	(Disable Broadcast Receive) Used to specify whether broadcast packets are to be received or not. This function is used only under limited conditions. It should normally be set to 0. 0: Receives broadcast packets 1: Does not receive broadcast packets
14	DDSTEN	0	(Default Destination Massaging enable) When the INT0 function (separate GPIO0 function) is enabled, the interrupt notice function is enabled and DDSTEN indicates that the destination address of the notice transmission is enabled. 0: Interrupt notice function is invalid 1: Interrupt notice function is valid and DADR0H, DADR0L is valid
13	Reserved	0	Reserved. Be sure to set 0.
12	SLPEN	0	(Sleep Mode Enable) Selects use or non-use of the sleep mode as the power management. For the sleep mode, refer to Chapter 6. 0: Does not use the sleep mode 1: Use the sleep mode ※ When PMWAIT = 0, however, the sleep mode is not available despite of the setting of this bit.
11	PSEN	0	(Power Save Mode Enable) It reduces the operating clock to 1/4 of the normal level in order to save power consumption. 0: Does not use the power save mode. 1: Use the power save mode.
10:8	SERCONF	000	(Serial Configuration) When the serial Interface pin (alternate function of GPIO[15:8] is enabled, it specifies how to use the pin. 000: Hardware control mode (Note 1) 010: Serial emulation mode Active Open (Client operation) 011: Serial emulation mode Passive Open (Server operation) Other than the above: Reserved. Note 1 : A fixed operation all the time irrespective of state of the GPIO10/MODE pin.
7:6	ESKDIV	00	(EEPROM Serial Clock Divide) It is used specify how the EEPROM Interface clock should be divided in comparison with the internal bus clock. The slower the clock is, the longer becomes the time required for the access. Set an appropriate time on the EEPROM connected. 11:/32 10:/64 01:/128 00:/256
5:4	MDCDIV	00	(MIF Clock Divide) It is used to specify how the MII Management Interface clock should be divided in comparison with the internal bus clock. The slower the clock is, the longer becomes the time required for the access. Set an appropriate division so that the clock may be 4MHz maximum. 11:1/4 10:1/8 01:1/16 00:1/32
3:0	Reserved	0000	Reserved. Be sure to set 0.

5.2.4 HIFCR

(Host Interface Configuration Register: offset 5h)

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Reserved	HIPOL	Reserved	HENDN	HSIZE	HIFSEL[2:0]		

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved							

bit	Name	Init.	Description
15	Reserved	0	Reserved. Be sure to set “0”.
14	HIPOL	pin	Host Interrupt Polarity: Sets the polarity when interrupts are used by the host I/F. 0:LOW active 1:HIGH active * The initial value depends on the status of the HIPOL pin when hardware is reset. This bit is set to “1” when the HIPOL pin is HIGH level, and set to “0” when the pin is LOW level.
13	HMUX	pin	Host Multiplex: Determines whether the multiplex bus is used by the host interface. 0:Separate bus 1:Multiplex bus * The initial value depends on the status of the HMUX pin when hardware is reset. This bit is set to “0” when the HMUX pin is HIGH level, and set to “1” when the pin is LOW level.
12	HENDN	pin	Host Endian: Sets the host I/F Endian type. 0:Little 1:Big * The initial value depends on the status of the HENDIAN pin when hardware is reset. This bit is set to “1” when the HENDIAN pin is HIGH level, and set to “0” when the pin is LOW level.
11	HSIZE	pin	Host Interface Size: Sets host I/F bus width. 0:16bit 1:8bit * The initial value depends on the status of the HSIZE pin when hardware is reset. This bit is set to “1” when the HSIZE pin is HIGH level, and set to “0” when the pin is LOW level.
10:8	HIFSEL	pin	Host Interface Type: Switches the class of the host I/F. For more details, please refer to Chapter 4.3. * The initial value depends on the status of the HIFSEL[2:0] pin when hardware is reset. These pins are set to “1” when the corresponding HIFSEL pins are HIGH level, and set to “0” when the pins are LOW level.
7:0	Reserved	00h	Reserved. Be sure to set “0”.

5.2.5 I2CSADR

(I^2C Slave Address Register: offset 6h)

It saves the address of S1S60000 when operated as I^2C slave device.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Reserved							

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	SADR[6:0]						

bit	Name	Init.	Description
15:7	Reserved	all 0	Reserved. Be sure to set 0.
6:0	SADR	30h	It is used to specify the slave address when S1S60000 operates as I^2C slave device. Specify a value in the range of 30h to 37h. **[Important]** The value specified here must be the one officially assigned by Philips of Holland. For the S1S60000, the range of 30h to 37h is assigned by Philips.

5.2.6 I2CCONF

(I^2C Configuration Register: offset 7h)
It is used to specify the clock when S1S60000 is operated as I^2C master device.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Reserved					NCCNT[2:0]		

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SCLCNT[7:0]							

bit	Name	Init.	Description
15:11	Reserved	00000	Reserved. Be sure to set 0.
10:8	NCCNT	000	(Noise Cancel count value: Master,Slave) It is used to select a value of the noise canceller of I²C bus. A larger value removes noise better. Normally the value is selected in the 0 to 2. For a noisy environment, select 3 or greater value.
7:0	SCLCNT	00h	(SCL delay count value: Master) When S1S60000 operates as I²C master device, it is used to specify the I²C transfer clock. The transfer clock is calculated according to the following formula. I²C transfer clock [Hz] = Internal bus clock /(2 × (SCLCNT+NCCNT)+15) When connecting the Fast mode device, the clock should be 400kHz maximum. And when connecting the Normal mode device, 100kHz maximum is recommended. **[Setting example]** When OSC3 input is 25MHz, Internal bus clock = 50MHz As for Fast mode: SCLCNT=53 (35h), NCCNT=2 As for Normal mode: SCLCNT=241 (F1h), NCCNT=2

5.2.7 GPALT

(GPIO Alternate Function Register: offset 8h)
It is set when enabling the alternate function of GPIO [15:0] pin.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
GPALT15	GPALT14	GPALT13	GPALT12	GPALT11	GPALT10	GPALT9	GPALT8

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GPALT7	GPALT6	GPALT5	GPALT4	GPALT3	GPALT2	GPALT1	GPALT0

bit	Name	Init.	Description
15:8	GPALT[15:8]	FFh	Used to enable function of GPIO [15:8] as the serial pin. Refer to Chapter 2.3 for detail. 0: GPIO function 1: Serial Interface pin **[Important]** Be sure to switch bit [15:8] in a lump. When set for any value other than "00h" or "FFh", does not operate normally for either function.
7	GPALT7	0	Used to enable function of GPIO7 as OSCCTL. After the sleep mode is turned on, GPIO7 is used to specify whether the external oscillator is to be stopped or not. When this bit is 1, GPIO7 generates output. In the normal operation, its output is HIGH level and in the sleep mode, LOW level is output. 0: GPIO7 1: OSCCTL output
6	GPALT6	0	Alternate function of GPIO6 is not prepared. Set “0”.
5	GPALT5	0	Alternate function of GPIO5 is not prepared. Set “0”.
4	GPALT4	0	Alternate function of GPIO4 is not prepared. Set “0”.
3	GPALT3	0	Alternate function of GPIO3 is not prepared. Set “0”.
2	GPALT2	0	Used to enable function of GPIO2 as CRS. In Half Duplex communication, GPIO2 is used CRS input. 0: GPIO2 1: CRS input
1	GPALT1	0	Alternate function of GPALT1 is not prepared. Set “0”.
0	GPALT0	0	Used to enable functions of GPIO0 as INT0. It detects the LOW level and enables the notification function on the network. Also, it restores the normal mode from the sleep mode. 0: GPIO0 1: INT0 (LOW Level) Note: When using it as INT0, design the peripheral circuits so that it comes to HIGH Level all the time other than interruption.

5.2.8 GPCFG

(GPIO I/O Configuration Register: offset 9h)
It is used select the input/output direction of GPIO pin.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
GPCFG15	GPCFG14	GPCFG13	GPCFG12	GPCFG11	GPCFG10	GPCFG9	GPCFG8

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GPCFG7	GPCFG6	GPCFG5	GPCFG4	GPCFG3	GPCFG2	GPCFG1	GPCFG0

bit	Name	Init.	Description
15:0	GPCFG15 to GPCFG0	0000h or C200h	Used to specify input or output for GPIO [15:0]. Bit [15:0] is corresponding to GPIO [15:0] enabling bit-by-bit setup. 0: Selects inputs 1: Selects output Initial setting changes depending on the GPIO[15:8] setting ● Initial value is C200h when serial pin is set (in hardware control mode, or serial emulation mode) ● Initial value is 0000h for any other case. Also, the value of this register changes depending on the GPALT setting. ● If GPALT[0]=1, then GPCFG[0]=0 (INT0 input) ● If GPALT[2]=1, then GPCFG[2]=0 (CRS input) ● If GPALT[7]=1, then GPCFG[7]=1 (OSCCTL output) ● If GPALT[15:8]=FFh, then GPCFG[15:8]=C2h (DTR#, RTS#, TXD output)

5.2.9 GPDAT

(GPIO Output Data Register: offset Ah)
Used to specify the output value of GPIO pin.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
GPDAT15	GPDAT14	GPDAT13	GPDAT12	GPDAT11	GPDAT10	GPDAT9	GPDAT8

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GPDAT7	GPDAT6	GPDAT5	GPDAT4	GPDAT3	GPDAT2	GPDAT1	GPDAT0

bit	Name	Init.	Description
15:0	GPDAT15 to GPDAT0	0000 or 0200h or 8200h	When the output mode is set for GPIO [15:0], it is used to specify the value to be output to the pin. Bit [15:0] is corresponding to GPIO [15:0] enabling bit-by-bit setup. When other than the output mode is selected, the value is saved on the register but not notified to the pin. 0: LOW output 1: HIGH output Initial setting changes depending on the GPIO[15:8] setting ● Initial value is 8200h for hardware control mode set in serial mode. ● Initial value is 0200h for serial emulation mode set in serial mode. ● Initial value is 0000h for any other case. Also, the value of this register changes depending on the GPALT setting. ● If GPALT[7]=1, then GPDAT[7]=1 (OSCCTL=High) ● If GPALT[15:8]=FFh, then GPDAT[9]=1 (TXD=High)

5.2.10 GPMSK

(GPIO Access Mask Register: offset Bh)
It is used to prohibit modifying the output value of GPIO pin from network.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
GPMSK15	GPMSK14	GPMSK13	GPMSK12	GPMSK11	GPMSK10	GPMSK9	GPMSK8

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GPMSK7	GPMSK6	GPMSK5	GPMSK4	GPMSK3	GPMSK2	GPMSK1	GPMSK0

bit	Name	Init.	Description
15:0	GPMSK15 to GPMSK0	0000h	It disables modifying the output value of GPIO from network. Bit [15:0] is corresponding to GPIO [15:0] enabling bit-by-bit setup. This setting is invalid when the output mode is not selected. However, the set value is maintained. 0: Allows modifications from network 1: Prohibits modifications from network

5.2.11 EPMSK

(EEPROM Access Mask Register: offset Ch)
It is used to specify an area on EEPROM where rewrite from network is prohibited.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
EPUSE[3:0]				PINGDIS	TFTPDIS	HTTPDIS	SNMPDIS

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
EPMSK[7:0]							

bit	Name	Init.	Description
15:12	EPUSE	0000	EEPROM Usage: ID that indicates how to use EEPROM user areas (28h to 7Fh). 0000 Standard (that users use freely.) 0001 – 0111 Reserve 1000 MIB system group 1001 – 1111 Reserve
11	PINGDIS	0	Pin0 Reply Disable: It is used to control the ping (ICMP Echo Reply) function. 0 – replies to ping. 1 – prohibits reply to ping.
10	TFTPDIS	0	TFTP Service Disable: It is used to control the TFTP function (to be used for the firmware update function). 0 – enables the TFTP function. 1 – disables the TFTP function.
9	HTTPDIS	0	HTTP Server Disable: It is used to control the HTTP server function (to be used for hardware control function). 0 – enables the HTTP server function. 1 – disables the HTTP server function.
8	SNMPDIS	0	SNMP Server Disable: It is used to control the SNMP server function. 0 – enables the SNMP server function. 1 – disables the SNMP server function.
7:0	EPMSK[7:0]	00h	EEPROM Access Mask: It is used to specify areas where EEPROM is not rewritten to indices below set values from network.

[EPUSE = 1000: MIB system group]
When EPUSE is set to 1000 (MIB system group), the EEPROM user area is interpreted as follows:

Offset	Area size (byte)	Usage
28h to 3Bh	40	Character string that becomes sysDescr of MIB-II system group.
3Ch to 3Fh	8	OID that becomes sysObjectID of MIB-II system group.

Store sysDescr in the form of character string. To store it as "test," for example, store the following value from the offset 28h.

Byte string: 0×74, 0×65, 0×73, 0×74
EEPROM: 0×6574, 0×7473

When the byte string includes 0 or comes to 40 bytes, sysDescr is regarded to end there.

Store sysObjectID from below enterprise. Before storing it, encode it to OID type with BER. When the sysObjectID is 1.3.6.1.4.1.1248.5.1.1.1, for example, store the following value from the offset 3Ch.

Byte string: 0×89, 0×60, 0×05, 0×01, 0×01, 0×01
EEPROM: 0×6089, 0×0105, 0×0101

When the byte string includes 0 or comes to 8 bytes, sysObjectID is regarded to end there. Your attention is requested to the fact that, if 1 stands at the most significant bit of the offset 3Fh, the data becomes abnormal.

5.2.12 I2CMSK

(I^2C Slave Access Mask Register: offset Dh)
Prohibits network from rewriting the external I^2C slave device

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Reserved							

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved		I2CMSK[5:0]					

bit	Name	Init.	Description
15:7	Reserved	all 0	Reserved. Be sure to set 0.
6:0	I2CMSK[6:0]	000000	Prevents I^2C rewrites from the network for Index values lower than the value set. Note: With devices that specify indexes as more than one byte, this mask is valid only for the first index specification data (data that follows the slave device address specification). Only the second piece of data following the slave device address specification is affected by this mask.

5.2.13 PMWAIT

(Power Management Wait Time Register: offset Eh)
When the power management mode is enabled, it is used to specify the waiting time until respective modes are turned on.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Reserved							

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved				SLPWAIT[3:0]			

bit	Name	Init.	Description
15:4	Reserved	000h	Reserved. Be sure to set 0.
3:0	SLPWAIT	0h	Sleep Wait Time It is used to specify the waiting time until the sleep mode is turned on from the power down mode. When the set value is n, the waiting time comes to 2^n(ms) approximately. When 0 is specified, the sleep mode is not turned on irrespective of setting of SLPEN of the GENCR register. Specifying a value in the range from 1 to 15 allows setting the waiting time in the range from 2ms to 32768ms.

5.2.14 PHYMODE

(Physical Layer Operation Mode: offset Fh)
It is used to specify an operation mode of PHY chip.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
ANEGD	Reserved				AMODE[2:0]		

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved						MLINK[1:0]	

bit	Name	Init.	Description
15	ANEGD	0	Auto Negotiation Disable: It is used to specify whether auto negotiation is used or not when a link is established. When a PHY chip to be used does not have the auto negotiation function or when the counterpart of the link does not support the auto negotiation function, 1 is set so that link conditions are set by MLINK bit. 0: Uses the auto negotiation function of PHY. 1: Does not use the auto negotiation function of PHY.
14:11	Reserved	0000	Reserved. Be sure to set 0.
10:8	AMODE	100	Auto Negotiation Link Mode: Used to specify an available link mode using the auto-negotiation. 000: 10BASE/Half Duplex 001: 10BASE/Full Duplex 010: 10BASE/Full or Half Duplex 011: 100BASE/Half Duplex 100: 100BASE/Half Duplex or 10BASE/Full or Half Duplex 101: 100BASE/Full Duplex or 10BASE/Full Duplex (reserved for future extension and thus not specifiable) 110: 100BASE/Full or Half Duplex (reserved for future extension and not thus specifiable) 111: Reserved
7:2	Reserved		Reserved. Be sure to set 0.
1:0	MLINK	00	Manual Link: When ANEGEN=1, the manual procedure is specified for establishing the link. 00: 10BASE/Half Duplex 01: 10BASE/Full Duplex 10: 100BASE/Half Duplex 11: 100BASE/Full Duplex (reserved for future extension and thus not specifiable)

5.2.15 ANEGR

(Auto Negotiation Result Information Register: offset 10h)
It is used to specify the storing method for the auto-negotiation function result of the PHY chip. S1S60000 selects internal processing for respective operating states by using this information. Refer to the data sheet of PHY to be used and set an appropriate value.
[Modification] PHY link information acquiring method was modified in Firmware Version 1, Revision 22 or later. Thus, the setting for this register was eliminated.
* The appropriate firmware is installed on products of product number S1S60000F00A500 (IC marking: S1S60000F00A5) or later.

When using these products, all bits become RESERVED and the value will be ignored.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
LSOFF[3:0]				Reserved		DINV	SINV

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DUPLEX[3:0]				SPEED[3:0]			

bit	Name	Init.	Description
15:12	LSOFF	0001	Link Status Offset: When the link is attempted through the auto-negotiation, which is unique to the PHY chip, is carried out, it is used to specify the position of MII management interface register to store the negotiation result as an offset from index 16. When it is 111, however, the index is 0. 0000: Index 16 register stores result of the attempt to establish the link. 0001: Index 17 register stores result of the attempt to establish the link. ... 1110: Index 30 register stores result of the attempt to establish the link. 1111: Index 0 register stores result of the attempt to establish the link.
11:10	Reserved	00	Reserved. Be sure to set 0.
9	DINV	0	Duplex Invert: Used to change the meaning of bit being specified for DUPLEX. 0: When Bit[DUPLEX]=1, Full Duplex and when Bit[DUPLEX]=0, Half Duplex. 1: When Bit[DUPLEX]=1, Half Duplex and when Bit[DUPLEX]=0, Full Duplex.
8	SINV	0	Speed Invert: Used to change the meaning of bit being specified with SPEED. 0: When Bit[SPEED]=1, 100BASE and when Bit[SPEED]=0, 10BASE. 1: When Bit[SPEED]=1, 10BASE and when Bit[SPEED]=0, 100BASE.
7:4	DUPLEX	1110	Duplex bit: It is used to specify the position of the bits to indicate the Duplex mode in the register storing the result of the auto-negotiation (indicated with LSOFF)/ 1111: bit15, 1110: bit14, ... 0001: bit1, 0000: bit0
3:0	SPEED	1111	Speed bit: It is used to specify the position of the bits to indicate the link speed in the register storing the result of the auto-negotiation (indicated with LSOFF). 1111: bit15, 1110: bit14, ... 0001: bit1, 0000: bit0

Setup example :
ICS1893-Y of ICS Company stores results of the auto negotiation in the register of Index 17, allocates the link speed to bit15 and the Duplex mode to bit14. Thus, the setup is as follows:
LSOFF=0001, DINV=0, SINV=0, DUPLEX=1110, SPEED=1111.

5.2.16 IPADRH,IPADRL

(Default IP Address: offset 11h, 12h)
Used to hold the own IP address. Table 5.11 shows the initial values and the register settings.

Table 5.11 Setup of Address and Subnet Mask

Target	Initial value	Notation in hex	Register setting	Offset
IP address	192.168.0.254	C0.A8.00.FE	IPADRH=A8C0h, IPADRL=FE00h	11h, 12h
Subnet mask	255.255.255.0	FF.FF.FF.00	SNMSKH=FFFFh, SNMSKL=00FFh	13h, 14h
Default gateway	192.168.0.1	C0.A8.00.01	DGWH=A8C0h, DGWL=0100h	15h, 16h
Destination address 0	192.168.0.2	C0.A8.00.02	DADR0H=A8C0h, DADR0L=0200h	17h, 18h,
Destination address 1	192.168.0.3	C0.A8.00.03	DADR1H=A8C0h, DADR1L=0300h	19h, 1Ah
Destination address 2	192.168.0.4	C0.A8.00.04	DADR2H=A8C0h, DADR2L=0400h	1Bh, 1Ch
Destination address 3	192.168.0.5	C0.A8.00.05	DADR3H=A8C0h, DADR3L=0500h	1Dh, 1Eh

5.2.17 SNMSKH,SNMSKL

(Subnet Mask: offset 13h, 14h)
Used to hold the subnet mask. The initial values and register settings are the same as those shown in Table 5.11.

5.2.18 DGWH,DGWL

(Default Gateway: offset 15h, 16h)
Used to hold the address of the default gateway. The initial values and register settings are the same as those shown in Table 5.11.

5.2.19 DADRnH,DADRnL

(Destination Address: offset 17h to 1Eh)
Used to hold the destination address. DADR0H, DADR0L, DADR1H, DADR1L, DADR2H, DADR2L, DADR3H and DADR3L hold the four destination addresses. Also, DADR0H, DADR0L are used as the IP address in the following cases.
・Connection destination IP address while client (Active Open) is operating in serial emulation mode.
・Transmit destination IP address when using the GPIO0 interrupt notice function.
The initial values and register settings are the same as those shown in Table 5.11.

5.2.20 PORT

(Default Port: offset 1Fh)
It is used as Port Number in the following cases:
・Listening port number in a server (Passive Open) operation in the serial emulation mode.
・Transmit source port number of the transmit packet while client (Active Open) is operating in serial emulation mode.
・Transmit source port number of the transmit packet when using the GPIO0 interrupt notice function.
The default value is C000h (49152).

5.2.21 DPORT

(Destination Port: offset 20h)
It is used as Port Number in the following cases:
・Destination port number in a client (Active Open) operation in the serial emulation mode.
・Destination port number in using the interrupt notification function of GPIO0.
The default value is C001h (49153).

5.2.22 SERMODE

(Serial Mode: offset 21h)
SERMODE sets the operation mode for the serial emulation operation. SERMODE is specified with the SERCONF setting of the GENCR register.
The bits are assigned as follows for GENCR.SERCONF=010 (serial emulation mode).

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Reserved							BAUD[2]

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BAUD[1:0]		LEN	STOP	PARITY		FLOW	

bit	Name	Init.	Descriptions
15:9	Reserved	all 0	Reserved. Be sure to set 0.
8:6	BAUD	011	Baud rate: Used to specify baud rate of the serial interface. 000: 1200 001: 2400 010: 4800 011: 9600 100: 19200 101: 38400 110: 57600 111: 115200
5	LEN	1	Data Length: Data length 0: 7bit 1: 8bit
4	STOP	0	Stop bit: Stop bit length 0: 1bit 1: 2bit
3:2	PARITY	00	Parity: Parity check setting 00: None 01: Reserved 10: Even number parity 11: Odd number parity
1:0	FLOW	01	Flow Control: Flow control setting 00: None 01: RTS/CTS 10 or 11: Reserved.

5.2.23 TMOUT

(Timeout: offset 22h)
Used to specify the timeout value for TCP connection on the second time scale. The default value is 64 (40h). When 0 is specified, it is set to the default value (64 seconds). This setting is used for the following purposes in the same way as when TCP is specified by option parameters 12 and 13 of the open command.

- TTL of the IP datagram to be transmitted.
- Time taken to give up active open of the TCP.
- Time taken to wait for ACK to receive TCP transmitted data.
- Time taken to wait for host CPU's response for a received SNMP request.

5.2.24 SOPAR

(System Open Parameter: offset 23h)
Used to store flag setup information at the SYSTEM communication end point. When bit0 of flag data (No. 2 byte of option data) is 1 in opening the SYSTEM communication end point from the host interface, this setup is enabled. When bit0 is 0, this setup is disabled. Also, this setting is used as an open parameter even when the serial emulation mode is enabled.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
RPHOLD	Reserved						

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DLEN	IPEN	SNMEN	DGWEN	Reserved			

bit	Name	Init.	Descriptions
15	RPHOLD	0	Receive Packet Hold: It is used to extend the hold time of packets, which are reversely received during the TCP connection. This function is available only on Firmware Version 1, Revision 22 or later. 0: Existing compatibility (no extension) 1: TCP/IP connection Linux2.4 compliant Extend the reverse packet hold time 1 sec.
14:8	Reserved	all 0	Reserved. Be sure to set 0.
7	DLEN	0	DATALINK Enable: It is used to specify if the DATALINK layer is directly used. When this setup is enabled, the protocol processing built in S1S60000 is not used and data transmitted and received on the network is handled as transmission and receive date of the host interface as it is. However, the create and check functions of FCS data are enabled. 0: The built-in protocol processing is used. 1: Data is directly input and output in and from the DATALINK layer.
6	IPEN	1	IP Address Enable: It is used to specify whether specifying IP address from the host interface is enabled or disabled. 0: Disables specifying IP address and tries to acquire it by means of DHCP. 1: Enables specifying IP address. ∗ To enable specification with the built-in registers IPADRH and IPADRL, specify 0.0.0.0 to IP addresses to be specified from the host interface.
5	SNMEN	1	Subnet Mask Enable: It is used to specify whether specifying subnet mask from the host interface is enabled or disabled. 0: Disables specifying subnet mask and specifies default values of IP addresses. 1: Enables specifying subnet mask. ∗ To enable specification with the built-in registers SNMSKH and SNMSKL, specify 0.0.0.0 to subnet masks to be specified from the host interface.
4	DGWEN	1	Default Gateway Enable: It is used to specify whether specifying default gateway from the host interface is enabled or disabled. 0: Disables specifying default gateway. 1: Enables specifying default gateway. ∗ To enable specification with the built-in registers DGWH and DGWL, specify 0.0.0.0 to default gateway to be specified from the host interface.
3:0	Reserved	all 0	Reserved. Be sure to set 0.

5.2.25 COMN0,COMN1,COMN2,COMN3

(Community Name: offset 24h to 27h)
It holds community name that can be set to the SNMP agent. Initial values and set values of respective registers are as shown in Table 5.12. The default community name of the SNMP agent is "public" irrespective of values of the built-in registers.

Table 5.12 Setting of SNMP Community Name

Target	Initial value	Notation in hex	Register setting	Offset
Community name	public	70.75.62.6C.69.63.00.00	COMN0=7570h, COMN1=6C62h, COMN2=6369h, COMN3=0000h	24h 25h 26h 27h

5.3 GPIO

As GPIO (General Purpose Input/Output), S1S60000 has 16 GPIO pins of GPIO[7:0] and GPIO[15:8]. Each pin allows independent operation. Special functions other than the GPIO function are assigned to some pins. You can switch the functions by changing setting of the GPALT register.

After the reset, every pin usable as GPIO is set for the input and the output value is initialized to 0. When an output operation is conducted on a pin being specified set for input, the specified data is set as a requested output value but actual output is not generated. If the pin is set as an output pin after that, the specified value will be output from the pin. When you want to maintain the GPIO output at HIGH level after the hardware reset, set the level of the pins currently being reset at HIGH by use of the external pull-up register and then select 1 for the output setting.

Table 5.13 GPIO Pin Functions

Pin name	Characteristics (*1)	Special function	Priority
GPIO0/INT0	5V tolerant input	Interrupt notice/return from sleep mode	1
GPIO1	5V tolerant input		1
GPIO2/CRS	5V tolerant input	CRS input	1
GPIO3	5V tolerant input		2
GPIO4	5V tolerant input		3
GPIO5	5V tolerant input		3
GPIO6	5V tolerant input		3
GPIO7/OSCCTL	5V tolerant input	Control of external OSC	3
GPIO8/RXD	3.3V schmitt input	Serial Interface	2
GPIO9/TXD	3.3V schmitt input	Serial Interface	2
GPIO10/MODE	3.3V schmitt input	Serial Interface	2
GPIO11/RSV1	3.3V schmitt input	Serial Interface	2
GPIO12/CTS#	3.3V schmitt input	Serial Interface	1
GPIO13/DSR#	3.3V schmitt input	Serial Interface	1
GPIO14/RTS#	3.3V schmitt input	Serial Interface	1
GPIO15/DTR#	3.3V schmitt input	Serial Interface	1

*1: Every pin conforms to CMOS input/output.

Priority indicates the order of operation when two or more pins are to be operated at the same time. Switching occurs at the same time among the pins with the same priority level. Among the pins with different priority levels, however, there occurs some differences in input and output (due to the time required for the software-based operation). If you want such pins to change at the same time, an additional arrangement such as an external latch to be operated by GPIO is required.

When the INT0 function is enabled, GPIO0 can be used as the LOW level input interrupt pin. This interrupt takes the S1S60000 out of the sleep mode. Also, when the DDSTEN bit of the GENCR register is set to "1", the notice packet can be sent to the preset network connection destination. For more details, please refer to "5.3.1 Interrupt Notice Function".

GPIO2 is used as CRS input pin in Half Duplex communication.

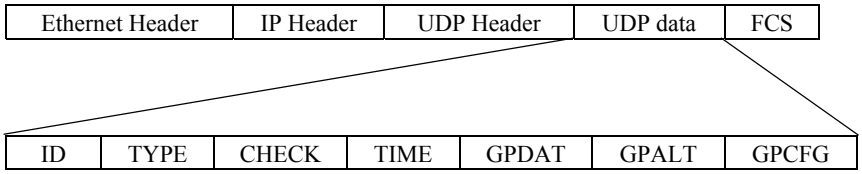
When the OSCCTL function is enabled, GPI07 functions as the control pin of the external oscillator. In this setup, this pin output HIGH level during the normal operation, but if the sleep mode is turned on and the operating clock is switched to OSC1, its output is switched to LOW level. By this arrangement, the external oscillator is stopped reducing the overall power consumption as the result. When exiting from the sleep mode with the trigger, GPIO7 is set to HIGH and, after a predetermined oscillation stabilizing time (approximately 10ms), switching to OSC3 takes place to recover the normal mode.

GPIO [15:8] can be used as the start-stop synchronous serial pin from the setting of SERCONF of GENCR register. For the detail, refer to "2.3 Serial Interface".

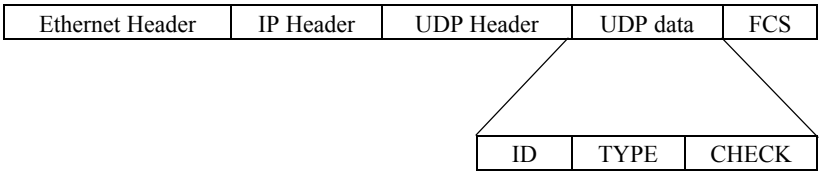
5.3.1 Interrupt Notice Function

When an INT0 interrupt occurs while the interrupt notice function is enabled, a packet is transmitted as notification of the GPIO status to the DPORT port address specified by the IP address in the DADR0H, DADR0L registers. At the notice destination, after the CHECK confirms that the correct packet as been received, transmit the ACK packet in the specified format. For details about operation, please refer to "Technical Information No.11".
The packet configuration is described below.

(1) Configuration of Packets Transmitted from S1S60000 (Interrupt Notice Packets)



(2) ACK Packet Configuration



(3) Packet Contents

Ethernet Header (14 Bytes):	Standard Ethernet Header
IP Header (20 Bytes):	Standard IP Header
UDP Header (8 Bytes):	A standard UDP header consists of the port number of the transmission source, port number of the transmission destination, UDP length, and checksum.
ID (4 Bytes):	Number of Interrupt occurrences.
Type (2 Bytes):	Interrupt notice packet = 0×0000, ACK packet=0×0001
CHECK (2 Bytes):	UDP data checksum Checksum is calculated in 16-bit units in the following order: (1) Sets CHECK field (2 bytes) to "0". (2) Divides the UDP data into 16-bit segments and calculates one complement sum. (3) The result of the calculation becomes 1 complement and replaces the CHECK.
TIME (4 Bytes):	TIME (4 Bytes): The amount of time elapsed (Unit: ms) from S1S60000 startup to occurrence of the interrupt.
GPDAT (2 Bytes):	GPDAT register value (GPIO I/O value)
GPALT (2 Bytes):	GPALT register value
GPCFG (2 Bytes):	GPCFG register value (GPIO I/O setting)

5.4 I²C

I²C is an Inter IC Bus developed by Philips. S1S60000 contains the I²C master/slave function. Following describes features of the function.

- Master/slave transmission and reception
- Bus arbitration function
- Clock synchronization function
- Restart generating function
- Bus error detecting function
- Programmable noise cancel function
- 10-bit/7-bit master/slave addressing
- Supports Standard mode (Max. 100Kbps) /HIGH-speed mode (Max.400Kbps)
- Support multi-master

Fig.5.1 shows the basic format of I²C bus transfer.

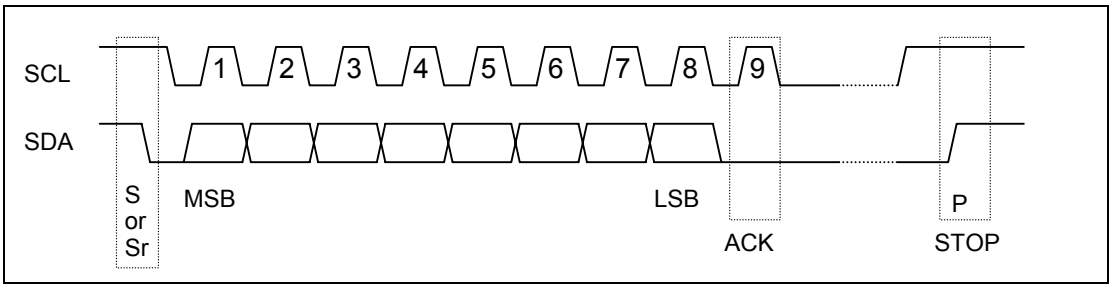


Fig.5.1 I²C Basic Format

[Precautions]
When ACK is returned from S1S60000, the response time fluctuates (because response is returned after processing with software inside S1S60000). During the time, S1S60000 maintains SCL at the LOW level to extend the period up to ACK. Note that the time varies with the internal processing state.

5.4.1 Master Function

Master function of S1S60000 supports the multi-master. When another master device is present on I²C bus, this function synchronizes the clock. Thus, as long another master device maintains SCL signal at LOW level, S1S60000 refrains from latching SDA. This arrangement enables to specify the minimum HIGH or LOW retaining period of SCL on I2CCONF register thereby allowing the I²C bus clock to change responding to the period.

• Procedure of communication with master device
Following describes the communication procedure when S1S60000 is the master and the external device is the slave.

[Procedure 1]
Addressing coding procedure
When the external device has the automatic address increment function, data can be continuously sent once the addressing is done at the start. The received address is added on byte basis.

(1) S1S60000 sends the start condition
(2) S1S60000 sends the slave address of the external device and R/W bit from the write mode
(3) Confirms acknowledge from the external device
(4) S1S60000 sends the address to be written to the external device
(5) Confirms acknowledge from the external device
(6) S1S60000 sends the data to be written to the address specified in step (4) above
(7) Confirms acknowledge from the external device
(8) Above (6) and (7) are repeated as needed. Addresses are automatically incremented in the external device.
(9) S1S60000 sends the stop condition

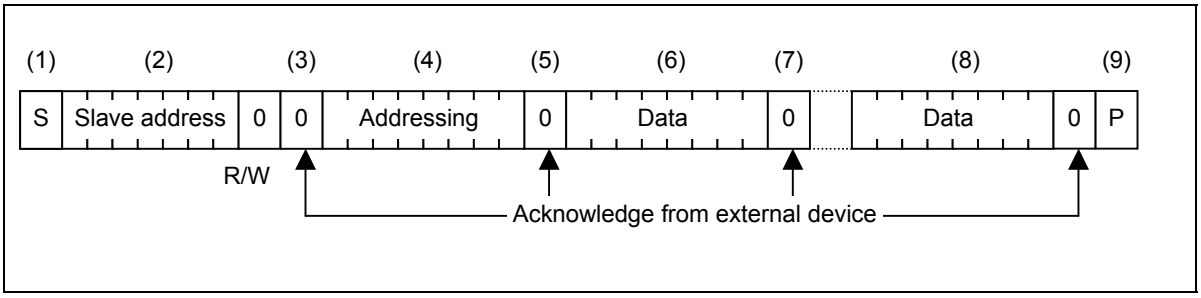


Fig.5.2 Writes Addressing as I²C Master

[Procedure 2]
Addressing read procedure
From the write mode, S1S60000 writes the address to be read and then turns on the read mode to read the actual data.

(1) S1S60000 sends the start condition
(2) S1S60000 sends the slave address of the external device and R/W bits from the write mode
(3) Confirms acknowledge from the external device
(4) S1S60000 sends the address to be written to the external device
(5) Confirms acknowledge from the external device
(6) S1S60000 sends the start condition (stop condition is not sent): Restart
(7) S1S60000 sends the slave address of the external device and R/W bits from the read mode
(8) Confirms acknowledge from the external device (from this step, S1S60000 becomes the receiver and the external device becomes the transmitter)
(9) The external device sends data of the address specified in (4) above
(10) S1S60000 sends acknowledge to the external device
(11) As needed, (9) and (10) are repeated. Addresses to be read are automatically incremented in the external device.
(12) S1S60000 sends "1" as acknowledge
(13) S1S60000 sends the stop condition

In the above steps, the restart in (6) is automatically generated if the upper bits for containing the transmit data are specified. And, acknowledge in (12) is automatically output as S1S60000 received every specified data.

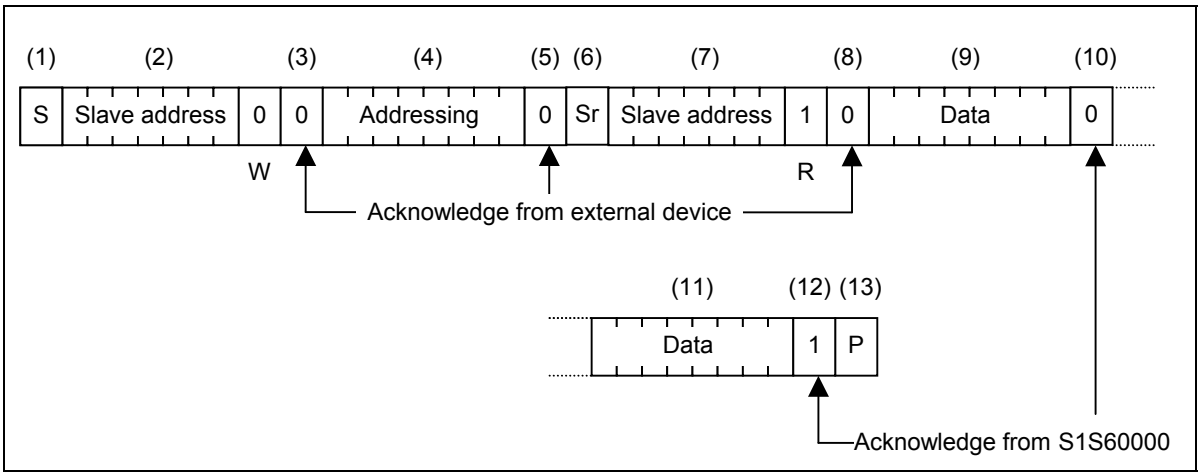


Fig.5.3 Reads Addressing as I²C Master

5.4.2 Slave Function

The slave address of S1S60000 is as shown below. This slave addresses is set on S1S60000 register I2CSADR. In bit [2:0], an address that does not compete against that of other connected devices is set.

Note: Since S1S60000 allows setting the slave address using software, it is possible to specify other address than shown in Table 5.14. However, user is requested not to try to use another address. When setting the address from EEPROM, the stipulated value is used for value other than bit [2:0].

Table 5.14 Slave Address

bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	1	1	0	X	X	X

Table 5.15 lists the built-in registers that are accessible as the slave devices. For detail of the built-in registers, refer to Chapter 5.2.

Table 5.15 I²C Slave Register Map

Address	Content	Address	Content
0h	Device ID (C3h)	22h	SNMSKH register LOW
1h	Revision (00h)	23h	SNMSKH register HIGH
2h	MAC0 register LOW	24h	SNMSKL register LOW
3h	MAC0 register HIGH	25h	SNMSKL register HIGH
4h	MAC1 register LOW	26h	DGWH register LOW
5h	MAC1 register HIGH	27h	DGWH register HIGH
6h	MAC2 register LOW	28h	DGWL register LOW
7h	MAC2 register HIGH	29h	DGWL register HIGH
8h	GENCR register LOW	2Ah	DADR0H register LOW
9h	GENCR register HIGH	2Bh	DADR0H register HIGH
Ah	HIFCR register LOW	2Ch	DADR0L register LOW
Bh	HIFCR register HIGH	2Dh	DADR0L register HIGH
Ch	GPALT register LOW	2Eh	DADR1H register LOW
Dh	GPALT register HIGH	2Fh	DADR1H register HIGH
Eh	GPCFG register LOW	30h	DADR1L register LOW
Fh	GPCFG register HIGH	31h	DADR1L register HIGH
10h	GPDAT register LOW	32h	DADR2H register LOW
11h	GPDAT register HIGH	33h	DADR2H register HIGH
12h	GPMSK register LOW	34h	DADR2L register LOW
13h	GPMSK register HIGH	35h	DADR2L register HIGH
14h	EPMSK register LOW	36h	DADR3H register LOW
15h	EPMSK register HIGH	37h	DADR3H register HIGH
16h	I2CMSK register LOW	38h	DADR3L register LOW
17h	I2CMSK register HIGH	39h	DADR3L register HIGH
18h	PMWAIT register LOW	3Ah	PORT register LOW
19h	PMWAIT register HIGH	3Bh	PORT register HIGH
1Ah	PHYMODE register LOW	3Ch	DPORT register LOW
1Bh	PHYMODE register HIGH	3Dh	DPORT register HIGH
1Ch	ANEGR register HIGH	3Eh	SERMODE register LOW
1Dh	ANEGR register LOW	3Fh	SERMODE register HIGH
1Eh	IPADRH register LOW	40h	TMOUT register LOW
1Fh	IPADRH register HIGH	41h	TMOUT register HIGH
20h	IPADRL register LOW	42h	SOPAR register LOW
21h	IPADRL register HIGH	43h	SOPAR register HIGH

• Communication Procedure as Slave Device

Following describes the communication procedure when the external device is the maser and S1S60000 is the slave.

[Procedure 1]

Addressing write procedure

S1S60000 has the automatic address increment function. So, after addressing is done at the start, data can be sent continuously. Addresses received by S1S60000 are incremented on byte basis.

(1) The master sends the start condition
(2) The master sends the slave address of S1S60000 and R/W bits from the write mode
(3) Confirms acknowledge from S1S60000
(4) The master sends the address to be written to S1S60000
(5) Confirms acknowledge from S1S60000
(6) Sends the data to be written to the address specified in (4) above
(7) Confirms acknowledge from S1S60000
(8) As needed, (6) and (7) are repeated. Addressed are automatically incremented in S1S60000.
(9) The mater sends the stop condition

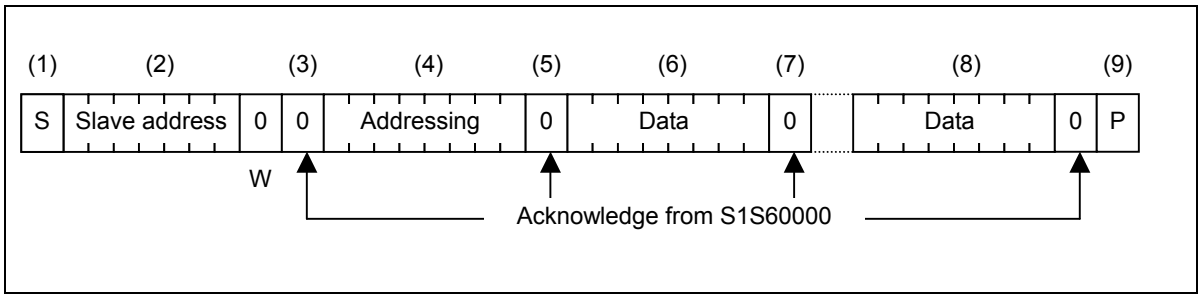


Fig.5.4 Addressing Write Procedure

[Procedure 2]

Addressing read procedure

S1S60000 writes the address to be read from the write mode and then turn on the read mode to read actual data.

(1) The master sends the start condition
(2) The master sends the slave address of S1S60000 and R/W bit from the write mode
(3) Confirms acknowledge from S1S60000
(4) The master sends address to be written to S1S60000
(5) Confirms acknowledge from S1S60000
(6) The master sends the start condition (stop condition is not sent): Restart
(7) The master sends the slave address of S1S60000 and R/W bit from the read mode
(8) Confirms acknowledge from S1S60000 (from this step, the master becomes the receiver and S1S60000 becomes the transmitter)
(9) S1S60000 sends the data of the address specified in (4) above
(10) The master sends acknowledge to S1S60000
(11) As needed, (9) and (10) are repeated. Read addresses are automatically incremented in S1S60000.
(12) The master sends "1" as acknowledge
(13) The master sends the stop condition

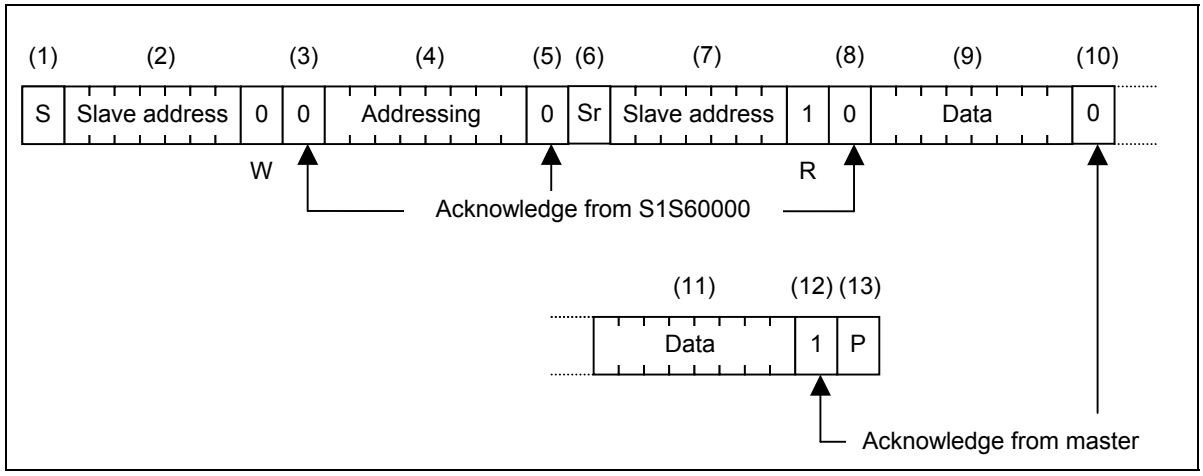


Fig.5.5 Addressing Read Procedure

[Procedure 3]
Read procedure when addressing is absent
Turning on the read mode first immediately enables the data read. In this case, the address to be accessed is +1 of the address being accessed the last.

(1) The master sends the start condition
(2) The master sends the slave address of S1S60000 and R/W bit from the read mode.
(3) Confirms acknowledge from S1S60000 (from this step, the master becomes the receiver and S1S60000 becomes the transmitter)
(4) S1S60000 sends the data of the address incremented by 1 from the address being accessed the last time
(5) The master sends acknowledge to S1S60000
(6) As needed, (4) and (5) are repeated. Read addresses are automatically incremented in S1S60000.
(7) The master sends "1" as the acknowledge
(8) The master sends the stop condition

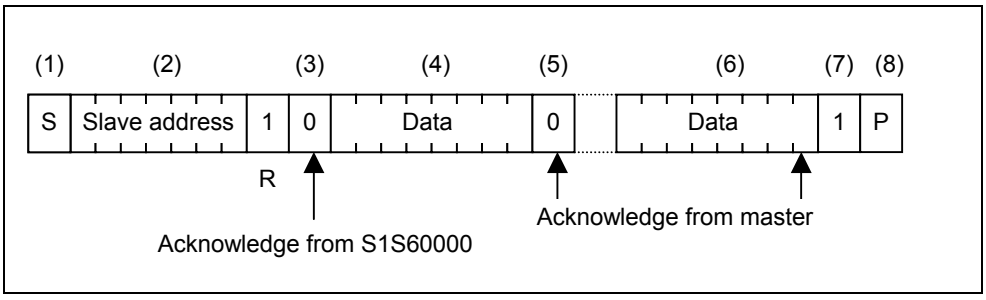


Fig.5.6 Read Procedure when Addressing is absent

5.5 EEPROM

5.5.1 EEPROM Specification

Following type of EEPROM is available.

- 3-Wire type (93C46 compatible type)
- +3.3V operation or +5V operation
- 16bit word

EEPROM interface block of S1S60000 structured to 5V tolerant. Thus, the products designed for supply voltage of +5V or +3.3V are usable.

5.5.2 Data Stored

Each data of EEPROM is of 16-bit width. Table 5.16 shows the data map of the area to be used by S1S60000. Data at Indices from 01h to 23h are set in the corresponding internal registers after the reset.

Table 5.16 EEPROM Data Map

Index	Data	Content
00h	ID	Fixed to 0xE0C3. In other cases than this value, a correct EEPROM judges non-existence of their values, and no access is possible. ※ This value has no relation with the ID of the built-in register.
01h	MAC0	Initial value of MAC register. For the content, refer to Chapter 5.2.2.
02h	MAC1	
03h	MAC2	
04h	GENCR	GENCR register set value. For the content, refer to Chapter5.2.3.
05h	HIFCR	HIFCR register set value. For the content, refer to Chapter 5.2.4.
06h	I2CSADR	I2CSADR register set value. For the content, refer to Chapter 5.2.5.
07h	I2CCONF	I2CCONF register set value. For the content, refer to Chapter 5.2.6.
08h	GPALT	GPALT register set value. For the content, refer to Chapter 5.2.7.
09h	GPCFG	GPCFG register set value. For the content, refer to Chapter 5.2.8.
0Ah	GPDAT	GPDAT register set value. For the content, refer to Chapter 5.2.9.
0Bh	GPMSK	GPMSK register set value. For the content, refer to Chapter 5.2.10.
0Ch	EPMSK	EPMSK register set value. For the content, refer to Chapter 5.2.11.
0Dh	I2CMSK	I2CMSK register set value. For the content, refer to Chapter 5.2.12.
0Eh	PMWAIT	PMWAIT register set value. For the content, refer to Chapter 5.2.13.
0Fh	PHYMODE	PHYMODE register set value. For the content, refer to Chapter 5.2.14.
10h	ANEGR	ANEGR register set value. For the content, refer to Chapter 5.2.15.
11h	IPADRH	IP Address: Initial value of own station's IP address. For the content, refer to Chapter 5.2.16.
12h	IPADRL	
13h	SNMSKH	Subnet Mask: Subnet mask initial value. For the content, refer to Chapter 5.2.17.
14h	SNMSKL	
15h	DGWH	Default Gateway: Default gateway initial value. For the content, refer to Chapter 5.2.18.
16h	DGWL	
17h	DADR0H	Destination IP Address 0: Destination address 0 is set. For the content, refer to Chapter 5.2.19.
18h	DADR0L	
19h	DADR1H	Destination IP Address 1: Destination address 1 is set. For the content, refer to Chapter 5.2.19.
1Ah	DADR1L	
1Bh	DADR2H	Destination IP Address 2: Destination address 2 is set. For the content, refer to Chapter 5.2.19.
1Ch	DADR2L	
1Dh	DADR3H	Destination IP Address 3: Destination address 3 is set. For the content, refer to Chapter 5.2.19.
1Eh	DADR3L	
1Fh	PORT	PORT register set value. For the content, refer to Chapter 5.2.20.
20h	DPORT	DPORT register set value. For the content, refer to Chapter 5.2.21.
21h	SERMODE	SERMODE register set value. For the content, refer to Chapter 5.2.22.
22h	TMOUT	TMOUT register set value. For the content, refer to Chapter 5.2.23.
23h	SOPAR	SOPAR register set value. For the content, refer to Chapter 5.2.24.
24h	COMN0	COMN0, COMN1, COMN2 and COMN3 register set value. For the content, refer to Chapter 5.2.25.
25h	COMN1	
26h	COMN2	
27h	COMN3	

Note: Access from network to the area from 00h to 10h for rewrite is prohibited at any time. Don't try to rewrite this area from network.

5.5.3 Transmission/Receiving Format

The commands sent from S1S60000 to EEPROM are read (READ:10), write enable (WEN:0011), write (WRITE:01) and write disable (WDS:0000).
Since EP_DI pin contains a pull-up resister, it remains at HIGH level as long as HIGH impedance mode is continued. Signal change of EP_CS,EP_DO and input to EP_DI take place at the negative-going edge of EP_SK.
After the addressing, read is started from data at EP_DI. Fig.5.7 shows timing of respective signals.

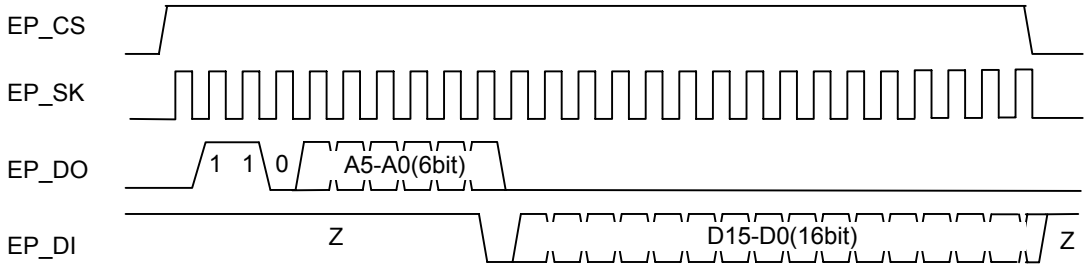


Fig.5.7 EEPROM (93C46) Read Format

When reading data, WEN is turned on first and then the WRITE command is issued. After data is output, the WRITE command sets EP_CS="0" once and then sets EP_CS="1" again to monitor EP_DI. Then it ends the operation after confirming that EP_DI="1" (Complete) referencing the hardware. WDS status is then restored. Fig.5.8 shows the timing at execution of the WRITE command.

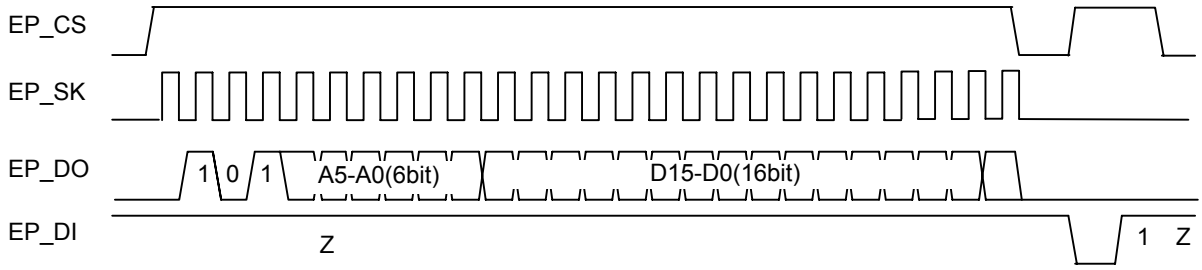


Fig.5.8 EEPROM (93C46) Write Format

5.5.4 Automatic Read

As S1S60000 is reset, automatic read from EEPROM is turned on starting with the data at address 0. When this data is E0C3h, data in the EEPROM is regarded valid and read is continued. Read data is set on respective registers. When EEPROM is not connected or the data read is not E0C3h, read is stopped and thus data is not set on the built-in registers.

6. POWER MANAGEMENT CONTROL

The power save mode and the sleep mode are available on S1S60000 as the power management mode. When turning on these modes, enable the corresponding bit of GENCR register and then, in case of the sleep mode, specify the timer value.

• Normal mode

It is the mode used for normal operation. The internal bus clock (=CPU clock) becomes twice the OSC3 clock.

• Power save mode

In this mode, the internal bus clock operates at 1/4 of the normal setting (1/2 of OSC3 clock) to reduce power consumption of S1S60000. You can enable this mode by setting "1" on bit 11 (PSEN) of GENCR register. Since the internal bus clock is modified, you must pay attention the related timing. If a necessary timing is not met, you must modify the setting.

(1) Setting of GENCR register ESKDIV (EEPROM Interface clock)
(2) Setting of GENCR register MDCDIV (MII management Interface clock)
(3) Setting of I2CCONF register SCLCNT (I^2C master clock)
(4) Host Interface sampling interval

Note: ・ As long as this mode is enabled, 100BASE-TX based communication is unavailable.
・ To change the ESKDIV settings, use a method that will not change the EEPROM initial values. After the EEPROM is reset, Auto Load sets the GENCR register and, until the system enters the power save mode, it operates with the clock that results from dividing the Normal mode clock with ESKDIV. During this time, the EP_SK clock may exceed the allowable input frequency of connected elements.

• Sleep mode

In this mode, core CPU operates on 32kHz of OSC1 and OSC3 circuit is stopped. Power consumption of S1S60000 is reduced to approximately 1/30 of the normal operation. You can stop external OSC by setting GPALT7 bit of GPALT register to "1" and connecting GPIO7 pin to the oscillation control pin (Active LOW) of external OSC. This arrangement further reduces the power consumption.
When enabling this mode, set SLPEN of GENCR register to "1" and then set the timer value (until this mode is turned on from the power down mode) on SLPWAIT (bit[11:8]) of PMWAIT register.

Note: Be sure to feed power while the sleep mode is turned on. If the operating supply voltage is not maintained, results of the succeeding operations become unpredictable.

The sleep mode is turned on in the following procedure.

(1) S1S60000 sends the sleep status notice to the host CPU
(2) Specifies GPIO0 as the recovery trigger input in order to prohibit interrupt from other
(3) Switching the Operation Clock to OSC1
(4) When GPIO7 is specified as OSCCTL, selects OSCCTL="0" in order to stop the external oscillator.
(5) Executes slp

Recovery starts when the LOW level is entered to GPIO0 and proceeds according to the following procedures:

(1) When GPIO7 is specified as OSCCTL, S1S60000 starts the external oscillator
(2) Starts up OSC3 oscillation circuit and waits until oscillation is stabilized
(3) Switching the Operation Clock to OSC3
(4) Sends the wake up status notice to the host CPU after recovery

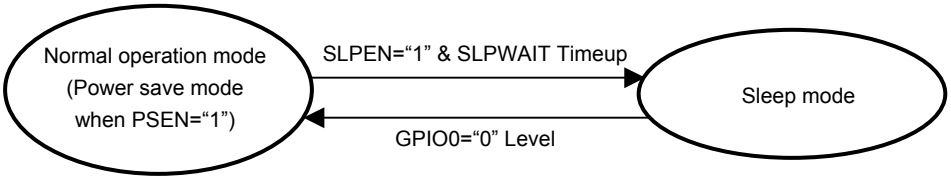


Fig.6.1 Power Management Status Transition

7. PRECAUTIONS ON IMPLEMENTATION

Following describes the precautions to be heeded when designing substrates and implementing ICs.

■ Oscillation circuit

- Oscillation characteristics vary depending on given conditions (such as parts used and substrate patterns). In particular, when using ceramic or crystal transducers, maker specified constants of components such as capacitance and resistance should be strictly observed.
- Disturbance of oscillation clock due to noises can cause malfunctioning. Pay attention to the following in order to prevent above trouble.
  (1) Be sure to minimize the distance when connecting parts such as transducer, resistor and capacitor to OSC3 (OSC1), OSC4 (OSC2) and PLLC pin.
  (2) Be sure to provide as much VSS pattern as possible to OSC3 (OSC1) and OSC4 (OSC2) pins as well as to peripheral areas of the parts connected to these pins. The same applies to PLLC pin, too. Don't try to connect non-oscillation system parts to this VSS pattern.
  (3) When entering external clock to OSC3 (OSC1) pin, be sure to minimize the distance from the clock source. In this case, OSC4 (OSC2) pin must be made open.
- In order to prevent unstable operation of the oscillation circuit due to leak current across OSC3 (OSC1) - VDD, be sure to locate OSC3(OSC1) sufficiently away from VDD power supply and signal line on the substrate pattern.
- When feeding clock to PHY chip by use of OSCO pin, try to minimize the pattern length. And, make sure that the clock satisfies the frequency accuracy required by PHY.

■ Reset circuit

- Reset signal entered to RESET# pin at powering on is affected by factors (such as turn on time of power supply, parts used and substrate patterns). Before employing the constants such as capacitance and resistance, be sure to test them carefully using applied products. As for the pull-up resister of RESET# pin, dispersion of resistance values must be carefully studied before finalizing the constant.
- In order to prevent the reset due to noise during operation, be sure to connect the parts such as capacitor and resistor to RESET# pin with the minimum distance.

■ Power supply circuit

- Sudden fluctuations in voltage due to noise can cause malfunctioning. In order to prevent above trouble, following rules should be observed.
  (1) Use the shortest and thickest pattern as much as practicable for the connection between power supply and VDD or VSS pin.
  (2) Connect VDD pin and VSS pin with the minimum distance when connecting a bypass capacitor across VDD - VSS.

■ Layout of signal line

- Don't route a large current signal line near to circuits susceptible to noise (such as oscillation circuit). This rule must be observed in order to prevent electromagnetic induced noise resulting from mutual inductance.
- If a HIGH-speed signal line is routed for a long distance in parallel with another signal line or if such line is routed across another line, noises can be generated from mutual interference between the signals resulting in the system malfunctioning. In particular, you must avoid routing a HIGH-speed signal line near to the circuits susceptible to noises.

■ Network block

- Don't route the signal lines for signals input to and output from PHY (such as TXP, TXN, RXP, and XN) near to the oscillation block.

■ Processing Unused Pins

- Unused GPIO pins should either be set for output, or their input levels should be fixed with pull-up or pull-down resistors. (Avoid connecting them directly to VDD or VSS. Inadvertently setting output could result in overcurrent flow and destruction of the chip.)
- If the environment contains lots of noise, pins should be provided with external pull-up/pull-down resistors even if they are provided with internal pull-up/pull-down. It recommends connecting the pull-up resistance not more than 10kΩ especially to a DSIO terminal.

8. ELECTRIC CHARACTERISTICS

8.1 Absolute Maximum Rating

(VSS=0V)

Item	Symbol	Condition	Rating	Unit	Note
Supply voltage	VDD		-0.3 to +4.0	V	
Input voltage	VI	Except FailSafe pin (*1)	-0.3 to VDD+0.5	V	
		FailSafe pin (*1)	-0.3 to +7.0	V	
HIGH level output current	IOH	1 pin	-10	mA	
		Total of all pins	-40	mA	
LOW level output current	IOL	1 pin	10	mA	
		Total of all pins	40	mA	
Storage temperature	TSTG		-65 to +150	°C	

*1: FailSafe pin = HCS#,HA[2:0],HD[15:0],HRD0#,HRD1#,HWR0#,HWR1#,GPIO[7:0],EP_DI

8.2 Recommended Operating Conditions

(VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage	VDD		3.00	—	3.60	V	
Input voltage	VI	Except FailSafe pin (*1)	VSS	—	VDD	V	
		FailSafe pin (*1)	VSS	—	5.5	V	1
CPU operating frequency	f_{CPU}		—	—	50	MHz	
LOW-speed oscillation operating frequency	f_{OSC1}		—	32.768	—	kHz	
Operating temperature	Ta	During normal operation.	-40	25	85	°C	
		When writing to Flash ROM	0	25	70	°C	
Input rise time (normal input)	tri		—	—	50	ns	
Input fall time (normal input)	tfi		—	—	50	ns	
Input rise time (Schmitt input)	tri		—	—	5	ms	
Input fall time (Schmitt input)	tfi		—	—	5	ms	

*1: FailSafe pin=HCS#,HA[2:0],HD[15:0],HRD0#,HRD1#,HWR0#,HWR1#,GPIO[7:0],EP_DI

Note : When “HIGH” level output is turned on, don’t apply external voltage HIGHer than the output voltage to FailSafe pin.

8.3 DC Characteristics

(Except where otherwise specified: V_{DD}=3.0V to 3.6V, Ta=-40°C to +85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
Static current consumption	I_{DDS}	Static state, Tj=85°C		—	—	120	μA	
Large leak current	I_{LI}			-1	—	1	μA	
Off-state leak current	I_{OZ}			-1	—	1	μA	
HIGH level output voltage	V_{OH}	I_{OH}=-2mA (Type1), I_{OH}=-6mA (Type2), V_{DD}=Min.		V_{DD} -0.4	—	—	V	
LOW level output voltage	V_{OL}	I_{OL}=2mA (Type1), I_{OL}=6mA (Type2), V_{DD}=Min.		—	—	0.4	V	
HIGH level input voltage	V_{IH}	CMOS level, V_{DD}=Max.		2.4	—	—	V	
LOW level input voltage	V_{IL}	CMOS level, V_{DD}=Min.		—	—	0.4	V	
Positive trigger input voltage	V_{T^+}	CMOS Schmitt, V_{DD}=Max.		1.1	—	2.4	V	
Negative trigger input voltage	V_{T^-}	CMOS Schmitt, V_{DD}=Min.		0.6	—	1.8	V	
Hysteresis voltage	V_H	CMOS Schmitt		0.1	—	—	V	
Pull-up resistor	R_{PU}	V_I=0V	Other than DSIO	80	200	480	kΩ	
			DSIO	40	100	240	kΩ	
Pull-down resistor	R_{PD}	V_I=V_{DD} (TEST0,TEST1)		40	100	240	kΩ	
Input pin capacitance	C_I	f=1MHz, V_{DD} =0V		—	—	10	pF	
Output pin capacitance	C_O	f=1MHz, V_{DD} =0V		—	—	10	pF	
Input/output pin capacitance	C_{IO}	f=1MHz, V_{DD} =0V		—	—	10	pF	

Note: For the characteristics of pins, refer to "Appendix B List of Pin Characteristics".

8.4 Current consumption

(Except where otherwise specified: V_{DD}=3.0V to 3.6V, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Current consumption	I_{DD1}	f_{CPU}=50MHz	—	100	120	mA	1
When power save mode is turned on	I_{DD2}	f_{CPU}=12.5MHz	—	80	100	mA	2
When sleep mode is turned on	I_{DD3}	OSC1 oscillation is 32.768kHz	—	30	120	mA	3

1: When transmission and reception are conducted at the same time by use f internal loop back.
2: OSC3 and OSC1 are operated.
3: OSC3 is stopped and OSC1 is operated.

8.5 AC Characteristics

8.5.1 Description of Symbols

t_{CYC}: Bus clock cycle time : Depends on OSC3 input value.
When OSC3 input = 25MHz, the internal bus clock = 50MHz : t_{CYC} = 20ns

8.5.2 AC Characteristics Measuring Condition

Signal detection level: Input signal HIGH level V_{IH}=V_{DD}-0.4V
LOW level V_{IL}=0.4V
Output signal HIGH level V_{OH}=1/2 V_{DD}
LOW level V_{OL}=1/2 V_{DD}
Following conditions are assumed when external clock is entered to OSC3
Input signal HIGH level V_{IH}=1/2 V_{DD}
LOW level V_{IL}=1/2 V_{DD}

Input signal waveform: Rise (10%→90%V_{DD}) 5ns
Fall (90%→10%V_{DD}) 5ns
Output load capacitance: C_L=50pF

8.5.3 AC Characteristics Table

■ **External clock input characteristics**

(Except where otherwise specified: V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C)

Item	Symbol	Min.	Max.	Unit	Note
HIGH-speed clock cycle time	t_{C3}	40	100	ns	
OSC3 clock input duty	t_{C3ED}	45	55	%	
OSC3 clock input rise time	t_{IF}	—	5	ns	
OSC3 clock input fall time	t_{IR}	—	5	ns	
Minimum reset pulse width	t_{RST}	6 t_{CYC}	—	ns	

■ **Input, output and input/output port**

(Except where otherwise specified: V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C)

Item	Symbol	Min.	Max.	Unit	Note
Input data setup time	t_{INPS}	20	—	ns	
Input data hold time	t_{INPH}	10	—	ns	
Output data delay time	t_{OUTD}	—	20	ns	

■ **Host interface**

(Except where otherwise specified: V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C)

Item	Symbol	Min.	Max.	Unit	Note
Host Interface access enabled period (HCS#,HA[2:0],HWR0#,HWR1#, HRD0#,HRD1#)	t_{HAV}	$2t_{CYC}$+5	—	ns	
Host Interface output data delay time	t_{HOD}	—	25	ns	
Host Interface output floating delay time	t_{HZD}	—	25	ns	
Host Interface interrupt output delay time	t_{HIOD}	—	20	ns	
Host Interface interrupt floating delay time	t_{HIZD}	—	20	ns	
Host Interface set input setup time	t_{HIS}	10	—	ns	
Host Interface set input hold time	t_{HID}	10	—	ns	

■ **MII**

(Except where otherwise specified: V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C)

Item	Symbol	Min.	Max.	Unit	Note
MII output data delay time	t_{TXD}	0	15	ns	
MII input data setup time	t_{RXS}	10	—	ns	
MII input data hold time	t_{RXH}	10	—	ns	
MDIO output delay	t_{MOD}	t_{CYC}	t_{CYC}+5	ns	
MDIO data setup time	t_{MIS}	3	—	ns	
MDIO data hold time	t_{MIH}	0	—	ns	

■ **Serial EEPROM**

(Except where otherwise specified: V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C)

Item	Symbol	Min.	Max.	Unit	Note
Input data setup time	t_{EIS}	15	—	ns	
Input data hold time	t_{EIH}	0	—	ns	
Output data delay time	t_{EOD}	—	5	ns	

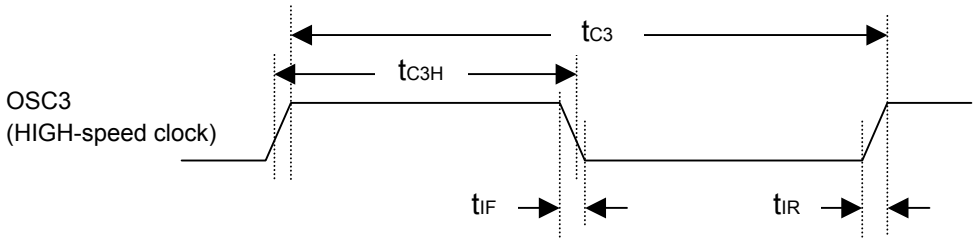
■ **I^2C bus**

(Except where otherwise specified: V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C)

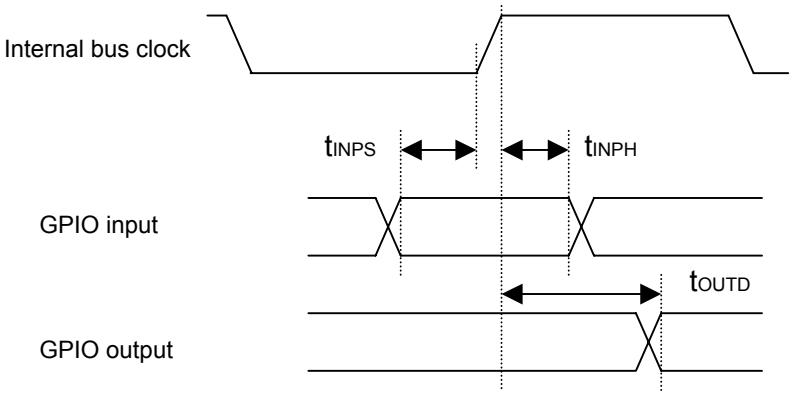
Item	Symbol	Min.	Max.	Unit	Note
SDA data setup time	t_{IIS}	5	—	ns	
SDA output delay time	t_{IOD}	$5t_{CYC}$	—	ns	

8.5.4 AC Characteristics Timing Chart

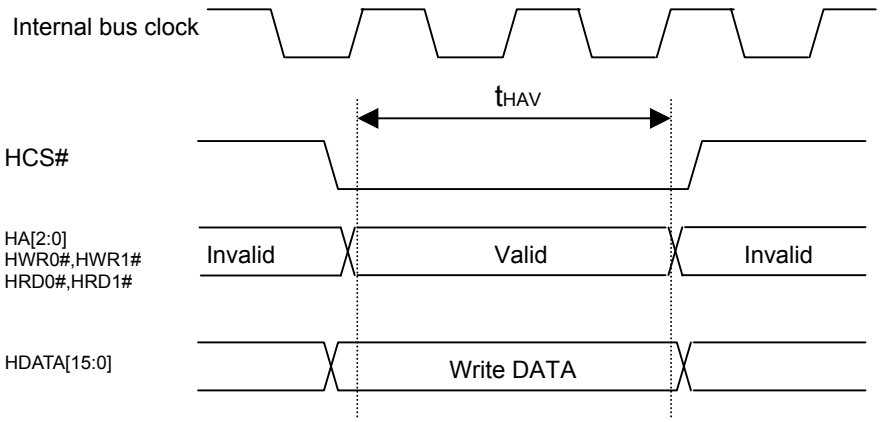
■ **Clock**



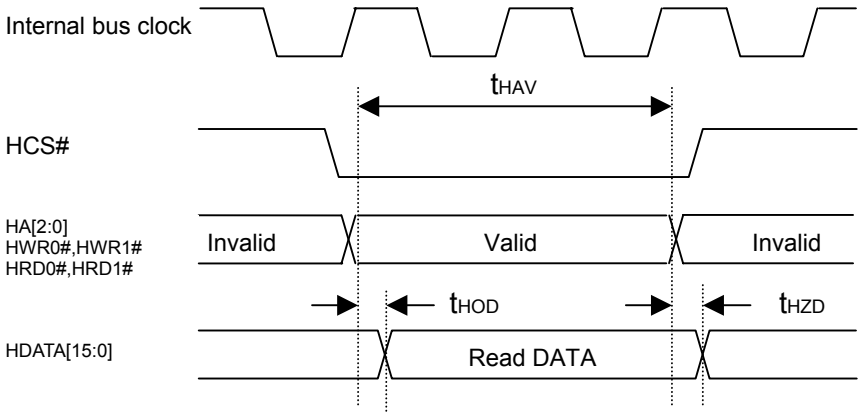
■ **Input, output, input/output port**



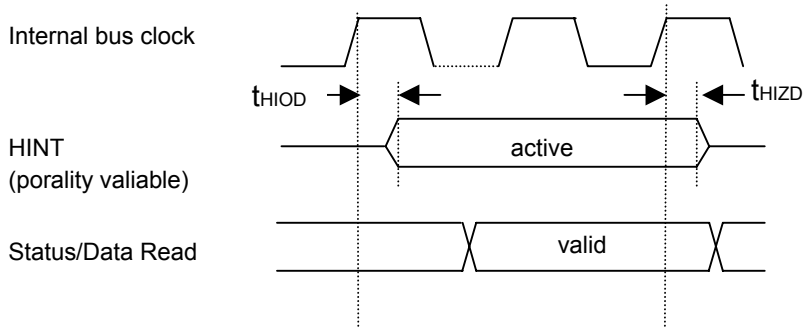
■ **Host interface (Write)**



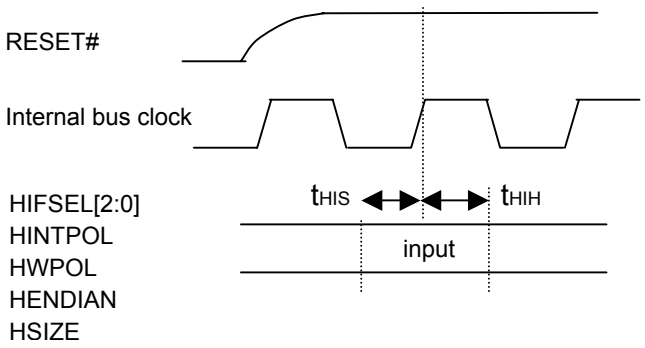
■ **Host interface (Read)**



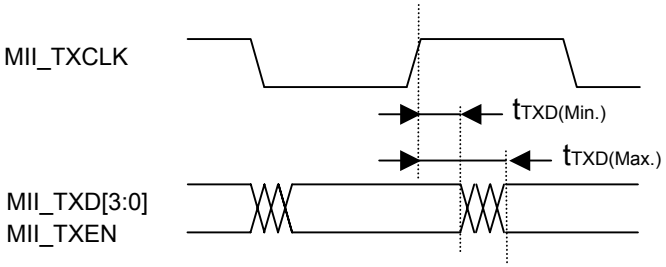
■ **Host interface (control line)**



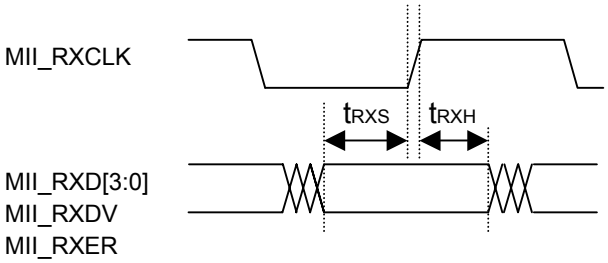
■ **Reset (set input)**



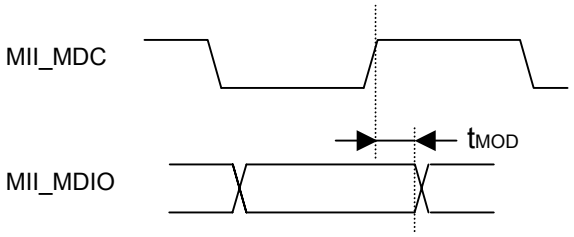
■ **MII transmit**



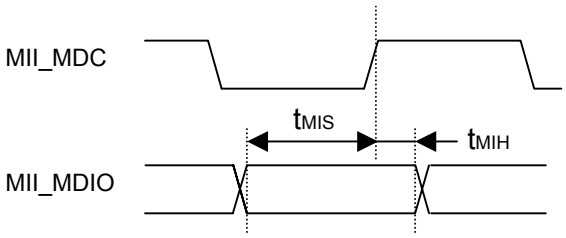
■ **MII receive**



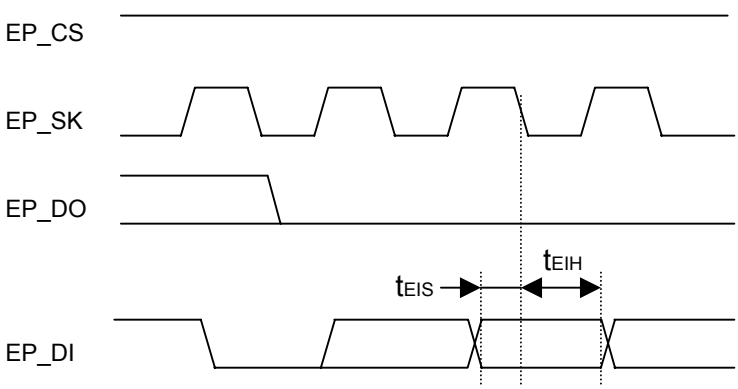
■ **MDIO output**



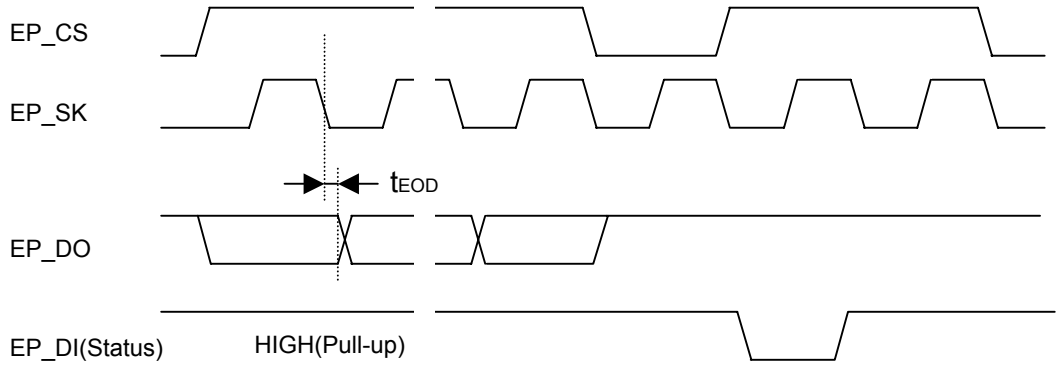
■ **MDIO input**



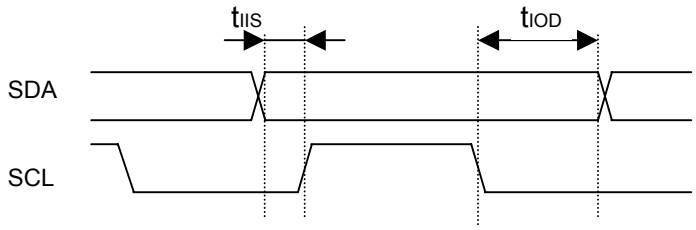
■ **Serial EEPROM (Read)**



■ **Serial EEPROM (Write)**



■ **I²C bus**



8.6 Oscillation Characteristics

Oscillation characteristics can vary depending various factors (such as parts used and substrate patterns). Following capacitance is for your information only. In particular, when using ceramic or crystal transducers, maker specified constants of components such as capacitance and resistance should be strictly observed.

■ OSC1 crystal oscillation

(Except where otherwise specified: Crystal transducer=C-002RX*1 32.768kHz, Rf1=20MΩ, C_{G1}=C_{D1}=15pF*2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating temperature	Ta	V_{DD}=3.0 to 3.6V	-40	—	85	°C	

*1 C-002RX: Crystal transducer from Seiko Epson *2 C_{G1}=C_{D1}=15pF includes capacitance of substrate.

(Except where otherwise specified: V_{DD}=3.3V, V_{SS}=0V, Crystal transducer = C-002RX*1 32.768kHz, Rf1=20MΩ, C_{G1}=C_{D1}=15pF*2, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	t_{STA1}		—	—	3	sec	
Capacitance of external gate and drain	C_{G1},C_{D1}	C_{G1}=C_{D1}, including capacitance of substrate	5	—	25	pF	
Frequency IC deviation	△f/ΔIC		-10	—	10	ppm	
Frequency supply voltage deviation	△f/ΔV		-10	—	10	ppm/V	
Frequency adjustment range	△f/ΔC_G	C_{G1}=C_{D1}=5 to 25pF	50	—	—	ppm	

*1 C-002RX: Crystal transducer from Seiko Epson *2 C_{G1}=C_{D1}=15pF includes capacitance of substrate.

■ OSC3 crystal oscillation

Note: For OSC3 crystal oscillation circuit, "a crystal transducer that operates on the fundamental frequency" must be used.

(Except where otherwise specified : V_{SS}=0V, crystal transducer =MA-306*1 25.000MHz, Rf1=20MΩ,C_{G1}=C_{D1}=15pF*2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	t_{STA3}	V_{DD}=3.3V	—	—	10	ms	

*1 MA-306: Crystal transducer from Seiko Epson *2 C_{G1}=C_{D1}=15pF includes capacitance of substrate.

■ OSC3 ceramic oscillation

(Except where otherwise specified : V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	t_{STA3}	25MHz ceramic transducer	—	—	5	ms	1

Note:

No	Ceramic transducer	Recommended constant			Supply voltage	Remarks
	Type name	C_{G2}(pF)	C_{D2}(pF)	Rf2(MΩ)	Range (V)	
1	CST25.00MXW0H1	5	5	1	2.7 to 3.6	Ceramic transducer from Murata Manufacturing

*1 Frequency tends to become higher by 0.3%.

8.7 PLL Characteristics

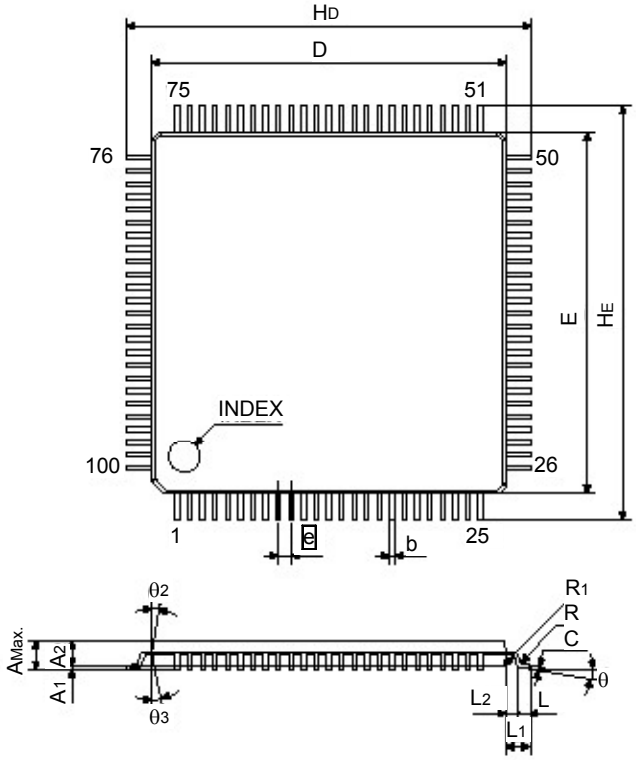
(Except where otherwise specified:V_{DD}=3.0 to 3.6V,V_{SS}=0V, Crystal transducer =SG-8002*1,C_1=100pF,C_2=5pF,Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Jitter (Peak jitter)	tpj		-1	—	1	ns	
Lockup time	tpll		—	—	1	ms	

*1 SG-8002: Crystal transducer from Seiko Epson

9. PACKAGE

QFP15-100pin : Plastic QFP 100pin Body size 14 × 14 × 1.4mm



Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	13.9	14	14.1
D	13.9	14	14.1
A			1.7
A_1		0.1	
A_2	1.3	1.4	1.5
e		0.5	
b	0.13	0.18	0.28
C	0.1	0.125	0.175
θ	0°		10°
L	0.3	0.5	0.7
L_1		1	
L_2		0.5	
H_E	15.7	16	16.3
H_D	15.7	16	16.3
θ_2		12°	
θ_3		12°	
R		0.2	
R_1		0.2	

∗ Restrictions on Power Consumption

Chip temperature goes higher as power consumption of LSI grows larger. Temperature of LSI chip in the package is calculated based on its ambient temperature Ta, heat resistance of package θj-a and power consumption PD as shown below.

Chip temperature (Tj) = Ta + (PD × θj-a) (°C)

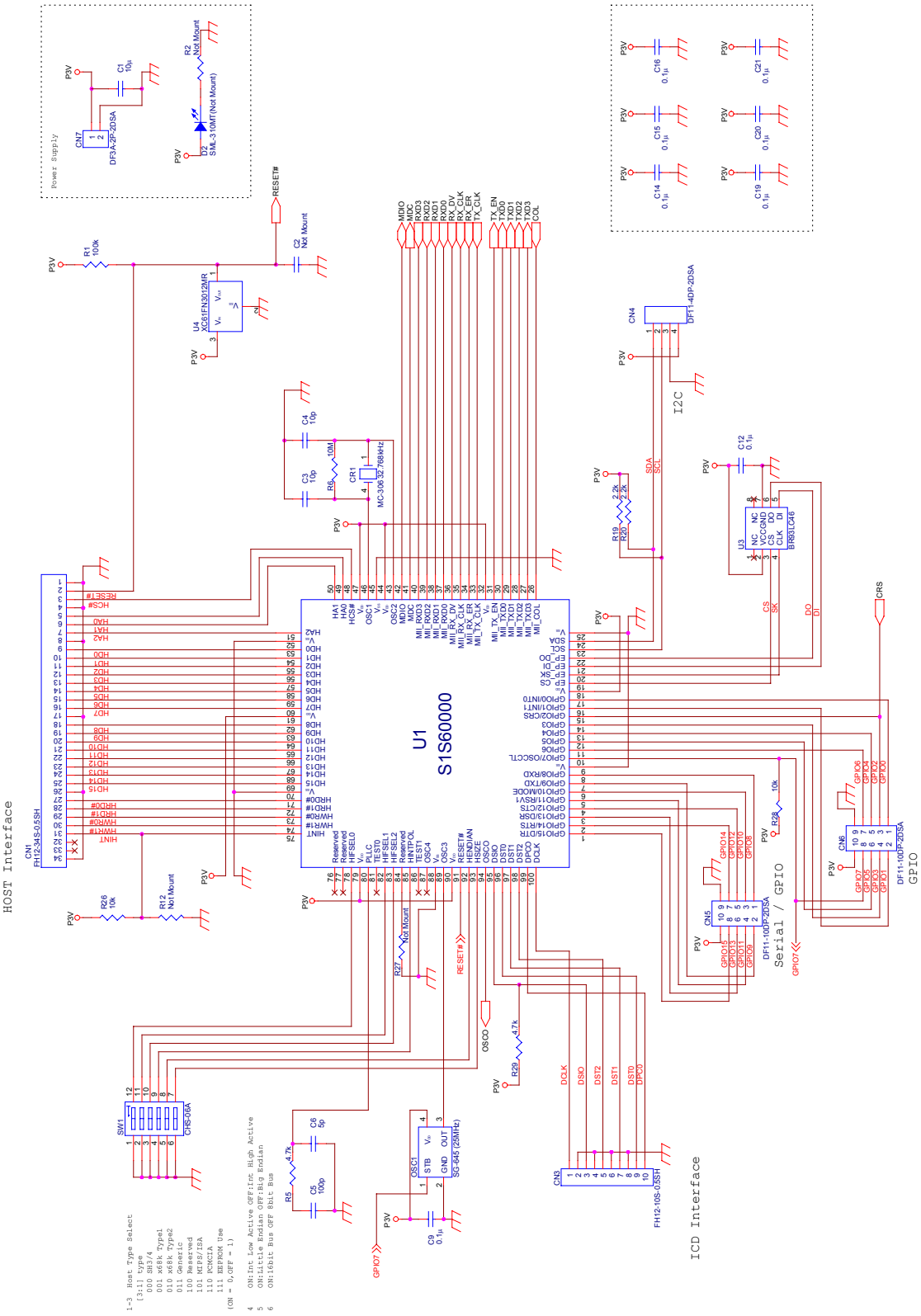
In the normal operation, it is recommended to maintain the chip temperature (Tj) below 85°C.

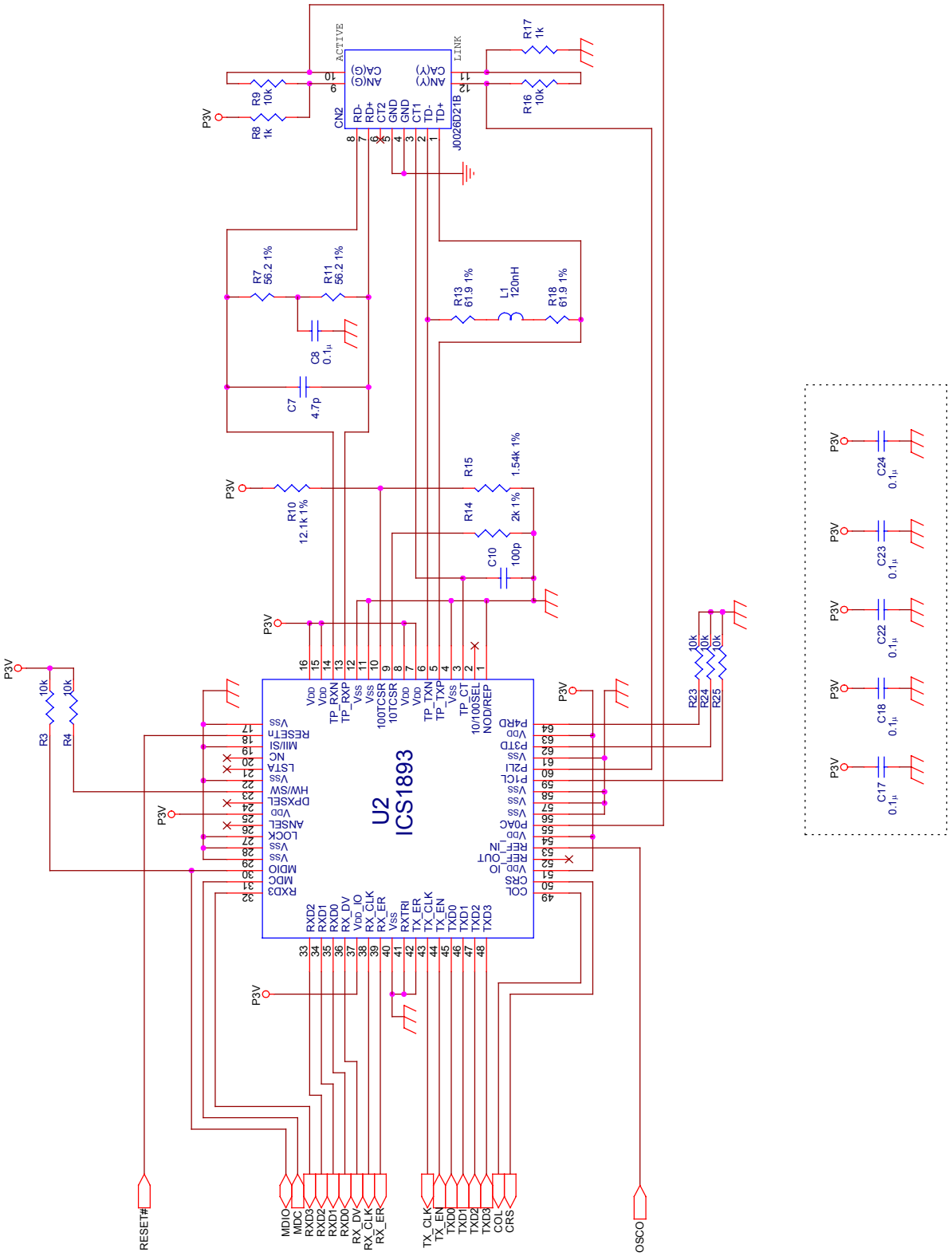
Following shows heat resistance of QFP15-100pin package.

Heat resistance θj-a = 100(°C /W)

Above heat resistance value is obtained from the sample hung in windless air. Heat resistance can vary significantly depending on how a package is implemented on the substrate as well as presence or absence of forced air-cooling.

APPENDIX A. REFERENCE CIRCUIT




U2
ICS1893
CN2
J0026D21B
ACTIVE
LINK
P3V
R3 10k
R4 10k
R7 56.2 1%
R11 56.2 1%
R8 1k
R9 10k
R10 12.1k 1%
R13 61.9 1%
L1 120nH
R18 61.9 1%
R17 1k
R16 10k
R15 1.54k 1%
R14 2k 1%
C7 4.7p
C8 0.1µ
C10 100p
R23 10k
R24 10k
R25 10k
C24 0.1µ
C23 0.1µ
C22 0.1µ
C18 0.1µ
C17 0.1µ
RESET#
MDIO
MDC
RXD3
RXD2
RXD1
RXD0
RX_DV
RX_CLK
RX_ER
TX_CLK
TX_EN
TXD0
TXD1
TXD2
TXD3
COL
CRS
OSCO

APPENDIX A. REFERENCE CIRCUIT

Bill of Material

No.	Name	Reference	Maker	Qty	Address	Note
101	S1S60000	100Pin QFP	EPSON	1	U1	
102	ICS1893Y-10	Ethernet PHY 64Pin TQFP	ICS	1	U2	
103	BR93LC46FV	Serial EEPROM 8Pin SSOP	ROHM	1	U3	
104	XC61FN3012MR	V-det. Nch 3.0V delay SOT-23	TOREX	1	U4	
301	SML-310FT	LED(Green)	ROHM	1	D2	Not imple-mented
402	MCR03EZHJ181	180 5% 1608	ROHM	1	R2	Not imple-mented
403	MCR03EZHJ102	1K 5% 1608	ROHM	2	R8,R17	
404	MCR03EZHJ222	2.2K 5% 1608	ROHM	2	R19,R20	
405	MCR03EZHJ472	4.7K 5% 1608	ROHM	1	R5,R29	
406	MCR03EZHJ103	10K 5% 1608	ROHM	9	R3,R4,R9,R16, R23-26,R28	
407	MCR03EZHJ104	100K 5% 1608	ROHM	1	R1	
408	MCR03EZHJ106	10M 5% 1608	ROHM	1	R6	
409	MCR03EZHF56R2	56.2 1% 1608	ROHM	2	R7,R11	
410	MCR03EZHF61R9	61.9 1% 1608	ROHM	2	R13,R18	
411	MCR03EZHF1541	1.54K 1% 1608	ROHM	1	R15	
412	MCR03EZHF2001	2K 1% 1608	ROHM	1	R14	
413	MCR03EZHF1212	12.1K 1% 1608	ROHM	1	R10	
414	MCR03EZHJ000	Not Mount 1608	—	1	R12,R27	Not imple-mented
415	MCR03EZHF1803	180K 1% 1608	ROHM	1	R21	
416	MCR03EZHF1803	220K 1% 1608	ROHM	1	R22	
501	GRM1882C1H4R7CZ01B	4.7pF 50V 1608	MURATA	1	C7	
502	GRM1882C1H5R0JZ01D	5pF 50V 1608	MURATA	1	C6	
503	GRM1882C1H100JZ01D	10pF 50V 1608	MURATA	2	C3,C4	
504	GRM1882C1H101JA01B	100pF 50V 1608	MURATA	2	C5,C10	
505	GRM188B11H103KA01D	0.01μF 50V 1608	MURATA	1	C2	Not imple-mented
507	GRM188B11H104KA01D	0.1μF 25V 1608	MURATA	14	C8,C9,C12, C14-C24	
508	GRM31CB11A106KC01L	10μF 10V 3225	MURATA	1	C1	
601	FH12-34S-0.5SH	34Pin FFC Connector	HIROSE	1	CN1	
602	J0026D21B	RJ45 Jack with Magnetics	PULSE	1	CN2	
603	FH12-10S-0.5SH	10Pin FFC Connector	HIROSE	1	CN3	
604	DF11-4DP-2DSA	4Pin Header (2×2, 2mm)	HIROSE	1	CN4	
605	DF11-10DP-2DSA	10Pin Header (5×2, 2mm)	HIROSE	2	CN5,CN6	
606	DF3A-2P-2DSA	2Pin Header (2mm)	HIROSE	1	CN7	
607	CHS-06A	6bit Dip Switch	COPAL	1	SW1	
701	SG-645 SCG 25.0MHz B	25.0MHz B(±50ppm) Standby	EPSON	1	OSC1	
703	MC-306	32.768KHz ±20ppm	EPSON	1	CR1	
704	ELJRER12JF3	120nH 1608	MATSUSHITA	1	L1	
799	PCB	4layer, t=1.6, FR-4		1		

Note: This reference circuit intended to show an example of use. It does not necessary warrant the operation.

APPENDIX B. LIST OF PIN CHARACTERISTICS

Pin	Signal name	I/O	I/O Cell	Input characteristics	Output characteristics	PU/PD	Type	Remarks
1	GPIO15	IO	XBH1T	CMOS SCHMITT	2mA		1	
2	GPIO14	IO	XBH1T	CMOS SCHMITT	2mA		1	
3	GPIO13	IO	XBH1T	CMOS SCHMITT	2mA		1	
4	GPIO12	IO	XBH1T	CMOS SCHMITT	2mA		1	
5	GPIO11	IO	XBH1T	CMOS SCHMITT	2mA		1	
6	GPIO10	IO	XBH1T	CMOS SCHMITT	2mA		1	
7	GPIO9	IO	XBH1T	CMOS SCHMITT	2mA		1	
8	GPIO8	IO	XBH1T	CMOS SCHMITT	2mA		1	
9	V_{SS}							
10	GPIO7	IO	XBB1	CMOS(Fail Safe)	2mA		1	
11	GPIO6	IO	XBB1	CMOS(Fail Safe)	2mA		1	
12	GPIO5	IO	XBB1	CMOS(Fail Safe)	2mA		1	
13	GPIO4	IO	XBB1	CMOS(Fail Safe)	2mA		1	
14	GPIO3	IO	XBB1	CMOS(Fail Safe)	2mA		1	
15	GPIO2	IO	XBB1	CMOS(Fail Safe)	2mA		1	
16	GPIO1	IO	XBB1	CMOS(Fail Safe)	2mA		1	
17	GPIO0	IO	XBB1	CMOS(Fail Safe)	2mA		1	
18	V_{DD}							
19	EP_CS	O	XBB1	CMOS(Fail Safe)	2mA		1	Note 1
20	EP_SK	O	XBB1	CMOS(Fail Safe)	2mA		1	Note 1
21	EP_DI	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
22	EP_DO	O	XBB1	CMOS(Fail Safe)	2mA		1	Note 1
23	SCL	IO	XBDH1T	CMOS SCHMITT	N-OD/2mA		1	
24	SDA	IO	XBDH1T	CMOS SCHMITT	N-OD/2mA		1	
25	V_{SS}							
26	MII_COL	I	XIBC	CMOS	—			
27	MII_TXD3	O	XOB1CT	—	2mA		1	
28	MII_TXD2	O	XOB1CT	—	2mA		1	
29	MII_TXD1	O	XOB1CT	—	2mA		1	
30	MII_TXD0	O	XBC1T	CMOS	2mA		1	Note 1
31	MII_TXEN	O	XBC1T	CMOS	2mA		1	Note 1
32	V_{DD}							
33	MII_TXCLK	I	XBC1T	CMOS	2mA		1	Note 2
34	MII_RXER	I	XBC1T	CMOS	2mA		1	Note 2
35	MII_RXCLK	I	XBC1T	CMOS	2mA		1	Note 2
36	MII_RXDV	I	XBC1T	CMOS	2mA		1	Note 2
37	MII_RXD0	I	XBC1T	CMOS	2mA		1	Note 2
38	MII_RXD1	I	XBC1T	CMOS	2mA		1	Note 2
39	MII_RXD2	I	XBC1T	CMOS	2mA		1	Note 2
40	MII_RXD3	I	XBC1T	CMOS	2mA		1	Note 2
41	MDC	O	XOB1CT	–	2mA		1	
42	MDIO	IO	XBC1T	CMOS	2mA		1	
43	OSC2	O	XLOT	TRANSPARENT	—			
44	V_{DD}							
45	V_{SS}							
46	OSC1	I	XLIN	TRANSPARENT	—			
47	V_{DD}							
48	HCS#	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
49	HA0	I	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	Note 2
50	HA1	I	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	Note 2

Pin	Signal name	I/O	I/O Cell	Input characteristics	Output characteristics	PU/PD	Type	Remarks
51	HA2	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
52	VSS							
53	HD0	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
54	HD1	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
55	HD2	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
56	HD3	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
57	HD4	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
58	HD5	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
59	HD6	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
60	HD7	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
61	VDD							
62	HD8	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
63	HD9	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
64	HD10	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
65	HD11	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
66	HD12	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
67	HD13	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
68	HD14	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
69	HD15	IO	XBB1P1	CMOS(Fail Safe)	2mA	Pull-up	1	
70	VSS							
71	HRD0#	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
72	HRD1#	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
73	HWR0#	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
74	HWR1#	I	XIBBP1	CMOS(Fail Safe)	—	Pull-up		
75	HINT	O	XTB1T	—	Tri/2mA		1	
76	Reserve	O	XTB1T	—	Tri/2mA		1	
77	Reserve	O	XTB1T	—	Tri/2mA		1	
78	HIFSEL0	I	XBH1P2T	CMOS SCHMITT	2mA	Pull-up	1	
79	VDD							
80	PLLC	I	XLIN	TRANSPARENT	—			
81	TEST0	I	XIBCD2	CMOS	—	Pull-down		
82	HIFSEL1	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
83	HIFSEL2	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
84	HMUX	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
85	HINTPOL	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
86	TEST1	I	XIBCD2	CMOS	—	Pull-down		
87	OSC4	O	XLOT	TRANSPARENT				
88	VSS							
89	OSC3	I	XLIN	TRANSPARENT	—			
90	VDD							
91	RESET#	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
92	HENDIAN	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
93	HSIZE	I	XIBHP2	CMOS SCHMITT	—	Pull-up		
94	OSCO	O	XBC2T	CMOS	6mA		1	Note 1
95	DSIO	IO	XBH2P2T	CMOS SCHMITT	6mA	Pull-up	2	
96	DST0	IO	XBH2T	CMOS SCHMITT	6mA		2	
97	DST1	IO	XBH2T	CMOS SCHMITT	6mA		2	
98	DST2	IO	XBH2T	CMOS SCHMITT	6mA		2	
99	DPCO	IO	XBH2T	CMOS SCHMITT	6mA		2	
100	DCLK	IO	XBH2T	CMOS SCHMITT	6mA		2	

Note 1: This pin is used as an input pin in the device test. In the normal operation, it is used as an output pin.
Note 2: This pin is used as an out pin in the device test. In the normal operation, it is used as an input pin.

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