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S1R72U16 FAQ

SEIKO EPSON CORPORATION

Rev.1.12

How to Use This FAQ

Reading all FAQs

"Chapter 1: ALL" contains all of the FAQs.

Reading FAQs by category

The FAQs listed in Chapter 1 are also arranged by category in Chapter 2 onward.
For example, see "Chapter 3: Power supply" for the FAQs related to power supply.

The categories can be seen in the Contents or in the Index bar.

Searching for FAQs by keyword

Use the PDF search function (Ctrl + F).
To facilitate searching, the FAQs include keywords not actually used within the text.

Table of Contents

1. ALL

Q 1.1 What clock frequency should be input?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.

Set the CLKSEL pin based on the clock used.

Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

There are no differences in performance, current consumption, and any other requirements due to frequency with either 12 MHz or 24 MHz selected.

Q 1.2 What is the CLKSEL pin used for?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.

Set the CLKSEL pin based on the clock used.

Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

Q 1.3 What level of accuracy is required for the clock frequency input?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Accuracy, Deviation, USB standard

A crystal oscillator accurate to within ± 100 ppm is recommended.

The USB 2.0 High Speed standard defines the frequency accuracy as ± 500 ppm. The frequency accuracy described above is recommended to ensure signal quality at the product level, since the USB signal waveform is greatly affected by clock jitter and frequency accuracy.

Q 1.4 What voltage is required for the power supply? Do any restrictions apply to the power on/off sequence?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

The USB requires HVDD (3.3 V), the LSI internal circuits require LVDD (1.8 V), and the system interface require IOVDD (1.8 to 3.3 V).

The LSI requires the above three power supplies, but the system can be configured using two power supplies by combining the IOVDD with another power supply, as shown below.

- If the system interface voltage is 3.3 V, the IOVDD can use the same power supply as the HVDD.
- If the system interface voltage is 1.8 V, the IOVDD can use the same power supply as the LVDD.

To ensure LSI reliability, we recommend turning the HVDD and IOVDD on or off with the LVDD provided, as described in the S1R72U16 Data Sheet. However, the HVDD or IOVDD may be turned on with the LVDD turned off, provided this is done for no more than 1 second.

This means that the IOVDD and LVDD may share the same power supply and that the HVDD may be used to regulate the LVDD, provided this interval is within the 1 second interval described above.

The power on/off timing is as shown below.

(→ Power on/off timing)

Q 1.5 What voltage should be used for the IOVDD in IDE mode?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

The IOVDD should be 3.3 V when in IDE mode.

Q 1.6 What is the exact state when power is turned off?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

This refers to the state in which no current is drawn by the LSI power supply, and the LSI is grounded.

Even if a potential difference persists due to a charged load, the power supply is deemed to be turned off if it is shut off from the exterior.

Q 1.7 Is an evaluation board available?

Keyword : Evaluation, Board, Circuit board, Bridge

Yes. An evaluation board is available for the IDE device - USB bridge. The S1R72U16 Evaluation Board Manual is also provided with the board. Please contact Seiko Epson Sales to obtain this evaluation board.

Q 1.8 Do you recommend any USB peripheral circuit pattern guides?

Keyword : USB, Peripheral circuit, Pattern

See the S1R72U16 USB 2.0 PCB Design Guide.

Q 1.9 Do you recommend any USB peripheral circuit protective components?

Keyword：USB, Peripheral circuit, Noise, Surge, EMI, Protective components, Components

See the S1R72U16 USB 2.0 PCB Design Guide.

Q 1.10 What are the actual transfer rates?

Keyword：Transfer rate

Transfer rates of up to 31 MB/s (248 Mbps) have been confirmed in tests done by Seiko Epson.

<Test conditions>
IDE host: PC IDE port
Benchmark software: HDBENCH

Since transfer rates depend on the IDE host (PC) and USB storage device used, these values cannot be guaranteed for the user's specific configuration.

Q 1.11 Are the pins Hi-z when the LSI power supply is turned off?

Keyword：Power supply, Pin, Power off, Shutoff, Hi-z

The pins do not switch to Hi-z when the LSI power supply is turned off.
A current path is formed to the LSI power supply via protective components and output transistors.

This means the following scenarios are possible if the main CPU power supply is on while LSI power supply is turned off.

- The main CPU cannot drive the bus to High.
- Main CPU current consumption increases.
- The LSI is powered by a rerouted power supply from the bus.

Q 1.12 What are the TEST pins used for? How should they be connected?

Keyword：TEST, Pin, Connection, Setting

These pins are not normally used by the user.

For detailed information on individual pin connection and setting, refer to “Pin Function Description” in the S1R72U16 Data Sheet.

Q 1.13 What are the DEBUG I/F pins used for? How should they be connected?

Keyword：DEBUG, Pin, Connection, Setting

These pins are not normally used by the user.

For detailed information on individual pin connection and setting, refer to “Pin Function Description” in the S1R72U16 Data Sheet.

Q 1.14 What are the Serial I/F pins used for? How should they be connected?

Keyword：Serial, Pin, Connection, Setting

These pins are used for simple debugging by the user during product (system) development by verifying connections to the main CPU and displaying the LSI processing history on a PC.
They are also used to launch authentication software for USB compliance testing.

For detailed information, refer to the S1R72U16 Development Support Manual and S1R72U16 Embedded Host Compliance Guide.
For detailed information on connection and setting, refer to the S1R72U16 Evaluation Board Manual.

Q 1.15 What are the GPI pins used for? How should they be connected?

Keyword：GPI, Pin, Connection, Setting

These pins are used to set the S1R72U16 operating mode.

For detailed information, refer to “Mode Settings” in the S1R72U16 Technical Manual.

Q 1.16 What are the GPO pins used for? How should they be connected?

Keyword：GPO, Pin, Connection, Setting

These pins are used for the following three main purposes:

- Indicating connection/disconnection and monitoring status to treat USB storage devices as removable devices
- Monitoring the start of PLL oscillation to confirm the LSI start-up state
- Indicating errors for USB compliance testing

For detailed information, refer to the S1R72U16 Technical Manual.

For detailed information on connection and setting, refer to the S1R72U16 Evaluation Board Manual.

Q 1.17 Are the IDE I/F pins 5 V tolerant?

Keyword：IDE, 5 V

No. This LSI is intended for 3.3 V interfaces.

Q 1.18 The crystal oscillator does not oscillate even after the power supply is turned on.

Keyword：Crystal, Oscillator, Resonator, Oscillation

Check the following:

- Are the power supplies providing the specified voltage?
- Has a reset (XRESET) been asserted?
- Does the crystal oscillator circuit have the correct circuit constants?

Q 1.19 PLL_Locked is not asserted even after the power supply is turned on.

Keyword：Crystal, Oscillator, Resonator, Oscillation, PLL

Check the following:

- Is the crystal oscillator oscillating?
- Are the power supplies providing the specified voltage?
- Has a reset (XRESET) been asserted?
- Does the crystal oscillator circuit have the correct circuit constants?

Q 1.20 Please explain USB 2.0 logo certification (compliance testing).

Keyword：USB, Logo, Certification, Compliance, Embedded Host

Refer to the S1R72U16 Embedded Host Compliance Guide.

Q 1.21 Please explain the crystal oscillator and crystal oscillator circuit.

Keyword：Crystal, Oscillator, Resonator, Oscillator circuit

Refer to the S1R72U16 USB 2.0 PCB Design Guide.
This document gives the recommended crystal devices and circuit constants.

Q 1.22 What precautions are necessary with resets?

Keyword：Reset

The precautions are the same as for regular resets.

The LSI status will not be established unless a reset is input. It should be reset when power is turned on and the reset canceled after the power supply has been established. (Power-on reset)

The reset input when turning on power should be a signal with a pulse width that satisfies the AC timing described in the S1R72U16 Data Sheet.

Note that a reset is not triggered accidentally by noise, etc. when the LSI is operating.

Q 1.23 Please explain the specifics of the USB power switch IC. Can this be formed using a discrete component without using the dedicated IC?

Keyword：USB, VBUS, Power switch, High side switch

For more information on USB power switches, refer to the S1R72U16 USB 2.0 PCB Design Guide.

Functions can be achieved using discrete components, but no application examples are provided. The user is responsible for determining the configuration.

Q 1.24 How do I obtain the IDE driver?

Keyword：IDE, ATA/ATAPI, Driver

Please contact the retailer from whom you purchased the file system.

Seiko Epson provides sample code with settings for CPU bus connections. The code can be downloaded on web site.

Q 1.25 Can I use an FS USB hub?

Keyword：USB, Hub, FS

Yes. However, note that transfers to and from USB storage devices connected to an FS hub will be FS, even if the device is HS.

Q 1.26 This is the first time we've attempted to design a USB board. Are there any reference materials?

Keyword：USB, Board, PCB

Refer to the S1R72U16 USB 2.0 PCB Design Guide.

Q 1.27 What kinds of USB devices can I connect? Can I connect USB memory and USB mouse devices?

Keyword：USB, Device, Memory, Mouse, HDD, Storage

Storage devices such as USB memory and hubs can be connected, but not USB mouse devices.

For detailed information, refer to the S1R72U16 Technical Manual.

Q 1.28 Can the LSI be used without an IDE host?

Keyword：IDE, ATA/ATAPI, CPU, Bus

Yes, by connecting to the CPU memory bus. For detailed information on bus connections, refer to the S1R72U16 Evaluation Board Manual. For detailed information on control methods, refer to the S1R72U16 Application Note.

The protocol complies with ATA/ATAPI, allowing control using an IDE driver.

Seiko Epson provides sample code for CPU bus connection. The code can be downloaded on web site.

Q 1.29 How should the CPU bus be connected?

Keyword：CPU bus

Connect to the CPU memory bus. For detailed information on bus connections, refer to the S1R72U16 Evaluation Board Manual. For detailed information on control methods, refer to the S1R72U16 Application Note.

The protocol complies with ATA/ATAPI, allowing control using an IDE driver.

Seiko Epson provides sample code for CPU bus connection. The code can be downloaded on web site.

Q 1.30 Please explain the DMA details for CPU bus connections.

Keyword：CPU, Bus, DMA

This is basically the same as for IDE Multi Word DMA. Transfer uses request and acknowledge handshakes. Both request and acknowledge are negative logic signals.

Precautions for using DMA are given below. CPUs contain a wide range of DMAC. The user should determine whether DMA transfer is possible and whether external logic is present. If DMA cannot be used, transfer data using PIO.

- Connections are normally not possible to CPUs featuring DMAC with no acknowledge or with edge triggers.
- External logic is required when connecting to CPUs featuring DMAC asserted by CS during DMA.

Q 1.31 The system includes a 12 MHz (24 MHz) clock. Is it possible to connect the clock input directly without using a crystal oscillator?

Keyword：Clock, Crystal, Oscillator, Resonator

We recommend using a crystal oscillator to ensure satisfactory USB signal quality. Note the following points if connecting the clock input directly (in which case the user is responsible for determining suitability).

- Connect the clock input to the XI pin.
- The input level is 1.8 V.
- The clock accuracy should be within ± 100 ppm.
- Hold the XO pin open, and avoid applying a load when a mounted land is provided.

For detailed information on clock duty, refer to the AC characteristics section in the S1R72U16 Data Sheet.

No restrictions apply to rise/fall time and jitter. The need for clock input should be determined based on the precautions above.

Q 1.32 What does the term “storage device” refer to?

Keyword：USB, Storage memory, HDD, CD, DVD

This is the general term applied to USB storage devices, including USB memory, USB-HDD, USB-CD, and USB-DVD devices.

Q 1.33 Can vendor commands be issued to storage devices?

Keyword：ATA, IDE, Vendor, Command, Unsupported

This LSI treats unsupported commands as vendor commands and issues them to the storage devices.

This means unique control is possible using vendor commands, except for data transfer.

For detailed information, refer to “Processing Unsupported Commands” in the S1R72U16 Technical Manual.

Q 1.34 What happens when unsupported commands are issued?

Keyword：ATA, IDE, Vendor, Command, Unsupported

This LSI treats unsupported commands as vendor commands and issues them to the storage devices.

This means unique control is possible using vendor commands, except for data transfer.

For detailed information, refer to “Processing Unsupported Commands” in the S1R72U16 Technical Manual.

Q 1.35 What happens if a command is issued when no storage device is connected?

Keyword：ATA, IDE, Command, Status

An error status will be returned for commands such as Read or Write attempting to access a storage device. A normal status will be returned for all other commands, which are processed within the LSI.

For detailed information, refer to “Supported Command List” in the S1R72U16 Technical Manual.

Q 1.36 How does IDE implement support for USB storage device connections/ disconnections?

Keyword：Connection, Disconnection, Connection/Disconnection, Removable, Driver

This LSI includes pins for informing the system of the USB storage device connection status.

Use these pins together with connection/disconnection processing in the application.

Support can also be implemented without using these pins by using a driver supporting ATA/ATAPI removable devices.

Q 1.37 An HDD is connected to the Main CPU as IDE master. Can this LSI be connected to the Main CPU as IDE slave?

Keyword：ATA, IDE, Master, Slave, HDD, Connection

Yes. For detailed information, refer to “System Configuration Examples” in the S1R72U16 Application Note.

Q 1.38 Is there a limit to the capacity of USB storage devices that can be connected?

Keyword：Storage, Capacity, Drive

Less than 2 Tbytes for E100; up to 2 Tbytes for E200.

This means USB storage devices of 137 GB or larger can be used as Big Drive devices.

Q 1.39 How should TPL data be prepared?

Keyword：USB, Logo, Certification, Compliance, Embedded host, TPL

A TPL generation tool can be downloaded on web site.

Q 1.40 Does USB support hot plugs?

Keyword：Hot plug

Yes.

Q 1.41 Is there a limit on the number of USB devices that can be connected?

Keyword：Constraint, Restriction, Device number, Connection

Up to two (master/slave) USB storage devices can be connected via the USB hub. Additional connected devices will be ignored by this LSI. Up to three HUBs can be connected. This LSI ignores additional connected HUBs.

Q 1.42 What constraints or precautions are associated with the main system file system?

Keyword：Constraint, File system

No particular constraints apply. (The LSI will return an error if a write/read attempt is made while the USB device is disconnected.)

Q 1.43 Is the driver source code endian-dependent?

Keyword：Sample, Driver, Endian, Source, Code

Yes. It assumes little-endian.

Q 1.44 Can USB floppy disk drives be used?

Keyword：Mass storage class, MSC, Restriction, Constraint, Floppy, Storage

No. The LSI does not support floppy disk drives (UFI subclass devices).

Q 1.45 Does the S1R72U16 ever negate DMARQ before the specified transfer has been completed? If so, when does this occur?

Keyword：IDE, DMARQ, DMA transfer, Terminate

DMARQ is negated in either of the following conditions.

1. If the IDE host performs a host terminate
2. If the IDE host exceeds 8 Mbytes (800000h) in the Read direction (LSI to Main CPU)

DMARQ is negated for each 8 Mbyte transfer if a data transfer is requested.

Ex: If the Main CPU issues a READ command for 24 Mbytes, the LSI divides the 24 Mbytes of data into three.

DMARQ is therefore negated twice during UltraDMA transfer.

For conditions other than those described above, the DMARQ signal is not negated before the specified transfer is completed.

In the case of WRITE, only condition 1 above applies for negating the DMARQ signal, since the LSI usage restrictions limit the maximum size of data that can be requested to 8 Mbytes.

Q 1.46 Does the S1R72U16 ever negate DMARQ if the USB bus is defective, resulting in repeated packet errors?

Keyword：IDE, DMARQ, DMA transfer, Packet error, Transfer error

DMARQ is not negated even if packet errors occur during DMARQ assertion.

DMARQ will be treated as follows depending on the timing of the NAK returned continuously by the READ command.

1. If NAK is returned continuously for CBW command issue

DMARQ is not asserted and the LSI does not start UltraDMA transfer.

The status register will be BSY=1 and DRQ=0.

2. If NAK is returned continuously for the first BulkIN transfer after CBW issue

Same as for 1.

3. If NAK is returned continuously after ACK has been returned at least once for first BulkIN transfer

DMARQ is asserted and UltraDMA transfer is not completed.

The status register will be BSY=0 and DRQ=1.

4. If NAK is returned repeatedly for the CSW (status) issued

The UltraDMA transfer will end, but the Status register will show BSY=1, DRQ=0.

The same applies for the WRITE command also.

Q 1.47 Are there any figures for transfer rates for CPU bus connections?

Keyword：Transfer rate, Transfer speed, CPU bus, Memory bus

No figures area available for transfer rates. Actual transfer rates will depend on the user's system configuration, including access to devices other than the LSI (e.g., ROM/RAM).

The theoretical maximum value is 16.6 Mbytes/s, as the AC specifications are the same as for the IDE bus PIO.

No measurement data is available, but the actual transfer rate should be less than half, even under ideal conditions.

Q 1.48 Are ATA/ATAPI commands used to control the S1R72U16? Which commands should be used?

Keyword：IDE, ATA, ATAPI, Command

Yes. ATA/ATAPI commands are used.

Use ATAPI commands if a CD or DVD drive is connected.

Either may be used with a USB memory or HDD connected. Select the command to suit the driver included with the file system or main CPU used.

Q 1.49 How are ATA/ATAPI commands processed? Is there any information available describing the basic details?

Keyword：IDE, ATA, ATAPI, Command

The basic arrangement consists of issuing a command, reading/writing data, and setting operating settings.

Consult published general instruction manuals, which provide more specific information. Also refer to the Epson Sample Driver reference.

Q 1.50 Can the LSI be used connected to a PC IDE port?

Keyword：PC, IDE

This LSI uses a 3.3 V I/F. It can be connected provided the PC I/F voltage is 3.3 V. Note that most desktop PCs have a 5 V I/F; check the voltage before connecting the LSI.

Use the following settings when connecting to a PC.

- IDE mode: CPUxIDE pin = “0”
- ATAPI mode: ATAxATAPI pin = “0”
- Single device mode: 2x1 pin = “0”

Also, set CSEL_T pin according to whether the device is used as Master (CSEL_T pin = “0”) or as Slave (CSEL_T pin = “1”).

Q 1.51 Does the S1R72U16 contain a file system?

Keyword：File system

This LSI does not include a file system. The file system must be mounted on the user's system.

Q 1.52 Are any specific procedures required to use the S1R72U16 and install the USB Host functions in a product? Can certification be requested at any time?

Keyword：USB, Certification, Compliance

No special procedures are required to create products that simply involve connecting devices such as USB memory. You must obtain USB certification to use the familiar USB logo with specific products. For information on obtaining USB certification, see the S1R72U16 Embedded Host Compliance Guide.

Certification can be requested at any time. Refer to the certification body for details.

Q 1.53 Can the main CPU obtain the Vendor ID and Product ID of USB devices connected to the S1R72U16? If not, is there a way to obtain identifying information about USB devices?

Keyword：USB, Device, ID, Identifying information

The CPU cannot obtain the Vendor ID or Product ID of USB devices.

However, identifying information about connected USB devices can be obtained using the IDENTIFY DEVICE, IDENTIFY PACKET DEVICE, and INQUIRY commands if the information exists in the command parameters. For details of the identifying information that can be obtained, see the section on specifications for information returned for each command in the S1R72U16 Technical Manual.

Q 1.54 Is there a way to restrict connections to specific USB devices?

Keyword：USB, Device, TPL, Restriction, Specific

Yes. This LSI includes a function that restricts the devices that can be connected by determining USB device information.

See the TPL section in the S1R72U16 Technical Manual or the section on downloading in S1R72U16 Application Note.

Q 1.55 Is there a way to determine whether a download was successful for the DOWNLOAD MICROCODE command or to determine whether correct or corrupted Update data was loaded?

Keyword：Download, ATA, Command, Update

The status value can be used to check whether a command was successfully completed.

An error status is returned if the download fails.

The Update data includes a CRC value. The validity of the data is compared against the calculated CRC value. An error status is returned if the CRC values fail to match.

Q 1.56 What is the purpose of the common mode choke coil included in the DP/DM? Is it intended to prevent DP/DM degradation due to external noise?

Keyword：Common mode, Choke coil, Board, Prevention, Noise

The common mode choke coil is intended to minimize common mode noise. It does not directly prevent DP/DM degradation.

Note that common mode noise occurs when a current (common mode current) flows in the same direction in the differential signal line.

Q 1.57 Is it possible to connect an HS USB device as an FS device?

Keyword：Hub, HS, FS, Device

The LSI does not provide this function.

It is possible to connect the device as an FS device via an FS hub, as shown below.

72U16 ⇔ FS hub ⇔ HS device

Q 1.58 What is the maximum current consumption?

Keyword：Current consumption, Maximum

The maximum current consumption will depend on usage (i.e., user's board design and bus load), so no specific figure can be given.

The power supply should generally be selected to provide approximately 1.5 times the typical value appropriate for the customer's board.

Current consumption varies with temperature, power supply voltage, and individual LSIs, but maximum current consumption should generally not exceed 1.5 times the typical value.

The data sheet only stipulates typical values for maximum operational load using the Seiko Epson evaluation setup.

Q 1.59 What is power consumption?

Keyword：Power consumption

Refer to the S1R72U16 Data Sheet.

The power consumption value can be obtained by calculating power supply voltage x power supply current.

Q 1.60 What is the margin for AC characteristics CPUIF timing (e.g. address, data setup/hold)?

Keyword：AC characteristics, Timing, Margin

This normally complies with ATA/ATAPI standards, since circuits are shared in CPU and IDE modes.

Comply with AC characteristics.

Q 1.61 Are there any reference materials for board design?

Keyword：PCB, Board design, Design guide

For detailed information on package and pin functions, refer to S1R72U16 Data Sheet.

For detailed information on USB peripheral circuit design, refer to the S1R72U16 USB 2.0 PCB Design Guide.

For detailed information on other overall board design and recommended circuits, refer to the S1R72U16 Evaluation Board Manual.

This FAQ (Board design) also provides details on setting and other processing of unused pins.

Q 1.62 Please explain noise countermeasures and static electricity protection products.

Keyword：Noise, Static electricity

The main noise countermeasure is a common mode coil provided in the DP/DM line, which suppresses current flowing in the same direction in the differential signal line. This improves DP/DM signal phase offset and voltage differences and prevents common mode noise.

Common mode impedance should ideally be 90 Ω with a small DC resistance component.

Protection against static electricity is generally provided by including a chip varistor in the DP/DM line. As a general rule, this should be less than 10 pF for USB HS, since high static capacitance may affect USB signal wave quality.

The varistor voltage must be higher than the USB amplitude maximum voltage of 3.6 V.

In either case, the product's ability to support USB 2.0 should also be a factor when considering component selection.

Q 1.63 Operation is not as expected. Is there an archive of past questions and problems?

Keyword：Past cases, Case studies

Details of past problems are available. Please check whether the problem in this case corresponds to any particular past problem.

(→ Details of past problems)

Q 1.64 How should unused pins be handled?

Keyword：Unused, Pin treatment

Refer to the table below.

(→ Unused pin treatment)

Q 1.65 How should the CSEL_T and 2x1 pins be set?

Keyword：Mode, Pin settings

For individual pin functions, refer to S1R72U16 Data Sheet.

1. When an IDE device and the S1R72U16 are connected to a host on the IDE bus in IDE mode, set the 2x1 pin to single-device mode (“0”) and CSEL_T pin to master (“0”) or slave (“1”) as required.

2. When connecting the S1R72U16 only on the IDE bus in IDE mode, set the 2x1 pin to 2-device mode (“1”) and CSEL_T pin to master (“0”). You can also use this setting either when only one USB device is connected downstream of the S1R72U16 or when two USB devices are connected using a hub downstream of the S1R72U16.

3. When connecting in CPU mode, the settings are the same as for 2.

Q 1.66 How should the XINT (interrupt request) signal be used when connecting in CPU mode?

Keyword：CPUIF, CPU bus, Memory bus, Interrupt

The XINT pin corresponds to the ATA/ATAPI standard INTRQ signal and is used to indicate Status register status changes.

For details, refer to the ATA/ATAPI standard.

Interrupts should be used with a level sense method.

Interrupts are not required to check Status register status changes when polling the ATA register. In this case, it should be set to Open.

Q 1.67 How should the XHRESET signal be used when connecting in CPU mode?

Keyword：CPUIF, CPU bus, Memory bus, Reset

XHRESET corresponds to the ATA/ATAPI standard Hardware Reset and is used to abort (bus reset) an ATA/ATAPI command when initializing or operating the IDE device. Use this signal for command timeout and other processing.

For details, refer to the ATA/ATAPI standard.

For details of hardware reset operations with the S1R72U16, refer to "2.4 Operation Specifications for Resetting" in the S1R72U16 Technical Manual. (The Hardware reset will not clear data downloaded with the DOWNLOAD MICROCODE command.)

The signal assert time will be at least 25 μs (ATA/ATAPI standard value).

Pull up if no bus reset is used.

Note that the function differs from the chip reset XRESET pin.

Q 1.68 Do any particular precautions apply for USB board design?

Keyword：USB, Board, PCB

Refer to S1R72U16 USB 2.0 PCB Design Guide.

Check the following points when seeking to improve analog waveforms.

- Is the power supply noise-free?
- Have you installed decoupling capacitors with the appropriate capacity at appropriate locations in accordance with the S1R72U16 USB 2.0 PCB Design Guide?
- Have USB transmission paths (DP/DM) been designed in accordance with the S1R72U16 USB 2.0 PCB Design Guide?
- Are the components installed on the USB transmission paths (DP/DM) USB HS components?

Q 1.69 What's the procedure for confirming whether the ATA register is accessed correctly when checking connections between the Main CPU and U16?

Keyword：ATA, Register, Access, Default

Read the following default values to check access to the ATA register.

	In ATA mode	In ATAPI mode
Sector Count	01h	01h
LBA Low	01h	01h
LBA Mid	00h	14h
LBA High	00h	EBh
Device	00h	00h
Status	50h	00h

Q 1.70 How does the XCD0/XCD1 function when "PORT14 (ComplianceErr1) Unsupported Device" is detected? How does the XCD0/XCD1 function when "PORT15 (ComplianceErr2) Too Many Devices" is detected? How does the XCD0/XCD1 function when "PORT16 (ComplianceErr3) Too Many Hubs" is detected?

Keyword：NSF, Pin, XCD

There are no changes in any of these cases.

Q 1.71 How many devices can be connected before "PORT15 (ComplianceErr2) Too Many Devices" is detected?

Keyword：NSF, Pin, XCD

Detected when connected to the third or subsequent device, regardless of mode settings.

Q 1.72 It is not possible to access a USB storage device.

Keyword：Fault, Access, USB device, USB storage

The S1R72U16 complies with USB standards, but certain USB storage devices do not comply fully with USB standards.

The following USB storage devices cannot be connected.

- Devices that continuously return NAK
- Devices that return an illegal CSW

Q 1.73 Is the VBUS supply stopped (VBUS_EN = OFF) when the Sleep command is issued?

Keyword：Sleep, Suspend, VBUS

This depends on whether a USB storage device is connected.

- If the device is connected:
  VBUS supply is not stopped and only suspended.
- If the device is not connected:
  VBUS supply is stopped.

Q 1.74 The sample source does not operate with the S1R72U16xxxE200 when used unmodified.

Keyword：Sample source, E100, E200

When using the S1R72U16xxxE200, delete the include statement in U16_Update.h defined in U16_SampleDriverII U16_Command.c.

The sample source describes downloading UpdateData.

Q 1.75 How can I detect insertion/removal of media such as card readers, CDs, or DVDs?

Keyword：Card reader, Media detection

Use GET MEDIA STATUS (in ATA mode), TEST UNIT READY (in ATAPI mode), or media access (read/write) command errors. Notification of media changes is issued only once after media insertion.

The detection methods in ATA mode are shown below. For details, refer to the ATA/ATAPI-6 standard.

- Detection of media removal → insertion
  Detected when error register MC (Media Change) bit (bit 5) becomes 1.
- Detection of media insertion → removal
  Detected when error register NM (No Media) bit (bit 1) becomes 1.
  The detection methods in ATAPI mode are as shown below. For details, refer to the MMC-5 standard.
- Detection of media removal → insertion
  Detected when error data (obtained via REQUEST SENSE command) becomes SenseKey = 06h and ASC = 28h.
- Detection of media insertion → removal
  Detected when error data (obtained via REQUEST SENSE command) becomes SenseKey = 02h and ASC = 3Ah.

The status is confirmed as shown below.

In ATA mode:

(1) Issue GET MEDIA STATUS command periodically.

1. If ended normally: Media insertion status
2. If ended with error

Error register NM bit (bit 1) = 1: No media

Error register MC bit (bit 5) = 1: Media change

(2) Issue a media access (read/write) command and check the error register value.

The error register details are the same as for (1) GET MEDIA STATUS command.

In ATAPI mode:

(1) Issue TEST UNIT READY command periodically.

1. If ended normally: Media insertion status
2. If ended with error: Check using error data (obtained via REQUEST SENSE command).

For details, refer to “10.2.5.2 ATAPI Mode Checking Method” in the S1R72U16 Application Note.

(2) Issue a media access (read/write) command and check using the error data (obtained via REQUEST SENSE command).

The error data details are the same as for (1) TEST UNIT READY command.

Q 1.76 What methods support USB storage device connection and disconnection?

Keyword：Mount/unmount, Application, File system, Connection/disconnection

This requires a file system that supports removable drives (e.g. mount/unmount architecture). Connection and disconnection are generally handled using mount/unmount processing.

2. Clock

Q 2.1 What clock frequency should be input?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.

Set the CLKSEL pin based on the clock used.

Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

There are no differences in performance, current consumption, and any other requirements due to frequency with either 12 MHz or 24 MHz selected.

Q 2.2 What is the CLKSEL pin used for?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.

Set the CLKSEL pin based on the clock used.

Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

Q 2.3 What level of accuracy is required for the clock frequency input?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Accuracy, Deviation, USB standard

A crystal oscillator accurate to within ± 100 ppm is recommended.

The USB 2.0 High Speed standard defines the frequency accuracy as ± 500 ppm. The frequency accuracy described above is recommended to ensure signal quality at the product level, since the USB signal waveform is greatly affected by clock jitter and frequency accuracy.

Q 2.4 The crystal oscillator does not oscillate even after the power supply is turned on.

Keyword：Crystal, Oscillator, Resonator, Oscillation

Check the following:

- Are the power supplies providing the specified voltage?
- Has a reset (XRESET) been asserted?
- Does the crystal oscillator circuit have the correct circuit constants?

Q 2.5 PLL_Locked is not asserted even after the power supply is turned on.

Keyword：Crystal, Oscillator, Resonator, Oscillation, PLL

Check the following:

- Is the crystal oscillator oscillating?
- Are the power supplies providing the specified voltage?
- Has a reset (XRESET) been asserted?
- Does the crystal oscillator circuit have the correct circuit constants?

Q 2.6 Please explain the crystal oscillator and crystal oscillator circuit.

Keyword：Crystal, Oscillator, Resonator, Oscillator circuit

Refer to the S1R72U16 USB 2.0 PCB Design Guide.
This document gives the recommended crystal devices and circuit constants.

Q 2.7 The system includes a 12 MHz (24 MHz) clock. Is it possible to connect the clock input directly without using a crystal oscillator?

Keyword：Clock, Crystal, Oscillator, Resonator

We recommend using a crystal oscillator to ensure satisfactory USB signal quality. Note the following points if connecting the clock input directly (in which case the user is responsible for determining suitability).

- Connect the clock input to the XI pin.
- The input level is 1.8 V.
- The clock accuracy should be within ± 100 ppm.
- Hold the XO pin open, and avoid applying a load when a mounted land is provided.

For detailed information on clock duty, refer to the AC characteristics section in the S1R72U16 Data Sheet.
No restrictions apply to rise/fall time and jitter. The need for clock input should be determined based on the precautions above.

3. Power supply

Q 3.1 What voltage is required for the power supply? Do any restrictions apply to the power on/off sequence?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

The USB requires HVDD (3.3 V), the LSI internal circuits require LVDD (1.8 V), and the system interface require IOVDD (1.8 to 3.3 V).

The LSI requires the above three power supplies, but the system can be configured using two power supplies by combining the IOVDD with another power supply, as shown below.

- If the system interface voltage is 3.3 V, the IOVDD can use the same power supply as the HVDD.
- If the system interface voltage is 1.8 V, the IOVDD can use the same power supply as the LVDD.

To ensure LSI reliability, we recommend turning the HVDD and IOVDD on or off with the LVDD provided, as described in the S1R72U16 Data Sheet. However, the HVDD or IOVDD may be turned on with the LVDD turned off, provided this is done for no more than 1 second.

This means that the IOVDD and LVDD may share the same power supply and that the HVDD may be used to regulate the LVDD, provided this interval is within the 1 second interval described above.

The power on/off timing is as shown below.

(→ Power on/off timing)

Q 3.2 What voltage should be used for the IOVDD in IDE mode?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

The IOVDD should be 3.3 V when in IDE mode.

Q 3.3 What is the exact state when power is turned off?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

This refers to the state in which no current is drawn by the LSI power supply, and the LSI is grounded.

Even if a potential difference persists due to a charged load, the power supply is deemed to be turned off if it is shut off from the exterior.

Q 3.4 Are the pins Hi-z when the LSI power supply is turned off?

Keyword：Power supply, Pin, Power off, Shutoff, Hi-z

The pins do not switch to Hi-z when the LSI power supply is turned off.

A current path is formed to the LSI power supply via protective components and output transistors.

This means the following scenarios are possible if the main CPU power supply is on while LSI power supply is turned off.

- The main CPU cannot drive the bus to High.
- Main CPU current consumption increases.
- The LSI is powered by a rerouted power supply from the bus.

Q 3.5 What is the maximum current consumption?

Keyword：Current consumption, Maximum

The maximum current consumption will depend on usage (i.e., user's board design and bus load), so no specific figure can be given.

The power supply should generally be selected to provide approximately 1.5 times the typical value appropriate for the customer's board.

Current consumption varies with temperature, power supply voltage, and individual LSIs, but maximum current consumption should generally not exceed 1.5 times the typical value.

The data sheet only stipulates typical values for maximum operational load using the Seiko Epson evaluation setup.

Q 3.6 What is power consumption?

Keyword：Power consumption

Refer to the S1R72U16 Data Sheet.

The power consumption value can be obtained by calculating power supply voltage x power supply current.

4. Non-USB/IDE pin function

Q 4.1 What is the CLKSEL pin used for?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.
Set the CLKSEL pin based on the clock used.
Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

Q 4.2 What are the TEST pins used for? How should they be connected?

Keyword：TEST, Pin, Connection, Setting

These pins are not normally used by the user.

For detailed information on individual pin connection and setting, refer to "Pin Function Description" in the S1R72U16 Data Sheet.

Q 4.3 What are the DEBUG I/F pins used for? How should they be connected?

Keyword：DEBUG, Pin, Connection, Setting

These pins are not normally used by the user.

For detailed information on individual pin connection and setting, refer to "Pin Function Description" in the S1R72U16 Data Sheet.

Q 4.4 What are the Serial I/F pins used for? How should they be connected?

Keyword：Serial, Pin, Connection, Setting

These pins are used for simple debugging by the user during product (system) development by verifying connections to the main CPU and displaying the LSI processing history on a PC.
They are also used to launch authentication software for USB compliance testing.

For detailed information, refer to the S1R72U16 Development Support Manual and S1R72U16 Embedded Host Compliance Guide.
For detailed information on connection and setting, refer to the S1R72U16 Evaluation Board Manual.

Q 4.5 What are the GPI pins used for? How should they be connected?

Keyword：GPI, Pin, Connection, Setting

These pins are used to set the S1R72U16 operating mode.

For detailed information, refer to “Mode Settings” in the S1R72U16 Technical Manual.

Q 4.6 What are the GPO pins used for? How should they be connected?

Keyword：GPO, Pin, Connection, Setting

These pins are used for the following three main purposes:

- Indicating connection/disconnection and monitoring status to treat USB storage devices as removable devices
- Monitoring the start of PLL oscillation to confirm the LSI start-up state
- Indicating errors for USB compliance testing

For detailed information, refer to the S1R72U16 Technical Manual.

For detailed information on connection and setting, refer to the S1R72U16 Evaluation Board Manual.

Q 4.7 What precautions are necessary with resets?

Keyword：Reset

The precautions are the same as for regular resets.

The LSI status will not be established unless a reset is input. It should be reset when power is turned on and the reset canceled after the power supply has been established. (Power-on reset)

The reset input when turning on power should be a signal with a pulse width that satisfies the AC timing described in the S1R72U16 Data Sheet.

Note that a reset is not triggered accidentally by noise, etc. when the LSI is operating.

Q 4.8 How should the CSEL_T and 2x1 pins be set?

Keyword：Mode, Pin settings

For individual pin functions, refer to S1R72U16 Data Sheet.

1. When an IDE device and the S1R72U16 are connected to a host on the IDE bus in IDE mode, set the 2x1 pin to single-device mode (“0”) and CSEL_T pin to master (“0”) or slave (“1”) as required.

2. When connecting the S1R72U16 only on the IDE bus in IDE mode, set the 2x1 pin to 2-device mode (“1”) and CSEL_T pin to master (“0”). You can also use this setting either when only one USB device is connected downstream of the S1R72U16 or when two USB devices are connected using a hub downstream of the S1R72U16.

3. When connecting in CPU mode, the settings are the same as for 2.

Q 4.9 How does the XCD0/XCD1 function when “PORT14 (ComplianceErr1) Unsupported Device” is detected? How does the XCD0/XCD1 function when “PORT15 (ComplianceErr2) Too Many Devices” is detected? How does the XCD0/XCD1 function when “PORT16 (ComplianceErr3) Too Many Hubs” is detected?

Keyword：NSF, Pin, XCD

There are no changes in any of these cases.

Q 4.10 How many devices can be connected before “PORT15 (ComplianceErr2) Too Many Devices” is detected?

Keyword：NSF, Pin, XCD

Detected when connected to the third or subsequent device, regardless of mode settings.

5. Board design

Q 5.1 What clock frequency should be input?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.

Set the CLKSEL pin based on the clock used.

Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

There are no differences in performance, current consumption, and any other requirements due to frequency with either 12 MHz or 24 MHz selected.

Q 5.2 What is the CLKSEL pin used for?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Clock selection, CLKSEL

This LSI supports 12 MHz and 24 MHz crystal oscillators.

Set the CLKSEL pin based on the clock used.

Set the CLKSEL pin to Low for 12 MHz and to High for 24 MHz.

Note that the LSI will not operate correctly if the CLKSEL pin setting differs from the actual clock frequency input.

Q 5.3 What level of accuracy is required for the clock frequency input?

Keyword：Crystal, Oscillator, Resonator, Clock, Frequency, Accuracy, Deviation, USB standard

A crystal oscillator accurate to within ± 100 ppm is recommended.

The USB 2.0 High Speed standard defines the frequency accuracy as ± 500 ppm. The frequency accuracy described above is recommended to ensure signal quality at the product level, since the USB signal waveform is greatly affected by clock jitter and frequency accuracy.

Q 5.4 What voltage is required for the power supply? Do any restrictions apply to the power on/off sequence?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

The USB requires HVDD (3.3 V), the LSI internal circuits require LVDD (1.8 V), and the system interface require IOVDD (1.8 to 3.3 V).

The LSI requires the above three power supplies, but the system can be configured using two power supplies by combining the IOVDD with another power supply, as shown below.

- If the system interface voltage is 3.3 V, the IOVDD can use the same power supply as the HVDD.
- If the system interface voltage is 1.8 V, the IOVDD can use the same power supply as the LVDD.

To ensure LSI reliability, we recommend turning the HVDD and IOVDD on or off with the LVDD provided, as described in the S1R72U16 Data Sheet. However, the HVDD or IOVDD may be turned on with the LVDD turned off, provided this is done for no more than 1 second.

This means that the IOVDD and LVDD may share the same power supply and that the HVDD may be used to regulate the LVDD, provided this interval is within the 1 second interval described above.

The power on/off timing is as shown below.

(→ Power on/off timing)

Q 5.5 What voltage should be used for the IOVDD in IDE mode?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

The IOVDD should be 3.3 V when in IDE mode.

Q 5.6 What is the exact state when power is turned off?

Keyword : Power supply, Power on, Power off, Shutoff, Sequence, Interface

This refers to the state in which no current is drawn by the LSI power supply, and the LSI is grounded.

Even if a potential difference persists due to a charged load, the power supply is deemed to be turned off if it is shut off from the exterior.

Q 5.7 Do you recommend any USB peripheral circuit pattern guides?

Keyword : USB, Peripheral circuit, Pattern

See the S1R72U16 USB 2.0 PCB Design Guide.

Q 5.8 Do you recommend any USB peripheral circuit protective components?

Keyword : USB, Peripheral circuit, Noise, Surge, EMI, Protective components, Components

See the S1R72U16 USB 2.0 PCB Design Guide.

Q 5.9 Are the pins Hi-z when the LSI power supply is turned off?

Keyword：Power supply, Pin, Power off, Shutoff, Hi-z

The pins do not switch to Hi-z when the LSI power supply is turned off.
A current path is formed to the LSI power supply via protective components and output transistors.

This means the following scenarios are possible if the main CPU power supply is on while LSI power supply is turned off.

- The main CPU cannot drive the bus to High.
- Main CPU current consumption increases.
- The LSI is powered by a rerouted power supply from the bus.

Q 5.10 What are the TEST pins used for? How should they be connected?

Keyword：TEST, Pin, Connection, Setting

These pins are not normally used by the user.

For detailed information on individual pin connection and setting, refer to "Pin Function Description" in the S1R72U16 Data Sheet.

Q 5.11 What are the DEBUG I/F pins used for? How should they be connected?

Keyword：DEBUG, Pin, Connection, Setting

These pins are not normally used by the user.

For detailed information on individual pin connection and setting, refer to "Pin Function Description" in the S1R72U16 Data Sheet.

Q 5.12 What are the Serial I/F pins used for? How should they be connected?

Keyword：Serial, Pin, Connection, Setting

These pins are used for simple debugging by the user during product (system) development by verifying connections to the main CPU and displaying the LSI processing history on a PC.
They are also used to launch authentication software for USB compliance testing.

For detailed information, refer to the S1R72U16 Development Support Manual and S1R72U16 Embedded Host Compliance Guide.
For detailed information on connection and setting, refer to the S1R72U16 Evaluation Board Manual.

Q 5.13 What are the GPI pins used for? How should they be connected?

Keyword：GPI, Pin, Connection, Setting

These pins are used to set the S1R72U16 operating mode.

For detailed information, refer to “Mode Settings” in the S1R72U16 Technical Manual.

Q 5.14 What are the GPO pins used for? How should they be connected?

Keyword：GPO, Pin, Connection, Setting

These pins are used for the following three main purposes:

- Indicating connection/disconnection and monitoring status to treat USB storage devices as removable devices
- Monitoring the start of PLL oscillation to confirm the LSI start-up state
- Indicating errors for USB compliance testing

For detailed information, refer to the S1R72U16 Technical Manual.

For detailed information on connection and setting, refer to the S1R72U16 Evaluation Board Manual.

Q 5.15 Please explain the crystal oscillator and crystal oscillator circuit.

Keyword：Crystal, Oscillator, Resonator, Oscillator circuit

Refer to the S1R72U16 USB 2.0 PCB Design Guide.
This document gives the recommended crystal devices and circuit constants.

Q 5.16 What precautions are necessary with resets?

Keyword：Reset

The precautions are the same as for regular resets.

The LSI status will not be established unless a reset is input. It should be reset when power is turned on and the reset canceled after the power supply has been established. (Power-on reset)
The reset input when turning on power should be a signal with a pulse width that satisfies the AC timing described in the S1R72U16 Data Sheet.
Note that a reset is not triggered accidentally by noise, etc. when the LSI is operating.

Q 5.17 Please explain the specifics of the USB power switch IC. Can this be formed using a discrete component without using the dedicated IC?

Keyword：USB, VBUS, Power switch, High side switch

For more information on USB power switches, refer to the S1R72U16 USB 2.0 PCB Design Guide.

Functions can be achieved using discrete components, but no application examples are provided. The user is responsible for determining the configuration.

Q 5.18 This is the first time we've attempted to design a USB board. Are there any reference materials?

Keyword：USB, Board, PCB

Refer to the S1R72U16 USB 2.0 PCB Design Guide.

Q 5.19 The system includes a 12 MHz (24 MHz) clock. Is it possible to connect the clock input directly without using a crystal oscillator?

Keyword：Clock, Crystal, Oscillator, Resonator

We recommend using a crystal oscillator to ensure satisfactory USB signal quality. Note the following points if connecting the clock input directly (in which case the user is responsible for determining suitability).

- Connect the clock input to the XI pin.
- The input level is 1.8 V.
- The clock accuracy should be within ± 100 ppm.
- Hold the XO pin open, and avoid applying a load when a mounted land is provided.

For detailed information on clock duty, refer to the AC characteristics section in the S1R72U16 Data Sheet.

No restrictions apply to rise/fall time and jitter. The need for clock input should be determined based on the precautions above.

Q 5.20 What is the purpose of the common mode choke coil included in the DP/DM? Is it intended to prevent DP/DM degradation due to external noise?

Keyword：Common mode, Choke coil, Board, Prevention, Noise

The common mode choke coil is intended to minimize common mode noise. It does not directly prevent DP/DM degradation.

Note that common mode noise occurs when a current (common mode current) flows in the same direction in the differential signal line.

Q 5.21 What is the maximum current consumption?

Keyword：Current consumption, Maximum

The maximum current consumption will depend on usage (i.e., user's board design and bus load), so no specific figure can be given.

The power supply should generally be selected to provide approximately 1.5 times the typical value appropriate for the customer's board.

Current consumption varies with temperature, power supply voltage, and individual LSIs, but maximum current consumption should generally not exceed 1.5 times the typical value.

The data sheet only stipulates typical values for maximum operational load using the Seiko Epson evaluation setup.

Q 5.22 What is power consumption?

Keyword：Power consumption

Refer to the S1R72U16 Data Sheet.

The power consumption value can be obtained by calculating power supply voltage x power supply current.

Q 5.23 What is the margin for AC characteristics CPUIF timing (e.g. address, data setup/hold)?

Keyword：AC characteristics, Timing, Margin

This normally complies with ATA/ATAPI standards, since circuits are shared in CPU and IDE modes.

Comply with AC characteristics.

Q 5.24 Are there any reference materials for board design?

Keyword：PCB, Board design, Design guide

For detailed information on package and pin functions, refer to S1R72U16 Data Sheet.

For detailed information on USB peripheral circuit design, refer to the S1R72U16 USB 2.0 PCB Design Guide.

For detailed information on other overall board design and recommended circuits, refer to the S1R72U16 Evaluation Board Manual.

This FAQ (Board design) also provides details on setting and other processing of unused pins.

Q 5.25 Please explain noise countermeasures and static electricity protection products.

Keyword：Noise, Static electricity

The main noise countermeasure is a common mode coil provided in the DP/DM line, which suppresses current flowing in the same direction in the differential signal line. This improves DP/DM signal phase offset and voltage differences and prevents common mode noise.

Common mode impedance should ideally be 90 Ω with a small DC resistance component.

Protection against static electricity is generally provided by including a chip varistor in the DP/DM line. As a general rule, this should be less than 10 pF for USB HS, since high static capacitance may affect USB signal wave quality.

The varistor voltage must be higher than the USB amplitude maximum voltage of 3.6 V.

In either case, the product's ability to support USB 2.0 should also be a factor when considering component selection.

Q 5.26 How should unused pins be handled?

Keyword：Unused, Pin treatment

Refer to the table below.

(→ Unused pin treatment)

Q 5.27 Do any particular precautions apply for USB board design?

Keyword：USB, Board, PCB

Refer to S1R72U16 USB 2.0 PCB Design Guide.

Check the following points when seeking to improve analog waveforms.

- Is the power supply noise-free?
- Have you installed decoupling capacitors with the appropriate capacity at appropriate locations in accordance with the S1R72U16 USB 2.0 PCB Design Guide?
- Have USB transmission paths (DP/DM) been designed in accordance with the S1R72U16 USB 2.0 PCB Design Guide?
- Are the components installed on the USB transmission paths (DP/DM) USB HS components?

6. IDE

Q 6.1 What voltage should be used for the IOVDD in IDE mode?

Keyword：Power supply, Power on, Power off, Shutoff, Sequence, Interface

The IOVDD should be 3.3 V when in IDE mode.

Q 6.2 Are the IDE I/F pins 5 V tolerant?

Keyword：IDE, 5 V

No. This LSI is intended for 3.3 V interfaces.

Q 6.3 How do I obtain the IDE driver?

Keyword：IDE, ATA/ATAPI, Driver

Please contact the retailer from whom you purchased the file system.

Seiko Epson provides sample code with settings for CPU bus connections. The code can be downloaded on web site.

Q 6.4 Can the LSI be used without an IDE host?

Keyword：IDE, ATA/ATAPI, CPU, Bus

Yes, by connecting to the CPU memory bus. For detailed information on bus connections, refer to the S1R72U16 Evaluation Board Manual. For detailed information on control methods, refer to the S1R72U16 Application Note.

The protocol complies with ATA/ATAPI, allowing control using an IDE driver.

Seiko Epson provides sample code for CPU bus connection. The code can be downloaded on web site.

Q 6.5 An HDD is connected to the Main CPU as IDE master. Can this LSI be connected to the Main CPU as IDE slave?

Keyword：ATA, IDE, Master, Slave, HDD, Connection

Yes. For detailed information, refer to “System Configuration Examples” in the S1R72U16 Application Note.

Q 6.6 Is the driver source code endian-dependent?

Keyword：Sample, Driver, Endian, Source, Code

Yes. It assumes little-endian.

Q 6.7 Does the S1R72U16 ever negate DMARQ before the specified transfer has been completed? If so, when does this occur?

Keyword：IDE, DMARQ, DMA transfer, Terminate

DMARQ is negated in either of the following conditions.

1. If the IDE host performs a host terminate

2. If the IDE host exceeds 8 Mbytes (800000h) in the Read direction (LSI to Main CPU)

DMARQ is negated for each 8 Mbyte transfer if a data transfer is requested.

Ex: If the Main CPU issues a READ command for 24 Mbytes, the LSI divides the 24 Mbytes of data into three.

DMARQ is therefore negated twice during UltraDMA transfer.

For conditions other than those described above, the DMARQ signal is not negated before the specified transfer is completed.

In the case of WRITE, only condition 1 above applies for negating the DMARQ signal, since the LSI usage restrictions limit the maximum size of data that can be requested to 8 Mbytes.

Q 6.8 Does the S1R72U16 ever negate DMARQ if the USB bus is defective, resulting in repeated packet errors?

Keyword：IDE, DMARQ, DMA transfer, Packet error, Transfer error

DMARQ is not negated even if packet errors occur during DMARQ assertion.

DMARQ will be treated as follows depending on the timing of the NAK returned continuously by the READ command.

1. If NAK is returned continuously for CBW command issue

DMARQ is not asserted and the LSI does not start UltraDMA transfer.

The status register will be BSY=1 and DRQ=0.

2. If NAK is returned continuously for the first BulkIN transfer after CBW issue

Same as for 1.

3. If NAK is returned continuously after ACK has been returned at least once for first BulkIN transfer

DMARQ is asserted and UltraDMA transfer is not completed.

The status register will be BSY=0 and DRQ=1.

4. If NAK is returned repeatedly for the CSW (status) issued

The UltraDMA transfer will end, but the Status register will show BSY=1, DRQ=0.

The same applies for the WRITE command also.

Q 6.9 Can the LSI be used connected to a PC IDE port?

Keyword：PC, IDE

This LSI uses a 3.3 V I/F. It can be connected provided the PC I/F voltage is 3.3 V. Note that most desktop PCs have a 5 V I/F; check the voltage before connecting the LSI.

Use the following settings when connecting to a PC.

- IDE mode: CPUxIDE pin = “0”
- ATAPI mode: ATAxATAPI pin = “0”
- Single device mode: 2x1 pin = “0”

Also, set CSEL_T pin according to whether the device is used as Master (CSEL_T pin = “0”) or as Slave (CSEL_T pin = “1”).

Q 6.10 What methods support USB storage device connection and disconnection?

Keyword：Mount/unmount, Application, File system, Connection/disconnection

This requires a file system that supports removable drives (e.g. mount/unmount architecture). Connection and disconnection are generally handled using mount/unmount processing.

7. USB

Q 7.1 Do you recommend any USB peripheral circuit pattern guides?

Keyword：USB, Peripheral circuit, Pattern

See the S1R72U16 USB 2.0 PCB Design Guide.

Q 7.2 Do you recommend any USB peripheral circuit protective components?

Keyword：USB, Peripheral circuit, Noise, Surge, EMI, Protective components, Components

See the S1R72U16 USB 2.0 PCB Design Guide.

Q 7.3 Please explain USB 2.0 logo certification (compliance testing).

Keyword：USB, Logo, Certification, Compliance, Embedded Host

Refer to the S1R72U16 Embedded Host Compliance Guide.

Q 7.4 Please explain the specifics of the USB power switch IC. Can this be formed using a discrete component without using the dedicated IC?

Keyword：USB, VBUS, Power switch, High side switch

For more information on USB power switches, refer to the S1R72U16 USB 2.0 PCB Design Guide.

Functions can be achieved using discrete components, but no application examples are provided. The user is responsible for determining the configuration.

Q 7.5 Can I use an FS USB hub?

Keyword：USB, Hub, FS

Yes. However, note that transfers to and from USB storage devices connected to an FS hub will be FS, even if the device is HS.

Q 7.6 This is the first time we've attempted to design a USB board. Are there any reference materials?

Keyword：USB, Board, PCB

Refer to the S1R72U16 USB 2.0 PCB Design Guide.

Q 7.7 What kinds of USB devices can I connect? Can I connect USB memory and USB mouse devices?

Keyword：USB, Device, Memory, Mouse, HDD, Storage

Storage devices such as USB memory and hubs can be connected, but not USB mouse devices.

For detailed information, refer to the S1R72U16 Technical Manual.

Q 7.8 What does the term “storage device” refer to?

Keyword：USB, Storage memory, HDD, CD, DVD

This is the general term applied to USB storage devices, including USB memory, USB-HDD, USB-CD, and USB-DVD devices.

Q 7.9 Is there a limit to the capacity of USB storage devices that can be connected?

Keyword：Storage, Capacity, Drive

Less than 2 Tbytes for E100; up to 2 Tbytes for E200.

This means USB storage devices of 137 GB or larger can be used as Big Drive devices.

Q 7.10 How should TPL data be prepared?

Keyword：USB, Logo, Certification, Compliance, Embedded host, TPL

A TPL generation tool can be downloaded on web site.

Q 7.11 Does USB support hot plugs?

Keyword：Hot plug

Yes.

Q 7.12 Is there a limit on the number of USB devices that can be connected?

Keyword：Constraint, Restriction, Device number, Connection

Up to two (master/slave) USB storage devices can be connected via the USB hub. Additional connected devices will be ignored by this LSI. Up to three HUBs can be connected. This LSI ignores additional connected HUBs.

Q 7.13 Can USB floppy disk drives be used?

Keyword：Mass storage class, MSC, Restriction, Constraint, Floppy, Storage

No. The LSI does not support floppy disk drives (UFI subclass devices).

Q 7.14 Does the S1R72U16 ever negate DMARQ if the USB bus is defective, resulting in repeated packet errors?

Keyword：IDE, DMARQ, DMA transfer, Packet error, Transfer error

DMARQ is not negated even if packet errors occur during DMARQ assertion.

DMARQ will be treated as follows depending on the timing of the NAK returned continuously by the READ command.

1. If NAK is returned continuously for CBW command issue

DMARQ is not asserted and the LSI does not start UltraDMA transfer.

The status register will be BSY=1 and DRQ=0.

2. If NAK is returned continuously for the first BulkIN transfer after CBW issue

Same as for 1.

3. If NAK is returned continuously after ACK has been returned at least once for first BulkIN transfer

DMARQ is asserted and UltraDMA transfer is not completed.

The status register will be BSY=0 and DRQ=1.

4. If NAK is returned repeatedly for the CSW (status) issued

The UltraDMA transfer will end, but the Status register will show BSY=1, DRQ=0.

The same applies for the WRITE command also.

Q 7.15 Are any specific procedures required to use the S1R72U16 and install the USB Host functions in a product? Can certification be requested at any time?

Keyword：USB, Certification, Compliance

No special procedures are required to create products that simply involve connecting devices such as USB memory. You must obtain USB certification to use the familiar USB logo with specific products. For information on obtaining USB certification, see the S1R72U16 Embedded Host Compliance Guide.

Certification can be requested at any time. Refer to the certification body for details.

Q 7.16 Can the main CPU obtain the Vendor ID and Product ID of USB devices connected to the S1R72U16? If not, is there a way to obtain identifying information about USB devices?

Keyword：USB, Device, ID, Identifying information

The CPU cannot obtain the Vendor ID or Product ID of USB devices.

However, identifying information about connected USB devices can be obtained using the IDENTIFY DEVICE, IDENTIFY PACKET DEVICE, and INQUIRY commands if the information exists in the command parameters. For details of the identifying information that can be obtained, see the section on specifications for information returned for each command in the S1R72U16 Technical Manual.

Q 7.17 Is there a way to restrict connections to specific USB devices?

Keyword：USB, Device, TPL, Restriction, Specific

Yes. This LSI includes a function that restricts the devices that can be connected by determining USB device information.

See the TPL section in the S1R72U16 Technical Manual or the section on downloading in S1R72U16 Application Note.

Q 7.18 What is the purpose of the common mode choke coil included in the DP/DM? Is it intended to prevent DP/DM degradation due to external noise?

Keyword：Common mode, Choke coil, Board, Prevention, Noise

The common mode choke coil is intended to minimize common mode noise. It does not directly prevent DP/DM degradation.

Note that common mode noise occurs when a current (common mode current) flows in the same direction in the differential signal line.

Q 7.19 Is it possible to connect an HS USB device as an FS device?

Keyword：Hub, HS, FS, Device

The LSI does not provide this function.

It is possible to connect the device as an FS device via an FS hub, as shown below.

72U16 ⇔ FS hub ⇔ HS device

Q 7.20 Please explain noise countermeasures and static electricity protection products.

Keyword：Noise, Static electricity

The main noise countermeasure is a common mode coil provided in the DP/DM line, which suppresses current flowing in the same direction in the differential signal line. This improves DP/DM signal phase offset and voltage differences and prevents common mode noise.

Common mode impedance should ideally be 90 Ω with a small DC resistance component.

Protection against static electricity is generally provided by including a chip varistor in the DP/DM line. As a general rule, this should be less than 10 pF for USB HS, since high static capacitance may affect USB signal wave quality.

The varistor voltage must be higher than the USB amplitude maximum voltage of 3.6 V.

In either case, the product's ability to support USB 2.0 should also be a factor when considering component selection.

Q 7.21 Do any particular precautions apply for USB board design?

Keyword：USB, Board, PCB

Refer to S1R72U16 USB 2.0 PCB Design Guide.

Check the following points when seeking to improve analog waveforms.

- Is the power supply noise-free?
- Have you installed decoupling capacitors with the appropriate capacity at appropriate locations in accordance with the S1R72U16 USB 2.0 PCB Design Guide?
- Have USB transmission paths (DP/DM) been designed in accordance with the S1R72U16 USB 2.0 PCB Design Guide?
- Are the components installed on the USB transmission paths (DP/DM) USB HS components?

Q 7.22 Is the VBUS supply stopped (VBUS_EN = OFF) when the Sleep command is issued?

Keyword：Sleep, Suspend, VBUS

This depends on whether a USB storage device is connected.

- If the device is connected:
  VBUS supply is not stopped and only suspended.
- If the device is not connected:
  VBUS supply is stopped.

8. System configuration

Q 8.1 Is an evaluation board available?

Keyword：Evaluation, Board, Circuit board, Bridge

Yes. An evaluation board is available for the IDE device - USB bridge. The S1R72U16 Evaluation Board Manual is also provided with the board. Please contact Seiko Epson Sales to obtain this evaluation board.

Q 8.2 What are the actual transfer rates?

Keyword：Transfer rate

Transfer rates of up to 31 MB/s (248 Mbps) have been confirmed in tests done by Seiko Epson.

<Test conditions>
IDE host: PC IDE port
Benchmark software: HDBENCH

Since transfer rates depend on the IDE host (PC) and USB storage device used, these values cannot be guaranteed for the user's specific configuration.

Q 8.3 Are the IDE I/F pins 5 V tolerant?

Keyword：IDE, 5 V

No. This LSI is intended for 3.3 V interfaces.

Q 8.4 Can I use an FS USB hub?

Keyword：USB, Hub, FS

Yes. However, note that transfers to and from USB storage devices connected to an FS hub will be FS, even if the device is HS.

Q 8.5 What kinds of USB devices can I connect? Can I connect USB memory and USB mouse devices?

Keyword：USB, Device, Memory, Mouse, HDD, Storage

Storage devices such as USB memory and hubs can be connected, but not USB mouse devices.
For detailed information, refer to the S1R72U16 Technical Manual.

Q 8.6 Can the LSI be used without an IDE host?

Keyword：IDE, ATA/ATAPI, CPU, Bus

Yes, by connecting to the CPU memory bus. For detailed information on bus connections, refer to the S1R72U16 Evaluation Board Manual. For detailed information on control methods, refer to the S1R72U16 Application Note.

The protocol complies with ATA/ATAPI, allowing control using an IDE driver.

Seiko Epson provides sample code for CPU bus connection. The code can be downloaded on web site.

Q 8.7 How should the CPU bus be connected?

Keyword：CPU bus

Connect to the CPU memory bus. For detailed information on bus connections, refer to the S1R72U16 Evaluation Board Manual. For detailed information on control methods, refer to the S1R72U16 Application Note.

The protocol complies with ATA/ATAPI, allowing control using an IDE driver.

Seiko Epson provides sample code for CPU bus connection. The code can be downloaded on web site.

Q 8.8 Please explain the DMA details for CPU bus connections.

Keyword：CPU, Bus, DMA

This is basically the same as for IDE Multi Word DMA. Transfer uses request and acknowledge handshakes. Both request and acknowledge are negative logic signals.

Precautions for using DMA are given below. CPUs contain a wide range of DMAC. The user should determine whether DMA transfer is possible and whether external logic is present. If DMA cannot be used, transfer data using PIO.

- Connections are normally not possible to CPUs featuring DMAC with no acknowledge or with edge triggers.
- External logic is required when connecting to CPUs featuring DMAC asserted by CS during DMA.

Q 8.9 An HDD is connected to the Main CPU as IDE master. Can this LSI be connected to the Main CPU as IDE slave?

Keyword：ATA, IDE, Master, Slave, HDD, Connection

Yes. For detailed information, refer to “System Configuration Examples” in the S1R72U16 Application Note.

Q 8.10 Is there a limit to the capacity of USB storage devices that can be connected?

Keyword：Storage, Capacity, Drive

Less than 2 Tbytes for E100; up to 2 Tbytes for E200.

This means USB storage devices of 137 GB or larger can be used as Big Drive devices.

Q 8.11 How should TPL data be prepared?

Keyword：USB, Logo, Certification, Compliance, Embedded host, TPL

A TPL generation tool can be downloaded on web site.

Q 8.12 Does USB support hot plugs?

Keyword：Hot plug

Yes.

Q 8.13 Is there a limit on the number of USB devices that can be connected?

Keyword：Constraint, Restriction, Device number, Connection

Up to two (master/slave) USB storage devices can be connected via the USB hub. Additional connected devices will be ignored by this LSI. Up to three HUBs can be connected. This LSI ignores additional connected HUBs.

Q 8.14 What constraints or precautions are associated with the main system file system?

Keyword：Constraint, File system

No particular constraints apply. (The LSI will return an error if a write/read attempt is made while the USB device is disconnected.)

Q 8.15 Can USB floppy disk drives be used?

Keyword：Mass storage class, MSC, Restriction, Constraint, Floppy, Storage

No. The LSI does not support floppy disk drives (UFI subclass devices).

Q 8.16 Are there any figures for transfer rates for CPU bus connections?

Keyword：Transfer rate, Transfer speed, CPU bus, Memory bus

No figures area available for transfer rates. Actual transfer rates will depend on the user's system configuration, including access to devices other than the LSI (e.g., ROM/RAM).

The theoretical maximum value is 16.6 Mbytes/s, as the AC specifications are the same as for the IDE bus PIO.

No measurement data is available, but the actual transfer rate should be less than half, even under ideal conditions.

Q 8.17 Are ATA/ATAPI commands used to control the S1R72U16? Which commands should be used?

Keyword：IDE, ATA, ATAPI, Command

Yes. ATA/ATAPI commands are used.

Use ATAPI commands if a CD or DVD drive is connected.

Either may be used with a USB memory or HDD connected. Select the command to suit the driver included with the file system or main CPU used.

Q 8.18 Can the LSI be used connected to a PC IDE port?

Keyword：PC, IDE

This LSI uses a 3.3 V I/F. It can be connected provided the PC I/F voltage is 3.3 V. Note that most desktop PCs have a 5 V I/F; check the voltage before connecting the LSI.

Use the following settings when connecting to a PC.

- IDE mode: CPUxIDE pin = “0”
- ATAPI mode: ATAxATAPI pin = “0”
- Single device mode: 2x1 pin = “0”

Also, set CSEL_T pin according to whether the device is used as Master (CSEL_T pin = “0”) or as Slave (CSEL_T pin = “1”).

Q 8.19 Does the S1R72U16 contain a file system?

Keyword：File system

This LSI does not include a file system. The file system must be mounted on the user's system.

Q 8.20 Are any specific procedures required to use the S1R72U16 and install the USB Host functions in a product? Can certification be requested at any time?

Keyword：USB, Certification, Compliance

No special procedures are required to create products that simply involve connecting devices such as USB memory. You must obtain USB certification to use the familiar USB logo with specific products. For information on obtaining USB certification, see the S1R72U16 Embedded Host Compliance Guide.

Certification can be requested at any time. Refer to the certification body for details.

Q 8.21 Can the main CPU obtain the Vendor ID and Product ID of USB devices connected to the S1R72U16? If not, is there a way to obtain identifying information about USB devices?

Keyword：USB, Device, ID, Identifying information

The CPU cannot obtain the Vendor ID or Product ID of USB devices.

However, identifying information about connected USB devices can be obtained using the IDENTIFY DEVICE, IDENTIFY PACKET DEVICE, and INQUIRY commands if the information exists in the command parameters. For details of the identifying information that can be obtained, see the section on specifications for information returned for each command in the S1R72U16 Technical Manual.

Q 8.22 Is there a way to restrict connections to specific USB devices?

Keyword：USB, Device, TPL, Restriction, Specific

Yes. This LSI includes a function that restricts the devices that can be connected by determining USB device information.

See the TPL section in the S1R72U16 Technical Manual or the section on downloading in S1R72U16 Application Note.

Q 8.23 Is it possible to connect an HS USB device as an FS device?

Keyword：Hub, HS, FS, Device

The LSI does not provide this function.

It is possible to connect the device as an FS device via an FS hub, as shown below.

72U16 ⇔ FS hub ⇔ HS device

Q 8.24 What is the margin for AC characteristics CPUIF timing (e.g. address, data setup/hold)?

Keyword：AC characteristics, Timing, Margin

This normally complies with ATA/ATAPI standards, since circuits are shared in CPU and IDE modes.

Comply with AC characteristics.

Q 8.25 Operation is not as expected. Is there an archive of past questions and problems?

Keyword：Past cases, Case studies

Details of past problems are available. Please check whether the problem in this case corresponds to any particular past problem.

(→ Details of past problems)

Q 8.26 How should unused pins be handled?

Keyword：Unused, Pin treatment

Refer to the table below.

(→ Unused pin treatment)

Q 8.27 How should the CSEL_T and 2x1 pins be set?

Keyword：Mode, Pin settings

For individual pin functions, refer to S1R72U16 Data Sheet.

1. When an IDE device and the S1R72U16 are connected to a host on the IDE bus in IDE mode, set the 2x1 pin to single-device mode (“0”) and CSEL_T pin to master (“0”) or slave (“1”) as required.

2. When connecting the S1R72U16 only on the IDE bus in IDE mode, set the 2x1 pin to 2-device mode (“1”) and CSEL_T pin to master (“0”). You can also use this setting either when only one USB device is connected downstream of the S1R72U16 or when two USB devices are connected using a hub downstream of the S1R72U16.

3. When connecting in CPU mode, the settings are the same as for 2.

Q 8.28 How should the XINT (interrupt request) signal be used when connecting in CPU mode?

Keyword：CPUIF, CPU bus, Memory bus, Interrupt

The XINT pin corresponds to the ATA/ATAPI standard INTRQ signal and is used to indicate Status register status changes.

For details, refer to the ATA/ATAPI standard.

Interrupts should be used with a level sense method.

Interrupts are not required to check Status register status changes when polling the ATA register. In this case, it should be set to Open.

Q 8.29 How should the XHRESET signal be used when connecting in CPU mode?

Keyword：CPUIF, CPU bus, Memory bus, Reset

XHRESET corresponds to the ATA/ATAPI standard Hardware Reset and is used to abort (bus reset) an ATA/ATAPI command when initializing or operating the IDE device. Use this signal for command timeout and other processing.

For details, refer to the ATA/ATAPI standard.

For details of hardware reset operations with the S1R72U16, refer to "2.4 Operation Specifications for Resetting" in the S1R72U16 Technical Manual. (The Hardware reset will not clear data downloaded with the DOWNLOAD MICROCODE command.)

The signal assert time will be at least 25 μs (ATA/ATAPI standard value).

Pull up if no bus reset is used.

Note that the function differs from the chip reset XRESET pin.

Q 8.30 How does the XCD0/XCD1 function when "PORT14 (ComplianceErr1) Unsupported Device" is detected? How does the XCD0/XCD1 function when "PORT15 (ComplianceErr2) Too Many Devices" is detected? How does the XCD0/XCD1 function when "PORT16 (ComplianceErr3) Too Many Hubs" is detected?

Keyword：NSF, Pin, XCD

There are no changes in any of these cases.

Q 8.31 How many devices can be connected before "PORT15 (ComplianceErr2) Too Many Devices" is detected?

Keyword：NSF, Pin, XCD

Detected when connected to the third or subsequent device, regardless of mode settings.

Q 8.32 It is not possible to access a USB storage device.

Keyword：Fault, Access, USB device, USB storage

The S1R72U16 complies with USB standards, but certain USB storage devices do not comply fully with USB standards.

The following USB storage devices cannot be connected.

- Devices that continuously return NAK
- Devices that return an illegal CSW

Q 8.33 How can I detect insertion/removal of media such as card readers, CDs, or DVDs?

Keyword：Card reader, Media detection

Use GET MEDIA STATUS (in ATA mode), TEST UNIT READY (in ATAPI mode), or media access (read/write) command errors. Notification of media changes is issued only once after media insertion.

The detection methods in ATA mode are shown below. For details, refer to the ATA/ATAPI-6 standard.

- Detection of media removal → insertion
  Detected when error register MC (Media Change) bit (bit 5) becomes 1.
- Detection of media insertion → removal
  Detected when error register NM (No Media) bit (bit 1) becomes 1.
  The detection methods in ATAPI mode are as shown below. For details, refer to the MMC-5 standard.
- Detection of media removal → insertion
  Detected when error data (obtained via REQUEST SENSE command) becomes SenseKey = 06h and ASC = 28h.
- Detection of media insertion → removal
  Detected when error data (obtained via REQUEST SENSE command) becomes SenseKey = 02h and ASC = 3Ah.

The status is confirmed as shown below.

In ATA mode:

(1) Issue GET MEDIA STATUS command periodically.

1. If ended normally: Media insertion status
2. If ended with error

Error register NM bit (bit 1) = 1: No media

Error register MC bit (bit 5) = 1: Media change

(2) Issue a media access (read/write) command and check the error register value.

The error register details are the same as for (1) GET MEDIA STATUS command.

In ATAPI mode:

(1) Issue TEST UNIT READY command periodically.

1. If ended normally: Media insertion status
2. If ended with error: Check using error data (obtained via REQUEST SENSE command).

For details, refer to “10.2.5.2 ATAPI Mode Checking Method” in the S1R72U16 Application Note.

(2) Issue a media access (read/write) command and check using the error data (obtained via REQUEST SENSE command).

The error data details are the same as for (1) TEST UNIT READY command.

Q 8.34 What methods support USB storage device connection and disconnection?

Keyword：Mount/unmount, Application, File system, Connection/disconnection

This requires a file system that supports removable drives (e.g. mount/unmount architecture). Connection and disconnection are generally handled using mount/unmount processing.

9. Evaluation

Q 9.1 Is an evaluation board available?

Keyword：Evaluation, Board, Circuit board, Bridge

Yes. An evaluation board is available for the IDE device - USB bridge. The S1R72U16 Evaluation Board Manual is also provided with the board. Please contact Seiko Epson Sales to obtain this evaluation board.

Q 9.2 What are the actual transfer rates?

Keyword：Transfer rate

Transfer rates of up to 31 MB/s (248 Mbps) have been confirmed in tests done by Seiko Epson.

<Test conditions>
IDE host: PC IDE port
Benchmark software: HDBENCH

Since transfer rates depend on the IDE host (PC) and USB storage device used, these values cannot be guaranteed for the user's specific configuration.

Q 9.3 The crystal oscillator does not oscillate even after the power supply is turned on.

Keyword：Crystal, Oscillator, Resonator, Oscillation

Check the following:

- Are the power supplies providing the specified voltage?
- Has a reset (XRESET) been asserted?
- Does the crystal oscillator circuit have the correct circuit constants?

Q 9.4 PLL_Locked is not asserted even after the power supply is turned on.

Keyword：Crystal, Oscillator, Resonator, Oscillation, PLL

Check the following:

- Is the crystal oscillator oscillating?
- Are the power supplies providing the specified voltage?
- Has a reset (XRESET) been asserted?
- Does the crystal oscillator circuit have the correct circuit constants?

Q 9.5 Are there any figures for transfer rates for CPU bus connections?

Keyword：Transfer rate, Transfer speed, CPU bus, Memory bus

No figures area available for transfer rates. Actual transfer rates will depend on the user's system configuration, including access to devices other than the LSI (e.g., ROM/RAM).

The theoretical maximum value is 16.6 Mbytes/s, as the AC specifications are the same as for the IDE bus PIO.

No measurement data is available, but the actual transfer rate should be less than half, even under ideal conditions.

Q 9.6 Can the LSI be used connected to a PC IDE port?

Keyword：PC, IDE

This LSI uses a 3.3 V I/F. It can be connected provided the PC I/F voltage is 3.3 V. Note that most desktop PCs have a 5 V I/F; check the voltage before connecting the LSI.

Use the following settings when connecting to a PC.

- IDE mode: CPUxIDE pin = “0”
- ATAPI mode: ATAxATAPI pin = “0”
- Single device mode: 2x1 pin = “0”

Also, set CSEL_T pin according to whether the device is used as Master (CSEL_T pin = “0”) or as Slave (CSEL_T pin = “1”).

Q 9.7 Operation is not as expected. Is there an archive of past questions and problems?

Keyword：Past cases, Case studies

Details of past problems are available. Please check whether the problem in this case corresponds to any particular past problem.

(→ Details of past problems)

Q 9.8 What's the procedure for confirming whether the ATA register is accessed correctly when checking connections between the Main CPU and U16?

Keyword：ATA, Register, Access, Default

Read the following default values to check access to the ATA register.

	In ATA mode	In ATAPI mode
Sector Count	01h	01h
LBA Low	01h	01h
LBA Mid	00h	14h
LBA High	00h	EBh
Device	00h	00h
Status	50h	00h

Q 9.9 It is not possible to access a USB storage device.

Keyword：Fault, Access, USB device, USB storage

The S1R72U16 complies with USB standards, but certain USB storage devices do not comply fully with USB standards.

The following USB storage devices cannot be connected.

- Devices that continuously return NAK
- Devices that return an illegal CSW

10. Driver

Q 10.1 How do I obtain the IDE driver?

Keyword：IDE, ATA/ATAPI, Driver

Please contact the retailer from whom you purchased the file system.

Seiko Epson provides sample code with settings for CPU bus connections. The code can be downloaded on web site.

Q 10.2 Can vendor commands be issued to storage devices?

Keyword：ATA, IDE, Vendor, Command, Unsupported

This LSI treats unsupported commands as vendor commands and issues them to the storage devices.

This means unique control is possible using vendor commands, except for data transfer.

For detailed information, refer to “Processing Unsupported Commands” in the S1R72U16 Technical Manual.

Q 10.3 What happens when unsupported commands are issued?

Keyword：ATA, IDE, Vendor, Command, Unsupported

This LSI treats unsupported commands as vendor commands and issues them to the storage devices.

This means unique control is possible using vendor commands, except for data transfer.

For detailed information, refer to “Processing Unsupported Commands” in the S1R72U16 Technical Manual.

Q 10.4 What happens if a command is issued when no storage device is connected?

Keyword：ATA, IDE, Command, Status

An error status will be returned for commands such as Read or Write attempting to access a storage device. A normal status will be returned for all other commands, which are processed within the LSI.

For detailed information, refer to “Supported Command List” in the S1R72U16 Technical Manual.

Q 10.5 How does IDE implement support for USB storage device connections/ disconnections?

Keyword：Connection, Disconnection, Connection/Disconnection, Removable, Driver

This LSI includes pins for informing the system of the USB storage device connection status.

Use these pins together with connection/disconnection processing in the application.

Support can also be implemented without using these pins by using a driver supporting ATA/ATAPI removable devices.

Q 10.6 What constraints or precautions are associated with the main system file system?

Keyword：Constraint, File system

No particular constraints apply. (The LSI will return an error if a write/read attempt is made while the USB device is disconnected.)

Q 10.7 Is the driver source code endian-dependent?

Keyword：Sample, Driver, Endian, Source, Code

Yes. It assumes little-endian.

Q 10.8 Does the S1R72U16 ever negate DMARQ before the specified transfer has been completed? If so, when does this occur?

Keyword：IDE, DMARQ, DMA transfer, Terminate

DMARQ is negated in either of the following conditions.

1. If the IDE host performs a host terminate
2. If the IDE host exceeds 8 Mbytes (800000h) in the Read direction (LSI to Main CPU)

DMARQ is negated for each 8 Mbyte transfer if a data transfer is requested.

Ex: If the Main CPU issues a READ command for 24 Mbytes, the LSI divides the 24 Mbytes of data into three.

DMARQ is therefore negated twice during UltraDMA transfer.

For conditions other than those described above, the DMARQ signal is not negated before the specified transfer is completed.

In the case of WRITE, only condition 1 above applies for negating the DMARQ signal, since the LSI usage restrictions limit the maximum size of data that can be requested to 8 Mbytes.

Q 10.9 Does the S1R72U16 ever negate DMARQ if the USB bus is defective, resulting in repeated packet errors?

Keyword：IDE, DMARQ, DMA transfer, Packet error, Transfer error

DMARQ is not negated even if packet errors occur during DMARQ assertion.

DMARQ will be treated as follows depending on the timing of the NAK returned continuously by the READ command.

1. If NAK is returned continuously for CBW command issue

DMARQ is not asserted and the LSI does not start UltraDMA transfer.

The status register will be BSY=1 and DRQ=0.

2. If NAK is returned continuously for the first BulkIN transfer after CBW issue

Same as for 1.

3. If NAK is returned continuously after ACK has been returned at least once for first BulkIN transfer

DMARQ is asserted and UltraDMA transfer is not completed.

The status register will be BSY=0 and DRQ=1.

4. If NAK is returned repeatedly for the CSW (status) issued

The UltraDMA transfer will end, but the Status register will show BSY=1, DRQ=0.

The same applies for the WRITE command also.

Q 10.10 Are ATA/ATAPI commands used to control the S1R72U16? Which commands should be used?

Keyword：IDE, ATA, ATAPI, Command

Yes. ATA/ATAPI commands are used.

Use ATAPI commands if a CD or DVD drive is connected.

Either may be used with a USB memory or HDD connected. Select the command to suit the driver included with the file system or main CPU used.

Q 10.11 How are ATA/ATAPI commands processed? Is there any information available describing the basic details?

Keyword：IDE, ATA, ATAPI, Command

The basic arrangement consists of issuing a command, reading/writing data, and setting operating settings.

Consult published general instruction manuals, which provide more specific information. Also refer to the Epson Sample Driver reference.

Q 10.12 Is there a way to determine whether a download was successful for the DOWNLOAD MICROCODE command or to determine whether correct or corrupted Update data was loaded?

Keyword：Download, ATA, Command, Update

The status value can be used to check whether a command was successfully completed.

An error status is returned if the download fails.

The Update data includes a CRC value. The validity of the data is compared against the calculated CRC value. An error status is returned if the CRC values fail to match.

Q 10.13 Operation is not as expected. Is there an archive of past questions and problems?

Keyword：Past cases, Case studies

Details of past problems are available. Please check whether the problem in this case corresponds to any particular past problem.

(→ Details of past problems)

Q 10.14 Is the VBUS supply stopped (VBUS_EN = OFF) when the Sleep command is issued?

Keyword：Sleep, Suspend, VBUS

This depends on whether a USB storage device is connected.

- If the device is connected:
  VBUS supply is not stopped and only suspended.
- If the device is not connected:
  VBUS supply is stopped.

Q 10.15 The sample source does not operate with the S1R72U16xxxE200 when used unmodified.

Keyword：Sample source, E100, E200

When using the S1R72U16xxxE200, delete the include statement in U16_Update.h defined in U16_SampleDriverII U16_Command.c.

The sample source describes downloading UpdateData.

Q 10.16 How can I detect insertion/removal of media such as card readers, CDs, or DVDs?

Keyword：Card reader, Media detection

Use GET MEDIA STATUS (in ATA mode), TEST UNIT READY (in ATAPI mode), or media access (read/write) command errors. Notification of media changes is issued only once after media insertion.

The detection methods in ATA mode are shown below. For details, refer to the ATA/ATAPI-6 standard.

- Detection of media removal → insertion
  Detected when error register MC (Media Change) bit (bit 5) becomes 1.
- Detection of media insertion → removal
  Detected when error register NM (No Media) bit (bit 1) becomes 1.
  The detection methods in ATAPI mode are as shown below. For details, refer to the MMC-5 standard.
- Detection of media removal → insertion
  Detected when error data (obtained via REQUEST SENSE command) becomes SenseKey = 06h and ASC = 28h.
- Detection of media insertion → removal
  Detected when error data (obtained via REQUEST SENSE command) becomes SenseKey = 02h and ASC = 3Ah.

The status is confirmed as shown below.

In ATA mode:

(1) Issue GET MEDIA STATUS command periodically.

1. If ended normally: Media insertion status
2. If ended with error

Error register NM bit (bit 1) = 1: No media

Error register MC bit (bit 5) = 1: Media change

(2) Issue a media access (read/write) command and check the error register value.

The error register details are the same as for (1) GET MEDIA STATUS command.

In ATAPI mode:

(1) Issue TEST UNIT READY command periodically.

1. If ended normally: Media insertion status
2. If ended with error: Check using error data (obtained via REQUEST SENSE command).

For details, refer to “10.2.5.2 ATAPI Mode Checking Method” in the S1R72U16 Application Note.

(2) Issue a media access (read/write) command and check using the error data (obtained via REQUEST SENSE command).

The error data details are the same as for (1) TEST UNIT READY command.

Q 10.17 What methods support USB storage device connection and disconnection?

Keyword：Mount/unmount, Application, File system, Connection/disconnection

This requires a file system that supports removable drives (e.g. mount/unmount architecture). Connection and disconnection are generally handled using mount/unmount processing.

Appendix

A. Power on/off timing

1. Power supply on/off timing (for LVDD⇒ HVDD / HVDD ⇒LVDD recommended parameters)

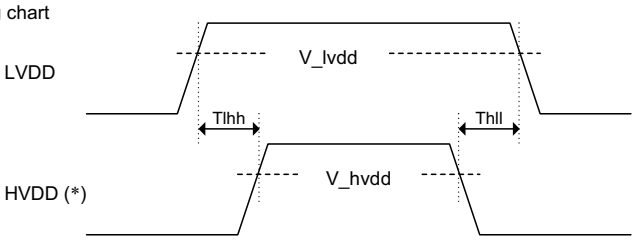
Timing parameters

Item	Code	min	typ	max	Units
HVDD power on timing	Tlhh	0	-	10	sec
HVDD power off timing	Thll	0	-	10	sec

Voltage parameters

Item	Code	Voltage parameters		Units
		At power on	At power off	
LVDD start voltage	V_lvdd	LVDD_min	LVDD_min	V
HVDD start voltage	V_hvdd	HVDD_min	HVDD_min	V

Timing chart



2. Power supply on/off timing (for HVDD⇒LVDD / LVDD ⇒ HVDD)

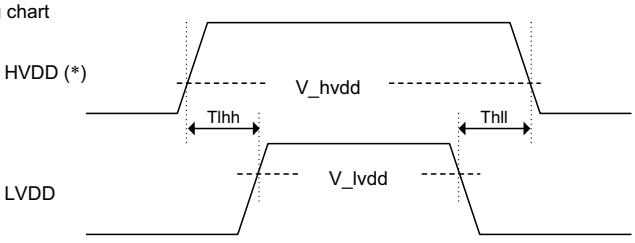
Timing parameters

Item	Code	min	typ	max	Units
LVDD power on timing	Tlhh	0	-	1	sec
LVDD power off timing	Thll	0	-	1	sec

Voltage parameters

Item	Code	Voltage parameters		Units
		At power on	At power off	
LVDD start voltage	V_lvdd	LVDD_min	LVDD_min	V
HVDD start voltage	V_hvdd	0.1	0.1	V

Timing chart



*: HVDD refers to USB HVDD and interface IOVDD.

*: For LVDD⇒HVDD timing for both power on and off, refer to paragraph 1 for power on and paragraph 2 for power off.

Similarly, for HVDD⇒LVDD timing for both power on and off, refer to paragraph 2 for power on and paragraph 1 for power off.

B. Details of past problems

Mode	Fault	Cause	Check points
CPU mode	Data transfer is not completed.	Insufficient address/XCS hold time.	Check AC characteristics.
	Unable to access register.	XDACK signal was “0.”	Connect to negative-logic signal when using XDACK signal. Pull up if not using XDACK signal.
		CSEL_T pin setting failed to match DEVICE/HEAD register DEV bit setting.	Check ATA/ATAPI standard.
	Operation stops with STATUS register at BSY or DRQ.	A new command was issued while a command was being executed.	Check control method.
	The data is corrupted.	CPU XDREQ signal sampling point did not satisfy AC characteristics.	Check AC characteristics.
	XDREQ signal is asserted before data transfer started.	Was set to IDE mode.	Check pin settings against the settings shown in the *S1R72U16 Data Sheet* and *S1R72U16 Technical Manual*.
IDE mode	The data is corrupted.	UDMA not supported by Main CPU hardware was executed by software.	Check control method.
General	Operation is unstable.	Power supply was fluctuating.	Use an oscilloscope to check the stability of the power supply. Check whether an appropriate bypass capacitor is used in accordance with *S1R72U16 PCB Design Guide* and *S1R72U16 EVA Board Manual*.
		VBUS has insufficient supply capacity.	Check operations by applying a VBUS feed from a stabilized power supply. Check operations using a self-powered USB device.
		The USB transmission path design was inadequate, and a problem occurred in the USB analog waveform.	Check the board design in accordance with *S1R72U16 EVA Board Manual*.
		Noise was present in the interface with the Main CPU.	Use an oscilloscope to check the interface with the Main CPU.
	The data is corrupted.	Certain sectors on the USB device were defective.	Measures are required in Main CPU software to avoid defective sectors.
	BSY status persists even after HRST.	USB device returned an NAK response.	Remove the USB device or apply chip reset.
	Storage device cannot be accessed in ATA mode (ATA x ATAPI = “1”).	USB device sector size was not 512 bytes (was 2,047 bytes).	Try using a different USB device or repeat the action in ATAPI mode.

C. Unused pin treatment

Function	Pin name	Method when unused
TEST	TSTEN	Refer to “Pin Functions” in *S1R72U16 Data Sheet*.
	ATPGEN	
	BURNIN	
DEBUG I/F	DBGDCLK	Refer to “Pin Functions” in *S1R72U16 Data Sheet*.
	DBGDT	
	DBGST	
USB	VBUSFLG	Open or pull up.
	VBUSEN	Open.
Serial I/F	SCLK0	Refer to “Pin Functions” in *S1R72U16 Data Sheet*.
	SIN0	Open or pull up.
	SOUT0	Open.
GPIO	PORT10 (XChgInt)	Open.
	PORT11 (XCD0)	
	PORT12 (XCD1)	
	PORT13 (PLL_Locked)	
	PORT14 (ComplianceErr0)	
	PORT15 (ComplianceErr1)	
	PORT16 (ComplianceErr2)	
	PORT17 (ComplianceErr3)	
<In IDE mode> IDE Device I/F	HDMARQ_T	Open.
	XHDMACK_T	Pull up.
	HIORDY_T	Open.
	HINTRQ_T	
	XHRESET	Pull up.
	XHADSP_T	
	XHPDIAG_T	
<In CPU mode> CPU Memory Bus I/F (Pin name in IDE mode)	XDREQ (HDMARQ_T)	Open.
	XDACK (XHDMACK_T)	Pull up.
	- (HIORDY_T)	Refer to “Pin Functions” in *S1R72U16 Data Sheet*.
	XINT (HINTRQ_T)	Open.
	XHRESET (XHRESET)	Pull up.
	- (XHADSP_T)	Refer to “Pin Functions” in *S1R72U16 Data Sheet*.
	- (XHPDIAG_T)	

Document Code：411136905
First Issue June 2007
Revised September 2009